

Automotive N-Channel 40 V (D-S) 175 °C MOSFET



RoHS
COMPLIANT
HALOGEN
FREE

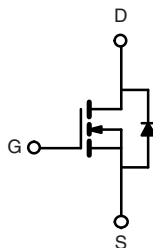
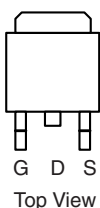
PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0017
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0020
I_D (A)	120
Configuration	Single

FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested
- AEC-Q101 Qualified^d
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?999912

TO-263



N-Channel MOSFET

ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and Halogen-free	SQM120N04-1m7L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25$ °C	120	A
	$T_C = 125$ °C	120	
Continuous Source Current (Diode Conduction) ^a	I_S	120	
Pulsed Drain Current ^b	I_{DM}	480	
Single Pulse Avalanche Current	I_{AS}	92	mJ
Single Pulse Avalanche Energy	E_{AS}	423	
Maximum Power Dissipation ^b	$T_C = 25$ °C	375	W
	$T_C = 125$ °C	125	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.4	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2.0	2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	150	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	5	mA
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	120	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A	-	0.0014	0.0017	Ω
		V _{GS} = 10 V	I _D = 30 A, T _J = 125 °C	-	-	0.0028	
		V _{GS} = 10 V	I _D = 30 A, T _J = 175 °C	-	-	0.0034	
		V _{GS} = 4.5 V	I _D = 20 A	-	0.0015	0.0020	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 30 A		-	212	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	-	11 685	14 606	pF
Output Capacitance	C _{oss}			-	1652	2065	
Reverse Transfer Capacitance	C _{rss}			-	726	908	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 20 A	-	190	285	nC
Gate-Source Charge ^c	Q _{gs}			-	29	-	
Gate-Drain Charge ^c	Q _{gd}			-	27	-	
Gate Resistance	R _g	f = 1 MHz		0.5	1.07	1.7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 1 Ω I _D ≅ 20 A, V _{GEN} = 10 V, R _g = 1 Ω		-	15	23	ns
Rise Time ^c	t _r			-	10	15	
Turn-Off Delay Time ^c	t _{d(off)}			-	74	110	
Fall Time ^c	t _f			-	12	18	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	480	A
Forward Voltage	V _{SD}	I _F = 60 A, V _{GS} = 0 V		-	0.8	1.5	V

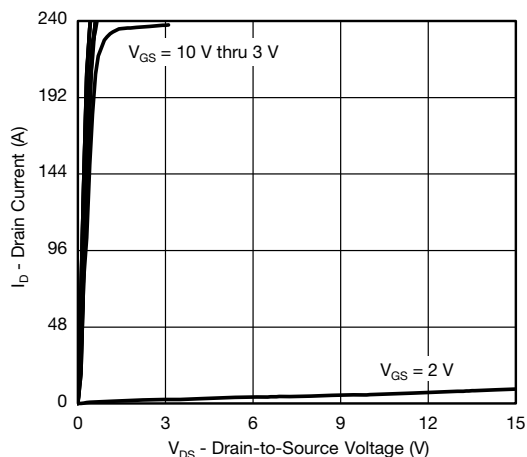
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

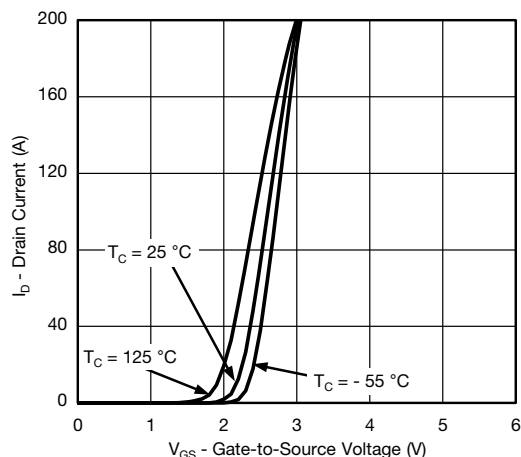
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



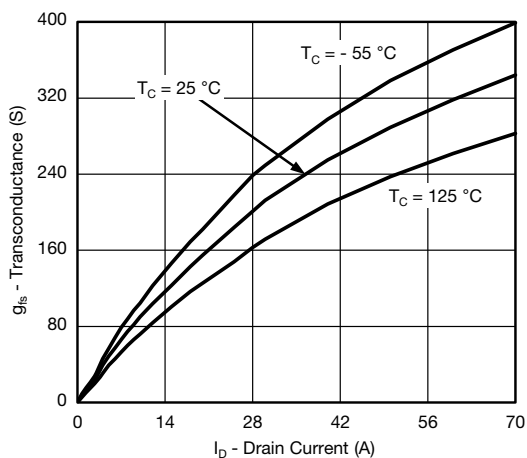
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



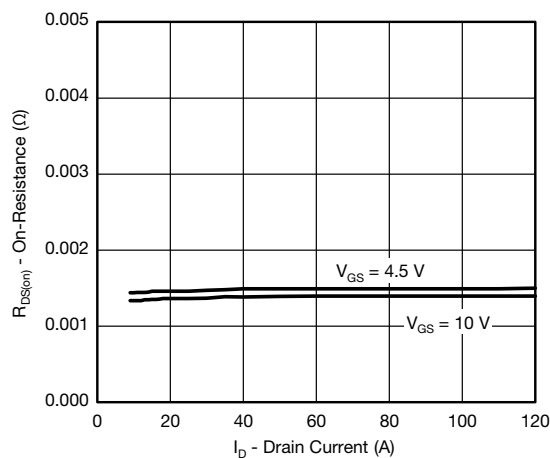
Output Characteristics



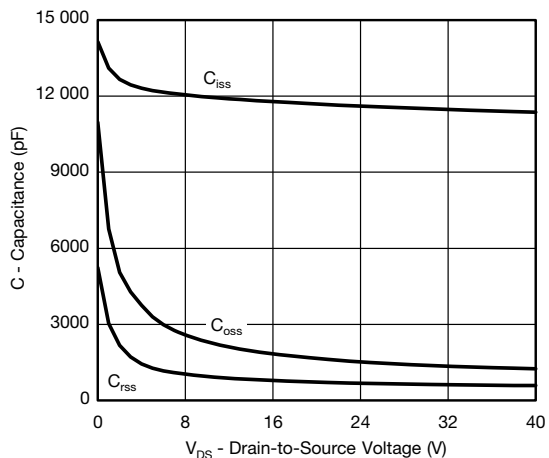
Transfer Characteristics



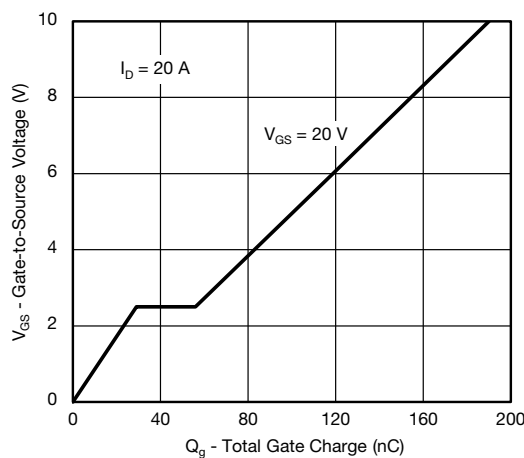
Transconductance



On-Resistance vs. Drain Current



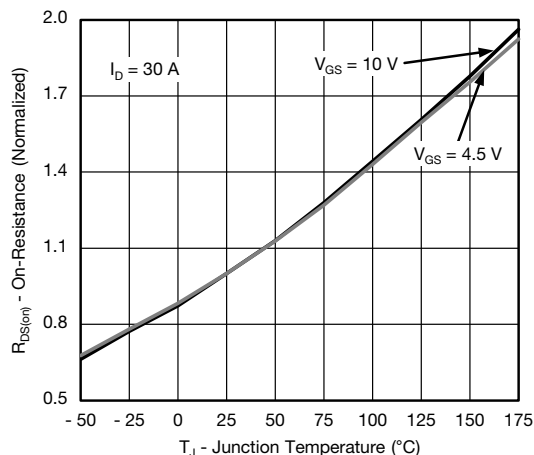
Capacitance



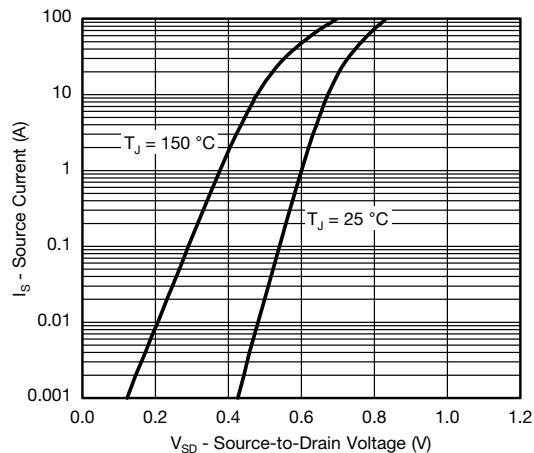
Gate Charge



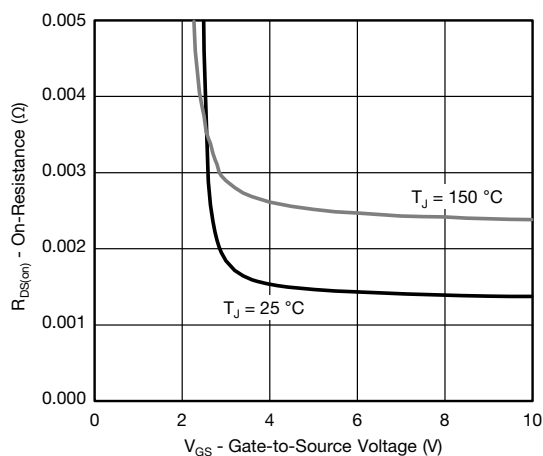
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



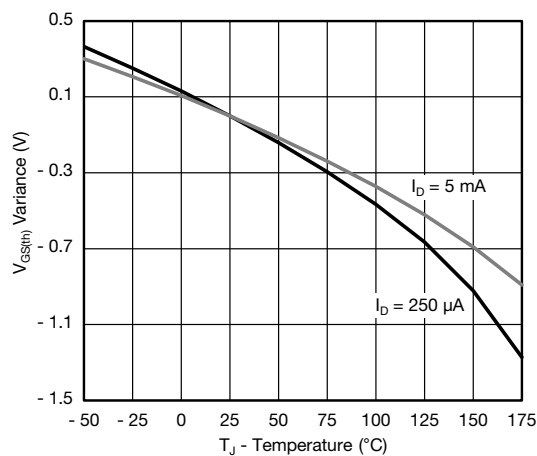
On-Resistance vs. Junction Temperature



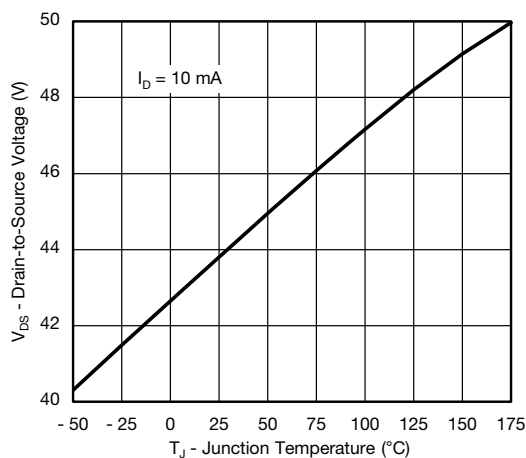
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



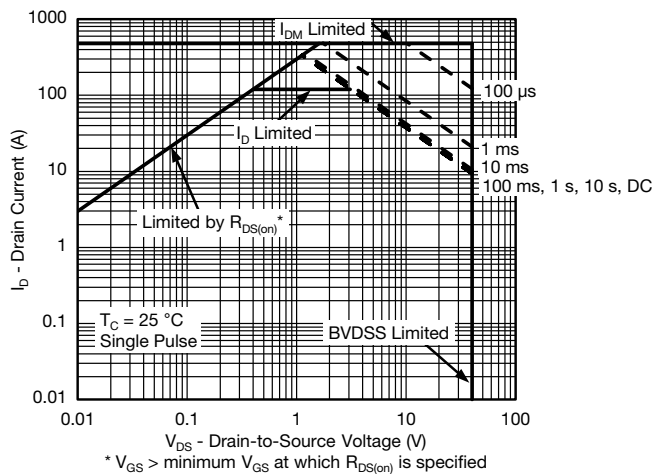
Threshold Voltage



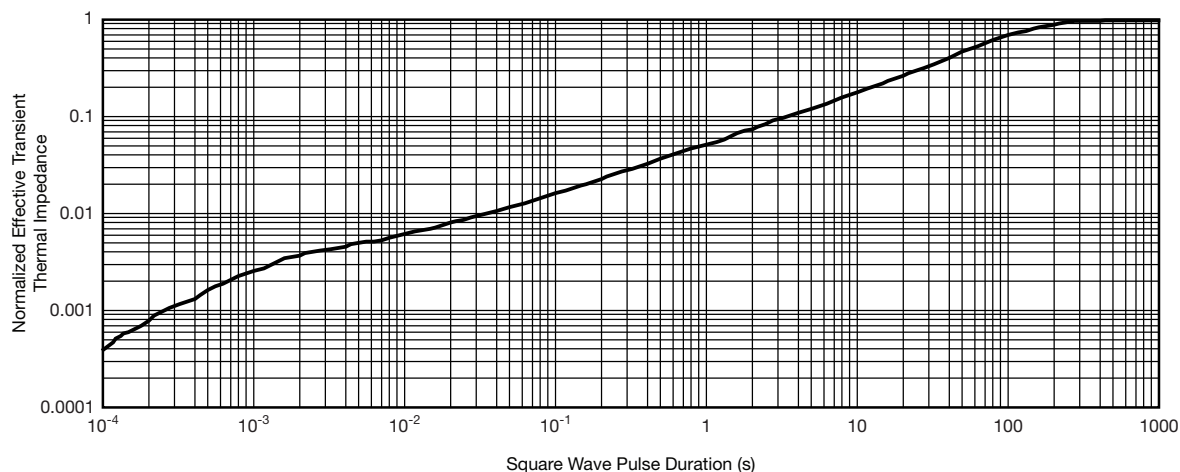
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



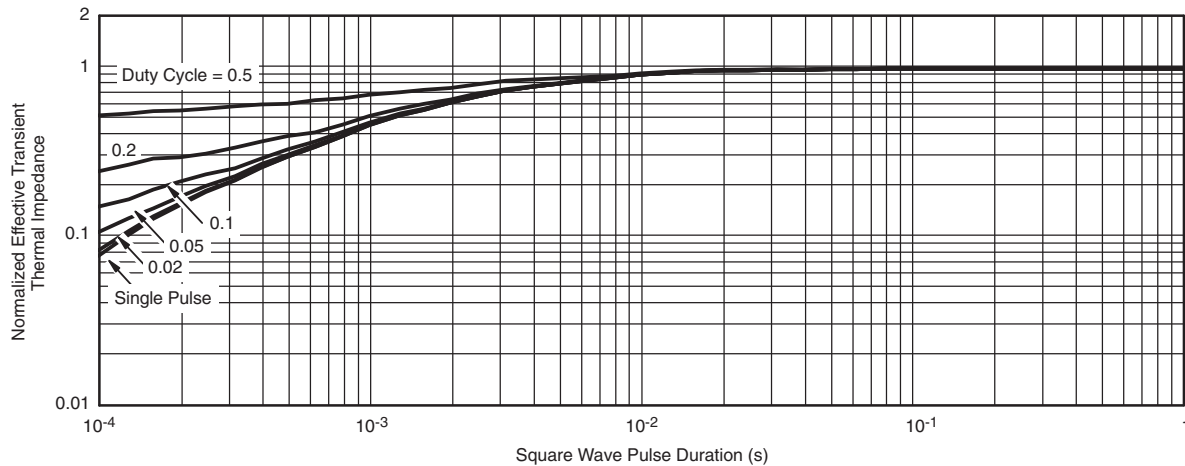
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

V

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65729.

TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)



SECTION A-A

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

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DWG: 5843

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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