



## 0.37 $\Omega$ , Low Capacitance, Dual DPDT / Quad SPDT Analog Switch

### DESCRIPTION

The DG2788A, is a four-channel single-pole double-throw (SPDT) analog switch with two control inputs. It is also known as a two-channel double-pole double-throw (DPDT) configuration. The part is designed to operate from 1.8 V to 5.5 V single power rail. All switches conduct equally well in both directions, offering rail to rail signal switching and can be used both as multiplexers as well as de-multiplexers.

The DG2788A offers low parasitic capacitance and highly matched low and flat switch resistance over the full signal range. It features break-before-make switching and low control logic threshold. The part supports rail to rail fast edge pulsing signals and have 0.1 ns/typ. propagation delay. It is ideal for both analog and digital signal switching in space constrain applications requiring high performance and efficient use of board space.

The DG2788A comes in a small miniQFN-16 lead package of 2.6 mm x 1.8 mm x 0.55 mm.

### FEATURES

- 1.8 V to 5.5 V single supply operation
- Low resistance: 0.37  $\Omega$ /typ. at 2.7 V
- Highly flat and matched  $R_{ON}$
- Low parasitic capacitance,  $C_{ON} = 26$  pF,  $C_{OFF} = 14.5$  pF
- High bandwidth: 338 MHz
- 0.1 ns/typ. propagation delay for rail to rail fast edge pulsing signal
- Guaranteed logic high 1.2 V, logic low 0.3 V
- Break before make switching
- Signal swing over  $V_+$  capable
- Power down protection
- Latch up current: 300 mA (JESD78)
- ESD / HBM: > 2 kV
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

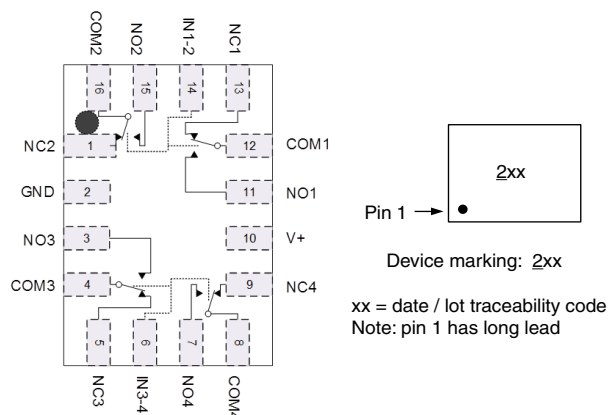
### BENEFITS

- Low and flat resistance
- Excellent total harmonic distortion
- Low parasitic capacitance
- Low voltage control interface

### APPLICATIONS

- Analog and digital signal switching
- SMA optical image stabilization
- Relay replacement
- Portable instrumentation
- Smart phones and tablets
- Modems and peripherals
- Data storage

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



### TRUTH TABLE

LOGIC	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	On	Off
1	Off	On

**ORDERING INFORMATION**

TEMPERATURE RANGE	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY
-40 °C to +85 °C lead (Pb)-free	miniQFN-16	DG2788ADN-T1-GE4	Tape and reel, 3000 units

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Reference to GND	V+	-0.3 to +6	V
	IN, COM, NC, NO <sup>a</sup>	-0.3 to (V+ + 0.3)	
Current (any terminal except NO, NC, or COM)		30	mA
Continuous current (NO, NC, or COM)		± 300	
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage temperature (D suffix)		-65 to +150	°C
Package solder reflow conditions <sup>d</sup>	miniQFN-16	250	
Power dissipation (packages) <sup>b</sup>	miniQFN-16 <sup>c</sup>	525	mW

**Notes**

- Signals on NC, NO, or COM, or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings
- All leads welded or soldered to PC board
- Derate 6.6 mW/°C above 70 °C
- Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS unless otherwise specified V+ = 3 V, ± 10 %, VIN = 0.5 or 1.4 V e	TEMP. a	LIMITS -40 °C to +85 °C			UNIT
				MIN. b	TYP. c	MAX. b	
Analog Switch							
Analog signal range d	VNO, VNC, VCOM		Full	0	-	V+	V
On-resistance	RON	V+ = 2.7 V, VCOM = 0 to 2.7 V, INO, INC = 100 mA	Room	-	0.37	0.5	Ω
			Full	-	-	0.6	
RON flatness d	RON flatness	V+ = 2.7 V, VCOM = 0 to V+, INO, INC = 100 mA	Room	-	0.01	0.05	
RON match d	ΔRON		Room	-	0.05	-	
Switch off leakage current	INO(off), INC(off)	V+ = 5.5 V, VNO, VNC = 0.5 V / 4 V, VCOM = 4 V / 0.5 V	Room	-0.1	-	0.1	μA
			Full	-0.5	-	0.5	
	ICOM(off)		Room	-1.2	-	1.2	
			Full	-2	-	2	
Channel-on leakage current	ICOM(on)	V+ = 5.5 V, VNO, VNC = VCOM = 0.5 V / 4 V	Room	-1.2	-	1.2	
			Full	-2	-	2	
Digital Control							
Input high voltage	VINH		Full	1.2	-	-	V
Input low voltage	VINL		Full	-	-	0.3	
Input capacitance	CIN		Full	-	5	-	pF
Input current	IINL or IINH	VIN = 0 or V+	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time	tON	VNO or VNC = 1.5 V, RL = 50 Ω, CL = 35 pF	Room	-	30	50	μs
			Full	-	-	150	
Turn-off time	tOFF		Room	-	0.35	1	
			Full	-	-	3	
Break-before-make time	td		Full	1	-	-	
Charge injection d	QINJ	CL = 1 nF, VGEN = 1.5 V, RGEN = 0 Ω	Room	-	-245	-	pC
-3 dB bandwidth	BW	RL = 50 Ω, CL = 5 pF	Room	-	338	-	MHz
Off-isolation d	OIRR	RL = 50 Ω, CL = 5 pF, f = 100 kHz	Room	-	-82	-	dB
		RL = 50 Ω, CL = 5 pF, f = 1 MHz		-	-56	-	
Crosstalk d, f	XTALK	RL = 50 Ω, CL = 5 pF, f = 100 kHz		-	-87	-	
		RL = 50 Ω, CL = 5 pF, f = 1 MHz		-	-61	-	
Total harmonic distortion and noise	THD+N	RL = 50 Ω, 1 Vp-p, f = 1 kHz	Room	-	-104.1	-	dB
NO, NC off capacitance d	CNO(off)	f = 1 MHz	Room	-	14.5	-	pF
	CNC(off)		Room	-	14.5	-	
Channel-on capacitance d	CNO(on)		Room	-	26	-	
	CNC(on)		Room	-	26	-	
Power Supply							
Power supply range	V+			1.8	-	5.5	V
Power supply current	I+	VIN = 0 or V+	Full	-	24	60	μA

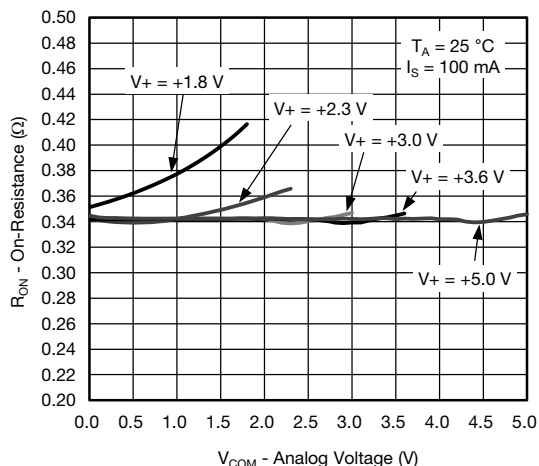
**Notes**

- a. Room = 25 °C, full = as determined by the operating suffix  
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet  
c. Typical values are for design aid only, not guaranteed nor subject to production testing  
d. Guarantee by design, not subjected to production test  
e.  $V_{IN}$  = input voltage to perform proper function  
f. Crosstalk measured between channels

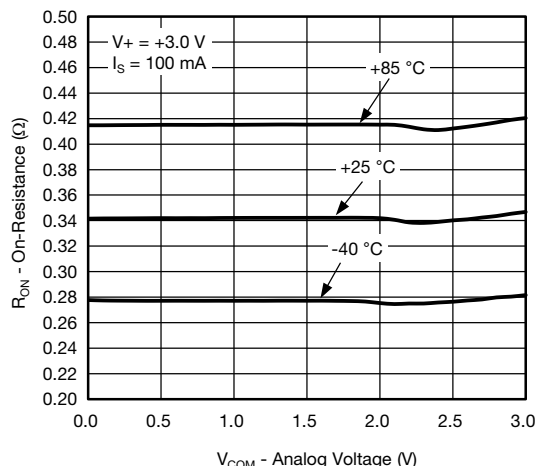
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



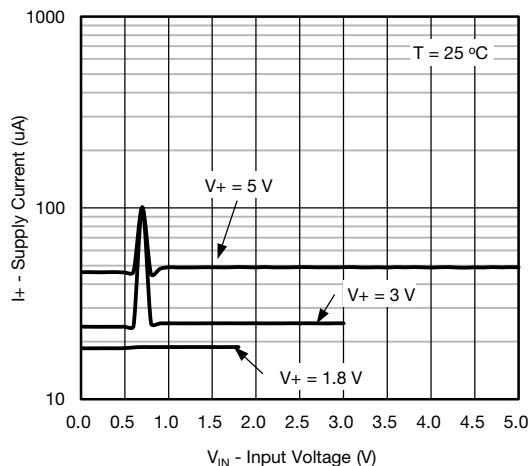
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



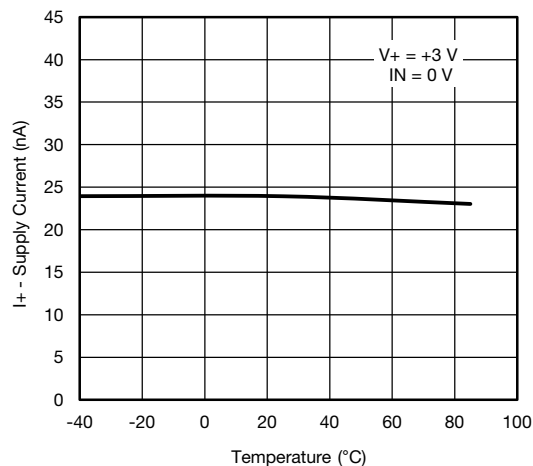
**$R_{ON}$  vs.  $V_{COM}$  and Supply Voltage**



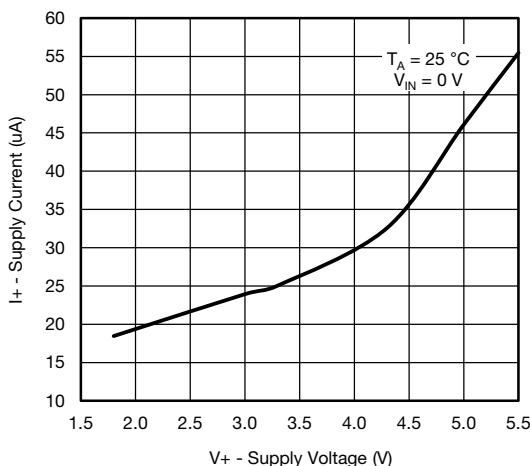
**$R_{ON}$  vs. Analog Voltage and Temperature**



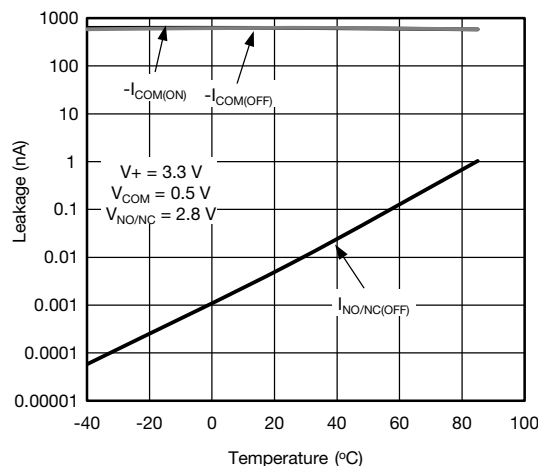
**Supply Current vs. Input Voltage**



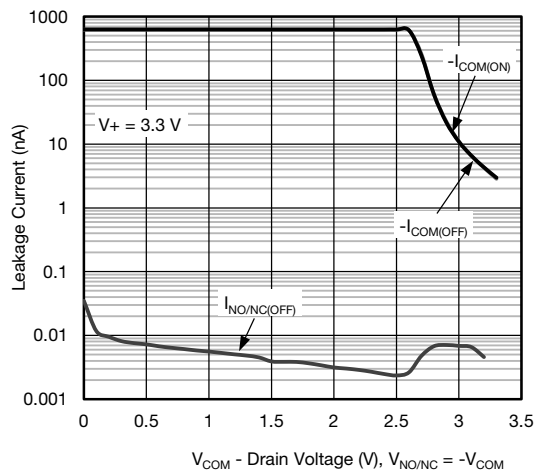
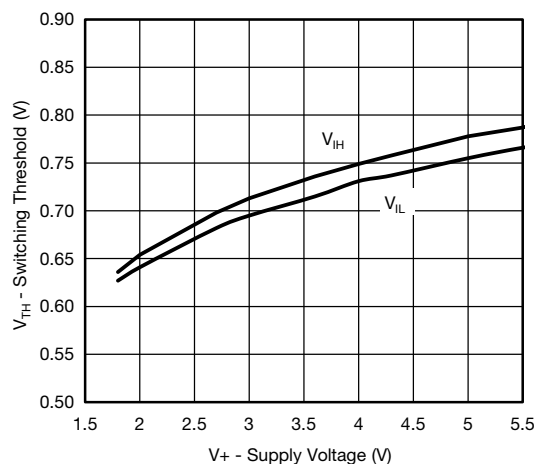
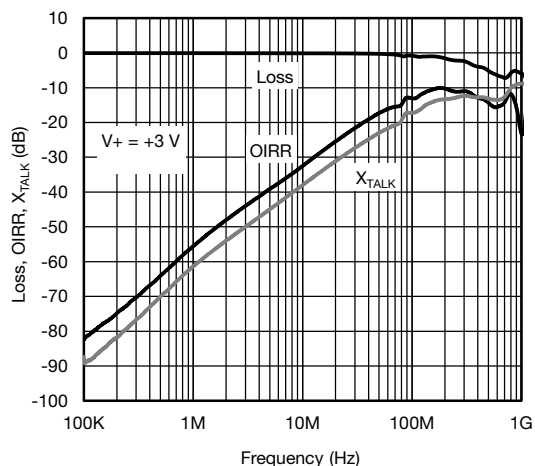
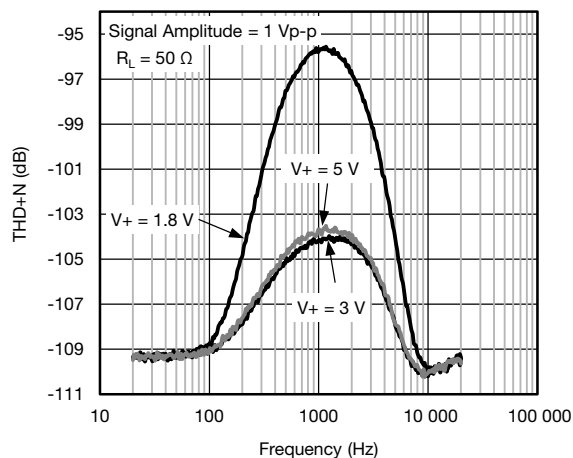
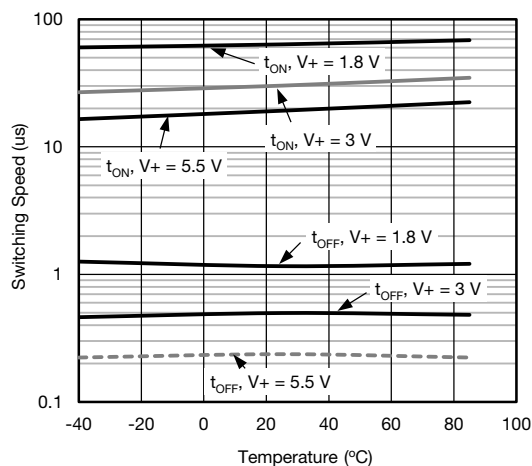
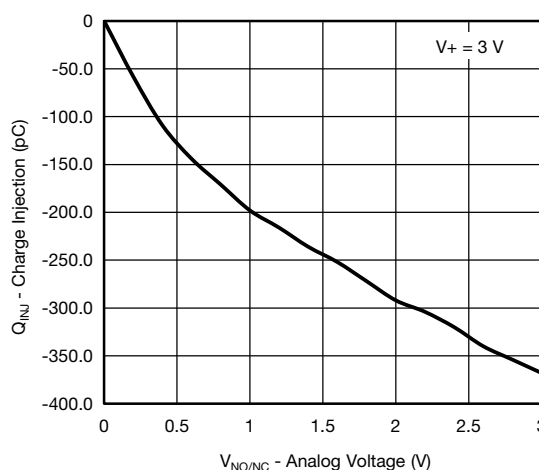
**Supply Current vs. Temperature**

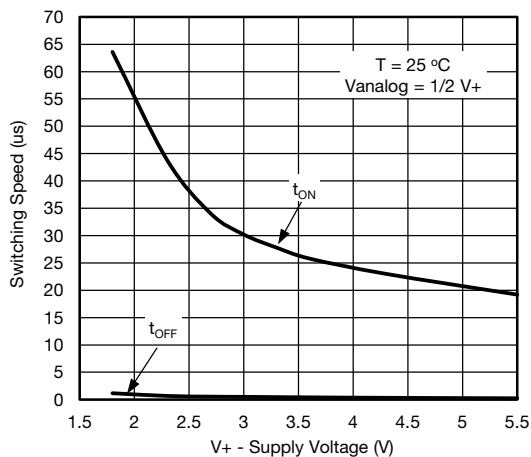
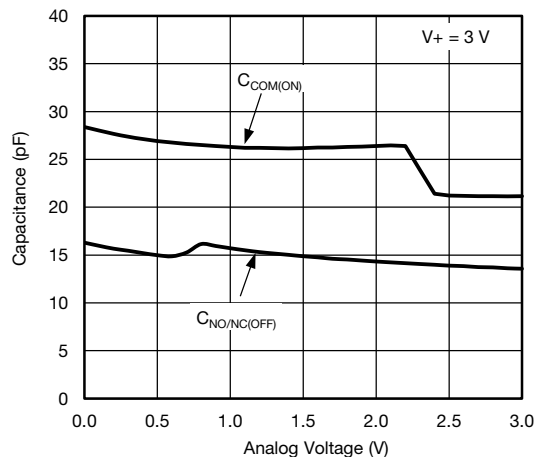
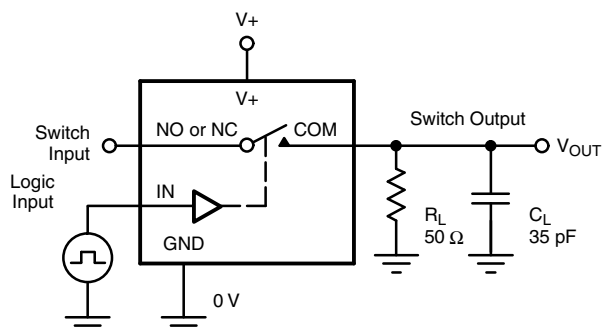


**Supply Current vs. Supply Voltage**

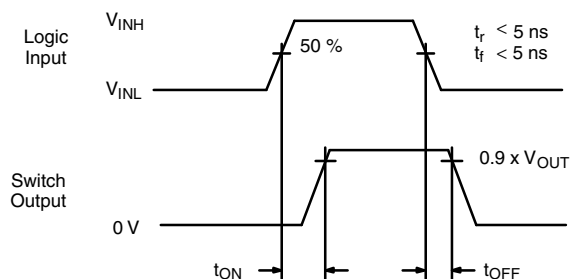


**Leakage Current vs. Temperature**

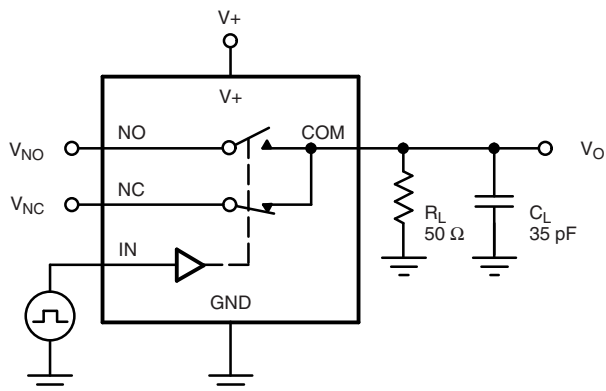
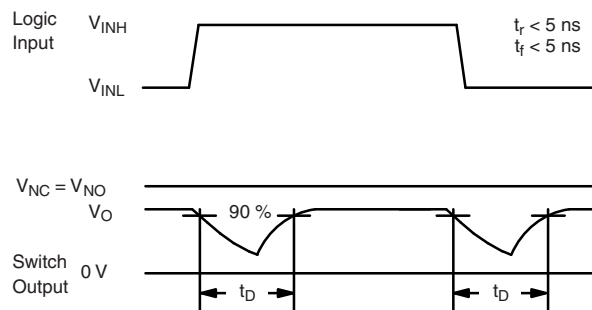
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Leakage Current vs. Drain Voltage**

**Switching Threshold vs. Supply Voltage**

**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

**Total Harmonic Distortion and Noise vs. Frequency**

**Switching Time vs. Temperature**

**Charge Injection vs. Analog Voltage**

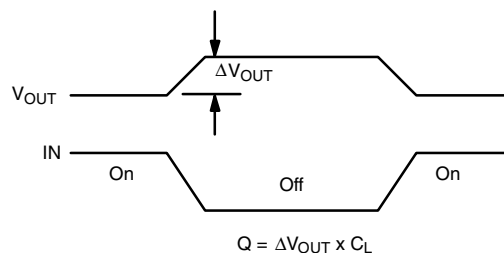
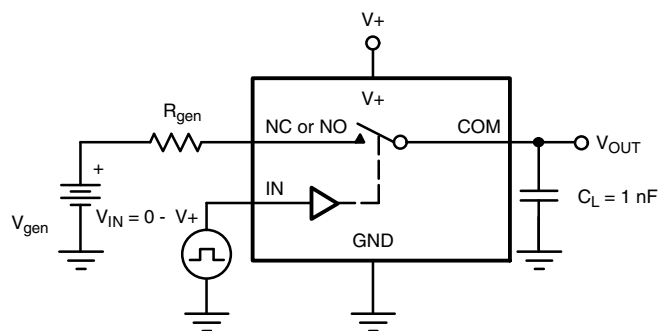
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Switching Time vs. Supply Voltage**

**Capacitance vs. Analog Voltage**
**TEST CIRCUITS**

 $C_L$  (includes fixture and stray capacitance)

$$V_{\text{OUT}} = V_{\text{COM}} \left( \frac{R_L}{R_L + R_{\text{ON}}} \right)$$



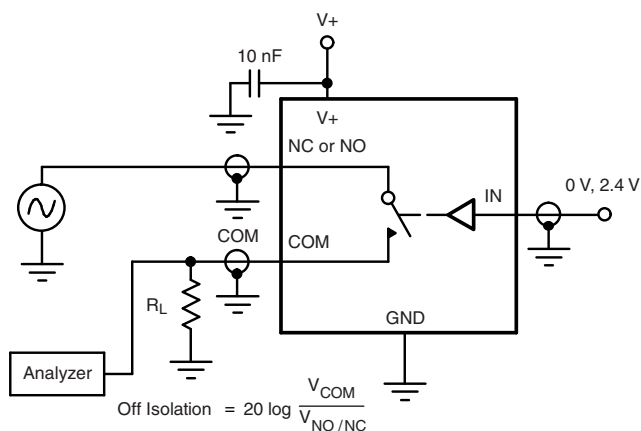
Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

**Fig. 1 - Switching Time**

 $C_L$  (includes fixture and stray capacitance)

**Fig. 2 - Break-Before-Make Interval**

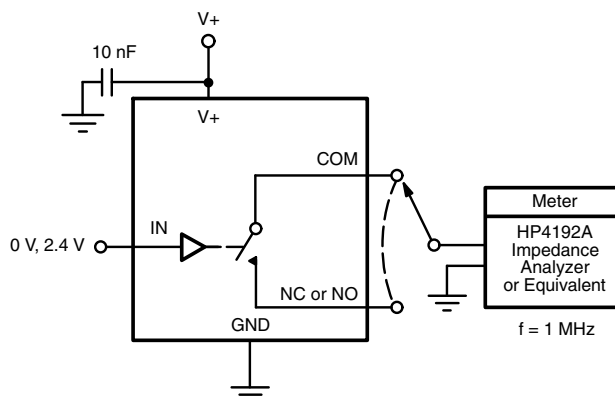


IN depends on switch configuration: input polarity determined by sense of switch.

**Fig. 3 - Charge Injection**



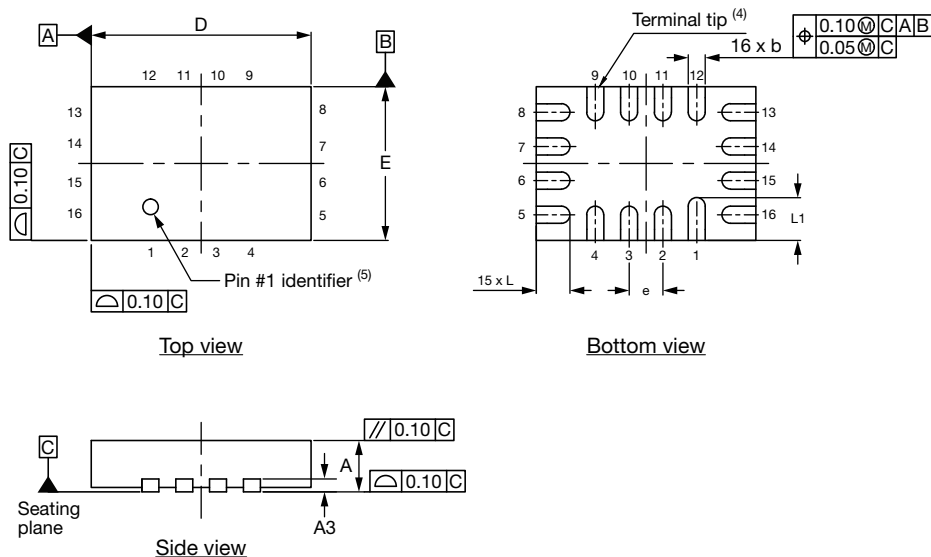
**Fig. 4 - Off-Isolation**



**Fig. 5 - Channel Off / On Capacitance**

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## Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS <sup>(1)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N <sup>(3)</sup>	16			16		
Nd <sup>(3)</sup>	4			4		
Ne <sup>(3)</sup>	4			4		

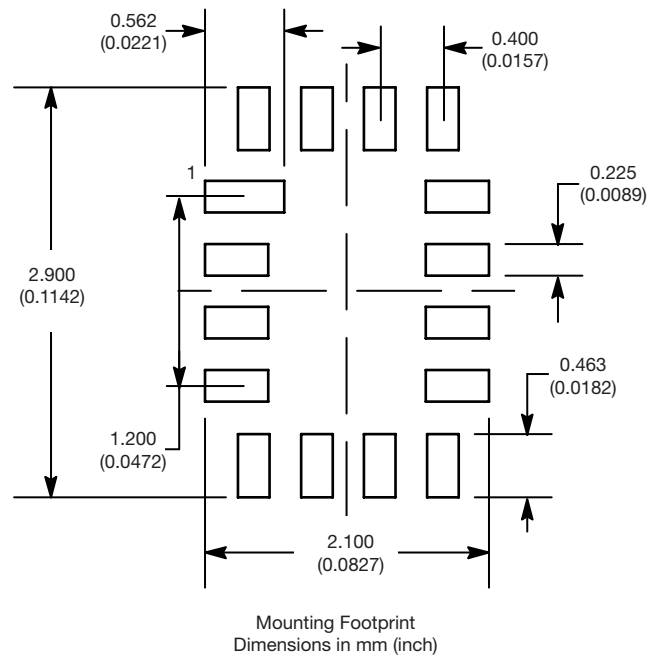
### Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16  
DWG: 6023



## RECOMMENDED MINIMUM PADS FOR MINI QFN 16L





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