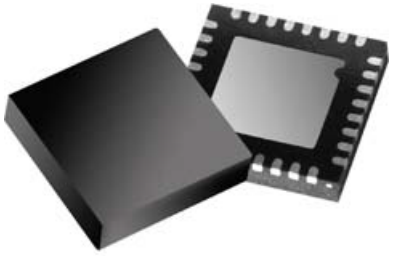
SPSB081

Datasheet

Automotive power management IC with LIN and CAN-FD



QFN32L Epad
(5.0x5.0x1.0 mm)

Product status link
SPSB081

Product summary		
Order code	**Package**	**Packing**
SPSB0815-TR	QFN32L Epad 5.0x50.x1.0 mm	Tape and reel
SPSB0813-TR		
SPSB081C5-TR		
SPSB081C3-TR		

Features

- AEC-Q100 qualified
- One 5 V (or 3.3 V for SPSB0813 and SPSB081C3) low drop voltage regulator (V1) for microcontroller and peripheral supply
- One configurable 5 V or 3.3 V low drop voltage regulator V2 selectable via SPI, tracker for V1
- Minimum current limitation of 450 mA for V1 and 400 mA for V2
- No electrolytic capacitor required on regulator outputs
- Very low quiescent current in standby modes (typ. 15 µA)
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog
- LIN transceivers ISO 17987-4/2016 compliant (only for SPSB0815 and SPSB0813)
- CAN-FD transceiver (ISO 11898-2/2016, SAE J2284 compliant) with local failure and bus failure diagnosis
- Complete 2-channel contact monitoring interface (WU1 and WU2 input pins) with programmable cyclic sense functionality. WU2 also with DIR functionality
- Programmable periodic system wake-up feature
- STM standard serial peripheral interface (32Bit/ST-SPI)
- 4 HS drivers for 0.14 A (R_{ON} = 7 Ω) suitable to drive external LED modules with high input capacitance value or to also supply external contacts
- Internal 10-bit PWM timer for each standalone high-side driver
- Buffered supply for all voltage regulators
- DIAGN output pin for fail-safe signalization
- Current monitor output for all internal high-side drivers
- Open-load diagnosis for all outputs
- Overcurrent protection for all outputs
- V1 overvoltage detection and protection
- Device contains temperature warning and protection
- Thermal cluster
- Limited documentation available for customers that need support when dealing with ASIL requirements as per ISO 26262

Applications

- Body control modules (BCM)
- Gateway applications
- Telematic control unit
- Passive keyless entry and start modules
- Control panel
- Heating, ventilation and air conditioning (HVAC)
- Seat control modules
- Sunroof modules

- Tailgate modules
- Door modules
- Light control modules
- Gear shifters
- Steering column
- Fuel pump

Description

The SPSB081 is a power management system IC providing electronic control modules with enhanced power management functionality, including various standby modes to minimize the power consumption with programmable local and remote wake-up capability, as well as LIN (only for SPSB0815 and SPSB0813) and CAN FD physical communication layers. The device has one low-drop voltage regulator to supply the system microcontroller and one voltage tracker to supply external peripheral loads such as sensors. V1 is available with a fixed rail (5 V or 3.3 V) and V1 overvoltage detection and protection solution, while V2 is a tracker voltage regulator of V1, programmable by SPI with 5 V or 3.3 V. Moreover, the device features four high-side drivers to supply LEDs and sensors. All outputs are short-circuit (SC) protected and implement open-load diagnosis. The ST standard SPI interface allows control and diagnosis of the device and enables generic software development.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **Functional block diagram of SPSB0815 and SPSB0813**

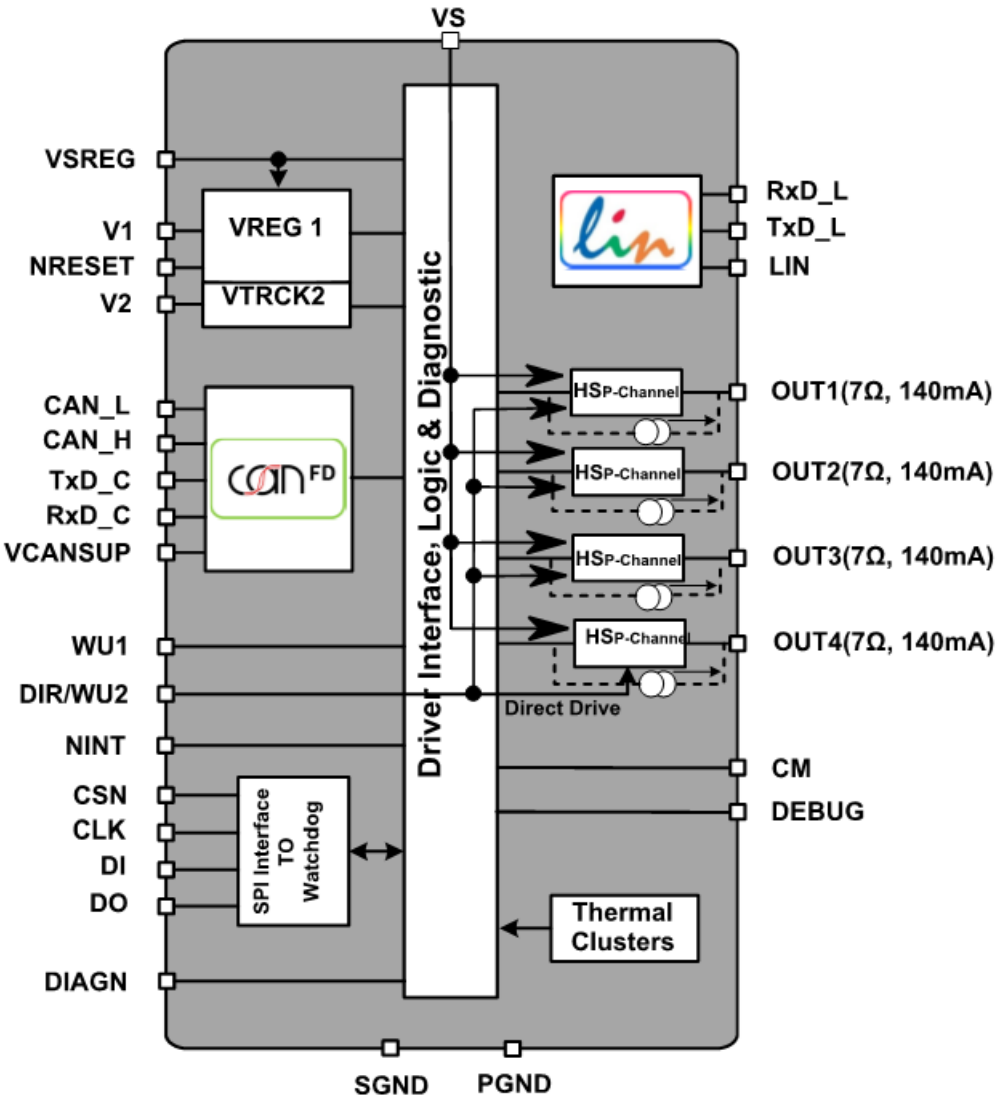
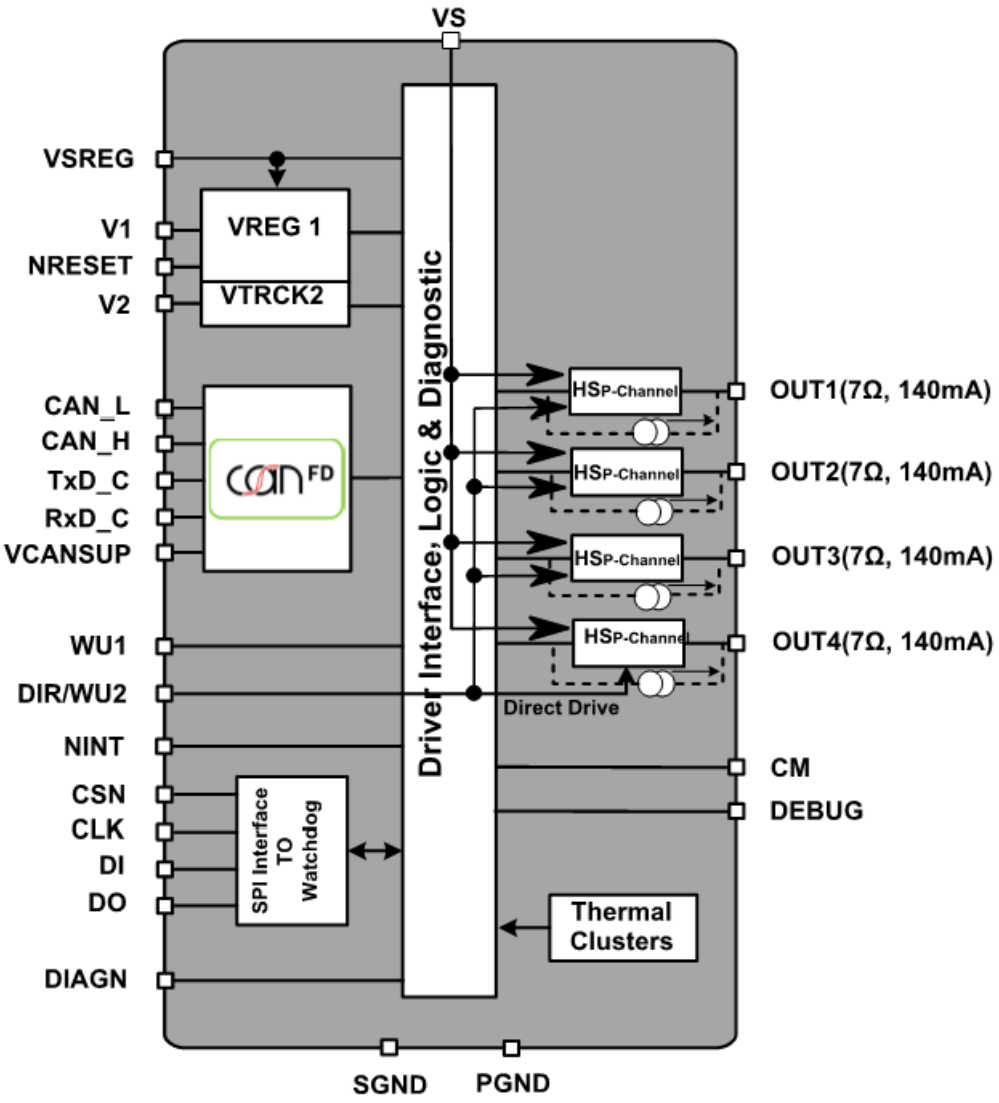


Figure 2. **Functional block diagram of SPSB081C5 and SPSB081C3**



1.2 Pin description

Figure 3. SPSB0815 and SPSB0813 - pin connection (top view)

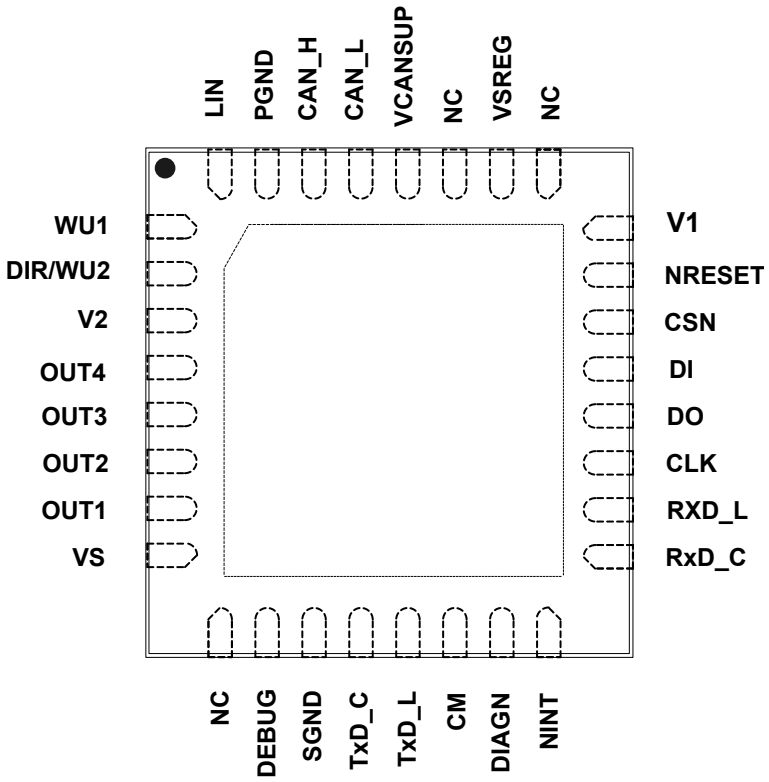


Figure 4. SPSB081C5 and SPSB081C3 - pin connection (top view)

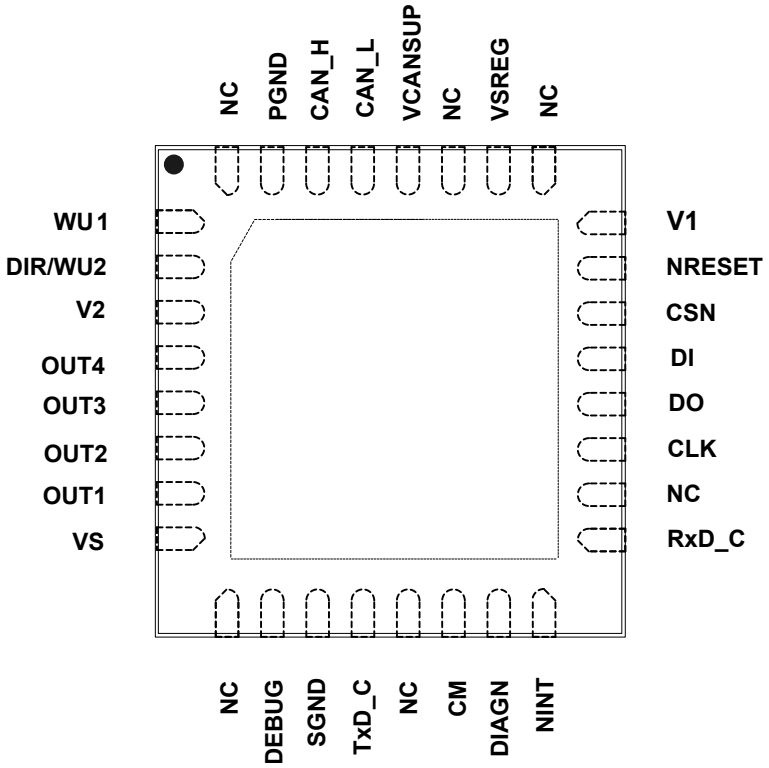


Table 1. Pin function

Pin SPSB081x	Pin SPSB081Cx	Pin name	Description	I/O type
1	1	WU1	Wake-up inputs 1: input pin for static or cyclic monitoring of external contacts	I
2	2	DIR/WU2	DIR → direct HS drive WU2 → input pin for static or cyclic monitoring of external contacts	I
3	3	V2	Voltage regulator 2 or tracker 2 output: 5 V or 3.3 V supply for external loads or CAN FD transceiver V2 pin is protected against reverse supply	O
4	4	OUT4	High-side-driver output to drive LEDs, sensors or to supply contacts	O
5	5	OUT3	High-side-driver output to drive LEDs, sensors or to supply contacts	O
6	6	OUT2	High-side-driver output to drive LEDs, sensors or to supply contacts	O
7	7	OUT1	High-side-driver output to drive LEDs, sensors or to supply contacts	O
8	8	VS	Power supply voltage for power stage outputs OUT1, OUT2, OUT3, and OUT4 (external reverse battery protection required). For this input, a ceramic capacitor as close as possible to GND is recommended	P
9	9	NC	Not connected	-
10	10	Debug	Debug input to deactivate the window watchdog (high active)	I
11	11	SGND	Signal ground	P
12	12	TxD_C	CAN transmit data input	I
13	-	TxD_L	LIN transmit data input	I
14	14	CM	Current monitor output: depending on the selected multiplexer bits of the control register this output sources an image of the instant current through the corresponding high side driver with a fixed ratio	O
15	15	DIAGN	Logical error indication output. Active low	O
16	16	NINT	indicates device errors, warning, and local/remote wake-up events	O
17	17	RxD_C	CAN receive data output (push pull output stages)	O
18	-	RxD_L	RxDL → LIN receive data output (only for SPSB0815 and SPSB0813)	O
19	19	CLK	SPI: serial clock input	I
20	20	DO	SPI: serial data output (push pull output stage)	O
21	21	DI	SPI: serial data input	I
22	22	CSN	SPI: chip select not input	I
23	23	NRESET	NReset output to microcontroller; internal pull-up of typical 25 kΩ (active low output stage)	O
24	24	V1	Voltage regulator 1 output: 5 V or 3.3 V supply, for example, microcontroller, CAN FD transceiver	O
25	25	NC	Not connected	-
26	26	VSREG	Power supply voltage to feed the internal voltage regulators; all internal regulated voltages for analog and digital functionality; LIN transceiver; CAN transceiver and the wake-up features (external reverse battery protection required/diode). For this input, a ceramic capacitor as close as possible to GND and an electrolytic backup capacitor are recommended	P
27	27	NC	Not connected	-

Pin SPSB081x	Pin SPSB081Cx	Pin name	Description	I/O type
28	28	VCANSUP	CAN supply input; to allow external CAN supply from V1, V2 or other external power supply	P
29	29	CAN_L	CAN low level voltage I/O	I/O
30	30	CAN_H	CAN high level voltage I/O	I/O
31	31	PGND	Power ground	P
32	-	LIN	LIN bus line	I/O
-	-	TAB	Ground connection	-

Note: Not connected pins must be connected to ground.

2 Maximum ratings

2.1 Operating range

Within the operating range, the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part recovers with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All the voltages are related to the potential at substrate ground.

2.1.1 Supply voltage ranges

All SPI communication, logic, and oscillator parameters work down to V_{SREG} = 3.5 V and are specified accordingly.

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for $V_S < V_{POR}$)
- Reset threshold correctly detected

2.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground.

Table 2. Absolute maximum ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_S	DC supply voltage	Jump start	-0.3	-	28	V
		Single pulse/tmax < 400 ms “transient load dump”	-0.3	-	40	V
V_{SREG}	DC supply voltage	Jump start	-0.3	-	28	V
		Single pulse/tmax < 400 ms “transient load dump”	-0.3	-	40	V
V1	Stabilized supply voltage, logic supply	V1 < V_{SREG}	-0.3	-	6.5	V
V2	Stabilized supply voltage(1)	-	-0.3	-	28	V
V_{DI}	Logic input	-	-0.3	-	V1 + 0.3	V
V_{CLK}	Logic input	-	-0.3	-	V1 + 0.3	V
V_{CSN}	Logic input	-	-0.3	-	V1 + 0.3	V
V_{DO}	Logic output	-	-0.3	-	V1 + 0.3	V
V_{RXDL}	Logic output	-	-0.3	-	V1 + 0.3	V
V_{RXDC}	Logic output	-	-0.3	-	V1 + 0.3	V
V_{NRESET}	Logic output	-	-0.3	-	V1 + 0.3	V
V_{CM}	Output voltage range	-	-0.3	-	V1 + 0.3	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DIAGN}	Logic output	-	-0.3	-	V1 + 0.3	V
V_{TXDC}	Logic input	-	-0.3	-	V1 + 0.3	V
V_{TXDL}	Logic input	-	-0.3	-	V1 + 0.3	V
V_{DEBUG}	Debug input pin voltage range	-	-0.3	-	V1 + 0.3	V
V_{WU1}	DC wake-up input voltage	-	-0.3	-	V_{SREG} + 0.3	V
$V_{DIR/WU2}$	DC wake-up input voltage	-	-0.3	-	V_{SREG} + 0.3	V
V_{LIN}	LIN bus I/O voltage range	-	-27	-	40	V
I_{INPUT}	Current injection into Vs related input pins	-	-	20	-	mA
I_{OUT_INJ}	Current injection into vs related outputs	-	-	20	-	mA
V_{CANSUP}	CAN supply	-	-0.3	-	5.25	V
V_{CANH}	CAN bus I/O voltage range	-	-27	-	40	V
V_{CANL}	CAN bus I/O voltage range	-	-27	-	40	V
V_{CANH} - V_{CANL}	Differential CAN-Bus voltage	-	-5	-	10	V
V_{OUT1}	Output voltage	-	-0.3	-	V_S + 0.3	V
V_{OUT2}	Output voltage	-	-0.3	-	V_S + 0.3	V
V_{OUT3}	Output voltage	-	-0.3	-	V_S + 0.3	V
V_{OUT4}	Output voltage	-	-0.3	-	V_S + 0.3	V
I_{VS}	Maximum cumulated current at VS drawn by OUT1; OUT2; OUT3; OUT4	-	-1.25	-	1.25	A
I_{VSREG}	Maximum cumulated current at VSREG drawn by LDO1; LDO2; LIN; CAN at wake-up	-	-1.25	-	1.25	A
I_{OUT1}	Output current(2)	-	-1.25	-	1.25	A
I_{OUT2}	Output current(2)	-	-1.25	-	1.25	A
I_{OUT3}	Output current(2)	-	-1.25	-	1.25	A
I_{OUT4}	Output current(2)	-	-1.25	-	1.25	A
I_{SGND}	Maximum current at SGND(2)	-	-1.25	-	1.25	A
I_{PGND}	Maximum current at PGND(2)	-	-1.25	-	1.25	A
GND pins	PGND versus SGND	-	-0.3	-	0.3	V

1. *SPSB081 is protected against V2 shorted to V_{SREG} and V2 reverse biasing when V_{SREG} is higher than 3.5 V.*
2. *Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.*

All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

Table 3. ESD protection

Item	Parameter	Condition	Values	Unit
Pins	All pins	HBM (1)	±2	kV
Power output pin	OUT1	HBM(2)	±4	kV

Item	Parameter	Condition	Values	Unit
Power output pin	OUT2	HBM(2)	±4	kV
Power output pin	OUT3	HBM(2)	±4	kV
Power output pin	OUT4	HBM(2)	±4	kV
Transceiver	LIN	HBM(2)	±8	kV
		Indirect ESD(3)	±8	kV
		Direct ESD(4)	±6	kV
Transceiver	CAN_H	HBM(2)	±8	kV
		Direct ESD(4)	±6	kV
Transceiver	CAN_L	HBM(2)	±8	kV
		Direct ESD(4)	±6	kV
Pins (5)	Corner pins	CDM (values for corner pins in brackets)	±500/(±750)	V

1. *HBM (human body model, 100 pF, 1.5 kW) according to AEC-Q100-002.*
2. *HBM with all none zapped pins grounded.*
3. *Indirect ESD test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'hardware requirements for LIN, CAN and flexray interfaces in automotive applications' (version 1.3, 2012-05-04).*
4. *Direct ESD test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'hardware requirements for LIN, CAN and Flexray interfaces in automotive applications' (version 1.3, 2012-05-04).*
5. *CDM (charged device model) according to AEC-Q100-011.*

Table 4. Transient immunity ratings according to ISO 7637-2

	Parameter	Value	Unit
ISO 7637-2 and IEC 62215-3 transients immunity according to "OEM_HW_Requirements_For_CAN_LIN_FR-Interfaces_V1.3_2012" and IBEE EMC test specifications (1) (LIN and CAN)	Pulse1	-100	V
	Pulse2a	+75	V
	Pulse3a	-150	V
	Pulse3b	+100	V

1. *ISO 7637 is a system level transient test. Different system level configurations may lead to different results.*

2.3 Temperature ranges and thermal data

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
T_{AMB}	Operating temperature (ECU environment)	-	-40	-	125	°C	F.019
T_J	Operating junction temperature	-	-40	-	175	°C	F.020
T_{STG}	Storage temperature	-	-55	-	150	°C	F.021
$T_{W\ ON}$(1)	Thermal over temperature warning threshold	-	140	-	160	°C	F.022
$T_{SD1\ OFF}$(1)	Thermal shut-down junction temperature 1	-	165	-	185	°C	F.023
$T_{SD2\ OFF}$(1)	Thermal shut-down temperature	-	175	-	195	°C	F.024
$T_{SD12HYS}$(1)	Thermal shut-down temperature hysteresis	-	-	5	-	°C	F.025
t_{fTjTW}	Thermal warning/shut-down filter time	Tested by scan	24	32	43	µs	F.026
$R_{TH\ JAMB}$(2)	Thermal resistance junction-to-ambient	-	-	38	-	°C/W	F.027

1. *Non-overlapping.*
2. *The values quoted are for PCB 129 mm x 60 mm x 1.6 mm, FR4, four layers; Cu thickness 0.070 mm (outer layers). Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm ±0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 3.5 mm x 3.5 mm.*

All parameters are guaranteed in the temperature range from -40 °C to 50 °C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 175 °C).

Parameters limits at higher temperatures than 150 °C may change with respect to what is specified as per the standard temperature range.

Device functionality at high temperature is guaranteed by characterization.

SPSB081 embeds a multitude of junctions housed in a relatively small piece of silicon. The devices contain, among all the described features, four high-sides, two voltage regulators (one of which can work as voltage tracker). For this reason, using the thermal impedance of a single junction (that is, voltage regulator or major power dissipation contributor) does not allow to predict thermal behavior of the whole device and therefore it is not possible to assess if a device is thermally suitable for a given activation profile and loads characteristics. Some representative and realistic worst-case thermal profiles are described in the below paragraph. The following measurement methods can be easily implemented, by final user, for a specific activation profile.

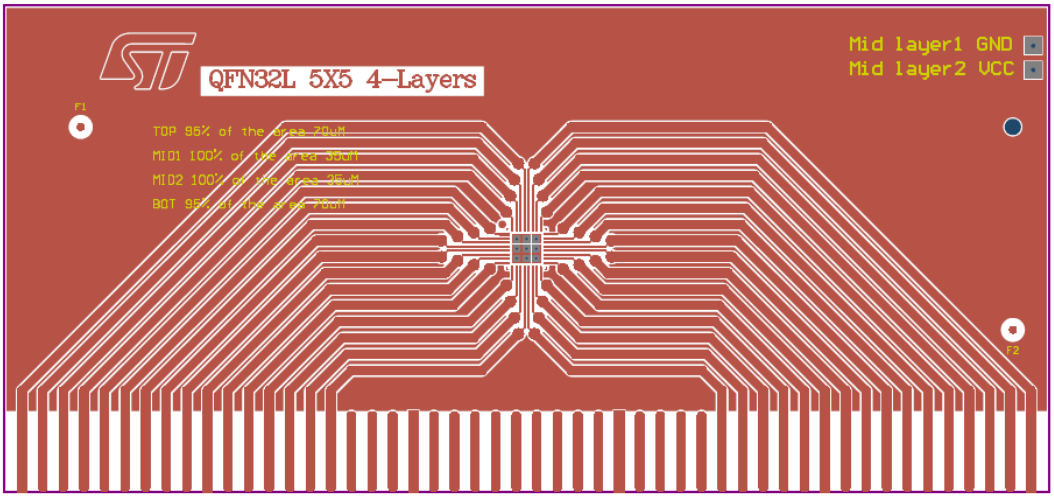
Activation profile battery voltage: 16 V, ambient temperature starts at 85 °C.

DC activation:

- V1 (3.3 V) charged with 70 mA; R_{DSON} = 470 Ω (DC activation)
- V2 (3.3 V) charged with 50 mA; R_{DSON} = 680 Ω (DC activation)
- OUT1: I_{LOAD} = 50 mA; R_{DSON} = 330 Ω (DC activation)
- OUT2: I_{LOAD} = 50 mA; R_{DSON} = 330 Ω (DC activation)
- OUT3: I_{LOAD} = 50 mA; R_{DSON} = 330 Ω (DC activation)
- OUT4: I_{LOAD} = 50 mA; R_{DSON} = 330 Ω (DC activation)
- CAN-LIN not relevant

Test execution: once thermal equilibrium is reached with all DC load active, the “cyclic activation” sequence is applied. The device operates always without triggering the thermal warning threshold.

Figure 5. QFN32L (5.0x5.0x1.0 mm) 4-layers



Note: PCB 129 mm x 60 mm x 1.6 mm, FR4, four layers; Cu thickness 0.070 mm (outer layers). Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm ±0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 3.5 mm x 3.5 mm.

3 Functional description

3.1 Supply VS and VSREG

VSREG supplies voltage regulators V1 and V2, all internal regulated voltages for analog and digital functionality, LIN, CAN and the wake-up features. P-channel high side switches OUT1, OUT2, OUT3, OUT4 and fail-safe block are supplied by VS. In case of VSREG pin disconnected, all power devices connected to VS are automatically switched OFF.

Note: After device startup, it is suggested to perform a status registers read and clear command to clean any spurious error flags.

3.2 Voltage regulators

The SPSB081 contains one fully protected low drop voltage regulator (V1) and one low dropout tracking regulator (V2), which are designed for very fast transient response and do not require electrolytic output capacitors for stability. The two low drops out voltage regulators can provide 5 V or 3.3 V; the following table summarizes the possible configurations of the two LDOs:

Table 6. Voltage regulators configuration

Configuration	P/N	V1 output voltage (linear case)	V2 output voltage (linear case)	V2 output voltage (tracking case)	V2_TKR
1	SPSB0813 SPSB081C3	3.3 V	3.3 V(1)	YES	0 or 1
2			5.0 V	Not available	Only 0
3	SPSB0815 SPSB081C5	5.0 V	3.3 V	Not available	Only 0
4			5.0 V	YES	0 or 1

1. *In this case, the CAN transceiver embedded inside the SPSB0813 shall be supplied by an external V_{REG} at 5 V via the CAN supply pin.*

The voltage regulator V2 can be configured by means of the V2_TKR bit in CR2 as a linear independent LDO (V2_TKR = 0, default) or as a tracker of the V1 voltage regulator (V2_TKR = 1).

3.2.1 Voltage regulator: V1

The V1 voltage regulator provides 5 V (for SPSB0815 and SPSB081C5) or 3.3 V (for SPSB0813 and SPSB081C3) supply voltage (configurable by OTP) and up to 250 mA continuous load current to supply the system microcontroller and the integrated CAN transceiver. The V1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode. The V1 voltage regulator is supplied by pin V_{SREG}.

In addition, the V1 regulator supplies the device internal loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection must be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors ≥ 1 µF.

In case the device temperature exceeds the TSD1 threshold, all outputs (OUTx, V2, LIN, CAN) are deactivated except V1 regulator, which remains on. LIN and CAN transceivers are forced in "receive only" mode. Hence, the microcontroller has the possibility for interaction or error logging. If the chip temperature exceeds TSD2 threshold (TSD2 > TSD1), V1 is deactivated and all wake-up sources (CAN, LIN, WU1, WU2, and timer) are disabled. After t_{TSD}, the voltage regulator will restart automatically. If the restart fails seven times within one minute the SPSB081 is forced into VBAT_standby mode. The status bit in SR1 Forced_Sleep_TSD2/V1SC is set.

In case of overvoltage an internal pulldown circuit is activated to limit the current accumulated in the external capacitor.

3.2.2 Voltage regulator: V2

The SPSB081 embeds one 5 V or 3.3 V (configurable by V2_RAIL bit in CR2) low dropout tracking regulator designed to provide an output voltage that closely tracks (±20 mV) the V1 reference input while delivering on the V2 output pin up to 100 mA. The voltage regulator V2 can be configured by means of the V2_TKR bit in CR2 as a linear independent LDO (V2_TKR = 0, default) or as a tracker of the V1 voltage regulator (V2_TKR = 1).

The V2 can be configured as tracker of the V1 only at the same voltage output level 5 V for SPSB0815 and SPSB081C5 (Conf #4 in Table 6) and 3.3 V for the SPSB0813 and SPSB081C3 (Conf #1 in Table 6). The tracking regulator is protected against:

- Overload
- Overtemperature
- Short-circuit (short to ground and battery supply voltage)
- Reverse biasing

3.2.3 Voltage regulator failure

The V1 and V2 regulators output voltages are monitored.

In case of a drop below the V_1, V_2 fail thresholds ($V_{1,2} < V_{1,2FAIL}$, for $t > t_{V1,2FAIL}$), the failure bits V1FAIL, V2FAIL (SR2) are latched. The fail bits can be cleared by a dedicated SPI command.

3.2.4 Short to ground detection

At turn-on of the V1 and V2 regulators, a short to GND condition is detected by monitoring the regulator output voltage.

If V1 or V2 is below the $V_{1FAIL,}(V_{2FAIL})$ thresholds for $t > t_{V1SHORT}$ ($t > t_{V2SHORT}$) after turn-on, the SPSB081 will identify a short-circuit condition at the related regulator output and the regulator will be switched off.

In case of V1 short to GND the device enters VBAT_standby mode automatically.

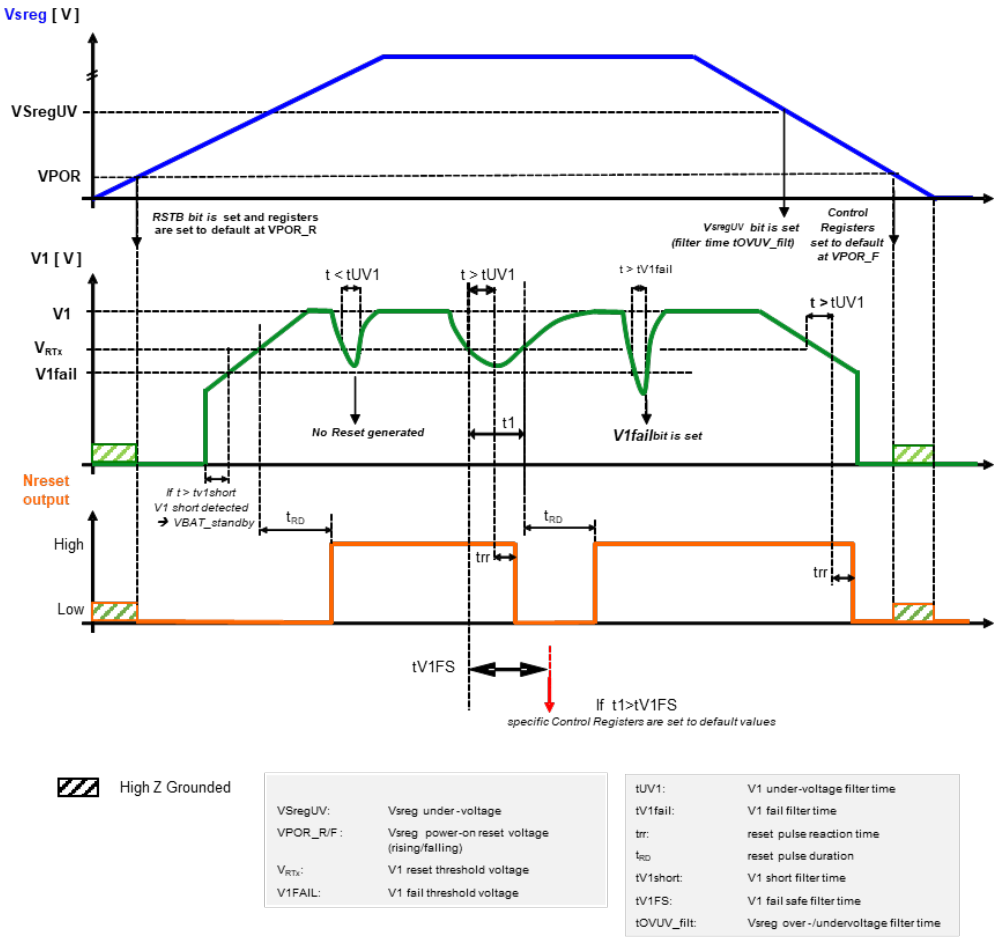
Bits FORCED_SLEEP_TSD2/V1SC (SR1) and V1FAIL (SR2) are set.

In case of a V2 short to GND failure the V2SC (SR2) and V2FAIL (SR2) bits are set.

Once the output voltage of the corresponding regulator exceeds the V_{1FAIL} (V_{2FAIL}) thresholds the short-to-ground detection is disabled. In case of a short-to-ground condition, the regulator is switched off due to thermal shutdown.

3.2.5 Voltage regulator behavior

Figure 6. Voltage regulator behavior and diagnosis during supply voltage ramp-up/ramp-down conditions



3.3 Operating modes

The device can be operated in four different operating modes:

- Active mode: normal operating mode
- SW-debug mode: software debugging
- V1_standby mode: low power mode
- VBAT_standby mode: ultralow power mode

3.3.1 Active mode

All functions are available, and the device is controlled by SPI.

3.3.2 SW-debug mode

To allow software debugging, the watchdog can be deactivated by applying an external voltage to the DEBUG input pin ($V_{DEBUG} > V_{diH}$).

In debug mode, all device functionality is available, including CAN, which is enabled by default. The watchdog is deactivated.

At exit from debug mode ($V_{DEBUG} < V_{diL}$) the watchdog starts with a long open window.

Note: The device includes a test mode that is activated by a dedicated sequence including, among others, a high voltage at the debug pin; debug mode is not intended for normal applicative conditions.

3.3.3 V1_standby mode

The transition from active mode to V1_standby mode is controlled by SPI (STBY_SEL bit and GO_STBY bit in CR2).

To supply the microcontroller in a low power mode, the V1 voltage regulator remains active.

After the V1_standby command (CSN low to high transition), the device enters V1_standby mode immediately and the watchdog starts a long open window (t_{LW}). The watchdog is deactivated as soon as the V1 load current drops below the I_{CMP} threshold ($I_{V1} < I_{CMP}$).

The V1 load current monitoring can be deactivated by setting ICMP = 1. In this configuration, the watchdog is deactivated upon transition into V1_standby mode without monitoring the V1 load current.

Writing ICMP (CR 34) = 1 is only possible with the first SPI command after setting ICMP_CONFIG_EN (Config Reg) = 1. The ICMP_CONFIG_EN bit is reset to ‘0’ automatically with next SPI command.

LIN and CAN transmitters are switched off in V1_standby mode.

OUT1, OUT2, OUT3, and OUT4 remain in the configuration programmed before the standby command.

V2 voltage regulator remains in the configuration programmed before the standby command. Even though LIN and CAN transceivers are switched off, they can still wake up the micro (see Table 7).

In V1_standby mode various wake-up sources can be individually programmed. Normally a wake-up event puts the device into active mode and forces the NINT pin to a low level indicating the wake-up condition to the microcontroller. Writing IWK (CR 34) = 1 a wake-up event on CAN and wake-up pins forces NINT pin to a low level indicating the wake-up condition to the microcontroller. However, no change in the SBC mode occurs.

3.3.4 Interrupt

The interrupt signal on NINT pin is generated to communicate a specific event to the microcontroller. NINT is pulled low after a reaction time when one of the following events occurs.

In active mode, this event can be related to each one of the status flags latched in the global status byte register (GSBN bit).

A bit register is available to mask each one of these flags:

- RSTB: MASK_RSTB (0x3F)
- PLE: MASK_PLE (0x3F)
- FE: MASK_FE (0x3F)
- DE: MASK_DE (0x3F)
- GW: MASK_GW (0x3F)

These masks are common for the generation of GSBN, NINT, and DIAGN (in extended mode).

NINT pulse can also be related to the CAN communication timeout event (no CAN communication for $t > t_{Silence}$). The CANTO flag is set. This interrupt can be masked by CANTO_NINT_MASK SPI bit.

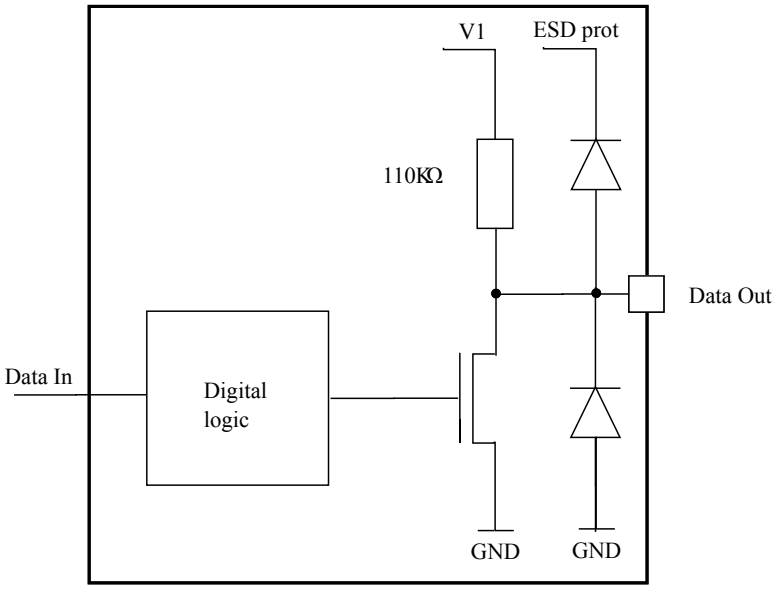
In V1 standby mode, it can also be related to the following events:

- CAN communication timeout (no CAN communication for $t > t_{SILENCE}$). The CANTO flag is set. This interrupt can be masked by CANTO_NINT_MASK SPI bit.
- Wake-up from V1_standby mode by any wake-up source (WU1, WU2, LIN, CAN, TIMER1/2, SPI). This interrupt can be masked by WU_NINT_MASK SPI bit.

In case of increasing V1 load current during V1_standby mode ($I_{V1} > I_{CMP}$), the device remains in standby mode and the watchdog starts with a long open window. No interrupt signal is generated.

NINT pin is an open drain structure to allow multiple connections.

Figure 7. **Interrupt pin**



3.3.5 VBAT_standby mode

The transition from active mode to VBAT_standby mode is initiated by an SPI command (STBY_SEL bit and GO_STBY bit in CR2).

In VBAT_standby mode, the voltage regulators V1 and V2, the power outputs as well as LIN and CAN transmitters are switched off.

An NReset pulse is generated and last asserted low upon wake-up from VBAT_standby mode and until 2ms after LDO1 is fully operative.

3.4 Wake-up from standby modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

Table 7. **Wake-up source**

Wake-up source	Description
LIN bus activity	It can be disabled by SPI
CAN bus activity	It can be disabled by SPI
Level change of WU	It can be configured or disabled by SPI
$I_{V1} > I_{CMP}$	The device remains in V1_standby mode but watchdog is enabled (if ICMP = 0). No interrupt is generated
Timer interrupt/ wake-up of µC by TIMER	Programmable by SPI: • V1_standby mode: device wakes up and interrupt signal is generated at NINT when programmable time-out has elapsed • VBAT_standby mode: device wakes up after programmable timer expiration. V1 regulator is turned on and NReset signal is generated when programmable time-out has elapsed
SPI access	Always active (except in VBAT_standby mode) Wake-up event: CSN falling edge

To prevent the system from a deadlock condition (no wake-up from standby possible) a configuration where all wake-up is disabled, is not allowed.

Accordingly, if the following condition is set by SPI:

- CAN_WU_EN = 0
- LIN_WU_EN = 0
- WU1_EN = 0
- WU2_EN = 0

The effect is to put all these register bits in their default condition:

- CAN_WU_EN = 1
- LIN_WU_EN = 1
- WU1_EN = 1
- WU2_EN = 1

For SPSB081C devices (without LIN), at least one of these WU sources has to be kept (CAN, WU1 or WU2).

All wake-up sources are configured to default values in case of such invalid setting. The SPI error bit (SPIE) in the global status register is set.

3.4.1 Wake-up inputs

The WU1 and WU2 inputs can be configured as wake-up sources. Each wake-up input is sensitive to any level transition (positive and negative edge) and can be configured for static or cyclic monitoring of the input voltage level by suitable setting of CR1 [8..11] bits (WUx_FILT_0 and WUx_FILT_1) which allows to choose the monitoring among static, cyclic with timer 1 or cyclic with timer 2. When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.

For static contact monitoring, a filter time of t_{WU_STAT} is implemented. The filter is started when the input voltage passes the specified threshold V_{WUTHP}. Wake-up status bit (WUx_STATE bit in SR5 [18..19]) is set only if this threshold is passed for more than t_{WU_STAT}.

Cyclic contact monitoring, conceived to reduce the quiescent current of the device, allows instead periodical (not threshold dependent) activation of the wake-up input to read the status of the external contact. The periodical activation is driven by timer 1 or timer 2 whose settings (on-time and period) can be configured through CR2 [8..13] and [16..21] bits (Tx_PER_y and Tx_ON_y bit). The input signal is filtered with a filter time of t_{WU_CYC} after a delay (80% of the configured timer on-time). A wake-up will be processed if the status has changed versus the previous cycle, therefore wake-up status bit (WUx_STATE bit in SR5 [18..19]) is set only if status during consecutive on-time is different, after the configured delay and t_{WU_CYC}.

The buffered outputs OUT1, OUT2, OUT3, and OUT4 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up input.

Figure 8. **Static monitoring: wake-up occurs if threshold is greater than the filter time**

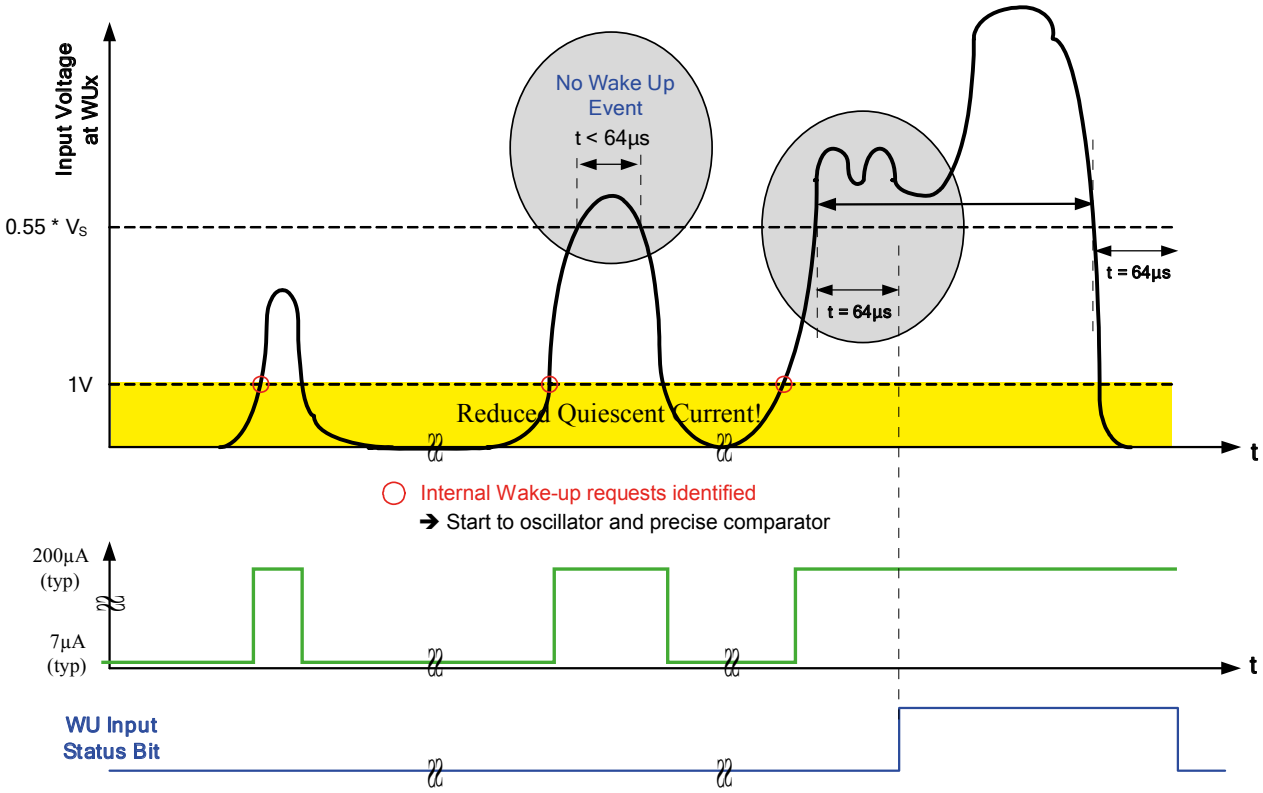
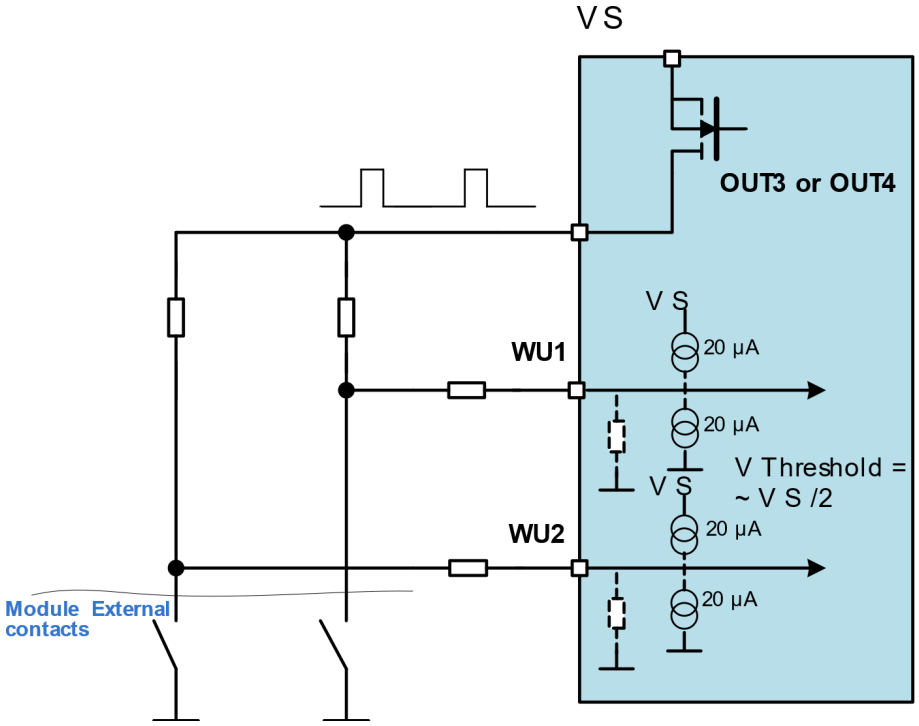


Figure 9. **Cyclic monitoring: the external contacts are supplied periodically by the internal timer**



In standby modes, the inputs are configurable with an internal pull-up or pull-down current source according to the setup of the external contact. Moreover, in case of cyclic sensing, an internal pull-down resistor (R_{WU_ACT}) is periodically activated on each rising edge of the TIMER_ON. R_{WU_ACT} is activated also for static wake-up, but in this case it occurs just after WU request (see the figure above), keeping this condition for at least the filter time t_{WU_STAT} (or more, if the WU is valid and the device enters in active mode).

In active mode, the inputs have in fact only the internal pull-down resistor and the input status can be read by SPI. Static sense should be configured before the read operation is started to reflect the actual input level.

Being DIR/WU2_EN enable bit, in config register (0x3F), set to 0 by default, the DIR/WU2 pin is configured as wake-up function. If DIR/WU2_EN enable bit is set to 1 the DIR/WU2 pin is a low voltage direct driving of OUT1..4. Threshold is set in this case at 1.5 V.

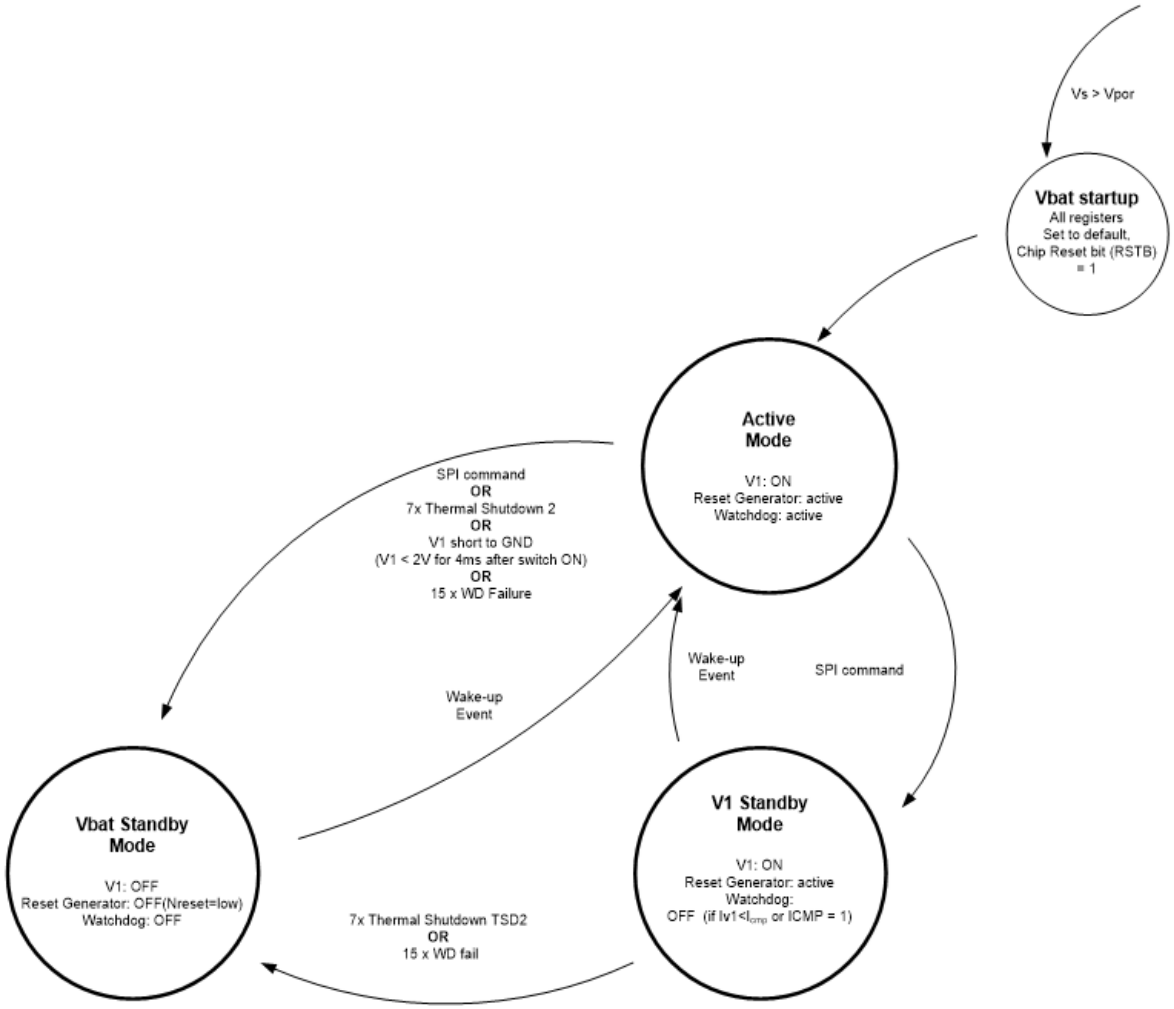
3.5 Functional overview (truth table)

Table 8. Functional overview

Version	Function	Comments	Operating modes		
			Active mode	V1_standby static mode (cyclic sense)	VBAT_standby static mode (cyclic sense)
3.4.1	Voltage regulator V1	VOUT = 5 V/3.3 V	On	On(1)	Off
3.4.2	Voltage regulator V2	VOUT = 5 V/3.3 V	On/Off(2)	On(2)/Off	On(2)/Off
3.4.3	Reset generator	-	On	On	Off
3.4.4	Window watchdog	V_1 monitor	On	Off (On if $I_{V1} > I_{CMP}$ and ICMP = 0)	Off
3.4.5	Wake-up	-	Off	Active(3)	Active(3)
3.4.6	HS-cyclic supply	Oscillator time base	On/Off	On(2)/Off	On(2)/Off
3.4.7	LIN	LIN ISO 17987-4/2016	On(2)	Off(4)	Off(4)
3.4.8	CAN FD	-	On/Off(5)	Off(4)	Off(4)
3.4.9	Oscillator	-	On	On/Off(6)	On/Off(6)
3.4.10	V_S monitor	-	On(7)	On/Off(7)	On/Off(7)
3.4.11	OUT1 (P-channel HS)	-	On/Off(2)	On/Off(2)	On/Off(2)
3.4.12	OUT2 (P-channel HS)	-	On/Off(2)	On/Off(2)	On/Off(2)
3.4.13	OUT3 (P-channel HS)	-	On/Off(2)	On/ Off(2)	On/Off(2)
3.4.14	OUT4 (P-channel HS)	-	On/Off(2)	On/ Off(2)	On/Off(2)
3.4.15	Thermal shutdown TSD2	-	On	On	Off
3.4.16	Thermal shutdown TSD1x (for P-channel HS)	-	On	On(8)	On/Off(2)

1. *Supply the processor in low current mode.*
2. *According to SPI setting.*
3. *Unless disabled by SPI.*
4. *The bus state is internally stored when going to standby mode. A change of bus state will lead to a wake-up after exceeding of internal filter time (if wake up by LIN or CAN is not disabled by SPI).*
5. *After power-on, the CAN FD transceiver is in 'CAN Trx standby' mode. It is activated by SPI command (CAN_ACT = 1).*
6. *ON, if is enabled at least one of the following: cyclic sense, OUT1, OUT2, OUT3, OUT4, V2.*
7. *ON when at least one OUTx is enabled and OFF when OUTx are disabled.*
8. *V1, V2, OUT1, OUT2, OUT3, and OUT4 are thermal monitored.*

Figure 10. **Main operating modes**



3.6 Configurable window watchdog

During normal operation, the watchdog monitors the microcontroller within a programmable trigger cycle.

After power-on or standby mode, the watchdog starts with a timeout (long open window t_{LW}). The timeout allows the microcontroller to run its own setup and then to start the window watchdog by setting TRIG = 1. Later, the microcontroller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area T_{SWX}. The trigger time is configurable by SPI.

A correct watchdog trigger signal will immediately start the next cycle.

After eight watchdog failures in sequence, the V1 regulator is switched off for t_{V1OFF}. After seven additional watchdog failures the V1 regulator is turned off permanently and the device is forced into VBAT_standby mode. The status bit FORCED_SLEEP_WD (SR1) is set. A wake-up is possible by any activated wake-up source.

In case of a watchdog failure, the power outputs and V2 are switched off and the device enters fail-safe mode. All control registers are set to their fail-safe values.

The following diagrams illustrate the watchdog behavior of the device. The diagrams are split into 3 parts. The first diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. The third diagram shows the transition in and out of debug mode. All three diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and debug mode.

Figure 11. **Watchdog in normal operating mode (no errors)**

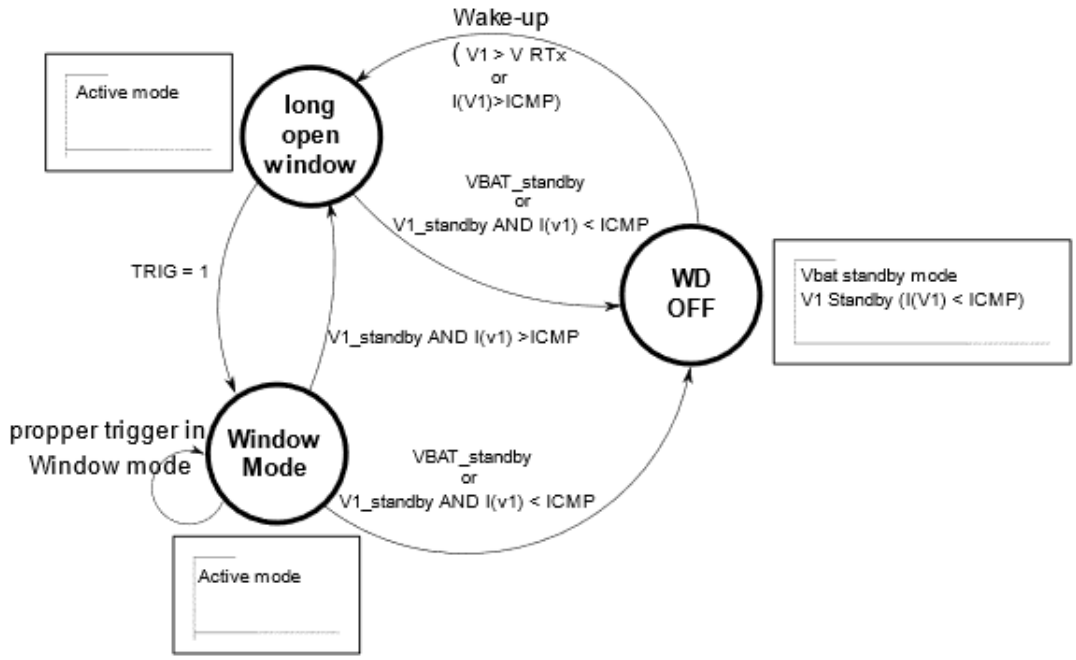


Figure 12. **Watchdog with error conditions**

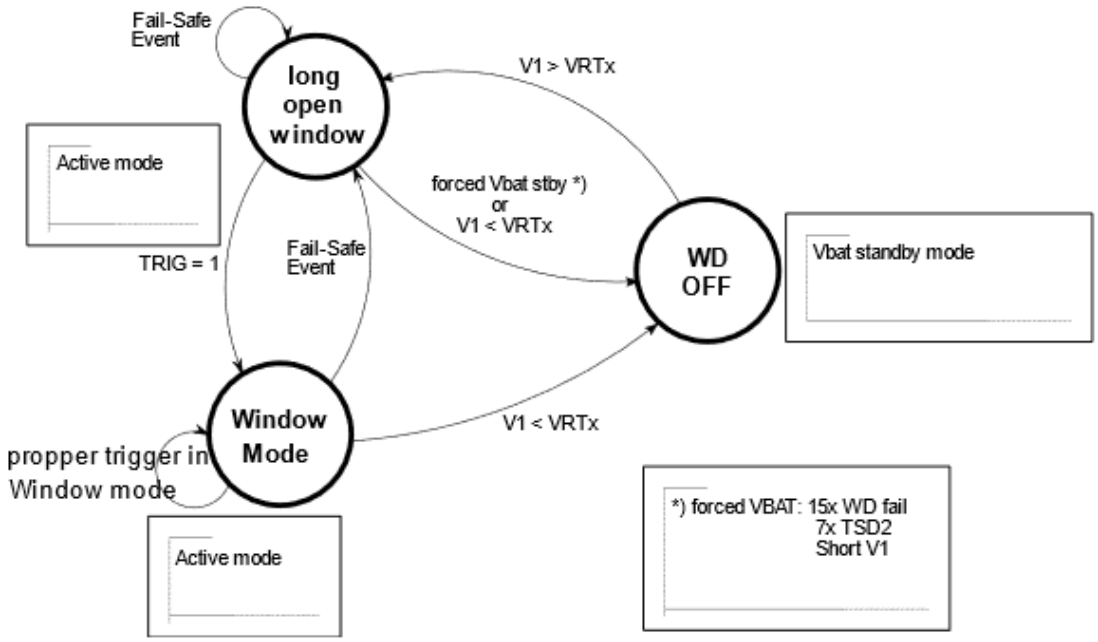
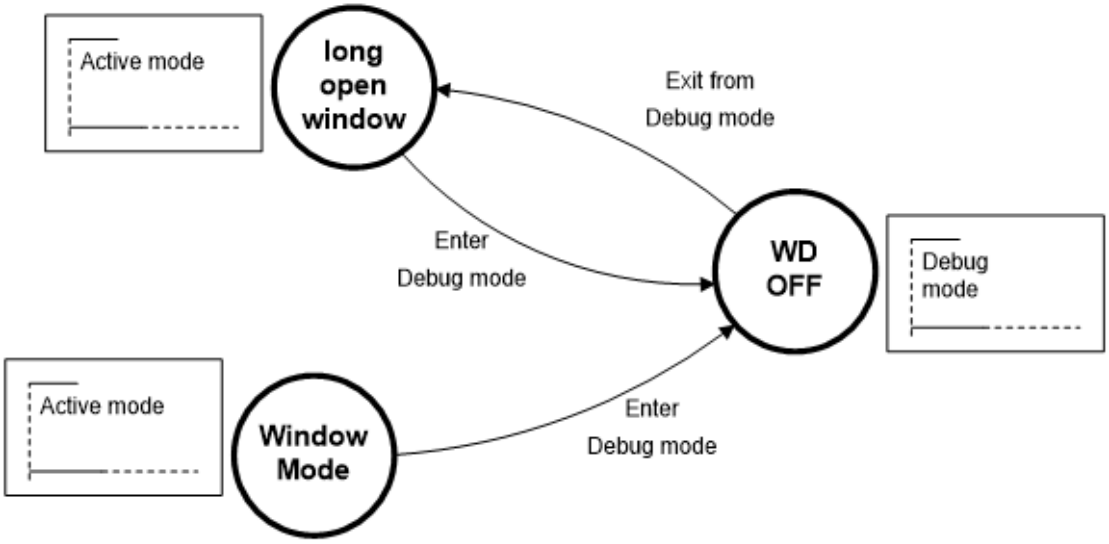


Figure 13. **Watchdog in debug mode**



Note: Whenever the device is operated without servicing the mandatory watchdog trigger events, a sequence of 15 consecutive reset events is performed and the device is forced into Vbat_Stby mode with bit FORCED_SLEEP_WD in SR1 set.

If the device is woken up after such a forced Vbat_Stby condition and the watchdog is still not serviced, the device, after one long open watchdog window is reforced into the same Vbat_Stby mode until the next wake-up event. In this case, an additional watchdog failure is generated, but the fail counter is not cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

3.6.1 Change watchdog timing

The watchdog trigger time can be configured by setting the WD_TIME (CR 2) bit. Writing to these bits is only possible with the first SPI command after setting WD_CONFIG_EN = 1 (Config register (0x3F)). The WD_CONFIG_EN bit is reset to 0 automatically with next SPI command.

When FAIL_SAFE is active, these SPI registers are not accessible. Therefore, the FAIL_SAFE status needs to be cleared. In case of a WD_FAIL, the clear is performed by starting a long open window.

When a new configuration has been programmed, the watchdog behaves with the old configuration until the next trig event.

The new value of WD_TIME is loaded in the watchdog module on the next trig event after the SPI configuration. The following watchdog cycle uses the new programmed value.

3.7 Fail safe mode

3.7.1 Temporary failures

SPSB081 enters fail-safe mode in case of:

- Watchdog failure
- V1 failure (V1 < V_{RTX} for t > t_{V1FS})
- Thermal shutdown TSD2

The fail-safe functionality is also available in V1_Standby mode. During V1_Standby mode the fail-safe mode is entered in the following cases:

- Watchdog failure (if watchdog still running due to I_{V1} > I_{CMP})
- V1 failure (V1 < V_{RTX} for t > t_{V1FS})
- Thermal shutdown TSD2

In fail-safe mode, the device returns to a fail-safe state. The fail-safe condition is indicated to the system in the global status byte. The conditions during the fail-safe mode are:

- All outputs and V2 are turned off
- All control registers are set to default values
- Write operations to control registers are blocked until the fail-safe condition is cleared (see table below). Only the following bits are not write-protected:
  - CR1 (0x01):
    - TRIG
    - CAN_ACT
  - CR2 (0x02):
    - Timer settings (bits 8…13 and bits 16…21)
  - CR5 (0x05):
    - OUT1_x (bits 0…2)
    - OUT2_x (bits 4…6)
    - OUT3_x (bits 8…10)
    - OUT4_x (bits 12…14)
  - CR9 (0x09) to CR11 (0x0B)
    - PWM frequency and duty cycles
  - Config register (0x3F)
    - V2_0
    - V2_1
- LIN transmitter remains on
- CAN FD transceiver remains on
- Wake-up is enabled
- Corresponding failure bits in status registers are set.
- FS bit (bit 0 global status byte) is set

If the fail-safe mode was entered, it keeps active until the fail-safe condition is removed and the fail-safe was read by SPI. Depending on the root cause of the fail-safe operation, the actions to exit fail-safe mode are as shown in the following table.

Table 9. Temporary failures conditions

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	Watchdog Early write failure or expired window	FS (global status byte) = 1 WDFAIL (SR1) = 1 WDFAIL_CNT_x (SR1) = n+1	TRIG = 1 during long open window read and clear SR1
V1	Undervoltage	FS (global status byte) = 1 V1UV (SR1) = 1(1) V1FAIL (SR2) = 1(2)	V1 > V_{RTX} Read and clear SR1
Temperature	T_J > TSD2	FS (global status byte) = 1 TW (SR2) = 1 TSD1 (SR1) = 1 TSD2 (SR1) = 1	T_J < TSD2 Read and clear SR1

1. *bit V1UV in SR1 is set for t > tuv1 (16 µs). Fail-Safe bit GSR/FS is set only after t_{RD} (NRESET low pulse).*
2. *If V1 < V_{1FAIL} (for t > t_{V1FAIL}). The fail-safe bit is located in the global status register.*

3.7.2 Non recoverable failures - Forced in VBAT_standby mode

If the fail-safe condition persists and all attempts to return to normal system operation fail, the SPSB081 is forced into VBAT_standby mode to prevent damage to the system. The VBAT_standby mode can be terminated by any wake-up source. The root cause of the VBAT_standby is indicated in the SPI status registers.

In VBAT_standby mode, all control registers are set to power on default.

The VBAT_standby mode is entered in case of:

- Multiple watchdog failures: FORCED_SLEEP_WD = 1 (15x watchdog failure)
- Multiple thermal shutdowns 2: FORCED_SLEEP_TSD2/V1SC = 1 (7x TSD2)
- V1 short at turn-on (V1 < V_{1FAIL} for t > $t_{V1SHORT}$): FORCED_SLEEP_TSD2/V1SC (SR 1) = 1
- Loss of ground: SGNDLOSS(SR6) = 1

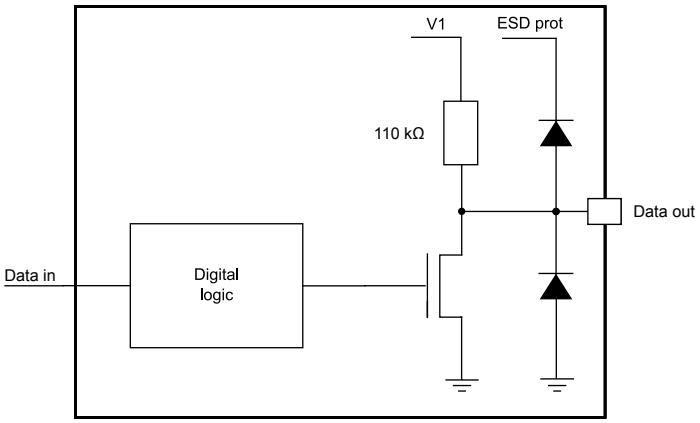
Table 10. Non recoverable failures conditions

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	15 consecutive watchdog failures	FS (global status byte) = 1 WDFAIL (SR 1) = 1 FORCED_SLEEP_WD (SR 1) = 1	Wake-up TRIG = 1 during long open window read and clear SR1
V1	Short at turn-on	FS (global status byte) = 1 V1FAIL = 1 FORCED_SLEEP_TSD2/V1SC (SR 1) = 1	Wake-up Read and clear SR1
V1	Overvoltage	FS (global status byte) = 1 FORCED_SLEEP_V1OV (SR2) = 1	Wake-up Read and clear SR1
Temperature	7 times TSD2	FS (global status byte) = 1 TW (SR 2) = 1 TSD1 (SR 1) = 1 TSD2 (SR 1) = 1 FORCED_SLEEP_TSD2/V1SC (SR 1) = 1	Wake-up Read and clear SR1
SGND	Loss of ground at SGND pin	FS (global status byte) = 1 SGNDLOSS (SR 6) = 1	Wake-up Read and clear SR1

3.8 Reset output (NRESET)

At power-up, the reset signal is low. When V_S > V_{POR}, the RSTB bit is set and SPI registers are set to default values. If V1 is turned on and the voltage exceeds the V1 reset programmable threshold V_{RTX} by SPI, the reset output “NRESET” is pulled up by internal pull-up resistor to V1 voltage after a reset delay time (t_{RD}). This is necessary for a defined start of the microcontroller when the application is switched on. As soon as the NRESET is released, the watchdog timing starts with a long open window. At power down, the device is reset, and control registers are set to default values and RSTB bit is set to “1” (see the following figure).

Figure 14. **NRESET pin**

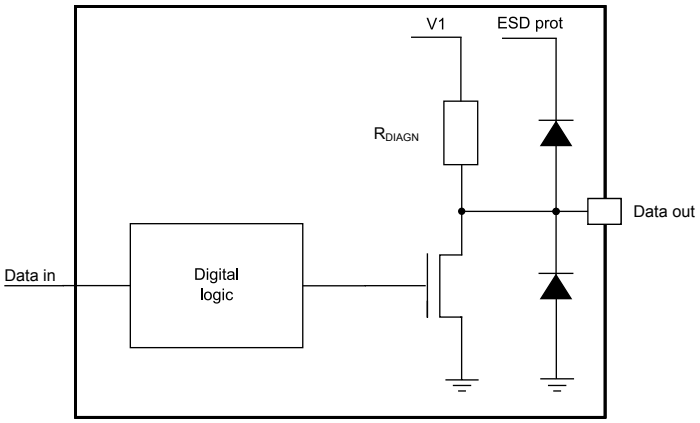


A reset pulse is generated in case of:

- V1 drops below V_{RTX} (configurable by SPI) for t > t_{UV1}
- Watchdog failure
- Turn-on of the V1 regulator (VSREG power-on or wake-up from VBAT_standby mode)

3.9 DIAGN output

Figure 15. **DIAGN pin**



DIAGN pin can be directly connected to the microcontroller and it is pulled up to V1 voltage by internal pull-up resistor.

DIAGN pin can be configured by DIAGN_EXT bit in normal mode or extended mode.

In default DIAGN configuration (DIAGN_EXT = 0), DIAGN pin is set low if a failure considered in fail safe mode occurs (for example, watchdog failure; V1 failure; thermal shutdown TSD2).

As soon as the FS error source is cleared, the signal is pulled up to V1 voltage.

In extended DIAGN configuration (DIAGN_EXT = 1), DIAGN pin reflects one or more errors such as reported in the GLOBAL STATUS BYTE register by global status bit not (GSBN) and it is set to low if at least one error condition occurs.

A bit register is available to mask each one of GSBN flags:

- RSTB: MASK_RSTB (0x3F)
- PLE: MASK_PLE (0x3F)
- FE: MASK_FE (0x3F)

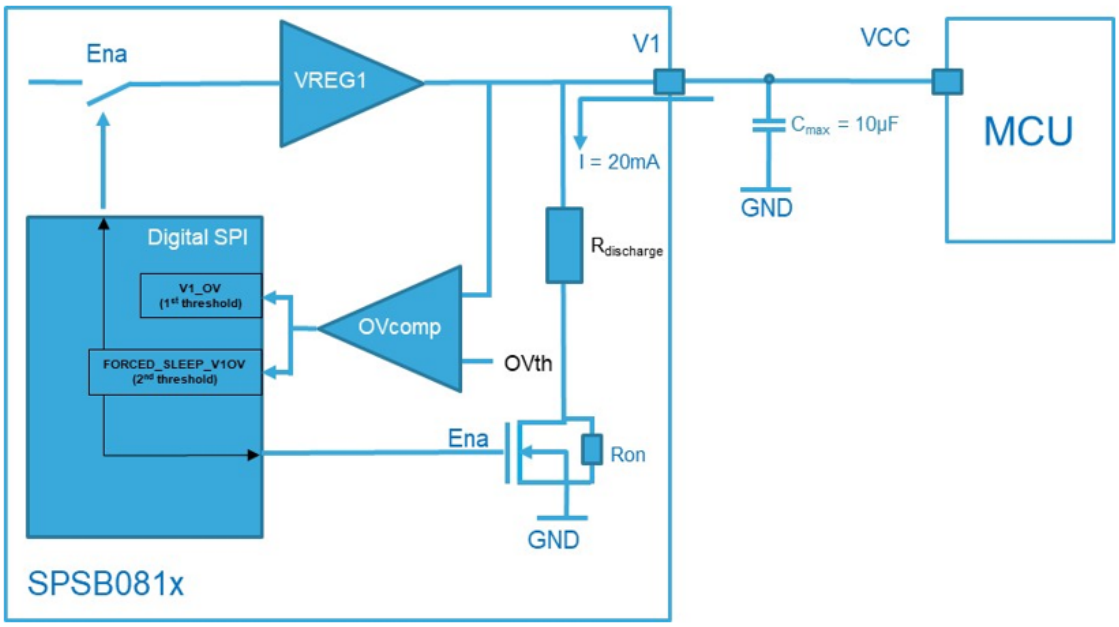
- DE: MASK_DE (0x3F)
- GW: MASK_GW (0x3F)

Note: DIAGN is automatically configured in normal mode (DIAGN_EXT = 0) after a reset event.

3.10 V1 overvoltage detection

SPSB081 protects the MCU against voltages over 5 V (or 3.3 V) that could harm its functionalities. For this purpose, to sink the exceeding current accumulated in the external capacitor usually directed to the MCU, the SPSB081 uses an internal pulldown circuit, where output current flows through the pulldown resistor to ground. If the bit V1_OVP = 1 in CR2 the overvoltage protection circuits is enabled. If V1_OVP = 0 there is no overvoltage protection anymore.

Figure 16. Overvoltage protection on V1



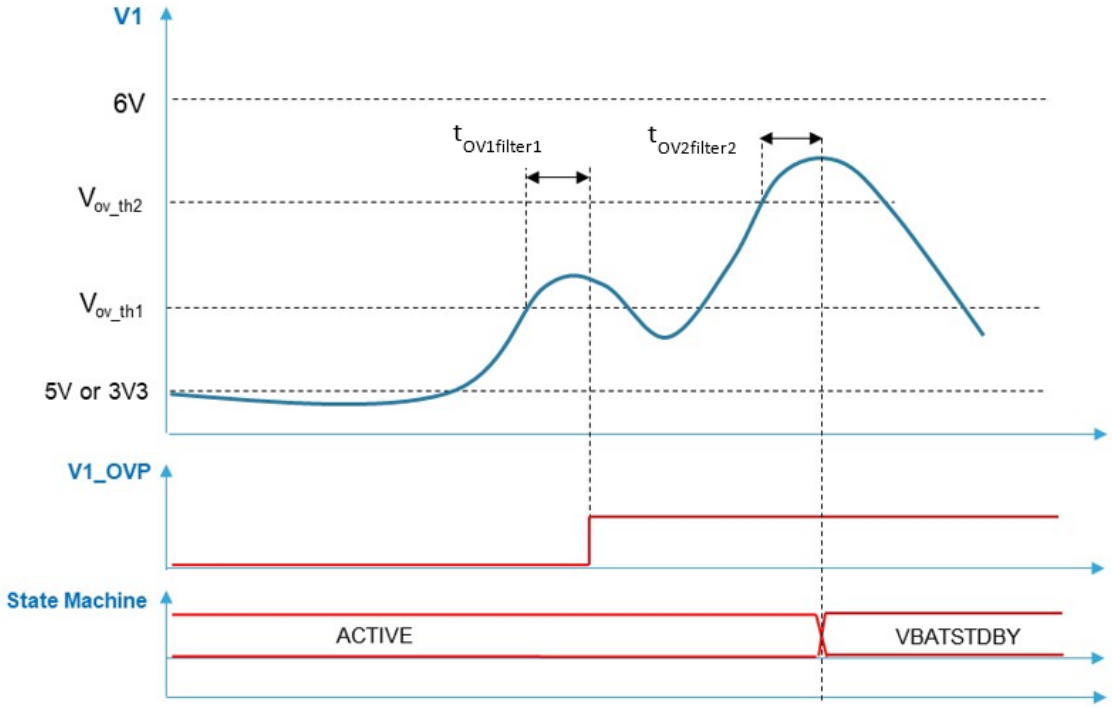
Two thresholds run the overvoltage event.

When SPSB081 detects an overvoltage event on the V1 pin:

- If $V1_{OV\_TH1} \leq V1 < V1_{OV\_TH82}$ → V1_OV status flag is raised after $t_{FILTER1}$ and in the same time NINT is pulled low for 56 µs.
- If $V1_{OV\_TH82} \leq V1 < 6.5$ V → It causes a non recoverable failure and the device is forced to V_{BAT} standby mode (V1 is switched OFF and FORCED_SLEEP_V1OV (SR2) is raised after $t_{OV1FILTER2}$). The internal pull-down transistor which will discharge the decoupling capacitor through the $R_{DISCHARGE}$ is activated

If the V_{BAT} stdby is caused by an output overvoltage on V1, the status flag stays set (V1_OV = 1).

Figure 17. **Overvoltage detection V1 = 5 V**



3.11 LIN bus interfaces (only for SPSB0815 and SPSB0813)

3.11.1 Features

- LIN ISO 17987-4/2016 compliant transceiver
- Meet OEM hardware requirements for CAN and LIN FR-Interfaces (version 1.3 2012)
- Data rate up to 20 kbit/s
- GND disconnection fail-safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Microcontroller interface with CMOS compatible I/O pins
- Internal pull-up resistor
- Transients immunity and ESD according to ISO 7637-2, ISO 62215-3 and EN/IEC 61000-4-2.
- Matched output slopes and propagation delay
- Wake up behavior according to LIN2.2a and ‘Hardware requirements for LIN, CAN and flexray interfaces (version 1.3)

At V_{SREG} > V_{POR} (that is, V_{SREG} power-on reset threshold), the LIN transceiver is enabled.

The LIN transmitter is disabled in case of the following errors:

- Dominant TxD_L time out
- LIN permanent recessive
- Thermal shutdown 1
  - with thermal sensor “global” in mode “no cluster”

or with thermal sensor “Th_CL4” in mode “cluster”

- V_{SREG} overvoltage/undervoltage
- V1 undervoltage

The LIN receiver is not disabled in case of any failure condition (it is reactivated in case of FS by thermal shutdown).

3.11.2 Error handling

The device LIN transceiver provides the following three error handling features.

3.11.2.1 Dominant TXD_L time out

If TXD_L is in dominant state (low) for t > $t_{DOM(TXDL)}$ the transmitter is disabled, the related status bit LIN_TXD_DOM (SR2) is set.

The transmitter remains disabled until the status bit is cleared.

The TXD dominant timeout detection can be disabled via SPI (LIN_TXD_TOUT_EN = 0).

3.11.2.2 Permanent recessive

If TXD_L changes to dominant (low) state but RXD_L signal does not follow within t < t_{LIN} the transmitter is disabled, the status bit LIN_PERM_REC (SR2) is set.

The transmitter remains disabled until the status bit is cleared.

3.11.2.3 Permanent dominant

If the bus state is dominant (low) for t > $t_{DOM(BUS)}$ a bus permanent dominant failure is detected. The status bit LIN_PERM_DOM (SR2) is set.

The transmitter is not disabled.

3.11.3 Wake-up from standby modes

In low power modes (V1_standby mode and VBAT_standby mode) the SPSB081 can receive two types of wake-up signals from the LIN bus (configurable by SPI bit LIN_WU_config):

- Recessive-Dominant-Recessive pattern with t > t_{DOM_LIN} (default, according to LIN ISO 17987-4/2016)

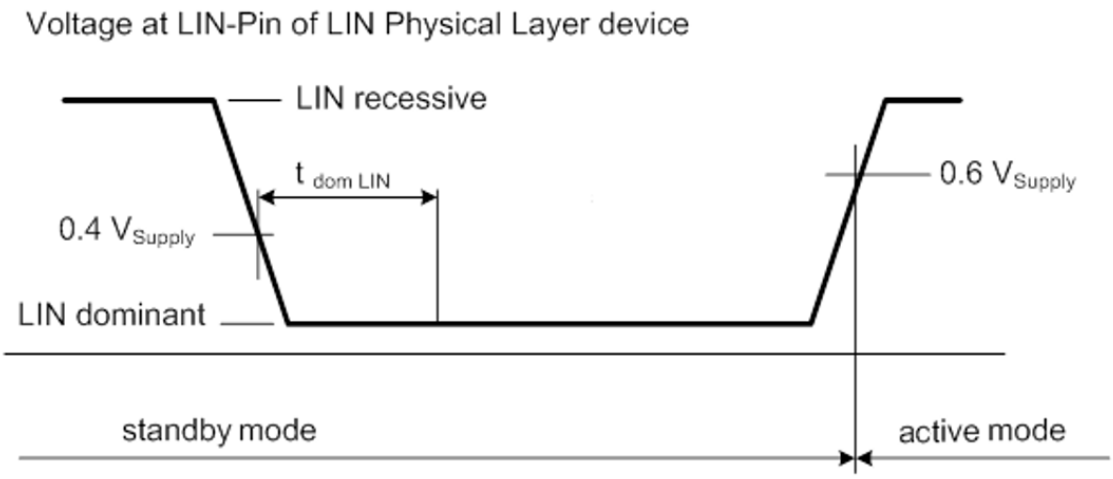
A dominant time of at least 150 µs must be identified as a wake-up. Shorter dominant times may wake up the device.

- State change recessive-to-dominant or dominant-to-recessive (according to LIN ISO 17987-4/2016)

Note: Dominant levels having duration less than a glitch filter time (it is defined 28 µs minimum, according to OEM requirements version 1.3) have to be filtered and therefore they cannot wake up the device.

3.11.3.1 Pattern wake-up (default)

Figure 18. Wake-up behavior according to LIN ISO 17987-4/2016



3.11.3.2 *Status change wake-up - Recessive-to-dominant*

Normal wake-up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for t_{LINBUS} switches the device to active mode.

3.11.3.3 *Status change wake-up - Dominant-to-recessive*

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t_{LINBUS}, switches the device to active mode.

3.12 CAN FD bus transceiver

3.12.1 Features

- ISO 11898-2:2016 compliant
- CAN-FD cell has been designed according to “Hardware requirements for transceivers (version 1.3)”
- Listen mode (transmitter disabled)
- SAE J2284 compliant
- Supported bitrates of at least 2 Mb/s for operation (5 Mb/s max bit rate)
- Function range from -27 V to +40 V DC at CAN pins.
- GND disconnection fail-safe at module level.
- GND shift operation at system level.
- Microcontroller interface with CMOS compatible I/O pins.
- ESD and transient immunity according to ISO7637 and EN/IEC61000-4-2
- Matched output slopes and propagation delay

3.12.2 CAN transceiver supply

The two low drops out voltage regulators (V1 and V2) are able to supply the CAN FD transceiver when configured as a 5 V LDO (see Table 6).

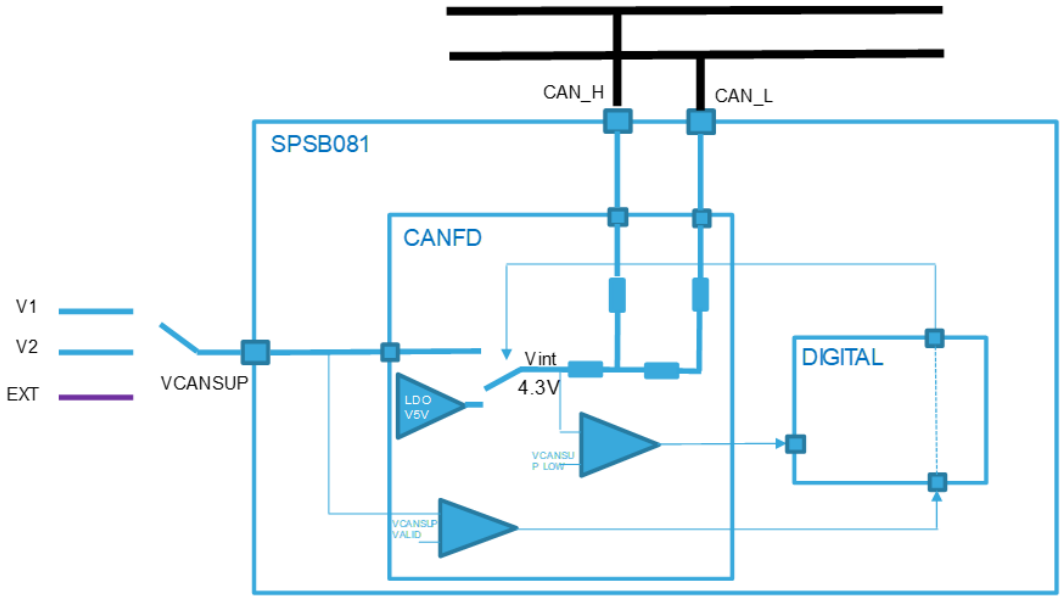
CAN FD supply is monitored, only in active mode, assuring the properly rail:

- If $V_{CANSUP} < V_{CANSUPLOW}$ then after the filter time $t_{CANSUPVALID}$
  - CAN_SUP_LOW flag is set to 1
  - CAN bus is biased by internal regulator
  - The transmitter is disabled
- When V_{CANSUP} pin > $V_{CANSUPVALID}$ then after the filter time $t_{CANSUPVALID}$
  - CAN_SUP_LOW flag can be cleared
  - CAN bus is biased by VCANSUP pin
  - The transmitter is enabled.

When V_{CANSUP} is connected to V2, and V2 is OFF during standby mode, the CAN_SUP_LOW flag is triggered when the device wakes up and goes back in ACTIVE mode.

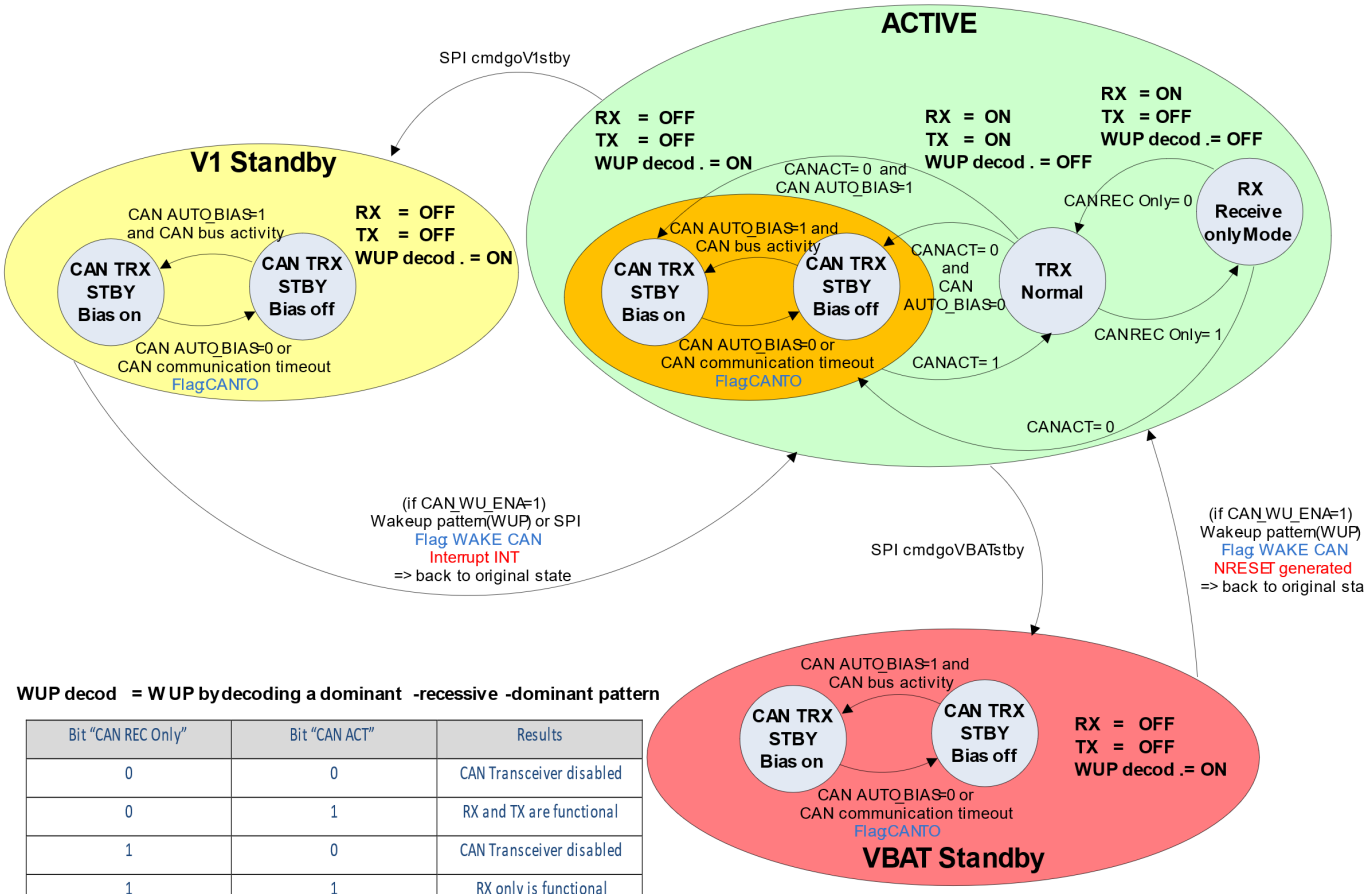
When V_{CANSUP} is connected to V1, and the device is put in VBAT_standby mode, the CAN_SUP_LOW flag is triggered when the device wakes up and goes back in ACTIVE mode.

Figure 19. **CANFD transceiver supply**



3.12.3 CAN transceiver operating modes

Figure 20. Transceiver state diagram



WUP decod = WUP by decoding a dominant -recessive -dominant pattern

Bit "CAN REC Only"	Bit "CAN ACT"	Results
0	0	CAN Transceiver disabled
0	1	RX and TX are functional
1	0	CAN Transceiver disabled
1	1	RX only is functional

TRX normal mode

Full functionality of the CAN-FD transceiver is available (transmitter and receiver) and the automatic voltage biasing is enabled.

State transitions from TRX normal mode to VBAT_Standby mode and V1_Standby mode are possible. No interrupt is generated in this mode.

CAN TRX STBY mode

The CAN-Transmitter is disabled in this mode and the RxD_C pin is kept at high (recessive) level. CAN-Receiver is capable of detecting a wake-up pattern (WUP). In V1_standby mode and VBAT_Standby mode, a WUP is indicated to the microcontroller by an interrupt signal.

There is no automatic state transition into TRX normal mode in case of a detected CAN wake up signal (WUP). In active mode, the microcontroller can initiate a state transition into TRX normal mode by setting the SPI bit CAN_ACT to '1' and can start communication after TBias.

Moreover, in this mode two further submodes are possible ("Bias ON" or "Bias OFF"), depending on CAN_AUTO_BIAS bit (compliant with ISO 11898-2:2016) or timeout conditions. In any case, when entering CAN TRX STBY mode, transition is always to the state "Bias ON".

3.12.4 CAN error handling

The devices provide the following four error handling features.

After power-on reset (V_{SREG} > V_{POR}), the CAN transceiver is disabled. The transceiver is enabled by setting CAN_ACT = 1.

The CAN transmitter is disabled automatically in case of the following errors:

- Dominant TxD_C time out
- CAN permanent recessive
- RxD_C permanent recessive
- Thermal shutdown 1
- Can supply low

The CAN receiver is not disabled in case of any failure condition.

3.12.4.1 *Dominant TXDC time out*

If TXD_C is in a dominant state (low) for t > $t_{DOM(TXDC)}$ the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI (CAN_TXD_ DOM in SR2). The transmitter remains disabled until the status register is cleared.

3.12.4.2 *CAN bus permanent recessive*

If TXD_C changes to dominant (low) state but CAN bus does not follow for four times, the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI (CAN_PERM_REC in SR2). The transmitter remains disabled until the status register is cleared.

3.12.4.3 *CAN Permanent dominant*

If the bus state is dominant (low) for t > t_{CAN} a permanent dominant status will be detected. The status bit will be latched and can be read and optionally cleared by SPI (CAN_PERM_DOM in SR2). The transmitter will not be disabled.

3.12.4.4 *RXDC permanent recessive*

If RXD_C pin is clamped to a recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXD_C does not follow TXD_C for four times the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI (CAN_RXD_REC in SR2). The transmitter remains disabled until the status register is cleared.

3.12.5 Wake-up by CAN

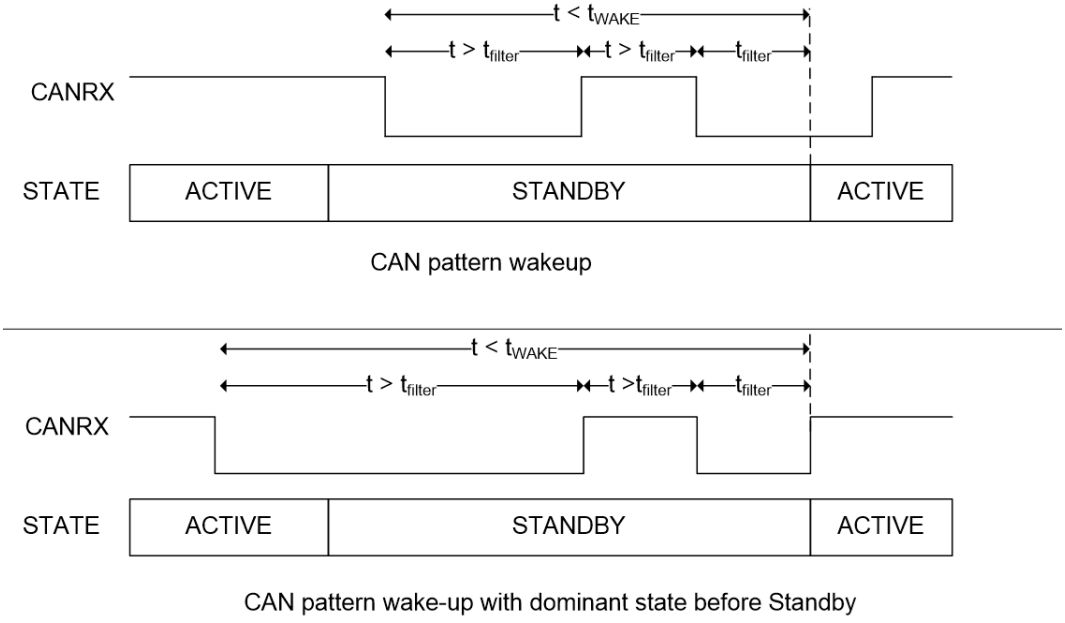
The default setting for the wake-up behavior after power-on reset is the wake-up by regular communication on the CAN bus. When the CAN transceiver is in a standby mode (CAN TRX STBY), the device can be woken-up by sending two consecutive dominant bits separated by a recessive bit.

For any activity on the CAN, CAN pattern wake-up option is enabled and the CAN transceiver was set in standby mode (CAN TRX STBY) while CAN bus was in recessive state or dominant state. In order to wake up the device, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than t_{filter}.
- The distance between two pulses must be longer than t_{FILTER}.
- The two pulses must occur within a time frame of t_{WAKE}.
- Wake-up occurs when the duration of a second pulse becomes longer than t_{FILTER}.

Note: A wake-up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

Figure 21. **CAN wake up capabilities**



Note: The figure above illustrate the wake-up behavior from V1_standby mode. For wake-up from VBAT_standby mode the NRESET signal (with 2 ms timing) is generated instead of the RXD_L (interrupt) signal.

3.12.6 CAN receive only mode

During TRX normal mode, with the CAN _REC_ONLY bit in CR1 it is possible to disable the CAN transmitter. In this mode it is possible to listen to the bus but not to send to it. The receiver termination network is still activated in this mode.

3.12.7 CAN looping mode

If the CAN_LOOP_EN (configuration register) is set, the TxD_C input is mapped directly to the RxD_C pin. This mode can be used in combination with the CAN receive-only mode, to run diagnosis for the CAN protocol handler of the microcontroller.

Note: To guarantee the correct behavior of the CAN_FD transceiver and to get its optimized electrical performances, the VCANSUP pin must be connected to V1, V2, or Vext pin (see Table 6).

3.13 Power supply fail

3.13.1 V_S supply failure

V_S overvoltage

If the supply voltage V_S reaches the over voltage threshold V_{SOV}:

- LIN remains enabled
- CAN remains enabled
- OUT1, OUT2, OUT3, and OUT4 are turned off (default).
  The shutdown of outputs may be disabled by SPI (VS_OV_SD_EN (CR3) = 0)
- Recovery of outputs after over-voltage condition is configurable by SPI:
  - VS_LOCK_EN (CR3) = 1: Outputs are off until read and clear VS_OV (SR2).
  - VS_ LOCK_EN (CR3) = 0: Outputs turned on automatically after V_S over-voltage condition has recovered.

- The overvoltage bit VS_OV (SR2) is set and can be cleared with a ‘read and clear’ command. The overvoltage bit is reset automatically if VS_LOCK_EN (CR3) = 0 and the overvoltage condition has recovered.

V_S undervoltage

If the supply voltage V_S drops below the under voltage threshold voltage (V_{SUV}):

- LIN remains enabled
- CAN remains enabled

Note: The functionality is not guaranteed in the range $V_{POR} < V_{SREG} < V_{SREGUV}$

- OUT1, OUT2, OUT3, and OUT4 are turned off (default). The shutdown of outputs may be disabled by SPI (VS_UV_SD_EN (CR3) = 0)
- Recovery of outputs after undervoltage condition is configurable by SPI:
  - VS_LOCK_EN (CR3) = 1: Outputs are off until read and clear VS_UV (SR2)
  - VS_LOCK_EN (CR3) = 0: Outputs turned on automatically after V_S undervoltage condition has recovered.
- The undervoltage bit (VSUV) is set and can be cleared with a ‘read and clear’ command. The undervoltage bit is removed automatically if VS_ LOCK_EN = 0 and the undervoltage condition has recovered.

3.13.2 V_{SREG} supply failure

V_{SREG} overvoltage

If the supply voltages V_{SREG} reaches the overvoltage threshold V_{SREGOV}:

- LIN is switched to high impedance (RX is still on)
- CAN remains enabled
- The over voltage bit VSREG_OV (SR2) is set and can be cleared with a ‘read and clear’ command. The overvoltage bit is reset automatically if VSREG_ LOCK_EN (CR3) = 0 and the overvoltage condition has recovered.

V_{SREG} undervoltage

If the supply voltage V_{SREG} drops below the under voltage threshold voltage (V_{SREG_UV}):

- LIN is switched to high impedance (RX is still on).

Note: The functionality is not guaranteed in the range $V_{POR} < V_{SREG} < V_{SREGUV}$

- CAN remains enabled
- The undervoltage bit (VSREG_UV (SR2) is set and can be cleared with a ‘read and clear’ command. The undervoltage bit is removed automatically if VSREG_LOCK_EN (CR3) = 0 and the undervoltage condition has recovered.

3.14 Thermal state machine

Figure 22. **Thermal shutdown protection and diagnosis related to thermal cluster 1**

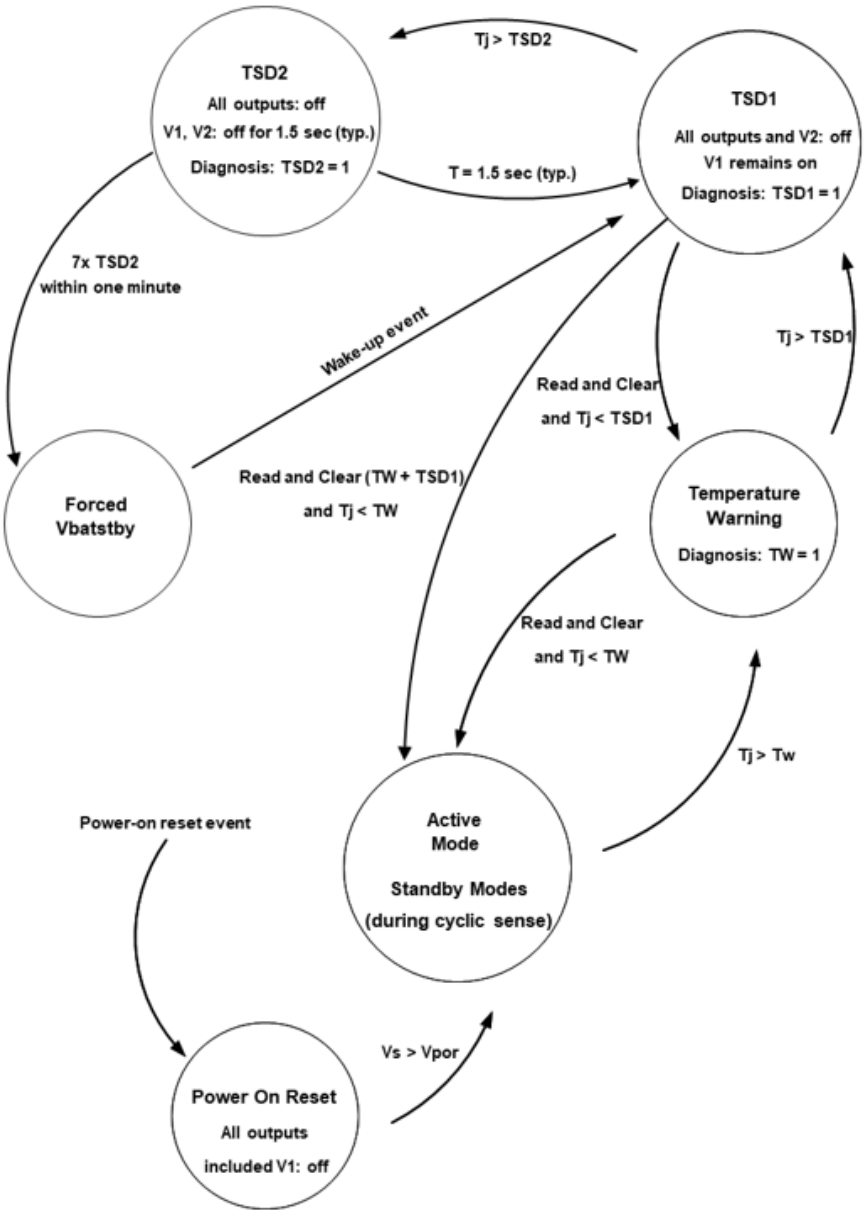
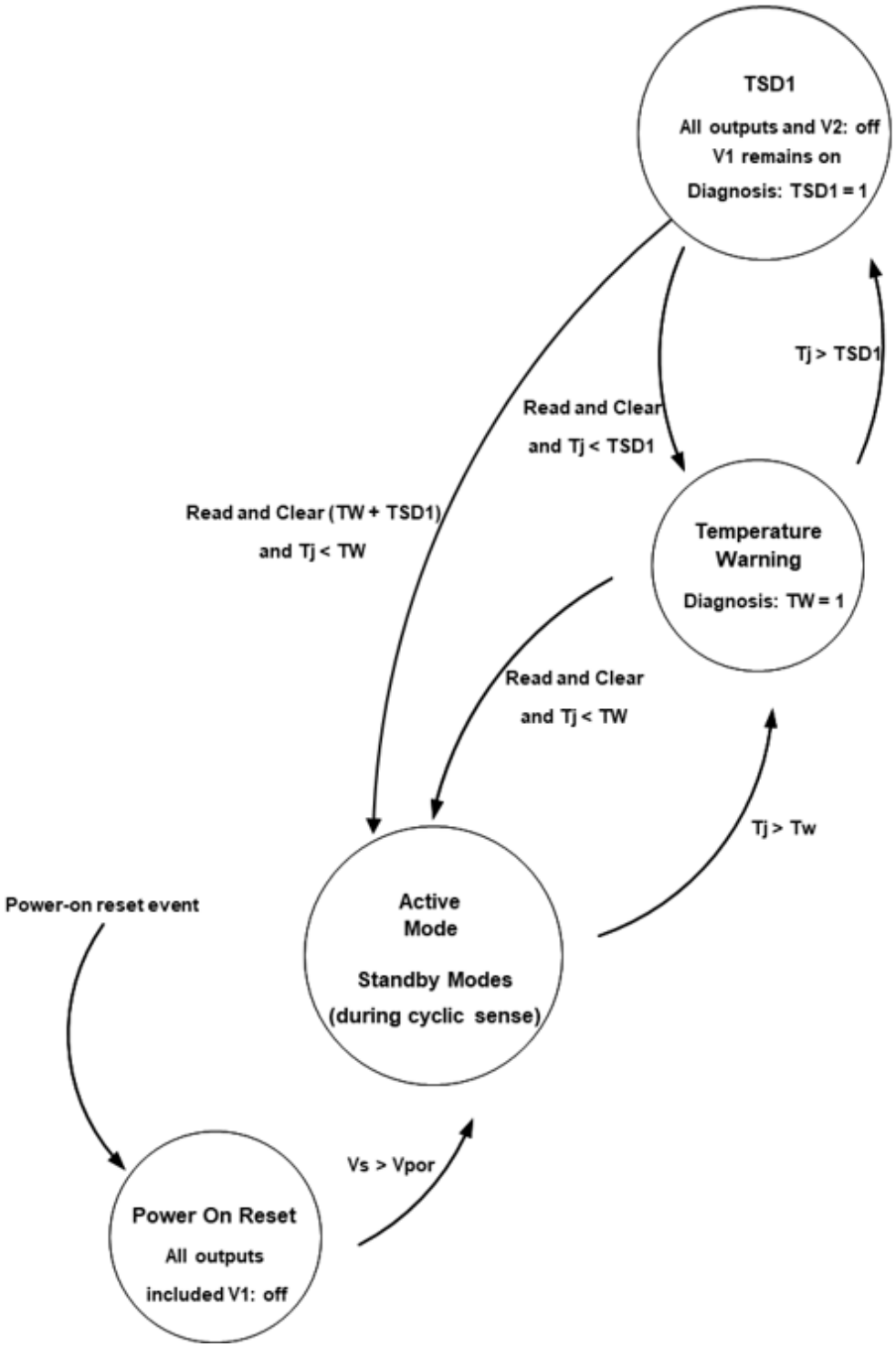


Figure 23. **Thermal shutdown protection and diagnosis related to thermal cluster 2, 3 and 4**



Note: The thermal state machine recovers the same state where it was before entering standby mode. In case of a TSD2 it enters TSD1 state.

3.15 Power outputs OUT1..4

The component provides a total of four standalone high side outputs OUT1, OUT2, OUT3, and OUT4 to drive, for example, LED's or to supply contacts. OUT1, OUT2, OUT3, and OUT4 are supplied by VS. OUT1, OUT2, OUT 3 and OUT4 are intended to be used as contact supply and can be activated in standby modes.

All high side outputs switch off in case of:

- VS overvoltage and undervoltage (depending on configuration, see Section 3.13 Power supply fail)
- Overcurrent (only the impacted high-side)
- Overtemperature (TSD1)
- Fail-safe event
- Loss of ground at SGND pin

In the case of overcurrent or overtemperature (TSD1 (SR1)) condition, the drivers will switch off. The related status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case of overvoltage and undervoltage conditions, the drivers are switched off. The relative status bit is latched and can be read and optionally cleared by SPI. If the VS_LOCK_EN bit is set to '1', the drivers remain off until the status is cleared. If the VS_LOCK_EN bit is set to '0', the drivers switch on automatically if the error condition disappears. Under-voltage and over-voltage shutdown can be disabled by setting < VS_UV_SD_EN > respectively < VS_OV_SD_EN > to '0'. In case of open load condition, the appropriate status register (in SR4) is set. The status can be read and optionally cleared by SPI. The high side outputs are not switched off in case of open load condition.

Note: The maximum voltage and current applied to the high-side outputs are specified in the 'absolute maximum ratings'. Appropriate external protection may be required in order to respect these limits under application conditions.

Each of the standalone high-side driver outputs OUT1..4 can be also driven either with an internal generated PWM signal or with an internal timer. OUT1..4 can be also directly driven with DIR/WU2 pin.

3.16 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open- load detection threshold (IOLDx) for at least t_{FOL} the corresponding open-load bit is set in the status register.

3.17 Overcurrent detection

In the case of an overcurrent condition, a status flag is set in the corresponding status register. If the overcurrent signal is valid for at least t_{BLK}, the overcurrent flag is set and the corresponding driver switches off to reduce the power dissipation and to protect the integrated circuit. If the overcurrent recovery bit of the output is cleared, the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.18 Current monitor

The current monitor sources a current image of the power stage output current at the current monitor pin, which has fixed ratio (I_{CMR} refer to Table 34) of the instantaneous current of the selected high-side driver. The signal at output CM is blanked after switching on the driver until correct settlement of the circuitry. The bits CM_SEL_x (CR6) define which of the outputs is multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open or overload condition. The current monitor output is enabled after the current-monitor blanking time, when the selected output is switched on. If this output is off, the current monitor output is in high-impedance mode. The current monitor can be turned on or off by selecting the corresponding setting for the CM on/off bit.

3.19 Constant current mode

For the OUT1, OUT2, OUT3, and OUT4 high-side drivers, it is available the CCM (constant current mode) feature, which is conceived to provide a constant current to the related output. The CCM feature is configurable via SPI, by setting the OUTx_CCM_EN bit (x = 1, 2, 3, 4) in CR20; these bits can be set only if the related driver is in OFF state and when the CCM is enabled, the overcurrent and short circuit detection of the related output is switched OFF while its open load detection is always ON.

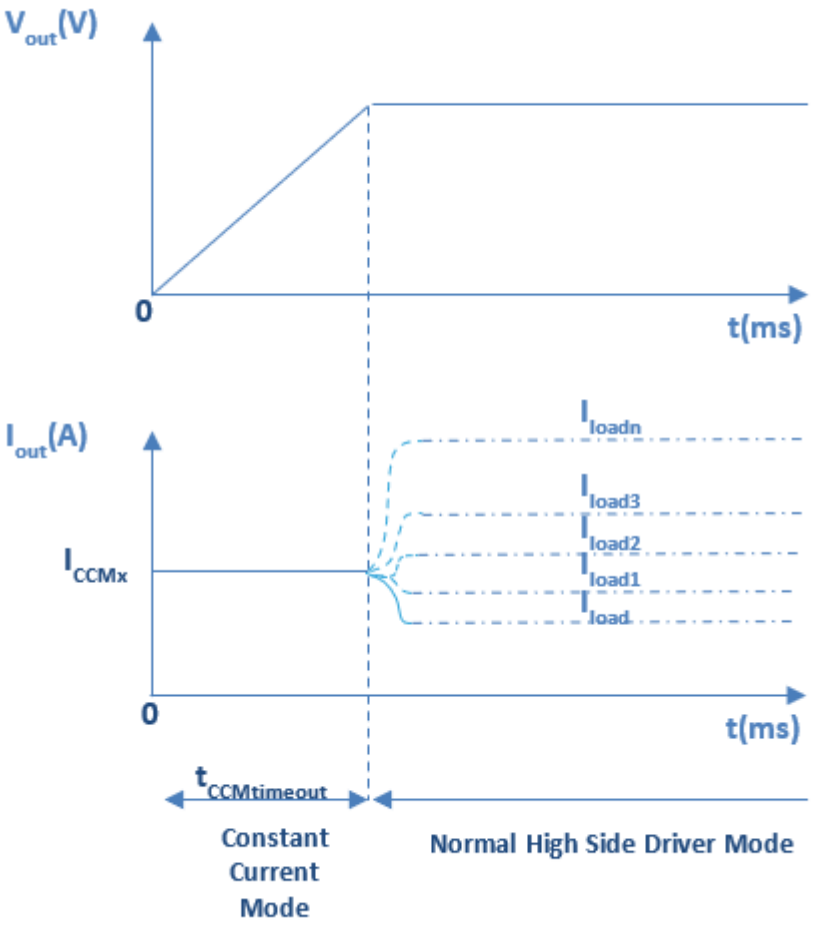
The CCM is automatically disabled after an expiration time $t_{CCMTIMEOUT}$.

The allowed sequences are:

- Set OUTx_CCM_EN bit, then turn ON the related driver by SPI (the other configurations of the OUTx_y in CR5 are ignored): driver starts in CCM for $t_{CCMTIMEOUT}$, then it switches to ON mode and the OUTx_CCM_EN bit is automatically cleared;
- If OUTx_CCM_EN = 1, after driver has been started in ON, PWM, timer modes then CCM bit is ignored;
- If OUTx_CCM_EN bit is cleared by the microcontroller before timeout, then the driver is switched to ON mode.

The short-circuit and overcurrent detection are enabled in ON, PWM, timer and DIR modes, but not in constant current mode. The default value for the OUTx_CCM_EN bit is 0, that is, the CCM is disabled by default.

Figure 24. Constant current mode



3.20 Temperature warning and shutdown

If any of the cluster junction temperatures rises above the temperature warning threshold ($T_{W\ ON}$), a temperature warning flag is set after the temperature warning filter time (t_{FTJTW}) and can be read via SPI. If the junction temperature increases above the temperature shutdown threshold ($T_{SD1\ OFF}$), the thermal shutdown bit is set and the power transistors of all output stages are switched off to protect the device after the thermal shutdown filter time. The temperature warning and thermal shutdown flags are latched and must be cleared by the microcontroller. This is done by a read and clear command on the relevant status register (TSD1 is bit 4 in status register 1 while TW is bit 8 in status register 2).

After these bits have been cleared, the output stages are reactivated. If the temperature is still above the thermal warning threshold, the thermal warning bit is set after t_{FTJTW}. Once this bit is set and the temperature is above the temperature shutdown threshold, temperature shutdown is detected after t_{FTJTW} and the outputs are switched off. Therefore, the minimum time after which the outputs are switched off after the bits have been cleared in case the temperature is still above the thermo shutdown threshold is twice the thermo warning/shutdown filter time t_{FTJTW}.

3.21 Thermal clusters

To provide an advanced on-chip temperature control, the power outputs are grouped in four clusters with dedicated thermal sensors. The sensors are suitably located on the device. In case the temperature of a cluster reaches the thermal shutdown threshold, the outputs assigned to this cluster are shut down (all other outputs remain active). Each output cluster has a dedicated temperature warning and shutdown flag (SR7 and SR8). Hence, the thermal cluster concept identifies a group of outputs in which one or more channels are in overload condition.

If thermal shutdown has occurred within an output cluster, or if temperature is rising within a cluster, it may be desired to identify which of the output(s) is (are) determining the temperature increase.

Thermal clusters can be configured using bit TSD_CLUSTER_EN (CR20):

- Standard mode (default): as soon as any cluster reaches thermal threshold the device is switched off. V1 regulator remains on and is switched off reaching TSD2.

All the thermal sensors are put in “OR”.

In fact, if one of these sensors reaches TSD1:

- All outputs drivers and V2 are turned OFF. V1 remains on until TSD2.LIN and CAN transmitter are turned OFF (but they are forced in "receive only" mode).
- Cluster mode: only the cluster, which reached shutdown temperature is switched off.

In case cluster Th_CL1 reaches TSD1:

- V1 remains ON until TSD2

In case cluster Th_CL4 reaches TSD1.

- All outputs drivers and V2 are turned OFF. V1 remains on until TSD2.
- LIN and CAN transmitter are turned OFF (but they are forced in "receive only" mode).

Figure 25. **Thermal clusters identification**

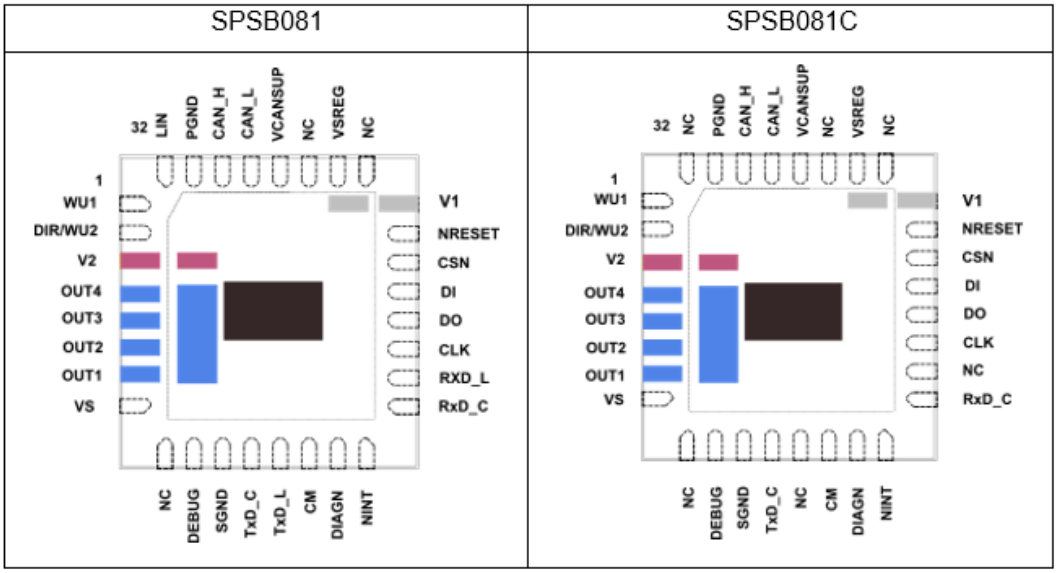


Table 11. **Thermal cluster definition**

Th_CL1	Th_CL2	Th_CL3	Th_CL4
V1	V2	OUT1, OUT2, OUT3, OUT4	Global
TW and TSD1, TSD2	TW and TSD1	TW and TSD1	TW and TSD1

3.22 Functional safety management

Even if not designed as safety HW element, the device contains some features that can be used to support application that needs to fulfill functional safety requirements. Analysis of the IC's capability to reach the required safety level, should be made at system level under user responsibility.

The following device safety requirements have been considered for a typical application:

Table 12. **Safety requirement**

ID	Description
TSR1	SPSB081 shall guarantee the correct operation of the voltage regulator V1 as specified in datasheet.
TSR2	SPSB081 shall guarantee the correct operation of the voltage regulator V2 as specified in datasheet.
TSR3	SPSB081 shall assert the NRESET signal in case of WD failure.
TSR4	The SPI interface embedded in SPSB081 shall provide to microcontroller device diagnostic info.
TSR5	SPSB081 shall guarantee the correct functionality of HSD(s) as for the datasheet specification.
TSR6	SPSB081 shall ensure LIN physical layer operation as defined in datasheet.
TSR7	SPSB081 shall ensure CAN FD physical layer operation as defined in datasheet.

More details about functional safety can be found in the device safety manual, provided on customer request.

4 Serial peripheral interface (SPI)

A 32-bit SPI is used for bidirectional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-Pin reflects the global error flag (fault condition) of the device.

- Chip select not (CSN)

  The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

  If CSN = low for t > $t_{CSNFAIL}$, the DO output is switched to high impedance in order not to block the signal line for other SPI nodes.

- Serial data in (DI)

  The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to data input register. The writing to the selected data input register is only enabled if exactly 32 bits are transmitted within one communication frame (that is, CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality, a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

- Serial data out (DO)

  The data output driver is activated by a logical low level at the CSN input and it goes from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

- Serial clock (CLK)

  The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK frequency up to 10 MHz.

4.1 ST-SPI

The ST-SPI is a standard used in ST automotive ASSP devices.

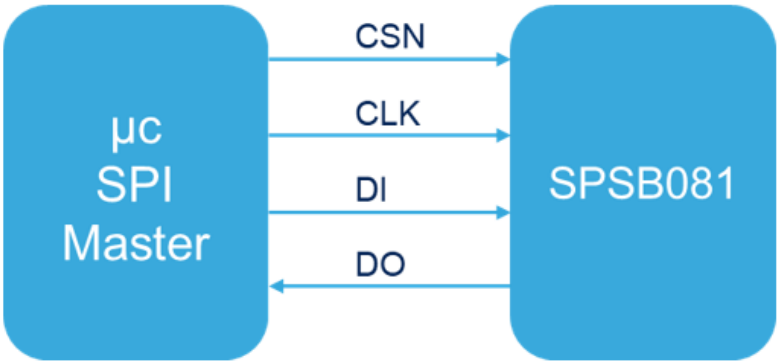
This chapter describes the SPI protocol standardization. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, fail-safe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

The device serial peripheral interface is compliant to the ST-SPI standard.

4.1.1 Physical layer

Figure 26. **SPI pin description**



4.2 Signal description

Chip select not (CSN)

The communication interface is de-selected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication starts and stops the serial clock (SCK) has to be logically low. The serial data out (SDO) is in high impedance when CSN is high or a communication timeout was detected.

Serial clock (SCK)

This SCK provides the clock of the SPI. Data present at serial data input (SDI) is latched on the rising edge of serial clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to serial data out (SDO).

Serial data input (SDI)

This input is used to transfer data serially into the device. Data is latched on the rising edge of serial clock (SCK).

Serial data output (SDO)

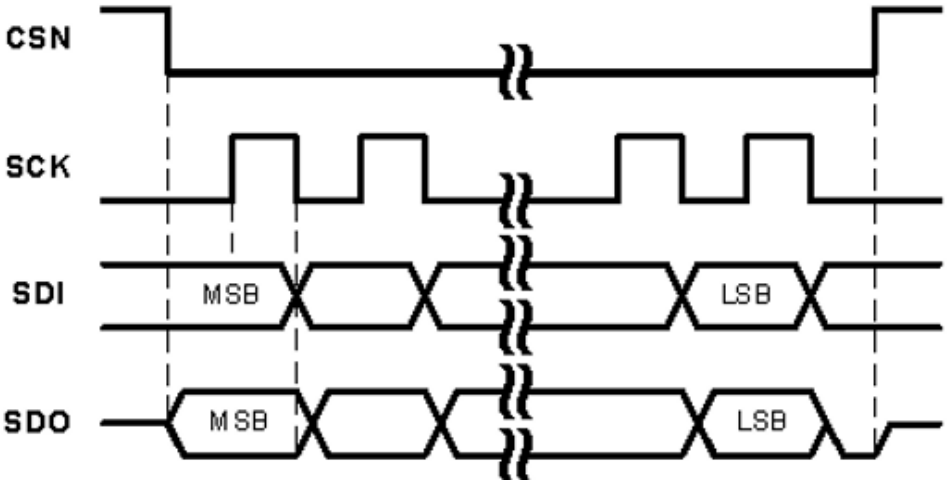
This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (SCK).

4.2.1 Clock and data characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in following mode:

- CPOL = 0
- CPHA = 0

Figure 27. **SPI signal description**



The communication frame starts with the falling edge of the CSN (communication start). SCK has to be low.

The SDI data is then full latched following the rising SCK edges into the internal shift registers.

After communication start the SDO leaves 3-state mode and presents the MSB of the data shifted out to SDO, it is then full latched following the falling SCK edges data and it is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication has taken place (for example, correct number of SCK cycles, access to a valid address), the requested operation according to the operating code will be performed (write or clear operation).

4.2.2 Communication protocol

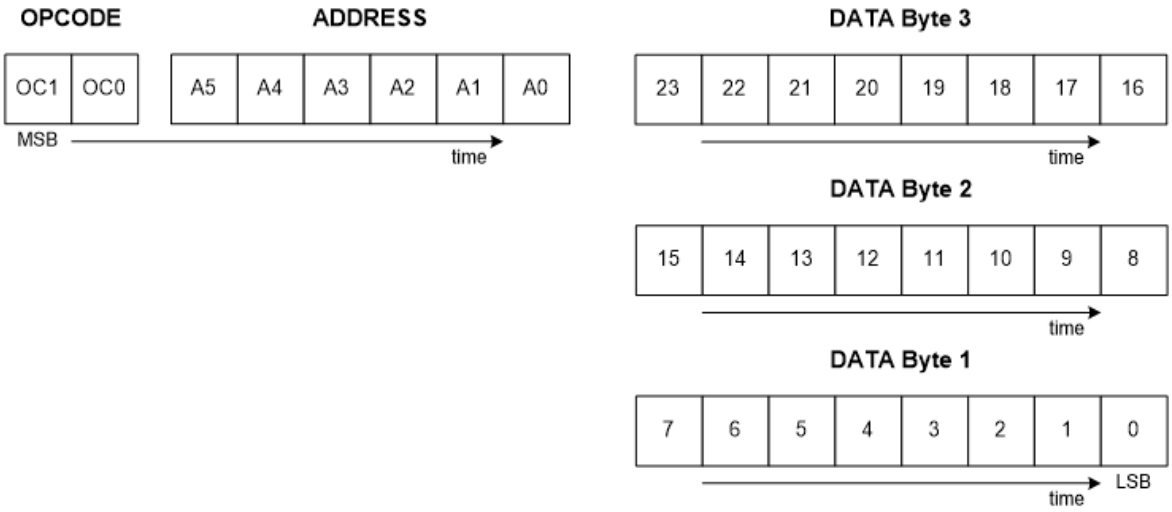
4.2.2.1 SDI frame

The devices data-in frame consists of 32 bits (OpCode (2 bits) + address (6 bits) + data byte 3 + data byte 2 + data byte 1).

The first two transmitted bits (MSB, MSB-1) contain the operation code which represents the instruction, which is performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation is performed.

The subsequent bytes contain the payload.

Figure 28. **SDI frame**



4.2.2.2 *Operating code*

The operating code is used to distinguish between different access modes to the registers of the slave device.

Table 13. Operation codes

OC1	OC0	Description
0	0	Write operation
0	1	Read operation
1	0	Read and clear operation
1	1	Read device information

A **write operation** leads to a modification of the addressed data by the payload if a write access is allowed (for example, control register, valid data). Beside this a shift out of the content (data present at communication start) of the registers is performed.

A **read operation** shifts out the data present in the addressed register at communication start. The payload data is ignored and internal data are not modified. In addition, a burst read can be performed.

A **read and clear** operation leads to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to '1'. Beside this a shift out of the content (data present at communication start) of the registers is performed.

Note: Status registers, which change status during communication could be cleared by the actual read and clear operation and are not reported in actual communication or in the following communications. To avoid a loss of any reported status, that it is recommended just clear status registers, which are already reported in the previous communication (selective bitwise clear).

4.2.2.3 *Advanced operation codes*

To provide beside the separate write of all control registers and the bitwise clear of all status registers, two advanced operation codes can be used to set all control registers to the default value and to clear all status registers.

A 'set all control registers to default' command is performed when an OpCode '11' at address b'111111 is performed.

Note: Please consider that potential device specific write protected registers cannot be cleared with this command as therefore a device power-on-reset is needed.

A 'clear all status registers' command is performed when an OpCode '10' at address b'111111 is performed.

4.2.2.4 *Data-in payload*

The payload (data byte 1 to data byte 3) is the data transferred to the device with every SPI communication. The payload always follows the OpCode and the address bits.

For write access the payload represents the new data written to the addressed register. For read and clear operations the payload defines which bits of the addressed status register is cleared. In case of a '1' at the corresponding bit position the bit will be cleared.

For a read operation, the payload is not used. For functional safety reasons it is recommended to set unused payload to '0'.

4.2.2.5 *SDO frame*

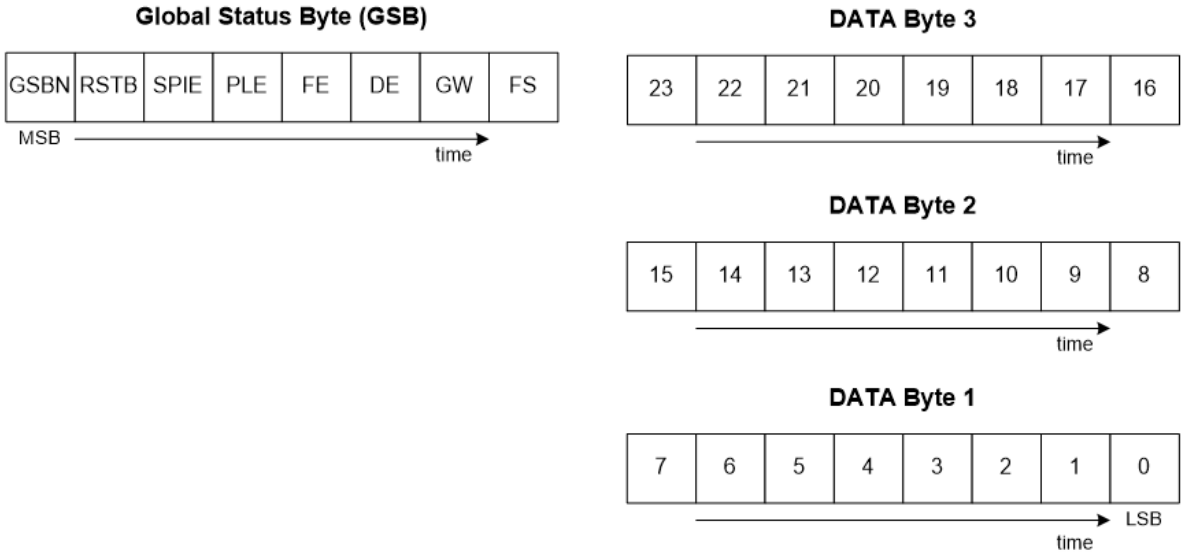
The data-out frame consists of 32 bits (GSB + data byte 1 to 3).

The first eight transmitted bits contain device related status information and are latched into the shift register at the time of the communication start. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive SCK edge.

This could lead to an inconsistency of data between the GSB and payload due to different shift register load times. Anyhow, no unwanted status register clear should appear, as status information should just be cleared with a dedicated bit clear after.

Figure 29. **SDO frame**



4.2.2.6 *Global status byte (GSB)*

The bits (Bit0 to Bit4) represent a logical OR combination of bits located in the status registers. Therefore, no direct read & clear can be performed on these bits inside the GSB.

Table 14. **Global status byte**

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS

Global status bit not (GSBN)

The GSBN is a logically NOR combination of bit 24 to bit 30. This bit can also be used as *global status flag* without starting a complete communication frame as it is present directly after pulling CSN low.

Reset bit (RSTB)

The RSTB indicates a device reset. In case this bit is set, specific internal control registers are set to default and kept in that state until the bit is cleared.

The RSTB bit is cleared after a read and clear of all the specific bits in the status registers, which caused the reset event.

SPI error (SPIE)

The SPIE is a logical OR combination of errors related to a wrong SPI communication.

Physical layer error (PLE)

The PLE is a logical OR combination of errors related to the LIN and CAN FD transceivers.

Functional error (FE)

The FE is a logical OR combination of errors coming from functional blocks (for example, high-side over current).

Device error (DE)

The DE is a logical OR combination of errors related to device specific blocks (for example, V_S over voltage, over temperature.

Global warning (GW)

The GW is a logical OR combination of warning flags (for example, thermal warning).

Fail-safe (FS)

The FS bit indicates that the device was forced into a safe state due to mistreatment or fundamental internal errors (for example, watchdog failure, voltage regulator failure).

4.2.2.7 *Data-out payload*

The payload (data bytes 1 to 3) is the data transferred from the slave device with every SPI communication to the master device. The payload always follows the OpCode and the address bits of the actual shifted in data (in-frame-response).

4.3 Address definition

Table 15. Device application access

Operating code	
OC1	OC0
0	0
0	1
1	0

Table 16. RAM address range

RAM address	Description	Access
3FH	Configuration register	R/W
38H	Status register 8	R/C
…	…	-
32H	Status register 2	R/C
31H	Status register 1	R/C
…	…	-
22H	Control register 34	R/W
18H	Control register 24	R/W
…	…	-
02H	Control register 2	R/W
01H	Control register 1	R/W
00H	Reserved	-

Table 17. Device information read access

Operating code	
OC1	OC0
1	1

Table 18. ROM address range

ROM address	Description	Access
3FH	<Advanced Op.>	W
3EH	<GSB options>	R
…	-	-
20H	<SPI CPHA test>	R
16H	<WD bit pos. 4>	R

ROM address	Description	Access
15H	<WD bit pos. 3>	R
14H	<WD bit pos. 2>	R
13H	<WD bit pos. 1>	R
12H	<WD type 2>	R
11H	<WD type 1>	R
10H	<SPI mode>	R
…	-	-
0AH	<silicon ver.>	R
…	-	-
05H	<device No.4>	R
04H	<device No.3>	R
03H	<device No.2>	R
02H	<device No.1>	R
01H	<device family>	R
00H	<company code>	R

4.3.1 Information registers

The device information registers can be read by using OpCode ‘11’. After shifting out the GSB the 8-bit wide payload is transmitted. By reading device information registers a communication width, which is minimum 16 bits plus a multiple by 8 can be used. After shifting out the GSB followed by the 8-bit wide payload a series of ‘0’ is shifted out at the SDO.

Table 19. SPSB081 information registers map

ROM address	Description	Access		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<Advanced Op.>										
3EH	<GSB options>	R	→	0	0	0	0	0	0	0	0
…	-										
20H	<SPI CPHA test>	R	→	0	1	0	1	0	1	0	1
16H	<WD bit pos. 4>	R	→	C0H							
15H	<WD bit pos. 3>	R	→	7FH							
14H	<WD bit pos. 2>	R	→	C0H							
13H	<WD bit pos. 1>	R	→	41H							
12H	<WD type 2>	R	→	91H							
11H	<WD type 1>	R	→	3CH							
10H	<SPI mode>	R	→	B0H							
…	-		→	-							
0AH	<silicon Ver.>	R	→	major revision				minor revision			
…	-		→	-							
05H	<device No.4>	R	→	50H							
04H	<device No.3>	R	→	37H							
03H	<device No.2>	R	→	52H							
02H	<device No.1>	R	→	55H							

ROM address	Description	Access		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01H	<device family>	R	→	01H							
00H	<company code>	R	→	00H							

4.3.1.1 *Device identification registers*

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD power management)

<Device No. 1>: 55H (ASCII code for U)

<Device No. 2>: 52H (ASCII code for R)

<Device No. 3>: 37H (ASCII code for 7)

<Device No. 4>: 50H (ASCII code for P)

4.3.1.2 *SPI modes*

By reading out the <SPI mode> register general information of SPI usage of the device application registers can be read.

Table 20. SPI mode register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	DL2	DL1	DL0	0	0	S1	S0
1	0	1	1	0	0	0	0

<SPI mode>: B0H (burst mode read available, 32 bit, no data consistency check).

4.3.1.3 *SPI burst read*

Table 21. Burst read bit

Bit 7	Description
0	BR not available
1	BR available

The SPI burst read bit indicates if a burst read operation is implemented. The intention of a burst read is, for example, used to perform a device internal memory dump to the SPI master.

The start of the burst read is like a normal *read operation*. The difference is, that after the SPI data length the CSN is not pulled high and the SCK is continuously clocked. When the normal SCK max count is reached (SPI data length), the consecutive addressed data is latched into the shift register. This procedure is performed every time when the SCK payload length is reached.

In case the automatically incremented address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached.

The SPI burst read is limited by the CSN low timeout.

4.3.1.4 *SPI data length*

The SPI data length value indicates the length of the SCK count monitor, which is running for all accesses to the device application registers. In case a communication frame with an SCK count is not equal to the reported one, it leads to a SPI error and the data are rejected.

Table 22. **SPI data length**

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	-
0	0	0	invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
0	1	1	32-bit SPI
-	-	-	…
1	1	1	64-bit SPI

4.3.1.4.1 Data consistency check (Parity/CRC)

Table 23. **Data consistency check**

Bit 1	Bit 0	Description
S1	S0	-
0	0	Not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

4.3.1.4.2 Watchdog definition

For further information, see also Section 3.6 Configurable window watchdog.

In case a watchdog is implemented the default settings can be read out via the device information registers.

Table 24. **WD Type/Timing**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	WD1	WD0	-					
<WD type 1/2>	0	0	Register is not used					
<WD type 1>	0	1	WT5	WT4	WT3	WT2	WT1	WT0
-	-	1	1	1	1	-	1	0
	-	-	Watchdog timeout/Long open window WT[5:0] * 5 ms					
<WD type 2>	1	0	OW2	OW1	OW0	CW2	CW1	CW0
	1	0	0	1	0	0	0	1
-	-	-	Open window OW[2:0] * 5 ms			Closed window CW[2:0] * 5 ms		
<WD type 1/2>	1	1	Invalid					

<WD type 1>: 3CH (long open window: 300 ms).

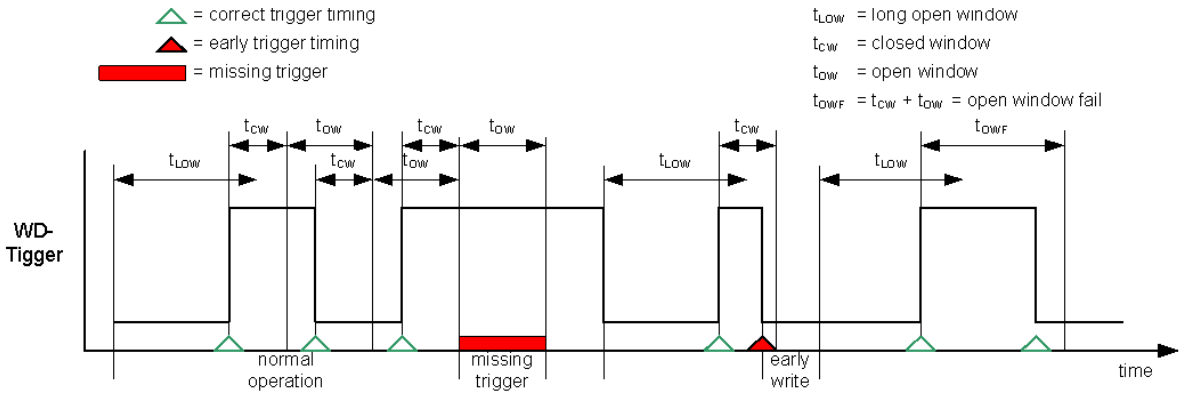
<WD type 2>: 91H (open window. 10 ms, closed window: 5 ms).

<WD type 1> indicates the long open window (timeout) which is opened at the start of the watchdog. The binary value of WT[5:0] times 5 ms indicates the typical value of the timeout time.

<WD type 2> describes the default timing of the window watchdog.

The binary value of CW[2:0] times 5 ms defines the typical closed window time (t_{CW}) and OW[2:0] times 5 ms defines the typical open window time (t_{OW}). See figure below where $t_{CW} = T_{EFW}$ and $t_{OW} = T_{LFW} - T_{EFW}$.

Figure 30. **Window watchdog operation**



The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 25. **WD bit position**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	WB1	WB0	-					
<WD bit pos. X>	0	0	Register is not used					
<WD bit pos. X>	0	1	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
<WD bit pos. 1>	0	1	0	0	0	0	0	1
<WD bit pos. 3>	0	1	1	1	1	1	1	1
			Defines the register addresses of the WD trigger bits					
<WD bit pos. X>	1	0	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
			Defines the stop address of the address range (previous <WD bit pos. X> is a WB = ‘01’) The consecutive <WD bitpos. X> has to be a WB = ‘11’					
<WD bit pos. X>	1	1	0	WBP4	WBP3	WBP2	WBP1	WBP0
<WD bit pos. 2>	1	1	0	0	0	0	0	0
<WD bit pos. 4>	1	1	0	0	0	0	0	0
				Defines the binary bit position of the WD trigger bit within the register				

<WD bit pos 1>: 41H; watchdog trigger bit located at address 01H (CR1).

<WD bit pos 2>: C0H; watchdog trigger bit location is bit0.

<WD bit pos 3>: 7FH; watchdog trigger bit located at address 3FH (config register).

<WD bit pos 4>: C0H; watchdog trigger bit location is bit0.

4.3.2 Device application registers (RAM)

The device application registers are all registers accessible using OpCode ‘00’, ‘01’ and ‘10’. The functions of these registers are defined in the device specification.

4.4 Protocol failure detection

To realize a protocol, which covers certain fail-safe requirements a basic set of failure detection mechanisms are implemented.

4.4.1 Clock monitor

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI data length, an SPIE is reported with the next command and the actual communication is rejected.

By accessing the device information registers (OpCode = ‘11’) the clock monitor is set to a minimum of 16 SCK edges plus a multiple by 8 (for example, 16, 24, 32, …).

Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE. For a SPI burst read also the SPI data length plus multiple numbers of payloads SCK edges are assumed as a valid communication.

4.4.2 SCK polarity (CPOL) check

To detect the wrong polarity access via SCK, the internal clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last will lead to an SPI error reported in the next communication and the actual data is rejected.

4.4.3 SCK phase (CPHA) check

To verify, that the SCK phase of the SPI master is set correctly a special device information register is implemented. By reading this register the data must be 55H. In case AAH is read the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

4.4.4 CSN timeout

By pulling CSN low the SDO is set active and leaves its tristate condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low a CSN timeout is implemented. By pulling CSN low an internal timer is started. After timer end is reached the actual communication is rejected and the SDO is set to tristate condition.

4.4.5 SDI stuck at GND

As a communication with data all-‘0’ and OpCode ‘00’ on address b’000000 cannot be distinguished between a valid command and a SDI stuck at GND this communication is not allowed. Nevertheless, in case a stuck at GND is detected the communication will be rejected and the SPIE will be set with the next communication.

4.4.6 SDI stuck at HIGH

As a communication with data all-‘1’ and OpCode ‘11’ on address b’111111 cannot be distinguished between a valid command and a SDI stuck at HIGH this communication is not allowed. In case a stuck at HIGH is detected the communication will be rejected and the SPIE will be set with the next communication.

4.4.7 SDO stuck at GND and HIGH

The SDO stuck at GND and stuck at HIGH has to be detected by the SPI master. As the definition of the GSB guarantees at least one toggle, a GSB with all-‘0’ or all-‘1’ reports a stuck at error.

5 Electrical characteristics

For an efficient and easy tracking, numbering has been added to each electrical parameter.

Device features are split into categories (see the following table), and each of them is represented by a letter (A, B, C, etc.); all parameters are completely identified by a letter and a three-digit number (for example, B.125, C.096…) for their whole lifetime.

New inserted parameters continue with the numbering of the related category, no matter of where they are placed.

To facilitate insertion, the last number inserted for each category is also reported in the second column of the following table.

Table 26. Electrical parameters numbering

Category	Parameters numbering
Analog I/O	A.xxx
Digital I/O	B.xxx
Voltage regulators	C.xxx
Outputs	D.xxx
Transceivers	E.xxx
Others	F.xxx

Due to these rules and taking into account that deleted parameter numbers are no more reassigned, numbering inside each category may be not sequential.

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

$6\ V \le V_S \le 28\ V$; $6\ V \le V_{SREG} \le 28\ V$, T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 27. Supply

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{SUV}	V_S undervoltage threshold	V_S decreasing	4.7	-	5.4	V	A.001
V_{hyst_UV}	V_S undervoltage hysteresis	V_S increasing	0.04	0.1	0.2	V	A.002
V_{SOV_I}	V_S overvoltage threshold	V_S increasing	19.95	21	22.5	V	A.003
V_{SOV_D}	V_S overvoltage threshold	V_S decreasing	18.5	20	22.5	V	A.004
V_{hyst_OV}	V_S overvoltage hysteresis	V_S decreasing	0.5	1.3	1.7	V	A.005
V_{SREGUV}	V_{SREG} undervoltage threshold	V_{SREG} decreasing	4.2	-	4.9	V	A.006
V_{hyst_UV}	VSREG undervoltage hysteresis	V_{SREG} increasing	0.04	0.1	0.2	V	A.007
V_{SREGOV_I}	V_{SREG} overvoltage threshold	V_{SREG} increasing	19.95	21	22.5	V	A.008
V_{SREGOV_D}	V_{SREG} overvoltage threshold	V_{SREG} decreasing	18.5	20	22.5	V	A.009
V_{hyst_OV}	V_{SREG} overvoltage hysteresis		0.5	1.3	1.7	V	A.010
t_{ovuv_filt}	V_S/ V_{SREG} over-/ undervoltage filter time	Tested by scan	45	64	80	µs	A.011
$I_{V(act)}$	Current consumption in active mode	V_S = 12 V	-	3	6	mA	A.012

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
		TxD CAN = high TxD LIN = high V1 ON, V2 OFF HS driver OFF CAN OFF					
$I_{V(VBAT,25)}$	Current consumption in VBAT_standby mode(1)(2)	V_S = 12 V, T_J = 25 °C Both voltage regulators deactivated HS driver OFF No CAN communication	-	15	25	µA	A.055
$I_{V(VBAT,85)}$(3)	Current consumption in VBAT_standby mode(1)(2)	V_S = 12 V, T_J = 85 °C Both voltage regulators deactivated HS driver OFF No CAN communication	-	25	30		A.013
$I_{V(BAT)CS}$	Current consumption in V_{BAT}-standby mode with cyclic sense enabled(1)	V_S = 12 V, T_J = 25 °C Both voltage regulators deactivated T = 50 ms, t_{on} = 100 µs	-	42	53	µA	A.056
		V_S = 12 V, T_J = 85 °C Both voltage regulators deactivated T = 50 ms, t_{on} = 100 µs	-	48	60		A.014
$I_{V(BAT)CW}$	Current consumption in V_{BAT}-standby mode with cyclic wake-up enabled(1)	V_S= 12 V, T_J = 25 °C Both voltage regulators deactivated In standby phase before wake-up on timer expiration	-	42	55	µA	A.057
		V_S= 12 V, T_j = 85 °C Both voltage regulators deactivated In standby phase before wake- up on timer expiration(3)	-	48	60		A.015
$I_{V(V1stby,25)}$	Current consumption in V1_standby mode(1)(2)	V_S = 12 V, T_J = 25 °C Voltage regulator V1 active, (Iv1 = 0) HS driver OFF Wake-up OFF except for LIN transceiver	-	48	60	µA	A.058
$I_{V(V1stby,85)}$(3)		V_S= 12 V, T_J = 85 °C Voltage regulator V1 active, (Iv1 = 0) HS driver OFF Wake-up OFF except for LIN transceiver	-	59	70		A.016
$I_{V(V1stby\_cc,25)}$(3)(4)	Current consumption for cyclic sense enabled	V1_standby WDG = OFF T_J = 25 °C	-	40	80	µA	A.059
$I_{V(V1stby\_cc,85)}$(3)(4)		V1_standby WDG = OFF T_J = 85 °C	-	48	96	µA	A.060
$I_{V(VBAT\_WU,25)}$(3)(4)	Current consumption for wake-up inputs	V_{BAT}_standby Voltage regulator V2 disabled	-	0.5	1.5	µA	A.061

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
	Current consumption for wake-up inputs	Wake-up on NO CAN NO LIN No activity on wake-up pins T_J = 25 °C				µA	
$I_{V(VBAT\_WU,85)}$[3][4]		V_{BAT}_standby Voltage regulator V2 disabled Wake-up on NO CAN NO LIN No activity on wake-up pins T_J = 85 °C	-	0.7	2.5		A.062
$I_{V(CANWU,25)}$[3][4]	Current consumption for CAN wake capability (silenced expired)	Standby modes CAN wake-up = ON WK = OFF Voltage regulator V2 disabled T_J = 25 °C	-	10	15	µA	A.063
$I_{V(CANWU\ 85)}$[3][4]		Standby modes CAN wake-up = ON WK = OFF Voltage regulator V2 disabled T_j = 85 °C	-	10	15		A.064
ICAN, rec[4]	Current consumption for CAN, recessive state	Active mode or V1 standby mode CAN = ON VCANSUP = 5 V VTXDC = 5 V No external resistance on CAN	4	7	10	mA	A.065
ICAN, dom[4]	Current consumption for CAN, dominant state	Active mode or V1 standby mode CAN = ON VCANSUP = 5 V VTXDC = GND No external resistance on CAN	7	10	13	mA	A.066
ICAN, rom[4]	Current consumption for CAN, receive only mode	Active mode or V1 standby mode CAN in receive mode VCANSUP = 5 V VTXDC = 5 V No external resistance on CAN	4	6	9	mA	A.067
$I_{V(VBAT\_LINWU,25)}$[3]	Current consumption for LIN wake capability	V_{BAT}_standby LIN wake-up = ON WK = OFF CAN = OFF T_J = 25 °C	-	15	25	µA	A.068
$I_{V(VBAT\_LINWU,85)}$[3]		V_{BAT}_standby	-	20	30		A.069

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
	Current consumption for LIN wake capability	LIN wake-up = ON WK = OFF CAN = OFF T_J = 85 °C				µA	
$I_{V(VBAT\_V2,25)}$[3]	Current consumption for voltage regulator V2 in V_{BAT} standby mode	V_{BAT}_standby V2 On (Iv2 = 0) CAN = OFF Wake-up = OFF T_J = 25 °C	-	48	84	µA	A.070
$I_{V(VBAT\_V2,85)}$[3]		V_{BAT}_standby V2 On (Iv2 = 0) CAN OFF Wake-up = OFF T_J = 85 °C	-	53	94		A.071
$I_{V(V1stby\_HS,25)}$[3]	Current consumption for HS drivers	V1_standby cyclic sense enabled[5] HSx (x = 3;4) = ON CAN = OFF Wake-up OFF except LIN transceiver T_J = 25 °C	-	550	950	µA	A.072
$I_{V(V1stby\_HS,85)}$[3]		V1_standby cyclic sense enabled[5] HSx (x = 3;4) = ON CAN = OFF Wake-up OFF except LIN transceiver T_J = 85 °C	-	570	1000		A.073

1. *Conditions for specified current consumption:*
   - *V_{LIN} > (V_{SREG} - 1.5 V)*
   - *(CAN_H - CAN_L) < 0.4 V or (CAN_H - CAN_L) > 1.2 V*
   - *V_{WU} < 1 V or V_{WU} > (V_{SREG} - 1.5 V)*
   - *LIN wake-up is possible, CAN wake up disabled, WUx_EN register set to 0*
2. *In SPSB081Cx it is mandatory to keep wake-up source capability (CANFD or wake-up pin) and in that case an additional contribution of $I_{V(VBAT\_WU,x)}$ or $I_{V(CANWU,x)}$ has to be considered.*
3. *Guaranteed by design.*
4. *Current consumption adders of features defined for SBC V1 stby mode or for SBC VBAT stby mode (unless otherwise specified).*
5. *Current consumption adder while only one HS is turned on with no load.*

5.1 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_J = -40 °C... 150 °C, unless otherwise specified.

Table 28. Oscillator

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
F_{CLK1}[1][2]	Oscillation frequency	-	0.80	1.0	1.20	MHz	A.018
F_{CLK2}[1]	Oscillation frequency	-	12.8	16.0	19.2	MHz	A.019

1. *1 MHz clock is used in standby mode. 16 MHz clock is used in active mode.*
2. *The clock frequency is further reduced in standby mode to sustain a very low quiescent current.*

5.2 Power-on reset (V_{SREG})

All outputs open: T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 29. Power-on reset

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{POR_R}	V_{POR} threshold	V_{SREG} rising	-	3.45	4.5	V	A.020
V_{POR_F}	V_{POR} threshold	V_{SREG} falling(1)	2.3	-	3.55	V	A.021

1. *This threshold is valid if V_{SREG} had already reached V_{POR_R}(max) previously.*

5.3 Voltage regulator V1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
4.5 ≤ V_S ≤ 28 V; 4.5V ≤ V_{SREG} ≤ 28 V; T_j = from -40 °C to 150 °C, unless otherwise specified.
The same parameter values in both 5 V and 3.3 V conditions apply unless otherwise specified.

Table 30. Voltage regulator V1

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V1	Output voltage including line and load regulation	V_{SREG}≥ 6.5 V	-	5.0	-	V	C.001
			-	3.3	-		C.041
$V1_{10mA}$	Output voltage tolerance (0...I_{CMP})	I_{LOAD} = 100 µA to I_{CMP} V_{SREG} = 13.5 V	-2.5	-	+2.5	%	C.003
$V1_{high\_acc}$	Output voltage tolerance High accuracy mode	I_{LOAD} = I_{CMP} to 100 mA, (active mode) V_{SREG} = 13.5 V	-2.5	-	+2.5	%	C.004
$V1_{250mA}$	Output voltage tolerance (100… 250 mA)	I_{LOAD} = 250mA, V_{SREG} = 13.5 V	-3	-	+3	%	C.005
V_{1ov_th1}	OverVoltage threshold 1 for V1	V1 rising	5.2	5.35	5.5	V	C.042
		V1 falling - V1 13V5/100 µA	0.1	-	0.4		
		V1 rising	3.5	3.65	3.8		C.066
		V1 falling - V1 13V5/100 µA	0.1	-	0.4		
V_{1ov_th2}	OverVoltage threshold 2 for V1	Define the test condition	5.5	5.65	5.8	V	C.043
		-	3.9	4.05	4.2		C.067
$R_{discharge}$	Resistance to be able to discharge 20 mA	V1 = 3.3 V	-	120	165	Ω	C.044
		V1 = 5 V	-	130	200		C.045
V_{DP1}	Drop-out voltage	I_{LOAD} = 50 mA, V_{SREG} = 5 V (V1 = 5 V)	-	0.2	0.25	V	C.006
		I_{LOAD} = 50 mA, V_{SREG} = 3.55 V(1)(V1 = 3.3 V)		0.25	0.35		C.046
		I_{LOAD} = 100 mA, V_{SREG}= 5 V (V1 = 5 V) and V_{SREG} = 3.55 V(1) below 3.55 V, the POR V_{SREG} can be activated and there is a device reset. (V1 = 3.3 V)		0.35	0.5		C.007

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{DP1}	Drop-out voltage	I_{LOAD} = 150 mA, V_{SREG} = 5 V and V_{SREG}= 3.55 V(1) (V1 = 3.3 V); T = 25 °C	-	0.35	0.5	V	C.008
I_{CCmax1}	Short circuit output current (to GND)	Current limitation	450	750	1100	mA	C.010
Cload1(2)	Load capacitor1	Ceramic (±20%)	1(3)	-	10(1)	µF	C.011
t_{TSD}	V1 deactivation time after thermal shut-down	Tested by scan	-	1.5	-	sec	C.012
ICMP_ris(4)	Current comp. rising threshold (to GND)	Rising current ICMP_SET = 0	1	4	7	mA	C.013
		Rising current ICMP_SET = 1	6	12	18		C.047
ICMP_fal(4)	Current comp. falling threshold (to GND)	Falling current ICMP_SET = 0	0.4	2.8	4.2	mA	C.014
		Falling current ICMP_SET = 1	4	10	15		C.048
ICMP_hys(4)	Current comp. hysteresis	ICMP_SET = 0		1.2		mA	C.015
		ICMP_SET = 1	1	2	4		C.049
V1fail	V1 fail threshold	V1 forced (V1 = 5 V)	-	2	3	V	C.016
		V1 forced (V1 = 3.3 V)	-	1.3	2		C.050
$t_{OV1filter1}$	V1 overvoltage filter time1	Tested by scan	-	20	30	µs	C.051
$t_{OV1filter2}$	V1 overvoltage filter time2	Tested by scan	-	20	30	µs	C.052
t_{V1fail}	V1 fail filter time	Tested by scan	6	13	20	µs	C.017
$t_{V1short}$	V1 short filter time	Tested by scan	2	4	5	ms	C.018
t_{V1FS}	V1 fail-safe filter time	Tested by scan	1.43	2	2.06	ms	C.019
t_{V1off}	V1 deactivation time after 8 consecutive WD failures	Tested by scan	-	200	270	ms	C.020

1. *Below 3.55 V, the POR VSREG can be activated and there is a device reset.*
2. *Guaranteed by design.*
3. *Nominal capacitor value required for stability of the regulator. Tested with 1 µF ceramic (±20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor value is recommended to minimize the DPI (Direct power injection) stress in the application.*
4. *In active mode, V1 regulator is switched to high accuracy mode. Below the Icmp threshold, regulator switches in any case to nominal accuracy mode (same behavior applies also in case of high current).*

5.4 Voltage regulator V2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

4.5 V ≤ V_S ≤ 28 V; 4.5 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

The same parameter values in both 5 V and 3.3 V conditions apply unless otherwise specified.

Table 31. Voltage regulator V2

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V2	Output voltage including line and load regulation	V_{SREG} ≥ 6.5 V	-	5.0	-	V	C.053
			-	3.3	-		C.054
$V2_{high\_acc}$	Output voltage tolerance High accuracy mode	I_{LOAD} = 100 µA to 50 mA, (active mode) V_{SREG} = 13.5 V	-2.5	-	+2.5	%	C.055
$V2_{100mA}$	Output voltage tolerance (50… 100 mA)	I_{LOAD} = 100 mA, V_{SREG} = 13.5 V	-3	-	+3	%	C.056

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
ΔVo(1)	Output voltage tracking accuracy	Icc2 = 100 µA to 100 mA, Icc1 = 30 mA, V_{SREG} = 6.5 V to 28 V	-20	-	20	mV	C.057
VDP2	Drop-out voltage	I_{LOAD} = 30 mA; V_{SREG} = 5.25 V (V2 = 5 V) and V_{SREG} = 3.55 V (V2 = 3.3 V)	-	0.3	0.5	V	C.022
		I_{LOAD} =100 mA AT T= 25°C; VSREG =5.0 V (V2 = 5.0 V) and VSREG = 3.55 V (V2 = 3.3 V)	-	0.75	0.85	V	C.058
ICCmax2	Output current limitation	-	400	600	1200	mA	C.023
Cload(2)(3)	Load capacitor	Ceramic (±20%)	1	-	10	µF	C.024
V2fail_5	V2 short circuit voltage to switch V2 off and set SPI bit	V2 forced (V2 = 5 V)	-	2	3	V	C.025
V2fail_33		V2 forced (V2 = 3.3 V)	-	1.3	2		C.060
t_{V2fail}	V2 fail filter time	Tested by scan	6	13	20	µs	C.068
tV2short	V2 short filter time	Tested by scan	-	4	-	ms	C.026

1. *Output voltage tracking accuracy are guaranteed only in DC condition.*
2. *Nominal capacitor value required for stability of the regulator. Tested with 1 µF ceramic (±20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor value is recommended to minimize the DPI stress in the application.*
3. *Guaranteed by design.*

5.5 Reset output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
4 V ≤ V_S ≤ 28 V; 4 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 32. Reset output

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{RT1_5}	Reset threshold voltage1	V_{V1} decreasing (V1 = 5 V)	3.3	3.5	3.7	V	C.027
V_{RT1_33}		V_{V1} decreasing (V1 = 3.3 V)	2.5	2.65	2.75		C.061
V_{RT2_5}	Reset threshold voltage2	V_{V1} decreasing (V1 = 5 V)	3.6	3.8	4	V	C.028
V_{RT2_33}		V_{V1} decreasing (V1 = 3.3 V)	2.6	2.75	2.85		C.062
V_{RT3_5}	Reset threshold voltage3	V_{V1} decreasing (V1 = 5 V)	3.8	4.0	4.2	V	C.029
V_{RT3_33}		V_{V1} decreasing (V1 = 3.3 V)	2.7	2.85	2.95		C.063
$V_{RT4\text{-}1\_5}$	Reset threshold voltage4	V_{V1} decreasing (V1 = 5 V)	4.4	4.6	4.8	V	C.030
$V_{RT4\text{-}1\_33}$		V_{V1} decreasing (V1 = 3.3 V)	2.8	2.9	3.05		C.064
$V_{RT4\text{-}2\_5}$	Reset threshold voltage4	V_{V1} increasing (V1 = 5 V)	4.65	4.8	4.9	V	C.031
$V_{RT4\text{-}2\_33}$		V_{V1} increasing (V1 = 3.3 V)	2.95	3.1	3.2		C.065
V_{RESET}	Reset pin low output voltage	V1 > 1 V, I_{RESET} = 5 mA	-	0.2	0.4	V	C.032
R_{RESET}	Reset pull up int. resistor	-	10	25	40	kΩ	C.033
t_{RR}	Reset reaction time	Iload = 1 mA; tested by scan	6	-	40	µs	C.034
t_{UV1}	V1 under-voltage filter time	Tested by scan	6	12	20	µs	C.035
t_{RD}	Reset pulse duration	Tested by scan	1.5	2.0	2.5	ms	C.036

5.6 DIAGN output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
4 V ≤ V_S ≤ 28 V; 4 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 33. DIAGN output

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{DIAGN}	DIAGN pin low output voltage	V1 > 1V, I_{DIAGN} = 5 mA	-	0.2	0.4	V	C.037
R_{DIAGN}	DIAGN pulls up int. resistor	-	10	25	40	kΩ	C.038

5.7 Watchdog

For further information, see Section 3.6 Configurable window watchdog.
4.5 V ≤ V_S ≤ 28 V; 4.5 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 34. Watchdog

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{LW}	Long open window	Tested by scan	240	300	360	ms	A.022
T_{EFW1}	Early failure window 1	Tested by scan	-	-	4.5	ms	A.023
T_{LFW1}	Late failure window 1	Tested by scan	20	-	-	ms	A.024
T_{SW1}	Safe window 1	Tested by scan	7.5	-	12	ms	A.025
T_{EFW2}	Early failure window 2	Tested by scan	-	-	22.3	ms	A.026
T_{LFW2}	Late failure window 2	Tested by scan	100	-	-	ms	A.027
T_{SW2}	Safe window 2	Tested by scan	37.5	-	60	ms	A.028

Figure 31. **Watchdog timing**

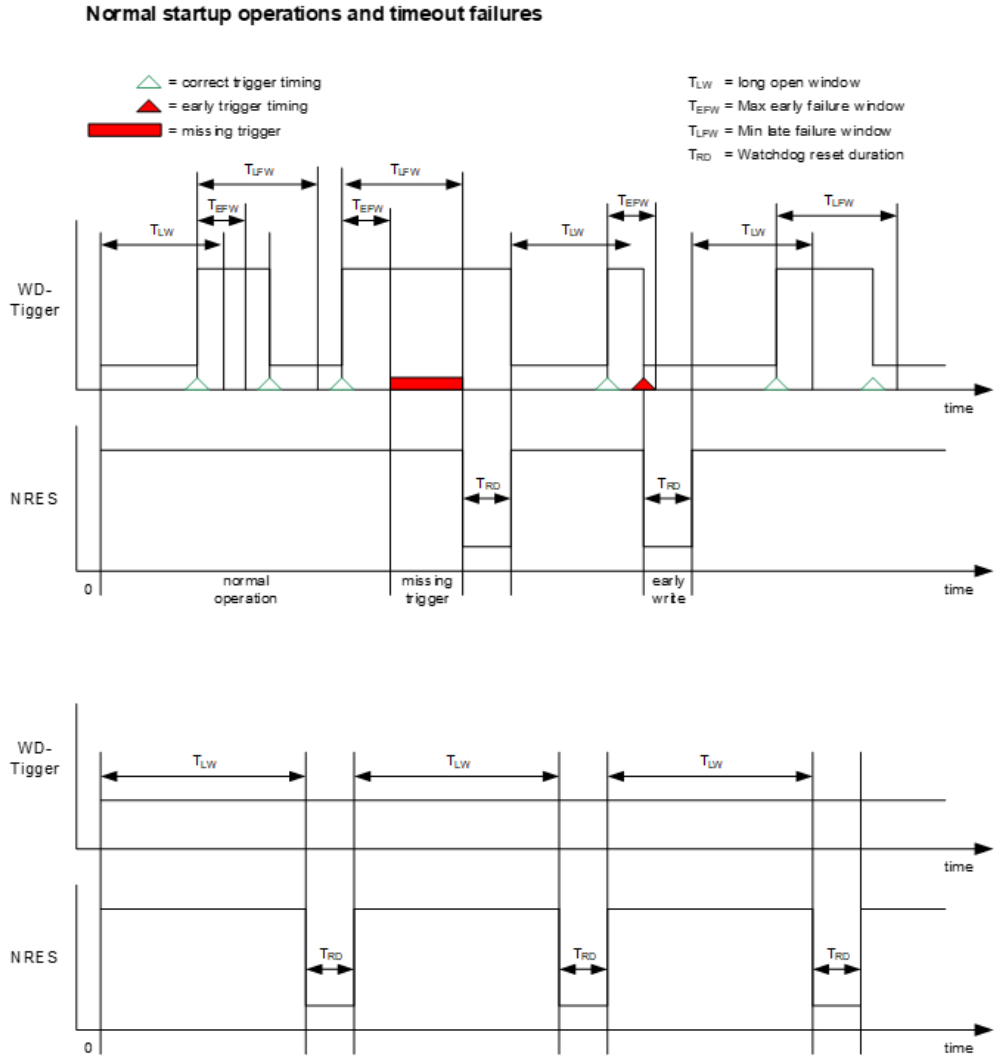
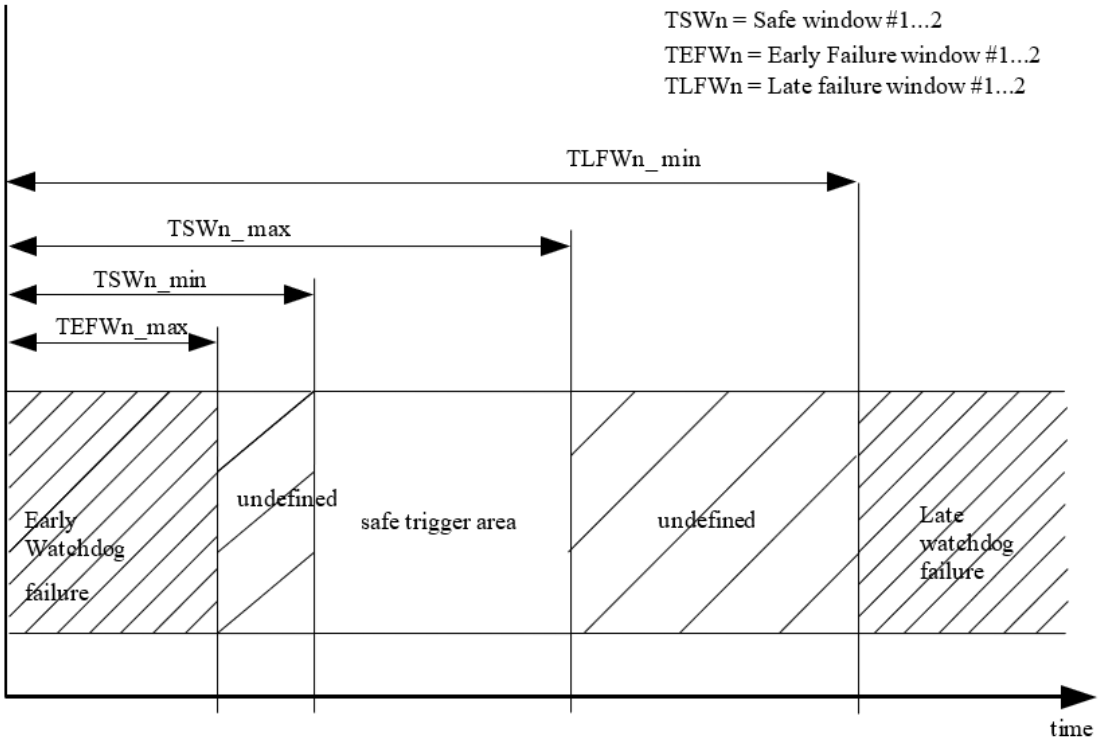


Figure 32. **Watchdog early, late and safe windows**



5.8 Current monitor output (CM)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 35. **Current monitor output (CM)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{CM}	Functional voltage range	-	0	-	V_1 - 1 V	V	A.029
I_{CMr}	$I_{CM}/I_{OUT1,2,3,4}$	0 V ≤ V_{CM} ≤ V_1 - 1 V	-	1/990	-	-	A.030
$I_{CM\ acc}$	Current monitor accuracy	Ranges extracted at the output: $I_{OUT1,2,3,4}$ I_{OUTmin} = 100 mA I_{OUTmax} = 130 mA	-8% -4% FS(1)	0	8% +4% FS(1)	A	A.031
t_{cmb}	Current monitor blanking time	Tested by scan	22	32	39	µs	A.032

1. *FS (full scale) = IOUTmax * ICMr_typ.*

5.9 Outputs OUT1..OUT4

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_S ≤ 18 V, all outputs open: T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 36. Outputs OUT1..OUT4

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$r_{ON\ OUT1,2,3,4\_25}$	On-resistance to supply	V_S = 13. 5 V, T_{amb} = +25 °C $I_{OUT1,2,3,4}$ = - 60 mA	-	7	9	Ω	D.001
$r_{ON\ OUT1,2,3,4\_125}$		V_S = 13.5 V, T_{amb} = +125 °C $I_{OUT1,2,3,4}$ = - 60 mA	-	14	20	Ω	D.002
I_{QLH_stdby}	Switched-off output current high side drivers of OUT1..4(1)	V_{OUT} = 0 V, standby mode	-5	-	-	µA	D.003
$I_{QLH\_stdby\_act}$		V_{OUT} = 0 V, active mode	-10	-	-	µA	D.004

1. *Negative value: leakages internally sink from driver output pin to internal IC ground positive value: leakage sourced from internal driver output pin to external ground.*

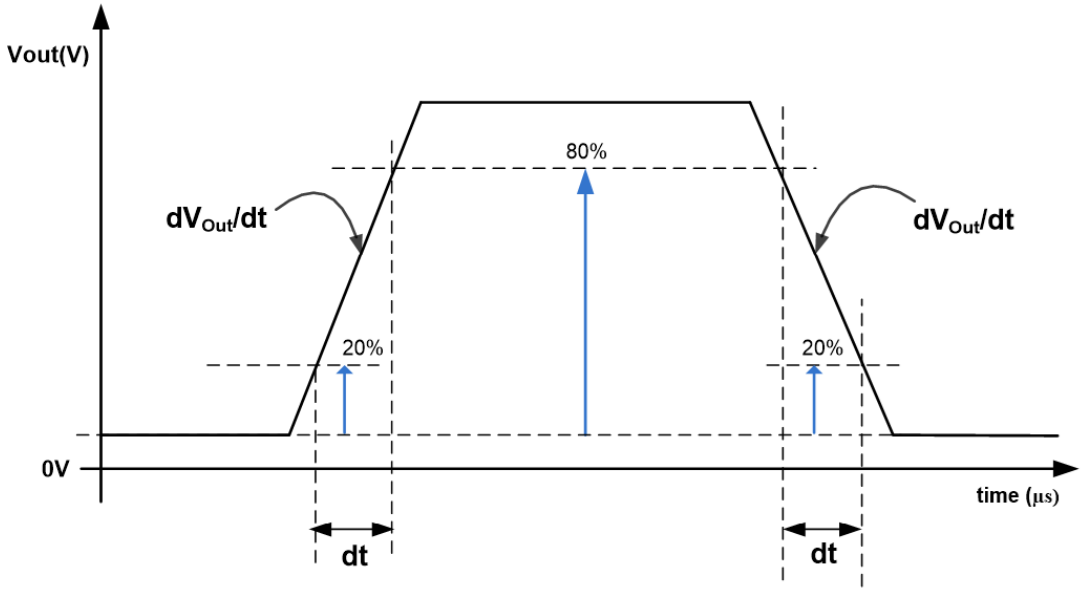
5.10 Power outputs switching times

Table 37. Power outputs switching times

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$t_{d\ OFF\ H}$	Output delay time high-side driver OFF (OUT1,2,3,4) (delay between CSN 50 % to OUT at 20% of V_S) (see Figure 39)	V_S = 13.5 V V1 = 5 V R_{load} = 128 Ω	20	-	140	µs	D.005
$t_{d\ ON\ H}$	Output delay time high-side driver ON (OUT1,2,3,4) (delay between CSN 50% to OUT at 80% of V_S) (see Figure 39)	V_S= 13.5 V V1 = 5 V R_{load} = 128 Ω	10	-	60	µs	D.006
dV_{OUT}/dt	Slew rate for drivers OUT1..4	V_S = 13.5 V(1)(2)	0.1	0.2	0.5	V/µs	D.007
f_{PWM1}	PWM switching frequency	V_S/V_{SREG} = 13.5 V; tested by scan	-	125	-	Hz	D.008
f_{PWM2}	PWM switching frequency	V_S/V_{SREG} = 13.5 V; tested by scan	-	250	-	Hz	D.009
DC	SPI configurable duty cycle for OUT1..4	0.1% steps; tested by scan	0.1	-	100	%	D.010

1. *R_{LOAD} = 128 Ω at $OUT_{1,2,3,4}$, in high on-resistance mode.*
2. *Slope dV_{OUT}/dt is measured between 20% and 80% of the final output voltage value.*

Figure 33. **Slew-rate of the drivers**



5.11 Output current threshold

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 38. **Output current threshold**

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$\|I_{OC1}\|$	Over-current threshold HS1	V_S = 13.5 V, source	0.14	-	0.35	A	D.011
$\|I_{OC2}\|$	Over-current threshold HS2	V_S = 13.5 V, source	0.14	-	0.35	A	D.022
$\|I_{OC3}\|$	Over-current threshold HS3	V_S = 13.5 V, source	0.14	-	0.35	A	D.023
$\|I_{OC4}\|$	Over-current threshold HS4	V_S = 13.5 V, source	0.14	-	0.35	A	D.024
$\|I_{CCM1}\|$	Constant current mode value for OUT1 (high on resistance mode)	V_S = 13.5 V OUT1_CCM_EN = 1	100	142	200	mA	D.012
$\|I_{CCM2}\|$	Constant current mode value for OUT2 (high on resistance mode)	V_S = 13.5 V OUT2_CCM_EN = 1	100	145	200	mA	D.025
$\|I_{CCM3}\|$	Constant current mode value for OUT3 (high on resistance mode)	V_S = 13.5 V OUT3_CCM_EN = 1	100	145	200	mA	D.026
$\|I_{CCM4}\|$	Constant current mode value for OUT4 (high on resistance mode)	V_S = 13.5 V OUT4_CCM_EN = 1	100	145	200	mA	D.027
$t_{CCMtimeout}$	Constant current mode expiration time;	OUTx_CCM_EN = 1 (x = 1 to 4) Tested by scan	-	20	-	ms	D.013
t_{BLK}	Blanking time of over-current signal in high sides	Tested by scan	33	40	56	µs	D.015
t_{OCR00}	T_{ON} time of over-current signal (including blanking time t_{BLK})	xx_OCR_TON[0,1] = 00 Tested by scan	76	88	116	µs	D.016

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{OCR01}	T_{ON} time of over-current signal (including blanking time t_{BLK})	xx_OCR_TON[0,1] = 01 Tested by scan	70	80	106	µs	D.017
t_{OCR10}		xx_OCR_TON[0,1] = 10 Tested by scan	64	72	96	µs	D.018
t_{OCR11}		xx_OCR_ TON[0,1] = 11 Tested by scan	57	64	87	µs	D.019
$\|I_{OLD1}\|$(1)	Under-current threshold HS1	V_S/V_{SREG} = 13.5 V, source	0.2	0.65	1.5	mA	D.020
$\|I_{OLD2}\|$(1)	Under-current threshold HS2	V_S/V_{SREG} = 13.5 V, source	0.2	0.65	1.5	mA	D.028
$\|I_{OLD3}\|$(1)	Under-current threshold HS3	V_S/V_{SREG} = 13.5 V, source	0.2	0.65	1.5	mA	D.029
$\|I_{OLD4}\|$(1)	Under-current threshold HS4	V_S/V_{SREG} = 13.5 V, source	0.2	0.65	1.5	mA	D.030
t_{FOL}	Filter time of open-load signal	Duration of open-load condition to set the status bit Tested by scan	155	200	270	µs	D.021

1. *I_{OLD} parameters, in the range 8 V to 16 V, are guaranteed by design and characterization. Production testing is done at 13.5 V.*

5.12 Wake-up inputs (WU1, DIR/WU2)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{SREG} ≤ 28 V; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 39. Wake-up inputs

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{WUthp}	Wake-up positive edge threshold voltage	-	0.4 V_{SREG}	0.45 V_{SREG}	0.5 V_{SREG}	V	A.033
V_{WUthn}	Wake-up negative edge threshold voltage	-	0.5 V_{SREG}	0.55 V_{SREG}	0.6 V_{SREG}	V	A.034
V_{DIRth}	DIR threshold voltage	-	0.5	1.5	2.5	V	A.035
V_{HYST}	Hysteresis(1)	-	0.05 V_{SREG}	0.1 V_{SREG}	0.15 V_{SREG}	V	A.036
t_{WU_stat}	Static wake filter time	Tested by scan	-	64(2)	-	µs	A.037
R_{WU_act}	Input resistor to GND in active mode and in standby mode during wake-up input sensing	-	80	160	300	kΩ	A.039
t_{WU_cyc}	Cyclic wake filter time	Tested by scan	12	16	20	µs	A.040

1. *In DIR configuration, no appreciable hysteresis is observed.*
2. *Guaranteed by design.*

5.13 CAN FD transceiver

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{SREG} ≤ 18 V; 4.8 V ≤ Vcansup ≤ 5.2 V; $T_{junction}$ = from -40 °C to 150 °C, unless otherwise specified.
-12 V ≤ (CANH + CANL)/2 ≤ 12 V

- ISO 11898-2:2016 compliant
- SAE J2284 compliant

Table 40. CAN communication operating range

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{SREG\_Transmitter}$	Supply voltage operating range for CAN transmitter(1)	-	6.5	-	28	V	E.001
$V_{SREG\_Receiver}$	Supply voltage operating range for CAN receiver	-	6.5	-	28	V	E.002
$V_{CANSUPvalid}$	CAN supply valid voltage flag	V_{V1} = V_{CANSUP} decreasing or V_{V2} = V_{CANSUP} decreasing or external supply = V_{CANSUP} decreasing	4.5	4.65	4.8	V	E.105
$V_{CANSUPext}$	External CAN supply output voltage	-	4.9	5.0	5.1	V	E.106
$t_{CANSUPvalid}$	CAN supply UV filter time	Tested by scan	-	22	-	µs	E.107
$V_{CANSUPlow}$	CAN supply low voltage flag	V_{V1} = V_{CANSUP} decreasing or V_{V2} = V_{CANSUP} decreasing or External supply = V_{CANSUP} decreasing	4.1	4.3	4.5	V	E.031
$V_{CANHL, CM}$	Common mode Bus voltage (V_{CANH} + V_{CANL})/2	Measured with respect to the ground of each CAN transceiver	-12	-	12	V	E.113
I_{TRCV}	Transceiver current consumption during normal mode	Active mode: RL = 50 Ω…65 Ω 70% V_{RXDC} (rising) - 30% V_{RXDC} (falling) CRXD = 15 pF TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%) Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width Rectangular pulse signal TTXDC = 6*TBIT(2), high pulse 1*TBIT, low pulse 5*TBIT	-	-	120	mA	E.003
I_{TRCV_short}	Transceiver current consumption during output short	R_L = 50 Ω…65 Ω V_{CANH} = -3 V or V_{CANL} = 40 V	-	-	120	mA	E.004
$I_{TRCVLPbias}$	Transceiver current consumption; biasing active	R_L = 50 Ω…65 Ω V_{TXDC} = $V_{TXDCHIGH}$	-	400	600	µA	E.005
I_{TRCVLP}	Transceiver current consumption during low-power mode; biasing inactive	RL = 50 Ω…65 Ω V_{TXDC} = $V_{TXDCHIGH}$	-	10	50	µA	E.006
BR	Supported bitrates	Supported bitrates at which all requirements are fulfilled	-	-	5	Mb/s	E.007

1. *VAt V_{SREG} < $V_{SREG\_Tranmitter}$(min) the transceiver shall enter high impedance state .*

2. *The bit time T_{BIT} is the nominal bit time at a given bit rate (T_{BIT} = 1/BR). For example at BR = 2 Mb/s → T_{BIT} = 500 ns*

Table 41. CAN transmit data input: Pin TxDC

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{TXDCLOW}$	Input voltage dominant level	Active mode	1.0	1.45	2.0	V	E.008
$V_{TXDCHIGH}$	Input voltage recessive level	Active mode	1.2	1.85	2.3	V	E.009
$V_{TXDCHYS}$	$V_{TXDCHIGH}$ - $V_{TXDCLOW}$	Active mode	0.2	-	0.7	V	E.010
R_{TXDCPU}	TXDC pull up resistor	Active mode	20	50	110	kΩ	E.011
$t_{d,TXDC(dom-rec)}$	TXDC - $CAN_{H,L}$ delay time dominant - recessive	R_L = 50 Ω…65 Ω; 70 % V_{TXD} - 30% V_{DIFF} 5.5 V ≤ V_{SREG} ≤ 18 V TXDC rise time = 10 ns (10% - 90%)	0	120	-	ns	E.012
$t_{d,TXDC(rec-diff)}$	TXDC - CANH,L delay time recessive - dominant	R_L = 50 Ω…65 Ω 30 % V_{TXD} - 70% V_{DIFF} 5.5 V ≤ V_{SREG} ≤ 18 V TXDC fall time = 10 ns (90% - 10%)	0	120	-	ns	E.013
$t_{dom(TXDC)}$	TXDC dominant time-out	Tested by scan	0.8	2	5	ms	E.014

Table 42. CAN receive data output: Pin RxDC

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{RXDCLOW}$	Output voltage dominant level	Active mode, I_{RXDC} = 2 mA	0	0.2	0.5	V	E.015
$V_{RXDCHIGH}$	Output voltage recessive level	Active mode, I_{RXDC} = -2 mA	V1 - 0.5	V1 - 0.2	V1	V	E.016
$t_{r,RXDC}$	RxDC rise time	C_L = 15 pF 30% - 70% V_{RXDC}(1)	0	-	25	ns	E.017
$t_{f,RXDC}$	RxDC fall time	C_L = 15 pF 70% - 30% V_{RXDC}(1)	0	-	25	ns	E.018
$t_{d,\ RXDC(dom-rec)}$	$CAN_{H,L}$ RxDC delay time dominant - recessive	C_L = 15 pF 30% V_{DIFF} - 70% V_{RXDC}(1)	0	120	-	ns	E.019
$t_{d,\ RXDC(rec\ -\ dom)}$	$CAN_{H,L}$ RxDC delay time dominant - recessive	C_L = 15 pF 70% V_{DIFF} - 30% V_{RXDC}(1)	0	120	-	ns	E.020

1. *Guaranteed by design.*

Table 43. CAN transmitter dominant output characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{CANHdom}$	Single ended CANH voltage level in dominant state	V_{TXDC} = $V_{TXDCLOW}$ R_L = 50 Ω…65 Ω	2.75	3.5	4.5	V	E.021
$V_{CANLdom}$	Single ended CANL voltage level in dominant state	V_{TXDC} = $V_{TXDCLOW}$ R_L = 50 Ω…65 Ω	0.5	1.5	2.25	V	E.022
$V_{DIFF,dom}$	Differential output voltage in dominant state: $V_{CANHdom}$ - $V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$ R_L = 50 Ω…65 Ω	1.5	2.0	3	V	E.023

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{DIFF_Arb}	Differential output voltage in dominant state during arbitration: $V_{CANHdom}$ - $V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$ R_L = 2240 Ω	1.5	-	5	V	E.024
V_{DIFF,dom_ext}	Differential output voltage in dominant state on extended bus load range: $V_{CANHdom}$ - $V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$ R_L = 45 Ω…70 Ω	1.4	-	3.3	V	E.025
$V_{DIFF,domVsLow}$	Differential output voltage in dominant state: $V_{CANHdom}$ - $V_{CANLdom}$ at low V_{SREG}	V_{TXDC} = $V_{TXDCLOW}$ R_L = 50 Ω…65 Ω 5 V < V_{SREG} < 5.5 V(1)	1.35	-	3	V	E.026
V_{DIFF,dom_ext_VsLow}	Differential output voltage in dominant state: $V_{CANHdom}$ - $V_{CANLdom}$ with 45 Ω…70 Ω load at low V_{SREG}	VT_{XDC} = $V_{TXDCLOW}$ RL = 45 Ω…70 Ω 5 V < V_{SREG} < 5.5 V (1)	1.25	-	3.3	V	E.027
V_{SYM}	Driver symmetry V_{SYM} = (V_{CANH} + V_{CANL})/V_{CANSUP} V_{CANSUP} = 5 V(2)	R_L = 60 Ω ±1% f_{TXDC} = 1 MHz(3) C_{SPLIT} = 4.7 nF (±5%)	0.9	1	1.1	-	E.028
$I_{OCANH,dom\ (-3\ V)}$	CANH output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$ V_{CANH} = -3 V…18 V	-115	-	115	mA	E.029
$I_{OCANL,dom\ (18\ V)}$	CANL output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$ V_{CANL} = -3 V…18 V	-115	-	115	mA	E.030
$I_{OCANL,dom\ (40\ V)}$	CANL output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$; V_{CANL} = 40 V V_{SREG} = 40 V	0	-	115	mA	E.032

1. *V_{SREG} at device pin after reverse battery protection, while application is supplied with 6 V. Operating condition has to be adapted, if higher voltage drop occur in the application.*
2. *Put into the datasheet, if it is an internal voltage. If it is an external pin, it should be supplied externally.*
3. *Measurement equipment input load < 20 pF, > 1 MΩ, guaranteed by E.025, E.026, E.029, E.030, E.053, E.054 measurements.*

Table 44. CAN transmitter recessive output characteristics, CAN normal mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{CANHrec}$	CANH voltage level in recessive state (normal mode)	V_{TXDC} = $V_{TXDCHIGH}$ No load	2	2.5	3	V	E.033
$V_{CANLrec}$	CANL voltage level in recessive state (normal mode)	V_{TXDC} = $V_{TXDCHIGH}$ No load	2	2.5	3	V	E.034
$V_{DIFF,recOUT}$	Differential output voltage in recessive state (normal mode): $V_{CANHrec}$ - $V_{CANLrec}$	V_{TXDC} = $V_{TXDCHIGH}$ No load	-50	-	50	mV	E.035

Note: CAN normal mode: tested in TRX normal state while the device is in active mode.

Table 45. CAN receiver input characteristics during CAN normal mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{THdom}	Differential receiver threshold voltage recessive to dominant state	-12V ≤ V_{CANH} ≤ 12 V 12 V ≤ V_{CANL} ≤ 12 V	0.5	-	0.9	V	E.036
V_{dom_range}	Differential dominant input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V -12 V ≤ V_{CANL} ≤ 12 V	0.9	-	10	V	E.037
V_{THrec}	Differential receiver threshold voltage dominant to recessive state	12 V ≤ V_{CANH} ≤ 12 V -12 V ≤ V_{CANL} ≤ 12 V	0.5	-	0.9	V	E.038
V_{rec_range}	Differential recessive input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V -12V ≤ V_{CANL} ≤ 12 V	-5	-	0.5	V	E.039

Note: CAN normal mode: tested in TRX normal state while the device is in active mode.

Table 46. CAN receiver input characteristics during CAN low power mode, biasing inactive

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{THdomLP}$	sferential receiver threshold voltage recessive to dominant state	12 V ≤ V_{CANH} ≤ 12 V -12 V ≤ V_{CANL} ≤ 12 V	0.4	-	1.15	V	E.040
$V_{dom\_range\_LP}$	Differential dominant input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V -12 V ≤ V_{CANL} ≤ 12 V	1.15	-	10	V	E.041
$V_{THrecLP}$	Differential receiver threshold voltage dominant to recessive state	12 V ≤ V_{CANH} ≤ 12 V -12 V ≤ V_{CANL} ≤ 12 V	0.4	-	1.15	V	E.042
$V_{rec\_range\_LP}$	Differential recessive input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V -12 V ≤ V_{CANL} ≤ 12 V	-5	-	0.4	V	E.043
$V_{CANHrecLP}$	CANH output voltage in recessive state	-	-0.1	-	0.1	V	E.108
$V_{CANLrecLP}$	CANL output voltage in recessive state	-	-0.1	-	0.1	V	E.109
$V_{DIFF,recOUTLP}$	Differential output voltage in recessive state: $V_{CANHrecLP}$ - $V_{CANLrecLP}$	-	-0.2	-	0.2	V	E.110

Note: CAN low power mode, biasing inactive: Tested in CAN TRX STDBY (bias off) state while the device is in active mode, V1_standby mode and Vbat_standby mode.

Table 47. CAN receiver input resistance

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
R_{diff}	Differential internal resistance	V_{TXDC} = $V_{TXDCHIGH}$ no load R_{diff} = R_{CANH} + R_{CANL} -2.0 V ≤ V_{CANH} ≤ +7.0 V -2.0 V ≤ V_{CANL} ≤ +7.0 V(1)	12	-	100	kΩ	E.044
$R_{CANH, CANL}$	Single ended internal resistance	V_{TXDC} = $V_{TXDCHIGH}$ No load -2.0 V ≤ V_{CANH} ≤ +7.0 V -2.0 V ≤ V_{CANL} ≤ +7.0 V(1)	6	-	50	kΩ	E.045

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
m_R	Internal Resistance matching $R_{CANH,CANL}$	Biasing active; $V_{TXDC} = V_{TXDCHIGH}$; No load $m_R = 2 \times (R_{CAN\_H} - R_{CAN\_L})/(R_{CAN\_H} + R_{CAN\_L})$ 10 kΩ resistor between CANH - CANL pin with external 5 V	-0.03	-	0.03	-	E.046

1. *Voltage range is taken from ISO CD 16845-2 (high-speed medium access unit - conformance test plan).*

Note: CAN normal and low power mode, biasing active: Tested in TRX normal and CAN TRX STDBY (bias on) state while the device is in active and V1_standby mode.

Table 48. CAN transceiver delay

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$t_{LOOP,hl}$	Loop delay TXDC to RXDC (high to low)	5.5 V < V_{SREG} < 18 V; R_L = 60 Ω ±1% C_L = 100 pF 30% V_{TXDC} - 30% V_{RXDC}; TXDC fall time = 10 ns (90% - 10%) C_{RXDC} = 15 pF	-	-	255	ns	E.047
$t_{LOOP,lh}$	Loop delay TXDC to RXDC (low to high)	5.5 V < V_{SREG} < 18 V R_L = 60 Ω ±1% C_L = 100 pF 70% V_{TXD} - 70% V_{RXD} TXDC rise time = 10 ns (10% - 90%) C_{RXDC} = 15 pF	-	-	255	ns	E.048
$t_{LOOP150,hl}$	Loop delay TXDC to RXDC (high to low) with 150Ω bus load	5.5 V < V_{SREG} < 18 V R_L = 150 Ω C_L = 100 pF 30% V_{TXDC} - 30% V_{RXDC} TXDC fall time = 10 ns (90% - 10%) C_{RXDC} = 15 pF	-	-	350	ns	E.049
$t_{LOOP150,lh}$	Loop delay TXDC to RXDC (low to high) with 150Ω bus load	5.5 V < V_{SREG} < 18 V R_L = 150 Ω C_L = 100 pF; 70% V_{TXD} - 70% V_{RXD} TXDC rise time = 10 ns (10% - 90%) C_{RXDC} = 15 pF	-	-	350	ns	E.050
$T_{Bit(RXD)} \leq$ 1Mb/s (1)	Recessive bit symmetry at RXDC	5.5 V < V_{SREG} < 18 V R_L = 60 Ω ±1% 70% V_{RXDC} (rising) - 30% V_{TXDC} (falling) C_L = 100 pF C_{RXD} = 15pF TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%)	900	1000	1050	ns	E.051

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
	Recessive bit symmetry at RXDC	Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width Rectangular pulse signal T_{TXDC} = 6000 ns, high pulse 1000 ns, low pulse 5000 ns				ns	
$T_{Bit(RXD)\_150\ ohm}$ ≤ 1 Mb/s		R_L = 150 Ω Other conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s Value may be obtained by characterization only.	800	-	1050		E.052
$T_{Bit(RXD)}$ ≤ 2 Mb/s		Conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s Rectangular pulse signal T_{TXDC} = 3000 ns, high pulse 500 ns, low pulse 2500 ns	400	500	550		E.053
$T_{Bit(RXD)\_150\ ohm}$ ≤ 2Mb/s		R_L=150 Ω other conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s Value may be obtained by characterization only	300	-	550		E.054
T_{Bit}(RXD) ≤ 5 Mb/s		Conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s Rectangular pulse signal T_{TXDC} = 1200 ns, high pulse 200 ns, low pulse 1000 ns	120	200	220		E.055
$T_{Bit(BUS)}$ ≤ 1 Mb/s	Recessive bit symmetry at CAN-Bus	5.5 V < V_{SREG} < 18V R_L = 60 Ω ±1% V_{DIFF}: 0.5 V(falling) - 0.9 V (rising) $_L$ = 100 pF C_{RXD} = 15 pF TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%) Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width Rectangular pulse signal T_{TXDC} = 6000 ns, high pulse 1000 ns, low pulse 5000 ns	935	1000	1030	ns	E.056
$T_{Bit(BUS)}$ ≤ 2 Mb/s		Conditions as $T_{Bit(BUS)}$ ≤ 1 Mb/s Rectangular pulse signal T_{TXDC} = 3000 ns, high pulse 500 ns, low pulse 2500 ns	435	500	530		E.057
$T_{Bit(BUS)}$ ≤ 5 Mb/s		Conditions as $T_{Bit(BUS)}$ ≤ 1 Mb/s Rectangular pulse signal T_{TXDC} = 1200 ns, high pulse 200 ns, low pulse 1000 ns	155	200	210		E.058
Δt_{REC} ≤ 2 Mb/s	Receiver timing symmetry ($T_{Bit(RXD)}$ - $T_{Bit(BUS)}$)	5.5 V < V_{SREG} < 18 V R_L = 60 Ω ±1% C_L = 100 pF C_{RXD} = 15 pF Rectangular pulse signal T_{TXDC} = 3000 ns, high pulse 500 ns, low pulse 2500 ns	-65	-	40	ns	E.059
Δt_{REC} ≤ 5 Mb/s		5.5 V < V_{SREG} < 18 V R_L = 60 Ω ±1% C_L = 100 pF	-45	-	15		E.060

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
	Receiver timing symmetry ($T_{Bit(RXD)}$ - $T_{Bit(BUS)}$)	C_{RXD} = 15 pF Rectangular pulse signal T_{TXDC} = 1200 ns, high pulse 200 ns, low pulse 1000 ns				ns	
t_{CAN}(2)	CAN permanent dominant time out	Tested by scan	600	700	900	µs	E.061
t_{WUP} - V_{Cansup}	time between WUP on the CAN bus until V_{Cansup} goes active	Wake-up-pattern wake-up 70% V_{DIFF} - 90% V_{Cansup}(min)	0	-	200	µs	E.062
t_{WUP} - RXD	time between WUP (3) on the CAN bus until RXD is active (i.e. the CAN signal is represented at the RXD output)	Wake-up-pattern wake-up RXD output enabled Tested by scan	0	-	1	ms	E.063
$t_{VCANSUPlow}$	Filter time needed to display CANSUPlow flag	Tested by scan	-	5	-	µs	E.111

1. *TBit(RXD) for the highest supported data rate has to be specified (1 Mb/s, 2 Mb/s or 5 Mb/s).*
2. *At the expiration of this filter time a flag is set.*
3. *Time starts with the end of last dominant phase of the WUP.*

Table 49. CAN receiver input resistance

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$I_{Leakage,CANH,105}$	Input leakage current CANH	Unpowered device; V_{CANH} = 5 V; V_{CANL} = 5 V V_{SREG} < V_{POR_F}(1) V_{SREG}, V_{CANSUP}(2) connected via 0 Ω to GND V_{SREG}, V_{CANSUP}(2) connected via 47 kΩ to GND T_J = -40 °C to 105 °C	-10	-	10	µA	E.064
$I_{Leakage,CANH,130}$		Unpowered device; V_{CANH} = 5 V; V_{CANL} = 5 V V_{SREG} < V_{POR_F}(1) V_{SREG}, V_{CANSUP}(2) connected via 0 Ω to GND V_{SREG}, V_{CANSUP}(2) T_J = 130 °C	-12		12	µA	E.065
$I_{Leakage,CANL,105}$	Input leakage current CANL	Unpowered device; V_{CANH} = 5 V; V_{CANL} = 5 V V_{SREG} < V_{POR_F}(1) V_{SREG}, V_{CANSUP}(3)connected via 0 Ω to GND V_{SREG}, V_{CANSUP}(4) T_J = -40 °C to 105 °C	-10	-	10	µA	E.066
$I_{Leakage,CANL,130}$		Unpowered device; V_{CANH} = 5 V; V_{CANL} = 5 V V_{SREG} < V_{POR_F} (1) V_{SREG}, V_{CANSUP}(3) connected via 0 Ω to GND V_{SREG}, V_{CANSUP} connected via 47 kΩ to GND(4)	-12		12	µA	E.067

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
	Input leakage current CANL	T_J = 130 °C		-			

1. *V_{SREG} not floating.*
2. *Related to the external supply pin of the CAN-transceiver. If the transceiver supply is generated entirely inside of the device the parameter is measured with respect to the supply of the device.*
3. *Related to the external supply pin of the CAN-transceiver. If the transceiver supply is generated entirely inside of the device the parameter is measured with respect to the supply of the device; if the transceiver is supplied by its own supply pin, this pin has to fulfill this specification as well as the supply that is used to generate the transceiver voltage in case it is on the same device.*
4. *Related to the external supply pin of the CAN-transceiver. If the transceiver supply is generated entirely inside of the device the parameter is measured with respect to the supply of the device; if the transceiver is supplied by its own supply pin, this pin has to fulfill this specification as well as the supply that is used to generate the transceiver voltage in case it is on the same device. It is connected via 47 kΩ to GND.*

Table 50. Biasing control timings

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{filter}	CAN activity filter time	Tested by scan	0.5	-	1.8	µs	E.068
t_{wake}	Wake-up time out	Tested by scan	0.8	1	5	ms	E.069
$t_{Silence}$	CAN timeout	Tested by scan	600	700	1200	ms	E.070
T_{Bias}	CAN bias reaction time	-	-	-	250	µs	E.112

5.14 LIN transceiver (only for SPSB0815 and SPSB0813)

LIN ISO 17987-4:2016 compliant. For data rates up to 20 Kbit/s

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_{SREG} ≤ 18 V; T_J = from -40 °C to 150 °C unless otherwise specified.

Table 51. LIN transmit data input: pin TxD

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{TXDLOW}	Input voltage dominant level	Active mode	1.0	1.45	-	V	E.071
$V_{TXDHIGH}$	Input voltage recessive level	Active mode	-	1.85	2.3	V	E.072
V_{TXDHYS}	$V_{TXDHIGH}$ - V_{TXDLOW}	Active mode	0.2	0.4	-	V	E.073
R_{TXDPU}	TXD pulls up resistor	Active mode	13	29	49	kΩ	E.074

Table 52. LIN receive data output: pin RxD

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{RXDLOW}	Output voltage dominant level	Active mode	-	0.2	0.5	V	E.075
$V_{RXDHIGH}$	Output voltage recessive level	Active mode	V1 - 0.5	V1 - 0.2	-	V	E.076

Table 53. LIN transmitter and receiver: pin LIN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{THdom}	Receiver threshold voltage recessive to dominant state	-	0.4 * V_{SREG}	0.45 * V_{SREG}	0.5 * V_{SREG}	V	E.077

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{Busdom}	Receiver dominant state	-	-	-	0.4 * V_{SREG}	V	E.078
V_{THrec}	Receiver threshold voltage dominant to recessive state	-	0.5 * V_{SREG}	0.55 * V_{SREG}	0.6 * V_{SREG}	V	E.079
V_{Busrec}	Receiver recessive state	-	0.6 * V_{SREG}	-	-	V	E.080
V_{THhys}	Receiver threshold hysteresis: V_{THrec} - V_{THdom}	-	0.07 * V_{SREG}	0.1 * V_{SREG}	0.175 * V_{SREG}	V	E.081
V_{THcnt}	Receiver tolerance center value: (V_{THrec} + V_{THdom})/2	-	0.475 * V_{SREG}	0.5 * V_{SREG}	0.525 * V_{SREG}	V	E.082
V_{THwkup}	Receiver wakeup threshold activation voltage (rising edge)	-	0.5 * V_{SREG}	0.55 * V_{SREG}	0.6 * V_{SREG}	V	E.083
$V_{THwkdwn}$	Receiver wakeup threshold activation voltage(falling edge)	-	0.4 * V_{SREG}	0.45 * V_{SREG}	0.5 * V_{SREG}	V	E.084
t_{linbus}	LIN Bus wake-up dominant filter time	Sleep mode; edge: rec-dom; tested by scan	40	64	80	µs	E.085
t_{dom_LIN}	LIN Bus wake-up dominant filter time	Sleep mode; edge: rec-dom-rec; tested by scan	28	-	-	µs	E.086
$I_{LINDomSC}$	Transmitter input current limit in dominant state	V_{TXD} = V_{TXDLOW} V_{LIN} = V_{BAT} = 18 V	40	100	180	mA	E.087
$I_{bus\_PAS\_dom}$	Input leakage current at the receiver incl. pull-up resistor	V_{TXD} = $V_{TXDHIGH}$ V_{LIN} = 0 V V_{BAT} = 12 V slave mode	-1	-	-	mA	E.088
$I_{bus\_PAS\_rec}$	Transmitter input current in recessive state	In standby modes V_{TXD} = $V_{TXDHIGH}$ V_{LIN} > 8 V V_{BAT} < 18 V V_{LIN} > = V_{BAT}	-	-	20	µA	E.089
$I_{bus\_NO\_GND}$	Input current if loss of GND at device	GND = V_{SREG} 0 V < V_{LIN} < 18 V V_{BAT} = 12 V	-1	-	1	mA	E.090
I_{bus}	Input current if loss of V_{BAT} at device	GND = V_{SREG} 0 V < V_{LIN} < 18 V	-	-	30	µA	E.091
V_{LINdom}	LIN voltage level in dominant state	Active mode; V_{TXD}=V_{TXDLOW} R_{bus} = 500 Ω	-	-	1.2	V	E.092
V_{LINrec}	LIN voltage level in recessive state	Active mode; V_{TXD} = $V_{TXDHIGH}$ I_{LIN} = 10 µA	0.8 * V_{SREG}	-	-	V	E.093

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
R_{LINup}	LIN output pulls up resistor	V_{LIN} = 0 V	20	40	60	kΩ	E.094
C_{LIN}(1)	LIN input capacitance	-	-	-	30	pF	E.095

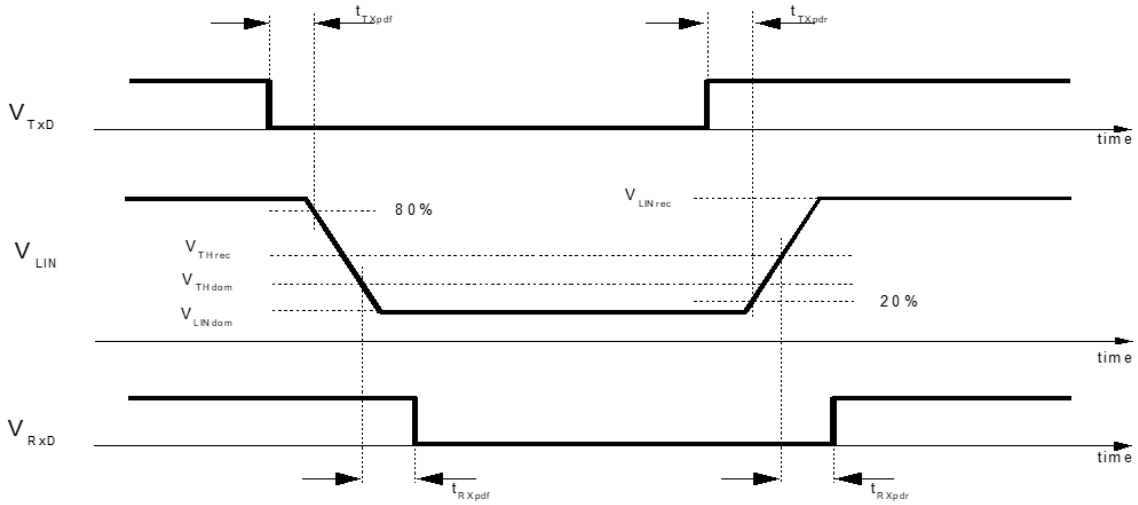
1. *Guaranteed by design.*

Table 54. LIN transceiver timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{RXpd}	Receiver propagation delay time	t_{RXpd} = max (t_{RXpdr}, t_{RXpdf}) t_{RXpdf} = t(0.5 V_{RXD}) - t(0.45 V_{LIN}) t_{RXpdr} = t(0.5 V_{RXD}) - t(0.55 V_{LIN}) V_{SREG} = 12 V, C_{RXD} = 20 pF R_{bus} = 1k Ω, C_{bus} = 1 nF R_{bus} = 660 Ω, C_{bus} = 6.8 nF R_{bus} = 500 Ω, C_{bus} = 10 nF	-	-	6	µs	E.096
t_{RXpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	t_{RXpd_sym} = t_{RXpdr} - t_{RXpdf} V_{SREG} = 12 V R_{bus} = 1 kΩ, C_{bus} = 1 nF C_{RXD} = 20 pF	-2	-	2	µs	E.097
D1	Duty cycle 1	TH_{Rec}(max) = 0.744 * V_{SREG} TH_{Dom}(max) = 0.581 * V_{SREG} V_{SREG} = 7…18 V, t_{bit}= 50 µs D1 = t_{bus_rec}(min)/(2xt_{bit}) R_{bus} = 1 kΩ, C_{bus} = 1 nF R_{bus} = 660 Ω, C_{bus} = 6.8 nF R_{bus} = 500 Ω, C_{bus} = 10 nF	0.396	-	-	-	E.098
D2	Duty cycle 2	TH_{Rec}(min) = 0.422 * V_{SREG} TH_{Dom}(min) = 0.284 * V_{SREG} V_{SREG} = 7.6…18 V, t_{bit} = 50 µs D2 = t_{bus_rec}(max)/(2xt_{bit}) R_{bus} = 1 kΩ, C_{bus} = 1 nF R_{bus} = 660 Ω, C_{bus} = 6.8 nF R_{bus} = 500 Ω, C_{bus} = 10 nF	-	-	0.581	-	E.099
D3	Duty cycle 3	TH_{Rec}(max) = 0.778 * V_{SREG} TH_{Dom}(max) = 0.616 * V_{SREG} V_{SREG}=7…18 V, t_{bit} = 96 µs D3 = t_{bus_rec}(min)/(2xt_{bit}) R_{bus} = 1 kΩ, C_{bus} = 1 nF R_{bus} = 660 Ω, C_{bus} = 6.8 nF R_{bus} = 500 Ω, C_{bus} = 10 nF	0.417	-	-	-	E.100
D4	Duty cycle 4	TH_{Rec}(min) = 0.389 * V_{SREG} TH_{Dom}(min) = 0.251 * V_{SREG}	-	-	0.590	-	E.101

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
		V_{SREG} = 7.6…18 V, t_{bit} = 96 µs D4 = $t_{bus\_rec}(max)/(2xt_{bit})$ R_{bus} = 1 kΩ, C_{bus} = 1 nF R_{bus} = 660 Ω, C_{bus} = 6.8 nF R_{bus} = 500 Ω, C_{bus} = 10 nF					
$t_{dom(TXDL)}$	TXDL dominant time-out	Tested by scan	-	12	-	ms	E.102
t_{LIN}	LIN permanent recessive time-out	Tested by scan	-	40	-	µs	E.103
Tdom(bus)	LIN Bus permanent dominant time-out	Tested by scan	-	12	-	ms	E.104

Figure 34. LIN transmit, receive timing



5.15 SPI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
6 V < V_{SREG} < 18 V; all outputs open; T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 55. Input: CSN

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
VCSNLOW	Input voltage low level	Normal mode, V1 = 5 V	1.0	1.45	-	V	B.001
VCSNHIGH	Input voltage high level	Normal mode, V1 = 5 V	-	1.85	2.3	V	B.002
VCSNHYS	VCSNHIGH - VCSNLOW	Normal mode, V1 = 5 V	0.2	0.4	-	V	B.003
ICSNPU	CSN pull up resistor	Normal mode, V1 = 5 V	13	29	46	kΩ	B.004

Table 56. Inputs: CLK, DI

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{set}	Delay time from V1_standby mode to active mode	Switching from V1_standby mode to active mode using SPI wake- up access. Time until output drivers(p-channel) are enabled after CSN going to high	-	60	-	µs	B.005

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
		Tested by scan					
$V_{in\ L}$	Input low level	V1 = 5 V	1.0	1.45	-	V	B.007
$V_{in\ H}$	Input low level	V1 = 5 V	-	1.8	2.3	V	B.008
$V_{in\ Hyst}$	Input hysteresis	V1 = 5 V	0.2	0.4	-	V	B.009
I_{in}	Pull down current at input	V_{in} = 1 V	5	30	60	µA	B.010
C_{in} (1)	Input capacitance at input CSN, CLK, DI and $PWM_{1,2}$	0 V < V1 < 5.3 V	-	10	15	pF	B.011
f_{CLK}	SPI input frequency at CLK	Tested by scan	-	-	10	MHz	B.012

1. *Value of input capacity is not measured in production test. Parameter guaranteed by design.*

Table 57. DI, CLK and CSN timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{CLK}	Clock period	V1 = 5 V; tested by scan	100	-	-	ns	B.013
t_{CLKH}	Clock high time	V1 = 5 V	40	-	-	ns	B.014
t_{CLKL}	Clock low time	V1 = 5 V	40	-	-	ns	B.015
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V1 = 5 V	150	-	-	ns	B.016
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V1 = 5 V	150	-	-	ns	B.017
$t_{set\ DI}$	DI setup time	V1 = 5 V	25	-	-	ns	B.018
$t_{hold\ DI}$	DI hold time	V1 = 5 V	25	-	-	ns	B.019
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V1 = 5 V (1)	-	-	25	ns	B.020
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V1 = 5 V (1)	-	-	25	ns	B.021

1. *Guaranteed by design.*

Table 58. Output: DO

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{DOL}	Output low level	V1 = 5 V, I_{DO} = -4 mA	-	-	0.5	V	B.022
V_{DOH}	Output high level	V1 = 5 V, I_{DO} = 4 mA	V1-0.5	-	-	V	B.023
I_{DOLK}	Tristate leakage current	V_{CSN} = V1, 0V < V_{DO} <´V1	-10	-	10	µA	B.024
C_{DO} (1)	Tristate input capacitance	V_{CSN} = V1, 0 V < V1 < 5.3 V	-	10	15	pF	B.025

1. *Guaranteed by design.*

Table 59. DO timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$t_{r\ DO}$ (1)	DO rise time	C_L = 50 pF, I_{load} = -1 mA	-	-	25	ns	B.026
$t_{f\ DO}$ (1)	DO fall time	C_L = 50 pF, I_{load} = 1 mA	-	-	25	ns	B.027
$t_{en\ DO\ tri\ L}$ (1)	DO enable time from tristate to low level	C_L = 50 pF, I_{load} = 1 mA Pull-up load to V1	-	50	100	ns	B.028
$t_{dis\ DO\ L\ tri}$ (1)	DO disable time from low level to 3-state	C_L = 50 pF, I_{load} = 4 mA Pull-up load to V1	-	50	100	ns	B.029

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$t_{en\ DO\ tri\ H}$(1)	DO enable time from tristate to high level	C_L = 50 pF, I_{load} = -1 mA Pull-down load to GND	-	50	100	ns	B.030
$t_{d\ DO}$(1)	DO delay time	V_{DO} < 0.3 V1 or V_{DO} > 0.7 V1, C_L = 50 pF	-	25	30	ns	B.031

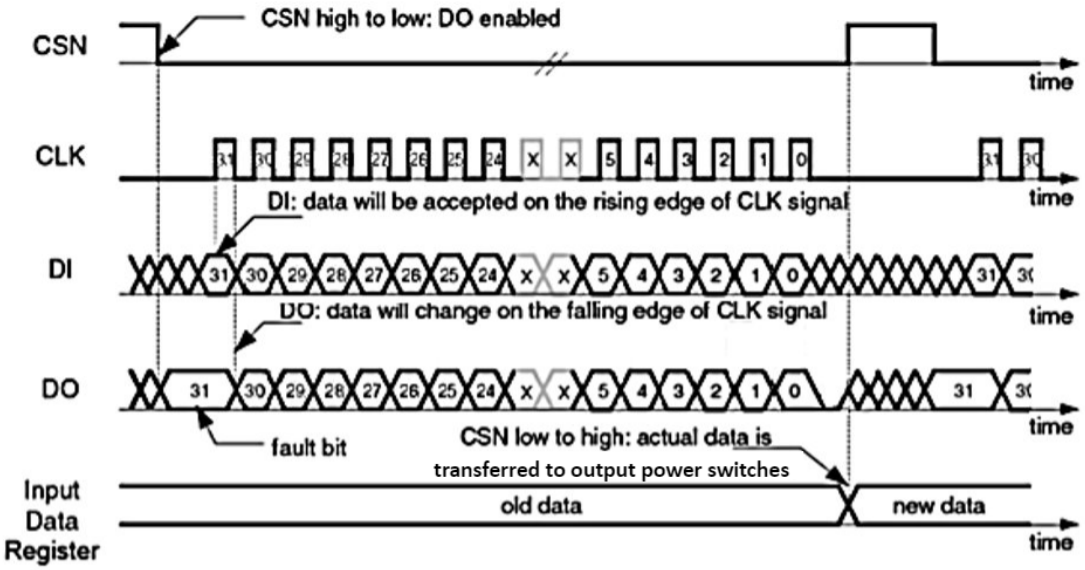
1. *Guaranteed by design.*

Table 60. CSN timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
tCSN_HI,min(1)	Minimum CSN HI time, active mode	Transfer of SPI-command to input register	0.5	-	-	µs	B.032
tCSNfail(1)	CSN low timeout	-	20	35	50	ms	B.033

1. *Guaranteed by design.*

Figure 35. SPI – transfer timing diagram



The SPI can be driven by a microcontroller with its SPI peripheral running in the following mode:
CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 36. **SPI input timing**

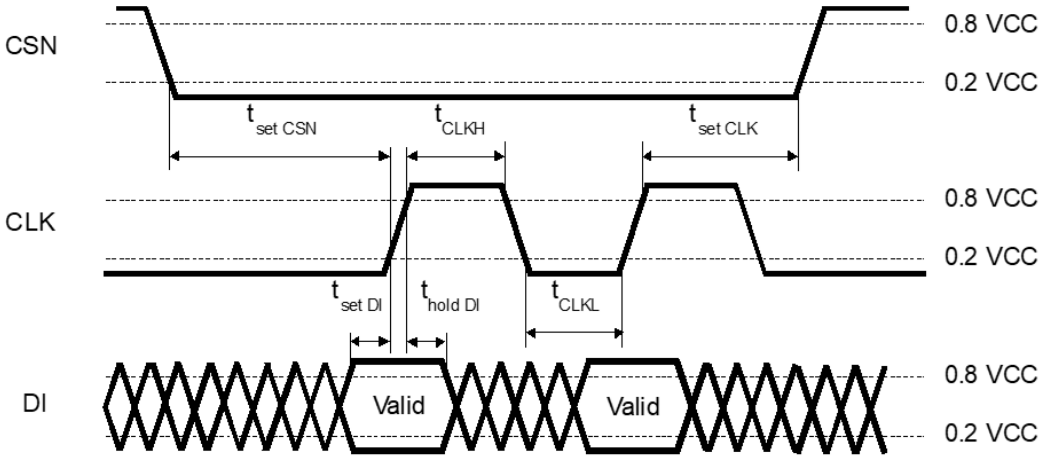


Figure 37. **SPI output timing**

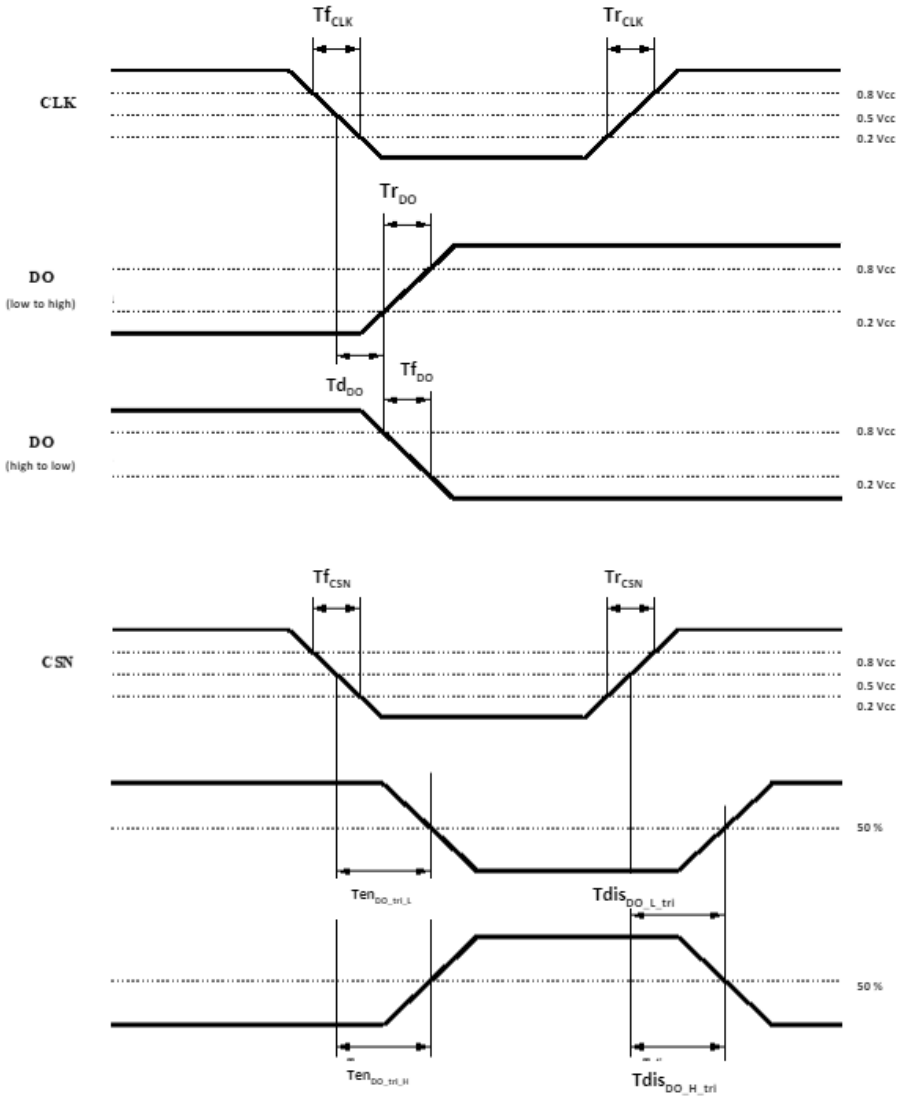


Figure 38. **SPI CSN - output timing**

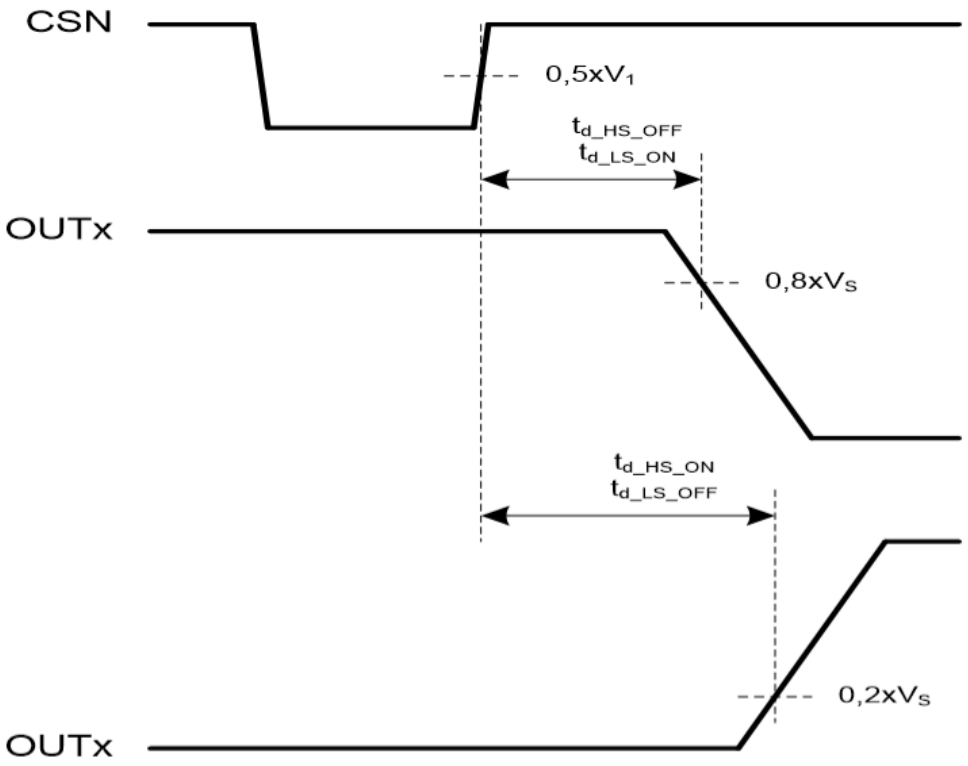
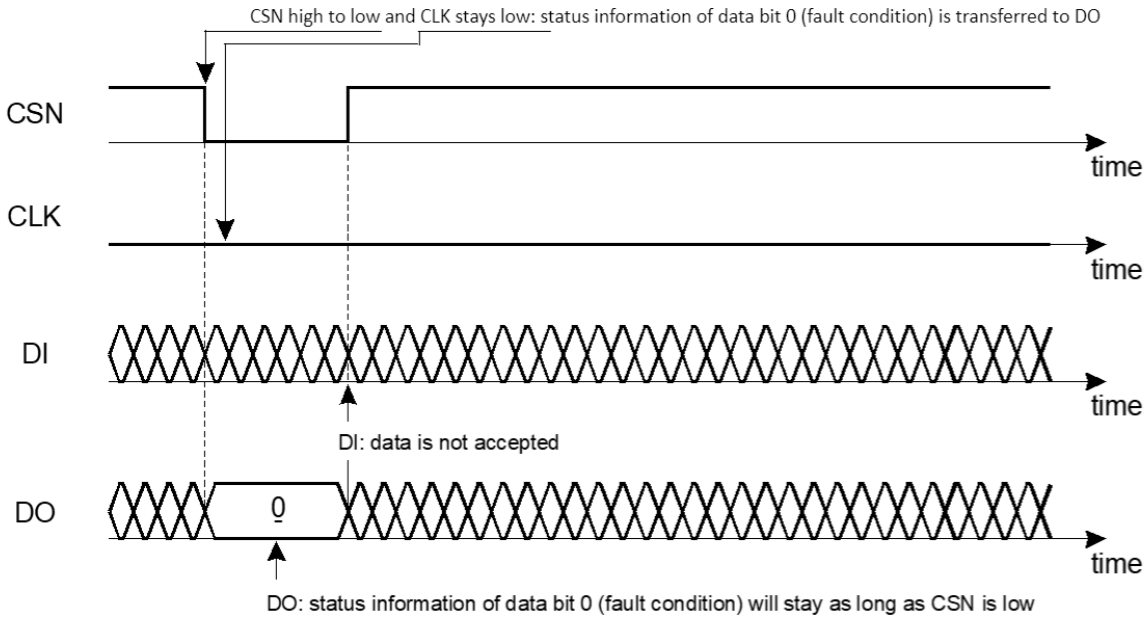


Figure 39. **SPI-CSN low to high transition and global status bit access**



5.16 Debug input

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
6V ≤ V_{SREG} ≤ 18 V, T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 61. Debug input

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{diL}	Input voltage low level	V1 = 3.3 V; 5 V	1	1.45	-	V	A.043
V_{diH}	Input voltage high level	V1 = 3.3 V; 5 V	-	1.8	2.3	V	A.044
V_{diHYS}	Input hysteresis	V1 = 3.3 V; 5 V	0.2	0.4	-	V	A.045
R_{in}	Pull-down resistor	-	13	29	45	kΩ	A.046

5.17 Interrupt output

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{SREG} ≤ 18 V, T_J= from -40 °C to 150 °C, unless otherwise specified.

Table 62. Interrupt output

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
V_{INTL}	Output low level	V1 = 3.3 V 5 V, I_{INT} = -4 mA	-	0.2	0.5	V	A.047
V_{INTH}	Output high level	V1 = 3.3 V 5 V, I_{INT} = 4 mA	V1 - 0.5	V1 - 0.2	-	V	A.048
I_{INTLK}	Tristate leakage current	0 V < V_{INT} < V1	-10	-	10	µA	A.049
$t_{Interrupt}$	Interrupt pulse duration (RxD_L)	Tested by scan	42	56	70	µs	A.050
R_{NINT}	NINT pull up int. resistor	-	10	25	40	kΩ	A.074

5.18 Timer1 and Timer2

6 V ≤ V_{SREG} ≤ 18 V, T_j = from -40 °C to 150 °C, unless otherwise specified.

Table 63. Timer1 and Timer2 values

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
t_{on1}	Timer on time	Tested by scan	-	0.1	-	ms	F.006
t_{on2}	Timer on time	Tested by scan	-	0.3	-	ms	F.007
t_{on3}	Timer on time	Tested by scan	-	1	-	ms	F.008
t_{on4}	Timer on time	Tested by scan	-	10	-	ms	F.009
t_{on5}	Timer on time	Tested by scan	-	20	-	ms	F.010
T1	Timer period	Tested by scan	-	10	-	ms	F.011
T2	Timer period	Tested by scan	-	20	-	ms	F.012
T3	Timer period	Tested by scan	-	50	-	ms	F.013
T4	Timer period	Tested by scan	-	100	-	ms	F.014
T5	Timer period	Tested by scan	-	200	-	ms	F.015

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
T6	Timer period	Tested by scan	-	500	-	ms	F.016
T7	Timer period	Tested by scan	-	1000	-	ms	F.017
T8	Timer period	Tested by scan	-	2000	-	ms	F.018

5.19 SGND loss comparator

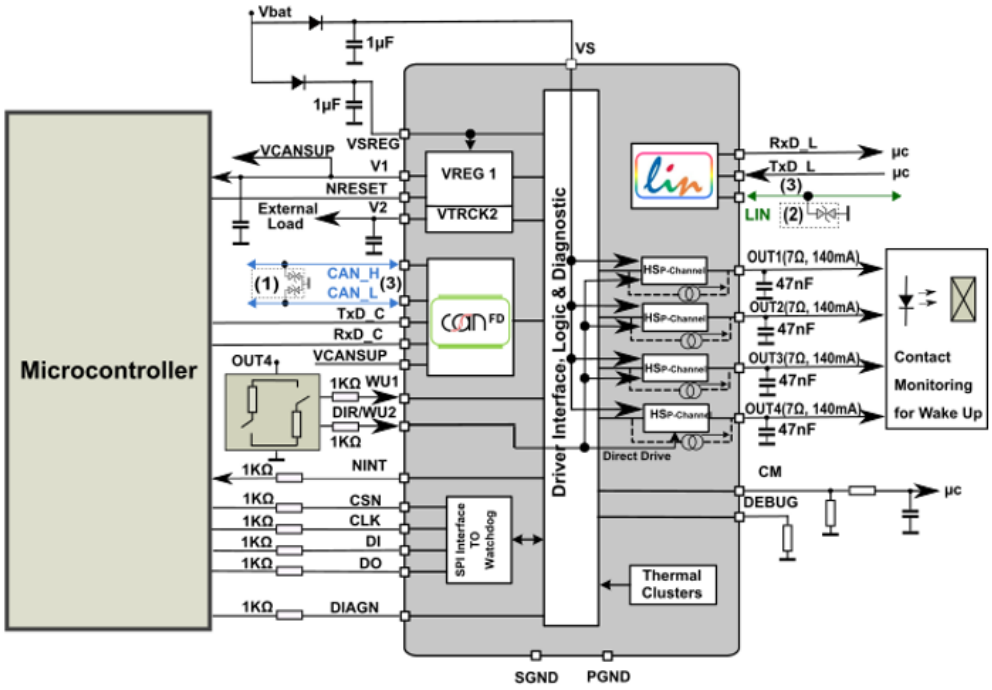
T_J = from -40 °C to 150 °C, unless otherwise specified.

Table 64. SGND loss comparator

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Item
$V_{SGNDloss}$	Input voltage low level	V_{SREG} = 13.5 V	200	400	600	mV	A.052
$t_{SGNDloss}$	Filter time	V_{SREG} = 13.5 V Tested by scan	-	7	-	µs	A.053

6 Application

Figure 40. **Typical application diagram**



1) ST ESDCAN04-2BWY is needed only for SAE J2962-2 compliance
2) ST ESDLIN1524BJ is needed only for SAE J2962-1 compliance
3) In case a LIN/CAN conformance test has to be executed on the device, suitable capacitors have to be placed on the Fixed-Function-Unit pins

7 SPI registers

7.1 Global status byte (GSB)

Table 65. Global status byte (GSB)

Global status byte (GSB)							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
1 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS
Global status bit inverted	Reset	SPI error	Physical layer error (CAN, LIN)	Functional error	Device error	Global warning	Fail safe

Table 66. Global status byte (GSB) description

Bit	Name	Description
31	GSBN	**Global status bit inverted** The GSBN is a logically NOR combination of GSB bits 24 to bit 30(1) This bit can also be used as global status flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low 0 = Error detected (1 or several GSB bits from 24 to 30 are set) 1 = No error detected (default after power on)
30	RSTB	**Reset** The RSTB indicates a device reset and is set in case of the following events: SR1 (0x31) • VPOR • WDFAIL • V1UV (when UV is more than t_{UV1}) • FORCED SLEEP TSD2/V1SC 0 = No reset signal has been generated (default) 1 = Reset signal has been generated RSTB is cleared by a read and clear command to all bits in status register 1 causing the reset event.
29	SPIE(2)	**SPI error bit** The SPIE indicates errors related to a wrong SPI communication SR7 (0x7) • SPI_INV_CMD • SPI_SCK_CNT The bit is also set in case of an SPI CSN time-out detection 0 = No error (default) 1 = Error detected
28	PLE(2)	**Physical layer error** The PLE is a logical OR combination of errors related to the LIN and CAN transceivers SR2 (0x32) and SR6 (0x36) • LIN_PERM_DOM

Bit	Name	Description
		• LIN_TXD_DOM • LIN_PERM_REC • CAN_RXD_REC • CAN_PERM_REC • CAN_PERM_DOM • CAN_TXD_DOM 0 = No error (default) 1 = Error detected PLE is cleared by a read and clear command to all related bits in status registers 2
27	FE	**Functional error bit** The FE is a logical OR combination of errors coming from functional blocks SR2 (0x32) • V2SC SR3 (0x33) • OUTx OC SR4 (0x34)(3) • OUTx OL 0 = No error (default) 1 = Error detected FE is cleared by a read and clear command to all related bits in status registers 2, 3, 4
26	DE	**Device error bit** DE is a logical OR combination of global errors related to the device SR1 (0x31) • TSD1 SR2 (0x32) • VS_OV • VS_UV • VSREG_OV • VSREG_UV • V1_OV 0 = No error (default) 1 = Error detected DE is cleared by a read and clear command to all related bits in status registers 2
25	GW(2)	**Global warning bit** GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch off of functions SR2 (0x32) • V1FAIL • V2FAIL • CAN_RXD_REC • TW(3) • SPI_INV_CMD • SPI SCK CNT SR6 (0x36) • CAN_SUP_LOW 0 = No error (default) 1 = Error detected GW is cleared by a read and clear command to all related bits in status register 2

Bit	Name	Description
24	FS	**Failsafe** The FS bit indicates that the device was forced into a safe state due to the following failure conditions SR1 (0x31) • WDFAIL • V1UV (when UV is more than 2ms) • TSD2 • FORCED SLEEP TSD/V1SC SR2(0x32) • FORCED SLEEP V1OV SR6 (0x36) • SGNDLOSS All control Registers are set to default Control registers are blocked for WRITE access except the following bits CR1 (0x01) • TRIG • CAN_ACT CR2 (0x02) • Timer settings (bits 8…13 and bits 16…21) CR5 (0x05) • OUT1_x (bits 0…2) • OUT2_x (bits 4…6) • OUT3_x (bits 8…10) • OUT4_x (bits 12…14) • CR9 (0x09) to CR11 (0x0B) PWM frequency and duty cycles Config register (0x3F) • V2_0 • V2_1 0 = Fail-safe inactive (default) 1 = Fail-safe active FS is cleared upon exit from fail-safe mode (refer to Section 3.7 Fail safe mode)

1. *Individual failure flags may be masked in the CR1 (0x26).*
2. *Bit may be masked in the configuration register (0x3F), that is, the bit will not be included in the global status bit (GSB).*
3. *Open load status flags may be masked in the Configuration register (0x3F), that is the open load flag will be included in the FE flag, but will not set the GSB. TW failure status flags may be masked in the Configuration register (0x3F), that is the TW flag will be included in the GW flag, but will not set the GSB.*

7.2 Control registers overview

Table 67. Global control registers

Bit								Mode
31	30	29	28	27	26	25	24	
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS	R

Table 68. Control registers overview

Addr.	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x00		MSB	Reserved								
			Reserved								
		LSB	Reserved								
0x01	CR1	MSB	RES	RES	WU2_PU	WU1_PU	RES	RES	WU2_EN	WU1_EN	R/W
			RES	RES	RES	RES	WU2_FILT_1	WU2_FILT_0	WU1_FILT_1	WU1_FILT_0	
		LSB	RES	CAN _REC_ONLY	CAN_ACT	LIN_WU_ EN	CAN_WU_EN	TIME_ NINT _SEL	TIMER_WU_ EN	TRIG	
0x2	CR2	MSB	RES	RES	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	R/W
			RES	RES	T1_ON_2	T1_ON_1	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	
		LSB	V1_RESET_1	V1_RESET_0	V1_OVP	WD_TIME	V2_TKR	V2_RAIL	STBY_SEL	GO_STBY	
0x3	CR3	MSB	VSREG_LOCK_ EN	VS_LOCK_EN	RES	RES	VS_OV_SD_EN	VS_UV_SD_EN	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0xa	CR4	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x5	CR5	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	OUT4_2	OUT4_1	OUT4_0	RES	OUT3_2	OUT3_1	OUT3_0	
		LSB	RES	OUT2_2	OUT2_1	OUT2_0	RES	OUT1_2	OUT1_1	OUT1_0	
0x6	CR6	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W

Addr.	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x6	CR6		RES	RES	RES	RES	RES	RES	RES	RES	R/W
		LSB	RES	RES	CM	RES	RES	RES	CM_SEL_1	CM_SEL_0	
0x7	CR7	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x8	CR8	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x9	CR9	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	PWM4_FREQ	PWM3_FREQ	PWM2_FREQ	PWM1_FREQ	
0x0A	CR10	MSB	RES	RES	PWM1_DC_9	PWM1_DC_8	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	R/W
			PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	RES	RES	PWM2_DC_9	PWM2_DC_8	
		LSB	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	
0x0B	CR11	MSB	RES	RES	PWM3_DC_9	PWM3_DC_8	PWM3_DC_7	PWM3_DC_6	PWM3_DC_5	PWM3_DC_4	R/W
			PWM3_DC_3	PWM3_DC_2	PWM3_DC_1	PWM3_DC_0	RES	RES	PWM4_DC_9	PWM4_DC_8	
		LSB	PWM4_DC_7	PWM4_DC_6	PWM4_DC_5	PWM4_DC_4	PWM4_DC_3	PWM4_DC_2	PWM4_DC_1	PWM4_DC_0	
0x0C	CR12	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x32	CR5	MSB	-	-	PWM9_DC_9	PWM9_DC_8	PWM9_DC_7	PWM9_DC_6	PWM9_DC_5	PWM9_DC_4	R/W
			PWM9_DC_3	PWM9_DC_2	PWM9_DC_1	PWM9_DC_0	-	-	PWM10_DC_9	PWM10_DC_8	
		LSB	PWM10_DC_7	PWM10_DC_6	PWM10_DC_5	PWM10_DC_4	PWM10_DC_3	PWM10_DC_2	PWM10_DC_1	PWM10_DC_0	
0x0D	CR13	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x0E	CR14	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	

Addr.	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x0F	CR15	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x10	CR16	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x11	CR17	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x12	CR18	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x13	CR19	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x14	CR20	MSB	RES	RES	RES	TSD_CLUSTER_EN	OUT4_CCM_EN	OUT3_CCM_EN	OUT2_CCM_EN	OUT1_CCM_EN	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x3B	CR14	MSB	-	-	-	-	-	-	-	-	R/W
			HS0_3	HS0_2	HS0_1	HS0_0	HS15_3	HS15_2	HS15_1	HS15_0	
		LSB	HS14_3	HS14_2	HS14_1	HS14_0	HS13_3	HS13_2	HS13_1	HS13_0	
0x15	CR21	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x16	CR22	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x17	CR23	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W

Addr.	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x17	CR23		RES	RES	RES	RES	RES	RES	RES	RES	R/W
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x22	CR34	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	IWK	ICMP	ICMP_SET	
0x3F	Conf Reg	MSB	CAN_LOOP_EN	LIN_TXD_TOUT_EN	LIN_WU_config	CANTO_NINT_MASK	WU_NINT_MASK	DIAGN_EXT	ICMP_CONFIG_EN	WD_CONFIG_EN	R/W
			-	-	MASK_TW	MASK_RSTB	MASK_OL	RES	MASK_PLE	MASK_GW	
		LSB	MASK_FE	MASK_DE	RES	CAN_AUTO_BIAS	DIR/WU2_EN	V2_1	V2_0	RES	

7.3 Status register overview

Table 69. Global status registers

Bit								Mode
31	30	29	28	27	26	25	24	
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS	R

Table 70. Status registers overview

Addr.	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x31	SR1	MSB	RES	RES	WU2_WAKE	WU1_WAKE	WAKE_CAN	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	R
			V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	
		LSB	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	Forced_Sleep_TSD2/V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR	
0x32	SR2	MSB	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC	CAN_RXD_REC	CAN_PERM_REC	CAN_PERM_DOM	CAN_TXD_DOM	CANTO	R
			FORCED_SLEEP_V1OV	RES	RES	RES	SPI_INV_CMD	SPI_SCK_CNT	V1_OV	TW	
		LSB	V2SC	V2FAIL	V1FAIL	RES	VSREG_OV	VSREG_UV	VS_OV	VS_UV	
0x33	SR3	MSB	RES	RES	OUT4_OC	OUT3_OC	OUT2_OC	OUT1_OC	RES	RES	R
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x34	SR4	MSB	RES	RES	OUT4_OL	OUT3_OL	OUT2_OL	OUT1_OL	RES	RES	R
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x35	SR5	MSB	WD_TIMER_STATE_1	WD_TIMER_STATE_0	RES	RES	WU2_STATE	WU1_STATE	RES	RES	R
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x36	SR6	MSB	RES	RES	RES	RES	RES	RES	RES	RES	R

Addr.	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x36	SR6		RES	RES	RES	RES	RES	RES	RES	RES	R
		LSB	RES	RES	SGNDLOSS	IP_SUP_LOW	CAN_SUP_LOW	RES	RES	RES	
0x37	SR7	MSB	RES	RES	RES	RES	TSD1 CL4	TSD1 CL3	TSD1 CL2	TSD1 CL1	R
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	
0x38	SR8	MSB	RES	RES	RES	RES	TW CL4	TW CL3	TW CL2	TW CL1	R
			RES	RES	RES	RES	RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	RES	RES	RES	RES	

7.4 Control registers

Table 71. Control register CR1 (0x01)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	WU2_PU	WU1_PU	RES	RES	WU2_EN	WU1_EN	RES	RES	RES	RES	WU2_FILT_1	WU2_FILT_0	WU1_FILT_1	WU1_FILT_0	RES	CAN_REC_ONLY	CAN_ACT	LIN_WU_EN	CAN_WU_EN	TIMER_NINT_SEL	TIMER_WU_EN	TRIG
Access	0 (R)		0 (R/W)		0 (R)		1 (R/W)		0 (R)				0 (R/W)				0 (R)	0 (R/W)		1 (R/W)		0 (R/W)		

Table 72. CR1 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	WU2_PU	Wake-up Input x (WUx): configuration of internal current source
20	WU1_PU	0 = Pull-down (default) 1 = Pull-up
19	RES	Reserved
18	RES	Reserved
17	WU2_EN	Wake-up Input x (WUx) enable
16	WU1_EN	0 = WUx disabled 1 = WUx enabled (default) *Note: For WU2 the setting is only valid if input is configured as wake-up input in configuration register (0x3F).*
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	WU2_FILT_1	WUx FILT_1, 0
10	WU2_FILT_0	00 = Wake-up inputs monitored in static mode (filter time t_{WU_stat}) (default)
9	WU1_FILT_1	01 = Wake-up inputs monitored in cyclic mode with Timer2 (filter time: t_{WU_cyclic}; blanking time 80% of timer ON time)(1)
8	WU1_FILT_0	10 = Wake-up inputs monitored in cyclic mode with Timer1 (filter time: t_{WU_cyclic}; blanking time 80% of timer ON time)(1) 11 = Invalid setting; command is ignored, and SPI INV CMD is set
7	RES	Reserved
6	CAN _REC_ONLY	CAN Receive only Mode 0 = CAN Receive only mode disabled (default) 1 = CAN Receive only mode enabled (CAN Trx must be activated, see CAN_ACT bit)
5	CAN_ACT	CAN Transceiver activation 0 = CAN Trx low power mode (default)

Bit	Name	Description
		1 = CAN Trx active mode At exit from active mode, this bit is set to '0' automatically
4	LIN_WU_EN(2)	Enable wake-up by LIN 0 = Disabled 1 = Enabled (default) *Note: The wake-up behavior is configurable in the configuration register (0x3F)*
3	CAN_WU_EN(2)	Enable wake-up by CAN 0 = Disabled 1 = Enabled (default) *Note: Wake-up occurs at a wake-up event according to ISO 11898-2.*
2	TIMER_NINT _SEL	Select timer for wake-up from standby modes 0 = Timer2 (default) 1 = Timer1
1	TIMER_WU _EN	Enable timer wake-up from standby modes 0 = Timer wake-up disabled (default) 1 = Timer wake-up enabled V1stby mode: device wakes-up after timer expiration and generates NINT pulse Vbatstby mode: device wakes-up after timer expiration and generates Nreset
0	TRIG	Watchdog trigger bit

1. *Lower is the timer duration and major is the contribution of output t_{dON}.*
2. *For SPSB0815 and SPSB0813 either LIN, CAN or WUx must be enabled as wake-up source. For SPSB081C devices (without LIN), the LIN_WU_EN is forced to 0. If DIR_WU2_EN is set to 0, setting all bits 3, 4, 16 and 17 to '0' is an invalid setting. If DIR_WU2_EN is set to 1, setting all bits 3, 4, 16 to '0' is an invalid setting. In case of invalid setting, all wake-up sources will be configured according to default setting and SPI error bit (SPIE) in global status register will be set.*

Table 73. Control register CR2 (0x02)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	T2 ON_2	T2 ON_1	T2 ON_0	T2 PER_2	T2 PER_1	T2 PER_0	RES	RES	T1 ON_2	T1 ON_1	T1 ON_0	T1 PER_2	T1 PER_1	T1 PER_0	V1 RESET_1	V1 RESET_0	V1_OVP	WD_TIME	V2_TKR	V2_RAIL	STBY SEL	GO STBY
Access	0 (R)		0 (R/W)						0 (R)		0 (R/W)								1 (R/W)	0 (R/W)				

Table 74. CR2 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	T2 ON_2	Configuration of Timer2 on-time(1)
20	T2 ON_1	000 = t_{on1} (default)
19	T2 ON_0	001 = t_{on2} 010 = t_{on3} 011 = t_{on4}

Bit	Name	Description
		100 = t_{on5} 101 = invalid setting; command is ignored and SPI INV CMD is set
18	T2 PER_2	Configuration of Timer2 period (1) 000 = T1 (default) 001 = T2 010 = T3 011 = T4 100 = T5 101 = T6 110 = T7 111 = T8
17	T2 PER_1	
16	T2 PER_0	
15	RES	Reserved
14	RES	Reserved
13	T1 ON_2	Configuration of Timer1 on-time(1) 000 = t_{on1} (default) 001 = t_{on2} 010 = t_{on3} 011 = t_{on4} 100 = t_{on5} 101 = Invalid setting; command is ignored and SPI INV CMD is set 110 = Invalid setting; command is ignored and SPI INV CMD is set 111 = Invalid setting; command is ignored and SPI INV CMD is set
12	T1 ON_1	
11	T1 ON_0	
10	T1 PER_2	Configuration of Timer1 period(1) 000 = T1 (default) 001 = T2 010 = T3 011 = T4 100 = T5 101 = T6 110 = T7 111 = T8
9	T1 PER_1	
8	T1 PER_0	
7	V1 RESET_1	Voltage regulator V1 reset level 00 = V_{RT4} (default) 01 = V_{RT3} 10 = V_{RT2} 11 = V_{RT1}
6	V1 RESET_0	
5	V1_OVP	Voltage regulator V1 overvoltage protection set 0 = Disabled 1 = Enabled (default)
4	WD_TIME	Window watchdog trigger time 0 = TSW1 (default) 1 = TSW2 Writing to WD_TIME is blocked unless WD CONFIG EN = 1

Bit	Name	Description
		The modified WD trigger time is valid only after the next trig event. Before it, old TSW value is kept
3	V2_TKR	Voltage regulator V2 configurable as a linear independent LDO or a tracker of the V1 voltage regulator 0 = Linear independent LDO (default) 1 = Tracker of the V1 voltage regulator
2	V2_RAIL	Voltage regulator V2 rail configuration 0 = V2 = 3.3 V (default) 1 = V2 = 5 V
1	STBY SEL	Following are the valid settings: 11 = Go to V1 standby 10 = No transition to standby 01 = Go to VBAT_standby 00 = No transition to standby (default)
0	GO STBY	

1. *When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.*

Table 75. Control register CR3 (0x03)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	VSREG_LOCK_ENA	VS_LOCK_ENA	RES	RES	VS_OV_SD_EN	VS_UV_SD_EN	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	1 (R/W)		0 (R)		1 (R/W)		0 (R)		0 (R)															

Table 76. CR3 signals description

Bit	Name	Description
23	VSREG_LOCK_EN	Lockout of V_{SREG} related outputs after V_{SREG} over-/undervoltage shutdown 0 = V_{SREG} related outputs are turned on automatically and status bits (VSREG_UV, VSREG_OV) are cleared 1 = V_{SREG} related outputs remain turned off until status bits (VSREG_UV, VSREG_OV) are cleared (default) *Note: Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions.*
22	VS_LOCK_EN	Lockout of V_S related outputs after V_S over-/undervoltage shutdown 0 = V_S related outputs are turned on automatically and status bits (VS_UV, VS_OV) are cleared 1 = V_S related outputs remain turned off until status bits (VS_UV, VS_OV) are cleared (default) *Note: Lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions.*
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	
15	RES	Reserved
14	RES	
13	RES	Reserved
12	RES	
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 77. Control register CR4 (0x04)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 78. **CR4 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 79. **Control register CR5 (0x05)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	OUT4_2	OUT4_1	OUT4_0	RES	OUT3_2	OUT3_1	OUT3_0	RES	OUT2_2	OUT2_1	OUT2_0	RES	OUT1_2	OUT1_1	OUT1_0
Access	0 (R)									0 (R/W)			0 (R)	0 (R/W)			0 (R)	0 (R/W)			0 (R)	0 (R/W)		

Table 80. **CR5 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved

Bit	Name	Description
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	OUT4_2	High side driver OUT4 configuration OUT4_2,1,0: 000 = Off (default) 001 = On 010 = Timer1 011 = Timer2 100 = PWM4 101 = DIR/WU2 110 = Off 111 = Off
13	OUT4_1	
12	OUT4_0	
11	RES	Reserved
10	OUT3_2	High side driver OUT3 configuration OUT3_2,1,0: 000 = Off (default) 001 = On 010 = Timer1 011 = Timer2 100 = PWM3 101 = DIR/WU2 110 = Off 111 = Off
9	OUT3_1	
8	OUT3_0	
7	RES	Reserved
6	OUT2_2	High side driver OUT2 configuration OUT2_2,1,0: 000 = Off (default) 001 = On 010 = Timer1 011 = Timer2 100 = PWM2 101 = DIR/WU2 110 = Off 111 = Off
5	OUT2_1	
4	OUT2_0	
3	RES	Reserved
2	OUT1_2	High side driver OUT1 configuration OUT1_2,1,0: 000 = Off (default) 001 = On 010 = Timer1 011 = Timer2 100 = PWM1
1	OUT1_1	
0	OUT1_0	

Bit	Name	Description
		101 = DIR/WU2 110 = Off 111 = Off

Table 81. Control register CR6 (0x06)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	CM	RES	RES	RES	CM SEL_1	CM SEL_0
Access	0 (R)																		1 (R/W)	0 (R/W)				

Table 82. CR6 signals description

Bit	Name	Description.
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	CM	Current monitor: 0 = Off (tristate) 1 = On (default)
3	RES	Reserved
4	RES	Reserved
2	RES	Reserved
1	CM SEL_1	A current image of the selected binary coded output is multiplexed to the CM output
0	CM SEL_0	CM SEL_1, 0, selected output 00 = OUT1 (default)

Bit	Name	Description.
		01 = OUT2 10 = OUT3 11 = OUT4

Table 83. Control register CR7 (0x07)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 84. CR7 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 85. Control register CR8 (0x08)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 86. CR8 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 87. Control register CR9 (0x09)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	PMW4 FREQ	PMW3 FREQ	PMW2 FREQ	PMW1 FREQ
Access	0 (R)																				0 (R/W)			

Table 88. **CR9 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	PWM4_FREQ	Select PWM4 frequency 0 = f_{PWM1} = 125 Hz (default) 1 = f_{PWM2} = 250 Hz
2	PWM3_FREQ	Select PWM3 frequency 0 = f_{PWM1} = 125 Hz (default) 1 = f_{PWM2} = 250 Hz
1	PWM2_FREQ	Select PWM2 frequency 0 = f_{PWM1} = 125 Hz (default) 1 = f_{PWM2} = 250 Hz
0	PWM1_FREQ	Select PWM1 frequency 0 = f_{PWM1} = 125 Hz (default) 1 = f_{PWM2} = 250 Hz

Table 89. **Control register CR10 (0x0A)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	PWM1 DC_9	PWM1 DC_8	PWM1 DC_7	PWM1 DC_6	PWM1 DC_5	PWM1 DC_4	PWM1 DC_3	PWM1 DC_2	PWM1 DC_1	PWM1 DC_0	RES	RES	PWM2 DC_9	PWM2 DC_8	PWM2 DC_7	PWM2 DC_6	PWM2 DC_5	PWM2 DC_4	PWM2 DC_3	PWM2 DC_2	PWM2 DC_1	PWM2 DC_0
Access	0 (R)		0 (R/W)										0 (R)		0 (R/W)									

Table 90. CR10 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	PWM1 DC_9	Binary coded on-dutycycle of PWM channel PWMx(1) PWM1_DC_9,8...0 duty cycle 0000000000 = Off 0000000001 = 1*100/1024 0000000010 = 2*100/1024 ... ... 1111111101 = 1021*100/1024 1111111110 = 1022*100/1024 1111111111 = 1023*100/1024
20	PWM1 DC_8	
19	PWM1 DC_7	
18	PWM1 DC_6	
17	PWM1 DC_5	
16	PWM1 DC_4	
15	PWM1 DC_3	Binary coded on-duty cycle of PWM channel PWM1 (see above)
14	PWM1 DC_2	
13	PWM1 DC_1	
12	PWM1 DC_0	
11	RES	Reserved
10	RES	Reserved
9	PWM2 DC_9	Binary coded on-dutycycle of PWM channel PWM2 (see below)
8	PWM2 DC_8	
7	PWM2 DC_7	Binary coded on-dutycycle of PWM channel PWM2(1) PWM2_DC_9,8...0 duty cycle 0000000000 = Off 0000000001 = 1*100/1024 0000000010 = 2*100/1024 ... ... 1111111101 = 1021*100/1024 1111111110 = 1022*100/1024 1111111111 = 1023*100/1024
6	PWM2 DC_6	
5	PWM2 DC_5	
4	PWM2 DC_4	
3	PWM2 DC_3	
2	PWM2 DC_2	
1	PWM2 DC_1	
0	PWM2 DC_0	

1. *To have a duty cycle equal to 100%, the output configuration shall be set in ON mode.*

Table 91. Control register CR11 (0x0B)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	PWM1 DC_9	PWM1 DC_8	PWM1 DC_7	PWM1 DC_6	PWM1 DC_5	PWM1 DC_4	PWM1 DC_3	PWM1 DC_2	PWM1 DC_1	PWM1 DC_0	RES	RES	PWM2 DC_9	PWM2 DC_8	PWM2 DC_7	PWM2 DC_6	PWM2 DC_5	PWM2 DC_4	PWM2 DC_3	PWM2 DC_2	PWM2 DC_1	PWM2 DC_0
Access	0 (R)		0 (R/W)										0 (R)		0 (R/W)									

Table 92. CR11 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	PWM1 DC_9	Binary coded on-dutycycle of PWM channel PWMx(1) PWM1_DC_9,8...0 duty cycle 0000000000 = Off 0000000001 = 1*100/1024 0000000010 = 2*100/1024 ... ... 1111111101 = 1021*100/1024 1111111110 = 1022*100/1024 1111111111 = 1023*100/1024
20	PWM1 DC_8	
19	PWM1 DC_7	
18	PWM1 DC_6	
17	PWM1 DC_5	
16	PWM1 DC_4	
15	PWM1 DC_3	Binary coded on-duty cycle of PWM channel PWM1 (see above)
14	PWM1 DC_2	
13	PWM1 DC_1	
12	PWM1 DC_0	
11	RES	Reserved
10	RES	Reserved
9	PWM2 DC_9	Binary coded on-dutycycle of PWM channel PWM2 (see below)
8	PWM2 DC_8	
7	PWM2 DC_7	Binary coded on-dutycycle of PWM channel PWM2(1) PWM2_DC_9,8...0 duty cycle: 0000000000 = Off 0000000001 = 1*100/1024 0000000010 = 2*100/1024 ... ... 1111111101 = 1021*100/1024 1111111110 = 1022*100/1024 1111111111 = 1023*100/1024
6	PWM2 DC_6	
5	PWM2 DC_5	
4	PWM2 DC_4	
3	PWM2 DC_3	
2	PWM2 DC_2	
1	PWM2 DC_1	
0	PWM2 DC_0	

1. *To have a duty cycle equal to 100%, the output configuration shall be set in ON mode.*

Table 93. Control register CR12 (0x0C)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 94. CR12 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved

Bit	Name	Description
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 95. Control register CR13 (0x0D)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 96. CR13 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved

Bit	Name	Description
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 97. Control register CR14 (0x0E)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 98. CR14 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved

Bit	Name	Description
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 99. Control register CR15 (0x0F)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 100. CR15 signals description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 101. **Control register CR16 (0x10)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 102. **CR16 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 103. **Control register CR19 (0x13)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 104. **CR17 to CR19 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 105. **Control register CR20 (0x14)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	TSD_Cluster EN	OUT4_CCM_EN	OUT3_CCM_EN	OUT2_CCM_EN	OUT1_CCM_EN	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)			0 (R/W)	0 (R)																			

Table 106. **CR20 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved

Bit	Name	Description
21	RES	Reserved
20	TSD_Cluster EN	Enables thermal warning and shutdown of outputs by cluster 0 = TSD and TW by cluster off (default) 1 = TSD and TW by cluster on
19	OUT4_CCM_EN	Enable constant current mode for OUT4(1) 0 = Disable (default) 1 = Enable
18	OUT3_CCM_EN	Enable constant current mode for OUT3(1) 0 = Disable (default) 1 = Enable
17	OUT2_CCM_EN	Enable constant current mode for OUT2(1) 0 = Disable (default) 1 = Enable
16	OUT1_CCM_EN	Enable constant current mode for OUT1(1) 0 = Disable (default) 1 = Enable
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

1. *Refer to Section 3.19 Constant current mode for the correct sequence of constant current mode activation.*

Table 107. CR21(0x15) to CR24 (0x18)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	0 (R)																							

Table 108. **CR21(0x15) to CR24 (0x18) signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 109. **Control register CR34 (0x22)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	IWK	ICMP	ICMP_SET
Access	0 (R/W)																					0 (R/W)		

Table 110. **CR34 signals description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved

Bit	Name	Description
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	IWK	Wake-up event on CAN and wake-up pins in V1standby mode 0 = Device moves in active mode (default) 1 = Device remains in V1_standby mode. Interrupt generated on NINT pins
1	ICMP	V1 load current supervision 0 = Enabled: watchdog is disabled in V1_standby when $I_{V1} < I_{CMP}$ (default) 1 = Disabled: watchdog is disabled upon transition into V1_standby mode Setting ICMP = 1 is only possible when ICMP_config_en = 1
0	ICMP_SET	Set thresholds for ICMP: 0 = Low values for rising and falling (default) 1 = High values for rising and falling

Table 111. Configuration register (0x3F)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	CAN_LOOP_EN	LIN_TXD_TOUT_EN	LIN_WU_config	CANTO_NINT_MASK	WU_NINT_MASK	DIAGN_EXT	ICMP_CONFIG_EN	WD_CONFIG_EN	RES	RES	MASK_TW	MASK_RSTB	MASK_OL	RES	MASK_PLE	MASK_GW	MASK_FE	MASK_DE	RES	CAN_AUTO_BIAS	DIR/WU2_EN	V2_1	V2_0	RES
Access	0 (R/W)	1 (R/W)	0 (R/W)						0 (R)		0 (R/W)													0 (R)

Table 112. **Configuration register signals description**

Bit	Name	Description
23	CAN_LOOP_EN	CAN Looping of TxD_C to RxD_C 0 = CAN looping disabled (default) 1 = CAN looping enabled
22	LIN_TXD_TOUT_EN	LIN TxD timeout detection 0 = LIN TxD timeout detection disabled 1 = LIN TxD timeout detection enabled (default)
21	LIN_WU_config	Configuration of LIN wake-up behaviour 0 = Wake-up at recessive - dominant - recessive with t_dom > 28 µs (default), (according to LIN ISO 17987-4/2016 and Hardware Requirements for Transceivers version 1.3) 1 = Wake-up at recessive - dominant or dominant - recessive transition
20	CANTO_NINT_MASK	0 = CAN communication timeout is not masked (default) 1 = CAN communication timeout is masked
19	WU_NINT_MASK	0 = Wake-up is not masked (default) 1 = Wake-up is masked
18	DIAGN_EXT	Fail safe output configuration by DIAGN pin 0 = Only fail safe mode is considered (for example watchdog failure; V1 failure; thermal shutdown TSD2), (default). 1 = DIAGN pin reflects one or more errors such as reported in the GLOBAL STATUS BYTE register by global status bit not (GSBN)
17	ICMP_CONFIG_EN	0 writing ICMP = 1 is blocked (writing ICMP=0 is possible); (default) 1 writing ICMP = 1 is possible with next SPI command bit is automatically reset to 0 after next SPI command
16	WD_CONFIG_EN	0 = Writing to WD configuration (CR2 [0:1] is blocked (default) 1 = Writing to WD configuration bits is possible with next SPI command bit is automatically reset to 0 after next SPI command
15	RES	Reserved
14	RES	Reserved
13	MASK_TW	0 = Thermal warning is not masked (default) 1 = Thermal warning is masked For example it is reported as a global warning (GSB bit 1) but not as a global error (GSB bit 7)
12	MASK_RSTB	0 = V1_UV reset condition is not masked (default) 1 = V1_UV reset condition is masked For example reported as a reset (GSB bit 6) but not as a global error (GSB bit 7)
11	MASK_OL	0 = Open load condition at all outputs are not masked (default) 1 = Open load condition at all outputs are masked For example. it is reported as a functional error (GSB bit 27) but not as a global error (GSB bit 31)
10	RES	Reserved
9	MASK_PLE	0 = Physical layer errors are not masked (default) 1 = Physical layer errors are masked For example reported as a physical layer error (GSB bit 4) but not as a global error (GSB bit 7)
8	MASK_GW	0 = Global warning conditions are not masked (default) 1 = Global warning conditions are masked For example reported as a global warning (GSB bit 1) but not as a global error (GSB bit 7)

Bit	Name	Description
7	MASK_FE	0 = Functional error conditions are not masked (default) 1 = Functional error conditions are masked For example reported as a functional error (GSB bit 27) but not as a global error (GSB bit 31)
6	MASK_DE	0 = Device error conditions are not masked (default) 1 = Device error conditions are masked For example reported as a device error (GSB bit 2) but not as a global error (GSB bit 7)
5	RES	Reserved
4	CAN_AUTO_BIAS	CAN automatic biasing activation 0 = Auto biasing disabled (default) 1 = Auto biasing enabled
3	DIR/WU2_EN(1)	Enable DIR input for direct drive of OUT1..4 0 = WU2 configured as wake-up input (default) 1 = DIR function enabled
2	V2_1	Voltage regulator V2 configuration: 00 = V2 OFF in all modes (default) 01 = V2 ON in active mode; OFF in standby modes 10 = V2 ON in active and V1 standby mode; OFF in VBAT_standby mode 11 = V2 ON in all modes
1	V2_0	
0	RES	Reserved

7.5 Status registers

Table 113. Status register SR1 (0x31)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	WU2_WAKE	WU1_WAKE	WAKE_CAN	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2/V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR
Access	R		R/C							R							R/C							

Table 114. SR1 description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	WU2 WAKE	Shows wake-up source ‘1’ = wake-up Bits are latched until a “read and clear” command
20	WU1 WAKE	

Bit	Name	Description
19	WAKE CAN	Shows wake-up source '1' = wake-up Bits are latched until a "read and clear" command
18	WAKE LIN	
17	WAKE TIMER	
16	DEBUG _ACTIVE	Indicates device is in debug mode '1' = debug mode Bit is latched until a "read and clear" command
15	V1UV	Indicates undervoltage condition at voltage regulator V1 (V1 < V_{RTx}) '1' = undervoltage Bit is latched until a "read and clear" command
14	V1_RESTART_2	Indicates that the number of TSD2 events that caused a restart of voltage regulator V1 Bits cannot be cleared; the counter is automatically cleared if no additional TSD2 event occurs within 1 minute.
13	V1_ RESTART_1	
12	V1_ RESTART_0	
11	WDFAIL_CNT_3	Indicates number of subsequent watchdog failures Bits cannot be cleared; they are cleared with a valid watchdog trigger
10	WDFAIL_CNT_2	
9	WDFAIL_CNT_1	
8	WDFAIL_CNT_0	
7	DEVICE_STATE_1	00 = Active mode after power-on, or after read and clear command 01 = Active mode after wake-up from V_standby mode (before read and clear command) 10 = Active mode after wake-up from VBAT_standby mode (before read and clear command) 11 = Not used Bit is latched until a read&clear command After a "read and clear access", the device state is updated
6	DEVICE_STATE_0	
5	TSD2	Thermal shutdown 2 was reached Bit is latched until a "read and clear" command for Cluster 4 (bit 22 in SR7)
4	TSD1	Thermal shutdown 1 was reached Bit is latched until a "read and clear" command for all clusters (bit 16-23 in SR7)
3	FORCED_SLEEP_TSD2/V1SC	Device entered forced sleep mode due to: • Thermal shutdown or • Short circuit on V1 during startup Bit is latched until a read and clear command
2	FORCED_SLEEP_WD	Device entered forced sleep mode due to multiple watchdog failures Bit is latched until a read and clear command
1	WDFAIL	Watchdog failure Bit is latched until a "read and clear" command
0	VPOR	VREG power-on seset threshold (V_{POR})(1) reached Bit is latched until a "read and clear" command

1. *If V_{POR} is set after a cold startup, the device comes from a power-on reset.*

Table 115. Status register SR2 (0x32)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC	CAN_RXD_REC	CAN_PERM_REC	CAN_PERM_DOM	CAN_TXD_DOM	CANTO	FORCED_SLEEP_V1OV	RES	RES	RES	SPI_INV_CMD	SPI_SCK_CNT	V1_OV	TW	V2SC	V2FAIL	V1FAIL	RES	VSREG OV	VSREG UV	VS OV	VS UV
Access	R/C									R			R/C	R	R/C					R	R/C			

Table 116. SR2 description

Bit	Name	Description
23	LIN_PERM_DOM	LIN bus signal is dominant for t > $T_{dom(bus)}$ Bit is latched until a “read and clear” command
22	LIN_TXD_DOM	TxD_L pin is dominant for t > $t_{dom(TXDL)}$ The LIN transmitter is disabled until the bit is cleared Bit is latched until a “read and clear” command
21	LIN_PERM_REC	LIN bus signal does not follow TxD_L within t_{LIN} The LIN transmitter is disabled until the bit is cleared Bit is latched until a “read and clear” command
20	CAN_RXD_REC	RxD_C has not followed TxD_C for 4 times The CAN transmitter is disabled until the bit is cleared Bit is latched until a “read and clear” command
19	CAN_PERM_REC	CAN bus signal did not follow TxD_C for 4 times The CAN transmitter is disabled until the bit is cleared Bit is latched until a “read and clear” command
18	CAN_PERM_DOM	CAN bus signal is dominant for t > t_{CAN} Bit is latched until a “read and clear” command
17	CAN_TXD_ DOM	TxD_C pin is dominant for t > $t_{dom(TXDC)}$ The CAN transmitter is disabled until the bit is cleared Bit is latched until a “read and clear” command
16	CANTO	CAN communication timeout Bit is set if there is no communication on the bus for t > $t_{Silence}$ CANTO indicates that there was a transition from BIASON to BIASOFF Bit is latched until a read and clear access
15	FORCED_SLEEP_V1 OV	Device entered forced sleep mode due to an overvoltage occurrence on V1 Bit is latched until a “read and clear” command
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	SPI INV CMD	Invalid SPI command ‘1’ indicates one of the following conditions was detected:

Bit	Name	Description
		• access to undefined address • Write operation to status register • DI stuck at '0' or '1' • CSN timeout • Parity failure • invalid or undefined setting The SPI frame is ignored Bit is latched until a “read and clear” command
10	SPI SCK CNT	SPI clock counter ‘1’ indicates that an SPI frame with the wrong number of CLK cycles was detected Bit is latched until a valid SPI frame
9	V1_OV	V1 overvoltage ‘1’ indicates the voltage at V1 has reached the overvoltage threshold Bit is latched until a “read and clear” command
8	TW	Thermal warning ‘1’ indicates that the temperature has reached the thermal warning threshold Bit is latched until a “read and clear” command
7	V2SC	V2 short circuit detection ‘1’ indicates that a short circuit to GND condition of V2 at turn-on of the regulator (V2 < V2_fail for t > tv2_short) Bit is latched until a “read and clear” command
6	V2FAIL	V2 failure detection ‘1’ indicates that a V2 fail event occurred since last readout (V2 < V2_fail for t > tv2_fail) Bit is latched until a “read and clear” command
5	V1FAIL	V1 failure detection ‘1’ indicates that a V1 fail event occurred since last readout (V1 < V1_fail for t > tv1_fail) Bit is latched until a “read and clear” command
4	RES	Reserved
3	VSREG_OV	V_{SREG} overvoltage ‘1’ indicates that the voltage at V_{SREG} has reached the overvoltage threshold Bit is latched until a “read and clear” command
2	VSREG_UV	V_{SREG} undervoltage ‘1’ indicates that the voltage at V_{SREG} has reached the undervoltage threshold Bit is latched until a “read and clear” command
1	VS_OV	V_S overvoltage ‘1’ indicates that the voltage at V_S has reached the overvoltage threshold Bit is latched until a “read and clear” command
0	VS_UV	V_S undervoltage ‘1’ indicates that the voltage at V_S has reached the undervoltage threshold Bit is latched until a “read and clear” command

Table 117. Status register SR3 (0x33)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	OUT4_OC	OUT3_OC	OUT2_OC	OUT1_OC	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	R		R/C				R																	

Table 118. SR3 description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	OUT4_OC	Overcurrent shutdown ‘1’ indicates the output was shut down due to overcurrent condition. Bit is latched until a “read and clear” command
20	OUT3_OC	
19	OUT2_OC	
18	OUT1_OC	
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 119. Status register SR4 (0x34)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	OUT4_OL	OUT3_OL	OUT2_OL	OUT1_OL	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	R		R/C				R																	

Table 120. **SR4 description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	OUT4_OL	Open-load '1' indicates an open-load condition was detected at the output Bit is latched until a "read and clear" command
20	OUT3_OL	
19	OUT2_OL	
18	OUT1_OL	
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 121. **Status register SR5 (0x35)**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WD_TIMER_STATE_1	WD_TIMER_STATE_0	RES	RES	WU2_STATE	WU1_STATE	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	R																							

Table 122. SR5 description

Bit	Name	Description
23	WD_TIMER_STATE_1	Watchdog timer status: 00 = 0 - 33% 01 = 33 - 66% 11 = 66 - 100% 10 = Invalid configuration
22	WD_TIMER_STATE_0	
21	RES	Reserved
20	RES	Reserved
19	WU2_STATE	State of WUx input 0 = Input level is low 1 = Input level is high The bit shows the momentary status of WUx and cannot be cleared (“live bit”)
18	WU1_STATE	
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 123. Status register SR6 (0x36)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	SGNDLOSS	IP_SUP_LOW	CAN_SUP_LOW	RES	RES	RES
Access	R																		R/C			R		

Table 124. SR6 description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	SGNDLOSS	Loss of ground status bit ‘1’ indicates that ground at SGND pin has been lost Bit is not latched
4	IP_SUP_LOW	Internal IP voltage supply (analog and/or digital) is less than 3 V Bit is latched until a “read and clear” command
3	CAN_SUP_LOW	Voltage at the CAN supply pin reached the CAN supply low warning threshold $V_{CANSUP} < V_{CANSUPlow}$ Bit is latched until a “read and clear” command
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 125. Status register SR7 (0x37)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	R				R/C				R															

Table 126. SR7 description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	TSD1_CL4	Thermal shutdown of Cluster x '1' indicates Cluster x has reached the thermal shutdown threshold (TSD1) and the output cluster was shut down Bit is latched until a "read and clear" command of this bit only
18	TSD1_CL3	
17	TSD1_CL2	
16	TSD1_CL1	
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

Table 127. Status register SR8 (0x38)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RES	RES	RES	RES	TW_CL4	TW_CL3	TW_CL2	TW_CL1	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
Access	R				R/C				R															

Table 128. SR8 description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	TW_CL4	Thermal warning for Cluster x '1' indicates Cluster x has reached the thermal warning threshold

Bit	Name	Description
18	TW_CL3	Bit is latched until a “read and clear” command of this bit only
17	TW_CL2	
16	TW_CL1	
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	RES	Reserved
2	RES	Reserved
1	RES	Reserved
0	RES	Reserved

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN32L Epad (5.0x5.0x1.0 mm) package information

Figure 41. QFN32L Epad (5.0x5.0x1.0 mm) package outline

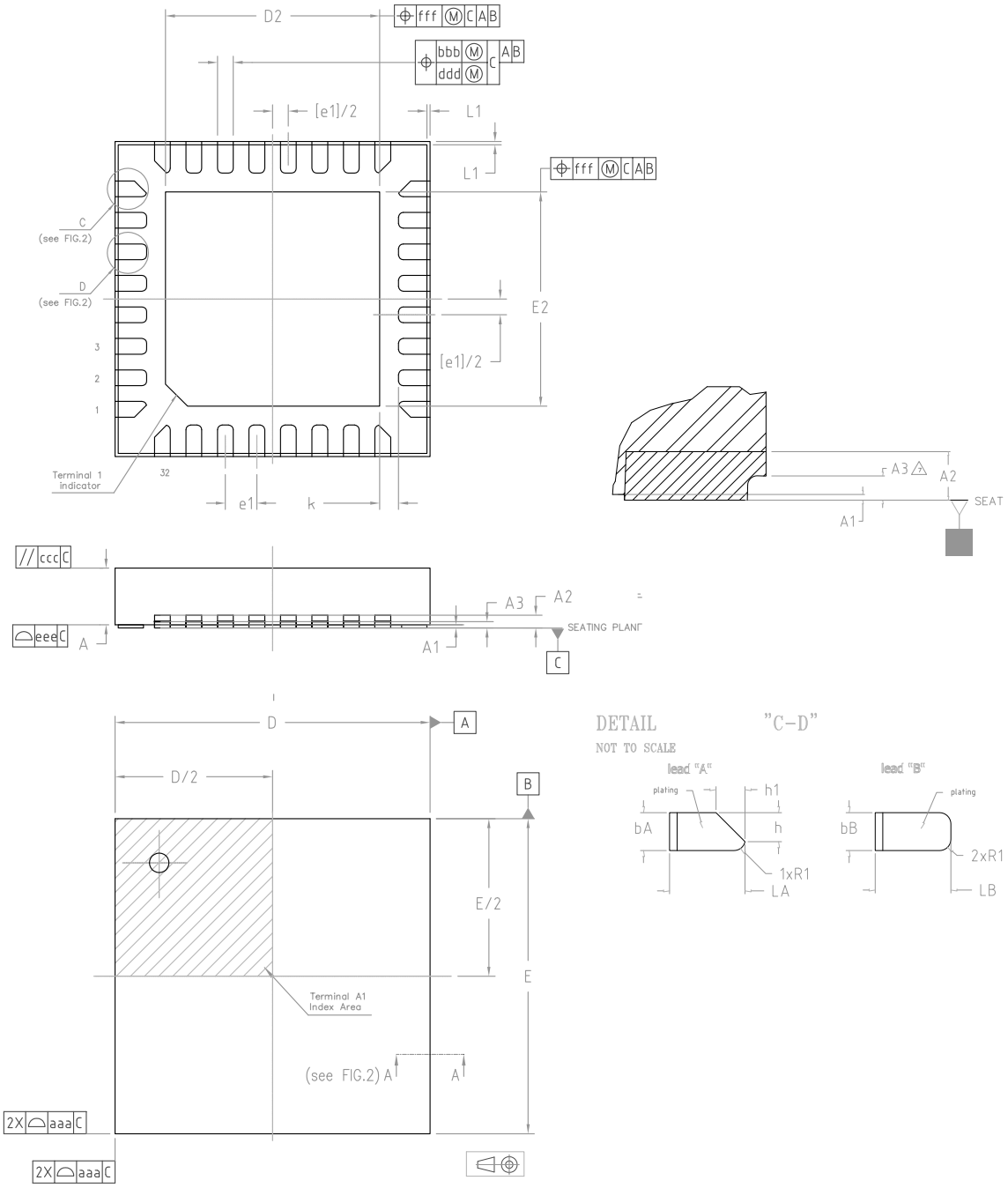


Table 129. QFN32L Epad (5.0x5.0x1.0 mm) package mechanical data

Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	-	0.05
A2	-	0.2 REF	-
A3	0.1	-	-
D		5.00 BSC	
D2	3.40	3.50	3.60
E		5.00 BSC	
E2	3.40	3.50	3.60
e1		0.5 BSC	
k	0.20	-	-
L1	-	.	0.05
La	0.40	0.50	0.50
bA	0.20	0.25	0.30
h	-	0.19 REF	-
h1	-	0.19 REF	-
LB	0.45	0.5	0.55
bB	0.20	0.25	0.30
N		32	
R1	-	-	0.1
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Revision history

Table 130. **Document revision history**

Date	Version	Changes
05-Oct-2022	1	Initial release.
12-Dec-2022	2	Updated: • Section Features; • Table 3. ESD protection; • Table 72. CR1 signals description; • Table 106. CR20 signals description. Minor text changes in: • Section 3.11.1 Features; • Section 3.11.3 Wake-up from standby modes; • Section 3.12.1 Features; • Table 8. Functional overview. Minor text changes to improve readability.

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