EFM8 Universal Bee Family
EFM8UB3 Data Sheet

The EFM8UB3, part of the Universal Bee family of MCUs, is a multi-purpose line of 8-bit microcontrollers with USB feature set in small packages.

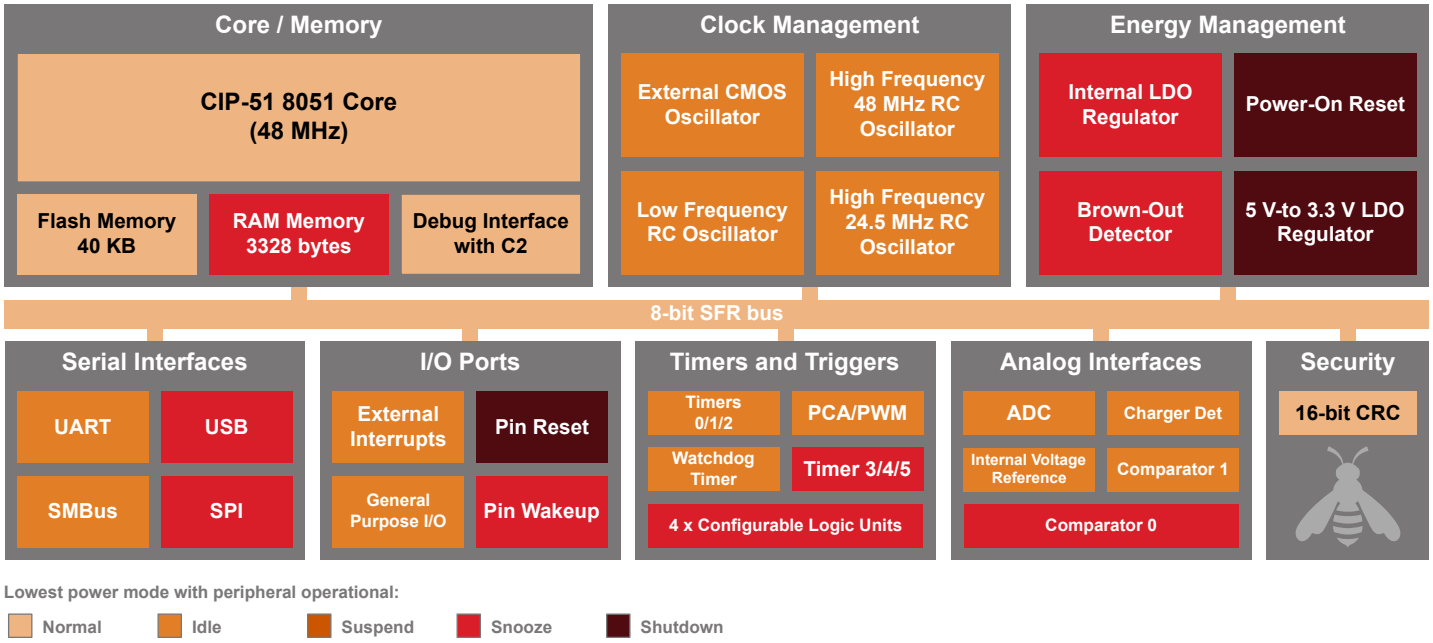
These devices offer high value by integrating an innovative energy-smart USB peripheral interface, charger detect circuit, 8 kV ESD protection, and enhanced high speed communication interfaces into small packages, making them ideal for space-constrained USB applications. With an efficient 8051 core and precision analog, the EFM8UB3 family is also optimal for embedded applications.

EFM8UB3 applications include the following:

- USB I/O controls
- Docking stations/USB hubs
- Dongles
- Consumer electronics
- USB Type-C converters
- USB Type-C billboard/alternate mode

KEY FEATURES

- Pipelined 8-bit C8051 core with 48 MHz maximum operating frequency
- Up to 17 multifunction I/O pins
- Low Energy USB with full- and low-speed support saves up to 90% of the USB energy
- USB charger detect circuit (USB-BCS 1.2 compliant)
- One 12-bit ADC and two analog comparators with internal voltage DAC as reference input
- Six 16-bit timers
- UART and SMBus master/slave
- Priority crossbar for flexible pin mapping



1. Feature List

The EFM8UB3 highlighted features are listed below.

- **High-speed CIP-51 MCU Core**
  - Pipelined instruction architecture; executes 70% of instruction set in 1 or 2 system clocks
  - Up to 48 MIPS throughput with 48 MHz clock
  - Uses standard 8051 instruction set
  - Expanded interrupt handler
- **Memory**
  - 40 KB Flash
  - Flash is in-system programmable in 512-byte sectors
  - 3328 bytes RAM, including:
    - 256 bytes standard 8051 RAM
    - 2048 bytes on-chip XRAM
    - 1024 bytes of USB buffer
- **On-chip Debug**
  - On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
  - Provides 4 hardware breakpoints, single stepping, inspect/modify memory and registers
- **12-bit Analog-to-Digital Converter**
  - Multiple selectable inputs
  - Up to 800 ksps 10-bit mode
  - Precise Internal VREF 1.65 V or external VREF supported
- **Clock Sources**
  - 48 MHz ± 1.5% precision internal oscillator and ±0.25% using USB clock recovery
  - 24.5 MHz low power internal oscillator with ±2% accuracy
  - 80 kHz low-frequency, low power internal oscillator (LFO)
  - External CMOS clock option
  - Flexible clock divider: Reduce frequency by up to 128x from any clock source
- **2 x Analog Comparators**
  - Multiplexed selectable inputs
  - Integrated 6-bit programmable reference voltage selectable as comparator input channel
  - Programmable hysteresis and response time
  - 400 nA current consumption in low power mode
- **Power Management**
  - 5 V-input LDO regulator for direct connection to USB supply
    - External LDO is needed for USB-C VBUS powered applications that require more than 5 V.
  - Internal low dropout (LDO) regulator for CPU core voltage
  - Power-on reset and brownout detect circuit
  - Multiple power modes supported to minimize power consumption while maintaining performance
- **General-Purpose I/O**
  - Up to 17 pins
  - V_{IO} + 2.5 V tolerant; push-pull or open-drain
  - Priority crossbar to support flexible digital peripheral pin assignments
- **Timers/Counters/PWM**
  - 6 general purpose 16-bit counters/timers
  - 16-bit Programmable Counter Array (PCA) with 3 channels of PWM, capture/compare, or frequency output capability, and hardware kill/safe state capability
  - Independent watchdog timer, clocked from the low frequency oscillator
- **Communication Interfaces and Digital Peripherals**
  - UART, up to 3 Mbaud
  - SMBus (1 Mbps)
  - USB 2.0-compliant full speed with integrated low-power transceiver, 4 bidirectional endpoints and dedicated 1024-byte buffer
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- **Single Voltage Supply**
  - (VREGIN shorted to VDD): 2.3 to 3.6 V
  - (VREGIN not shorted to VDD): 2.7 to 5.25 V
- **Pre-loaded USB Bootloader**
- **Package Options: QFN20, QFN24, QSOP24**
- **Temperature Range: -40 to +85 °C**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Devices are available in 20-pin QFN, 24-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

2. Ordering Information

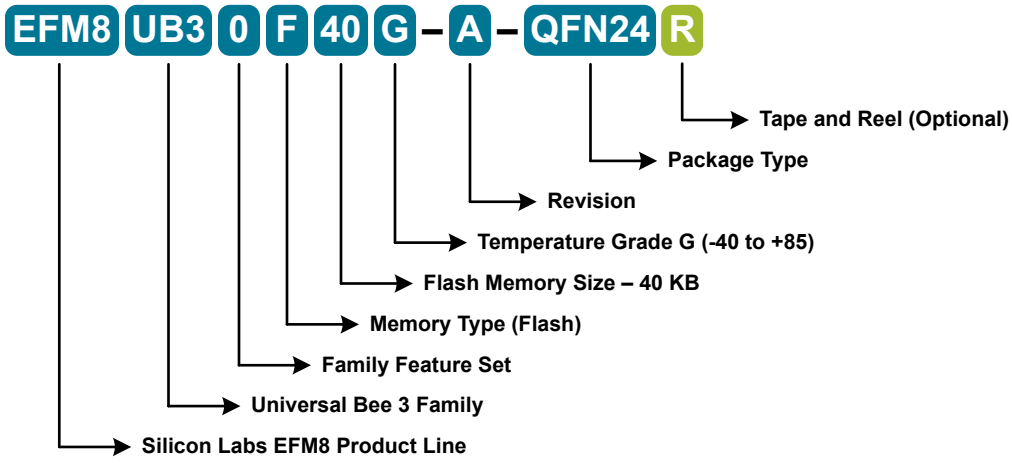


Figure 2.1. EFM8UB3 Part Numbering

All EFM8UB3 family members have the following features:

- CIP-51 Core running up to 48 MHz
- Three Internal Oscillators (48 MHz, 24.5 MHz, and 80 kHz)
- USB Full/Low speed Function Controller
- SMBus
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- Pre-loaded USB bootloader

In addition to these features, each part number in the EFM8UB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8UB31F40G-A-QSOP24	40	3328	17	16	8	8	Yes	-40 to +85 °C	QSOP24
EFM8UB31F40G-A-QFN24	40	3328	17	16	8	8	Yes	-40 to +85 °C	QFN24
EFM8UB30F40G-A-QFN20	40	3328	13	12	8	4	Yes	-40 to +85 °C	QFN20

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3. System Overview

3.1 Introduction

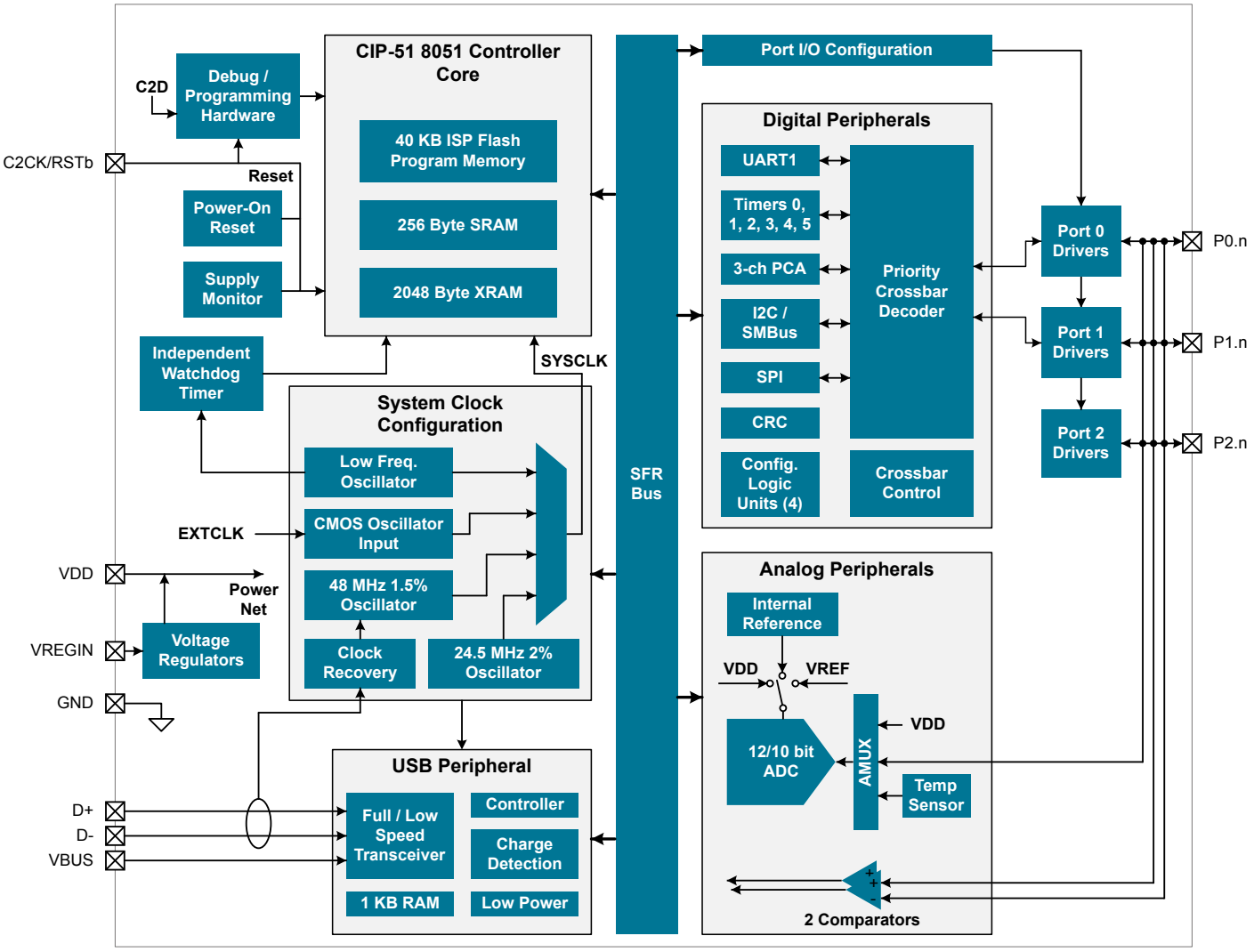


Figure 3.1. Detailed EFM8UB3 Block Diagram

This section describes the EFM8UB3 family at a high level.

For more information on the device packages and pinout, electrical specifications, and typical connection diagrams, see the EFM8UB3 Data Sheet. For more information on each module including register definitions, see the EFM8UB3 Reference Manual. For more information on any errata, see the EFM8UB3 Errata.

3.2 Power

Control over the device power consumption can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulators in normal bias mode for fast wake • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in PCON1	• USB0 Bus Activity • Timer 4 Event • SPI0 Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Stop	• All internal power nets shut down • 5V regulator remains active (if enabled) • Internal 1.8 V LDO on • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulators in low bias current mode for energy savings • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SNOOZE bit in PCON1	• USB0 Bus Activity • Timer 4 Event • SPI0 Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Shutdown	• All internal power nets shut down • 5V regulator remains active (if enabled) • Internal 1.8 V LDO off to save energy • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.6 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

The port control block offers the following features:

- Up to 17 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 17 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 48 MHz internal oscillator (HFOSC1), accurate to ±1.5% over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- USB Start-of-Frame (SOF) capture
- Configurable Logic output capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Serial Bus (USB0)

The USB0 peripheral provides a full-speed USB 2.0 compliant device controller and PHY with additional Low Energy USB features. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The USB function controller (USB0) consists of a Serial Interface Engine (SIE), USB transceiver (including matching resistors and configurable pull-up resistors), and 1 KB FIFO block. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget.

The USB0 module includes the following features:

- Full and Low Speed functionality.
- Implements 4 bidirectional endpoints.
- Low Energy Mode to reduce active supply current based on bus bandwidth.
- USB 2.0 compliant USB peripheral support (no host capability).
- Direct module access to 1 KB of RAM for FIFO memory.
- Clock recovery to meet USB clocking requirements with no external components.
- Charger detection circuitry with automatic detection of SDP, CDP, and DCP interfaces.
- D+ and D- can be routed to ADC input to support ACM and proprietary charger architectures.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to 12 Mbps in master or slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate (master).
- Programmable receive timeout (slave).
- Two byte FIFO on transmit and receive.
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), and Fast Mode Plus (1 Mbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive FIFOs (two-byte) to help increase throughput in faster applications

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

3.7 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O, internal timer sources, and configurable logic (CLU) sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 8 (CMP0) or 8 (CMP1) external positive inputs
- Up to 8 (CMP0) or 8 (CMP1) external negative inputs
- Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- USB reset

3.9 Debugging

The EFM8UB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a USB bootloader. This bootloader resides in the code security page and last pages of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

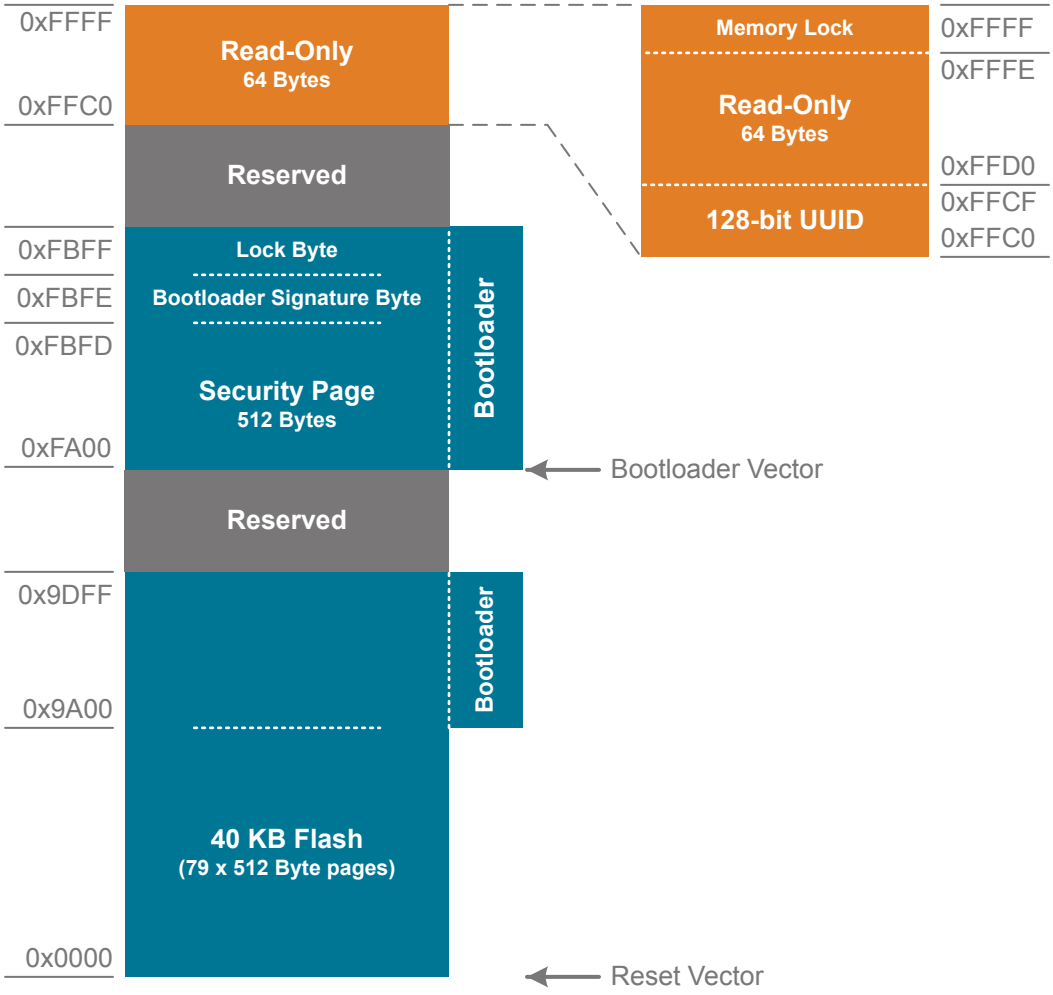


Figure 3.2. Flash Memory Map with Bootloader—40 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
USB	VBUS
	D+
	D-

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN24	P2.0 / C2D
QSOP24	P2.0 / C2D
QFN20	P2.0 / C2D

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in 4.1.1 Recommended Operating Conditions, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		2.3 [1]	—	3.6	V
Operating Supply Voltage on VIO [3, 4]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN [1]	V_{REGIN}		3.0 [1]	—	5.5	V
System Clock Frequency	f_{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation. If using the internal regulator to supply this voltage on VDD, the minimum regulator input voltage is 3.7 V.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 48 MHz (HFOSC1) [2]	—	9.6	10.5	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0) [2]	—	4.6	5.3	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0) [2]	—	616	—	µA
		F_{SYSCLK} = 80 kHz [3]	—	131	—	µA
Idle Mode-Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 48 MHz (HFOSC1) [2]	—	7.1	7.8	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0) [2]	—	3.4	3.9	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0) [2]	—	550	—	µA
		F_{SYSCLK} = 80 kHz [3]	—	139	—	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I_{DD}	LFO Running	—	125	—	µA
		LFO Stopped	—	120	—	µA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I_{DD}	LFO Running	—	25	—	µA
		LFO Stopped	—	20	—	µA
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I_{DD}		—	120	—	µA
Shutdown Mode—Core halted and all clocks stopped,Internal LDO Off, Supply monitor off.	I_{DD}		—	0.35	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	122	—	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 48 MHz, T_A = 25 °C	—	910	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	4.2	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on [4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	850	1085	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	420	545	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	385	—	µA
		100 ksps, V_{DD} = 3.0 V	—	193	—	µA
		10 ksps, V_{DD} = 3.0 V	—	20	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	495	—	µA
		100 ksps, V_{DD} = 3.0 V	—	250	—	µA
		10 ksps, V_{DD} = 3.0 V	—	25.5	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	520	—	µA
		50 ksps, V_{DD} = 3.0 V	—	260	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	970	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	425	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	86	—	µA
Internal ADC0 Reference, Always-on [5]	I_{VREFFS}	Normal Power Mode	—	690	765	µA
		Low Power Mode	—	166	195	µA
Temperature Sensor	I_{TSENSE}		—	68	110	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	9.1	—	µA
		CPMD = 00	—	24.2	—	µA
Comparator Reference[6]	I_{CPREF}		—	25.3	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	14	20	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5V Regulator	I_{VREG}	Normal Mode (SUSEN = 0, BIASENB = 0)	—	260	375	µA
		Suspend Mode (SUSEN = 1, BIASENB = 0)	—	67	123	µA
		Bias Disabled (BIASENB = 1)	—	1.8	16	µA
		Disabled (BIASENB = 1, REG1ENB = 1)	—	2.5	—	nA
USB (USB0) Full-Speed	I_{USB}	Low Energy Mode, 64 byte 1ms IN Interrupt transfers	—	850	—	µA
		Low Energy Mode, 64 byte 1ms OUT Interrupt transfers	—	250	—	µA
		Low Energy Mode, Idle (SOF only)	—	50	—	µA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
6. This value is the current sourced from the pin or supply selected as the full-scale reference to the comparator DAC.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		2.16	2.23	2.29	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.2	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.3 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1, 2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1, 2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming [3]	V_{PROG}	5 V Voltage Regulator used	2.7	—	5.5	V
		5 V Voltage Regulator bypassed	2.3	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	µs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUSPENDWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	12	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (48 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	45	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	48	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.		1.1		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range [1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	-3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	61	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	61	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	76	—	dB
		10 Bit Mode	—	73	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	-80	—	dB
		10 Bit Mode	—	-76	—	dB

Note:
1. Absolute input pin voltage is limited by the V_{DD} supply.

4.1.9 Voltage Reference

Table 4.9. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, V_{DD} > 2.6 V	2.34	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; VREF = 3.0 V	—	8	—	µA

4.1.10 Temperature Sensor

Table 4.10. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	757	—	mV
Offset Error [1]	E_{OFF}	T_A = 0 °C	—	17	—	mV
Slope	M		—	2.85	—	mV/°C
Slope Error [1]	E_M		—	70	—	µV/°
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs

Note:
1. Represents one standard deviation from the mean.

4.1.11 5 V Voltage Regulator

Table 4.11. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range [1]	V_{REGIN}	USB in use	3.7	—	5.5	V
		USB not in use	3.0	—	5.5	V
Output Voltage on VDD [2]	V_{REGOUT}	Regulation range (VREGIN ≥ 4.1V)	3.1	3.4	3.6	V
		Dropout range (VREGIN < 4.1V)	—	V_{REGIN} – $V_{DROPOUT}$	—	V
Output Current [2]	I_{REGOUT}		—	—	100	mA
Dropout Voltage	$V_{DROPOUT}$	Output Current = 100 mA	—	—	0.7	V

Note:
1. Input range to meet the Output Voltage on VDD specification. If the 5 V voltage regulator is not used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

4.1.12 1.8 V Internal LDO Voltage Regulator

Table 4.12. 1.8V Internal LDO Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT\_1.8V}$		1.77	1.84	1.92	V

4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential, V_{CM} = 1.65 V	—	250	—	ns
		-100 mV Differential, V_{CM} = 1.65 V	—	213	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential, V_{CM} = 1.65 V	—	1.06	—	µs
		-100 mV Differential, V_{CM} = 1.65 V	—	3.4	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.3	—	mV
		CPHYP = 01	—	8.55	—	mV
		CPHYP = 10	—	17.1	—	mV
		CPHYP = 11	—	33.6	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.3	—	mV
		CPHYN = 01	—	-8.55	—	mV
		CPHYN = 10	—	-17.1	—	mV
		CPHYN = 11	—	-34.2	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.2	—	mV
		CPHYP = 01	—	4.9	—	mV
		CPHYP = 10	—	10.4	—	mV
		CPHYP = 11	—	20.8	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.2	—	mV
		CPHYN = 01	—	-4.9	—	mV
		CPHYN = 10	—	-10	—	mV
		CPHYN = 11	—	-20.8	—	mV
Input Range (CP+ or CP-)	V_{IN}	Direct comparator input	-0.25	—	V_{DD}+0.25	V
		Reference DAC input	1.2		V_{DD}	V
Reference DAC Resolution	N_{bits}			6		bits
Reference DAC Input Impedance	R_{CPREF}		—	2.75	—	MΩ
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	68.5	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	65	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-11	-1.8	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay through LUT	t_{DLY_LUT}	Through single CLU Using an external pin	—	—	38.7	ns
		Through single CLU Using an internal connection	—	1.6	5.0	ns
Propagation Delay through D flip-flop clock	t_{DLY_DFF}	Through single CLU Using an external pin	—	—	38.7	ns
		Through single CLU Using an internal connection	—	1.4	5.6	ns
Clocking Frequency	F_{CLK}	1 or 2 CLUs Cascaded	—	—	48	MHz
		3 or 4 CLUs Cascaded	—	—	48	MHz

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.3 V ≤ V_{IO} < 3.0 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.3 V ≤ V_{IO} < 3.0 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.3 V ≤ V_{IO} < 3.0 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.3 V ≤ V_{IO} < 3.0 V	—	—	V_{IO} x 0.2	V
Input High Voltage (all port pins including VBUS)	V_{IH}		0.7 x V_{IO}	—	—	V
Input Low Voltage (all port pins including VBUS)	V_{IL}		—	—	0.3 x V_{IO}	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{IO} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.0 V	0	5	60	µA

Note:
1. On devices without a VIO pin, V_{IO} = V_{DD}.

4.1.16 USB Transceiver

Table 4.16. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmitter						
Output High Voltage	V_{OH}	V_{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V_{OL}	V_{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	28	36	44	Ω
		Driving Low	28	36	44	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
		Low Speed (D- Pull-up)				
Output Rise Time	T_R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T_F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

4.1.17 SMBus

Table 4.17. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		275[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[4]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	255[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		275[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[4]	µs
Fast Mode Plus (1 MHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	666[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	666[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.67	—	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		0.33	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		0.67	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		0.67	—	—	µs
Data Hold Time	$t_{HD:DAT}$		275[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		0.33	—	—	µs
Clock High Period	t_{HIGH}		0.67	—	50[4]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 40 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.18. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

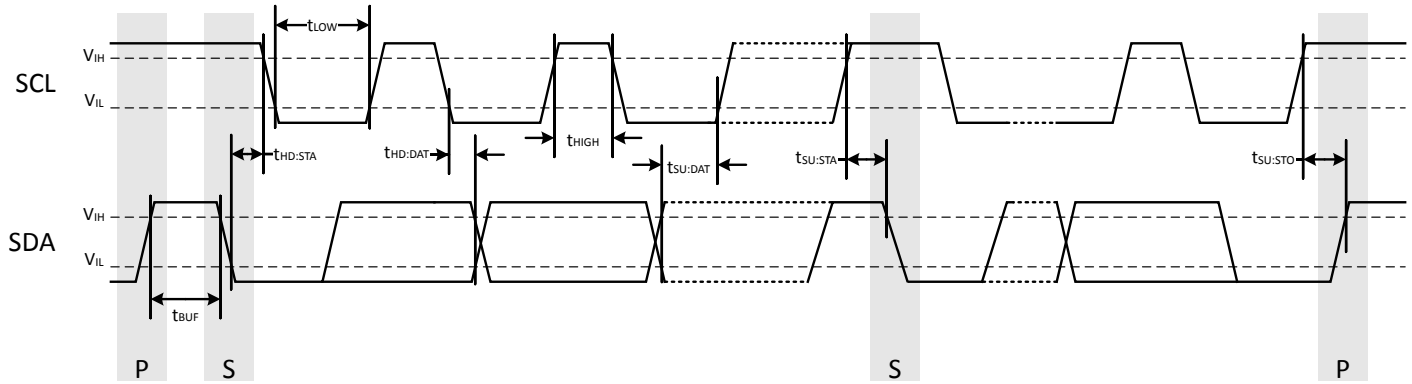


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.19. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN20 Packages	—	60	—	°C/W
		QFN24 Packages	—	30	—	°C/W
		QSOP24 Packages	—	65	—	°C/W
		QFN32 Packages	—	26	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.3 Absolute Maximum Ratings

Stresses above those listed in 4.3 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.20. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO[2]	V_{IO}		GND-0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND-0.3	5.8	V
Voltage on D+ or D-[2]	V_{USBD}		GND-0.3	V_{DD}+0.3	V
Voltage on I/O pins (including VBUS / P2.1) or RSTb[2]	V_{IN}	V_{IO} > 3.3 V	GND-0.3	5.8	V
		V_{IO} < 3.3 V	GND-0.3	V_{IO}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J		-40	105	°C

Note:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. On devices without a VIO pin, $V_{IO} = V_{DD}$.

5. Typical Connection Diagrams

5.1 Power

The figure below shows a typical connection diagram for the power pins of the EFM8UB3 devices when the internal regulator used and USB is connected (bus-powered).

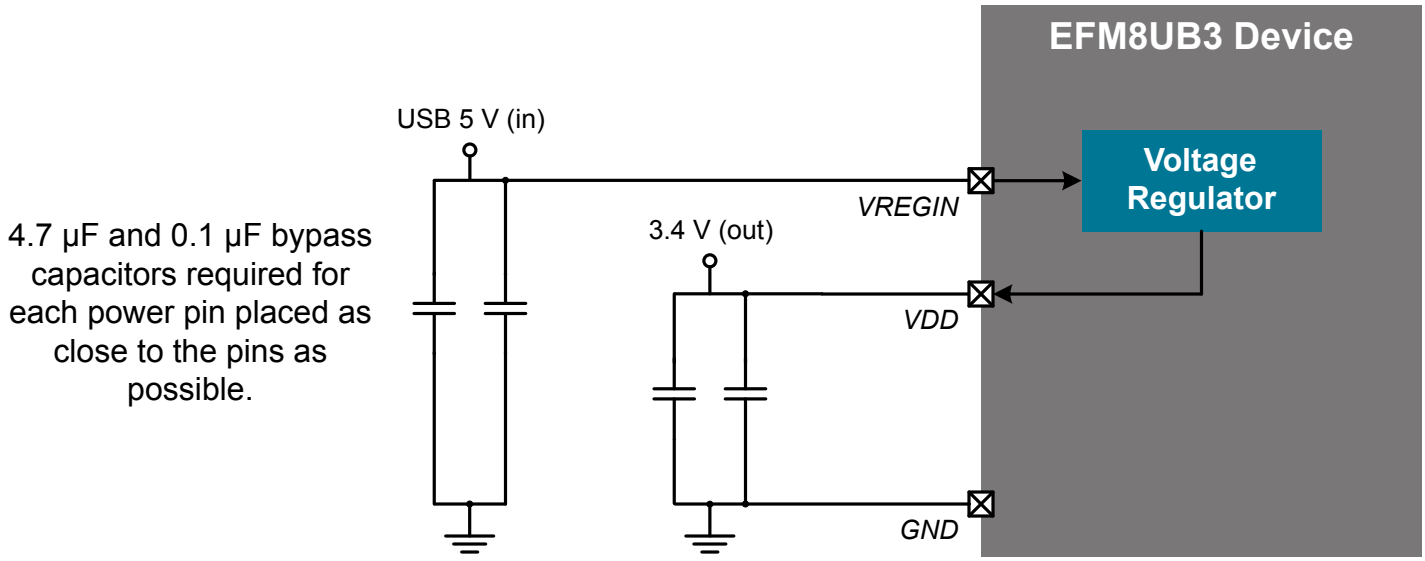


Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB3 devices when the internal regulator used and USB is connected (self-powered).

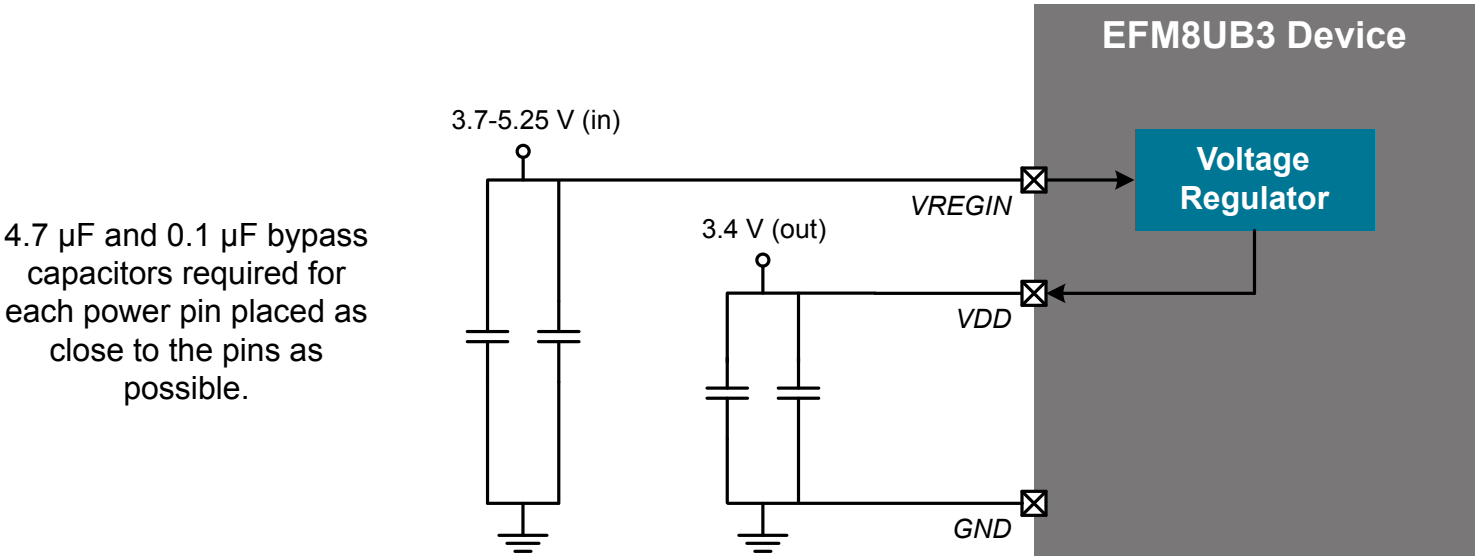


Figure 5.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB3 devices when the internal 5 V-to-3.3 V regulator is not used.

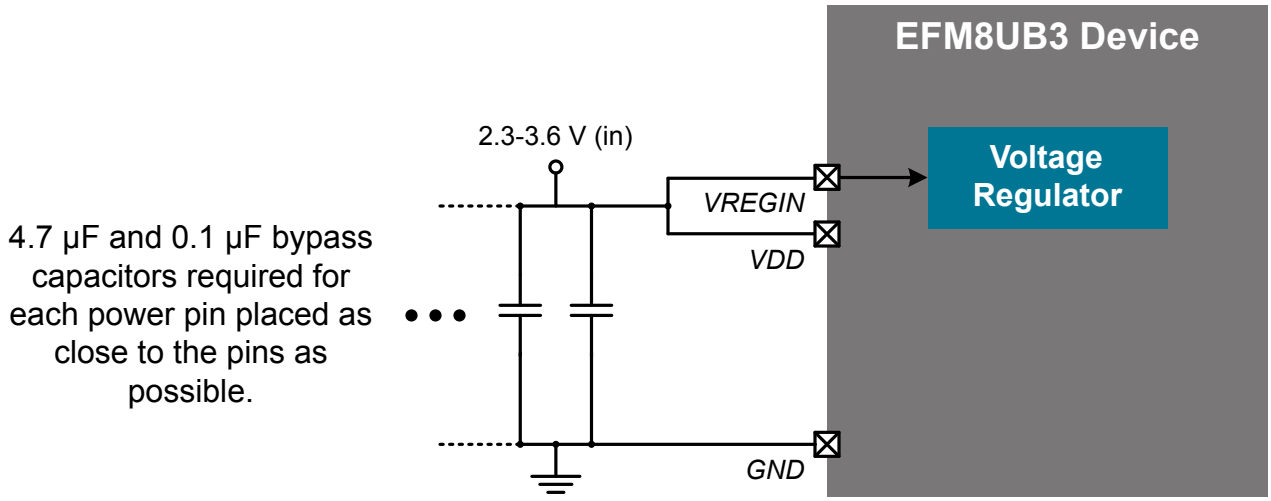


Figure 5.3. Connection Diagram with Voltage Regulator Not Used (Self-Powered)

5.2 USB

Figure 5.4 Bus-Powered Connection Diagram for USB Pins on page 35 shows a typical connection bus-powered diagram for the USB pins of the EFM8UB3 devices including ESD protection diodes on the USB pins. Bypass capacitors on VREGIN and VDD are required as discussed in 5.1 Power, but are not shown in the figure.

Note: The VBUS pin is not required as a sensing pin for proper operation in bus-powered configurations. Rather than using VBUS as a sensing pin, it is recommended to use the VBUS pin only as a GPIO by clearing VBUSEN and VBUSIE to 0 in the USB0CF register. To do this using the USB stack, set the device to use bus-powered mode.

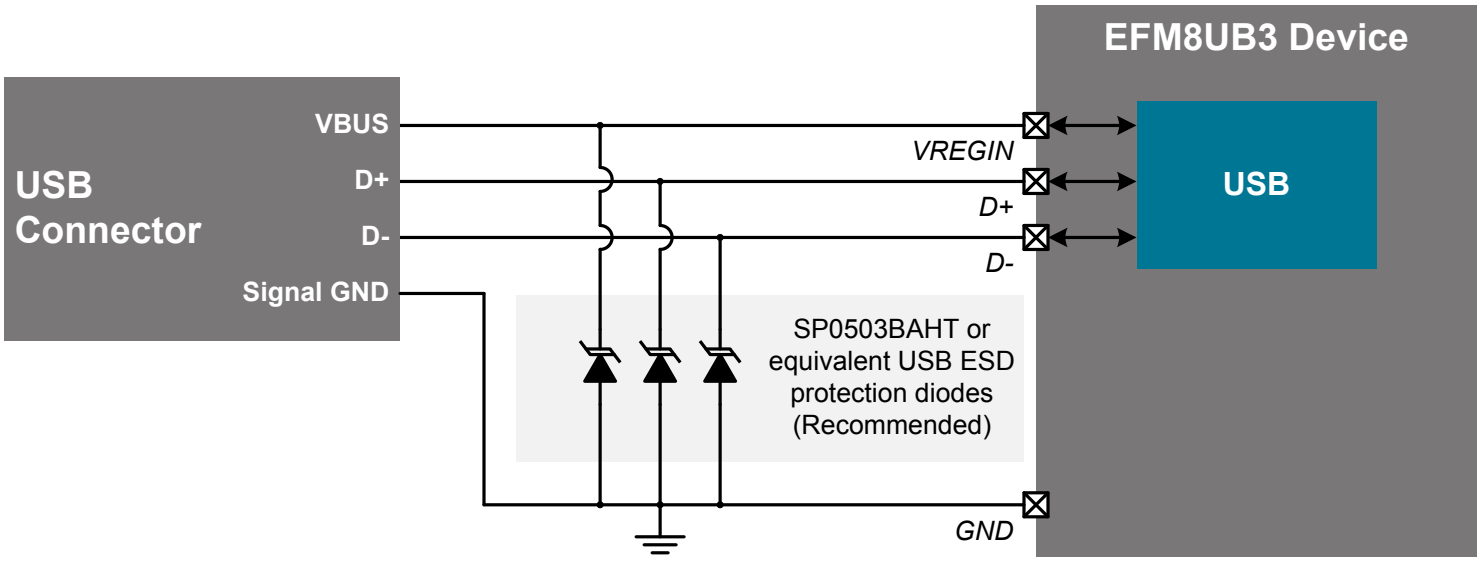


Figure 5.4. Bus-Powered Connection Diagram for USB Pins

Figure 5.5 Self-Powered Connection Diagram for USB Pins on page 36 shows a typical connection self-powered diagram for the USB pins of the EFM8UB3 devices including ESD protection diodes on the USB pins.

Note: There are two relevant restrictions on the VBUS pin voltage in this self-powered configuration. The first is the absolute maximum voltage on the VBUS pin, which is defined as V_{IO} + 2.5 V in Table 4.20 Absolute Maximum Ratings on page 32. The second is the Input High Voltage (VIH) for VBUS to detect when the device is connected to a bus, which is defined as 0.7 x V_{IO} in 4.1.15 Port I/O. For self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 4.4 V to 5.5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet these specifications and ensure reliable device operation. In this case, the current limitation of the resistor divider prevents overstress on the pin, even though the V_{IO} + 2.5 V specification is not strictly met.

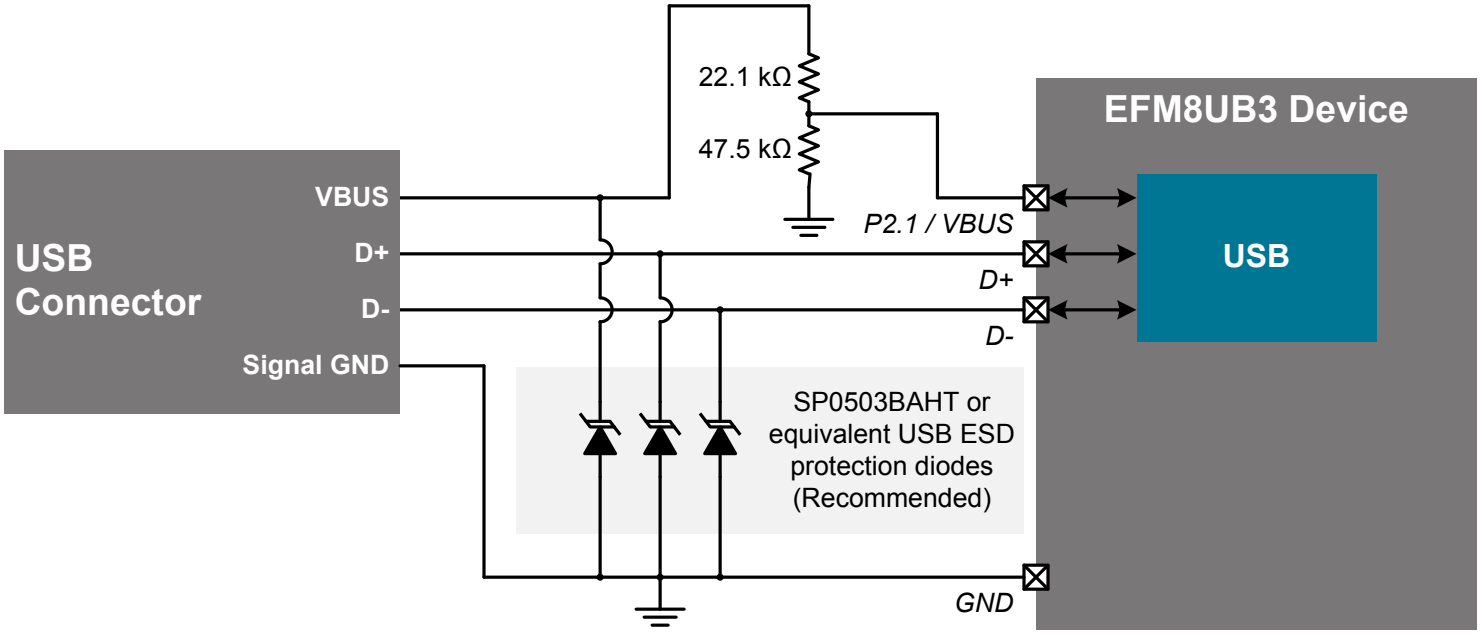


Figure 5.5. Self-Powered Connection Diagram for USB Pins

5.3 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in *AN124: Pin Sharing Techniques for the C2 Interface*. Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

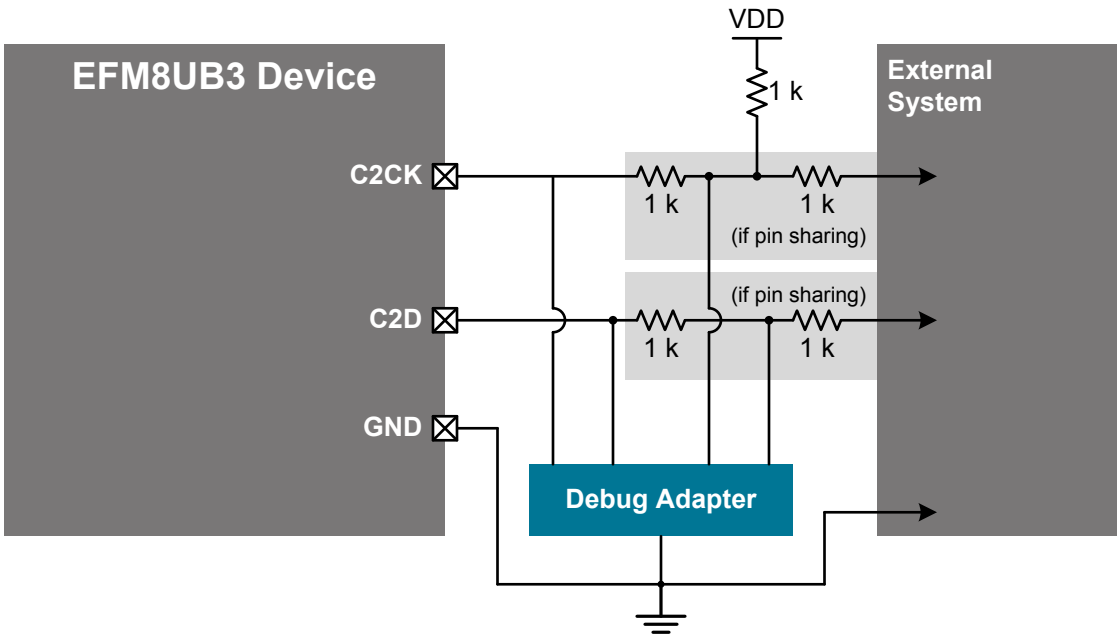


Figure 5.6. Debug Connection Diagram

5.4 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note *AN203: 8-bit MCU Printed Circuit Board Design Notes* contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

6. Pin Definitions

6.1 EFM8UB3x-QSOP24 Pin Definitions

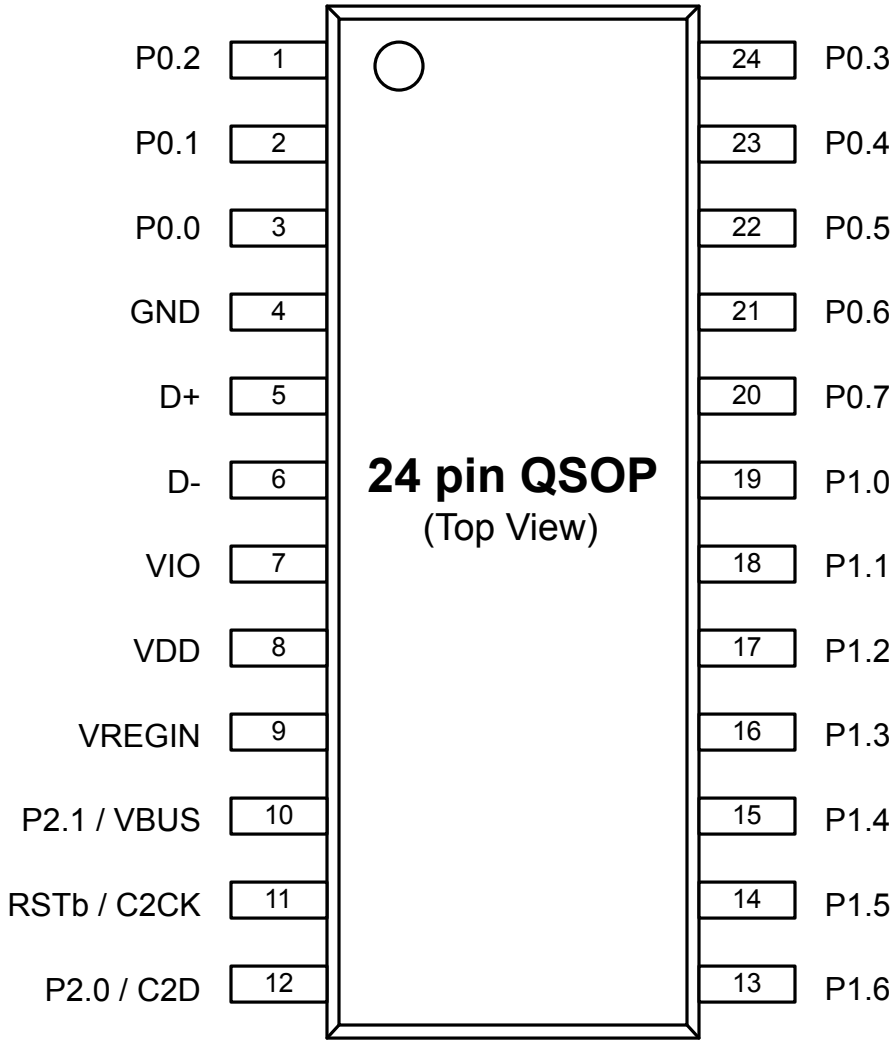


Figure 6.1. EFM8UB3x-QSOP24 Pinout

Table 6.1. Pin Definitions for EFM8UB3x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU2B.7 CLU3B.6 CLU0OUT	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0A.6 CLU3A.7	ADC0.1 CMP0P.1 CMP0N.1 AGND
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
4	GND	Ground			ADC0.19
5	D+	USB Data Positive			ADC0.28
6	D-	USB Data Negative			ADC0.29
7	VIO	I/O Power Input			
8	VDD	Supply Power Input / 5V Regulator Output			ADC0.18
9	VREGIN	5V Regulator Input			
10	P2.1	Multifunction I/O		VBUS	ADC0.24 CMP1P.13 CMP1N.13
11	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
12	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
13	P1.6	Multifunction I/O	Yes	CLU0A.7	ADC0.14 CMP1P.6 CMP1N.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes		ADC0.13 CMP1P.5 CMP1N.5
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
17	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
18	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
19	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0B.6 CLU2A.7 CLU3OUT	ADC0.8 CMP1P.0 CMP1N.0
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1A.7 CLU3A.6	ADC0.7 CMP0P.7 CMP0N.7
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU1B.6 CLU2OUT	ADC0.6 CMP0P.6 CMP0N.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART1_RX CLU1B.7 CLU2A.6	ADC0.5 CMP0P.5 CMP0N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 CLU0B.7 CLU2B.6 CLU1OUT UART1_TX	ADC0.4 CMP0P.4 CMP0N.4
24	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU1A.6 CLU3B.7	ADC0.3 CMP0P.3 CMP0N.3

6.2 EFM8UB3x-QFN24 Pin Definitions

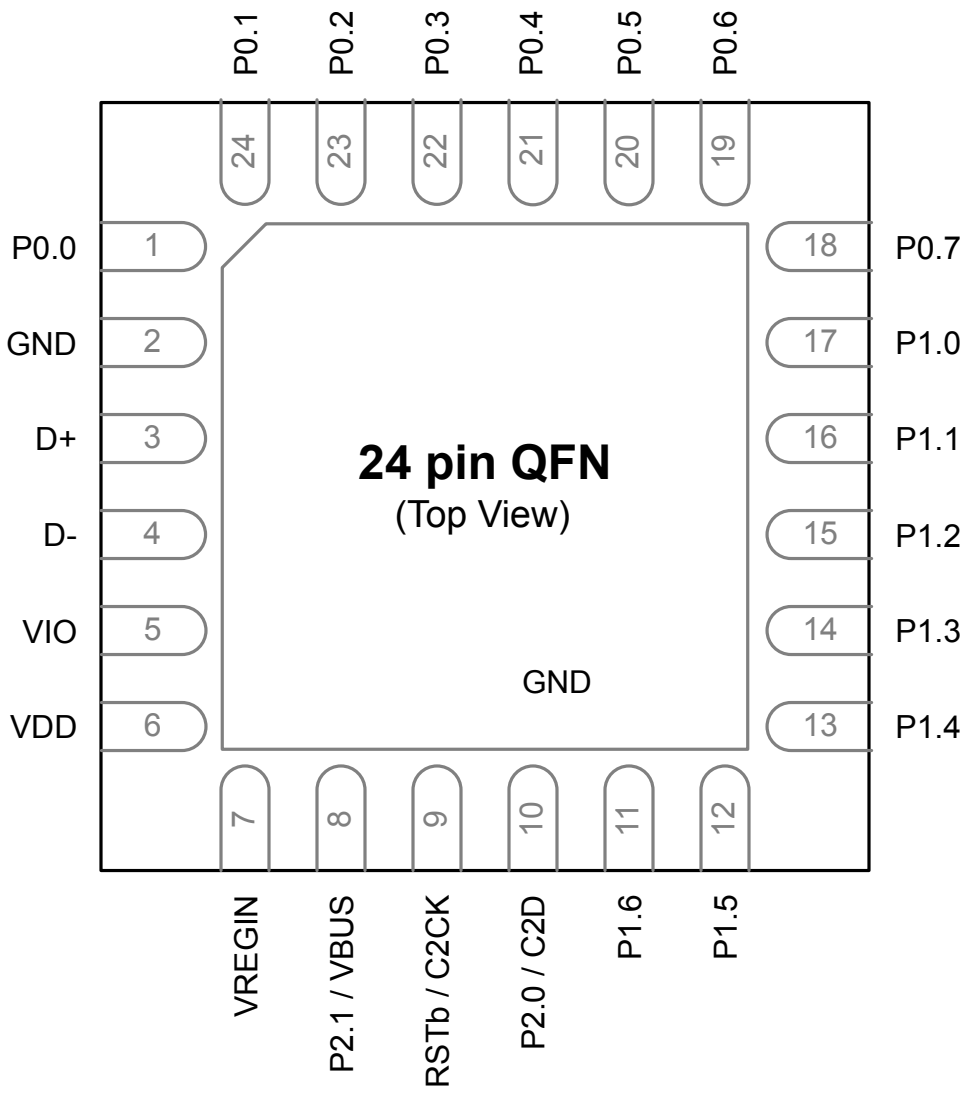


Figure 6.2. EFM8UB3x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8UB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
2	GND	Ground			ADC0.19

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	D+	USB Data Positive			ADC0.28
4	D-	USB Data Negative			ADC0.29
5	VIO	I/O Power Input			
6	VDD	Supply Power Input / 5V Regulator Output			ADC0.18
7	VREGIN	5V Regulator Input			
8	P2.1	Multifunction I/O		VBUS	ADC0.24 CMP1P.13 CMP1N.13
9	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
11	P1.6	Multifunction I/O	Yes	CLU0A.7	ADC0.14 CMP1P.6 CMP1N.6
12	P1.5	Multifunction I/O	Yes		ADC0.13 CMP1P.5 CMP1N.5
13	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
14	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
15	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
16	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
17	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0B.6 CLU2A.7 CLU3OUT	ADC0.8 CMP1P.0 CMP1N.0

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1A.7 CLU3A.6	ADC0.7 CMP0P.7 CMP0N.7
19	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU1B.6 CLU2OUT	ADC0.6 CMP0P.6 CMP0N.6
20	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART1_RX CLU1B.7 CLU2A.6	ADC0.5 CMP0P.5 CMP0N.5
21	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 CLU0B.7 CLU2B.6 CLU1OUT UART1_TX	ADC0.4 CMP0P.4 CMP0N.4
22	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU1A.6 CLU3B.7	ADC0.3 CMP0P.3 CMP0N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU2B.7 CLU3B.6 CLU0OUT	ADC0.2 CMP0P.2 CMP0N.2
24	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0A.6 CLU3A.7	ADC0.1 CMP0P.1 CMP0N.1 AGND
Center	GND	Ground			

6.3 EFM8UB3x-QFN20

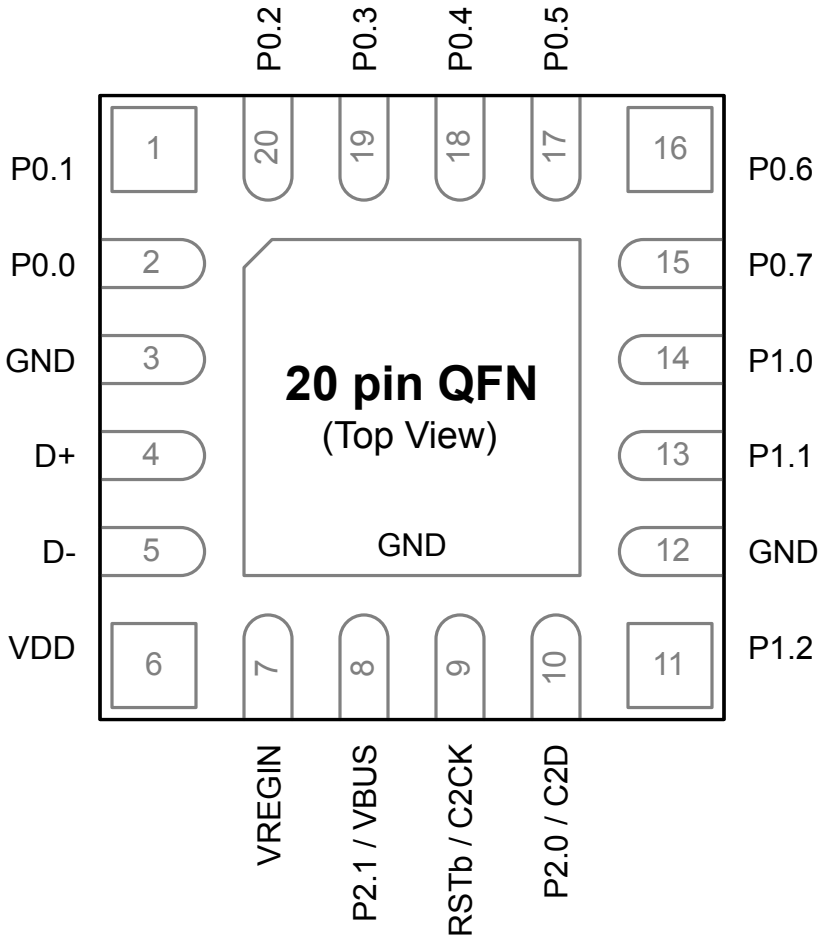


Figure 6.3. EFM8UB3x-QFN20 Pinout

Table 6.3. Pin Definitions for EFM8UB3x-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0A.6 CLU3A.7	ADC0.1 CMP0P.1 CMP0N.1 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
3	GND	Ground			ADC0.19
4	D+	USB Data Positive			ADC0.28
5	D-	USB Data Negative			ADC0.29
6	VDD	Supply Power Input / 5V Regulator Output			ADC0.18
7	VREGIN	5V Regulator Input			
8	P2.1	Multifunction I/O		VBUS	ADC0.24 CMP1P.13 CMP1N.13
9	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
11	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
14	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0B.6 CLU2A.7 CLU3OUT	ADC0.8 CMP1P.0 CMP1N.0
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1A.7 CLU3A.6	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU1B.6 CLU2OUT	ADC0.6 CMP0P.6 CMP0N.6
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART1_RX CLU1B.7 CLU2A.6	ADC0.5 CMP0P.5 CMP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 CLU0B.7 CLU2B.6 CLU1OUT UART1_TX	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU1A.6 CLU3B.7	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU2B.7 CLU3B.6 CLU0OUT	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

7. QFN24 Package Specifications

7.1 QFN24 Package Dimensions

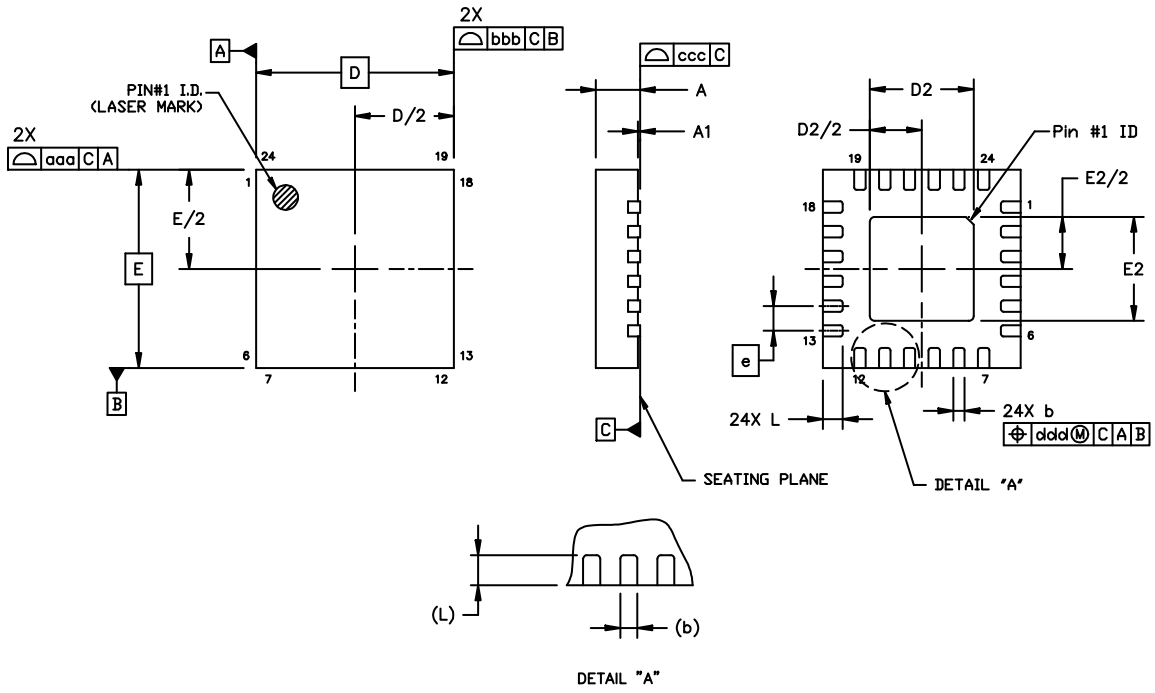


Figure 7.1. QFN24 Package Drawing

Table 7.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Dimension	Min	Typ	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 PCB Land Pattern

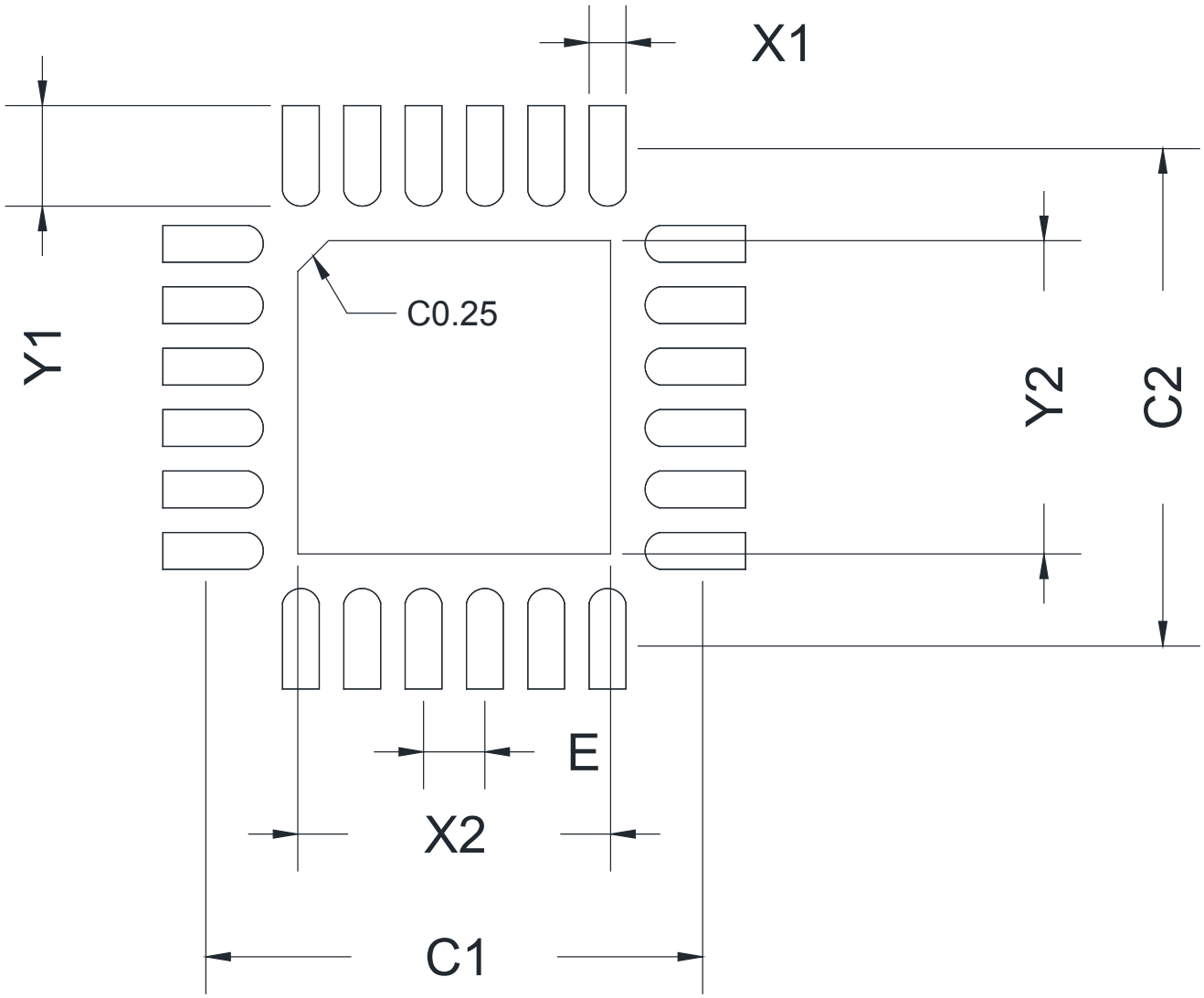


Figure 7.2. PCB Land Pattern Drawing

Table 7.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	
C2	3.90	
E	0.50	
X1	0.30	
X2	2.55	
Y1	0.85	
Y2	2.55	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 0.9 mm square openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 Package Marking

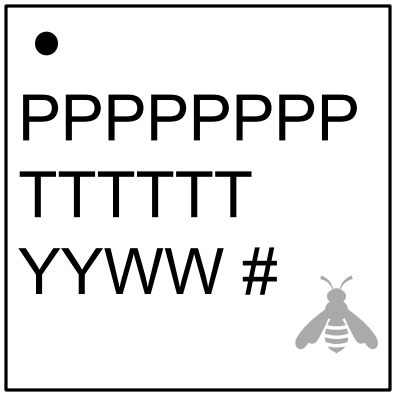


Figure 7.3. Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QSOP24 Package Specifications

8.1 Package Dimensions

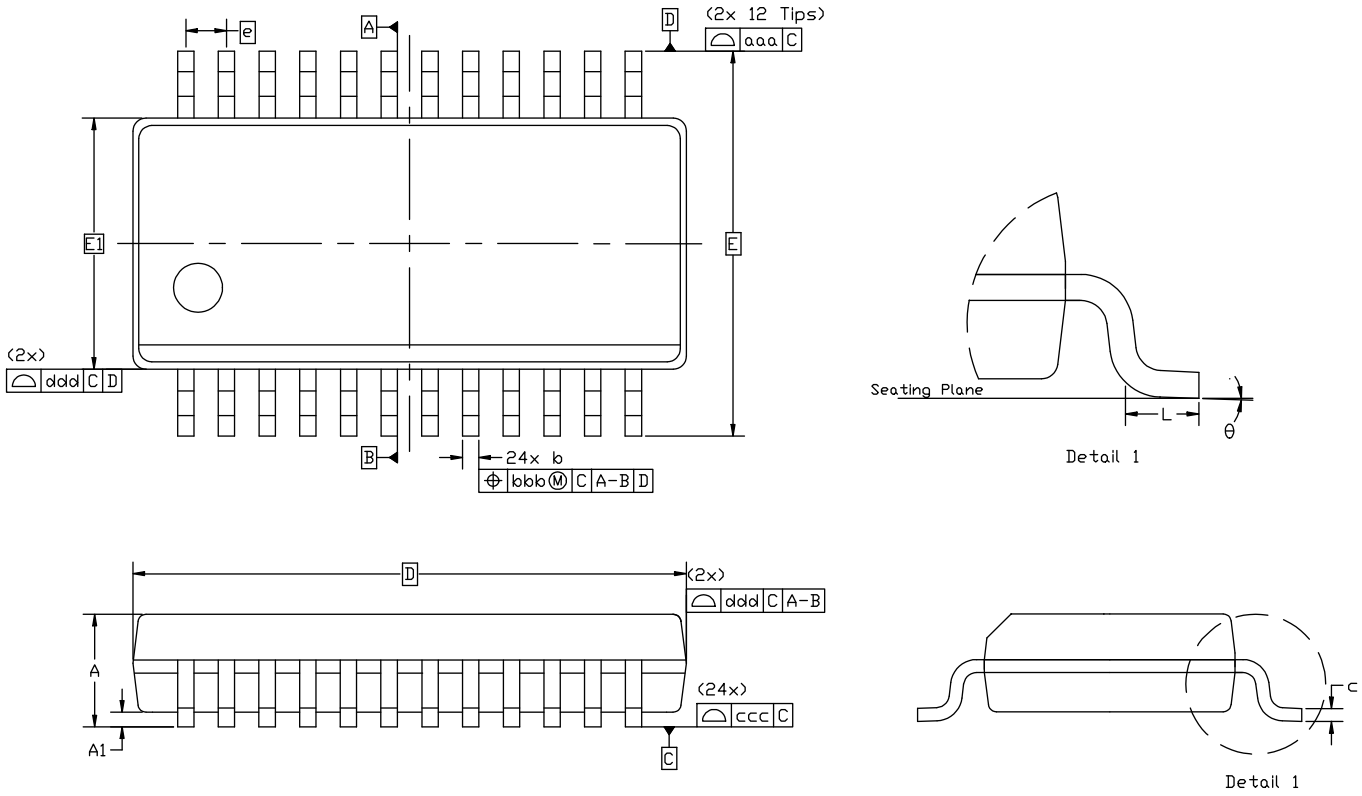


Figure 8.1. Package Drawing

Table 8.1. Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27

Dimension	Min	Typ	Max
theta	0º	—	8º
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 PCB Land Pattern

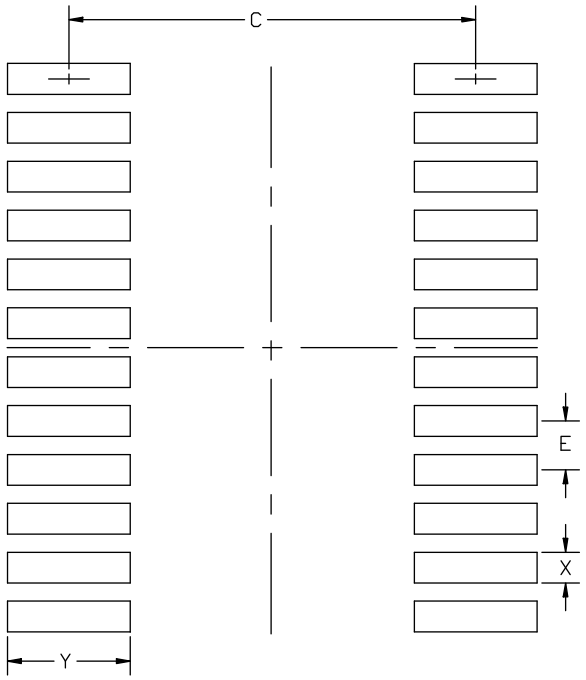


Figure 8.2. PCB Land Pattern Drawing

Table 8.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 Package Marking

Figure 8.3. Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions

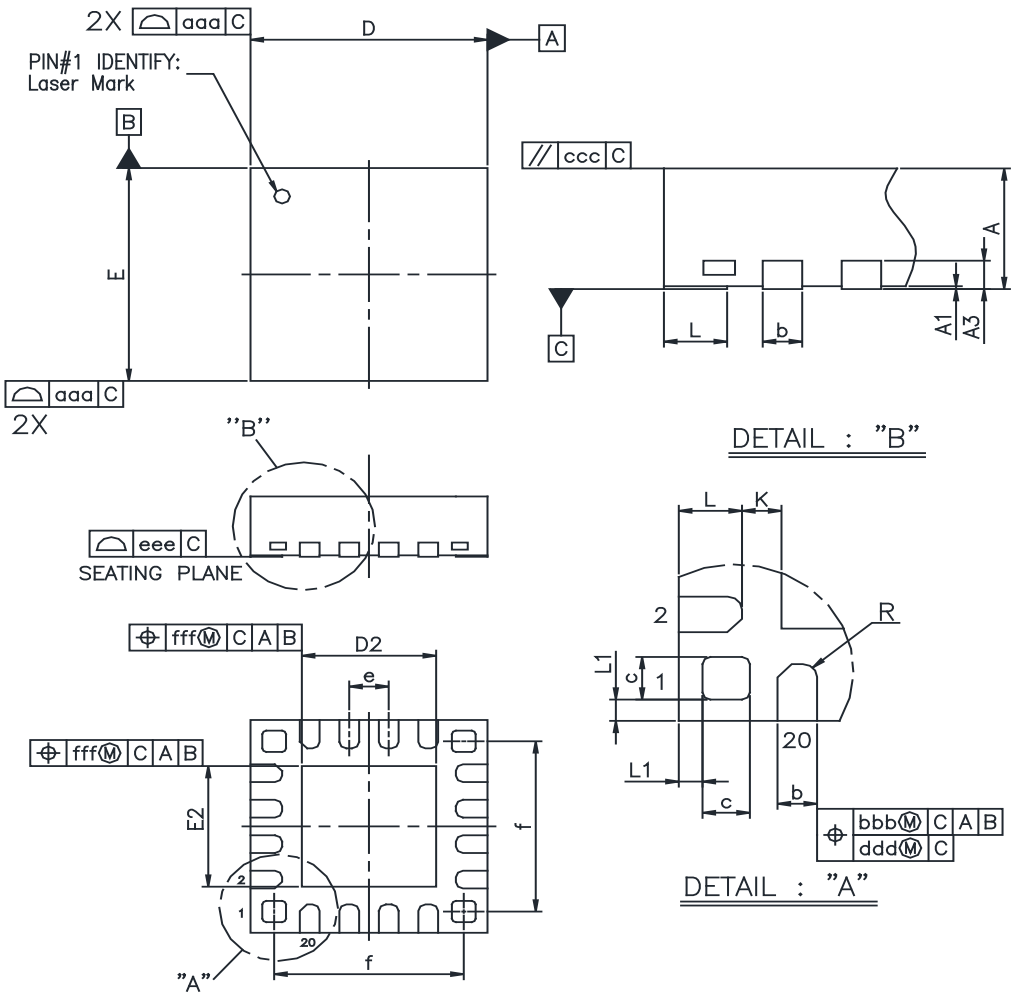


Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	1.70	1.80
e		0.50 BSC	
E		3.00 BSC	

Dimension	Min	Typ	Max
E2	1.60	1.70	1.80
f		2.50 BSC	
L	0.30	0.40	0.50
K		0.25 REF	
R	0.09	0.125	0.15
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 QFN20 PCB Land Pattern

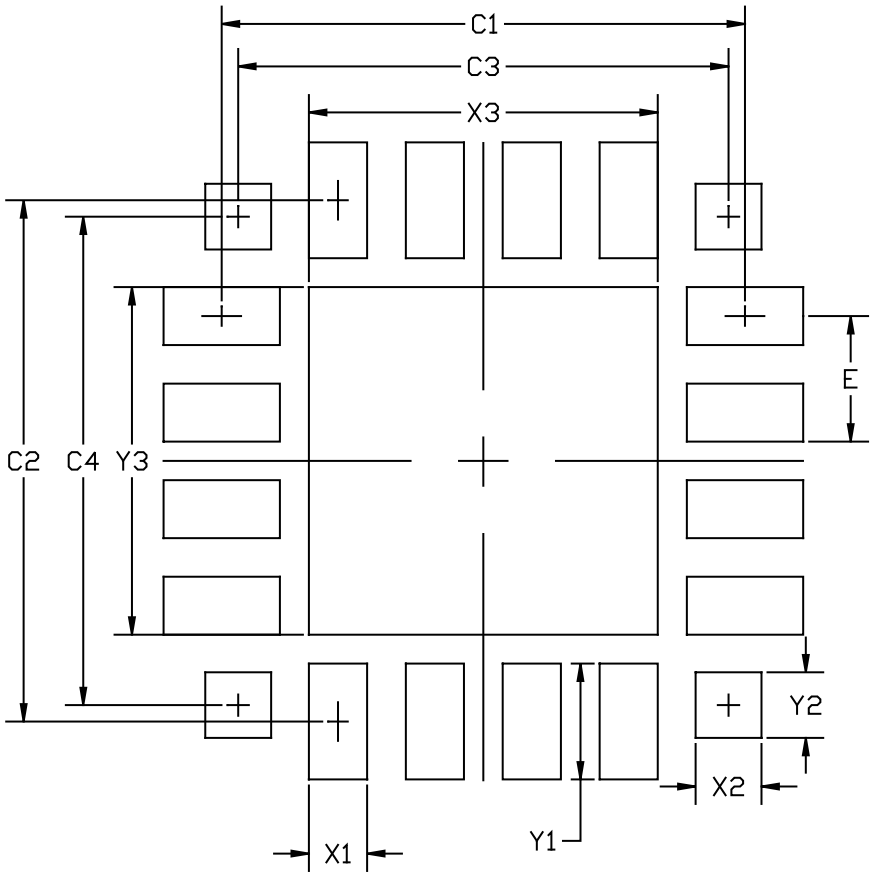


Figure 9.2. QFN20 PCB Land Pattern Drawing

Table 9.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.10	
C2	3.10	
C3	2.50	
C4	2.50	
E	0.50	
X1	0.30	
X2	0.25	0.35
X3	1.80	
Y1	0.90	
Y2	0.25	0.35
Y3	1.80	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
8. A 2 x 2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN20 Package Marking

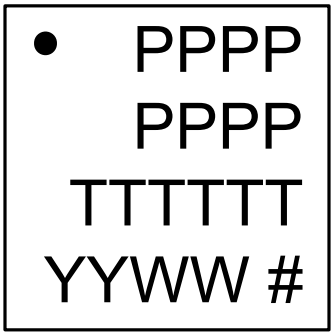


Figure 9.3. QFN20 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

Revision 1.1

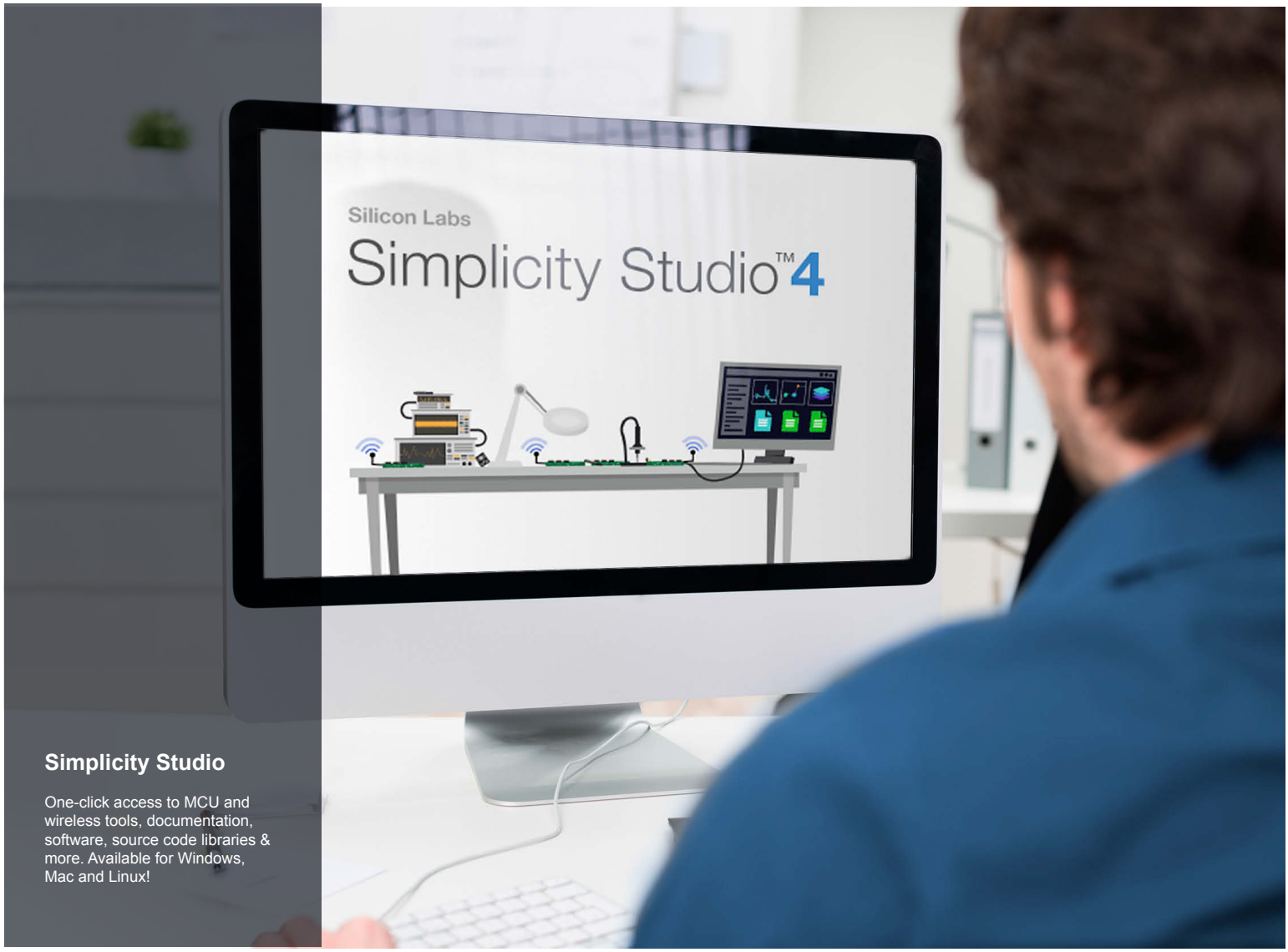
October 20th, 2017

- Updated the front page diagram to indicate USB and SPI are available in Snooze mode.
- Updated the front page and 1. Feature List to refer to two analog comparators.
- Corrected the number of I/O mentioned on the front page.
- Added "Pre-programmed USB Bootloader" to 1. Feature List.
- Updated I/O tolerance range to V_{IO} + 2.5 V in 1. Feature List.
- Updated 3.1 Introduction to mention all device documentation.
- Updated 3.2 Power to remove mention of the I2C Slave peripheral.
- Added bootloader pinout information to 3.10 Bootloader.
- Corrected the application note number for *AN124: Pin Sharing Techniques for the C2 Interface* in 5.3 Debug.
- Added a note to Table 4.2 Power Consumption on page 17 providing more information about the Comparator Reference specification.
- Added maximum specifications to 4.1.14 Configurable Logic Propagation Delay through LUT (internal connection) and Propagation Delay through D flip-flop clock (internal connection).
- Updated 4.1.15 Port I/O to refer to V_{IO} instead of V_{DD} for I/O specifications. Also added a note that V_{IO} = V_{DD} on devices without a VIO pin.
- Added specifications for 4.1.17 SMBus.
- Updated 4.3 Absolute Maximum Ratings to correct the GPIO pin associated with VBUS and update the maximum specfications to be relative to VIO, not VDD.
- Added a VIO specification to 4.3 Absolute Maximum Ratings.
- Updated text and figures in 5.1 Power to remove mention of the VBUS pin.
- Updated the title of Figure 5.3 Connection Diagram with Voltage Regulator Not Used (Self-Powered) on page 34 to include "Self-Powered".
- Updated to show a resistor divider on VBUS in Figure 5.5 Self-Powered Connection Diagram for USB Pins on page 36. Also added two notes regarding VBUS.
- Updated the revision history format.

Revision 1.0

July 20th, 2017

- Initial release.



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