Si3471 Data Sheet

Autonomous Single Ethernet Port IEEE 802.3af, 802.3at, and 802.3bt PoE PSE Device

The Si3471 is a fully autonomous Power over Ethernet (PoE) Power Sourcing Equipment (PSE) device. It is fully IEEE 802.3af, 802.3at, and 802.3bt compliant. It is optimized for use in PSE mid-spans and injectors that do not require a host or MCU. The Si3471 integrates one Ethernet port with the IEEE-required powered device (PD) detection and classification functionality. In addition, it features powered device (PD) disconnect using dc sense algorithms and a robust multipoint detection algorithm. Intelligent protection circuitry includes input undervoltage detection, output current limit, and short-circuit protection. The Si3471 works autonomously and does not require a host or MCU to program it. The Si3471 is programmed for maximum available power by pulling its configration pins high or low.

Applications

- IEEE 802.3af, 802.3at, and 802.3bt Power Sourcing Equipment (PSE)
- Power over Ethernet Injectors
- Single Port Mid-Spans
- Power over Ethernet Switches
- IP Phone Systems
- Smartgrid Switches
- Ruggedized and Industrial Switches

KEY FEATURES

- Single Ethernet port PoE Power Sourcing Equipment (PSE) device
- IEEE 802.3af, 802.3at, and 802.3bt compliant
- Multi-point detection
- Comprehensive fault protection circuitry includes:
  - Power undervoltage lockout
  - Output current limit and short-circuit protection
  - Thermal overload detection
- Extended operating temp range:

  –40 to +85 °C
- 38-pin QFN package (RoHS-compliant)

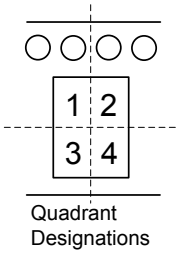
1. Ordering Guide

Table 1.1. Si3471 Ordering Guide

Ordering Part Number[1]	Product Revision	Package	Temperature Range (Ambient)
Si3471A-A01-IM	A01	38-pin QFN RoHS-compliant[2]	–40 to 85 °C

Note:

1. Add an “R” to the end of the part number for tape and reel option (e.g., Si3471A-A01-IM or Si3471A-A01-IMR).
2. Pin 1 is oriented in Quadrant 1 in the tape:



Quadrant Designations

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2. Summary of Operation

The Si3471 operates autonomously, without any external host or MCU control. All power on reset and brownout reset circuitry is internal. If the internal dc/dc converter is used, the VPWR rail activates the dc/dc and it automatically soft starts to generate the 3.3 V VDD and VDDA rails. Upon VDD and VDDA being applied, an internal pull up sets the RESETb pin high, releasing the Si3471 from reset. The Si3471 then reads the PWRAVL pins and configures itself to grant the maximum class set by the PWRAVL pins. The multi-point detection algorithm runs until a valid PoE PD signature is detected and then proceeds with classification. If the Si3471 is configured to grant the class the PD requests, it internally sets the current limit to the class requested by the PD and proceeds to grant power. Otherwise, the Si3471 follows the IEEE 802.3bt specification for power demotion. The Si3471 automatically detects when a PD disconnects and restarts the detection process, continuously looking for a valid detection signature. If any error or fault condition occurs, the Si3471 removes power from the PD and automatically restarts the detection process.

The Si3471 includes an LED pin for driving a status indicator LED. If a status LED is not used, then the pin can be left floating. The LED operation is shown in the table below and is not configurable.

Table 2.1. LED Operation

LED Indication	Status
LED on, no blinking	Port successfully powered at requested power level
LED blinking slowly	Looking for a valid detection signature
LED blinking quickly	Error condition, such as port overload or loss of VPWR

3. Typical Application Example

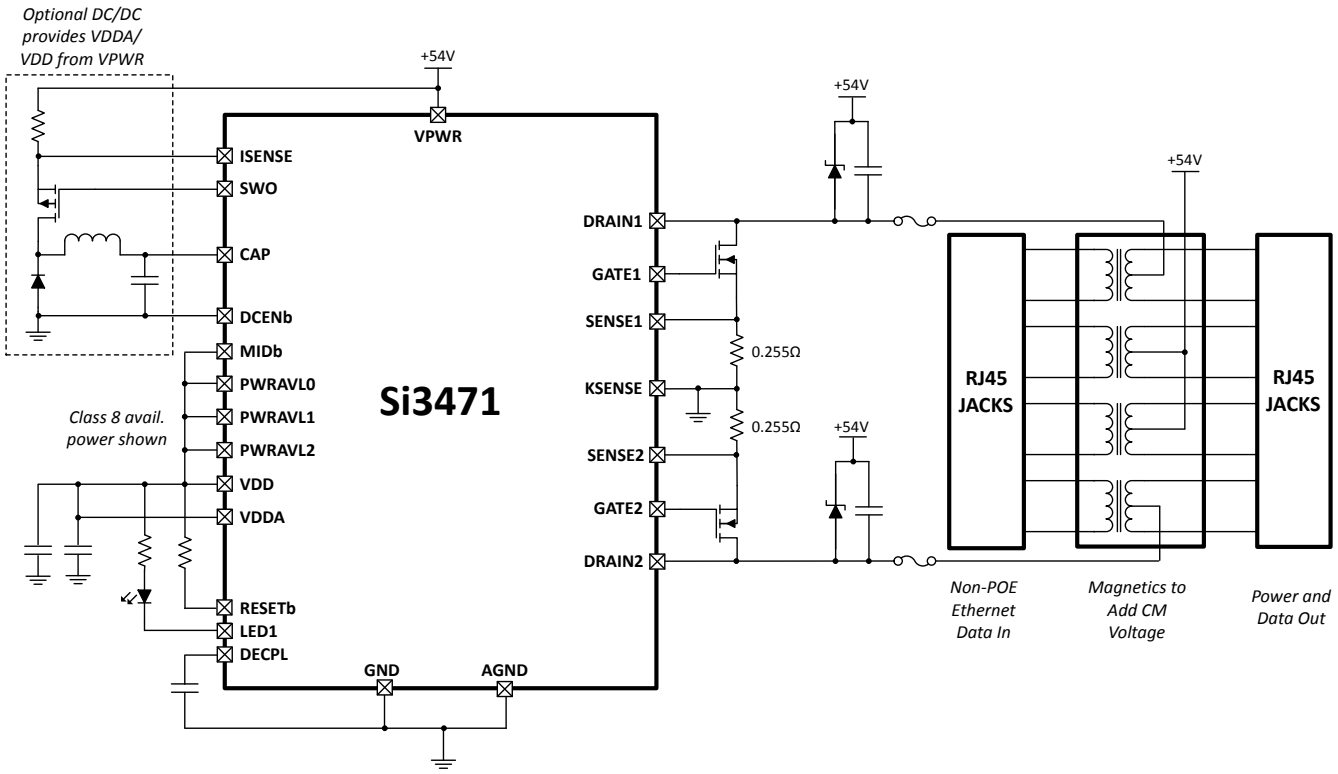


Figure 3.1. Typical Application Schematic

4. Functional Block Diagram

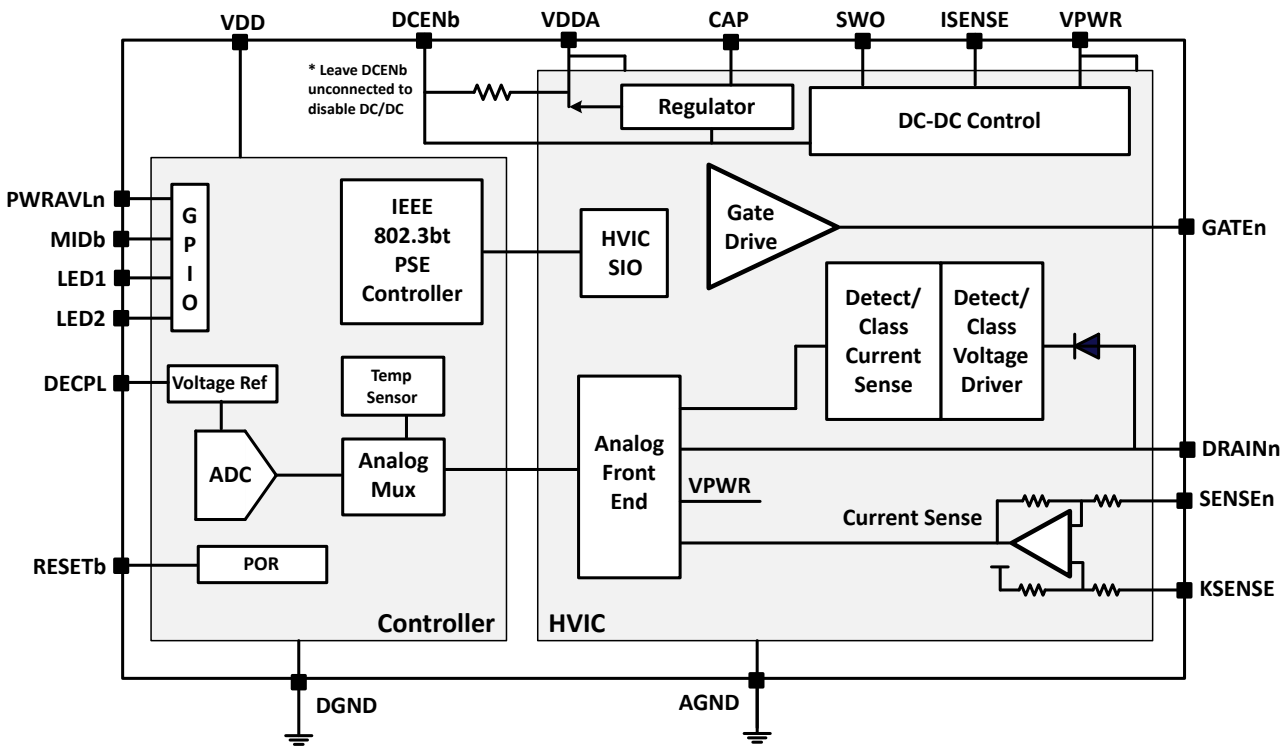


Figure 4.1. Si3471 Functional Block Diagram

5. Power Available Settings

The Si3471 can be configured to grant a maximum amount of power to a PD based on the PWRAVL pins. The Si3471 reads the PWRAVL pins at power up, upon being released from reset, or after auto-clearing a UVLO or over-temperature event. The PWRAVL pins are only read during these three conditions and cannot be dynamically adjusted while the Si3471 is operational.

The IEEE 802.3bt specification provides an option for powering a Class 4 PD using either two of the twisted pairs in the Ethernet cable or all four pairs. Using all four twisted pairs in the Ethernet cable reduces power loss in the cable, making the system more efficient. Class 2 and 3 always use only two of the four twisted pairs. An IEEE 802.3at compliant PD can be powered by either two or four pairs. When the maximum power available is Class 4, the Si3471 can be configured for either two pair or four pair operation. When the maximum power available is set to Class 5–8, the Si3471 automatically uses four pair powering for Class 4 PDs.

Table 5.1. Available Power by Class

Maximum Class	IEEE 802.3bt PSE Output Power[1]	PWRAVL2[2, 3, 4]	PWRAVL1[2, 3, 4]	PWRAVL0[2, 3, 4]
Class 8[5]	90 W	1	1	1
Class 7[5]	75 W	1	1	0
Class 6[5]	60 W	1	0	1
Class 5[5]	45 W	1	0	0
Class 4 (Four-Pair Power)[5]	30 W	0	1	1
Class 4 (Two-Pair Power)[6]	60 W (30 W per Ethernet port)	0	1	0
Class 3 (Two-Pair Power)[6]	30 W (15 W per Ethernet port)	0	0	1
Class 2 (Two-Pair Power)[6]	14 W (7 W per Ethernet port)	0	0	0

Note:

1. Si3471 PSE power supply must be sized to account for maximum class and power to operate support circuitry including the Si3471.
2. 1 = VDD
3. 0 = DGND
4. Setting MIDb = 0 PWRAVL = 011b is a reserved configuration.
5. Tie MIDb to VDD for Class 8–5 and Class 4, four-pair power. For more information see 9. Pin Descriptions.
6. In two-pair power operation, the Si3471 can be used to power one or two Ethernet ports. If only one Ethernet port is used in two-pair power operation, tie SENSEn and GATEn to AGND and leave DRAINn floating.

6. Operational Sequences and Example Waveforms

The Si3471 follows the IEEE 802.3bt specification for detection, connection check, classification, and power on. The waveforms shown below illustrate Si3471 operation for single-signature and dual-signature PDs.

Si3471 Boot-up

Upon being released from reset (RESETb pulled high), the Si3471 boots up and reads the PWRAVL configuration pins and internally sets the maximum class. The Si3471 auto-clears UVLO and over-temperature events, which also triggers the Si3471 to read the PWRAVL pins.

Detection and Connection Check

After boot up, when configured for four-pair operation (PWRAVL 111b, 110b, 101b, 100b, 011b), the Si3471 starts detection on one of the two pair sets. If a valid PD signature is found, the Si3471 executes a connection check on both pair sets. The connection check algorithm determines if a single signature or dual signature PD is connected. The Si3471 then performs detection on the second pair set to confirm a valid detection signature on both.

When configured for two-pair operation (PWRAVL 010b, 001b, 000b), each pair set is connected to a different Ethernet port, and the Si3471 treats each independently of the other. Therefore, a connection check is not performed, and the Si3471 performs detection independently on each pair set/Ethernet port.

Classification and Power On—Four Pair, Single Signature

After two valid detection signatures and a single signature connection check, the Si3471 beings the classification and power-on sequence. The first step is a class probe to determine what power the PD is requesting. Regardless of the PWRAVL setting, the Si3471 always performs a class probe. Next, the PD is reset using a class reset and the final classification and power-on sequence begins. The Si3471 always starts with a long first-class pulse to signal to the PD that it supports short maintain power signature (MPS). The Si3471 then continues with the full classification sequence to notify the PD of the granted class.

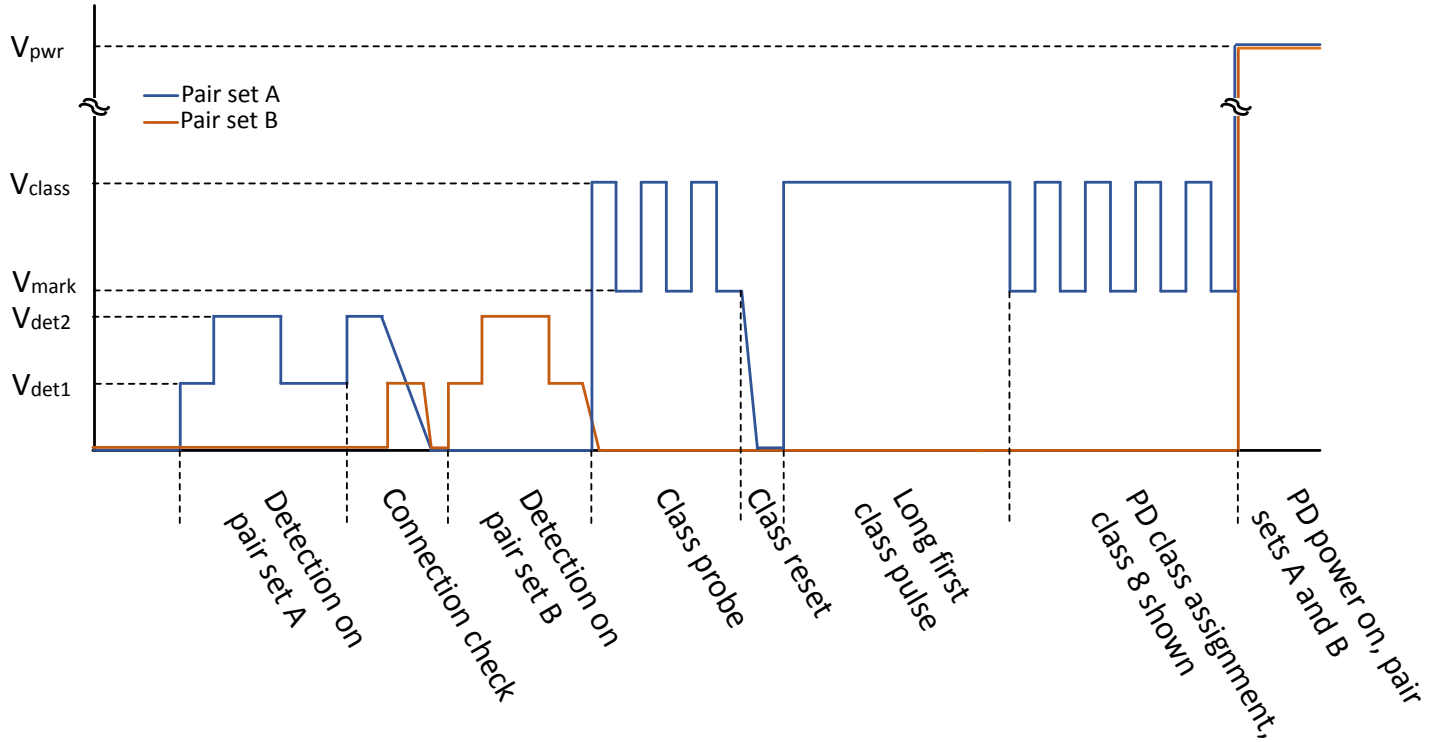


Figure 6.1. Example Waveform for 802.3bt Class 8 Single Signature Class 8

Classification and Power On—Four Pair, Dual Signature

After a valid detection signature and a dual signature connection check, the Si3471 begins the classification and power-on sequence for one of the pair sets. The first step is a class probe to determine what power the dual signature PD is requesting on one of the pair sets. Regardless of the PWRAVL setting, the Si3471 always performs a class probe. Next, the PD is reset using a class reset and the final classification and power-on sequence begins. The Si3471 always starts with a long first-class pulse to signal to the PD that it supports short maintain power signature (MPS). The Si3471 then continues with the full classification sequence to notify the PD of the granted class on one pair set. The figure below shows the classification waveform on one pair set for a Class 5 dual signature PD. Power is then applied to this pair set. The Si3471 then repeats the same procedure on the second pair set and applies power.

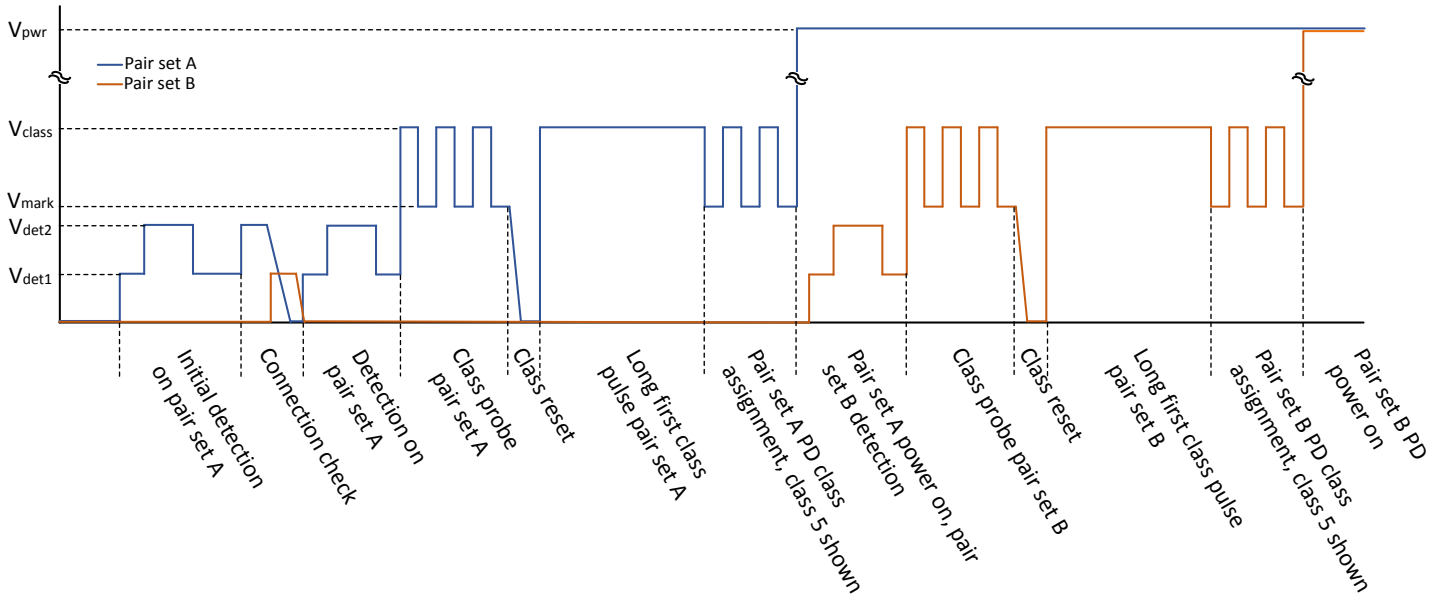


Figure 6.2. Example Waveform for 802.3bt Dual Signature PD, Class 5 on Both Pair Sets

Classification and Power On—Two Pair

After a valid detection signature, the Si3471 begins the classification and power-on sequence. The first step is a class probe to determine what power the PD is requesting. Regardless of the PWRAVL setting, the Si3471 always performs a class probe. Next, the PD is reset using a class reset and the final classification and power-on sequence begins. The Si3471 always starts with a long first-class pulse to signal to the PD that it supports short maintain power signature (MPS) even in two-pair mode. The Si3471 then continues with the full classification sequence to notify the PD of the granted class. Finally, it powers on the PD.

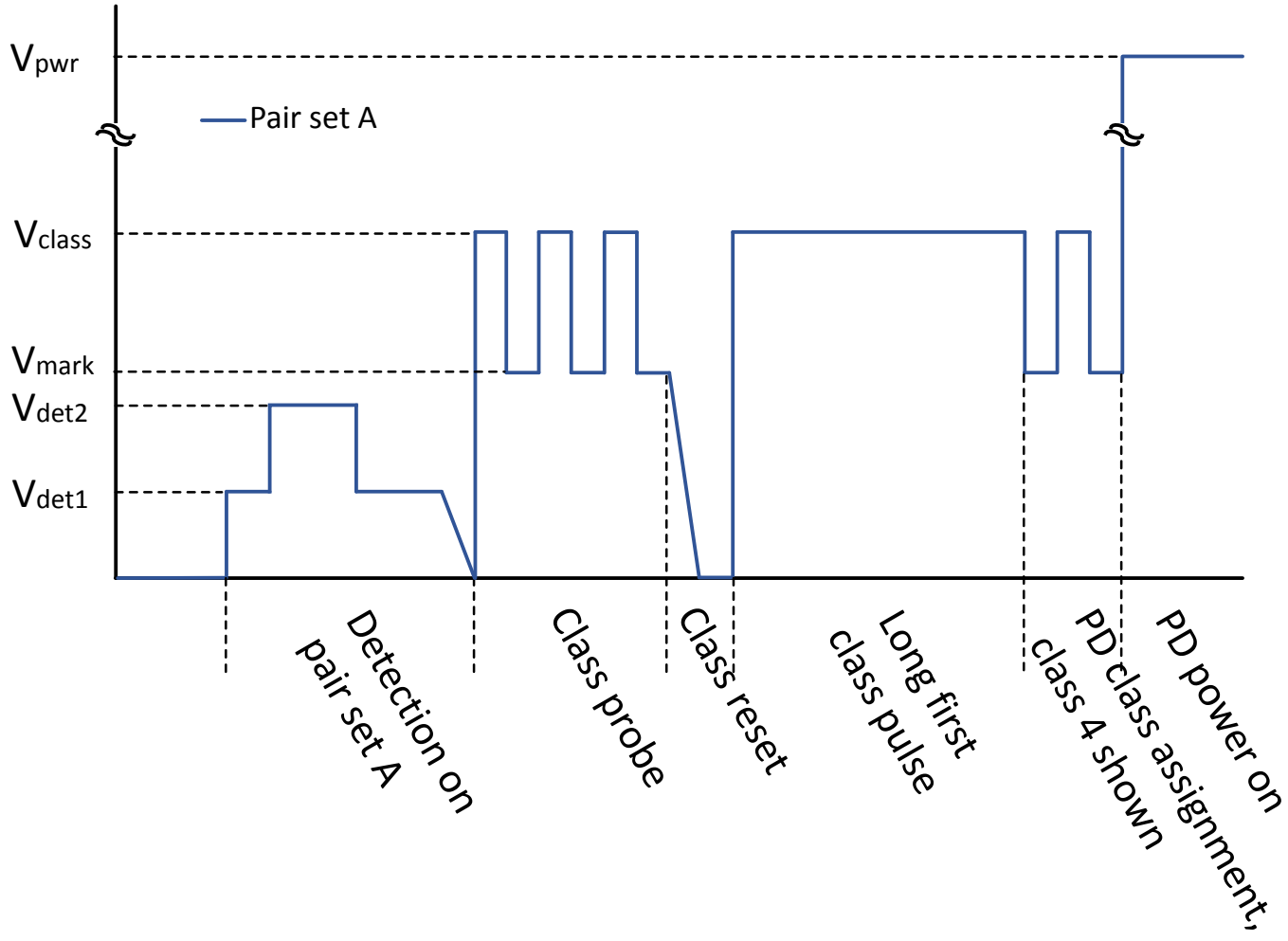


Figure 6.3. Example Waveform for 802.3at Two Pair Class 4

7. Electrical Characteristics

Table 7.1. Electrical Specifications

These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for TA = 25 °C, VDD = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 54 V. VPORTn, VCLASS, and VMARK voltages are referenced with respect to VDRAIN. All other voltages are referenced with respect to GND.

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Power Supply Voltages						
VPWR_UVLO	VPWR UVLO	Level below which chip is not operational	25	31	34	V
VPWR UVLO Input Voltage (to turn on)	VUVLO_ON		25	28	—	V
VPWR UVLO Input Voltage (to turn off)	VUVLO_OFF		—	31	34	V
VDD_UVLO	VDD UVLO	Voltage at which ports turn off	2.6	2.8	3.0	V
Hardware Reset Voltage	VRESET	VDD voltage causing reset	—	1.8	—	V
Power Supply Currents[1]						
VPWR Supply Current	IVPWR	During normal operation	—	2	5	mA
			—	7	8	mA
		VPWR = 8 V, VDD = 0 V	—	—	100	µA
VDD Supply Current	IDD	During normal operation with DCENb left floating	—	—	25	mA
Detection Specifications						
Detection Current Limit	IDET	Measured when Vdrain is shorted to VPWR	—	3.0	4.9	mA
Detection voltage when RDET =25.5 kΩ	VPORTn	Primary detection voltage	2.8	4.0	—	V
		Secondary detection voltage	—	8.0	10.0	V
Pairset Output Capacitance	Signature Capacitance		—	—	520	nF
Signature Resistance	Rgood	Signatures outside of this range will not be detected	19	—	26.5	kΩ
Minimum Signature Resistance @ PD	RDET_MIN		15	—	19	kΩ
Accept Signature Capacitance	Cgood		—	—	0.15	µF
Reject Signature Capacitance	Cbad		10	—	—	µF
Classification Specifications						
Class Event Voltage	Vclass	0 mA < ICLASS < 51 mA	15.5	—	20.5	V
Classification Reset Voltage	Vreset		0	—	2.8	V
Classification Current	IClass	Measured when Vdrain is shorted to VPWR	55	—	95	mA
Classification Reset Timing	TReset		15	—	—	ms
Class event IClass measurement timing	TClass		6	—	—	ms

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Classification Current Region	ICLASS_REGION	Class Signature 0	0	—	5	mA
		Either Class Signature 0 or 1	5	—	8	mA
		Class Signature 1	8	—	13	mA
		Either Class Signature 1 or 2	13	—	16	mA
		Class Signature 2	16	—	21	mA
		Either Class Signature 2 or 3	21	—	25	mA
		Class Signature 3	25	—	31	mA
		Either Class Signature 3 or 4	31	—	35	mA
		Class Signature 4	35	—	45	mA
		Either Class Signature 4 or invalid class	45	—	51	mA
Classification Mark Specifications						
Mark Event Voltage	VMark		7	—	10	V
Mark Event Current Limitation	IMark_LIM		5	—	100	mA
Mark Voltage	VMARK	IPORT = 0 mA	—	—	10	V
		IPORT = 5 mA	7	—	—	V
Output Voltage						
Turn on Rise Time per Pairset	Trise	IEEE Type 3-4	15	—	—	µs
Bias Current of DRAINn Pin	IDRAINn	V_{DRAINn} = 0 V	—	–25	—	µA
VPG	Power Good Threshold	Measured at VOUT with respect to GND	1.00	2.13	3.00	V
RDRAIN	Resistance from DRAIN to AGND		—	2.5	—	MΩ
IDRAIN	DRAIN pin bias current	VOUT > –10V	—	—	-6	µA
		–10V > VOUT > –30V	—	—	-18	µA
		V_{OUT} = –48V	—	-20	—	µA
Current Sense						
Sense Voltage at Overcurrent Detection	VICUT	VSENSEn – VKSENSE	89.25	95.60	102.00	mV
Sense Voltage at Current Limit	VILIM	VSENSEn – VKSENSE for VDRAINn < 30 V for IEEE Type 1	102.00	108.40	114.75	mV
		V_{SENSEn} – VKSENSE for VDRAINn < 20 V for IEEE Type 2	193.8	—	234.6	mV
		V_{SENSEn} – VKSENSE for VDRAINn > 54 V for IEEE Type 1, for VDRAINn > 44 V for IEEE Type 2	15.4	—	—	mV
DC Disconnect Sense Voltage	VDC_MIN	VSENSEn – VKSENSE	1.27	1.91	2.55	mV
SENSEn Pin Bias Current	ISENSE	VSENSEn – AGND	—	–1	—	µA
Current Sense Resistor	RSENSE	0.255 Ω, 1% tolerance				Ω

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
MOSFET Gate Drive[2]						
Drive Current from GATEn Pin (Active)		GATEn pin active VGATEn = AGND	–70	–50	–20	µA
Drive Current from GATEn Pin (Off)		GATEn pin shut off VGATEn = AGND + 5 V	—	50	—	mA
Voltage Difference Between any GATEn and AGND Pin		IGATEn = –1 µA	10	12	—	V
Digital Pin Characteristics						
Input Low Voltage	VIL	PWRAVLn	—	—	0.3 x VDD	V
Input High Voltage	VIH	RESETb, PWRAVLn	0.7 x VDD	—	—	V
Input Leakage	ILK	VDD < Vpin < VDD + 2.5 V, RESETb, PWRAVLn	0	5	150	µA
Pullup Current to VDD	IPU	RESETb, PWRAVLn	—	–20	—	µA

Note:
1. Positive values indicate currents flowing into the device. Negative currents indicate current flowing out of the device.
2. See "AN1228: FET Selection Guide for Si347x PSE Families" for detailed information on FET selection.

Table 7.2. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
VPWR Input Supply Voltage	VPWR	When generating IEEE-compliant output voltage	44	54	57	V
Analog Supply	VPWR	IEEE	44	—	57	V
VDD Supply Voltage	VDD		3.0	3.3	3.6	V
Port Voltage	VPORTn	IEEE Type 1 when port is ON	44	—	57	V
Port Voltage	VPORTn	IEEE Type 2–3 when port is ON	50	—	57	V
Port Voltage	VPORTn	IEEE Type 4 when port is ON	52	—	57	V

Note:
1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.

Table 7.3. DC-DC Converter Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Regulator Input Voltage	V_{CAP}	When DCENb is high	3.6	4.3	4.6	V
Regulator Output Voltage	V_{DDA}	55 mA load when DCENb is high	3.0	3.3	3.6	V
Regulator Output Current	I_{DDA}	When DCENb is high	0.1	—	55	mA

Table 7.4. High-Voltage Discharge

Model	Min	Unit
Human Body Model (HBM)	2	kV
Charge Device Model (CDM)	0.5	kV

Table 7.5. Absolute Maximum Ratings

Parameter	Range	Unit
Supply Voltage		
VDD	–0.3 to 4.0	V
VPWR	–0.3 to 80.0	V
DGND with Respect to AGND	0	V
Digital Signals		
All	–0.3 to 3.6	V
Analog Signals		
GATE with Respect to GND	–0.3 to 20.0	V
SOURx with Respect to GND	–0.3 to 3.0	V
DRAINx with Respect to GND	–3 to 80	V
Temperature[1]		
Junction	+150	°C
Storage	–55 to +150	°C
Solder (10 seconds)	+300	°C
Operation Ambient Temperature	–40 to +85	°C

Note:
1. Si3471 includes internal thermal shutdown above 150 °C.

8. DC-DC Converter Description

The Si3471 includes a dc-dc converter for generation of an approximately 4.3 V intermediate power rail, which is further down-regulated by an on-chip LDO to create the 3.3 V VDD power rail necessary for MCU operation and other support. The LDO is enabled by asserting (tying low) DCENb. The 3.3 V output of the LDO can also be used to power other 3.3 V devices in the system.

The dc-dc converter consists of a buck converter with accompanying external components to step down VPWR to approximately 4.3 V.

The ISENSE pin implements a cycle-by-cycle current limit by comparing a sensed voltage to an internal reference. When the external transistor is conducting, if ISENSE drops more than 200 mV below VPWR, the transistor will be shut off immediately to limit excessive currents. An appropriate external resistor should be selected to set the desired peak current level (i.e., Ipeak = 200 mV/Rsense). If ISENSE is left floating, an internal pull-up will effectively disable the current limit feature. A FET or bipolar transistor with appropriate base current limiting resistors can be used for the switching transistor.

The 4.3 V converter is a hysteretic controller that senses when the output capacitor is less than 3.6 V and turns on a switch for ~1 µs to recharge the capacitor through a 100 µH inductor. After the switch turns off, the inductor continues to charge the capacitor for several microseconds giving an average output voltage of approximately 4.3 V.

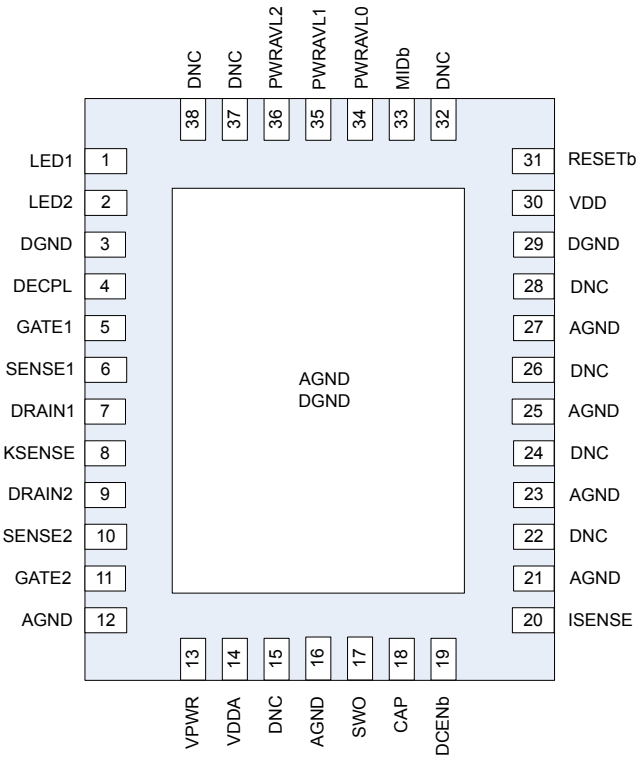
At start up, the duty cycle of the switch is allowed to gradually increase to give a soft start with the recommended 10 µF filter capacitor.

If an extreme overcurrent event (e.g., short-circuit) should occur, the dc-dc output voltage, CAP, will drop below its target level of 3.6 V. If CAP falls below 90% of that level (i.e., 3.24 V), a dc-dc fault will be declared, and the dc-dc and LDO will power down. The dc-dc will then attempt to restart at 4 ms intervals until the overcurrent fault is removed.

If DCENb is left floating, the dc-dc converter is disabled, which eliminates excess current draw by the VPWR pin. To disable the dc-dc converter, the related pins (DCENb, CAP, and SWO) should be left floating.

The dc-dc convertor can also be used to power additional Si3471 devices. The intermediate 4.3 V rail can be bussed to up to five adjacent, secondary Si3471s. Each Si3471 includes a series regulator for generation of 3.3 V for local use by that controller and other components in the system. While the primary controller requires several external components to enable the dc-dc, the secondary controllers do not require those external components. On the secondary controllers, the SWO pin should be direct-tied to VPWR. DCENb should be asserted on the primary and all secondary controllers.

9. Pin Descriptions



Pin	Name	Type	Description
1	LED1	Digital Output	Turns on an external LED when a PoE PD is connected and powered. When using Si3471 in 802.3at mode, LED1 turns on an external LED to indicate the status of Ethernet Port 1.
2	LED2	Digital Output	Leave floating when using Si3471 in 802.3bt mode. When using Si3471 in 802.3at mode, LED2 turns on an external LED to indicate the status of Ethernet Port 2.
15, 22, 24, 26, 28, 32, 37, 38	DNC	No Connect	No connections or nets allowed. Leave floating.
3, 29, ePAD	DGND	Digital Ground	Ground connection for 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3471 package.
4	DECPL	Analog Input	Add a 0.1 µF capacitor to this pin.
5	GATE1	Analog Output	Gate drive outputs to external MOSFETs. Connect the GATEn outputs to the external MOSFET gate node gate. A 50 µA pull-up source is used to turn on the external MOSFET. When a current limit is detected, the GATEn voltage is reduced to maintain constant current through the external MOSFET. If the fault timer limit is reached, GATEn pulls down, shutting off the external MOSFET. GATEn will clamp to 11.5 V (typical) above AGND. If the port is unused, leave the GATEn pin disconnected or tie to AGND.
11	GATE2		
6	SENSE1	Analog Input	Current sense inputs for external MOSFETs. The SENSEn pin measures current through an external 0.255 Ω resistor tied between the AGND supply rail and the SENSEn input. If the voltage across the sense resistor subsequently triggers (the overcurrent limit), the voltage driven onto the GATEn pin is modulated to provide constant current through the external MOSFET. Tie the SENSEn pin to AGND when the port is not used.
10	SENSE2		

Pin	Name	Type	Description
7	DRAIN1	Analog input with 25 µA pull-up to VPWR	MOSFET drain output voltage sense. DRAINn pins should be left floating if the port is unused.
9	DRAIN2		
8	KSENSE	Analog Input	Kelvin point for accurate measurement of voltage across 0.255 Ω sense resistor
13	VPWR	Analog Power	Positive PoE voltage (+44 to +57 V) relative to AGND.
14	VDDA	Analog Power	3.3 V supply to the analog side; tied with VDD at the PCB level.
12, 16, 21, 23, 25, 27, ePAD	AGND	Analog Ground	Ground connection for VPWR supply. DGND and AGND are tied together inside the Si3471 package.
17	SWO	Analog Output	Gate driver output for the external MOSFET component of the dcdc converter. If using only the local regulator of the part, tie SWO to VPWR. If not using the dc-dc converter or local regulator, leave this pin floating.
18	CAP	Analog Input	Input from the dc-dc converter. This elevated voltage can be bussed to the Si3471 and it will be down-regulated to VDD for local use.
19	DCENb	Digital input with 25 µA pull-up to VDD	Tie DCENb to DGND to enable the dc-dc converter and local regulator. If using only the local regulator of the part, DCENb must also be tied to DGND. If not using the dc-dc converter or local regulator, leave this pin floating.
20	ISENSE	Analog Input	Current sense input for dc-dc converter to detect overcurrent and short circuit conditions.
30	VDD	Digital Power	3.3 V digital supply (relative to DGND). Bypass VDD with a 0.1 µF capacitor to DGND as close as possible to the Si3471 power supply pins; tied with VDDA.
31	RESETb	Digital input with 20 µA pull-up to VDD	Active low device reset input. Generally, RESET is used at initial power up. If RESETb is asserted (pulled to DGND), the MCU is disabled, all internal regis- ters of the device are set to their default (power-up) state, and all output ports are shut off. Valid RESETb timing pulses must be >10 µs. If RESETb is not used, RESETb should be left floating.
33	MIDb	Digital Input	For 802.3bt operation, tie MIDb to VDD. For 802.3at 2 pair operation, configures the Si3471 to operate as a mid span or end span as follows: DGND = mid span, 2 second detection back off mode for powering on ALTB. VDD = end span, <400 msec detection intervals for powering on ALTA.
34	PWRAVL0	Digital Input	Sets the maximum power available to the Si3471.
35	PWRAVL1		
36	PWRAVL2		

10. Package Outline: 38-Pin QFN

The figure below illustrates the package details for the Si3471. The table lists the values for the dimensions shown in the illustration. The Si3471 is packaged in an industry-standard, RoHS-compliant, 38-pin QFN package. The lead plating material is matte tin.

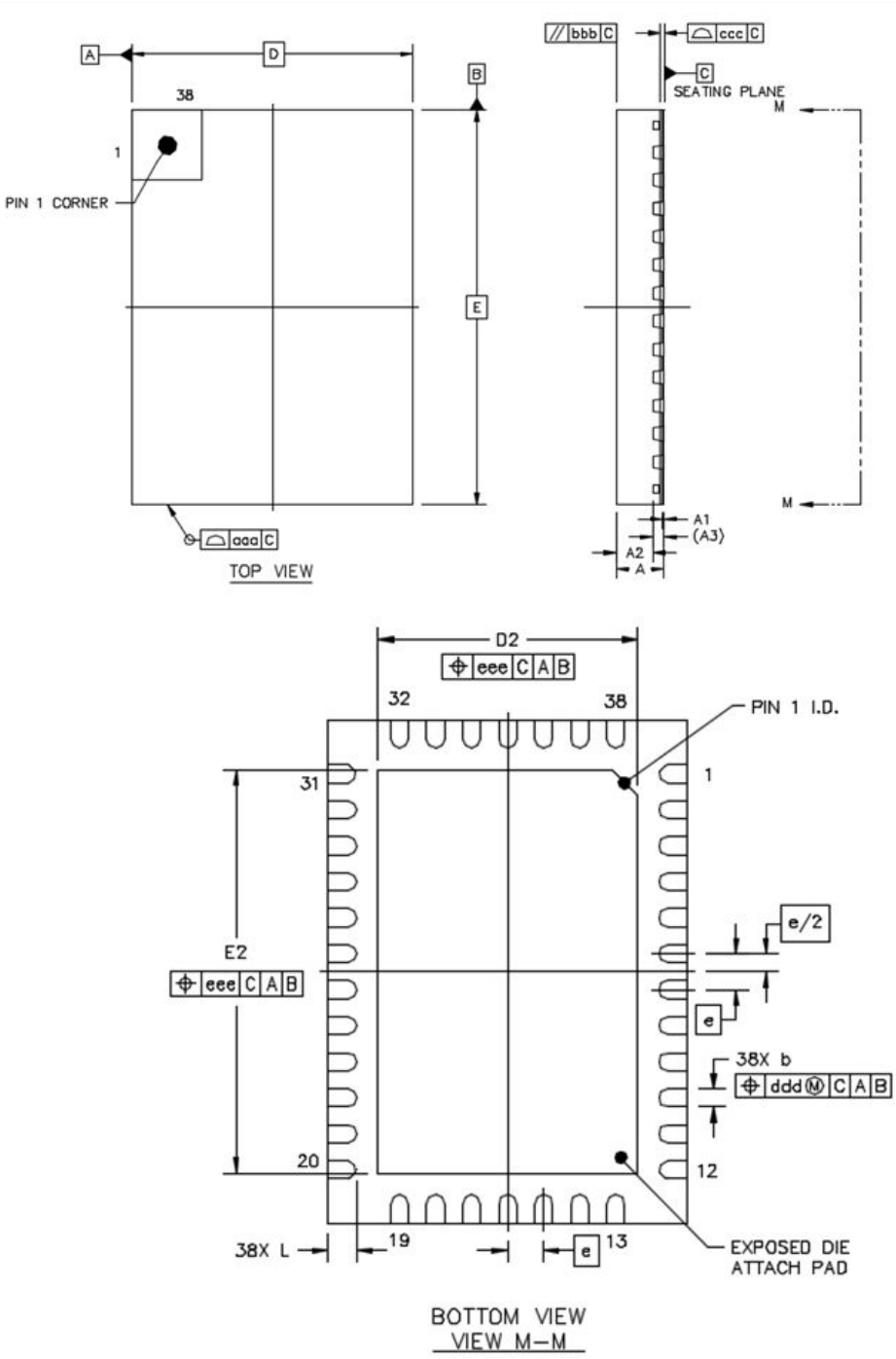


Figure 10.1. 38-Pin QFN Package

Table 10.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	6.90	7.00	7.10
D2	3.50	3.60	3.70
E2	5.50	5.60	5.70
e		0.50 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VLLD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Land Pattern

The following figure illustrates the land pattern details for the Si3471. The table lists the values for the dimensions shown in the illustration. The stencil design and notes are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

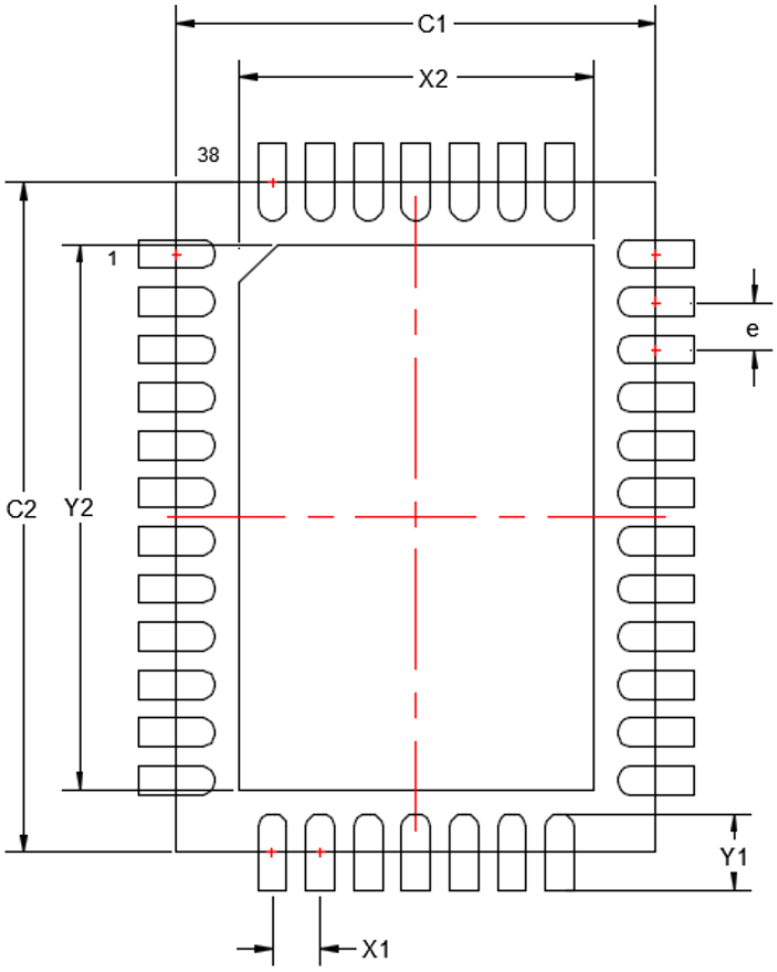


Figure 11.1. Si3471 Recommended Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Symbol	mm
C1	5.00
C2	7.00
e	0.50
X1	0.30
Y1	0.85
X2	3.70
Y2	5.70

Symbol	mm

Notes:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 3x5 array of 0.90 mm square openings on 1.10 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

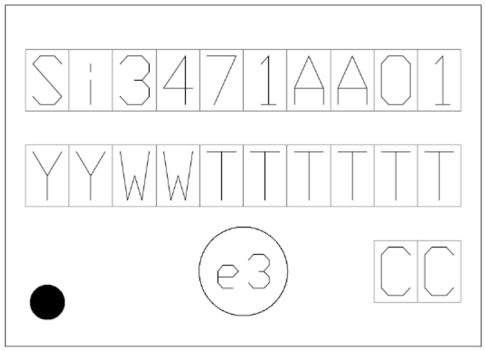


Figure 12.1. Si3471A Top Marking (QFN)

Table 12.1. Top Marking Explanation

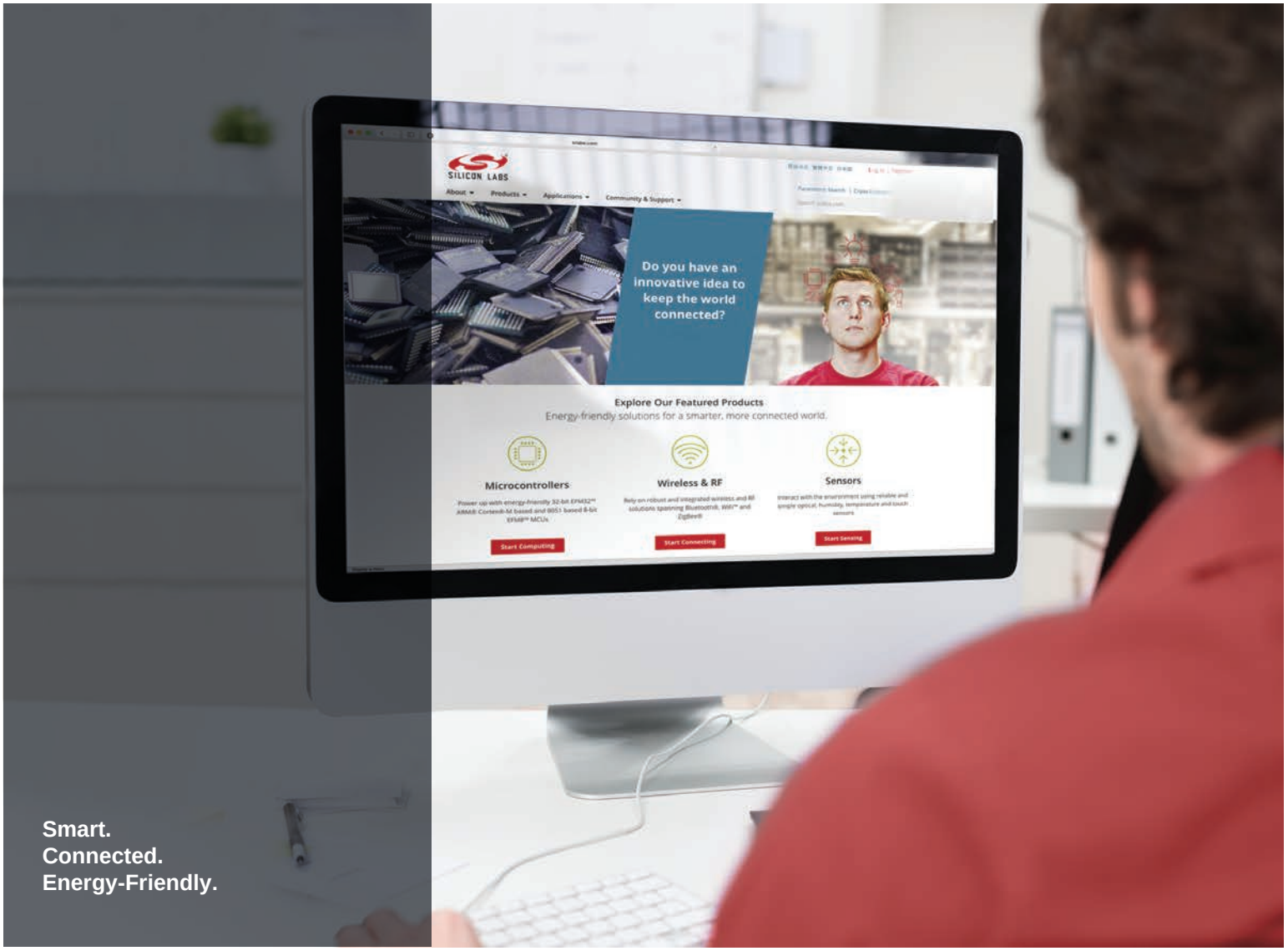
Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left-Justified	
Line 1 Mark Format:	Device Part Number	Si3471AA01
Line 2 Mark Format:	YY = Year WW = Work Week TTTTTT = Mfg Code	Year and Work Week of Assembly Manufacturing Code
Line 3 Mark Format:	Circle = 1.3 mm Diameter Country of Origin	“e3” Pb-Free Symbol TW = Taiwan

13. Revision History

Revision 0.1

February, 2019

- Initial release.



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