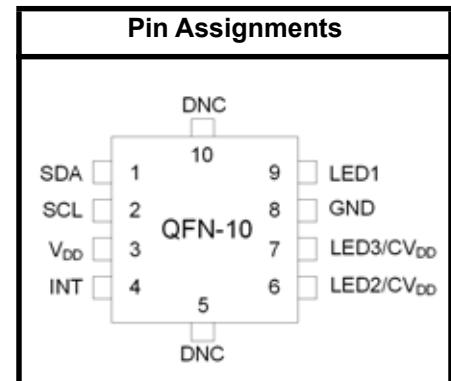


# PROXIMITY/AMBIENT LIGHT SENSOR IC WITH I<sup>2</sup>C INTERFACE

## Features

- Integrated infrared proximity detector
  - Proximity detection adjustable from under 1 cm up to 200 cm
  - Three independent LED drivers
  - 15 current settings from 5.6 mA to 360 mA for each LED driver
  - 25.6  $\mu$ s LED driver pulse width
  - 50 cm proximity range with single pulse (<3 klx)
  - 15 cm proximity range with single pulse (>3 klx)
  - Operates at up to 128 klx (direct sunlight)
  - High reflectance sensitivity < 1  $\mu$ W/cm<sup>2</sup>
  - High EMI immunity without shielded packaging
- Integrated ambient light sensor
  - 100 mlx resolution possible, allowing operation under dark glass
  - 1 to 128 klx dynamic range possible across two ADC range settings
- Accurate lux measurements with IR correction algorithm
- Industry's lowest power consumption
  - 1.71 to 3.6 V supply voltage
  - 9  $\mu$ A average current (LED pulsed 25.6  $\mu$ s every 800 ms at 180 mA plus 3  $\mu$ A Si114x supply)
  - < 500 nA standby current
  - 25.6  $\mu$ s LED "on" time keeps total power consumption duty cycle low without compromising performance or noise immunity
  - Internal and external wake support
  - Built-in voltage supply monitor and power-on reset controller
- Serial communications
  - Up to 3.4 Mbps data rate
  - Slave mode hardware address decoding (0x5A)
- Small-outline 10-lead 2x2 mm QFN
- Temperature Range
  - -40 to +85 °C



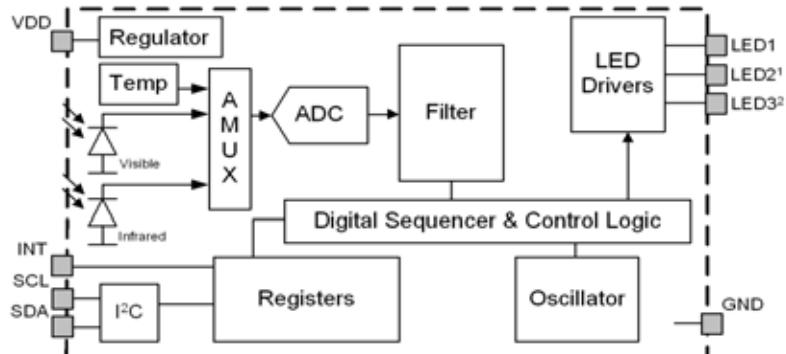
## Applications

- Handsets
- Heart rate monitoring
- Pulse oximetry
- Wearables
- Audio products
- Security panels
- Tamper detection circuits
- Dispensers
- Valve controls
- Smoke detectors
- Touchless switches
- Touchless sliders
- Occupancy sensors
- Consumer electronics
- Industrial automation
- Display backlighting control
- Photo-interrupters

## Description

The Si1141/42/43 is a low-power, reflectance-based, infrared proximity and ambient light sensor with I<sup>2</sup>C digital interface and programmable-event interrupt output. This touchless sensor IC includes an analog-to-digital converter, integrated high-sensitivity visible and infrared photodiodes, digital signal processor, and one, two, or three integrated infrared LED drivers with fifteen selectable drive levels. The Si1141/42/43 offers excellent performance under a wide dynamic range and a variety of light sources including direct sunlight. The Si1141/42/43 can also work under dark glass covers. The photodiode response and associated digital conversion circuitry provide excellent immunity to artificial light flicker noise and natural light flutter noise. With two or more LEDs, the Si1142/43 is capable of supporting multiple-axis proximity motion detection. The Si1141/42/43 devices are provided in a 10-lead 2x2 mm QFN package and are capable of operation from 1.71 to 3.6 V over the -40 to +85 °C temperature range.

## Functional Block Diagram



1. Si1142 and Si1143 only. Must be tied to V<sub>DD</sub> with Si1141.  
2. Si1143 only. Must be tied to V<sub>DD</sub> with Si1141 and Si1142.

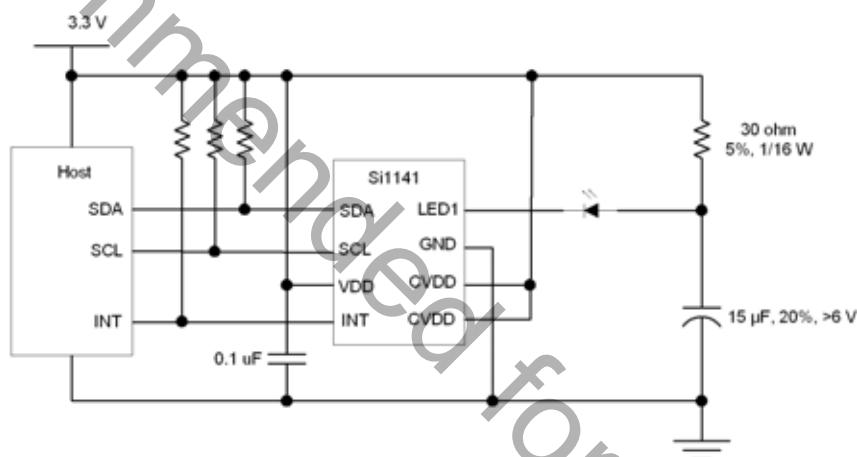


Figure 1. Si1141 Basic Application

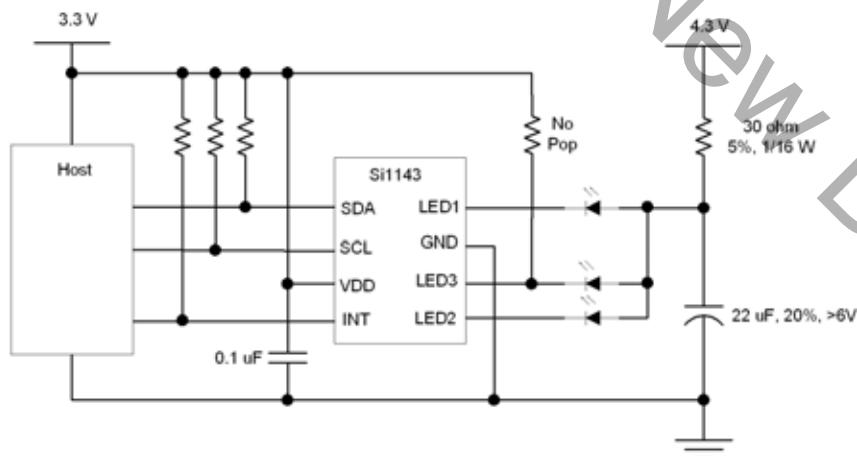


Figure 2. Si1143 Application with Three LEDs and Separate LED Power Supply

Note: For more application examples, refer to "AN498: Si114x Designer's Guide".

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## 1. Electrical Specifications

### 1.1. Performance Tables

Table 1. Recommended Operating Conditions

| Parameter                             | Symbol                          | Test Condition   | Min                   | Typ | Max                  | Unit         |
|---------------------------------------|---------------------------------|--|-----------------------|-----|----------------------|--------------|
| V <sub>DD</sub> Supply Voltage        | V <sub>DD</sub>                 |  | 1.71                  | —   | 3.6                  | V            |
| V <sub>DD</sub> OFF Supply Voltage    | V <sub>DD_OFF</sub>             | OFF mode   | -0.3                  | —   | 1.0                  | V            |
| V <sub>DD</sub> Supply Ripple Voltage |                                 | V <sub>DD</sub> = 3.3 V<br>1 kHz–10 MHz                                  | —                     | —   | 50                   | mVpp         |
| Operating Temperature                 | T                               |  | -40                   | 25  | 85                   | °C           |
| SCL, SDA, Input High Logic Voltage    | I <sup>2</sup> C <sub>VIH</sub> |  | V <sub>DD</sub> ×0.7  | —   | V <sub>DD</sub>      | V            |
| SCL, SDA Input Low Logic Voltage      | I <sup>2</sup> C <sub>VIL</sub> |  | 0                     | —   | V <sub>DD</sub> ×0.3 | V            |
| PS Operation under Direct Sunlight    | E <sub>dc</sub>                 |  | —                     | —   | 128                  | klx          |
| IrLED Emission Wavelength             | λ                               |  | 750                   | 850 | 950                  | nm           |
| IrLED Supply Voltage                  | V <sub>LED</sub>                | IrLED V <sub>F</sub> = 1.0 V nominal                                     | V <sub>DD</sub>       | —   | 4.3                  | V            |
| IrLED Supply Ripple Voltage           |                                 | Applies if IrLEDs use separate supply rail<br>0–30 kHz<br>30 kHz–100 MHz | —                     | —   | 250<br>100           | mVpp<br>mVpp |
| Start-Up Time                         |                                 | V <sub>DD</sub> above 1.71 V   | 25                    | —   | —                    | ms           |
| LED3 Voltage                          |                                 | Start-up   | V <sub>DD</sub> ×0.77 | —   | —                    | V            |

Table 2. Performance Characteristics<sup>1</sup>

| Parameter                    | Symbol           | Test Condition  | Min | Typ | Max  | Unit |
|------------------------------|------------------|---|-----|-----|------|------|
| I <sub>DD</sub> OFF Mode     | I <sub>off</sub> | V <sub>DD</sub> < V <sub>DD_OFF</sub> (leakage from SCL, SDA, and INT not included) | —   | 240 | 1000 | nA   |
| I <sub>DD</sub> Standby Mode | I <sub>sb</sub>  | No ALS / PS Conversions<br>No I <sup>2</sup> C Activity<br>V <sub>DD</sub> = 1.8 V  | —   | 150 | 500  | nA   |

Notes:

1. Unless specifically stated in "Conditions", electrical data assumes ambient light levels < 1 klx.
2. Proximity-detection performance may be degraded, especially when there is high optical crosstalk, if the LED supply and voltage drop allow the driver to saturate and current regulation is lost.
3. Guaranteed by design and characterization.
4. Represents the time during which the device is drawing a current equal to I<sub>active</sub> for power estimation purposes. Assumes default settings.

Table 2. Performance Characteristics<sup>1</sup> (Continued)

| Parameter   | Symbol              | Test Condition  | Min | Typ   | Max   | Unit |
|---|---------------------|---|-----|---|---|------|
| I <sub>DD</sub> Standby Mode                                      | I <sub>sb</sub>     | No ALS / PS Conversions<br>No I <sup>2</sup> C Activity<br>V <sub>DD</sub> = 3.3 V  | —   | 1.4   | —   | µA   |
| I <sub>DD</sub> Actively Measuring                                | I <sub>active</sub> | Without LED influence, V <sub>DD</sub> = 3.3 V  | —   | 4.3   | 5.5   | mA   |
| Peak I <sub>DD</sub> while LED1, LED2, or LED3 is Actively Driven |                     | V <sub>DD</sub> = 3.3 V   | —   | 8   | —   | mA   |
| LED Driver Saturation Voltage <sup>2,3</sup>                      |                     | V <sub>dd</sub> = 1.71 to 3.6 V<br>PS_LEDn = 0001<br>PS_LEDn = 0010<br>PS_LEDn = 0011<br>PS_LEDn = 0100<br>PS_LEDn = 0101<br>PS_LEDn = 0110<br>PS_LEDn = 0111<br>PS_LEDn = 1000<br>PS_LEDn = 1010<br>PS_LEDn = 1010<br>PS_LEDn = 1011<br>PS_LEDn = 1100<br>PS_LEDn = 1101<br>PS_LEDn = 1110<br>PS_LEDn = 1111 | —   | 50<br>60<br>70<br>80<br>115<br>150<br>185<br>220<br>255<br>290<br>315<br>340<br>360<br>385<br>410 | 70<br>105<br>105<br>105<br>450<br>450<br>450<br>450<br>450<br>450<br>600<br>600<br>600<br>600 | mV   |
| LED1, LED2, LED3 Pulse Width                                      | t <sub>PS</sub>     |   | —   | 25.6  | 30  | µs   |
| LED1, LED2, LED3, INT, SCL, SDA Leakage Current                   |                     | V <sub>DD</sub> = 3.3 V   | —1  | —   | 1   | µA   |

**Notes:**

1. Unless specifically stated in "Conditions", electrical data assumes ambient light levels < 1 klx.
2. Proximity-detection performance may be degraded, especially when there is high optical crosstalk, if the LED supply and voltage drop allow the driver to saturate and current regulation is lost.
3. Guaranteed by design and characterization.
4. Represents the time during which the device is drawing a current equal to I<sub>active</sub> for power estimation purposes. Assumes default settings.

**Table 2. Performance Characteristics<sup>1</sup> (Continued)**

Table 2. Performance Characteristics<sup>1</sup> (Continued)

| Parameter   | Symbol | Test Condition   | Min | Typ    | Max | Unit                         |
|---|--------|--|-----|--------|-----|------------------------------|
| Small Infrared Photodiode Response  |        | Sunlight<br>ALS_IR_ADC_GAIN = 0<br>IR_RANGE = 0                                | —   | 2.44   | —   | ADC counts/lux               |
|   |        | 2500K incandescent bulb<br>ALS_IR_ADC_GAIN = 0<br>IR_RANGE = 0                 | —   | 8.46   | —   | ADC counts/lux               |
|   |        | “Cool white” fluorescent<br>ALS_IR_ADC_GAIN = 0<br>IR_RANGE = 0                | —   | 0.71   | —   | ADC counts/lux               |
|   |        | Infrared LED (875 nm)<br>ALS_IR_ADC_GAIN = 0<br>IR_RANGE = 0                   | —   | 452.38 | —   | ADC counts.m <sup>2</sup> /W |
| Large Infrared Photodiode Response  |        | Sunlight<br>PS_ADC_GAIN = 0<br>PS_RANGE = 0<br>PS_ADC_MODE = 0                 | —   | 14.07  | —   | ADC counts/lux               |
|   |        | 2500K incandescent bulb<br>PS_ADC_GAIN = 0<br>PS_RANGE = 0<br>PS_ADC_MODE = 0  | —   | 50.47  | —   | ADC counts/lux               |
|   |        | “Cool white” fluorescent<br>PS_ADC_GAIN = 0<br>PS_RANGE = 0<br>PS_ADC_MODE = 0 | —   | 3.97   | —   | ADC counts/lux               |
|   |        | Infrared LED (875 nm)<br>PS_ADC_GAIN = 0<br>PS_RANGE = 0<br>PS_ADC_MODE = 0    | —   | 2734   | —   | ADC counts.m <sup>2</sup> /W |
| Visible Photodiode Noise  |        | All gain settings  | —   | 7      | —   | ADC counts RMS               |
| Small Infrared Photodiode Noise   |        | All gain settings  | —   | 1      | —   | ADC counts RMS               |
| <b>Notes:</b>   |        |  |     |        |     |                              |
| <ol style="list-style-type: none"> <li>1. Unless specifically stated in “Conditions”, electrical data assumes ambient light levels &lt; 1 klx.</li> <li>2. Proximity-detection performance may be degraded, especially when there is high optical crosstalk, if the LED supply and voltage drop allow the driver to saturate and current regulation is lost.</li> <li>3. Guaranteed by design and characterization.</li> <li>4. Represents the time during which the device is drawing a current equal to <math>I_{active}</math> for power estimation purposes. Assumes default settings.</li> </ol> |        |  |     |        |     |                              |

Table 2. Performance Characteristics<sup>1</sup> (Continued)

| Parameter                              | Symbol          | Test Condition  | Min    | Typ  | Max                          | Unit           |
|--|-----------------|---|--------|--|------------------------------|----------------|
| Large Infrared Photodiode Noise        |                 | All gain settings   | —      | 10   | —                            | ADC counts RMS |
| Visible Photodiode Offset Drift        |                 | VIS_RANGE = 0<br>ALS_VIS_ADC_GAIN = 0<br>ALS_VIS_ADC_GAIN = 1<br>ALS_VIS_ADC_GAIN = 2<br>ALS_VIS_ADC_GAIN = 3<br>ALS_VIS_ADC_GAIN = 4<br>ALS_VIS_ADC_GAIN = 5<br>ALS_VIS_ADC_GAIN = 6<br>ALS_VIS_ADC_GAIN = 7 | —      | -0.3<br>-0.11<br>-0.06<br>-0.03<br>-0.01<br>-0.008<br>-0.007<br>-0.008 | —                            | ADC counts/°C  |
| Small Infrared Photodiode Offset Drift |                 | IR_RANGE = 0<br>IR_GAIN = 0<br>IR_GAIN = 1<br>IR_GAIN = 2<br>IR_GAIN = 3  | —      | -0.3<br>-0.06<br>-0.03<br>-0.01  | —                            | ADC counts/°C  |
| SCL, SDA, INT Output Low Voltage       | V <sub>OL</sub> | I = 4 mA, V <sub>DD</sub> > 2.0 V<br>I = 4 mA, V <sub>DD</sub> < 2.0 V  | —<br>— | —<br>—   | V <sub>DD</sub> x 0.2<br>0.4 | V<br>V         |
| Temperature Sensor Offset              |                 | 25 °C   | —      | 11136  | —                            | ADC counts     |
| Temperature Sensor Gain                |                 |   | —      | 35   | —                            | ADC counts/°C  |

**Notes:**

1. Unless specifically stated in "Conditions", electrical data assumes ambient light levels < 1 klx.
2. Proximity-detection performance may be degraded, especially when there is high optical crosstalk, if the LED supply and voltage drop allow the driver to saturate and current regulation is lost.
3. Guaranteed by design and characterization.
4. Represents the time during which the device is drawing a current equal to I<sub>active</sub> for power estimation purposes. Assumes default settings.

**Table 3. I<sup>2</sup>C Timing Specifications**

| Parameter                  | Symbol       | Min  | Typ | Max | Unit |
|----------------------------|--------------|------|-----|-----|------|
| Clock Frequency            | $f_{SCL}$    | 0.09 | —   | 3.4 | MHz  |
| Clock Pulse Width Low      | $t_{LOW}$    | 160  | —   | —   | ns   |
| Clock Pulse Width High     | $t_{HIGH}$   | 60   | —   | —   | ns   |
| Rise Time                  | $t_R$        | 10   | —   | 40  | ns   |
| Fall Time                  | $t_F$        | 10   | —   | 40  | ns   |
| Start Condition Hold Time  | $t_{HD.STA}$ | 160  | —   | —   | ns   |
| Start Condition Setup Time | $t_{SU.STA}$ | 160  | —   | —   | ns   |
| Input Data Setup Time      | $t_{SU.DAT}$ | 10   | —   | —   | ns   |
| Input Data Hold Time       | $t_{HD.DAT}$ | 0    | —   | —   | ns   |
| Stop Condition Setup Time  | $t_{SU.STO}$ | 160  | —   | —   | ns   |

**Table 4. Absolute Maximum Limits**

| Parameter   | Test Condition  | Min         | Typ         | Max           | Unit          |
|---|---|-------------|-------------|---------------|---------------|
| $V_{DD}$ Supply Voltage                           |   | -0.3        | —           | 4             | V             |
| Operating Temperature                             |   | -40         | —           | 85            | °C            |
| Storage Temperature                               |   | -65         | —           | 85            | °C            |
| LED1, LED2, LED3 Voltage                          | at $V_{DD} = 0$ V, $T_A < 85$ °C                          | -0.5        | —           | 3.6           | V             |
| INT, SCL, SDA Voltage                             | at $V_{DD} = 0$ V, $T_A < 85$ °C                          | -0.5        | —           | 3.6           | V             |
| Maximum total current through LED1, LED2 and LED3 |   | —           | —           | 500           | mA            |
| Maximum total current through GND                 |   | —           | —           | 600           | mA            |
| ESD Rating  | Human Body Model<br>Machine Model<br>Charged-Device Model | —<br>—<br>— | —<br>—<br>— | 2<br>225<br>2 | kV<br>V<br>kV |

## 1.2. Typical Performance Graphs

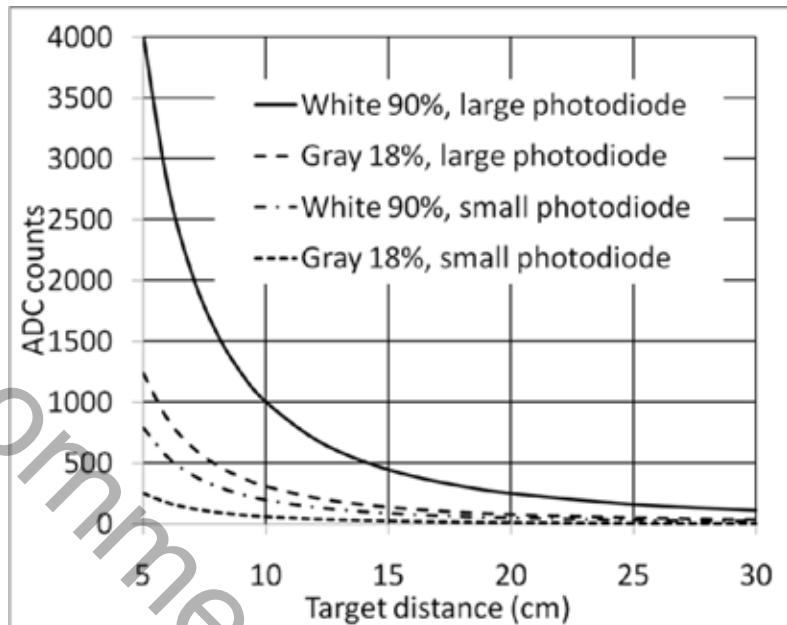


Figure 3. Proximity response using Kodak gray cards, PS\_RANGE = 0, PS\_ADC\_GAIN = 0 (single 25.6 $\mu$ s LED pulse),  $\pm 22^\circ$ LED view angle, 850 nm, 22.5 mW/sr, no overlay, 5 mm LED center to Si114x center

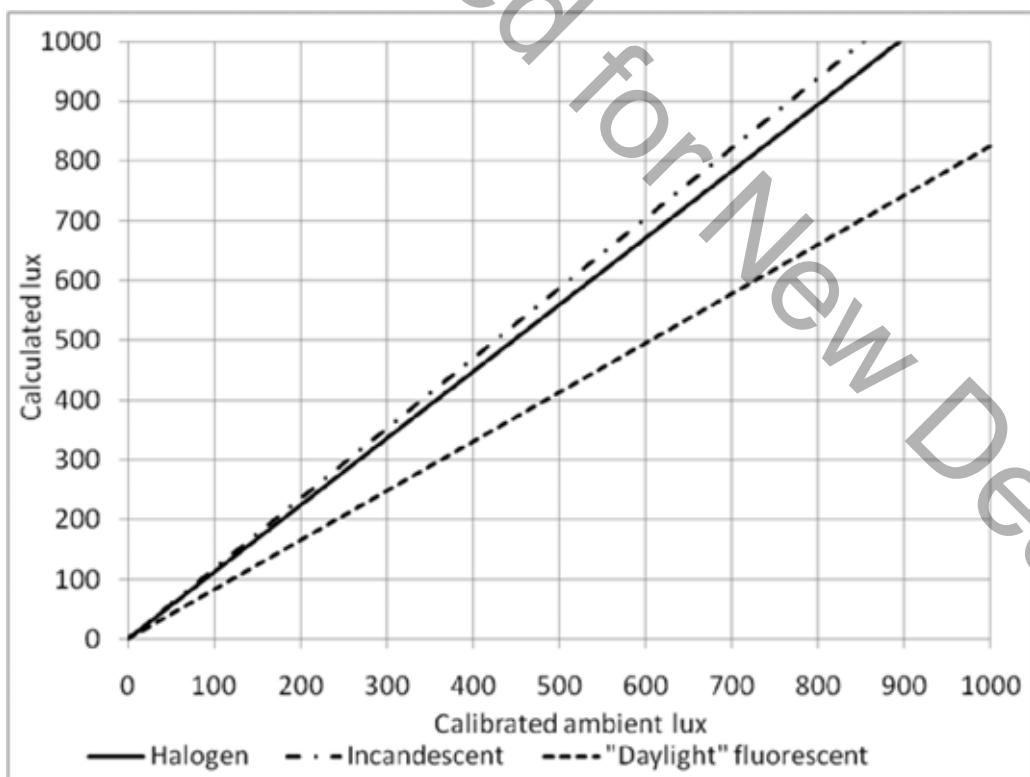


Figure 4. ALS variability with different light sources

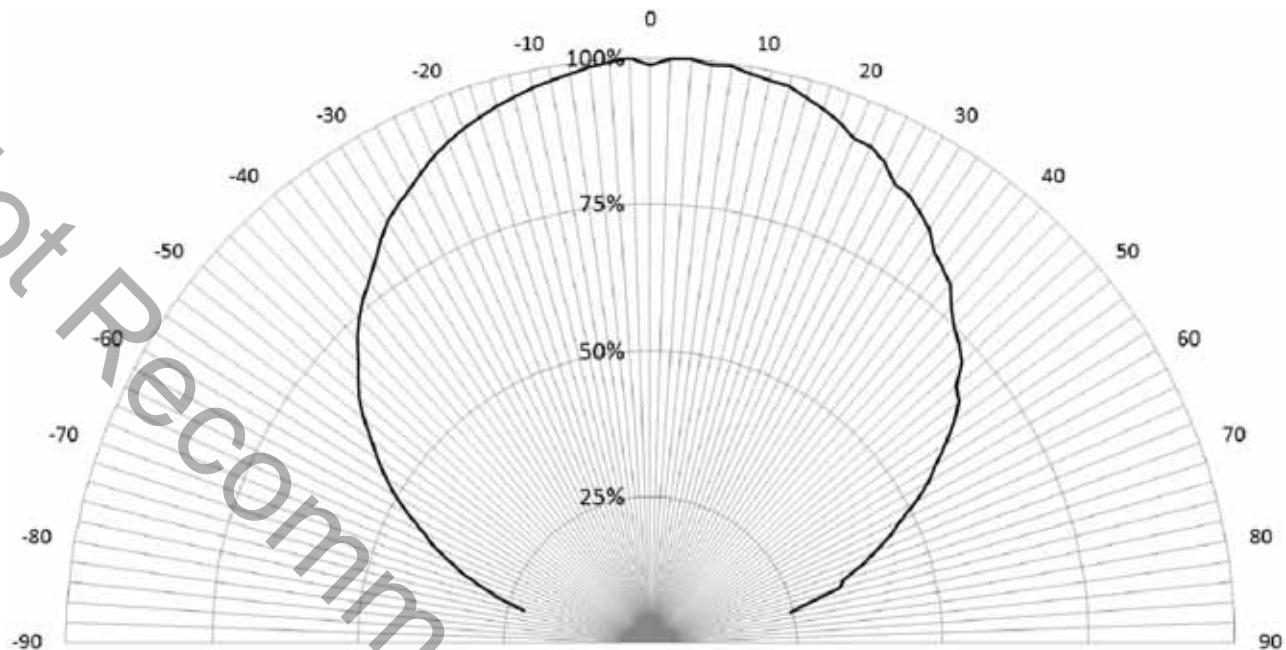


Figure 5. View angle, large photodiode rotated around the pin-5/pin-10 ("vertical") axis

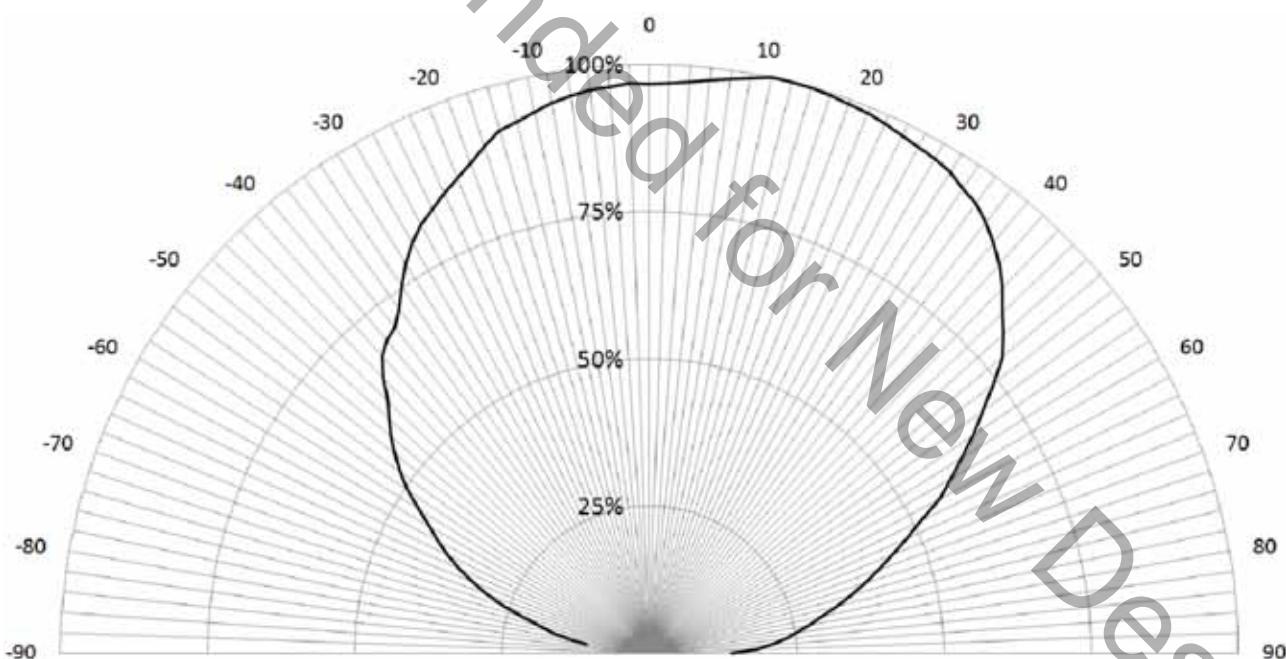


Figure 6. View angle, large photodiode rotated around "horizontal" axis and small photodiode rotated around either axis

## 2. Functional Description

### 2.1. Introduction

The Si1141/42/43 is an active optical reflectance proximity detector and ambient light sensor whose operational state is controlled through registers accessible through the I<sup>2</sup>C interface. The host can command the Si1141/42/43 to initiate on-demand proximity detection or ambient light sensing. The host can also place the Si1141/42/43 in an autonomous operational state where it performs measurements at set intervals and interrupts the host either after each measurement is completed or whenever a set threshold has been crossed. This results in an overall system power saving allowing the host controller to operate longer in its sleep state instead of polling the Si1141/42/43. For more details, refer to "AN498: Si114x Designer's Guide".

### 2.2. Proximity Sensing (PS)

The Si1141/42/43 has been optimized for use as either a dual-port or single-port active reflection proximity detector. Over distances of less than 50 cm, the dual-port active reflection proximity detector has significant advantages over single-port, motion-based infrared systems, which are only good for triggered events. Motion-based infrared detectors identify objects within proximity, but only if they are moving. Single-port motion-based infrared systems are ambiguous about stationary objects even if they are within the proximity field. The Si1141/42/43 can reliably detect an object entering or exiting a specified proximity field, even if the object is not moving or is moving very slowly. However, beyond about 30–50 cm, even with good optical isolation, single-port signal processing may be required due to static reflections from nearby objects, such as table tops, walls, etc. If motion detection is acceptable, the Si1141/42/43 can achieve ranges of up to 50 cm, through a single product window.

For small objects, the drop in reflectance is as much as the fourth power of the distance. This means that there is less range ambiguity than with passive motion-based devices. For example, a sixteenfold change in an object's reflectance means only a fifty-percent drop in detection range.

The Si1143 can drive three separate infrared LEDs. When the three infrared LEDs are placed in an L-shaped configuration, it is possible to triangulate an object within the three-dimensional proximity field. Thus, a touchless user interface can be implemented with the aid of host software.

The Si1141/42/43 can initiate proximity sense measurements when explicitly commanded by the host or periodically through an autonomous process. Refer to "3. Operational Modes" on page 17 for additional details of the Si1141/42/43's Operational Modes.

Whenever it is time to make a PS measurement, the Si1141/42/43 makes up to three measurements, depending on what is enabled in the CHLIST parameter. Other ADC parameters for these measurements can also be modified to allow proper operation under different ambient light conditions.

The LED choice is programmable for each of these three measurements. By default, each measurement turns on a single LED driver. However, the order of measurements can be easily reversed or even have all LEDs turned on at the same time. Optionally, each proximity measurement can be compared against a host-programmable threshold. With threshold settings for each PS channel, it is also possible for the Si1141/42/43 to notify the host whenever the threshold has been crossed. This reduces the number of interrupts to the host, aiding in efficient software algorithms.

The Si1141/42/43 can also generate an interrupt after a complete set of proximity measurements, ignoring any threshold settings.

To support different power usage cases dynamically, the infrared LED current of each output is independently programmable. The current can be programmed anywhere from a few to several hundred millamps. Therefore, the host can optimize for proximity detection performance or for power saving dynamically. This feature can be useful since it allows the host to reduce the LED current once an object has entered a proximity sphere, and the object can still be tracked at a lower current setting. Finally, the flexible current settings make it possible to control the infrared LED currents with a controlled current sink, resulting in higher precision.

The ADC properties are programmable. For indoor operation, the ADC should be configured for low signal range for best reflectance sensitivity. When under high ambient conditions, the ADC should be configured for high signal level range operation.

When operating in the lower signal range, it is possible to saturate the ADC when the ambient light level is high. Any overflow condition is reported in the RESPONSE register, and the corresponding data registers report a value of 0xFFFF. The host can then adjust the ADC sensitivity. Note however that the overflow condition is not sticky. If the light levels return to a range within the capabilities of the ADC, the corresponding data registers begin to operate normally. However, the RESPONSE register will continue to hold the overflow condition until a NOP command is received. Even if the RESPONSE register has an overflow condition, commands are still accepted and processed.

Proximity detection ranges beyond 50 cm and up to several meters can be achieved without lensing by selecting a longer integration time. The detection range may be increased further, even with high ambient light, by averaging multiple measurements. Refer to "AN498: Si114x Designer's Guide" for more details.

### 2.3. Ambient Light

The Si1141/42/43 has photodiodes capable of measuring both visible and infrared light. However, the visible photodiode is also influenced by infrared light. The measurement of illuminance requires the same spectral response as the human eye. If an accurate lux measurement is desired, the extra IR response of the visible-light photodiode must be compensated. Therefore, to allow the host to make corrections to the infrared light's influence, the Si1141/42/43 reports the infrared light measurement on a separate channel. The separate visible and IR photodiodes lend themselves to a variety of algorithmic solutions. The host can then take these two measurements and run an algorithm to derive an equivalent lux level as perceived by a human eye. Having the IR correction algorithm running in the host allows for the most flexibility in adjusting for system-dependent variables. For example, if the glass used in the system blocks visible light more than infrared light, the IR correction needs to be adjusted.

If the host is not making any infrared corrections, the infrared measurement can be turned off in the CHLIST parameter.

By default, the measurement parameters are optimized for indoor ambient light levels where it is possible to detect light levels as low as 6 lx. For operation under direct sunlight, the ADC can be programmed to operate in a high signal operation so that it is possible to measure direct sunlight without overflowing the 16-bit result.

For low-light applications, it is possible to increase the ADC integration time. Normally, the integration time is 25.6  $\mu$ s. By increasing this integration time to 410  $\mu$ s, the ADC can detect light levels as low as 1 lx. The ADC can be programmed with an integration time as high as 3.28 ms, allowing measurement to 100 mlx light levels. The ADC integration time for the Visible Light Ambient measurement can be programmed independently of the ADC integration time of the Infrared Light Ambient measurement. The independent ADC parameters allow operation under glass covers having a higher transmittance to Infrared Light than Visible Light.

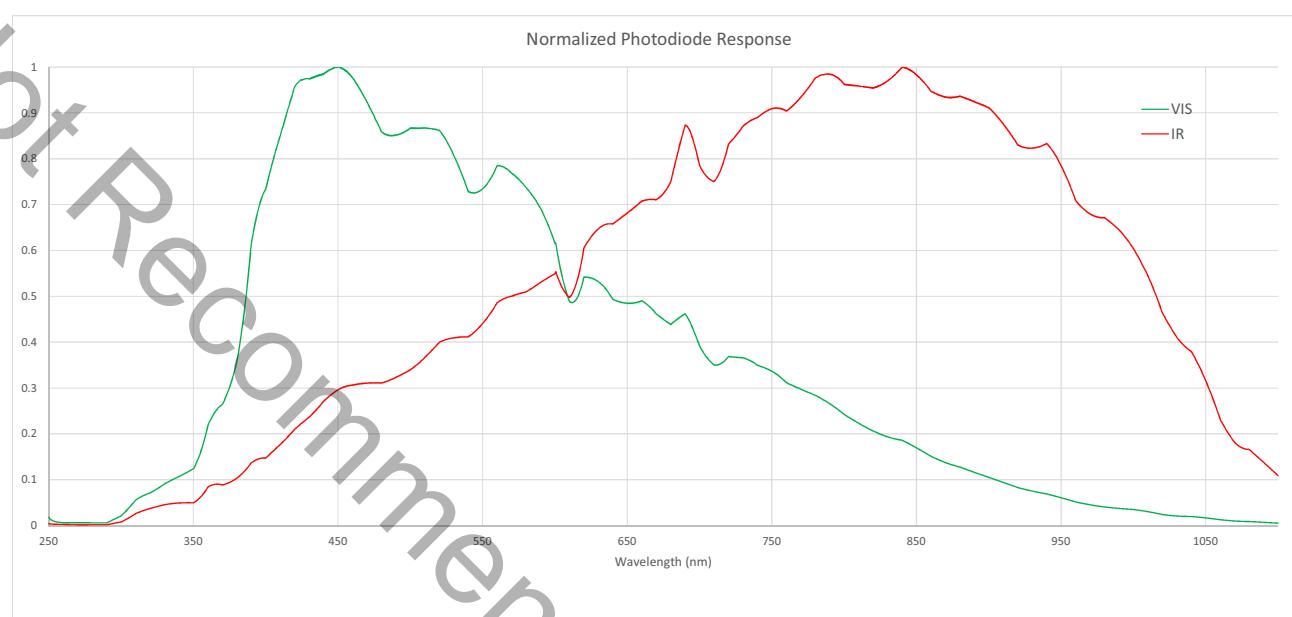
When operating in the lower signal range, or when the integration time is increased, it is possible to saturate the ADC when the ambient light suddenly increases. Any overflow condition is reported in the RESPONSE register, and the corresponding data registers report a value of 0xFFFF. Based on either of these two overflow indicators, the host can adjust the ADC sensitivity. However, the overflow condition is not sticky. If the light levels return to a range within the capabilities of the ADC, the corresponding data registers begin to operate normally. The RESPONSE register will continue to hold the overflow condition until a NOP command is received. Even if the RESPONSE register has an overflow condition, commands are still accepted and processed.

The Si1141/42/43 can initiate ALS measurements either when explicitly commanded by the host or periodically through an autonomous process. Refer to "3. Operational Modes" on page 17 for additional details of the Si1141/42/43's Operational Modes. The conversion frequency setting is programmable and independent of the Proximity Sensor. This allows the Proximity Sensor and Ambient Light sensor to operate at different conversion rates, increasing host control over the Si1141/42/43.

When operating autonomously, the ALS has a slightly different interrupt structure compared to the Proximity Sensor. An interrupt can be generated to the host on every sample, or when the ambient light has changed.

The "Ambient Light Changed" interrupt is accomplished through two thresholds working together to implement a window. As long as the ambient light stays within the window defined by the two thresholds, the host is not interrupted. When the ambient light changes and either threshold is crossed, an interrupt is sent to the host, thereby allowing the host notification that the ambient light has changed. This can be used by the host to trigger a recalculation of the lux values.

The window can be applied to either the Visible Ambient Measurement, or the Infrared Ambient Measurement, but not both. However, monitoring the ambient change in either channel should allow notification that the ambient light level has changed.



**Figure 7. Photodiode Spectral Response to Visible and Infrared Light (Indicative)**

## 2.4. Host Interface

The host interface to the Si1141/42/43 consists of three pins:

- SCL
- SDA
- INT

SCL and SDA are standard open-drain pins as required for I<sup>2</sup>C operation.

The Si1141/42/43 asserts the INT pin to interrupt the host processor. Right after internal power on reset, the INT pin is an input and should be driven to a high level. After that, the INT pin becomes an open-drain output.

A pull-up resistor to VDD is recommended for proper operation. The I<sup>2</sup>C/INT pins may be connected to VIO in systems. E.g., when Si114x is in OFF-mode, an I<sup>2</sup>C bus for other devices might need to be active. In this case, INT pins (via VIO through pull-up register) must be higher than 0.7xVDD within 20  $\mu$ s of VDD going above 1.6 V. During OFF-mode, total current on I<sup>2</sup>C/INT pins should be lower than 100 mA (600-500 mA). Refer to Table 4, "Absolute Maximum Limits," on page 9.

As an open-drain output, the INT pin can be shared with other open-drain interrupt sources in the system. If there is a possibility that other open-drain sources drive low around power on reset period, contact to Silicon Labs for details.

For proper operation, the Si1141/42/43 is expected to fully complete its Initialization Mode prior to any activity on the I<sup>2</sup>C.

The INT, SCL, and SDA pins are designed so that it is possible for the Si1141/42/43 to enter the Off Mode by software command without interfering with normal operation of other I<sup>2</sup>C devices on the bus.

The Si1141/42/43 I<sup>2</sup>C slave address is 0x5A. The Si1141/42/43 also responds to the global address (0x00) and the global reset command (0x06). Only 7-bit I<sup>2</sup>C addressing is supported; 10-bit I<sup>2</sup>C addressing is not supported.

Conceptually, the I<sup>2</sup>C interface allows access to the Si1141/42/43 internal registers. Table 15 on page 30 is a summary of these registers.

An I<sup>2</sup>C write access always begins with a start (or restart) condition. The first byte after the start condition is the I<sup>2</sup>C address and a read-write bit. The second byte specifies the starting address of the Si1141/42/43 internal register. Subsequent bytes are written to the Si1141/42/43 internal register sequentially until a stop condition is encountered. An I<sup>2</sup>C write access with only two bytes is typically used to set up the Si1141/42/43 internal address in preparation for an I<sup>2</sup>C read.

The I<sup>2</sup>C read access, like the I<sup>2</sup>C write access, begins with a start or restart condition. In an I<sup>2</sup>C read, the I<sup>2</sup>C master then continues to clock SCK to allow the Si1141/42/43 to drive the I<sup>2</sup>C with the internal register contents.

The Si1141/42/43 also supports burst reads and burst writes. The burst read is useful in collecting contiguous, sequential registers. The Si1141/42/43 register map was designed to optimize for burst reads for interrupt handlers, and the burst writes are designed to facilitate rapid programming of commonly used fields, such as thresholds registers.

The internal register address is a six-bit (bit 5 to bit 0) plus an Autoincrement Disable (on bit 6). The Autoincrement Disable is turned off by default. Disabling the autoincrementing feature allows the host to poll any single internal register repeatedly without having to keep updating the Si1141/42/43 internal address every time the register is read.

It is recommended that the host should read PS or ALS measurements (in the I<sup>2</sup>C Register Map) when the Si1141/42/43 asserts INT. Although the host can read any of the Si1141/42/43's I<sup>2</sup>C registers at any time, care must be taken when reading 2-byte measurements outside the context of an interrupt handler. The host could be reading part of the 2-byte measurement when the internal sequencer is updating that same measurement coincidentally. When this happens, the host could be reading a hybrid 2-byte quantity whose high byte and low byte are parts of different samples. If the host must read these 2-byte registers outside the context of an interrupt handler, the host should "double-check" a measurement if the measurement deviates significantly from a previous reading.

**I<sup>2</sup>C Broadcast Reset:** The I<sup>2</sup>C Broadcast Reset should be sent prior to any I<sup>2</sup>C register access to the Si114x. If any I<sup>2</sup>C register or parameter has already been written to the Si114x when the I<sup>2</sup>C Broadcast Reset is issued, the host must send a reset command and reinitialize the Si114x completely.

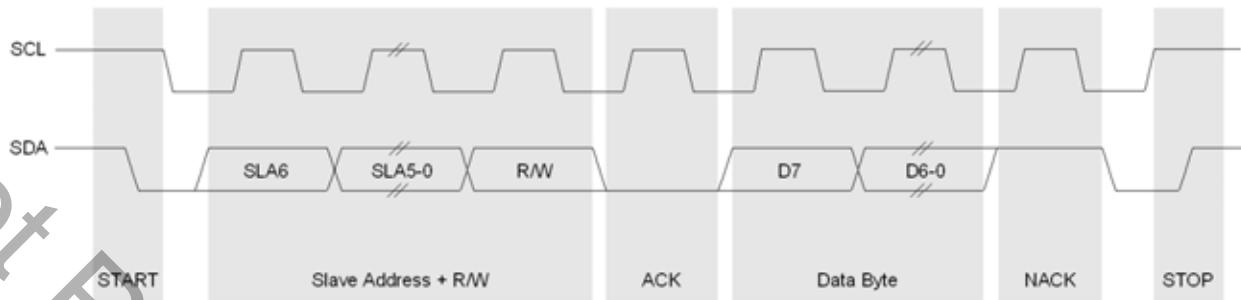


Figure 8. I<sup>2</sup>C Bit Timing Diagram



Figure 9. Host Interface Single Write

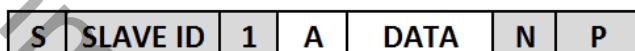


Figure 10. Host Interface Single Read

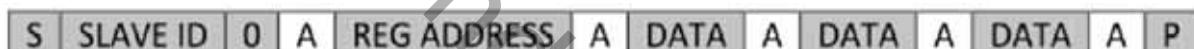


Figure 11. Host Interface Burst Write



Figure 12. Host Interface Burst Read

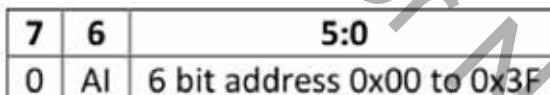


Figure 13. Si1141/42/43 REG ADDRESS Format

**Notes:**

- Gray boxes are driven by the host to the Si1141/42/43
- White boxes are driven by the Si1141/42/43 to the host
- A = ACK or “acknowledge”
- N = NACK or “no acknowledge”
- S = START condition
- Sr = repeat START condition
- P = STOP condition
- AI = Disable Auto Increment when set

### 3. Operational Modes

The Si1141/42/43 can be in one of many operational modes at any one time. It is important to consider the operational mode since the mode has an impact on the overall power consumption of the Si1141/42/43. The various modes are:

- Off Mode
- Initialization Mode
- Standby Mode
- Forced Conversion Mode
- Autonomous Mode

#### 3.1. Off Mode

The Si1141/42/43 is in the Off Mode when  $V_{DD}$  is either not connected to a power supply or if the  $V_{DD}$  voltage is below the stated  $VDD\_OFF$  voltage described in the electrical specifications. As long as the parameters stated in Table 4, "Absolute Maximum Limits," on page 9 are not violated, no current will flow through the Si1141/42/43. In the Off Mode, the Si1141/42/43 SCL and SDA pins do not interfere with other I<sup>2</sup>C devices on the bus. The LED pins will not draw current through the infrared diodes. Keeping  $V_{DD}$  less than  $VDD\_OFF$  is not intended as a method of achieving lowest system current draw. The reason is that the ESD protection devices on the SCL, SDA and INT pins also form a current path through  $V_{DD}$ . If  $V_{DD}$  is grounded for example, then, current flow from system power to system ground through the SCL, SDA and INT pull-up resistors and the ESD protection devices.

Allowing  $V_{DD}$  to be less than  $VDD\_OFF$  is intended to serve as a hardware method of resetting the Si1141/42/43 without a dedicated reset pin.

The Si1141/42/43 can also reenter the Off Mode upon receipt of either a general I<sup>2</sup>C reset or if a software reset sequence is initiated. When one of these software methods is used to enter the Off Mode, the Si1141/42/43 typically proceeds directly from the Off Mode to the Initialization Mode.

#### 3.2. Initialization Mode

When power is applied to  $V_{DD}$  and is greater than the minimum  $V_{DD}$  Supply Voltage stated in Table 1, "Recommended Operating Conditions," on page 4, the Si1141/42/43 enters its Initialization Mode. In the Initialization Mode, the Si1141/42/43 performs its initial startup sequence. Since the I<sup>2</sup>C may not yet be active, it is recommended that no I<sup>2</sup>C activity occur during this brief Initialization Mode period. The "Start-up time" specification in Table 1 is the minimum recommended time the host needs to wait before sending any I<sup>2</sup>C accesses following a power-up sequence. After Initialization Mode has completed, the Si1141/42/43 enters Standby Mode. The host must write 0x17 to the HW\_KEY register for proper operation.

#### 3.3. Standby Mode

The Si1141/42/43 spends most of its time in Standby Mode. After the Si1141/42/43 completes the Initialization Mode sequence, it enters Standby mode. While in Standby Mode, the Si1141/42/43 does not perform any Ambient Light measurements or Proximity Detection functions. However, the I<sup>2</sup>C interface is active and ready to accept reads and writes to the Si1141/42/43 registers. The internal Digital Sequence Controller is in its sleep state and does not draw much power. In addition, the INT output retains its state until it is cleared by the host.

I<sup>2</sup>C accesses do not necessarily cause the Si1141/42/43 to exit the Standby Mode. For example, reading Si1141/42/43 registers is accomplished without needing the Digital Sequence Controller to wake from its sleep state.

#### 3.4. Forced Conversion Mode

The Si1141/42/43 can operate in Forced Conversion Mode under the specific command of the host processor. The Forced Conversion Mode is entered if either the ALS\_FORCE or the PS\_FORCE command is sent. Upon completion of the conversion, the Si1141/42/43 can generate an interrupt to the host if the corresponding interrupt is enabled. It is possible to initiate both an ALS and multiple PS measurements with one command register write access by using the PSALS\_FORCE command.

## 3.5. Autonomous Operation Mode

The Si1141/42/43 can be placed in the Autonomous Operation Mode where measurements are performed automatically without requiring an explicit host command for every measurement. The PS\_AUTO, ALS\_AUTO and PSALS\_AUTO commands are used to place the Si1141/42/43 in the Autonomous Operation Mode.

The Si1141/42/43 updates the I<sup>2</sup>C registers for PS and ALS automatically. Each measurement is allocated a 16-bit register in the I<sup>2</sup>C map. It is possible to operate the Si1141/42/43 without interrupts. When doing so, the host poll rate must be at least twice the frequency of the conversion rates for the host to always receive a new measurement. The host can also choose to be notified when these new measurements are available by enabling interrupts.

The conversion frequencies for the PS and ALS measurements are set up by the host prior to the PS\_AUTO, ALS\_AUTO, or PSALS\_AUTO commands. The host can set a PS conversion frequency different from the ALS conversion frequency. However, they both need to be a multiple of the base conversion frequency in the MEAS\_RATE register in the I<sup>2</sup>C map.

The Si1141/42/43 can interrupt the host when the PS or ALS measurements reach a pre-set threshold. To assist in the handling of interrupts the registers are arranged so that the interrupt handler can perform an I<sup>2</sup>C burst read operation to read the necessary registers, beginning with the interrupt status register, and cycle through the ALS data registers followed by the individual Proximity readings.

## 3.6. ALWAYS\_ACTIVE Mode

In autonomous measurements mode, the device enters sleep mode during the measurement interval. If the device is configured as ALWAYS\_ACTIVE, the device does not enter sleep mode. This mode is added as a workaround to the “unexpected internal reset issue”. Details on this issue are described in Section “3.7. Avoiding an Unexpected Reset” of this document.

To enter ALWAYS\_ACTIVE mode, set Parameter 0x1B = 0x01 before enabling autonomous measurements. Setting Parameter 0x1B = 0x81 returns the device in “Normal Mode”. A side effect of this setting is that total power consumption will be higher due to ALWAYS\_ACTIVE

## 3.7. Avoiding an Unexpected Reset

If an internal wakeup event is generated less than 250  $\mu$ sec after entering sleep mode, the Si114x may generate an internal reset that returns the chip to a default state. This unexpected reset issue will not occur if an application code follows the information provided in this data sheet and summarized here.

The Si114x has only two wakeup sources:

- MEAS\_RATE timer in autonomous mode
- I<sup>2</sup>C write to 0x18(COMMAND register).

Examples of problem setups include:

- An interval shorter than 250  $\mu$ sec (MEAS\_RATE < 0x24) in autonomous mode with PS only.
- An interval shorter than “250  $\mu$ sec + ALS/VIS/IR measurement (active) period” in autonomous mode with PS+ALS/VIS/IR.
- An I<sup>2</sup>C write to 0x18 (COMMAND) received right after entering sleep mode

This issue is avoided by using ALWAYS\_ACTIVE mode because you never enter sleep mode. Set Parameter 0x1B to 0x01 (ALWAYS\_ACTIVE mode) before enabling autonomous measurements. A side effect of this setting is that total power consumption will be higher due to ALWAYS\_ACTIVE mode. This issue is avoided in Normal Mode by preventing wakeup events from being triggered immediately upon entering sleep state. Some points to consider are:

1. Follow minimum MEASRATE restriction in table.
2. Prior to sending an I<sup>2</sup>C Command, check that prior commands have completed:
  - Check if CHIPSTAT == 0x01 as implemented in sample code, or
  - Check RESPONSE counter increment as documented here

3. Use the following procedure to exit autonomous operation

- a. Write MEASRATE=0x00 to stop autonomous measurements
- b. Wait two complete measurement periods. For example, if INT pin pulses are observed every 750  $\mu$ s, the waiting period would be 1500  $\mu$ s. The measurement period must be determined by checking the INT pin pulses on the oscilloscope or by using system timers to time the arrival of incoming samples in the interrupt handler.
- c. When using forced measurements, after sending the Force command, don't send any other I<sup>2</sup>C commands until after measurements have been retrieved. (Forced measurements are completed when INT pin asserts or when IRQSTATUS is non-zero).

## 4. Programming Guide

### 4.1. Command and Response Structure

All Si1141/42/43 I<sup>2</sup>C registers (except writes to the COMMAND register) are read or written without waking up the internal sequencer. A complete list of the I<sup>2</sup>C registers can be found in "4.6. I<sup>2</sup>C Registers" on page 30. In addition to the I<sup>2</sup>C Registers, RAM parameters are memory locations maintained by the internal sequencer. These RAM Parameters are accessible through a Command Protocol (see "4.7. Parameter RAM" on page 54). A complete list of the RAM Parameters can be found in "4.7. Parameter RAM" on page 54.

The Si1141/42/43 can operate either in Forced Measurement or Autonomous Mode. When in Forced Measurement mode, the Si1141/42/43 does not make any measurements unless the host specifically requests the Si1141/42/43 to do so via specific commands (refer to the Section 3.2). The CHLIST parameter needs to be written so that the Si1141/42/43 would know which measurements to make. The parameter MEAS\_RATE, when zero, places the internal sequencer in Forced Measurement mode. When in Forced Measurement mode, the internal sequencer wakes up only when the host writes to the COMMAND register. The power consumption is lowest in Forced Measurement mode (MEAS\_RATE = 0).

The Si1141/42/43 operates in Autonomous Operation mode when MEAS\_RATE is non-zero. The MEAS\_RATE represents the time interval at which the Si1141/42/43 wakes up periodically. Once the internal sequencer has awoken, the sequencer manages an internal PS Counter and ALS Counter based on the PS\_RATE and ALS\_RATE registers.

When the internal PS counter has expired, up to three proximity measurements are made (PS1, PS2 and PS3) depending on which measurements are enabled via the upper bits of the CHLIST Parameter. All three PS measurements are performed, in sequence, beginning with the PS1 measurement channel. In the same way, when the ALS counter has expired, up to three measurements are made (ALS\_VIS, ALS\_IR and AUX) depending on which measurements are enabled via the upper bits of the CHLIST Parameter. All three measurements are made in the following sequence: ALS\_VIS, ALS\_IR and AUX.

PS\_RATE and ALS\_RATE are normally non-zero. A value of zero in PS\_RATE or ALS\_RATE causes the internal sequencer to never perform that measurement group. Typically, PS\_RATE or ALS\_RATE represents a value of one. A value of one essentially states that the specific measurement group is made every time the device wakes up.

It is possible for both the PS Counter and ALS Counter to both expire at the same time. When that occurs, the PS measurements are performed before the ALS measurements. When all measurements have been made, the internal sequencer goes back to sleep until next time, as dictated by the MEAS\_RATE parameter.

The operation of the Si1141/42/43 can be described as two measurement groups bound by some common factors. The PS Measurement group consists of the three PS measurements while the ALS Measurement group consists of the Visible Light Ambient Measurement (ALS\_VIS), the Infrared Light Ambient Measurement (ALS\_IR) and the Auxiliary measurement (AUX). Each measurement group has three measurements each. The Channel List (CHLIST) parameter enables the specific measurements for that measurement grouping.

Each measurement (PS1, PS2, PS3, ALS\_VIS, ALS\_IR, AUX) are controlled through a combination of I<sup>2</sup>C Register or Parameter RAM. Tables 7 to 9 below summarize the properties and resources used for each measurement.

## 4.2. Command Protocol

The I<sup>2</sup>C map implements a bidirectional message box between the host and the Si1141/42/43 Sequencer. Host-writable I<sup>2</sup>C registers facilitate host-to-Si1141/42/43 communication, while read-only I<sup>2</sup>C registers are used for Si1141/42/43-to-host communication.

Unlike the other host-writable I<sup>2</sup>C registers, the COMMAND register causes the internal sequencer to wake up from Standby mode to process the host request.

When a command is executed, the RESPONSE register is updated. Typically, when there is no error, the upper four bits are zeroes. To allow command tracking, the lower four bits implement a 4-bit circular counter. In general, if the upper nibble of the RESPONSE register is non-zero, this indicates an error or the need for special processing.

The PARAM\_WR and PARAM\_RD registers are additional mailbox registers.

In addition to the registers in the I<sup>2</sup>C map, there are environmental parameters accessible through the Command/Response interface. These parameters are stored in the internal ram space. These parameters generally take more I<sup>2</sup>C accesses to read and write. The Parameter RAM is described in "4.7. Parameter RAM" on page 54.

For every write to the Command register, the following sequence is required:

1. Write 0x00 to Command register to clear the Response register.
2. Read Response register and verify contents are 0x00.
3. Write Command value from Table 5 into Command register.
4. Read the Response register and verify contents are now non-zero. If contents are still 0x00, repeat this step.

**Note:** Step 4 is not applicable to the Reset Command because the device will reset itself and does not increment the Response register after reset. No Commands should be issued to the device for at least 1 ms after a Reset is issued.

The Response register will be incremented upon the successful completion of a Command. If the Response register remains 0x00 for over 25 ms after the Command write, the entire Command process should be repeated from Step 1.

**Table 5. Command Register Summary**

| COMMAND Register |           | PARAM_W<br>R Register | PARAM_RD<br>Register | Error Code in<br>RESPONSE Register | Description  |
|------------------|-----------|-----------------------|----------------------|------------------------------------|--|
| Name             | Encoding  |                       |                      |                                    |  |
| PARAM_QUERY      | 100 aaaaa | —                     | nnnn nnnn            | ✓                                  | Reads the parameter pointed to by bitfield [4:0] and writes value to PARAM_RD. See Table 16 for parameters.                                      |
| PARAM_SET        | 101 aaaaa | dddd<br>dddd          | nnnn nnnn            | ✓                                  | Sets parameter pointed by bitfield [4:0] with value in PARAM_WR, and writes value out to PARAM_RD. See Table 16 for parameters.                  |
| PARAM_AND        | 110 aaaaa | dddd<br>dddd          | nnnn nnnn            | ✓                                  | Performs a bit-wise AND between PARAM_WR and Parameter pointed by bitfield [4:0], writes updated value to PARAM_RD. See Table 16 for parameters. |

Table 5. Command Register Summary (Continued)

| COMMAND Register |           | PARAM_W<br>R Register | PARAM_RD<br>Register | Error Code in<br>RESPONSE Register | Description  |
|------------------|-----------|-----------------------|----------------------|------------------------------------|--|
| Name             | Encoding  |                       |                      |                                    |  |
| PARAM_OR         | 111 aaaaa | dddd dddd             | nnnn nnnn            | ✓                                  | Performs a bit-wise OR of PARAM_WR and parameter pointed by bitfield [4:0], writes updated value to PARAM_RD. See Table 16 for parameters. |
| NOP              | 000 00000 | —                     | —                    | ✓                                  | Forces a zero into the RESPONSE register   |
| RESET            | 000 00001 | —                     | —                    | ✓                                  | Performs a software reset of the firmware  |
| BUSADDR          | 000 00010 | —                     | —                    | —                                  | Modifies I <sup>2</sup> C address  |
| Reserved         | 000 00011 | —                     | —                    | —                                  | —  |
| Reserved         | 000 00100 | —                     | —                    | —                                  | —  |
| PS_FORCE         | 000 00101 | —                     | —                    | ✓                                  | Forces a single PS measurement   |
| ALS_FORCE        | 000 00110 | —                     | —                    | ✓                                  | Forces a single ALS measurement  |
| PSALS_FORCE      | 000 00111 | —                     | —                    | ✓                                  | Forces a single PS and ALS measurement   |
| Reserved         | 000 01000 | —                     | —                    | —                                  | —  |
| PS_PAUSE         | 000 01001 | —                     | —                    | ✓                                  | Pauses autonomous PS   |
| ALS_PAUSE        | 000 01010 | —                     | —                    | ✓                                  | Pauses autonomous ALS  |
| PSALS_PAUSE      | 000 01011 | —                     | —                    | ✓                                  | Pauses PS and ALS  |
| Reserved         | 000 01100 | —                     | —                    | ✓                                  | —  |
| PS_AUTO          | 000 01101 | —                     | —                    | ✓                                  | Starts/Restarts an autonomous PS Loop  |
| ALS_AUTO         | 000 01110 | —                     | —                    | ✓                                  | Starts/Restarts an autonomous ALS Loop   |
| PSALS_AUTO       | 000 01111 | —                     | —                    | ✓                                  | Starts/Restarts autonomous ALS and PS loop   |
| Reserved         | 000 1xxxx | —                     | —                    | —                                  | —  |

**Table 6. Response Register Error Codes**

| RESPONSE Register | Description  |
|-------------------|--|
| 0000 cccc         | NO_ERROR. The lower bit is a circular counter and is incremented every time a command has completed. This allows the host to keep track of commands sent to the Si1141/42/43. The circular counter may be cleared using the NOP command. |
| 1000 0000         | INVALID_SETTING. An invalid setting was encountered. Clear using the NOP command.  |
| 1000 1000         | PS1_ADC_OVERFLOW. Indicates proximity channel one conversion overflow.   |
| 1000 1001         | PS2_ADC_OVERFLOW. Indicates proximity channel two conversion overflow.   |
| 1000 1010         | PS3_ADC_OVERFLOW. Indicates proximity channel three conversion overflow.   |
| 1000 1100         | ALS_VIS_ADC_OVERFLOW. Indicates visible ambient light channel conversion overflow.   |
| 1000 1101         | ALS_IR_ADC_OVERFLOW. Indicates infrared ambient light channel conversion overflow.   |
| 1000 1110         | AUX_ADC_OVERFLOW. Indicates auxiliary channel conversion overflow.   |

#### 4.3. Command Write Timing Limitations

Commands should not be sent immediately after the Si114x enters sleep mode. Consider the following scenarios:

- Prior to sending any I<sup>2</sup>C commands, the software needs to check that prior commands have been completed. The software will verify that the CHIPSTAT == 0x01, as implemented in sample code, or the RESPONSE counter increment, as documented in the data sheet and application note.
- Use the following procedure to exit autonomous operation instead of a PAUSE command (any commands including PAUSE should not be addressed during autonomous operation):
  - Write MEASRATE = 0x00 to stop autonomous measurements
  - Wait two complete measurement periods (for example, if INT pin pulses are observed every 750 µs, the waiting period would be 1500 µs). The measurement period must be determined by checking the INT pin pulses on the oscilloscope or by using system timers to time the arrival of incoming samples in the interrupt handler.
- When using Forced measurements, do not send any other I<sup>2</sup>C commands until after the measurements have been retrieved. Forced measurements are completed when the INT pin asserts or when IRQSTATUS becomes non-zero.

## 4.4. Resource Summary

Table 7. Resource Summary for Interrupts and Threshold Checking

| Measurement Channel   | Channel Enable           | Interrupt Status Output         | Interrupt Enable                | Interrupt Mode                | Threshold Registers              | Threshold Hysteresis | History Checking | Autonomous Measurement Time Base |               |
|-----------------------|--------------------------|---------------------------------|---------------------------------|-------------------------------|----------------------------------|----------------------|------------------|----------------------------------|---------------|
| Proximity Sense 1     | EN_PS 1 in CHLIST [0]    | PS1_INT in IRQ_STATUS[2]        | PS1_IE in IRQ_EN-ABLE[2]        | PS1_IM[1:0] in IRQ_MODE1[5:4] | PS1_TH[7:0]                      | PS_HYST[7:0]         | PS_HISTORY[7:0]  | MEAS_RATE[7:0]                   | PS_RATE[7:0]  |
| Proximity Sense 2     | EN_PS 2 in CHLIST [1]    | PS2_INT in IRQ_STATUS[3]        | PS2_IE in IRQ_EN-ABLE[3]        | PS2_IM[1:0] in IRQ_MODE1[7:6] | PS2_TH[7:0]                      |                      |                  |                                  |               |
| Proximity Sense 3     | EN_PS 3 in CHLIST [2]    | PS3_INT in IRQ_STATUS[4]        | PS3_EN in IRQ_EN-ABLE[4]        | PS3_IM[1:0] in IRQ_MODE2[1:0] | PS3_TH[7:0]                      |                      |                  |                                  |               |
| ALS Visible           | EN_ALS_VIS in CHLIST [4] | ALS_INT[1:0] in IRQ_STATUS[1:0] | ALS_IE[1:0] in IRQ_EN-ABLE[1:0] | ALS_IM[2:0] in IRQ_MODE1[2:0] | ALS_LOW_TH[7:0] / ALS_HI_TH[7:0] | ALS_HYST[7:0]        | ALS_HISTORY[7:0] | ALS_RATE[7:0]                    | ALS_RATE[7:0] |
| ALS IR                | EN_ALS_IR in CHLIST [5]  |                                 |                                 |                               |                                  |                      |                  |                                  |               |
| Auxiliary Measurement | EN_AU_X in CHLIST [6]    | —                               | —                               | —                             | —                                | —                    | —                | —                                | —             |

Table 8. Resource Summary for LED Choice and ADC Parameters

| Measurement Channel   | LED Selection                       | ADC Mode                      | ADC Output                              | ADC Input Source                         | ADC Recovery Count                 | ADC High Signal Mode       | ADC Clock Divider                 | ADC Alignment                     | ADC Offset       |
|-----------------------|-------------------------------------|-------------------------------|---|--|------------------------------------|----------------------------|-----------------------------------|-----------------------------------|------------------|
| Proximity Sense 1     | PS1_LED[2:0] in PSLED12_SELECT[2:0] | PS_ADC_MODE in PS_ADC_MISC[2] | PS1_DA-TA1[7:0] / PS1_DA-TA0[7:0]       | PS1_ADC-MUX[7:0]                         | PS_ADC_REC in PS_ADC_COUNTER [6:4] | PS_RANGE in PS_ADC_MISC[5] | PS_AD-C_GAIN[3:0]                 | PS1_ALIGN in PS_EN-CODING[4]      | ADC_OFFSET [7:0] |
| Proximity Sense 2     | PS2_LED[2:0] in PSLED12_SELECT[6:4] |                               | PS2_DA-TA1[7:0] / PS2_DA-TA0[7:0]       | PS2_ADC-MUX[7:0]                         |                                    |                            |                                   | PS2_ALIGN in PS_EN-CODING[5]      |                  |
| Proximity Sense 3     | PS3_LED[2:0] in PSLED3_SELECT[2:0]  |                               | PS3_DA-TA1[7:0] / PS3_DA-TA0[7:0]       | PS3_ADC-MUX[7:0]                         |                                    |                            |                                   | PS3_ALIGN in PS_EN-CODING[6]      |                  |
| ALS Visible           | —                                   | —                             | ALS_VIS_DATA1 / ALS_VIS_DATA0           | VIS_ADC_REC in ALS_VIS_ADC_COUNTER [6:4] | VIS_RANGE in ALS_VIS_ADC_MISC[5]   | ALS_VIS_ADC_GAIN[3:0]      | ALS_VIS_ALIGN in ALS_EN-CODING[4] | ALS_VIS_ALIGN in ALS_EN-CODING[4] | ALS_OFFSET [7:0] |
| ALS IR                | —                                   |                               | ALS_IR_DA-TA1[7:0] / ALS_IR_DA-TA0[7:0] |  |                                    |                            |                                   |                                   |                  |
| Auxiliary Measurement | —                                   |                               | AUX_DA-TA1[7:0] / AUX_DA-TA0[7:0]       | AUX_ADC-MUX[7:0]                         | —                                  | —                          | —                                 | —                                 |                  |

**Table 9. Resource Summary for Hardware Pins**

| Pin Name | LED Current Drive      | Output Drive Disable | Analog Voltage Input Enable |
|----------|------------------------|----------------------|-----------------------------|
| LED1     | LED1_I in PSLED12[3:0] |                      | ANA_IN_KEY[31:0]            |
| LED2     | LED2_I in PSLED12[7:4] | HW_KEY[7:0]          | ANA_IN_KEY[31:0]            |
| LED3     | LED3_I in PSLED3[3:0]  | HW_KEY[7:0]          |                             |
| INT      |                        | INT_OE in INT_CFG[0] | ANA_IN_KEY[31:0]            |

The interrupts of the Si1141/42/43 are controlled through the INT\_CFG, IRQ\_ENABLE, IRQ\_MODE1, IRQ\_MODE2 and IRQ\_STATUS registers.

The INT hardware pin is enabled through the INT\_OE bit in the INT\_CFG register. The hardware essentially performs an AND function between the IRQ\_ENABLE register and IRQ\_STATUS register. After this AND function, if any bits are set, the INT pin is asserted. The INT\_MODE bit in the INT\_CFG register is conceptually a method of determining how the INT pin is deasserted. When INT\_MODE = 0, the host is responsible for clearing the interrupt by writing to the IRQ\_STATUS register. When the specific bits of the IRQ\_STATUS register is written with '1', that specific IRQ\_STATUS bit is cleared.

Typically, the host software is expected to read the IRQ\_STATUS register, stores a local copy, and then writes the same value back to the IRQ\_STATUS to clear the interrupt source. Unless specifically stated, INT\_MODE should be zero for normal interrupt handling operation. In summary, the INT\_CFG register is normally written with '1'.

The IRQ\_MODE1, IRQ\_MODE2 and IRQ\_ENABLE registers work together to define how the internal sequencer sets bits in the IRQ\_STATUS register (and as a consequence, asserting the INT pin).

The PS1 interrupts are described in Table 10. The PS2 interrupts are described in Table 11. The PS3 interrupts are described in Table 12. The ALS interrupts are described in Table 13, and the Command Interface interrupts are described in Table 14.

Table 10. PS1 Channel Interrupt Resources

| IRQ_ENABLE[2] | IRQ_MODE1[5:4] | Description |   |
|---------------|----------------|-------------|---|
| PS1_IE        | PS1_IM[1:0]    |             |   |
| 0             | 0              | 0           | No PS1 Interrupts   |
| 1             | 0              | 0           | PS1_INT set after every PS1 sample                              |
| 1             | 0              | 1           | PS1_INT set whenever PS1 threshold (PS1_TH) is crossed          |
| 1             | 1              | 1           | PS1_INT set whenever PS1 sample is above PS1 threshold (PS1_TH) |

**Note:** There is hysteresis applied (PS\_HYST) and history checking (PS\_HISTORY). PS\_HYST is encoded in 8-bit compressed format. In the Si114x, PS1\_TH is also encoded in compressed format.

Table 11. PS2 Channel Interrupt Resources

| IRQ_ENABLE[3] | IRQ_MODE1[7:6] | Description |   |
|---------------|----------------|-------------|---|
| PS2_IE        | PS2_IM[1:0]    |             |   |
| 0             | 0              | 0           | No PS2 Interrupts   |
| 1             | 0              | 0           | PS2_INT set after every PS2 sample                          |
| 1             | 0              | 1           | PS2_INT set whenever PS2 threshold (PS2_TH) is crossed      |
| 1             | 1              | 1           | PS2_INT set when PS2 sample is above PS2 threshold (PS2_TH) |

**Note:** There is hysteresis applied (PS\_HYST) and history checking (PS\_HISTORY). PS\_HYST is encoded in 8-bit compressed format. In the Si114x, PS2\_TH is also encoded in compressed format.

Table 12. PS3 Channel Interrupt Resources

| IRQ_ENABLE[4] | IRQ_MODE2[1:0] | Description |   |
|---------------|----------------|-------------|---|
| PS3_IE        | PS3_IM[1:0]    |             |   |
| 0             | 0              | 0           | No PS3 Interrupts   |
| 1             | 0              | 0           | PS3_INT set after every PS3 sample                              |
| 1             | 0              | 1           | PS3_INT set whenever PS3 threshold (PS3_TH) is crossed          |
| 1             | 1              | 1           | PS3_INT set whenever PS3 sample is above PS3 threshold (PS3_TH) |

**Note:** There is hysteresis applied (PS\_HYST) and history checking (PS\_HISTORY). PS\_HYST is encoded in 8-bit compressed format. In the Si114x, PS3\_TH is also encoded in compressed format.

Table 13. Ambient Light Sensing Interrupt Resources

| IRQ_ENABLE[1:0] |   | IRQ_MODE1[2:0] |   |   | Description   |
|-----------------|---|----------------|---|---|---|
| ALS_IE[1:0]     |   | ALS_IM[2:0]    |   |   |   |
| 0               | 0 | 0              | 0 | 0 | No ALS Interrupts   |
| 0               | 1 | 0              | 0 | 0 | ALS_INT [0] set after every ALS_VIS sample <sup>1</sup>   |
| x               | 1 | x              | 0 | 1 | Monitors ALS_VIS, ALS_INT [0] upon exiting region between low and high thresholds (ALS_LOW_TH and ALS_HI_TH)      |
| 1               | x | 1              | 0 | x | Monitors ALS_VIS, ALS_INT [1] set upon entering region between low and high thresholds (ALS_LOW_TH and ALS_HI_TH) |
| x               | 1 | x              | 1 | 1 | Monitors ALS_IR, ALS_INT [0] set upon exiting region between low and high thresholds (ALS_LOW_TH and ALS_HI_TH)   |
| 1               | x | 1              | 1 | x | Monitors ALS_IR, ALS_INT [1] set upon entering region between low and high thresholds (ALS_LOW_TH and ALS_HI_TH)  |

**Notes:**

1. For ALS\_IR channel, interrupts per sample is not possible without also enabling ALS\_VIS
2. All other combinations are invalid and may result in unintended operation
3. There is hysteresis applied (ALS\_TH) and history checking (ALS\_HISTORY). ALS\_HYST is encoded in 8-bit compressed format.
4. In the Si114x, ALS\_LOW\_TH and ALS\_HI\_TH are also encoded in compressed format.

Table 14. Command Interrupt Resources

| IRQ_ENABLE[5] |  | IRQ_MODE2[3:2] |   | Description  |
|---------------|--|----------------|---|--|
| CMD_IE        |  | CMD_IM[1:0]    |   |  |
| 0             |  | x              | 0 | No CMD Interrupts                                      |
| 1             |  | x              | 0 | CMD_INT set when there is a new RESPONSE               |
| 1             |  | x              | 1 | CMD_INT set when there is a new error code in RESPONSE |

## 4.5. Signal Path Software Model

The following diagram gives an overview of the signal paths, along with the I<sup>2</sup>C register and RAM Parameter bit fields that control them. Sections with detailed descriptions of the I<sup>2</sup>C registers and Parameter RAM follow.

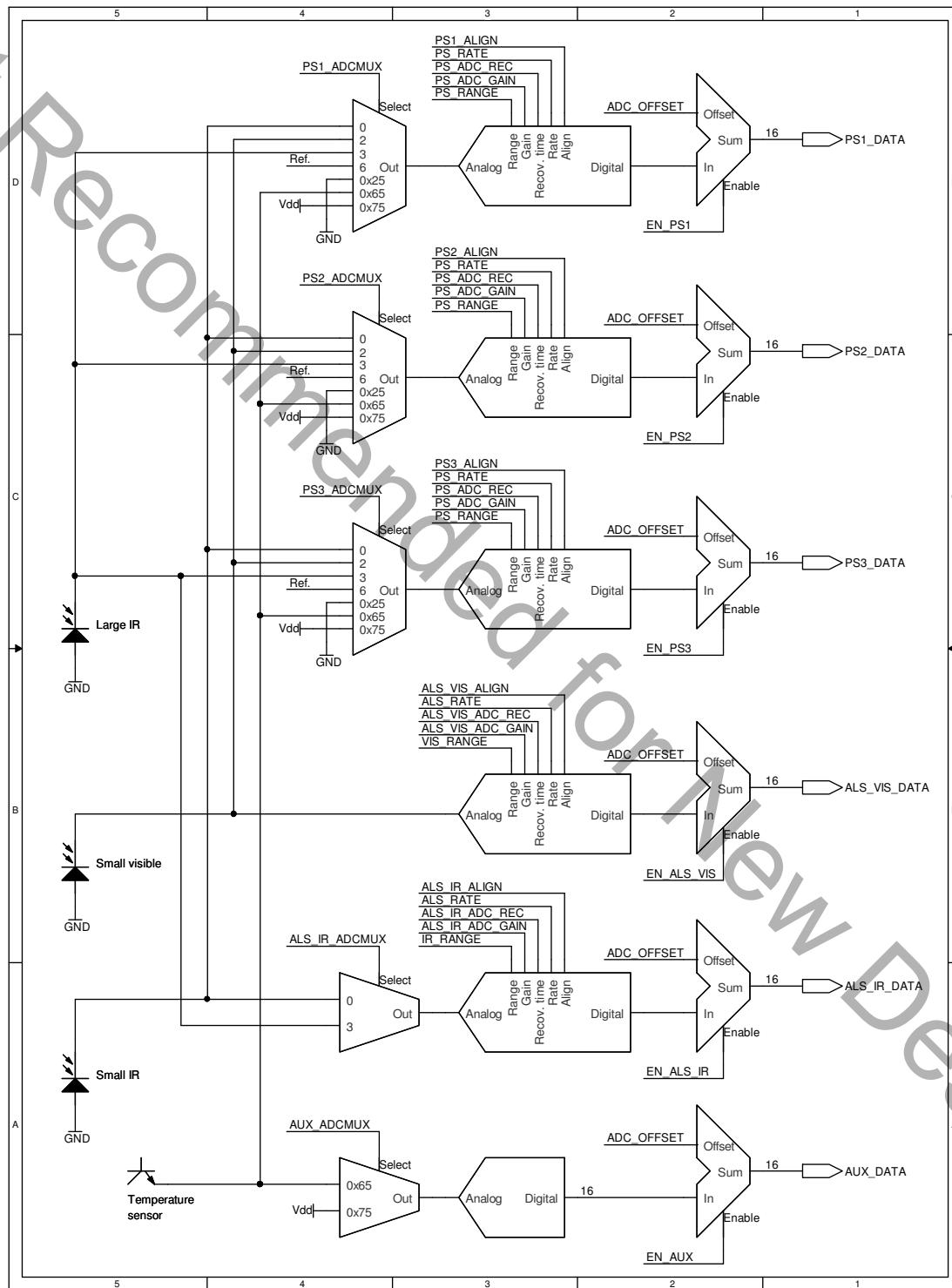


Figure 14. Signal Path Programming Model

## 4.6. I<sup>2</sup>C Registers

Table 15. I<sup>2</sup>C Register Summary

| I <sup>2</sup> C Register Name | Address | 7           | 6 | 5      | 4      | 3      | 2      | 1        | 0      |  |  |  |  |  |  |
|--------------------------------|---------|-------------|---|--------|--------|--------|--------|----------|--------|--|--|--|--|--|--|
| PART_ID                        | 0x00    | PART_ID     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| REV_ID                         | 0x01    | REV_ID      |   |        |        |        |        |          |        |  |  |  |  |  |  |
| SEQ_ID                         | 0x02    | SEQ_ID      |   |        |        |        |        |          |        |  |  |  |  |  |  |
| INT_CFG                        | 0x03    |             |   |        |        |        |        | INT_MODE | INT_OE |  |  |  |  |  |  |
| IRQ_ENABLE                     | 0x04    |             |   | CMD_IE | PS3_IE | PS2_IE | PS1_IE | ALS_IE   |        |  |  |  |  |  |  |
| IRQ_MODE1                      | 0x05    | PS2_IM      |   | PS1_IM |        | ALS_IM |        |          |        |  |  |  |  |  |  |
| IRQ_MODE2                      | 0x06    |             |   |        |        | CMD_IM |        | PS3_IM   |        |  |  |  |  |  |  |
| HW_KEY                         | 0x07    | HW_KEY      |   |        |        |        |        |          |        |  |  |  |  |  |  |
| MEAS_RATE                      | 0x08    | MEAS_RATE   |   |        |        |        |        |          |        |  |  |  |  |  |  |
| ALS_RATE                       | 0x09    | ALS_RATE    |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS_RATE                        | 0x0A    | PS_RATE     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| ALS_LOW_TH0                    | 0x0B    | ALS_LOW_TH0 |   |        |        |        |        |          |        |  |  |  |  |  |  |
| ALS_LOW_TH1                    | 0x0C    | ALS_LOW_TH1 |   |        |        |        |        |          |        |  |  |  |  |  |  |
| ALS_HI_TH0                     | 0x0D    | ALS_HI_TH0  |   |        |        |        |        |          |        |  |  |  |  |  |  |
| ALS_HI_TH1                     | 0x0E    | ALS_HI_TH1  |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS_LED21                       | 0x0F    | LED2_I      |   |        |        | LED1_I |        |          |        |  |  |  |  |  |  |
| PS_LED3                        | 0x10    |             |   |        |        | LED3_I |        |          |        |  |  |  |  |  |  |
| PS1_TH0                        | 0x11    | PS1_TH0     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS1_TH1                        | 0x12    | PS1_TH1     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS2_TH0                        | 0x13    | PS2_TH0     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS2_TH1                        | 0x14    | PS2_TH1     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS3_TH0                        | 0x15    | PS3_TH0     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PS3_TH1                        | 0x16    | PS3_TH1     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| PARAM_WR                       | 0x17    | PARAM_WR    |   |        |        |        |        |          |        |  |  |  |  |  |  |
| COMMAND                        | 0x18    | COMMAND     |   |        |        |        |        |          |        |  |  |  |  |  |  |
| RESPONSE                       | 0x20    | RESPONSE    |   |        |        |        |        |          |        |  |  |  |  |  |  |

Table 15. I<sup>2</sup>C Register Summary (Continued)

| I <sup>2</sup> C Register Name | Address   | 7 | 6 | 5        | 4             | 3        | 2        | 1        | 0     |
|--------------------------------|-----------|---|---|----------|---------------|----------|----------|----------|-------|
| IRQ_STATUS                     | 0x21      |   |   | CMD_IN_T | PS3_IN_T      | PS2_IN_T | PS1_IN_T | ALS_INT  |       |
| ALS_VIS_DATA0                  | 0x22      |   |   |          | ALS_VIS_DATA0 |          |          |          |       |
| ALS_VIS_DATA1                  | 0x23      |   |   |          | ALS_VIS_DATA1 |          |          |          |       |
| ALS_IR_DATA0                   | 0x24      |   |   |          | ALS_IR_DATA0  |          |          |          |       |
| ALS_IR_DATA1                   | 0x25      |   |   |          | ALS_IR_DATA1  |          |          |          |       |
| PS1_DATA0                      | 0x26      |   |   |          | PS1_DATA0     |          |          |          |       |
| PS1_DATA1                      | 0x27      |   |   |          | PS1_DATA1     |          |          |          |       |
| PS2_DATA0                      | 0x28      |   |   |          | PS2_DATA0     |          |          |          |       |
| PS2_DATA1                      | 0x29      |   |   |          | PS2_DATA1     |          |          |          |       |
| PS3_DATA0                      | 0x2A      |   |   |          | PS3_DATA0     |          |          |          |       |
| PS3_DATA1                      | 0x2B      |   |   |          | PS3_DATA1     |          |          |          |       |
| AUX_DATA0                      | 0x2C      |   |   |          | AUX_DATA0     |          |          |          |       |
| AUX_DATA1                      | 0x2D      |   |   |          | AUX_DATA1     |          |          |          |       |
| PARAM_RD                       | 0x2E      |   |   |          | PARAM_RD      |          |          |          |       |
| CHIP_STAT                      | 0x30      |   |   |          |               |          | RUN-NING | SUS-PEND | SLEEP |
| ANA_IN_KEY                     | 0x3B–0x3E |   |   |          | ANA_IN_KEY    |          |          |          |       |

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## PART\_ID @ 0x00

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| Bit         | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------|---|---|---|---|---|---|---|
| <b>Name</b> | PART_ID |   |   |   |   |   |   |   |
| <b>Type</b> | R       |   |   |   |   |   |   |   |

Reset value = 0100 0001 (Si1141)

Reset value = 0100 0010 (Si1142)

Reset value = 0100 0011 (Si1143)

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## REV\_ID @ 0x1

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| Bit         | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------|---|---|---|---|---|---|---|
| <b>Name</b> | REV_ID |   |   |   |   |   |   |   |
| <b>Type</b> | R      |   |   |   |   |   |   |   |

Reset value = 0000 0000

---

## SEQ\_ID @ 0x02

---

| Bit         | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------|---|---|---|---|---|---|---|
| <b>Name</b> | SEQ_ID |   |   |   |   |   |   |   |
| <b>Type</b> | R      |   |   |   |   |   |   |   |

Reset value = 0000 1000

| Bit | Name   | Function   |
|-----|--------|--|
| 7:0 | SEQ_ID | <b>Sequencer Revision.</b><br>0x01 Si114x-A01 (MAJOR_SEQ = 0, MINOR_SEQ = 1)<br>0x02 Si114x-A02 (MAJOR_SEQ = 0, MINOR_SEQ = 2)<br>0x03 Si114x-A03 (MAJOR_SEQ = 0, MINOR_SEQ = 3)<br>0x08 Si114x-A10 (MAJOR_SEQ = 1, MINOR_SEQ = 0)<br>0x09 Si114x-A11 (MAJOR_SEQ = 1, MINOR_SEQ = 1) |

## INT\_CFG @ 0x03

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1        | 0      |
|------|---|---|---|---|---|---|----------|--------|
| Name |   |   |   |   |   |   | INT_MODE | INT_OE |
| Type |   |   |   |   |   |   | RW       | RW     |

Reset value = 0000 0000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:2 | Reserved | <b>Reserved.</b>  |
| 1   | INT_MODE | <p><b>Interrupt Mode.</b></p> <p>The INT_MODE describes how the bits in the IRQ_STATUS Registers are cleared.</p> <p>0: The IRQ_STATUS Register bits are set by the internal sequencer and are sticky. It is the host's responsibility to clear the interrupt status bits in the IRQ_STATUS register to clear the interrupt.</p> <p>1: If the Parameter Field PSx_IM = 11, the internal sequencer clears the INT pin automatically.</p> |
| 0   | INT_OE   | <p><b>INT Output Enable.</b></p> <p>INT_OE controls the INT pin drive</p> <p>0: INT pin is never driven</p> <p>1: INT pin driven low whenever an IRQ_STATUS and its corresponding IRQ_ENABLE bits match</p>   |

## IRQ\_ENABLE @ 0x04

| Bit  | 7 | 6 | 5      | 4      | 3      | 2      | 1      | 0 |
|------|---|---|--------|--------|--------|--------|--------|---|
| Name |   |   | CMD_IE | PS3_IE | PS2_IE | PS1_IE | ALS_IE |   |
| Type |   |   | RW     | RW     | RW     | RW     | RW     |   |

Reset value = 0000 0000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:6 | Reserved | <b>Reserved.</b>  |
| 5   | CMD_IE   | <b>Command Interrupt Enable.</b><br>Enables interrupts based on COMMAND/RESPONSE activity.<br>0: INT never asserts due to COMMAND/RESPONSE interface activity.<br>1: Assert INT pin whenever CMD_INT is set by the internal sequencer.  |
| 4   | PS3_IE   | <b>PS3 Interrupt Enable.</b><br>Enables interrupts based on PS3 Channel Activity.<br>0: INT never asserts due to PS3 Channel activity.<br>1: Assert INT pin whenever PS3_INT is set by the internal sequencer.  |
| 3   | PS2_IE   | <b>PS2 Interrupt Enable.</b><br>Enables interrupts based on PS2 Channel Activity.<br>0: INT never asserts due to PS2 Channel activity.<br>1: Assert INT pin whenever PS2_INT is set by the internal sequencer.  |
| 2   | PS1_IE   | <b>PS1 Interrupt Enable.</b><br>Enables interrupts based on PS1 Channel Activity.<br>0: INT never asserts due to PS1 Channel activity.<br>1: Assert INT pin whenever PS1_INT is set by the internal sequencer.  |
| 1:0 | ALS_IE   | <b>ALS Interrupt Enable.</b><br>Enables interrupts based on ALS Activity.<br>00: INT never asserts due to ALS activity.<br>1x: Assert INT pin whenever ALS_INT[1] bit is set by the internal sequencer.<br>x1: Assert INT pin whenever ALS_INT[0] is set by the internal sequencer. |

## IRQ\_MODE1 @ 0x05

| Bit  | 7      | 6 | 5      | 4 | 3  | 2      | 1 | 0 |
|------|--------|---|--------|---|----|--------|---|---|
| Name | PS2_IM |   | PS1_IM |   |    | ALS_IM |   |   |
| Type | RW     |   | RW     |   | RW |        |   |   |

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:6 | PS2_IM   | PS2 Interrupt Mode applies only when PS2_IE is also set.<br>00: PS2_INT is set whenever a PS2 measurement has completed.<br>01: PS2_INT is set whenever the current PS2 measurement crosses the PS2_TH threshold.<br>11: PS2_INT is set whenever the current PS2 measurement is greater than the PS2_TH threshold.   |
| 5:4 | PS1_IM   | PS1 Interrupt Mode applies only when PS1_IE is also set.<br>00: PS1_INT is set whenever a PS1 measurement has completed.<br>01: PS1_INT is set whenever the current PS1 measurement crosses the PS1_TH threshold.<br>11: PS1_INT is set whenever the current PS1 measurement is greater than the PS1_TH threshold.   |
| 3   | Reserved | <b>Reserved.</b>   |
| 2:0 | ALS_IM   | ALS Interrupt Mode function is defined in conjunction with ALS_IE[1:0].<br>ALS_IE[1:0] / ALS_IM[2:0]:<br>00 / 000: Neither ALS_INT[1] nor ALS_INT[0] is ever set.<br>01 / 000: ALS_INT[0] sets after every ALS_VIS sample.<br>x1 / x01: Monitors ALS_VIS channel, ALS_INT[0] asserts if measurement exits window between ALS_LOW_TH and ALS_HIGH_TH.<br>x1 / x11: Monitors ALS_IR channel, ALS_INT[0] asserts if measurement exits window between ALS_LOW_TH and ALS_HIGH_TH.<br>1x / 10x: Monitors ALS_VIS channel, ALS_INT[1] asserts if measurement enters window between ALS_LOW_TH and ALS_HIGH_TH.<br>1x / 11x: Monitors ALS_IR channel, ALS_INT[1] asserts if measurement enters window between ALS_LOW_TH and ALS_HIGH_TH. |

Note: The ALS\_IM description applies only to sequencer revisions A03 or later.

## IRQ\_MODE2 @ 0x06

| Bit  | 7 | 6 | 5 | 4 | 3      | 2 | 1      | 0 |
|------|---|---|---|---|--------|---|--------|---|
| Name |   |   |   |   | CMD_IM |   | PS3_IM |   |
| Type |   |   |   |   | RW     |   | RW     |   |

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:4 | Reserved | <b>Reserved.</b>   |
| 3:2 | CMD_IM   | Command Interrupt Mode applies only when CMD_IE is also set.<br>00: CMD_INT is set whenever the RESPONSE register is written.<br>01: CMD_INT is set whenever the RESPONSE register is written with an error code (MSB set).<br>1x: Reserved.   |
| 1:0 | PS3_IM   | PS3 Interrupt Mode applies only when PS3_IE is also set.<br>00: PS3_INT is set whenever a PS3 measurement has completed.<br>01: PS3_INT is set whenever the current PS3 measurement crosses the PS3_TH threshold.<br>11: PS3_INT is set whenever the current PS3 measurement is greater than the PS3_TH threshold. |

## HW\_KEY @ 0x07

| Bit  | 7 | 6 | 5 | 4      | 3 | 2 | 1 | 0 |
|------|---|---|---|--------|---|---|---|---|
| Name |   |   |   | HW_KEY |   |   |   |   |
| Type |   |   |   | RW     |   |   |   |   |

Reset value = 0000 0000

| Bit | Name   | Function   |
|-----|--------|--|
| 7:0 | HW_KEY | The system must write the value 0x17 to this register for proper Si114x operation. |

**MEAS\_RATE @ 0x08**

| Bit  | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|---|---|---|---|---|---|---|
| Name | MEAS_RATE |   |   |   |   |   |   |   |
| Type | RW        |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name | Function |
|-----|------|----------|
|     |      |          |

| 7:0                                    | MEAS_RATE       | <p>MEAS_RATE is an 8-bit compressed value representing a 16-bit integer. The duration time between wake-up periods where measurements are made are calculated by the following steps.</p> <ol style="list-style-type: none"><li>1. A = decompress from 8-bit to 16-bit (as in application note, "AN498: Si114x Designer's Guide").</li><li>2. B = INT( (A-1)/2 )</li><li>3. Meas Rate(<math>\mu</math>s) = (B+2.5) * 62.5 <math>\mu</math>s</li></ol> <p>Calculation examples:</p> <p>0x84: The device wakes up every approx. 10 ms<br/>0x94: The device wakes up every approx. 20 ms<br/>0xB9: The device wakes up every approx. 100 ms<br/>0xDF: The device wakes up every approx. 496 ms<br/>0xFF: The device wakes up every approx. 1.984 seconds</p> <p>When either ALS_VIS or ALS_IR are enabled, the MEASRATE should be limited according to the following table:</p> <table border="1"><thead><tr><th>Larger of (VIS_ADC_GAIN or IR_ADCGAIN)</th><th>MEASRATE to Use</th></tr></thead><tbody><tr><td>0</td><td><math>\geq 0x38</math></td></tr><tr><td>1</td><td><math>\geq 0x3E</math></td></tr><tr><td>2</td><td><math>\geq 0x46</math></td></tr><tr><td>3</td><td><math>\geq 0x51</math></td></tr><tr><td>4</td><td><math>\geq 0x5E</math></td></tr><tr><td>5</td><td><math>\geq 0x6C</math></td></tr><tr><td>6</td><td><math>\geq 0x7B</math></td></tr><tr><td>7</td><td><math>\geq 0x8A</math></td></tr></tbody></table> <p>Additional Information:</p> <ul style="list-style-type: none"><li>■ 0x00: Turns off any internal oscillator and disables autonomous measurement. Use this setting to achieve lowest <math>V_{DD}</math> current draw for systems making use of only forced measurements.</li><li>■ 0x01-0x23: These values are not allowed when PS only or no ALS_VIS or no ALS_IR.</li><li>■ 0x18-0x23: These values can be used in ALWAYS_ACTIVE mode.</li></ul> | Larger of (VIS_ADC_GAIN or IR_ADCGAIN) | MEASRATE to Use | 0 | $\geq 0x38$ | 1 | $\geq 0x3E$ | 2 | $\geq 0x46$ | 3 | $\geq 0x51$ | 4 | $\geq 0x5E$ | 5 | $\geq 0x6C$ | 6 | $\geq 0x7B$ | 7 | $\geq 0x8A$ |
|--|-----------------|---|--|-----------------|---|-------------|---|-------------|---|-------------|---|-------------|---|-------------|---|-------------|---|-------------|---|-------------|
| Larger of (VIS_ADC_GAIN or IR_ADCGAIN) | MEASRATE to Use |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 0                                      | $\geq 0x38$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 1                                      | $\geq 0x3E$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 2                                      | $\geq 0x46$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 3                                      | $\geq 0x51$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 4                                      | $\geq 0x5E$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 5                                      | $\geq 0x6C$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 6                                      | $\geq 0x7B$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |
| 7                                      | $\geq 0x8A$     |   |  |                 |   |             |   |             |   |             |   |             |   |             |   |             |   |             |   |             |

**ALS\_RATE @ 0x09**

| Bit         | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|---|---|---|---|---|---|---|
| <b>Name</b> | ALS_RATE |   |   |   |   |   |   |   |
| <b>Type</b> | RW       |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:0 | ALS_RATE | <p>ALS_RATE is an 8-bit compressed value representing a 16-bit multiplier. This multiplier, in conjunction with the MEAS_RATE time, represents how often ALS Measurements are made. For a given ALS measurement period, MEAS_RATE should be as high as possible and ALS_RATE as low as possible in order to optimize power consumption.</p> <p>Example Values:</p> <ul style="list-style-type: none"> <li>0x00: Autonomous ALS Measurements are not made.</li> <li>0x08: ALS Measurements made every time the device wakes up.<br/>(<math>0x0001 \times \text{timeValueOf(MEAS\_RATE)}</math>)</li> <li>0x32: ALS Measurements made every 10 times the device wakes up.<br/>(<math>0x000A \times \text{timeValueOf(MEAS\_RATE)}</math>)</li> <li>0x69: ALS Measurements made every 100 times the device wakes up.<br/>(<math>0x0064 \times \text{timeValueOf(MEAS\_RATE)}</math>)</li> </ul> <p>Please refer to "AN498: Si114x Designer's Guide", Section 5.4 "Compression Concept."</p> |

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## PS\_RATE @ 0x0A

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| Bit  | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------|---|---|---|---|---|---|---|
| Name | PS_RATE |   |   |   |   |   |   |   |
| Type | RW      |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name    | Function   |
|-----|---------|--|
| 7:0 | PS_RATE | <p>PS_RATE is an 8-bit compressed value representing a 16-bit multiplier. This multiplier, in conjunction with the MEAS_RATE time, represents how often PS Measurements are made. For a given proximity measurement period, MEAS_RATE should be as high as possible and PS_RATE as low as possible in order to optimize power consumption.</p> <p>Example Values:</p> <ul style="list-style-type: none"><li>0x00: Autonomous PS Measurements are not made</li><li>0x08: PS Measurements made every time the device wakes up<br/>(0x0001 x timeValueOf(MEAS_RATE))</li><li>0x32: PS Measurements made every 10 times the device wakes up<br/>(0x000A x timeValueOf(MEAS_RATE))</li><li>0x69: PS Measurements made every 100 times the device wakes up<br/>(0x0064 x timeValueOf(MEAS_RATE))</li></ul> <p>Please refer to "AN498: Si114x Designer's Guide", Section 5.4 "Compression Concept."</p> |

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## ALS\_LOW\_TH0: ALS\_LOW\_TH Data Word Low Byte @ 0x0B

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| Bit  | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | ALS_LOW_TH[7:0] |   |   |   |   |   |   |   |
| Type | RW              |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name            | Function   |
|-----|-----------------|--|
| 7:0 | ALS_LOW_TH[7:0] | <p>ALS_LOW_TH is a 16-bit threshold value. When used in conjunction with ALS_HI_TH, it forms a window region applied to either ALS_VIS or ALS_IR measurements for interrupting the host. Once autonomous measurements have started, modification to ALS_LOW_TH should be preceded by an ALS_PAUSE or PSALS_PAUSE command. For revisions A10 and below, ALS_LOW_TH uses an 8-bit compressed format. Refer to "AN498: Si114x Designer's Guide", Section 5.4 "Compression Concept."</p> |

**ALS\_LOW\_TH1:ALS\_LOW\_TH Data Word High Byte @ 0x0C**

| Bit  | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|---|---|---|---|---|---|
| Name | ALS_LOW_TH[15:8] |   |   |   |   |   |   |   |
| Type | RW               |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name             | Function  |
|-----|------------------|---|
| 7:0 | ALS_LOW_TH[15:8] | ALS_LOW_TH is a 16-bit threshold value. When used in conjunction with ALS_HI_TH, it forms a window region applied to either ALS_VIS or ALS_IR measurements for interrupting the host. Once autonomous measurements have started, modification to ALS_LOW_TH should be preceded by an ALS_PAUSE or PSALS_PAUSE command. For revisions A10 and below, ALS_LOW_TH uses an 8-bit compressed format. Refer to "AN498: Si114x Designer's Guide", Section 5.4 "Compression Concept." |

**ALS\_HI\_TH0: ALS\_HI\_TH Data Word Low Byte @ 0x0D**

| Bit  | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | ALS_HI_TH[7:0] |   |   |   |   |   |   |   |
| Type | RW             |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name           | Function  |
|-----|----------------|---|
| 7:0 | ALS_HI_TH[7:0] | ALS_HI_TH is a 16-bit threshold value. When used in conjunction with ALS_LOW_TH, it forms a window region applied to either ALS_VIS or ALS_IR measurements for interrupting the host. Once autonomous measurements have started, modification to ALS_HI_TH should be preceded by an ALS_PAUSE or PSALS_PAUSE command. For revisions A10 and below, ALS_HI_TH uses an 8-bit compressed format. Refer to "AN498: Si114x Designer's Guide", Section 5.4 "Compression Concept." |

**Note:** This register available for sequencer revisions A03 or later.

## ALS\_HI\_TH1: ALS\_HI\_TH Data Word High Byte @ 0x0E

| Bit  | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | ALS_HI_TH[15:8] |   |   |   |   |   |   |   |
| Type | RW              |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit          | Name            | Function   |
|--------------|-----------------|--|
| 7:0          | ALS_HI_TH[15:8] | ALS_HI_TH is a 16-bit threshold value. When used in conjunction with ALS_LOW_TH, it forms a window region applied to either ALS_VIS or ALS_IR measurements for interrupting the host. Once autonomous measurements have started, modification to ALS_HI_TH should be preceded by an ALS_PAUSE or PSALS_PAUSE command. For revisions A10 and below, ALS_HI_TH uses an 8-bit compressed format. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |
| <b>Note:</b> |                 |  |

## PS\_LED21 @ 0x0F

| Bit  | 7      | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
|------|--------|---|---|---|--------|---|---|---|
| Name | LED2_I |   |   |   | LED1_I |   |   |   |
| Type | RW     |   |   |   |        |   |   |   |

Reset value = 0000 0000

| Bit | Name   | Function  |
|-----|--------|---|
| 7:4 | LED2_I | LED2_I Represents the irLED current sunk by the LED2 pin during a PS measurement. On the Si1141, these bits must be set to zero.  |
| 3:0 | LED1_I | LED1_I Represents the irLED current sunk by the LED1 pin during a PS measurement.<br><br>LED3_I, LED2_I, and LED1_I current encoded as follows:<br>0000: No current<br>0001: Minimum current<br>1111: Maximum current<br>Refer to Table 2, "Performance Characteristics <sup>1</sup> ," on page 4 for LED current values. |

## PS\_LED3 @ 0x10

| Bit  | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------|---|---|---|---|---|---|---|
| Name | LED3_I |   |   |   |   |   |   |   |
| Type | RW     |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:4 | Reserved | <b>Reserved.</b>   |
| 3:0 | LED3_I   | LED3_I Represents the irLED current sunk by the LED3 pin during a PS measurement. See PS_LED21 Register for additional details.<br>On the Si1141 and Si1142, these bits must be set to zero. |

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#### PS1\_TH0: PS1\_TH Data Word Low Byte @ 0x11

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|      |             |   |   |   |   |   |   |   |
|------|-------------|---|---|---|---|---|---|---|
| Bit  | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS1_TH[7:0] |   |   |   |   |   |   |   |
| Type | RW          |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name        | Function   |
|-----|-------------|--|
| 7:0 | PS1_TH[7:0] | PS1_TH is a 16-bit threshold value. It is compared to PS1 measurements during autonomous operation for interrupting the host. If the threshold register is updated while a measurement is in progress, it is possible that an invalid threshold will be applied if the first new threshold byte has been written and not the second. Remedies include ensuring no measurement during threshold updates and discarding measurements results immediately after threshold updates. Once autonomous measurements have started, modification to PS1_TH should be preceded by a PS_PAUSE or PSALS_PAUSE command. For Si114x revision A10 and below, PS1_TH uses an 8-bit compressed format at address 0x11. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |

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#### PS1\_TH1: PS1\_TH Data Word High Byte @ 0x12

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|      |              |   |   |   |   |   |   |   |
|------|--------------|---|---|---|---|---|---|---|
| Bit  | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS1_TH[15:8] |   |   |   |   |   |   |   |
| Type | RW           |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name         | Function   |
|-----|--------------|--|
| 7:0 | PS1_TH[15:8] | PS1_TH is a 16-bit threshold value. It is compared to PS1 measurements during autonomous operation for interrupting the host. If the threshold register is updated while a measurement is in progress, it is possible that an invalid threshold will be applied if the first new threshold byte has been written and not the second. Remedies include ensuring no measurement during threshold updates and discarding measurements results immediately after threshold updates. Once autonomous measurements have started, modification to PS1_TH should be preceded by a PS_PAUSE or PSALS_PAUSE command. For Si114x revision A10 and below, PS1_TH uses an 8-bit compressed format at address 0x11. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |

## PS2\_TH0: PS2\_TH Data Word Low Byte @ 0x13

|      |             |   |   |   |   |   |   |   |
|------|-------------|---|---|---|---|---|---|---|
| Bit  | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS2_TH[7:0] |   |   |   |   |   |   |   |
| Type | RW          |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name        | Function   |
|-----|-------------|--|
| 7:0 | PS2_TH[7:0] | PS2_TH is a 16-bit threshold value. It is compared to PS2 measurements during autonomous operation for interrupting the host. If the threshold register is updated while a measurement is in progress, it is possible that an invalid threshold will be applied if the first new threshold byte has been written and not the second. Remedies include ensuring no measurement during threshold updates and discarding measurements results immediately after threshold updates. Once autonomous measurements have started, modification to PS2_TH should be preceded by a PS_PAUSE or PSALS_PAUSE command. For Si114x revision A10 and below, PS2_TH uses an 8-bit compressed format at address 0x13. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |

## PS2\_TH1: PS2\_TH Data Word High Byte @ 0x14

|      |              |   |   |   |   |   |   |   |
|------|--------------|---|---|---|---|---|---|---|
| Bit  | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS2_TH[15:8] |   |   |   |   |   |   |   |
| Type | RW           |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name         | Function   |
|-----|--------------|--|
| 7:0 | PS2_TH[15:8] | PS2_TH is a 16-bit threshold value. It is compared to PS2 measurements during autonomous operation for interrupting the host. If the threshold register is updated while a measurement is in progress, it is possible that an invalid threshold will be applied if the first new threshold byte has been written and not the second. Remedies include ensuring no measurement during threshold updates and discarding measurements results immediately after threshold updates. Once autonomous measurements have started, modification to PS2_TH should be preceded by a PS_PAUSE or PSALS_PAUSE command. For Si114x revision A10 and below, PS2_TH uses an 8-bit compressed format at address 0x13. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |

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**PS3\_TH0: PS3\_TH Data Word Low Byte @ 0x15**


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| Bit         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| <b>Name</b> | PS3_TH[7:0] |   |   |   |   |   |   |   |
| <b>Type</b> | RW          |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name        | Function   |
|-----|-------------|--|
| 7:0 | PS3_TH[7:0] | PS3_TH is a 16-bit threshold value. It is compared to PS3 measurements during autonomous operation for interrupting the host. If the threshold register is updated while a measurement is in progress, it is possible that an invalid threshold will be applied if the first new threshold byte has been written and not the second. Remedies include ensuring no measurement during threshold updates and discarding measurements results immediately after threshold updates. Once autonomous measurements have started, modification to PS3_TH should be preceded by a PS_PAUSE or PSALS_PAUSE command. For Si114x revision A10 and below, PS3_TH uses an 8-bit compressed format at address 0x15. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |

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**PS3\_TH1: PS3\_TH Data Word High Byte @ 0x16**


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| Bit         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| <b>Name</b> | PS3_TH[15:8] |   |   |   |   |   |   |   |
| <b>Type</b> | RW           |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name         | Function   |
|-----|--------------|--|
| 7:0 | PS3_TH[15:8] | PS3_TH is a 16-bit threshold value. It is compared to PS3 measurements during autonomous operation for interrupting the host. If the threshold register is updated while a measurement is in progress, it is possible that an invalid threshold will be applied if the first new threshold byte has been written and not the second. Remedies include ensuring no measurement during threshold updates and discarding measurements results immediately after threshold updates. Once autonomous measurements have started, modification to PS3_TH should be preceded by a PS_PAUSE or PSALS_PAUSE command. For Si114x revision A10 and below, PS3_TH uses an 8-bit compressed format at address 0x15. Refer to "AN498: Si114x Designer's Guide" Section 5.4 "Compression Concept." |

## PARAM\_WR @ 0x17

| Bit  | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | PARAM_WR |   |   |   |   |   |   |   |
| Type | RW       |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:0 | PARAM_WR | Mailbox register for passing parameters from the host to the sequencer. |

## COMMAND @ 0x18

| Bit  | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------|---|---|---|---|---|---|---|
| Name | COMMAND |   |   |   |   |   |   |   |
| Type | RW      |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name    | Function  |
|-----|---------|---|
| 7:0 | COMMAND | <b>COMMAND Register.</b><br>The COMMAND Register is the primary mailbox register into the internal sequencer. Writing to the COMMAND register is the only I <sup>2</sup> C operation that wakes the device from standby mode. |

## RESPONSE @ 0x20

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
|     |   |   |   |   |   |   |   |   |

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RESPONSE @ 0x20

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|      |          |
|------|----------|
| Name | RESPONSE |
| Type | RW       |

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:0 | RESPONSE | <p>The Response register is used in conjunction with command processing. When an error is encountered, the response register will be loaded with an error code. All error codes will have the MSB is set.</p> <p>The error code is retained until a RESET or NOP command is received by the sequencer. Other commands other than RESET or NOP will be ignored. However, any autonomous operation in progress continues normal operation despite any error.</p> <p>0x00–0x0F: No Error. Bits 3:0 form an incrementing roll-over counter. The roll over counter in bit 3:0 increments when a command has been executed by the Si114x. Once autonomous measurements have started, the execution timing of any command becomes non-deterministic since a measurement could be in progress when the COMMAND register is written. The host software must make use of the rollover counter to ensure that commands are processed.</p> <p>0x80: Invalid Command Encountered during command processing</p> <p>0x88: ADC Overflow encountered during PS1 measurement</p> <p>0x89: ADC Overflow encountered during PS2 measurement</p> <p>0x8A: ADC Overflow encountered during PS3 measurement</p> <p>0x8C: ADC Overflow encountered during ALS-VIS measurement</p> <p>0x8D: ADC Overflow encountered during ALS-IR measurement</p> <p>0x8E: ADC Overflow encountered during AUX measurement</p> |

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IRQ\_STATUS @ 0x21

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| Bit  | 7 | 6 | 5       | 4       | 3       | 2       | 1 | 0       |
|------|---|---|---------|---------|---------|---------|---|---------|
| Name |   |   | CMD_INT | PS3_INT | PS2_INT | PS1_INT |   | ALS_INT |
| Type |   |   | RW      | RW      | RW      | RW      |   | RW      |

# Si1141/42/43

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:6 | Reserved | <b>Reserved.</b>   |
| 5   | CMD_INT  | <b>Command Interrupt Status.</b>                               |
| 4   | PS3_INT  | <b>PS3 Interrupt Status.</b>                                   |
| 3   | PS2_INT  | <b>PS3 Interrupt Status.</b>                                   |
| 2   | PS1_INT  | <b>PS1 Interrupt Status.</b>                                   |
| 1:0 | ALS_INT  | <b>ALS Interrupt Status. (Refer to Table 13 for encoding.)</b> |

**Notes:**

1. If the corresponding IRQ\_ENABLE bit is also set when the IRQ\_STATUS bit is set, the INT pin is asserted.
2. When INT\_MODE = 0, the host must write '1' to the corresponding XXX\_INT bit to clear the interrupt.
3. When INT\_MODE = 1, the internal sequencer clears all the XXX\_INT bits (and INT pin) automatically unless used with PS (Parameter Field PSx\_IM = 11). Use of INT\_MODE = 0 is recommended.

## ALS\_VIS\_DATA0: ALS\_VIS\_DATA Data Word Low Byte @ 0x22

|      |                   |   |   |   |   |   |   |   |
|------|-------------------|---|---|---|---|---|---|---|
| Bit  | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ALS_VIS_DATA[7:0] |   |   |   |   |   |   |   |
| Type | RW                |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name              | Function   |
|-----|-------------------|--|
| 7:0 | ALS_VIS_DATA[7:0] | <b>ALS VIS Data LSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

## ALS\_VIS\_DATA1: ALS\_VIS\_DATA Data Word High Byte @ 0x23

|      |                    |   |   |   |   |   |   |   |
|------|--------------------|---|---|---|---|---|---|---|
| Bit  | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ALS_VIS_DATA[15:8] |   |   |   |   |   |   |   |
| Type | RW                 |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name               | Function   |
|-----|--------------------|--|
| 7:0 | ALS_VIS_DATA[15:8] | <b>ALS VIS Data MSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

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ALS\_IR\_DATA0: ALS\_IR\_DATA Data Word Low Byte@ 0x24

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| Bit  | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------------------|---|---|---|---|---|---|---|
| Name | ALS_IR_DATA[7:0] |   |   |   |   |   |   |   |
| Type | RW               |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name             | Function  |
|-----|------------------|---|
| 7:0 | ALS_IR_DATA[7:0] | <b>ALS IR Data LSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

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ALS\_IR\_DATA1: ALS\_IR\_DATA Data Word High Byte @ 0x25

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| Bit  | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------|---|---|---|---|---|---|---|
| Name | ALS_IR_DATA[15:8] |   |   |   |   |   |   |   |
| Type | RW                |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name              | Function  |
|-----|-------------------|---|
| 7:0 | ALS_IR_DATA[15:8] | <b>ALS IR Data MSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

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PS1\_DATA0: PS1\_DATA Data Word Low Byte @ 0x26

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| Bit  | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | PS1_DATA[7:0] |   |   |   |   |   |   |   |
| Type | RW            |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name          | Function   |
|-----|---------------|--|
| 7:0 | PS1_DATA[7:0] | <b>PS1 Data LSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

## PS1\_DATA1: PS1\_DATA Data Word High Byte @ 0x27

---

| Bit  | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | PS1_DATA[15:8] |   |   |   |   |   |   |   |
| Type | RW             |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name           | Function   |
|-----|----------------|--|
| 7:0 | PS1_DATA[15:8] | <b>PS1 Data MSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

## PS2\_DATA0: PS2\_DATA Data Word Low Byte @ 0x28

---

| Bit  | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | PS2_DATA[7:0] |   |   |   |   |   |   |   |
| Type | RW            |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name           | Function   |
|-----|----------------|--|
| 7:0 | PS2_-DATA[7:0] | <b>PS2 Data LSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

## PS2\_DATA1: PS2\_DATA Data Word High Byte @ 0x29

---

| Bit  | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | PS2_DATA[15:8] |   |   |   |   |   |   |   |
| Type | RW             |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name           | Function   |
|-----|----------------|--|
| 7:0 | PS2_DATA[15:8] | <b>PS2 Data MSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

PS3\_DATA0: PS3\_DATA Data Word Low Byte @ 0x2A

---

| Bit  | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | PS3_DATA[7:0] |   |   |   |   |   |   |   |
| Type | RW            |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name          | Function   |
|-----|---------------|--|
| 7:0 | PS3_DATA[7:0] | <b>PS3 Data LSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

PS3\_DATA1: PS3\_DATA Data Word High Byte @ 0x2B

---

| Bit  | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | PS3_DATA[15:8] |   |   |   |   |   |   |   |
| Type | RW             |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name           | Function   |
|-----|----------------|--|
| 7:0 | PS3_DATA[15:8] | <b>PS3 Data MSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

AUX\_DATA0: AUX\_DATA Data Word Low Byte @ 0x2C

---

| Bit  | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | AUX_DATA[7:0] |   |   |   |   |   |   |   |
| Type | RW            |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name          | Function   |
|-----|---------------|--|
| 7:0 | AUX_DATA[7:0] | <b>AUX Data LSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

## AUX\_DATA1: AUX\_DATA Data Word High Byte @ 0x2D

---

| Bit  | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------|---|---|---|---|---|---|---|
| Name | AUX_DATA[15:8] |   |   |   |   |   |   |   |
| Type | RW             |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name           | Function   |
|-----|----------------|--|
| 7:0 | AUX_DATA[15:8] | <b>AUX Data MSB.</b> Once autonomous measurements have started, this register must be read after INT has asserted but before the next measurement is made. Refer to "AN498: Si114x Designer's Guide" Section 5.6.2 "Host Interrupt Latency." |

---

## PARAM\_RD @ 0x2E

---

| Bit  | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|---|---|---|---|---|---|---|
| Name | PARAM_RD |   |   |   |   |   |   |   |
| Type | RW       |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name     | Function  |
|-----|----------|---|
| 7:0 | PARAM_RD | Mailbox register for passing parameters from the sequencer to the host. |

---

## CHIP\_STAT @ 0x30

---

| Bit  | 7 | 6 | 5 | 4 | 3 | 2       | 1       | 0     |
|------|---|---|---|---|---|---------|---------|-------|
| Name |   |   |   |   |   | RUNNING | SUSPEND | SLEEP |
| Type |   |   |   |   |   | R       | R       | R     |

Reset value = 0000 0000

| Bit | Name     | Function   |
|-----|----------|--|
| 7:3 | Reserved | <b>Reserved</b>  |
| 2   | RUNNING  | Device is awake.   |
| 1   | SUSPEND  | Device is in a low-power state, waiting for a measurement to complete. |
| 0   | SLEEP    | Device is in its lowest power state.                                   |

---

**ANA\_IN\_KEY @ 0x3B to 0x3E**

---

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                 |
|------|---|---|---|---|---|---|---|-------------------|
| 0x3B |   |   |   |   |   |   |   | ANA_IN_KEY[31:24] |
| 0x3C |   |   |   |   |   |   |   | ANA_IN_KEY[23:16] |
| 0x3D |   |   |   |   |   |   |   | ANA_IN_KEY[15:8]  |
| 0x3E |   |   |   |   |   |   |   | ANA_IN_KEY[7:0]   |
| Type |   |   |   |   |   |   |   | RW                |

Reset value = 0000 0000

| Bit  | Name             | Function         |
|------|------------------|------------------|
| 31:0 | ANA_IN_KEY[31:0] | <b>Reserved.</b> |

## 4.7. Parameter RAM

Parameters are located in internal memory and are not directly addressable over I<sup>2</sup>C. They must be indirectly accessed using the PARAM\_QUERY and PARAM\_SET Commands that are described in "4.2. Command Protocol" on page 21.

Table 16. Parameter RAM Summary Table

| Parameter Name      | Offset    | Bit 7   | Bit 6       | Bit 5         | Bit 4         | Bit 3                      | Bit 2                      | Bit 1            | Bit 0  |  |  |  |  |  |  |
|---------------------|-----------|---|-------------|---------------|---------------|----------------------------|----------------------------|------------------|--------|--|--|--|--|--|--|
| I2C_ADDR            | 0x00      | I <sup>2</sup> C Address                              |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| CHLIST              | 0x01      | —   | EN_AUX      | EN_ALS_IR     | EN_ALS_VIS    | —                          | EN_PS3                     | EN_PS2           | EN_PS1 |  |  |  |  |  |  |
| PSLED12_SELECT      | 0x02      | —   | PS2_LED     |               |               |                            | —                          | PS1_LED          |        |  |  |  |  |  |  |
| PSLED3_SELECT       | 0x03      | —   |             |               |               | PS3_LED                    |                            |                  |        |  |  |  |  |  |  |
| Reserved            | 0x04      | Reserved (always set to 0)                            |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| PS_ENCODING         | 0x05      | —   | PS3_ALI_GN  | PS2_ALIGN     | PS1_ALIG_N    | Reserved (always set to 0) |                            |                  |        |  |  |  |  |  |  |
| ALS_ENCODING        | 0x06      | —   | —           | ALS_IR_ALI_GN | ALS_VIS_ALIGN | Reserved (always set to 0) |                            |                  |        |  |  |  |  |  |  |
| PS1_ADCMUX          | 0x07      | PS1 ADC Input Selection                               |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| PS2_ADCMUX          | 0x08      | PS2 ADC Input Selection                               |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| PS3_ADCMUX          | 0x09      | PS3 ADC Input Selection                               |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| PS_ADC_COUNTER      | 0x0A      | —   | PS_ADC_REC  |               |               |                            | Reserved (always set to 0) |                  |        |  |  |  |  |  |  |
| PS_ADC_GAIN         | 0x0B      | —   |             |               |               |                            |                            | PS_ADC_GAIN      |        |  |  |  |  |  |  |
| PS_ADC_MISC         | 0x0C      | —   | PS_RANGE    |               | —             | PS_ADC_MODE                |                            | —                | —      |  |  |  |  |  |  |
| Reserved            | 0x0D      | Reserved (do not modify from default setting of 0x02) |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| ALS_IR_ADCMUX       | 0x0E      | ALS_IR_ADCMUX   |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| AUX_ADCMUX          | 0x0F      | AUX ADC Input Selection                               |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| ALS_VIS_ADC_COUNTER | 0x10      | —   | VIS_ADC_REC |               |               |                            | Reserved (always set to 0) |                  |        |  |  |  |  |  |  |
| ALS_VIS_ADC_GAIN    | 0x11      | —   |             |               |               |                            |                            | ALS_VIS_ADC_GAIN |        |  |  |  |  |  |  |
| ALS_VIS_ADC_MISC    | 0x12      | Reserved (always set to 0)                            |             |               | VIS_RANGE     | Reserved (always set to 0) |                            |                  |        |  |  |  |  |  |  |
| Reserved            | 0x13      | Reserved (do not modify from default setting of 0x40) |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| Reserved            | 0x14–0x15 | Reserved (do not modify from default setting of 0x00) |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| ALS_HYST            | 0x16      | ALS Hysteresis  |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| PS_HYST             | 0x17      | PS Hysteresis   |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |
| PS_HISTORY          | 0x18      | PS History Setting                                    |             |               |               |                            |                            |                  |        |  |  |  |  |  |  |

Table 16. Parameter RAM Summary Table (Continued)

| Parameter Name    | Offset | Bit 7   | Bit 6      | Bit 5 | Bit 4                      | Bit 3 | Bit 2                      | Bit 1           | Bit 0 |
|-------------------|--------|---|------------|-------|----------------------------|-------|----------------------------|-----------------|-------|
| ALS_HISTORY       | 0x19   | ALS History Setting                                   |            |       |                            |       |                            |                 |       |
| ADC_OFFSET        | 0x1A   | ADC Offset  |            |       |                            |       |                            |                 |       |
| Reserved          | 0x1B   | Reserved (do not modify from default setting of 0x00) |            |       |                            |       |                            |                 |       |
| LED_REC           | 0x1C   | LED recovery time                                     |            |       |                            |       |                            |                 |       |
| ALS_IR_AD-COUNTER | 0x1D   | —   | IR_ADC_REC |       |                            |       | Reserved (always set to 0) |                 |       |
| ALS_IR_ADC_GAIN   | 0x1E   | —   |            |       |                            |       |                            | ALS_IR_ADC_GAIN |       |
| ALS_IR_ADC_MISC   | 0x1F   | Reserved<br>(always set to 0)                         | IR_RANGE   |       | Reserved (always set to 0) |       |                            |                 |       |

I<sup>2</sup>C @ 0x00

| Bit  | 7                             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------------------------------|---|---|---|---|---|---|---|
| Name | I <sup>2</sup> C Address[7:0] |   |   |   |   |   |   |   |
| Type | RW                            |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name                          | Function  |
|-----|-------------------------------|---|
| 7:0 | I <sup>2</sup> C Address[7:0] | Specifies a new I <sup>2</sup> C Address for the device to respond to. The new address takes effect when a BUSADDR command is received. |

## CHLIST @ 0x01

| Bit  | 7  | 6      | 5         | 4          | 3 | 2      | 1      | 0      |
|------|----|--------|-----------|------------|---|--------|--------|--------|
| Name |    | EN_AUX | EN_ALS_IR | EN_ALS_VIS |   | EN_PS3 | EN_PS2 | EN_PS1 |
| Type | RW |        |           |            |   |        |        |        |

Reset value = 0000 0000

| Bit | Name       | Function   |
|-----|------------|--|
| 7   | Reserved   |  |
| 6   | EN_AUX     | Enables Auxiliary Channel, data stored in AUX_DATA1[7:0] and AUX_DATA0[7:0].           |
| 5   | EN_ALS_IR  | Enables ALS IR Channel, data stored in ALS_IR_DATA1[7:0] and ALS_IR_DATA0[7:0].        |
| 4   | EN_ALS_VIS | Enables ALS Visible Channel, data stored in ALS_VIS_DATA1[7:0] and ALS_VIS_DATA0[7:0]. |

# Si1141/42/43

| Bit | Name     | Function  |
|-----|----------|---|
| 3   | Reserved |   |
| 2   | EN_PS3   | Enables PS Channel 3, data stored in PS3_DATA1[7:0] and PS3_DATA0[7:0]. |
| 1   | EN_PS2   | Enables PS Channel 2, data stored in PS2_DATA1[7:0] and PS2_DATA0[7:0]. |
| 0x  | EN_PS1   | Enables PS Channel 1, data stored in PS1_DATA1[7:0] and PS1_DATA0[7:0]. |

**Note:** For proper operation, CHLIST must be written with a non-zero value before forced measurements or autonomous operation is requested.

## PSLED12\_SELECT @ 0x02

| Bit  | 7 | 6 | 5            | 4 | 3 | 2 | 1            | 0 |
|------|---|---|--------------|---|---|---|--------------|---|
| Name |   |   | PS2_LED[2:0] |   |   |   | PS1_LED[2:0] |   |
| Type |   |   | RW           |   |   |   | RW           |   |

Reset value = 0010 0001

| Bit | Name         | Function  |
|-----|--------------|---|
| 7   | Reserved     |   |
| 6:4 | PS2_LED[2:0] | Specifies the LED pin driven during the PS2 Measurement. Note that any combination of irLEDs is possible.<br>000: NO LED DRIVE<br>xx1: LED1 Drive Enabled<br>x1x: LED2 Drive Enabled (Si1142 and Si1143 only. Clear for Si1141)<br>1xx: LED3 Drive Enabled (Si1143 only. Clear for Si1141 and Si1142) |
| 3   | Reserved     |   |
| 2:0 | PS1_LED[2:0] | Specifies the LED pin driven during the PS1 Measurement. Note that any combination of irLEDs is possible.<br>000: NO LED DRIVE<br>xx1: LED1 Drive Enabled<br>x1x: LED2 Drive Enabled (Si1142 and Si1143 only. Clear for Si1141)<br>1xx: LED3 Drive Enabled (Si1143 only. Clear for Si1141 and Si1142) |

## PSLED3\_SELECT @ 0x03

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1            | 0 |
|------|---|---|---|---|---|---|--------------|---|
| Name |   |   |   |   |   |   | PS3_LED[2:0] |   |
| Type |   |   |   |   |   |   | RW           |   |

Reset value = 0000 0100

| Bit | Name         | Function  |
|-----|--------------|---|
| 7:3 | Reserved     |   |
| 2:0 | PS3_LED[2:0] | Specifies the LED pin driven during the PS3 Measurement. Note that any combination of irLEDs is possible.<br>000: No LED drive.<br>xx1: LED1 drive enabled.<br>x1x: LED2 drive enabled (Si1142 and Si1143 only. Clear for Si1141).<br>1xx: LED3 drive enabled (Si1143 only. Clear for Si1141 and Si1142). |

---

**PS\_ENCODING @ 0x05**


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| Bit  | 7 | 6         | 5         | 4         | 3 | 2 | 1 | 0 |
|------|---|-----------|-----------|-----------|---|---|---|---|
| Name |   | PS3_ALIGN | PS2_ALIGN | PS1_ALIGN |   |   |   |   |
| Type |   | RW        | R/W       | R/W       |   |   |   |   |

Reset value = 0000 0000

| Bit | Name      | Function   |
|-----|-----------|--|
| 7   | Reserved  |  |
| 6   | PS3_ALIGN | When set, the ADC reports the least significant 16 bits of the 17-bit ADC when performing PS3 Measurement. Reports the 16 MSBs when cleared. |
| 5   | PS2_ALIGN | When set, the ADC reports the least significant 16 bits of the 17-bit ADC when performing PS2 Measurement. Reports the 16 MSBs when cleared. |
| 4   | PS1_ALIGN | When set, the ADC reports the least significant 16 bits of the 17-bit ADC when performing PS1 Measurement. Reports the 16 MSBs when cleared. |
| 3:0 | Reserved  | Always set to 0.   |

---

**ALS\_ENCODING @ 0x06**


---

| Bit  | 7 | 6 | 5            | 4             | 3 | 2 | 1 | 0 |
|------|---|---|--------------|---------------|---|---|---|---|
| Name |   |   | ALS_IR_ALIGN | ALS_VIS_ALIGN |   |   |   |   |
| Type |   |   | RW           | RW            |   |   |   |   |

Reset value = 0000 0000

| Bit | Name         | Function   |
|-----|--------------|--|
| 7:6 | Reserved     |  |
| 5   | ALS_IR_ALIGN | When set, the ADC reports the least significant 16 bits of the 17-bit ADC when performing ALS VIS Measurement. Reports the 16 MSBs when cleared. |

| Bit | Name          | Function  |
|-----|---------------|---|
| 4   | ALS_VIS_ALIGN | When set, the ADC reports the least significant 16 bits of the 17-bit ADC when performing ALS IR Measurement. Reports the 16 MSBs when cleared. |
| 3:0 | Reserved      | Always set to 0.  |

## PS1\_ADCMUX @ 0x07

| Bit  | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | PS1_ADCMUX[7:0] |   |   |   |   |   |   |   |
| Type | RW              |   |   |   |   |   |   |   |

Reset value = 0000 0011

| Bit | Name            | Function   |
|-----|-----------------|--|
| 7:0 | PS1_ADCMUX[7:0] | <p><b>Selects ADC Input for PS1 Measurement.</b></p> <p>The following selections are valid when PS_ADC_MODE = 1 (default). This setting is for normal Proximity Detection function.</p> <p>0x03: Large IR Photodiode<br/>0x00: Small IR Photodiode</p> <p>In addition, the following selections are valid for PS_ADC_MODE = 0. With this setting, irLED drives are disabled and the PS channels are no longer operating in normal Proximity Detection function. The results have no reference and the references needs to be measured in a separate measurement.</p> <p>0x02: Visible Photodiode<br/>A separate 'No Photodiode' measurement should be subtracted from this reading. Note that the result is a negative value. The result should therefore be negated to arrive at the Ambient Visible Light reading.</p> <p>0x03: Large IR Photodiode<br/>A separate "No Photodiode" measurement should be subtracted to arrive at Ambient IR reading.</p> <p>0x00: Small IR Photodiode<br/>A separate "No Photodiode" measurement should be subtracted to arrive at Ambient IR reading.</p> <p>0x06: No Photodiode<br/>This is typically used as reference for reading ambient IR or visible light.</p> <p>0x25: GND voltage<br/>This is typically used as the reference for electrical measurements.</p> <p><b>0x65: Temperature</b><br/>(Should be used only for relative temperature measurement. Absolute Temperature not guaranteed) A separate GND measurement should be subtracted from this reading.</p> <p>0x75: V<sub>DD</sub> voltage<br/>A separate GND measurement is needed to make the measurement meaningful.</p> |

## PS2\_ADCMUX @ 0x08

| Bit         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| <b>Name</b> | PS2_ADCMUX[7:0] |   |   |   |   |   |   |   |
| <b>Type</b> | R/W             |   |   |   |   |   |   |   |

Reset value = 0000 0011

| Bit | Name            | Function  |
|-----|-----------------|---|
| 7:0 | PS2_ADCMUX[7:0] | Selects input for PS2 measurement. See PS1_ADCMUX register description for details. |

## PS3\_ADCMUX @ 0x09

| Bit         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| <b>Name</b> | PS3_ADCMUX[7:0] |   |   |   |   |   |   |   |
| <b>Type</b> | R/W             |   |   |   |   |   |   |   |

Reset value = 0000 0011

| Bit | Name            | Function  |
|-----|-----------------|---|
| 7:0 | PS3_ADCMUX[7:0] | Selects input for PS3 measurement. See PS1_ADCMUX register description for details. |

## PS\_ADC\_COUNTER @ 0x0A

| Bit         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| <b>Name</b> | PS_ADC_REC[2:0] |   |   |   |   |   |   |   |
| <b>Type</b> | RW R/W R/W      |   |   |   |   |   |   |   |

Reset value = 0111 0000

| Bit | Name            | Function   |
|-----|-----------------|--|
| 7   | Reserved        |  |
| 6:4 | PS_ADC_REC[2:0] | <p>Recovery period the ADC takes before making a PS measurement.</p> <p>000: 1 ADC Clock (50 ns times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>001: 7 ADC Clock (350 ns times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>010: 15 ADC Clock (750 ns times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>011: 31 ADC Clock (1.55 <math>\mu</math>s times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>100: 63 ADC Clock (3.15 <math>\mu</math>s times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>101: 127 ADC Clock (6.35 <math>\mu</math>s times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>110: 255 ADC Clock (12.75 <math>\mu</math>s times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>111: 511 ADC Clock (25.55 <math>\mu</math>s times <math>2^{PS\_ADC\_GAIN}</math>)</p> <p>The recommended PS_ADC_REC value is the one's complement of PS_ADC_GAIN.</p> |
| 3:0 | Reserved        | Always set to 0.   |

## PS\_ADC\_GAIN @ 0x0B

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                  |     |     |
|------|---|---|---|---|---|---|---|---|------------------|-----|-----|
| Name |   |   |   |   |   |   |   |   | PS_ADC_GAIN[2:0] |     |     |
| Type |   |   |   |   |   |   |   |   | R/W              | R/W | R/W |

Reset value = 0000 0000

| Bit | Name             | Function   |
|-----|------------------|--|
| 7:3 | Reserved         |  |
| 2:0 | PS_ADC_GAIN[2:0] | <p>Increases the irLED pulse width and ADC integration time by a factor of <math>(2^{\wedge} PS\_ADC\_GAIN)</math> for all PS measurements.</p> <p>Care must be taken when using this feature. At an extreme case, each of the three PS measurements can be configured to drive three separate irLEDs, each of which, are configured for 359 mA. The internal sequencer does not protect the device from such an error. To prevent permanent damage to the device, do not enter any value greater than 5 without consulting with Silicon Labs.</p> <p>For Example:</p> <p>0x0: ADC Clock is divided by 1</p> <p>0x4: ADC Clock is divided by 16</p> <p>0x5: ADC Clock is divided by 32</p> |

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PS\_ADC\_MISC @ 0x0C

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| Bit  | 7  | 6 | 5        | 4 | 3 | 2           | 1 | 0 |
|------|----|---|----------|---|---|-------------|---|---|
| Name |    |   | PS_RANGE |   |   | PS_ADC_MODE |   |   |
| Type | RW |   |          |   |   | RW          |   |   |

Reset value = 0000 0100

| Bit | Name        | Function   |
|-----|-------------|--|
| 7:6 | Reserved    |  |
| 5   | PS_RANGE    | When performing PS measurements, the ADC can be programmed to operate in high sensitivity operation or high signal range. The high signal range is useful in operation under direct sunlight.<br>0: Normal Signal Range<br>1: High Signal Range (Gain divided by 14.5) |
| 4:3 | Reserved    |  |
| 2   | PS_ADC_MODE | PS Channels can either operate normally as PS channels, or it can be used to perform raw ADC measurements:<br>0: Raw ADC Measurement Mode<br>1: Normal Proximity Measurement Mode  |
| 1:0 | Reserved    |  |

---

ALS\_IR\_ADCMUX @ 0x0E

---

| Bit  | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | ALS_IR_ADCMUX |   |   |   |   |   |   |   |
| Type | RW            |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name          | Function   |
|-----|---------------|--|
| 7:0 | ALS_IR_ADCMUX | <b>Selects ADC Input for ALS_IR Measurement.</b><br>0x00: Small IR photodiode<br>0x03: Large IR photodiode |

## AUX\_ADCMUX @ 0x0F

| Bit  | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------------|---|---|---|---|---|---|---|
| Name | AUX_ADCMUX[7:0] |   |   |   |   |   |   |   |
| Type | RW              |   |   |   |   |   |   |   |

Reset value = 0110 0101

| Bit | Name            | Function   |
|-----|-----------------|--|
| 7:0 | AUX_ADCMUX[7:0] | Selects input for AUX Measurement. These measurements are referenced to GND.<br>0x65: Temperature (Should be used only for relative temperature measurement. Absolute Temperature not guaranteed)<br>0x75: V <sub>DD</sub> voltage |

## ALS\_VIS\_ADC\_COUNTER @ 0x10

| Bit  | 7 | 6                | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------|---|------------------|---|---|---|---|---|---|--|
| Name |   | VIS_ADC_REC[2:0] |   |   |   |   |   |   |  |
| Type |   | RW R/W R/W       |   |   |   |   |   |   |  |

Reset value = 0111 0000

| Bit | Name             | Function  |
|-----|------------------|---|
| 7   | Reserved         |   |
| 6:4 | VIS_ADC_REC[2:0] | Recovery period the ADC takes before making a ALS-VIS measurement.<br>000: 1 ADC Clock (50 ns times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>001: 7 ADC Clock (350 ns times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>010: 15 ADC Clock (750 ns times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>011: 31 ADC Clock (1.55 µs times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>100: 63 ADC Clock (3.15 µs times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>101: 127 ADC Clock (6.35 µs times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>110: 255 ADC Clock (12.75 µs times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>111: 511 ADC Clock (25.55 µs times 2 <sup>ALS_VIS_ADC_GAIN</sup> )<br>The recommended VIS_ADC_REC value is the one's complement of ALS_VIS_ADC_GAIN. |
| 3:0 | Reserved         | Always set to 0.  |

**Note:** For A02 and earlier, this parameter also controls ALS-IR measurements.

## ALS\_VIS\_ADC\_GAIN @ 0x11

| Bit  | 7 | 6 | 5 | 4 | 3 | 2  | 1   | 0                     |
|------|---|---|---|---|---|----|-----|-----------------------|
| Name |   |   |   |   |   |    |     | ALS_VIS_ADC_GAIN[2:0] |
| Type |   |   |   |   |   | RW | R/W | RW                    |

Reset value = 0000 0000

| Bit | Name                  | Function   |
|-----|-----------------------|--|
| 7:3 | Reserved              |  |
| 2:0 | ALS_VIS_ADC_GAIN[2:0] | <p>Increases the ADC integration time for ALS Visible measurements by a factor of (2 ^ ALS_VIS_ADC_GAIN). This allows visible light measurement under dark glass. The maximum gain is 128 (0x7).</p> <p>For Example:</p> <p>0x0: ADC Clock is divided by 1<br/> 0x4: ADC Clock is divided by 16<br/> 0x6: ADC Clock is divided by 64</p> |

**Note:** For A02 and earlier, this parameter also controls ALS-IR measurements.

## ALS\_VIS\_ADC\_MISC @ 0x12

| Bit  | 7 | 6 | 5         | 4 | 3 | 2 | 1 | 0 |
|------|---|---|-----------|---|---|---|---|---|
| Name |   |   | VIS_RANGE |   |   |   |   |   |
| Type |   |   | RW        |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name      | Function  |
|-----|-----------|---|
| 7:6 | Reserved  |   |
| 5   | VIS_RANGE | <p>When performing ALS-VIS measurements, the ADC can be programmed to operate in high sensitivity operation or high signal range.</p> <p>The high signal range is useful in operation under direct sunlight.</p> <p>0: Normal Signal Range<br/> 1: High Signal Range (Gain divided by 14.5)</p> |
| 4:0 | Reserved  |   |

**Note:** For A02 and earlier, this parameter also controls ALS-IR measurements.

## ALS\_HYST @ 0x16

---

| Bit  | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---|---|---|---|---|
| Name | ALS_HYST[7:0] |   |   |   |   |   |   |   |
| Type | RW            |   |   |   |   |   |   |   |

Reset value = 0100 1000

| Bit | Name          | Function  |
|-----|---------------|---|
| 7:0 | ALS_HYST[7:0] | ALS_HYST represents a hysteresis applied to the ALS_LOW_TH and ALS_HIGH_TH thresholds. This is in an 8-bit compressed format, representing a 16-bit value. For example:<br>0x48: 24 ADC Codes<br>Please refer to “AN498: Si114x Designer’s Guide”, Section 5.4 “Compression Concept.” |

## PS\_HYST @ 0x17

---

| Bit  | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | PS_HYST[7:0] |   |   |   |   |   |   |   |
| Type | RW           |   |   |   |   |   |   |   |

Reset value = 0100 1000

| Bit | Name         | Function  |
|-----|--------------|---|
| 7:0 | PS_HYST[7:0] | PS_HYST represents a hysteresis applied to the PS1_TH, PS2_TH and PS3_TH thresholds. This is in an 8-bit compressed format, representing a 16-bit value. For example: 0x48: 24 ADC Codes.<br>Please refer to “AN498: Si114x Designer’s Guide”, Section 5.4 “Compression Concept.” |

---

PS\_HISTORY @ 0x18

---

|      |                 |   |   |   |   |   |   |   |
|------|-----------------|---|---|---|---|---|---|---|
| Bit  | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS_HISTORY[7:0] |   |   |   |   |   |   |   |
| Type | RW              |   |   |   |   |   |   |   |

Reset value = 0000 0011

| Bit | Name            | Function   |
|-----|-----------------|--|
| 7:0 | PS_HISTORY[7:0] | PS_HISTORY is a bit-field representing the number of consecutive samples exceeding the threshold and hysteresis to change status.<br>For example:<br>0x03: 2 consecutive samples<br>0x07: 3 consecutive samples<br>0xFF: 8 consecutive samples |

---

ALS\_HISTORY @ 0x19

---

|      |                  |   |   |   |   |   |   |   |
|------|------------------|---|---|---|---|---|---|---|
| Bit  | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ALS_HISTORY[7:0] |   |   |   |   |   |   |   |
| Type | RW               |   |   |   |   |   |   |   |

Reset value = 0000 0011

| Bit | Name             | Function  |
|-----|------------------|---|
| 7:0 | ALS_HISTORY[7:0] | ALS_HISTORY is a bit-field representing the number of consecutive samples exceeding the threshold and hysteresis to change status.<br>For example:<br>0x03: Two consecutive samples<br>0x07: Three consecutive samples<br>0xFF: Eight consecutive samples |

---

ADC\_OFFSET @ 0x1A

---

|      |                 |   |   |   |   |   |   |   |
|------|-----------------|---|---|---|---|---|---|---|
| Bit  | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ADC_OFFSET[7:0] |   |   |   |   |   |   |   |
| Type | RW              |   |   |   |   |   |   |   |

Reset value = 1000 0000

| Bit | Name            | Function  |
|-----|-----------------|---|
| 7:0 | ADC_OFFSET[7:0] | <p>ADC_OFFSET is an 8-bit compressed value representing a 16-bit value added to all measurements. Since most measurements are relative measurements involving a arithmetic subtraction and can result in a negative value. Since 0xFFFF is treated as an overrange indicator, the ADC_OFFSET is added so that the values reported in the I<sup>2</sup>C register map are never confused with the 0xFFFF overrange indicator.</p> <p>For example:</p> <ul style="list-style-type: none"><li>0x60: Measurements have a 64-code offset</li><li>0x70: Measurements have a 128-code offset</li><li>0x80: Measurements have a 256-code offset</li></ul> <p>Please refer to “AN498: Si114x Designer’s Guide”, Section 5.4 “Compression Concept.”</p> |

## LED\_REC @ 0x1C

| Bit  | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|--------------|---|---|---|---|---|---|---|
| Name | LED_REC[7:0] |   |   |   |   |   |   |   |
| Type | RW           |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit | Name         | Function  |
|-----|--------------|-----------|
| 7:0 | LED_REC[7:0] | Reserved. |

## ALS\_IR\_ADC\_COUNTER @ 0x1D

| Bit  | 7  | 6               | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----|-----------------|---|---|---|---|---|---|
| Name |    | IR_ADC_REC[2:0] |   |   |   |   |   |   |
| Type | RW |                 |   |   |   |   |   |   |

Reset value = 0111 0000

| Bit   | Name            | Function  |
|---|-----------------|---|
| 7   | Reserved        |   |
| 6:4   | IR_ADC_REC[2:0] | Recovery period the ADC takes before making a ALS-IR measurement.<br>000: 1 ADC Clock (50 ns times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>001: 7 ADC Clock (350 ns times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>010: 15 ADC Clock (750 ns times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>011: 31 ADC Clock (1.55 $\mu$ s times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>100: 63 ADC Clock (3.15 $\mu$ s times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>101: 127 ADC Clock (6.35 $\mu$ s times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>110: 255 ADC Clock (12.75 $\mu$ s times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>111: 511 ADC Clock (25.55 $\mu$ s times $2^{\text{ALS\_IR\_ADC\_GAIN}}$ )<br>The recommended IR_ADC_REC value is the one's complement of ALS_IR_ADC_GAIN. |
| 3:0   | Reserved        | Always set to 0.  |
| <b>Note:</b> This parameter available for sequencer revisions A03 or later. |                 |   |

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**ALS\_IR\_ADC\_GAIN @ 0x1E**


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| Bit         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
|-------------|----------------------|---|---|---|---|---|---|-----|
| <b>Name</b> | ALS_IR_ADC_GAIN[2:0] |   |   |   |   |   |   |     |
| <b>Type</b> | R/W                  |   |   |   |   |   |   | R/W |

Reset value = 0000 0000

| Bit   | Name                 | Function  |
|---|----------------------|---|
| 7:3   | Reserved             |   |
| 2:0   | ALS_IR_ADC_GAIN[2:0] | Increases the ADC integration time for IR Ambient measurements by a factor of (2 ^ ALS_IR_ADC_GAIN). The maximum gain is 128 (0x7).<br>For Example:<br>0x0: ADC Clock is divided by 1<br>0x4: ADC Clock is divided by 16<br>0x6: ADC Clock is divided by 64 |
| <b>Note:</b> This parameter available for sequencer revisions A03 or later. |                      |   |

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**ALS\_IR\_ADC\_MISC @ 0x1F**


---

| Bit         | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|---|---|---|---|---|---|---|
| <b>Name</b> | IR_RANGE |   |   |   |   |   |   |   |
| <b>Type</b> | RW       |   |   |   |   |   |   |   |

Reset value = 0000 0000

| Bit  | Name     | Function  |
|--|----------|---|
| 7:6  | Reserved |   |
| 5  | IR_RANGE | When performing ALS-IR measurements, the ADC can be programmed to operate in high sensitivity operation or high signal range.<br>The high signal range is useful in operation under direct sunlight.<br>0: Normal Signal Range<br>1: High Signal Range (Gain divided by 14.5) |
| 4:0  | Reserved | Write operations to this RAM parameter must preserve this bit-field value using read-modify-write.  |
| <b>Note:</b> This parameter is available for sequencer revisions A03 or later. |          |   |

## 5. Pin Descriptions

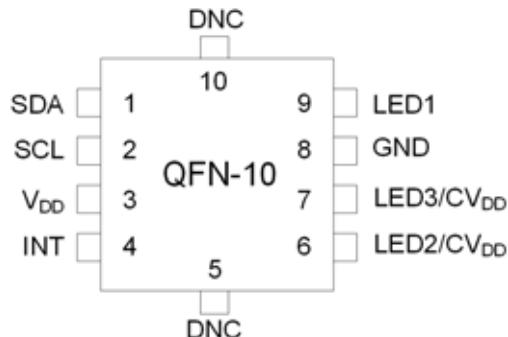


Table 17. Pin Descriptions

| Pin | Name                               | Type          | Description   |
|-----|------------------------------------|---------------|---|
| 1   | SDA                                | Bidirectional | I <sup>2</sup> C Data.  |
| 2   | SCL                                | Input         | I <sup>2</sup> C Clock.   |
| 3   | V <sub>DD</sub>                    | Power         | Power Supply.<br>Voltage source.  |
| 4   | INT                                | Bidirectional | Interrupt Output.<br>Open-drain interrupt output pin. Must be at logic level high during power-up sequence to enable low power operation.   |
| 5   | DNC                                |               | Do Not Connect.<br>This pin is electrically connected to an internal Si1141/42/43 node. It should remain unconnected.   |
| 6   | LED2/CV <sub>DD</sub> <sup>1</sup> | Output        | LED2 Output/Connect to V <sub>DD</sub> . <sup>1</sup><br>Programmable constant current sink normally connected to an infrared LED cathode. Connect directly to V <sub>DD</sub> when not in use.   |
| 7   | LED3/CV <sub>DD</sub> <sup>2</sup> | Output        | LED3 Output./Connect to V <sub>DD</sub> . <sup>2</sup><br>Programmable constant current sink normally connected to an infrared LED cathode. If V <sub>LED</sub> < (V <sub>DD</sub> + 0.5 V), a 47 kΩ pull-up resistor from LED3 to V <sub>DD</sub> is needed for proper operation. Connect directly to V <sub>DD</sub> when not in use. |
| 8   | GND                                | Power         | Ground.<br>Reference voltage.   |
| 9   | LED1                               | Output        | LED1 Output.<br>Programmable constant current sink normally connected to an infrared LED cathode.   |
| 10  | DNC                                |               | Do Not Connect.<br>This pin is electrically connected to an internal Si1141/42/43 node. It should remain unconnected.   |

**Notes:**

1. Si1142 and Si1143 only. Must connect to V<sub>DD</sub> in Si1141.
2. Si1143 only. Must connect to V<sub>DD</sub> in Si1141 and Si1142.

## 6. Ordering Guide

| Part Number                  | Package | LED Drivers | AEC-Q100 |
|------------------------------|---------|-------------|----------|
| Si1141-A11-GMR <sup>1</sup>  | QFN-10  | 1           | N        |
| Si1142-A11-GMR <sup>2</sup>  | QFN-10  | 2           | N        |
| Si1143-A11-GMR <sup>1</sup>  | QFN-10  | 3           | N        |
| Si1141-A11-YM0R <sup>2</sup> | QFN-10  | 1           | Y        |
| Si1143-A11-YM0R <sup>2</sup> | QFN-10  | 3           | Y        |

**Notes:**

- 1. Not Recommended for New Designs.
- 2. End of life.

## 7. Package Outline: 10-Pin QFN

Figure 15 illustrates the package details for the Si1141/42/43 QFN package. Table 18 lists the values for the dimensions shown in the illustration.

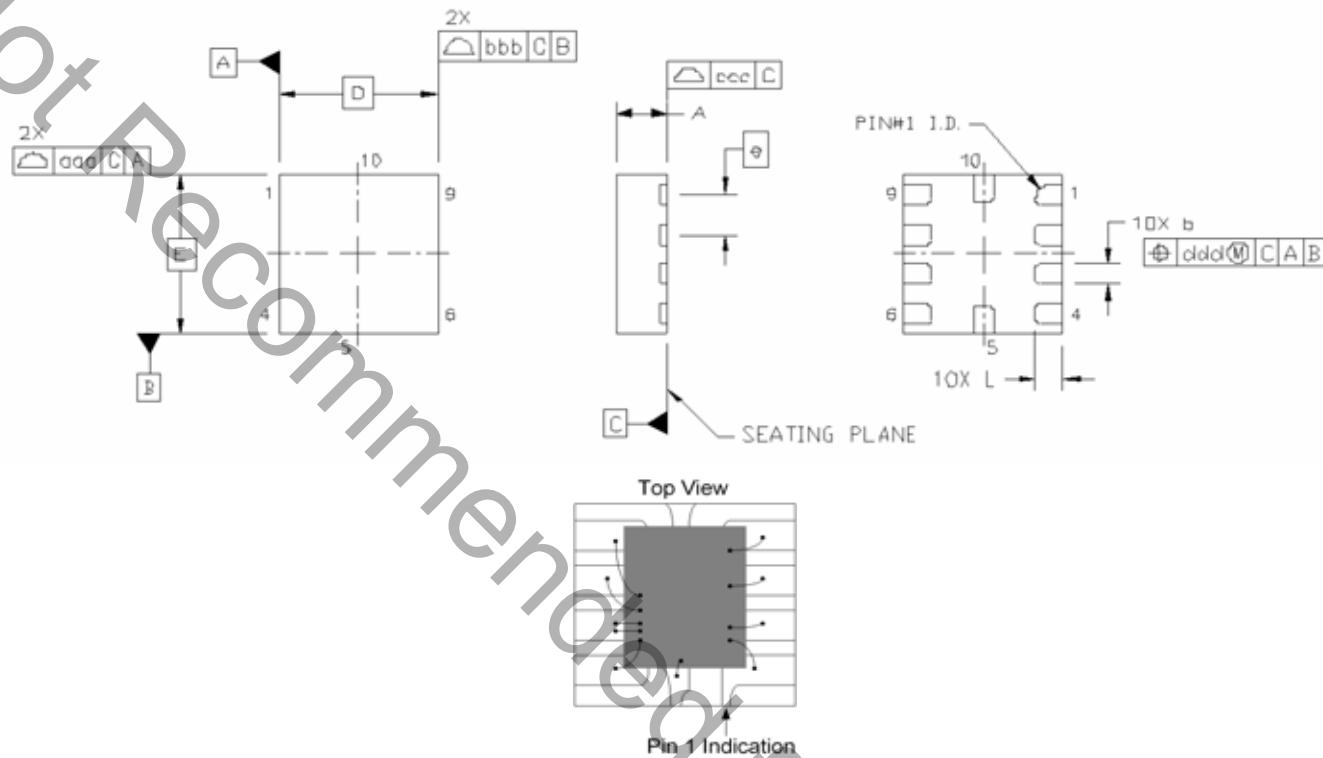


Figure 15. QFN Package Diagram Dimensions

Table 18. Package Diagram Dimensions

| Dimension   | Min  | Nom  | Max       |
|---|------|------|-----------|
| A   | 0.55 | 0.65 | 0.75      |
| b   | 0.20 | 0.25 | 0.30      |
| D   |      |      | 2.00 BSC. |
| e   |      |      | 0.50 BSC. |
| E   |      |      | 2.00 BSC. |
| L   | 0.30 | 0.35 | 0.40      |
| aaa   |      | 0.10 |           |
| bbb   |      | 0.10 |           |
| ccc   |      | 0.08 |           |
| ddd   |      | 0.10 |           |
| <b>Notes:</b>   |      |      |           |
| 1. All dimensions shown are in millimeters (mm).      |      |      |           |
| 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. |      |      |           |

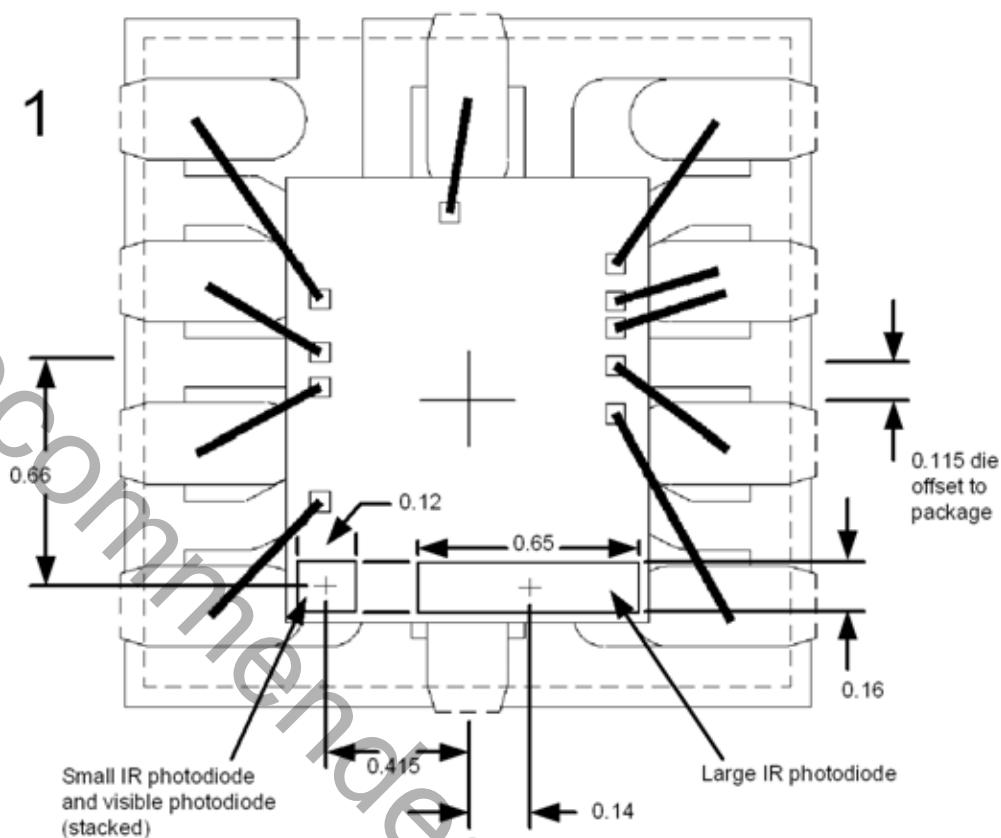
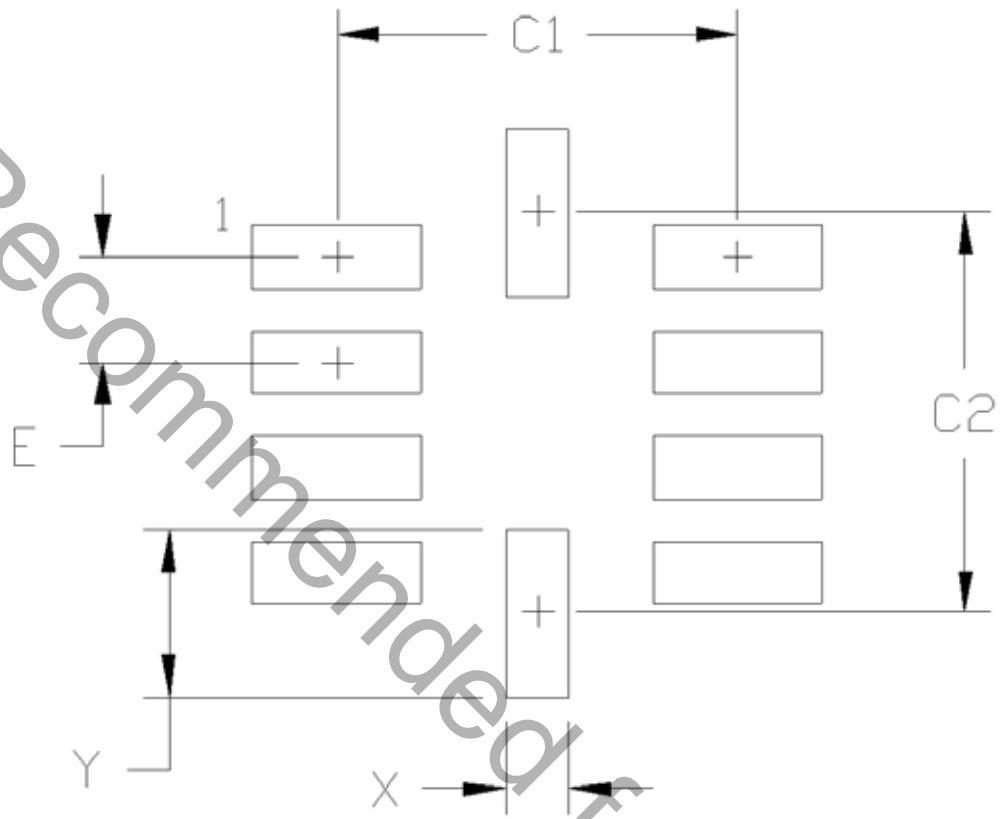


Figure 16. Photodiode Centers

## 8. Suggested PCB Land Pattern



| Dimension | mm   |
|-----------|------|
| C1        | 1.90 |
| C2        | 1.90 |
| E         | 0.50 |
| X         | 0.30 |
| Y         | 0.80 |

**Notes:****General**

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 0.060 mm minimum, all the way around the pad.

**Stencil Design**

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

**Card Assembly**

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

## DOCUMENT CHANGE LIST

### Revision 0.2 to Revision 0.3

- Updated document title from Si1140 to Si114x.
- Updated "7. Package Outline: 10-Pin QFN" on page 71.
- Updated Tables 4, 1, and 2.
- Added Figures 1, 2, and 4.
- Added register map and descriptions.

### Revision 0.3 to Revision 0.4

- Updated document title from Si114x to Si1143.
- Updated Applications Section
- Updated Tables 2 and 3.
- Updated Figure 1, Figure 4.
- Updated Table 8, Table 9.
- Updated Pin Assignments.
- Updated Register maps and description.

### Revision 0.4 to Revision 0.41

- Added Si1141 and Si1142 in addition to Si1143.
- Added the ODFN-8 package option.
- Some sections were rearranged.
- Added the signal-path software-model schematic.
- Renamed PARAM\_IN to PARAM\_WR for clarity.
- Renamed PARAM\_OUT to PARAM\_RD for clarity.
- Renamed PS\_ADC\_CLKDIV to PS\_ADC\_GAIN for clarity.
- Renamed ALS\_VIS\_ADC\_CLKDIV to ALS\_VIS\_ADC\_GAIN for clarity.
- Renamed ALS\_IR\_ADC\_CLKDIV to ALS\_IR\_ADC\_GAIN for clarity.
- Minor changes in register and parameter terminology.

### Revision 0.41 to Revision 0.5

- Updated Tables 1, 4, 2, and 15.
- Updated Figure 1.
- Added Figures 2 and 16.
- Updated register table reset values.
- Added "HW\_KEY @ 0x07" register.
- Updated "ALS\_VIS\_ADC\_MISC @ 0x12" register.
- Updated "ALS\_IR\_ADC\_MISC @ 0x1F" register.
- Updated "6. Ordering Guide".
- Updated "Features".
- Updated "Description".
- Updated "5. Pin Descriptions".
- Updated "6. Ordering Guide".

- Updated "7. Package Outline: 10-Pin QFN".
- Deleted Section 7.1.
- Deleted Section 7.2.

### Revision 0.5 to Revision 1.0

- Lux range and other minor changes on front page.
- Added sensitivity data for all three photodiodes.
- Added offset-drift data for all three photodiodes.
- Updated startup time to 25 ms.
- Minor bit-field definition corrections.
- Clarified ripple-voltage recommendation.
- Added MM and CDM ESD rating.
- Clarified standby-mode Idd.
- Clarified LED output leakage current.
- Added limits to LED active currents.
- Ordering code update.

### Revision 1.0 to Revision 1.1

- Corrected reset state of PS\_ADC\_COUNTER.
- Minor correction in signal-path programming model schematic.
- Corrected access mode of ALS\_IR\_ADCMUX from register space to parameter space.

### Revision 1.1 to Revision 1.2

- Corrected reset state of PS\_ADC\_COUNTER.
- Added leakage specifications for pins INT, SCL, and SDA.
- Changed format of proximity-threshold registers from compressed to uncompressed.
- Changed firmware revision from A10 to A11.
- Added reference to AN498 for details on the compression scheme.
- Clarified recovery times specified in PS\_ADC\_REC, VIS\_ADC\_REC, and IR\_ADC\_REC.
- Suggested PCB Land Pattern.
- Changed photodiode coordinate origin to package center.
- Added temperature sensor information.
- Added remarks on the use of MEAS\_RATE, ALS\_RATE, and PS\_RATE.
- Added remarks on I<sup>2</sup>C Broadcast Reset.
- Added performance graphs.
- Changed format of PS1TH, PS2TH, PS3TH, ALS\_LO\_TH, ALS\_HIGH\_TH from 8-bit compressed to 16-bit linear to allow finer threshold control.

## Revision 1.2 to Revision 1.3

- Updated bit names for ALS\_LOW\_TH0 @ 0x0B, ALS\_LOW\_TH1@0x0C, ALS\_HI\_TH0@0x0D, and ALS\_HI-TH1@0x0E.
- Changed IRQ\_MODE1 to IRQ\_MODE2 in Table 14.
- Changed pin name for pin 5 in pin diagrams on first page and start of section 5 from NC to DNC.
- Changed pin name and description for pin 5 in Table 17.
- Min  $V_{DD}$  changed from 1.8 V to 1.71 V.

## Revision 1.3 to Revision 1.4

- Added minimum I<sup>2</sup>C clock frequency.
- Updated photodiode spectral response.
- Clarified usage of Command Register and Parameter RAM.
- Clarified LED2 and LED3 connection when using Si1141 and Si1142.

## Revision 1.4 to Revision 1.41

- Revised document title from Si114x to Si1141-42-43.
- Updated "6. Ordering Guide" .
  - Added orderable part numbers with AEC-Q100 qualification.

## Revision 1.41 to Revision 1.42

- Added a missing ACK time period in Figure 12, "Host Interface Burst Read,".
- The description of INT operation in the "2.4. Host Interface" section is corrected.
- An ALWAYS\_ACTIVE mode is added and described in the "3. Operational Modes" section.
- The Limitation of MEAS\_RATE and the formula to use is corrected.
- The limitations of command write timing are explained in a new subsection in "3. Operational Modes" .
- Table 5, "Command Register Summary," on page 21 in the "4.2. Command Protocol" section contained references to an incorrect table number, which have been corrected.
- Table 15, "I2C Register Summary," on page 30 in the "4.6. I2C Registers" section has the HW\_KEY register corrected. The value takes up all eight bits at register address (0x07).
- A new section, "3.7. Avoiding an Unexpected Reset" , was added describing a reset that may happen if all the cautions in the other sections are not followed.
- Updated "6. Ordering Guide" on page 70.

## Revision 1.42 to Revision 1.43

- Updated "6. Ordering Guide" on page 70.

## Revision 1.43 to Revision 1.44

- Updated "6. Ordering Guide" on page 70 to note NRND and EOL OPNs.



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