

NTMJS1D5N04CL

Power MOSFET

40 V, 1.4 mΩ, 200 A, Single N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK8 Package, Industry Standard
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	$T_C = 25^\circ\text{C}$	I_D	200
			140
Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$	P_D	110
			53
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	$T_A = 25^\circ\text{C}$	I_D	38
			27
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	$T_A = 25^\circ\text{C}$	P_D	3.8
			1.9
Pulsed Drain Current	I_{DM}	900	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175	°C
Source Current (Body Diode)	I_S	120	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 15\text{ A}$)	E_{AS}	493	mJ
Single Pulse Drain-to-Source Voltage ($t_p = 10\text{ }\mu\text{s}$)	V_{DSM}	48	V
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.4	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	36	

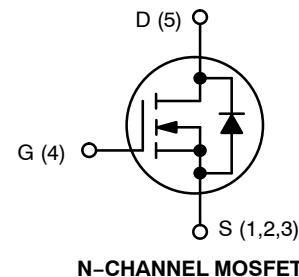
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
40 V	1.4 mΩ @ 10 V	
	2.2 mΩ @ 4.5 V	200 A



1D5N04CL = Specific Device Code

A = Assembly Location

WL = Wafer Lot

Y = Year

W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NTMJS1D5N04CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				2.0		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C			10	μA
			T _J = 125°C			250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 130 μA		1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.6		mV/°C
Drain-to-Source On Resistance	R _{DSS(on)}	V _{GS} = 4.5 V	I _D = 50 A		1.7	2.2	mΩ
		V _{GS} = 10 V	I _D = 50 A		1.2	1.4	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 50 A			256		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 20 V		4300		pF
Output Capacitance	C _{OSS}			1900		
Reverse Transfer Capacitance	C _{rss}			72		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 20 V; I _D = 50 A		32		nC
Total Gate Charge	Q _{G(TOT)}			70		
Threshold Gate Charge	Q _{G(TH)}			7.0		
Gate-to-Source Charge	Q _{GS}			12		
Gate-to-Drain Charge	Q _{GD}			9.0		
Plateau Voltage	V _{GP}			2.9		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 20 V, I _D = 50 A, R _G = 1 Ω		15		ns
Rise Time	t _r			140		
Turn-Off Delay Time	t _{d(OFF)}			31		
Fall Time	t _f			9		

DRAIN-SOURCE DIODE CHARACTERISTICS

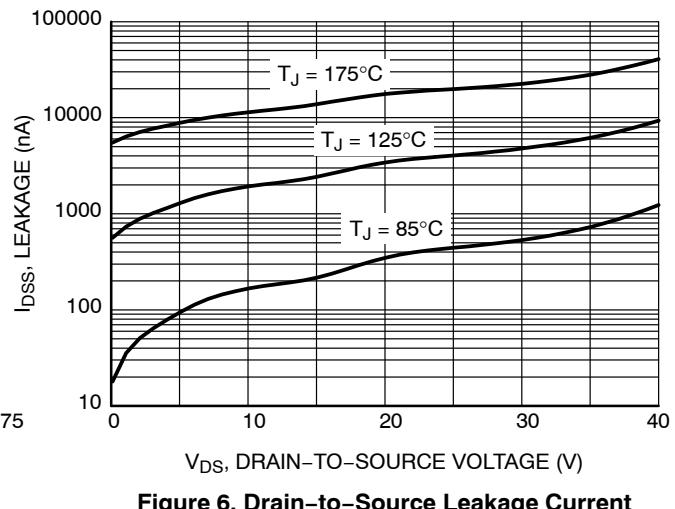
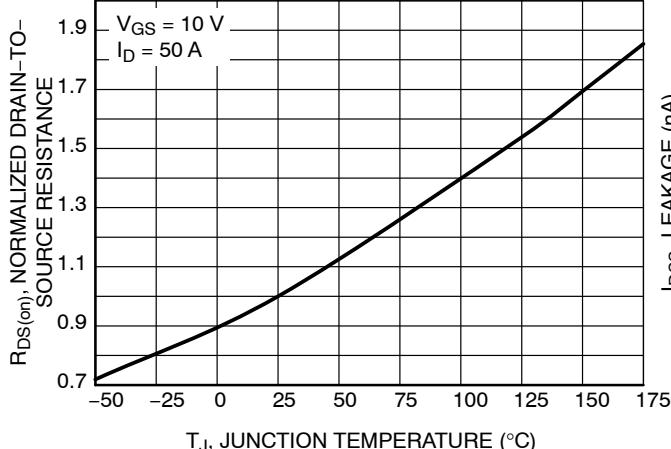
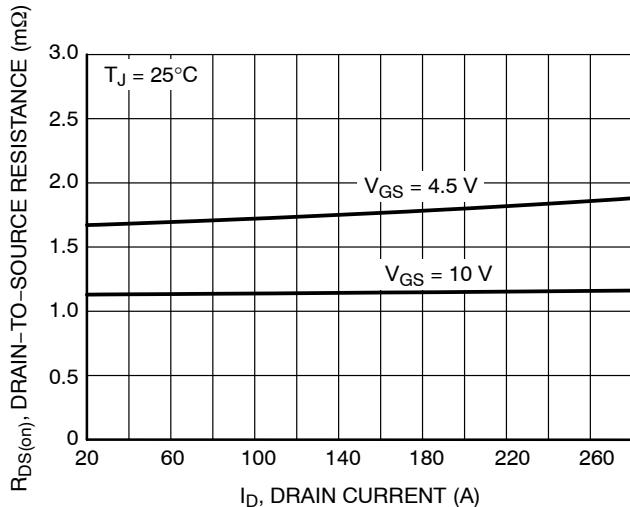
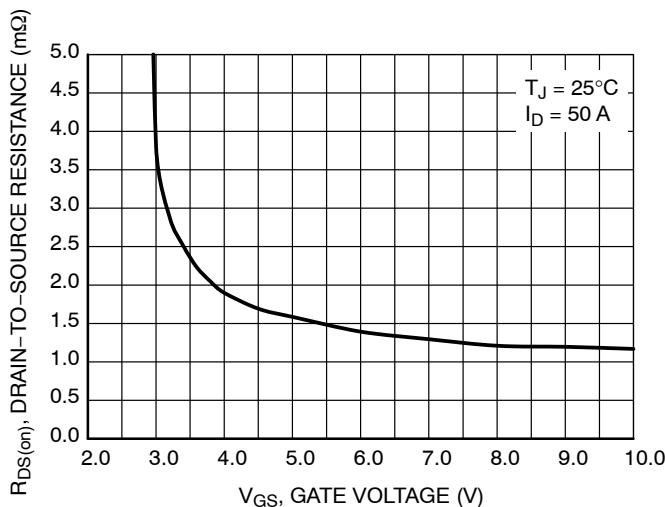
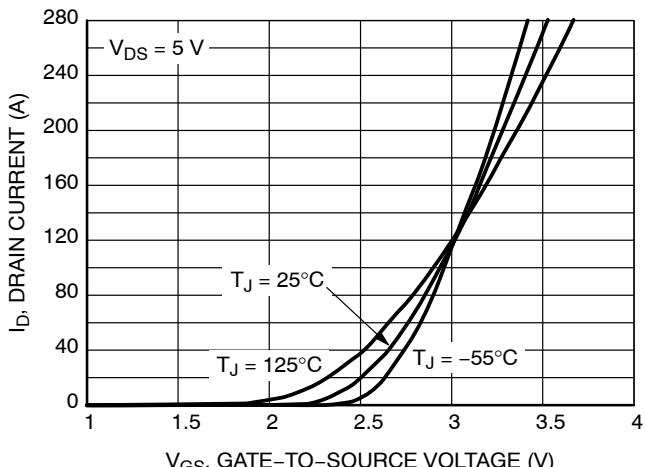
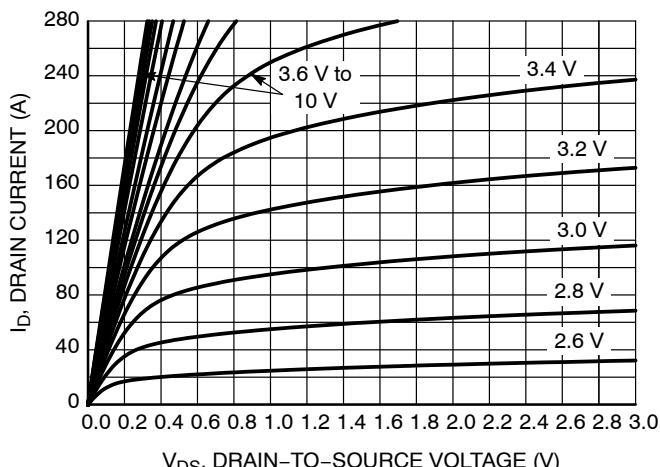
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 50 A	T _J = 25°C		0.81	1.2	V
			T _J = 125°C		0.68		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A			61		ns
Charge Time	t _a				29		
Discharge Time	t _b				32		
Reverse Recovery Charge	Q _{RR}				80		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

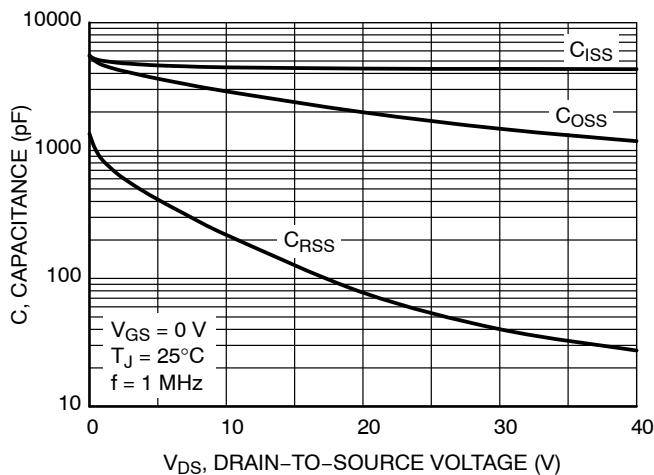


Figure 7. Capacitance Variation

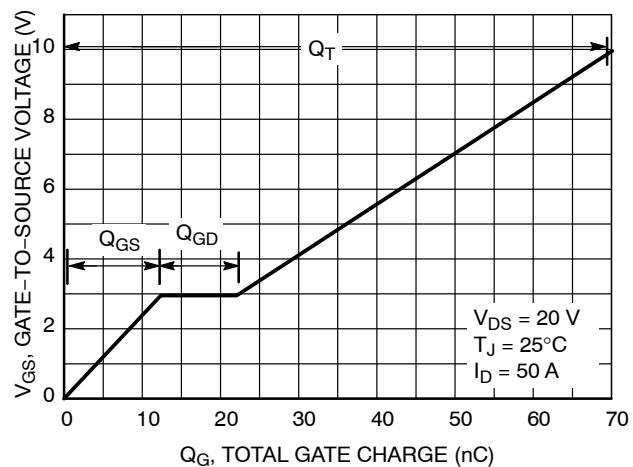


Figure 8. Gate-to-Source Voltage vs. Total Charge

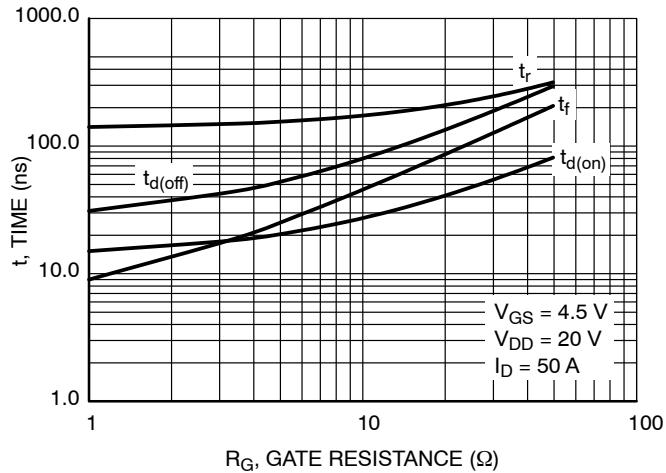


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

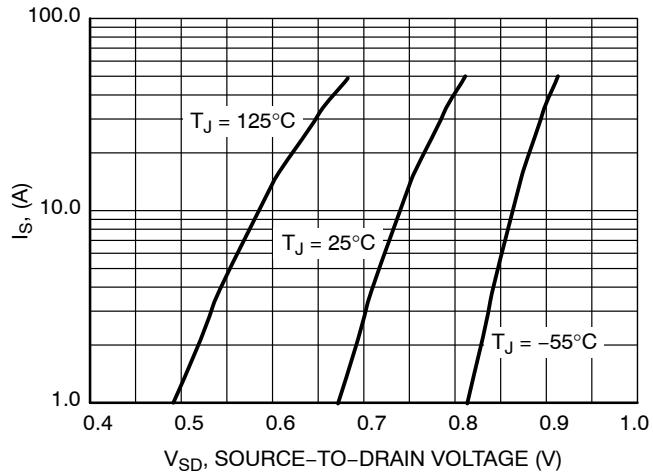


Figure 10. Diode Forward Voltage vs. Current

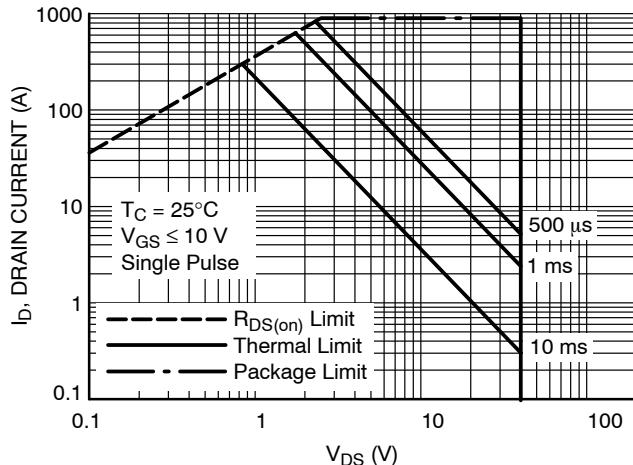
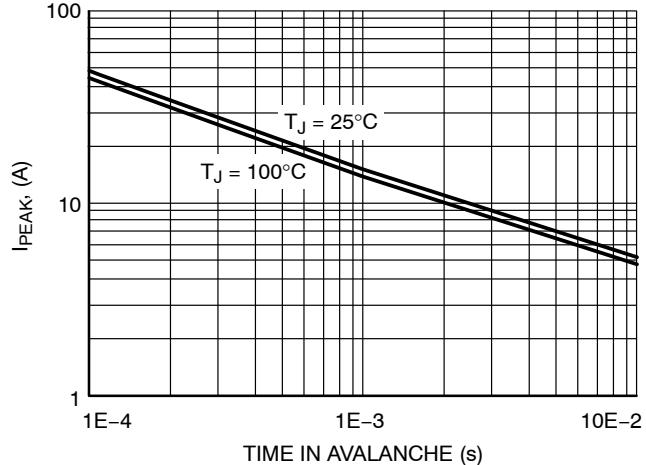


Figure 11. Safe Operating Area

Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

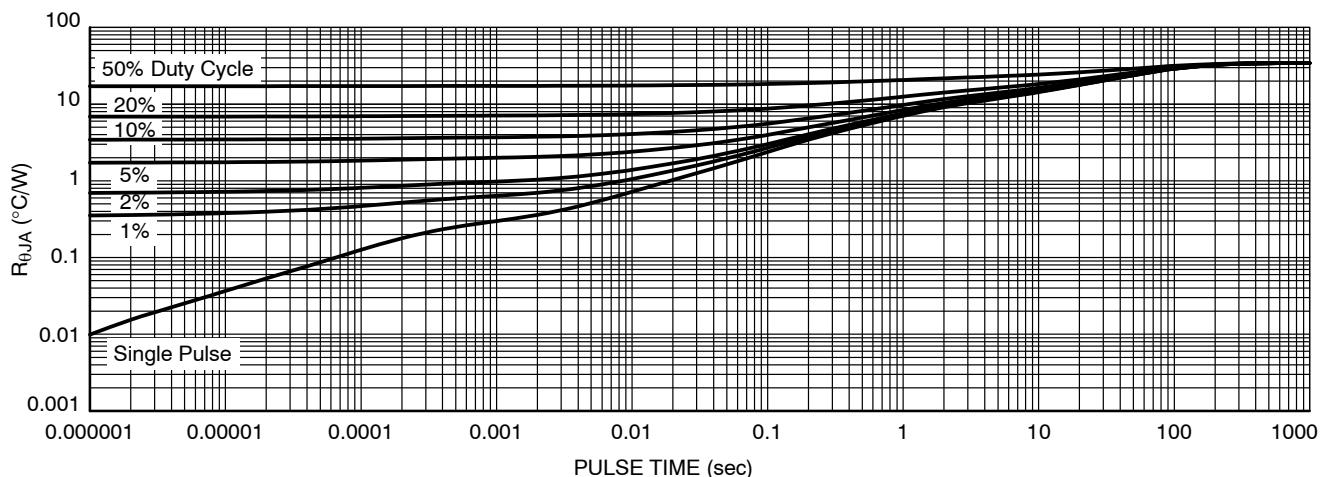


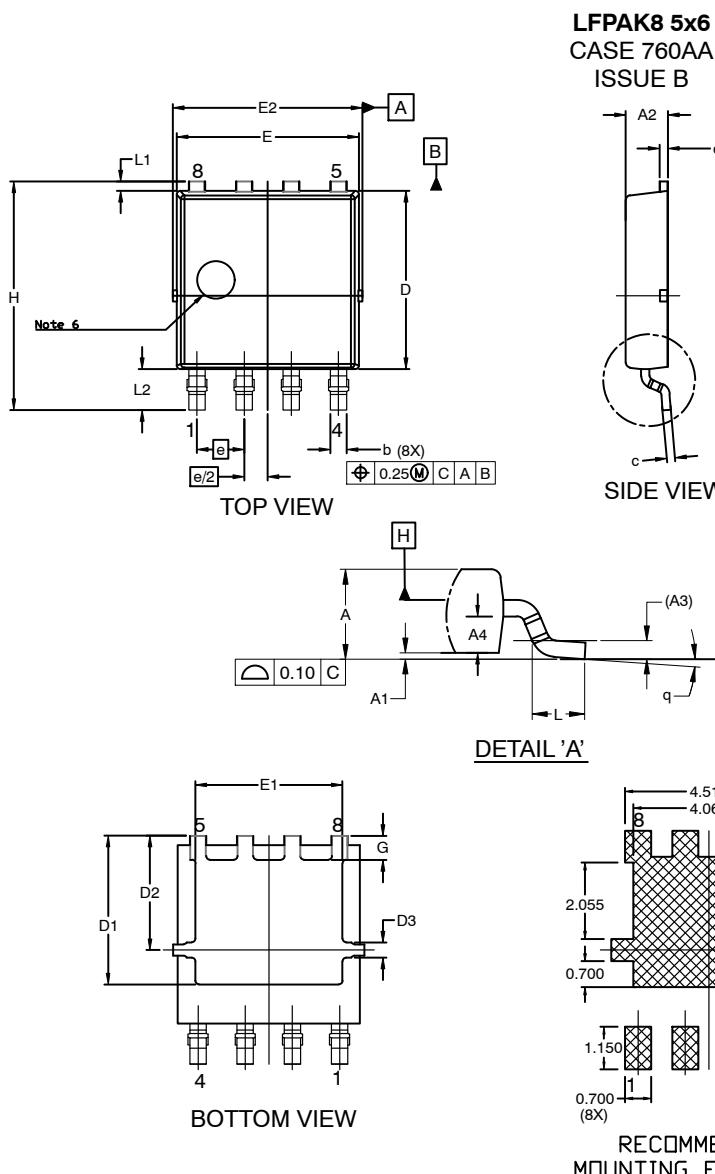
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMJS1D5N04CLTWG	1D5N04CL	LFPAK8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



LFPAK8 5x6
CASE 760AA
ISSUE B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 REF		
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	—	—	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
E	4.80	4.90	5.00
E1	3.90	4.00	4.10
E2	5.00	5.15	5.30
e	1.27 BSC		
G	0.55	0.65	0.75
H	6.00	6.15	6.30
L	0.40	0.65	0.85
L1	0.15	0.25	0.35
L2	0.80	1.05	1.30
q	0°	4°	8°

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERMM.

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