

# NTMFS5H419NL

## MOSFET – Power, Single, N-Channel 40 V, 2.1 mΩ, 155 A

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	40	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	$T_C = 25^\circ\text{C}$	$I_D$	155
			98
Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$	$P_D$	89
			36
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	$T_A = 25^\circ\text{C}$	$I_D$	29
			18
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	$T_A = 25^\circ\text{C}$	$P_D$	3.1
			1.3
Pulsed Drain Current	$I_{DM}$	900	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to + 150	°C
Source Current (Body Diode)	$I_S$	74	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 14$ A)	$E_{AS}$	375	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.4	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40	

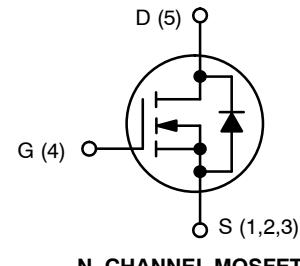
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



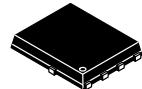
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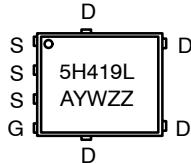
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
40 V	2.1 mΩ @ 10 V 3.1 mΩ @ 4.5 V	155 A



N-CHANNEL MOSFET



DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1



5H419L = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NTMFS5H419NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}}/T_J$				15.6		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 40 \text{ V}$	$T_J = 25^\circ\text{C}$		10		$\mu\text{A}$
			$T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = 20 \text{ V}$				100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250 \mu\text{A}$		1.2		2.0	V
Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})}/T_J$				-4.6		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$	$I_D = 20 \text{ A}$		1.7	2.1	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}$	$I_D = 20 \text{ A}$		2.5	3.1	
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = 15 \text{ V}, I_D = 20 \text{ A}$			80		S

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{\text{ISS}}$	$V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}, V_{\text{DS}} = 20 \text{ V}$		2900		pF
Output Capacitance	$C_{\text{OSS}}$			675		
Reverse Transfer Capacitance	$C_{\text{RSS}}$			37		
Output Charge	$Q_{\text{OSS}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DD}} = 20 \text{ V}$		29		nC
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$		$V_{\text{GS}} = 10 \text{ V}, V_{\text{DS}} = 20 \text{ V}; I_D = 20 \text{ A}$	45		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$			21		
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			4.8		
Gate-to-Source Charge	$Q_{\text{GS}}$			8.6		
Gate-to-Drain Charge	$Q_{\text{GD}}$			5.4		
Plateau Voltage	$V_{\text{GP}}$			3		V

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{\text{d}(\text{ON})}$	$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DS}} = 20 \text{ V}, I_D = 20 \text{ A}, R_G = 2.5 \Omega$		24		ns
Rise Time	$t_r$			56		
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$			62		
Fall Time	$t_f$			15		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{\text{SD}}$	$V_{\text{GS}} = 0 \text{ V}, I_S = 20 \text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	$t_{\text{RR}}$	$V_{\text{GS}} = 0 \text{ V}, dI_S/dt = 100 \text{ A}/\mu\text{s}, I_S = 20 \text{ A}$			40		ns
Charge Time	$t_a$				23		
Discharge Time	$t_b$				17		
Reverse Recovery Charge	$Q_{\text{RR}}$				38		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

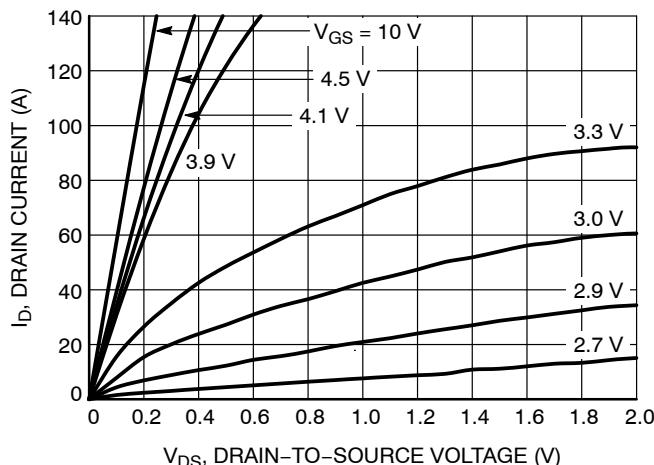


Figure 1. On-Region Characteristics

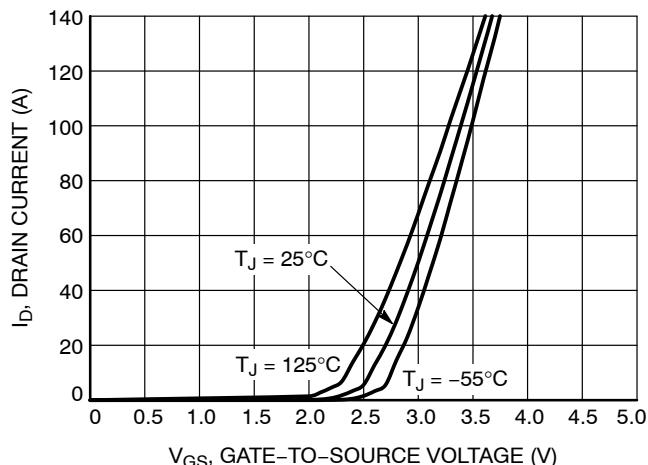


Figure 2. Transfer Characteristics

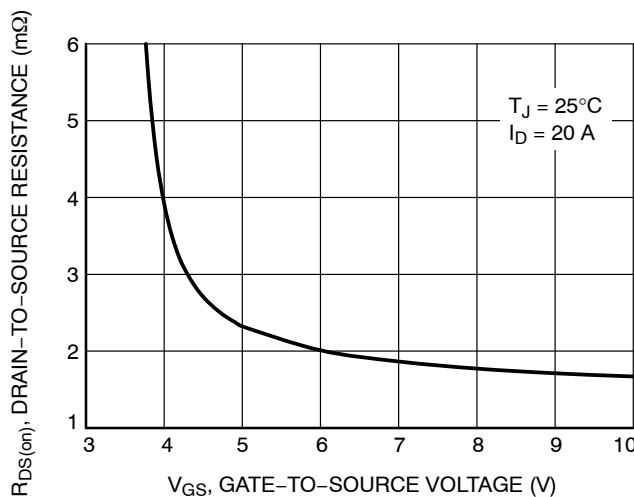


Figure 3. On-Resistance vs. Gate-to-Source Voltage

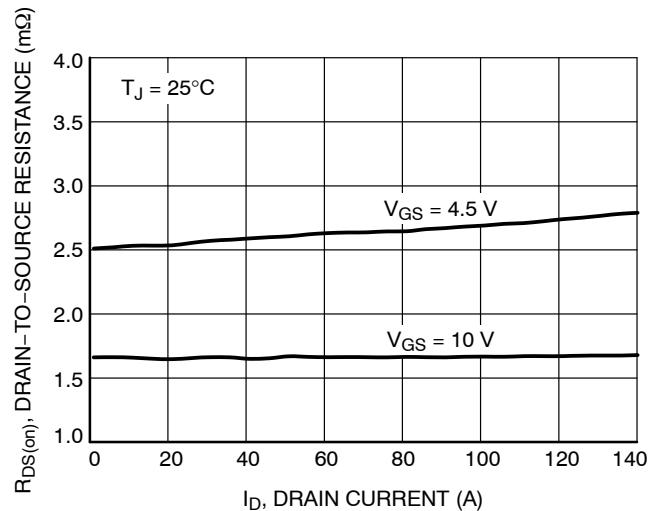


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

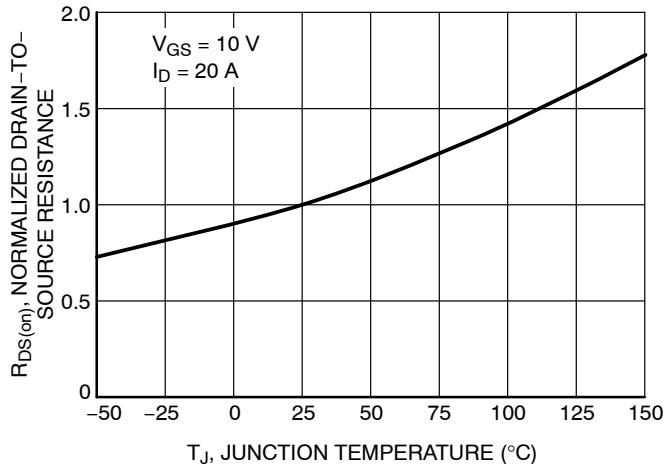


Figure 5. On-Resistance Variation with Temperature

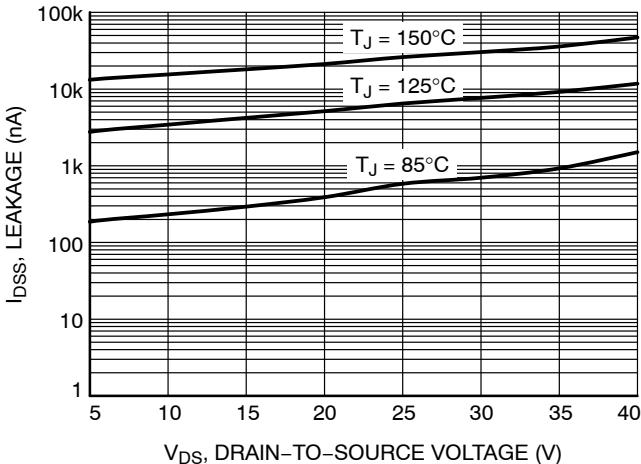


Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL CHARACTERISTICS

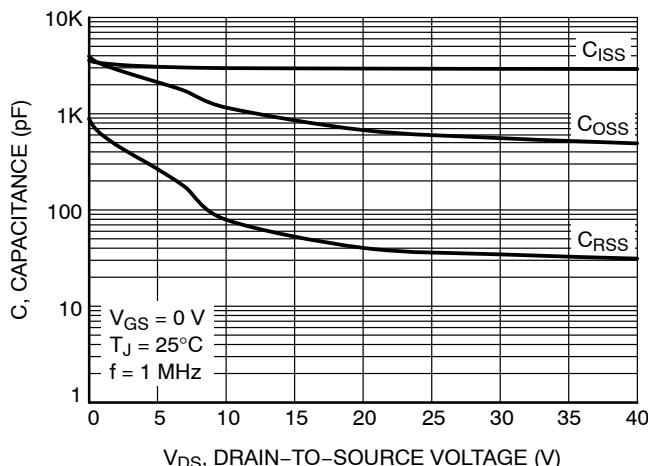


Figure 7. Capacitance Variation

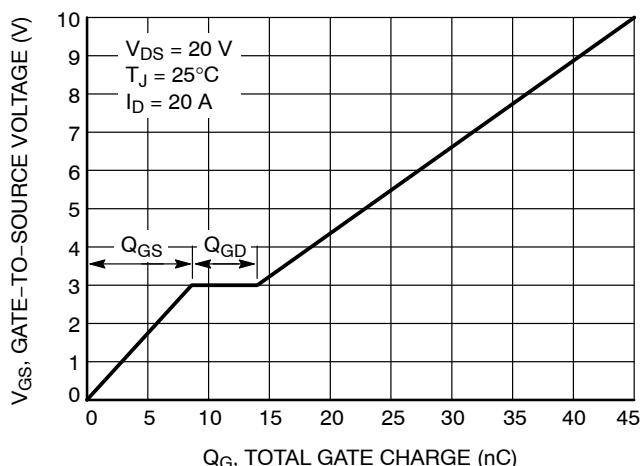


Figure 8. Gate-to-Source vs. Total Charge

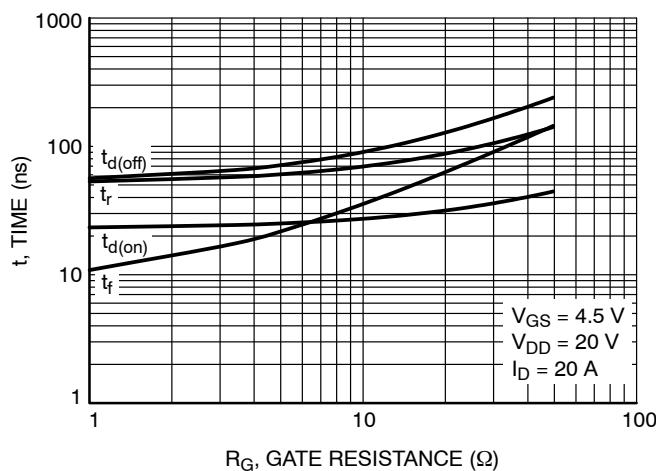


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

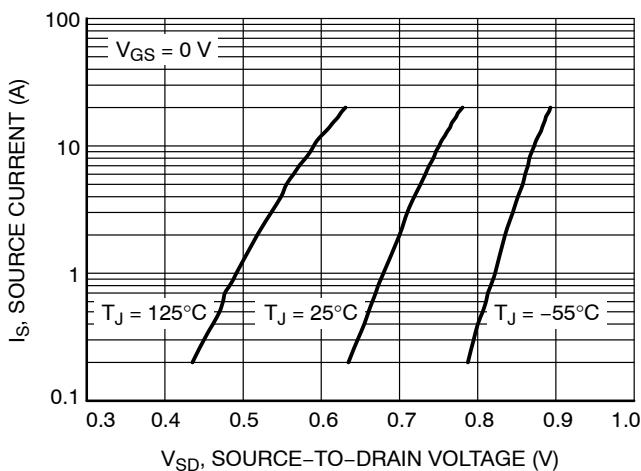


Figure 10. Diode Forward Voltage vs. Current

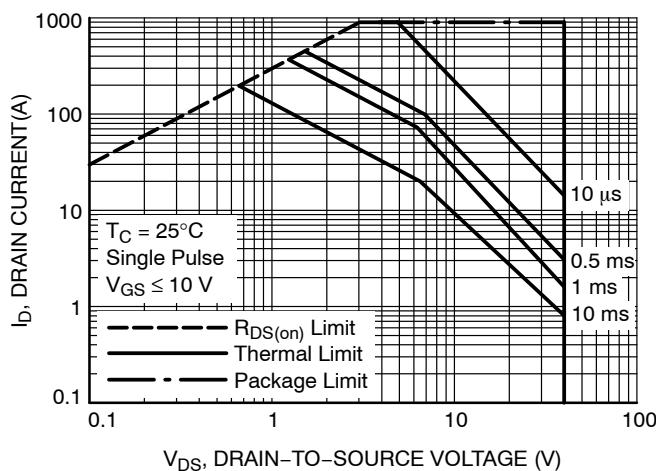
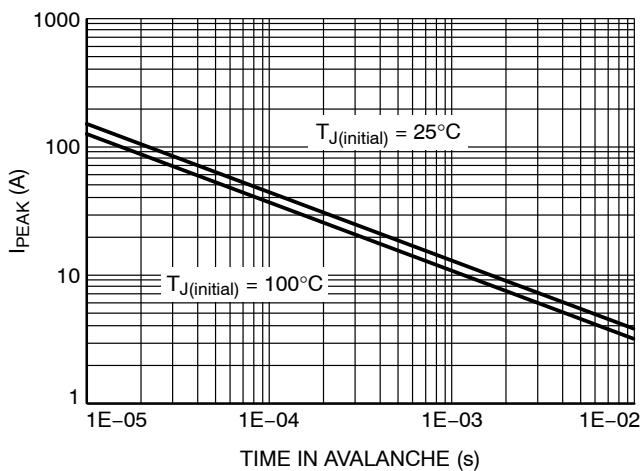


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

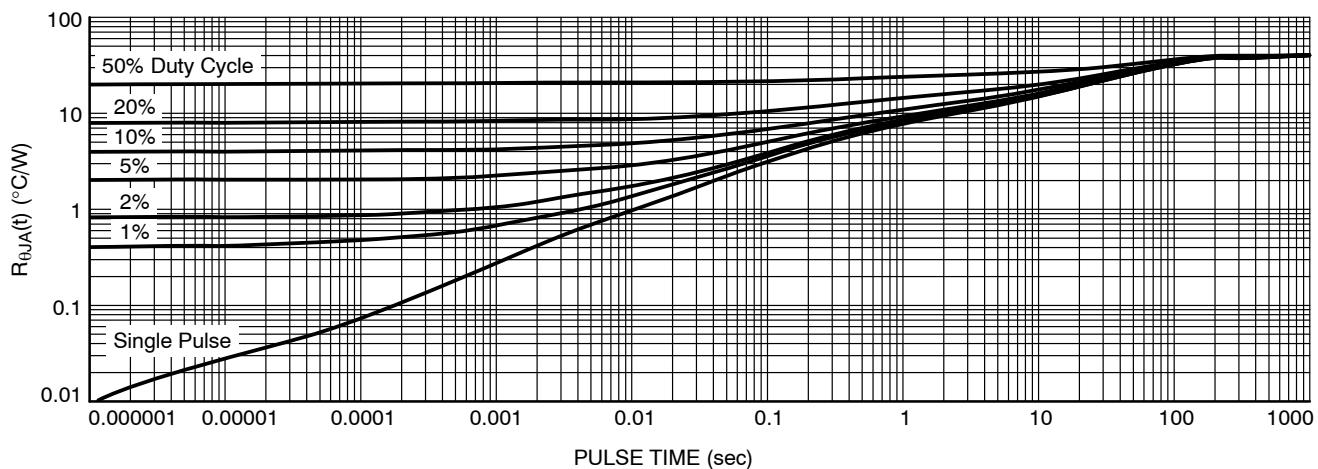


Figure 13. Thermal Characteristics

## DEVICE ORDERING INFORMATION

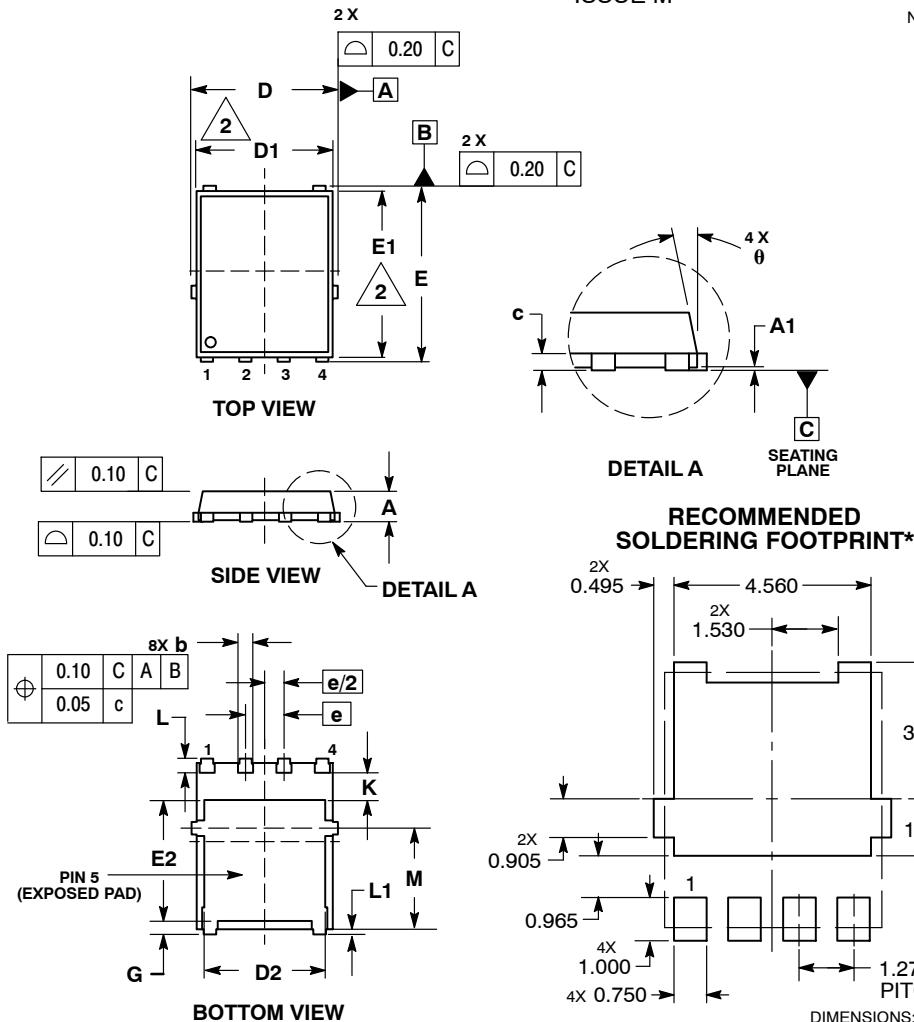
Device	Marking	Package	Shipping <sup>†</sup>
NTMFS5H419NLT1G	5H419L	DFN5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS5H419NL

## PACKAGE DIMENSIONS

**DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE M**

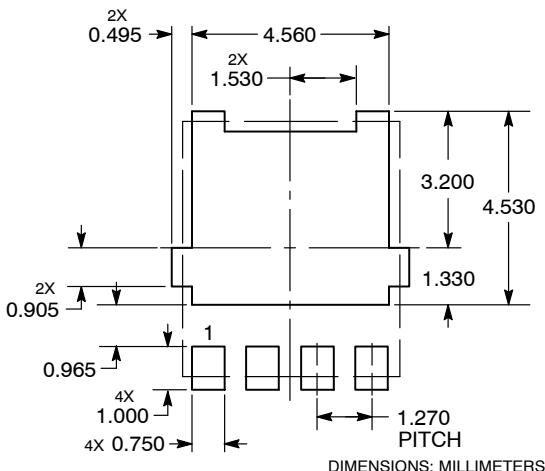


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
$\theta$	0 °	---	12 °

STYLE 1:  
 1. PIN 1. SOURCE  
 2. SOURCE  
 3. SOURCE  
 4. GATE  
 5. DRAIN



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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