MOSFET - Power, Single N-Channel, STD Gate, u8FL

40 V, 2.85 mΩ, 98 A

NVTFWS003N04XM

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	2.85 mΩ @ 10 V	98 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	98	A
	T_C = 100°C		69	
Power Dissipation	T_C = 25°C	P_D	52	W
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs	I_D	570	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Continuous Source-Drain Current (Body Diode)		I_S	66	A
Single Pulse Avalanche Energy (I_{PK} = 5 A)		E_{AS}	168	mJ
Lead Temperature for Soldering Purposes		T_L	260	°C

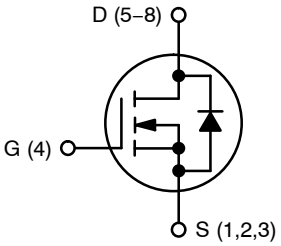
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

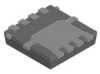
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.9	°C/W
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	48	

1. Surface mounted on FR4 board using 650 mm^2, 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

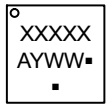
N-CHANNEL MOSFET





WDFNW8
(Full−Cut μ8FL WF)
CASE 515AN

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	40	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C	–	15	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, T_J = 25°C	–	–	1	μA
		V_{DS} = 40 V, T_J = 125°C	–	–	20	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A, T_J = 25°C	–	2.4	2.85	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 40 μA, T_J = 25°C	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 40 μA	–	7	–	mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 8 A	–	44	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	1042	–	pF
Output Capacitance	C_{OSS}		–	675	–	
Reverse Transfer Capacitance	C_{RSS}		–	14	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 32 V, I_D = 8 A, V_{GS} = 10 V	–	16	–	nC
Threshold Gate Charge	$Q_{G(TH)}$		–	3	–	
Gate-to-Source Charge	Q_{GS}		–	5	–	
Gate-to-Drain Charge	Q_{GD}		–	3	–	
Gate Resistance	R_G	f = 1 MHz	–	0.9	–	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 10 V, V_{DD} = 32 V, I_D = 8 A, R_G = 0 Ω	–	6	–	ns
Rise Time	t_r		–	9	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	9	–	
Fall Time	t_f		–	10	–	
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_S = 8 A, V_{GS} = 0 V, T_J = 25°C	–	0.78	1.2	V
		I_S = 8 A, V_{GS} = 0 V, T_J = 125°C	–	0.62	–	
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 8 A, dI/dt = 100 A/μs, V_{DD} = 32 V	–	59	–	ns
Charge Time	t_a		–	11	–	
Discharge Time	t_b		–	47	–	
Reverse Recovery Charge	Q_{RR}		–	24	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

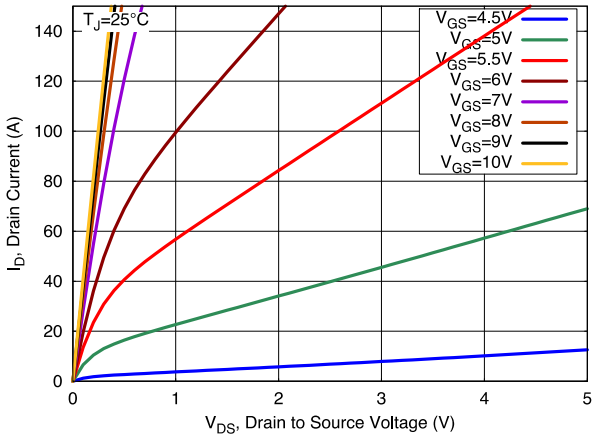


Figure 1. On-Region Characteristics

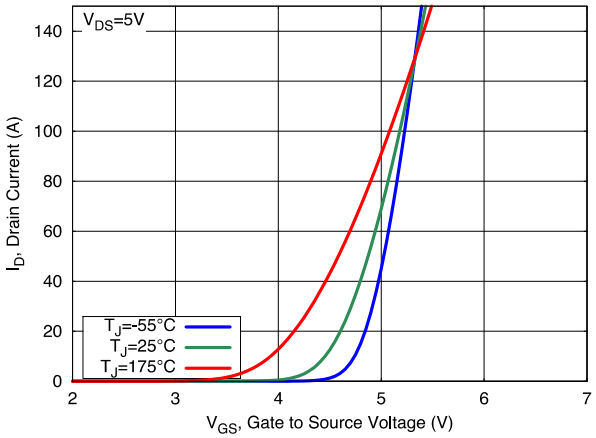


Figure 2. Transfer Characteristics

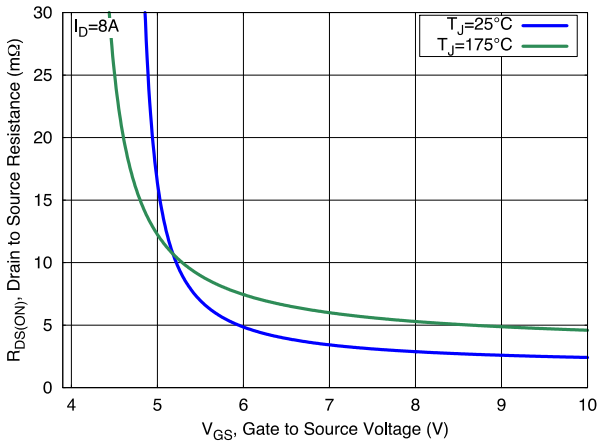


Figure 3. On-Resistance vs. Gate Voltage

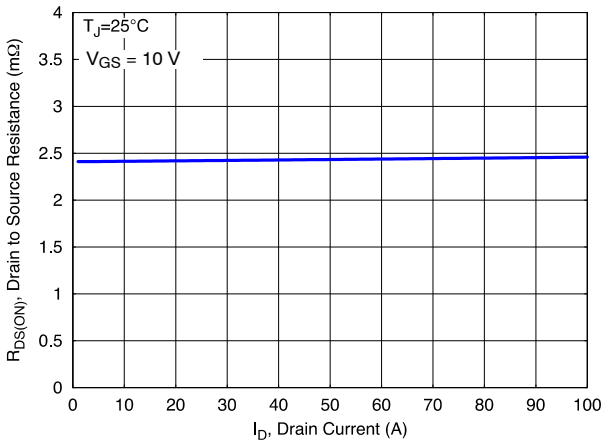


Figure 4. On-Resistance vs. Drain Current

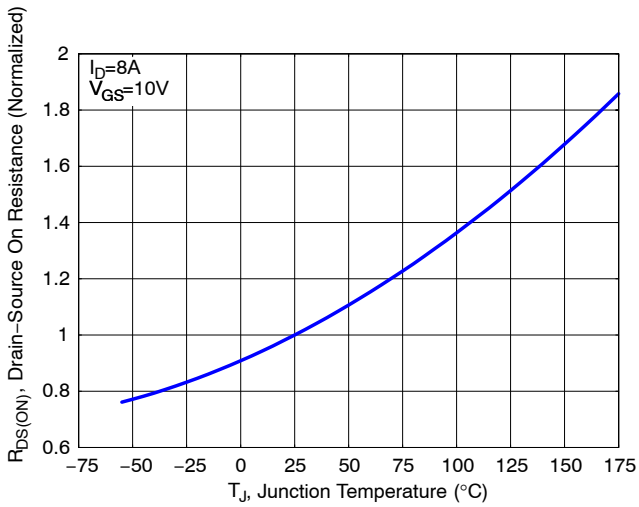


Figure 5. Normalized ON Resistance vs. Junction Temperature

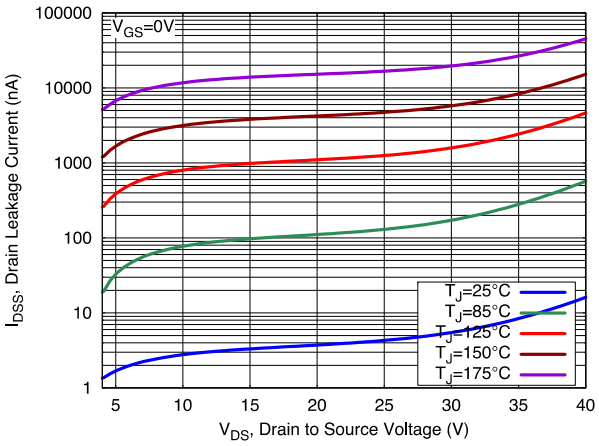


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

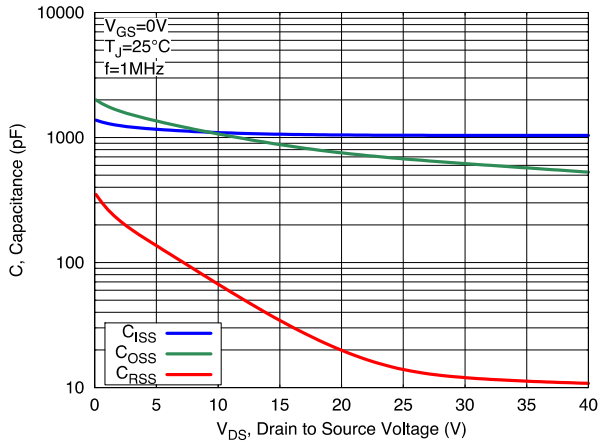


Figure 7. Capacitance Characteristics

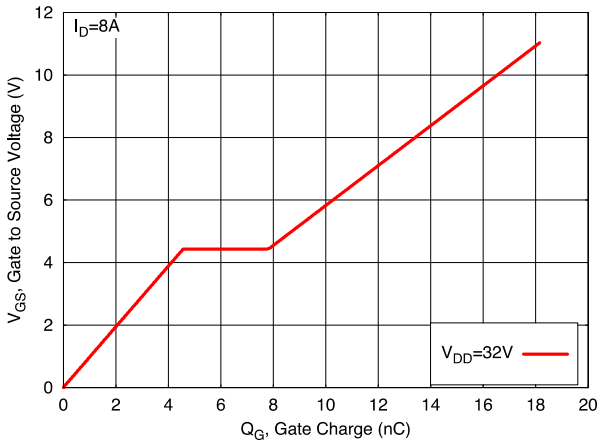


Figure 8. Gate Charge Characteristics

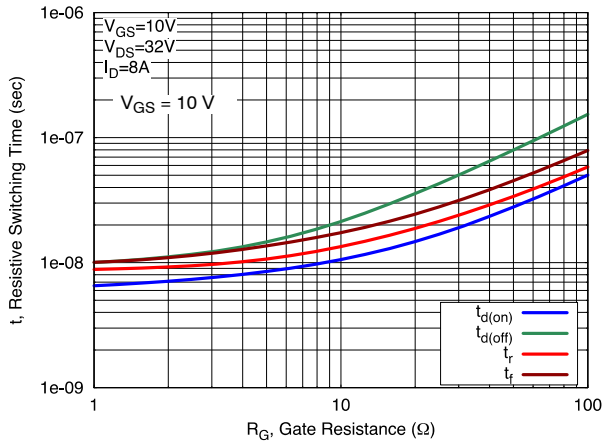


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

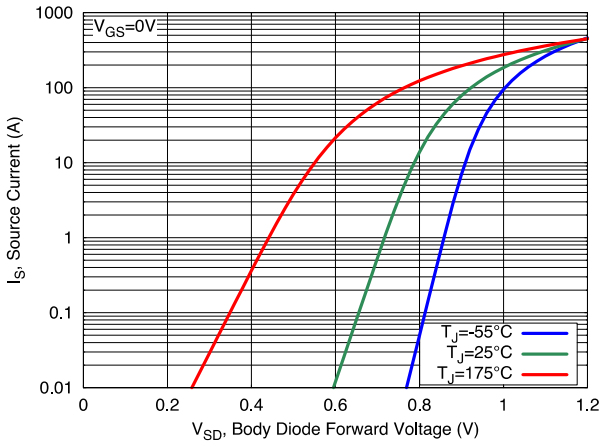


Figure 10. Diode Forward Characteristics

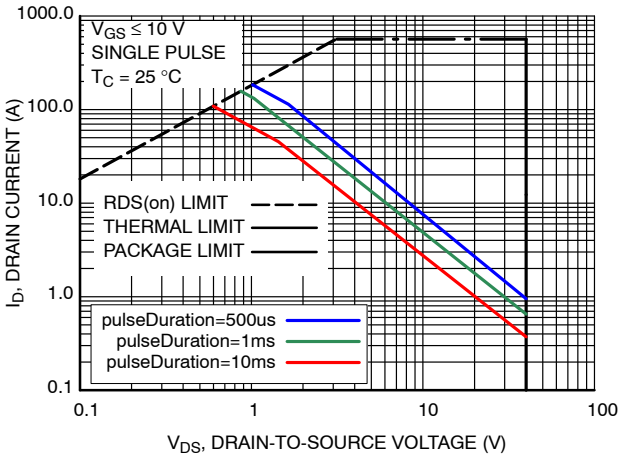


Figure 11. Safe Operating Area (SOA)

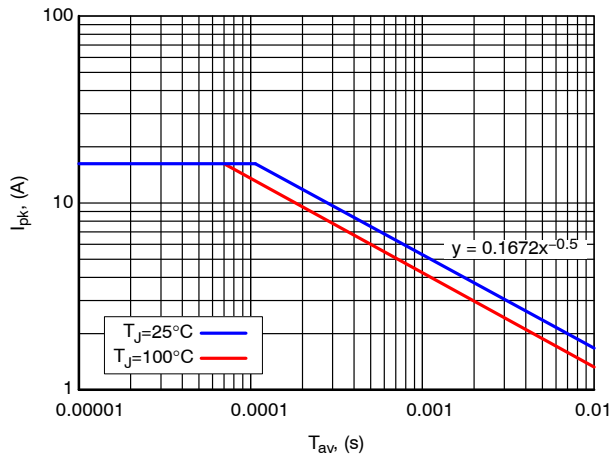


Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS

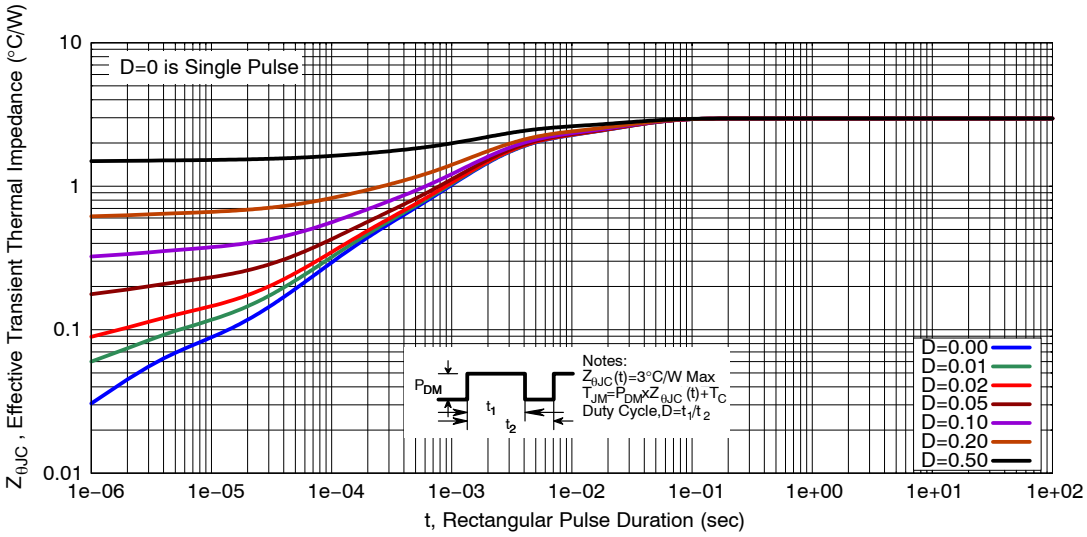


Figure 13. Transient Thermal Response

ORDERING INFORMATION

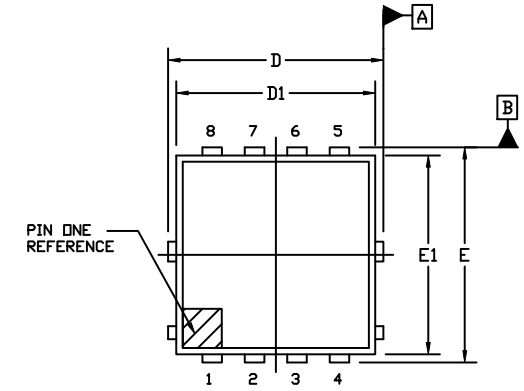
Device	Marking	Package Type	Shipping†
NVTFWS003N04XMTAG	003W	WDFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

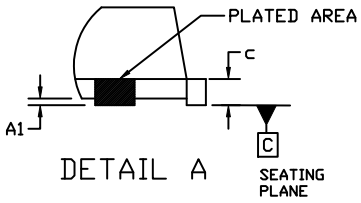
NVTFWS003N04XM

PACKAGE DIMENSIONS

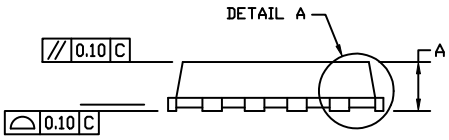
WDFNW8 3.3x3.3, 0.65P (Full−Cut μ8FL WF)
CASE 515AN
ISSUE O



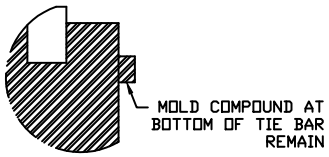
TOP VIEW



DETAIL A



SIDE VIEW

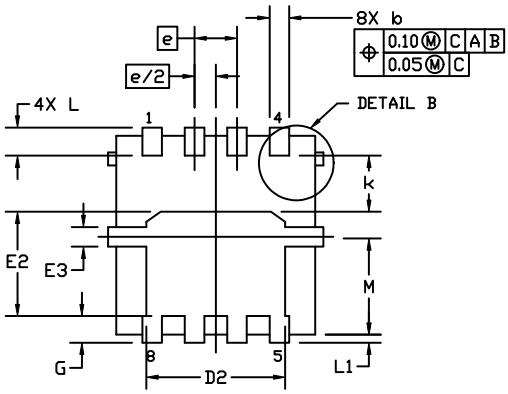


DETAIL B

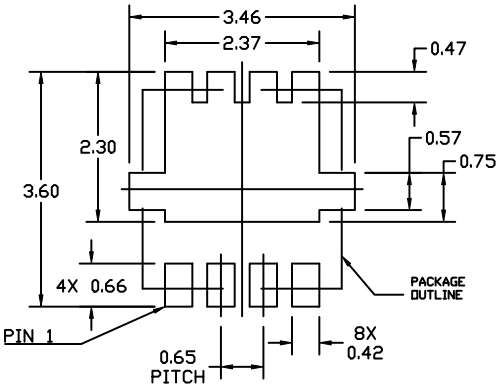
NOTES:

1. DIMENSIONING AND TOLERANCING PER.ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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