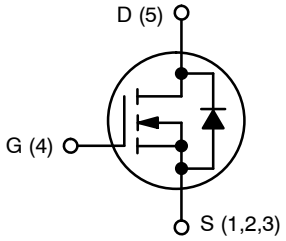
MOSFET - Power, Single N-Channel, STD Gate, SO8FL

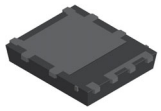
40 V, 0.45 mΩ, 469 A

NVMFWS0D45N04XM

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	0.45 mΩ @ V_{GS} = 10 V	469 A



N−CHANNEL MOSFET



DFNW5
S08FL WF
CASE 507BD

Features

- Low RDS(on) to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AECQ101 Qualified and PPAP Capable
- These Devices are PbFree, Halogen Free,BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

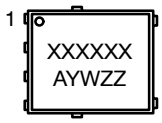
Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	40	V
Gate−to−Source Voltage	DC	V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	469	A
	T_C = 100°C		331	
Power Dissipation	T_C = 25°C	P_D	180	W
Pulsed Drain Current	T_C = 25°C, t_P = 10 μs	I_D	900	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)		I_S	260	A
Single Pulse Avalanche Energy (I_{PK} = 33.5 A)		E_{AS}	1040	mJ
Lead Temperature for Soldering Purposes		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance − Junction−to−Case	$R_{\theta JC}$	0.83	°C/W
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	38.5	

MARKING DIAGRAM



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, T_J = 25°C			1	μA
		V_{DS} = 40 V, T_J = 125°C			75	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A, T_J = 25°C		0.39	0.45	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 290 μA, T_J = 25°C	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 290 μA		−7		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 50 A		278		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		7374		pF
Output Capacitance	C_{OSS}			4696		
Reverse Transfer Capacitance	C_{RSS}			65		
Total Gate Charge	$Q_{G(tot)}$	V_{DD} = 32 V, I_D = 50 A, V_{GS} = 10 V		115		nC
Threshold Gate Charge	$Q_{G(th)}$			22		
Gate−to−Source Charge	Q_{GS}			32		
Gate−to−Drain Charge	Q_{GD}			22		
Gate Resistance	R_G	f = 1 MHz		0.53		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	Resistive Load V_{GS} = 0/10 V, V_{DD} = 32 V, I_D = 50 A, R_G = 0 Ω		11		ns
Turn−Off Delay Time	$t_{d(off)}$			46		
Rise Time	t_r			17		
Fall Time	t_f			5		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A, T_J = 25°C		0.77	1.2	V
		V_{GS} = 0 V, I_S = 50 A, T_J = 125°C		0.61		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 50 A, dI/dt = 100 A/μs, V_{DD} = 32 V		89		ns
Charge Time	T_A			49		
Discharge Time	T_B			40		
Reverse Recovery Charge	Q_{RR}			267		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

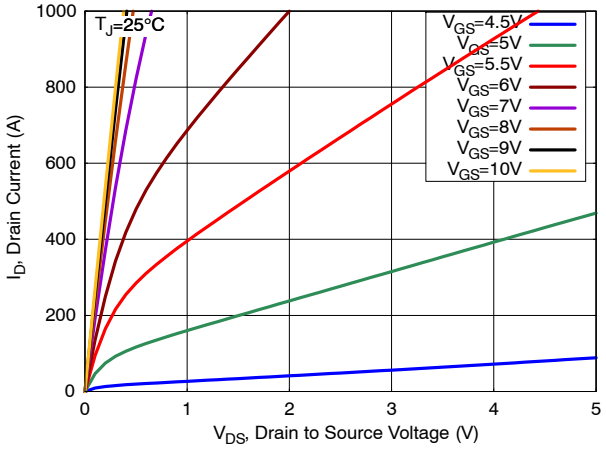


Figure 1. On−Region Characteristics

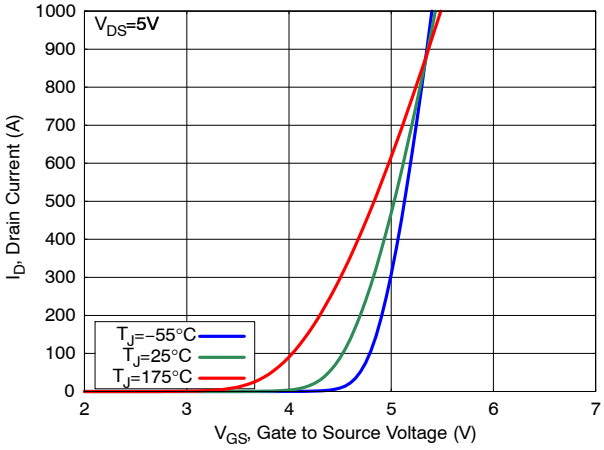


Figure 2. Transfer Characteristics

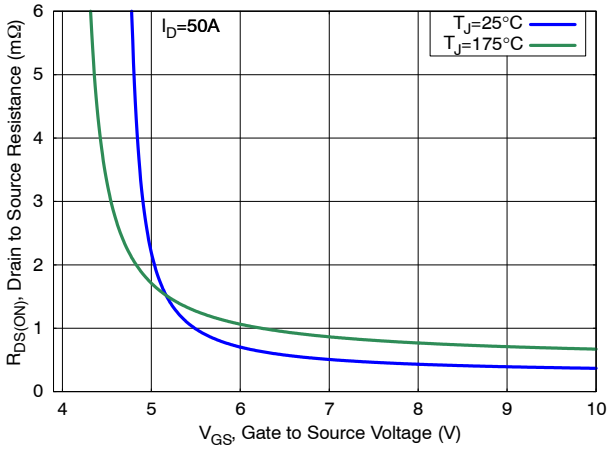


Figure 3. On−Resistance vs. Gate Voltage

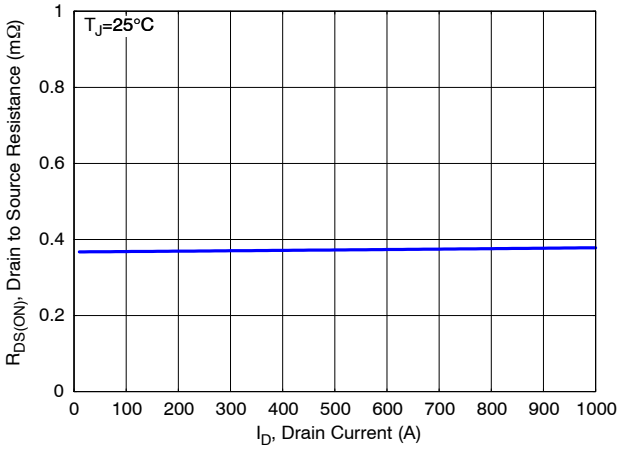


Figure 4. On−Resistance vs. Drain Current

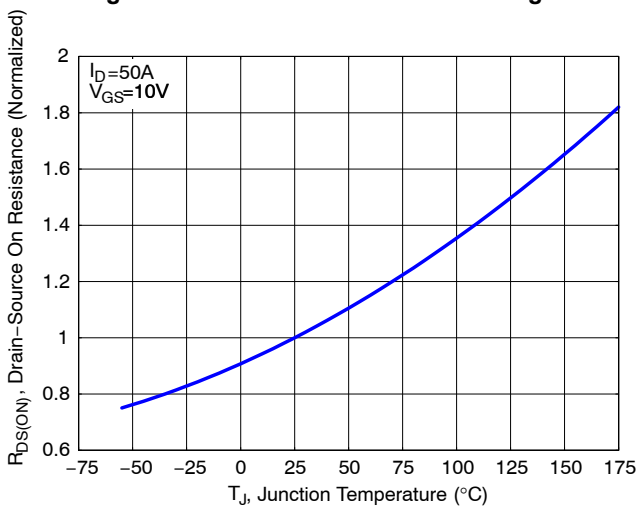


Figure 5. Normalized On−Resistance vs. Junction Temperature

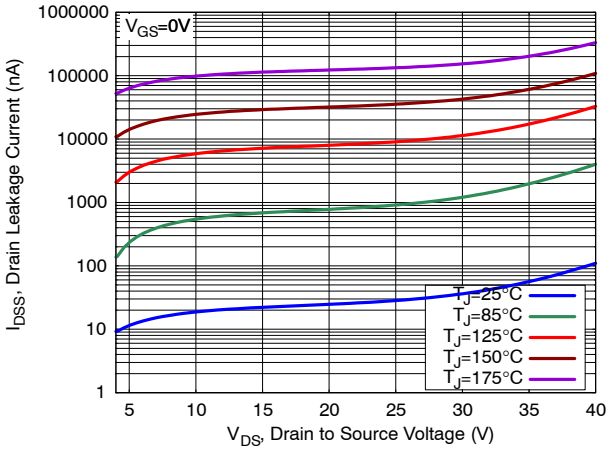


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

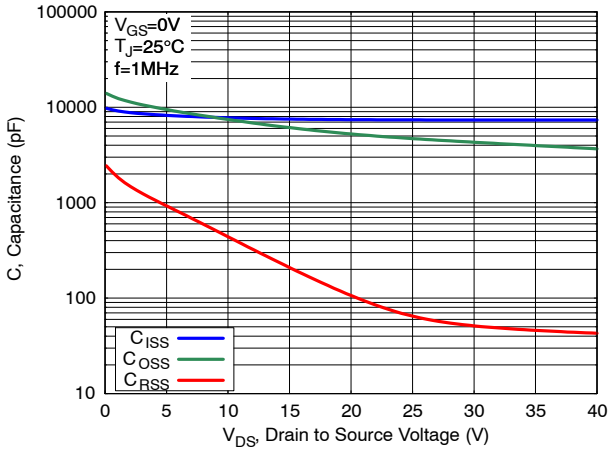


Figure 7. Capacitance Characteristics

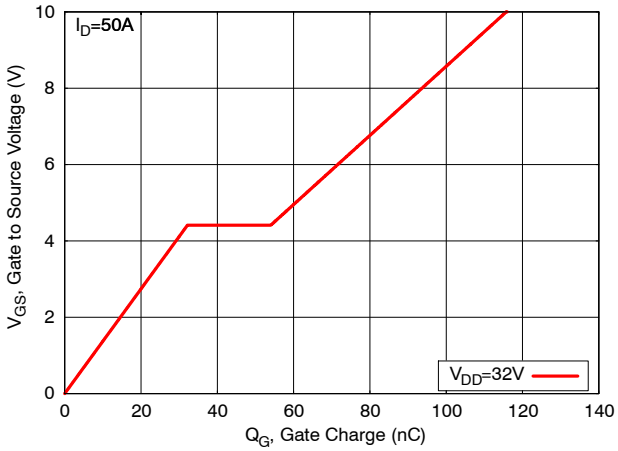


Figure 8. Gate Charge Characteristics

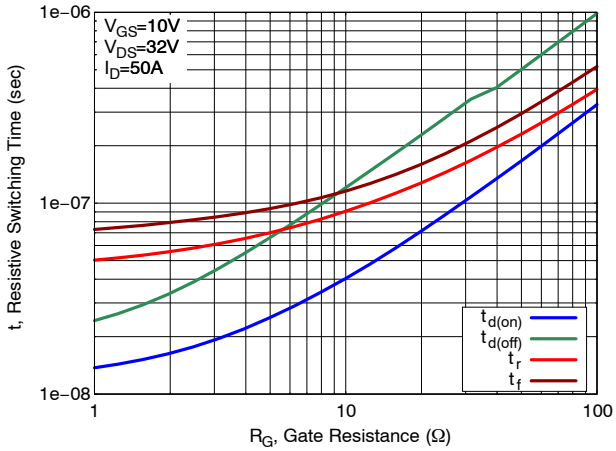


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

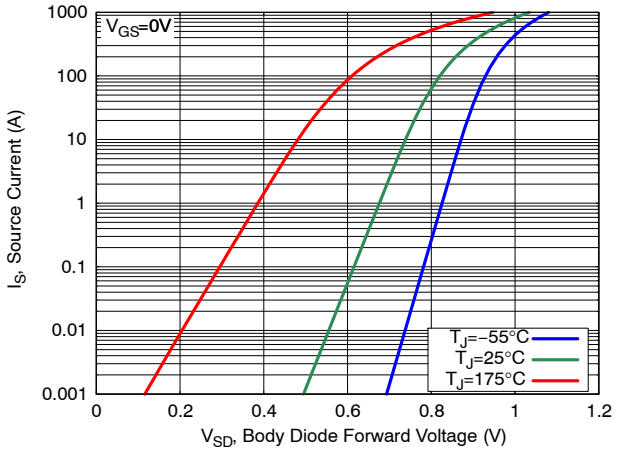


Figure 10. Diode Forward Characteristics

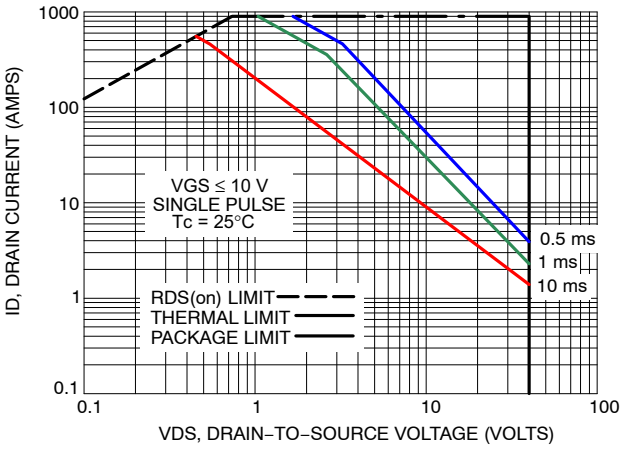


Figure 11. Maximum Rated Forward Biased Safe Operating Area

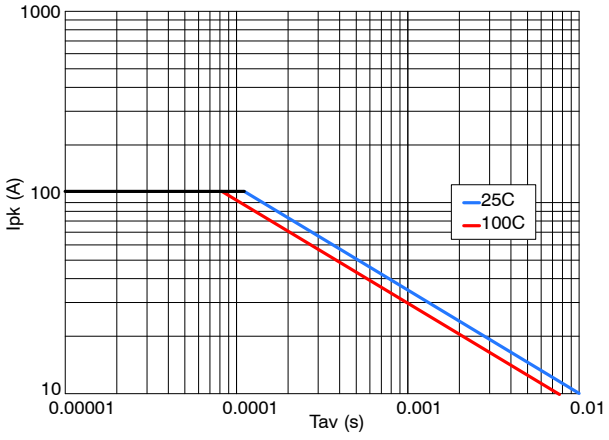


Figure 12. UIS

TYPICAL CHARACTERISTICS

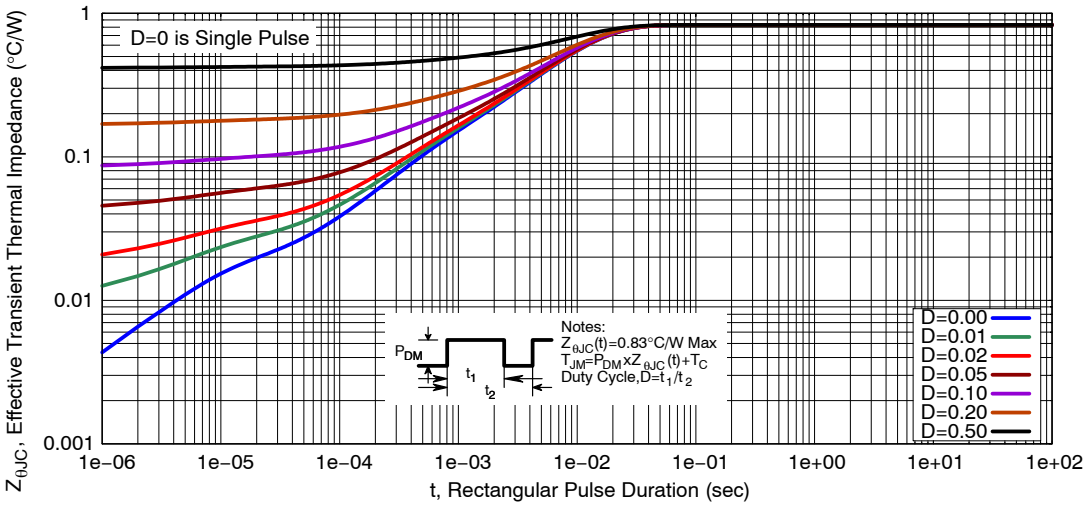
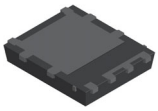


Figure 13. Transient Thermal Response

DEVICE ORDERING INFORMATION

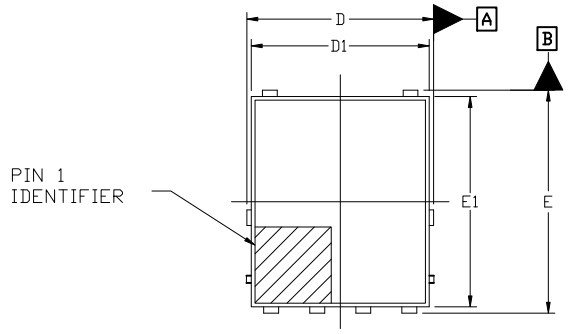
Device	Marking	Package	Shipping†
NVMFWS0D45N04XMT1G	045N4W	DFNW5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

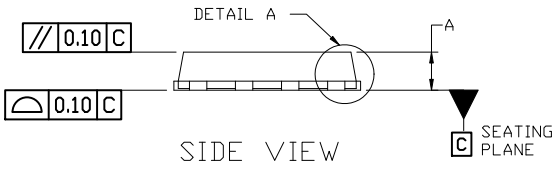


DFNW5 5x6, FULL−CUT SO8FL WF
CASE 507BD
ISSUE O

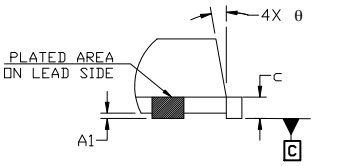
DATE 13 APR 2021



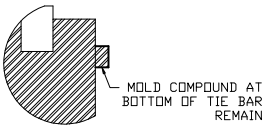
TOP VIEW



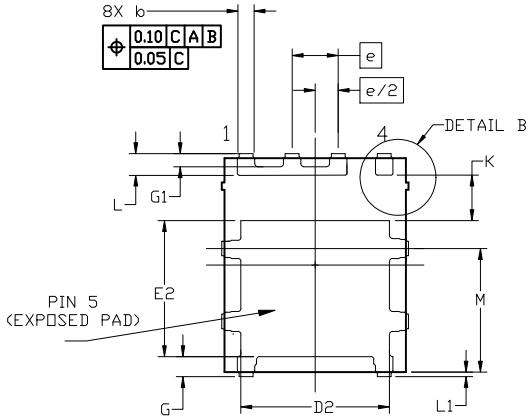
SIDE VIEW



DETAIL A



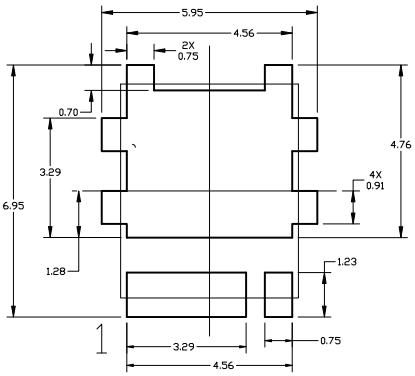
DETAIL B



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.80	5.00	5.20
D2	3.90	4.10	4.30
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.55	3.75	3.95
e	1.27 BSC		
G	0.50	0.55	0.70
G1	0.26	0.36	0.46
k	1.10	1.25	1.40
L	0.50	0.60	0.70
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW5 5x6, FULL−CUT SO8FL WF**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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