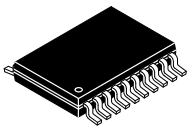
Synchronous Buck Controller, Automotive Grade

NCV8856A



TSSOP−20
SUFFIX DB
CASE 948E

The NCV8856A is an adjustable output, synchronous buck controller, which drives dual N−channel MOSFETs, ideal for high power applications. Average current mode control is employed for very fast transient response and tight regulation over wide input voltage and output load ranges. The IC incorporates an internal fixed 6.0 V low−dropout linear regulator (LDO), which supplies charge to the switch mode power supply's (SMPS) bottom gate driver, limiting the power lost to excess gate drive. The IC is designed for operation over an input voltage range of 4.5 V to 38 V and is capable of 10 to 1 voltage conversion at 500 kHz.

Additional controller features include undervoltage lockout, overvoltage shutdown, internal soft−start, low quiescent current sleep mode, programmable frequency, SYNC function, average current limiting, cycle−by−cycle overcurrent protection and thermal shutdown.

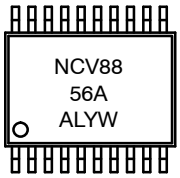
Features

- Average Current Mode Control
- 0.8 V ±2% Reference Voltage
- Wide Input Voltage Range of 4.5 V to 38 V
- Operates through Load Dump Conditions
- 6.0 V Low−dropout Linear Regulator (LDO)
- Input UVLO (Undervoltage Lockout)
- Internal Soft−start
- 6.2 μA Maximum Quiescent Current in Sleep Mode
- Adaptive Non−overlap Circuitry
- 180 ns Minimum High−side Gate Off−time
- Programmable Fixed Frequency – 170 kHz to 500 kHz
- External Clock Synchronization up to 600 kHz
- Average Current Limiting (ACL)
- Cycle−by−Cycle Overcurrent Protection (OCP)
- Thermal Shutdown (TSD)
- This is a Pb−Free Device

Applications

- Automotive Systems Requiring High Current
- Pre−regulated Supply for Low−voltage SMPSs and LDOs

MARKING DIAGRAM



NCV8856A = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCV8856ADBR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

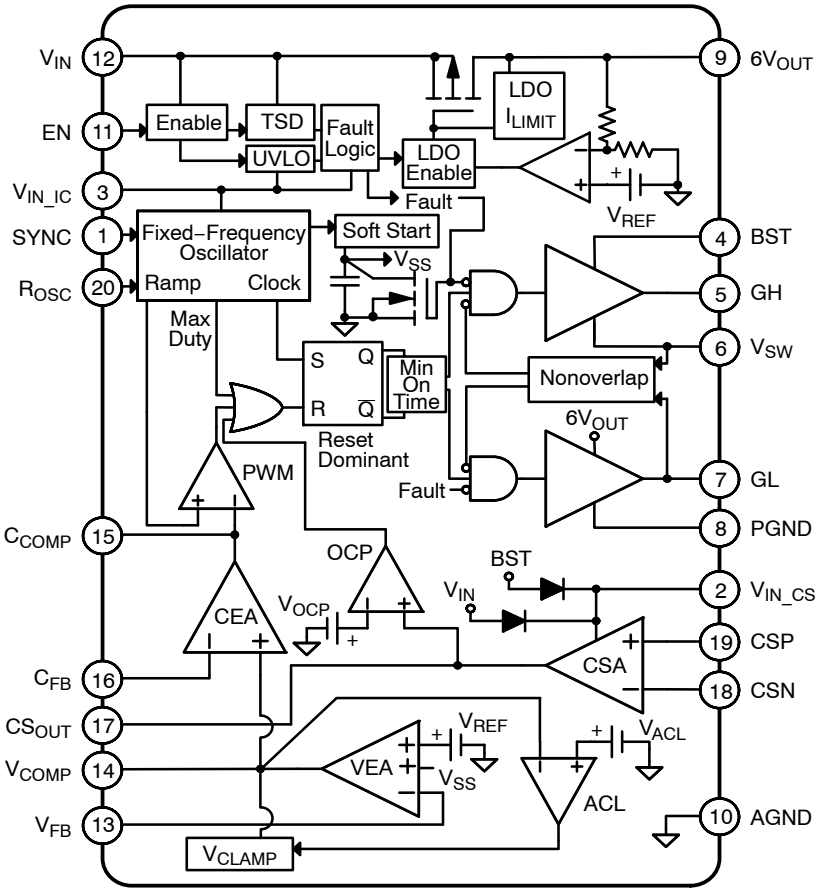


Figure 1. Functional Block Diagram

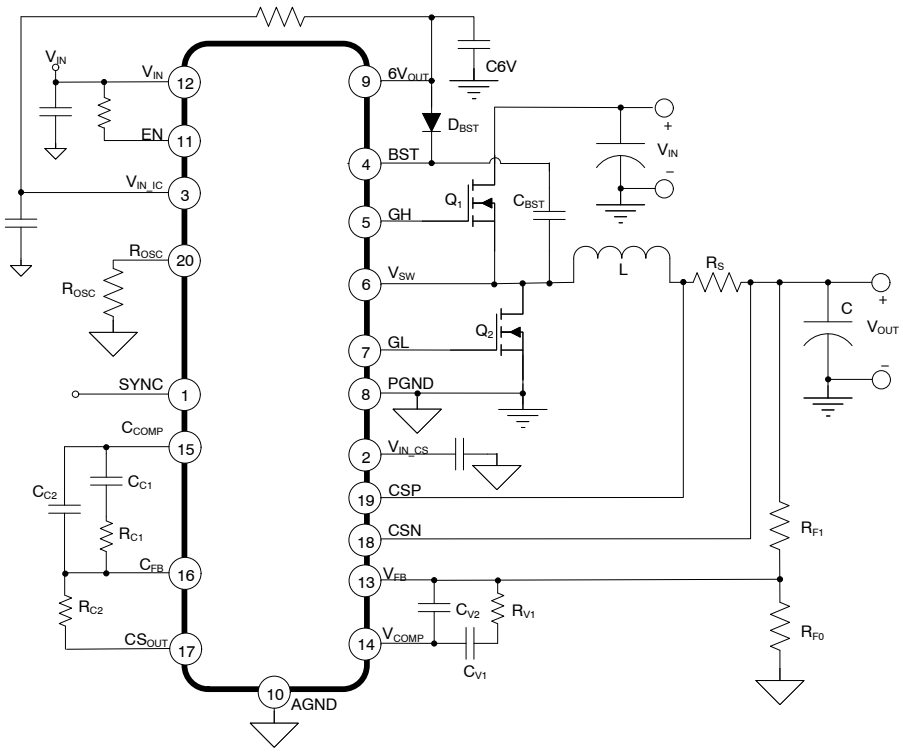


Figure 2. Application Schematic

Note: This part is recommended for synchronous use only.

PACKAGE PIN DESCRIPTIONS – 20 Lead TSSOP

Package Pin#	Pin Symbol	Function
1	SYNC	External clock synchronization input.
2	V_{IN_CS}	Supply input for the internal current sense amplifier.
3	V_{IN_IC}	Supply input for internal logic and analog circuitry.
4	BST	Supply input for the floating top gate driver. An external diode, D_{BST}, from $6V_{OUT}$ and a 0.1 μF to 1 μF capacitor, C_{BST}, to V_{SW} forms a boost circuit.
5	GH	Gate driver output for the external high−side NMOS FET.
6	V_{SW}	Switch−node. This pin connects to the source of the high−side MOSFET and drain of the low−side MOSFET.
7	GL	Gate driver output for the external low−side NMOS FET.
8	PGND	Power Ground. Ground reference for the high−current LS FET gate drive.
9	$6V_{OUT}$	Output of internal fixed 6.0 V LDO.
10	AGND	Analog Ground. Ground reference for the internal logic and analog circuitry as well as R_{OSC} and the compensators.
11	EN	Enable input. When disabled, the LDO, internal logic and analog circuitry and gate drivers enter sleep mode, drawing under 1 μA.
12	V_{IN}	Supply input for the SMPS.
13	V_{FB}	SMPS's voltage feedback. Inverting input to the voltage error amplifier. Connect to V_{OUT} through a resistive divider.
14	V_{COMP}	SMPS's voltage error amplifier output and non−inverting input to the current error amplifier.
15	C_{COMP}	SMPS's current error amplifier output and inverting input to the PWM comparator.
16	C_{FB}	SMPS's current feedback. Inverting input to the current error amplifier.
17	CS_{OUT}	Single−ended output of the differential current sense amplifier. Connect to C_{FB} through a resistor. Non−inverting input to the cycle−by−cycle overcurrent comparator.
18	CSN	Differential current sense amplifier inverting input.
19	CSP	Differential current sense amplifier non−inverting input.
20	R_{OSC}	Oscillator's frequency adjust pin. Resistor to ground sets the oscillator frequency.

MAXIMUM RATINGS (Voltages are with respect to GND unless otherwise indicated.) (Note 1)

Rating	Symbol	Value	Unit
Dc Supply Voltage Peak Transient Voltage (Load Dump, EN = 0 V)	EN, V_{IN}	−0.3 to 40 45	V
Dc Supply Voltage	V_{IN_IC}	6.5	V
Pin Voltage t ≤ 50 ns	V_{SW}	−0.3 to 38 −2	V
Pin Voltage	V_{IN_CS}	−0.3 to 44	V
Pin Voltage	BST, GH	−0.3 to 44 −0.3 to 6 wrt V_{SW}	V
Pin Voltage	GL	−0.3 to 7 wrt PGND	V
Pin Voltage	CSP, CSN	−0.3 to 10	V
Pin Voltage	V_{FB}, V_{COMP}, CS_{OUT}, C_{FB}, C_{COMP}, R_{OSC}	−0.3 to 3.6	V
Pin Voltage	SYNC	−0.3 to 6	V
Pin Voltage	$6V_{OUT}$	−0.3 to 7	V
Operating Junction Temperature	$T_{J(max)}$	−40 to 150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	1.5	kV
Moisture Sensitivity Level	MSL	1	
Lead Soldering Temperature Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics (Note 4) Thermal Resistance, Junction−to−Ambient (Note 5) Thermal Resistance, Junction−to−CaseTop (Note 5) Thermal Resistance, Junction−to−Board (Note 5)	 $R_{\theta JA}$ $R_{\psi JT}$ $R_{\psi JB}$	 99 16.1 63.1	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. Values based on copper area of 50 mm^2 of 1 oz copper on 4−layer FR4 board per JEDEC 51*−7.

ELECTRICAL CHARACTERISTICS

($-40°C < T_J < 150°C$, $4.5\ V < V_{IN} < 38\ V$, $4.5\ V < V_{BST} - V_{SW} < 6\ V$, $R_{OSC} = 51.1\ k\Omega$, unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
GENERAL						
Quiescent Current ($I_{VIN} + I_{VIN\_CS} + I_{BST}$)	V_{IN} = 13.2 V, EN = 0 V, Sleep Mode, $-40°C < T_A < 125°C$	$I_{Q,SLEEP}$	–	4.25	6.2	μA
	V_{IN} = 13.2 V, V_{FB} = 1 V, EN = 5 V, No Switching	I_{Q2}	–	3.25	4.24	mA
	V_{IN} = 13.2 V, V_{FB} = 0 V, EN = 5 V, Switching, No gate loads	I_{Q3}	1	4.35	5.30	mA
LDO Current	V_{IN} = 13.2 V, V_{FB} = 0 V, EN = 5 V, Switching, 3.3 nF on GH and GL	I_{LDO}	1	10	20	mA
Thermal Shutdown	Guaranteed by Design	T_{SD}	150	180	210	°C
Thermal Shutdown Hysteresis	Guaranteed by Design	$T_{SD,HYS}$	1	10	20	°C
Undervoltage Lockout (V_{IN_IC})	V_{IN_IC} increasing V_{IN_IC} decreasing	V_{UVLO}	4.1 3.9	4.3 4.18	4.5 4.45	V
Undervoltage Lockout Hysteresis		V_{UVHY}	50	125	200	mV
SWITCHING REGULATOR						
Reference Voltage		V_{ref}	0.784	0.8	0.816	V
Minimum GH Off Time		$t_{ON/MON}$	110	180	250	ns
Minimum GH Pulse Width	Static Operating	$t_{P,MIN}$	–	140	200	ns
OSCILLATOR						
Switching Frequency	R_{OSC} = 51.1 kΩ R_{OSC} = 23.2 kΩ R_{OSC} = 16.2 kΩ	f_{ROSC}	153 306 425	170 360 500	187 414 575	kHz
Ramp Voltage Amplitude		V_{Ramp}	0.9	1.1	1.3	V
VOLTAGE ERROR AMPLIFIER						
DC Gain	Guaranteed by Design	A_{VEA}	70	73	–	dB
Gain−Bandwidth Product	Guaranteed by Design	BW_{VEA}	8.0	10	–	MHz
Charge Currents	Source, V_{COMP} = 0 V	$I_{VEA,SO}$	2	4	–	mA
	Sink, V_{COMP} = 1.75 V	$I_{VEA,SI}$	1.3	3	–	mA
FB Bias Current	Guaranteed by Design	$I_{VEA,BIAS}$	–	0.1	1.0	μA
CURRENT SENSE AMPLIFIER						
Common−Mode Range		V_{CMR}	0	–	10.0	V
Amplifier Gain	$0 \le (CSP-CSN) \le 100\ mV$ $0\ V \le CSN \le 10.0\ V$	G_{CSA}	–	1	–	V/V
CURRENT ERROR AMPLIFIER						
DC Gain	Guaranteed by Design	A_{CSA}	70	73	–	dB
Gain−Bandwidth Product	Guaranteed by Design	BW_{CSA}	8.0	10	–	MHz
Charge Currents	Source, C_{COMP} = 1.75 V	$I_{CSA,SO}$	2	4	–	mA
	Sink, C_{COMP} = 1.75 V	$I_{CSA,SI}$	1.3	3	–	mA
FB Bias Current	Guaranteed by Design	$I_{CSA,BIAS}$	–	0.1	1.0	μA
Clamping Voltage		$V_{CSA,CLP}$	2.7	3.3	–	V

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 4.5 V < V_{IN} < 38 V, 4.5 V < V_{BST} − V_{SW} < 6 V, R_{OSC} = 51.1 kΩ, unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT LIMIT						
Average Current Limit Threshold	1.2 V ≤ CSN ≤ 6.5 V 6.5 V < CSN ≤ 10.0 V	$V_{ILIM,AV}$	80 72	100 100	125 133	mV
Cycle−by−Cycle Current Limit Threshold Voltage		V_{ILIMPK}	115	165	215	mV
Cycle−by−Cycle Current Limit Response Time	Guaranteed by Design	t_{LIM}	–	200	–	ns
Cycle−by−Cycle and Average Current Limit Threshold Difference		$V_{LIM.DIF}$	20	–	–	mV
SYNC						
SYNC Frequency Range	F_{SW} is defined by R_{OSC} switching frequency	f_{SYNC}	0.94 x F_{SW}	–	600	kHz
SYNC Pin Bias Current	V_{SYNC} = 0 V V_{SYNC} = 5.0 V	$f_{sync,bias}$	– –	0.1 10	0.2 20	μA
SYNC Threshold Voltage	Logic Low Logic High	$V_{SYNC,L}$ $V_{SYNC,H}$	– 2.0	– –	0.8 –	V
6.0 V LDO						
Output Voltage	I_{OUT} = 20 mA	V_{LDO}	5.8	6.0	6.2	V
Dropout Voltage	I_{OUT} = 20 mA	$V_{LDO,DO}$	–	–	220	mV
Current Limit		$I_{LDO,CL}$	30	75	120	mA
GATE DRIVERS						
GH Sink Current	V_{GH} = 2 V, V_{IN_IC} = 6 V, Guaranteed by Design	$I_{GH,SINK}$	1	1.5	2	A
GH Source Current	V_{GH} = 4 V, V_{IN_IC} = 6 V, Guaranteed by Design	$I_{GH,SRC}$	1	1.5	2	A
GL Sink Current	V_{IN_IC} = 6 V V_{GL} = 1.0 V Guaranteed by Design	$I_{GL,SINK}$	1	1.5	2	A
GL Source Current		$I_{GL,SRC}$	1	1.5	2	A
GH to GL Delay	V_{IN} = 13.2 V	$t_{GHGL,D}$	–	40	70	ns
GL to GH Delay	V_{IN} = 13.2 V	$t_{GLGH,D}$	–	40	70	ns
SOFT START						
Time	F_{SW} = 170 kHz, See Figure 19	t_{SSO}	–	14	–	ms
ENABLE (EN)						
Input Threshold	Logic Low Logic High	V_{ENLO} V_{ENHI}	– 2.0	– –	0.8 –	V
Input Current	EN = 2.0 V	$I_{EN,I}$	–	3.0	10	μA
Minimum Disable Time		$t_{EN,DIS}$	–	–	20	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_A = +25°C, V_{IN} = 13.2 V, R_{OSC} = 51.1 kΩ, unless otherwise noted)

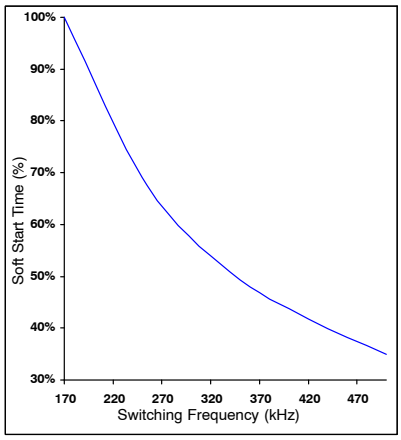


Figure 3. Soft−start Time vs. Frequency

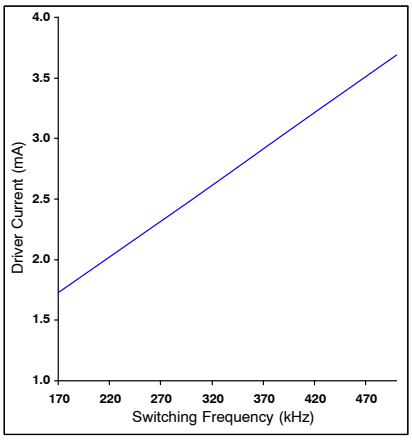


Figure 4. Driver Quiescent Current vs. Frequency

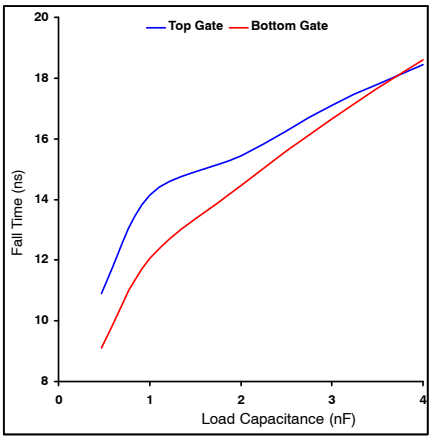


Figure 5. Driver Fall Time vs. Load Capacitance

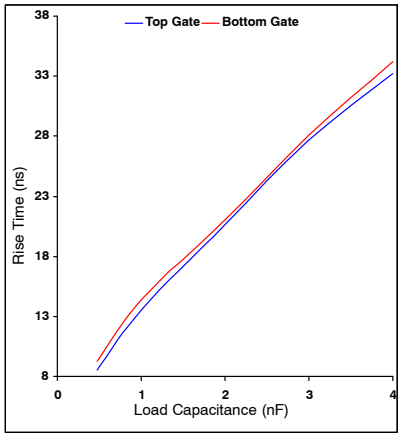


Figure 6. Driver Rise Time vs. Load Capacitance

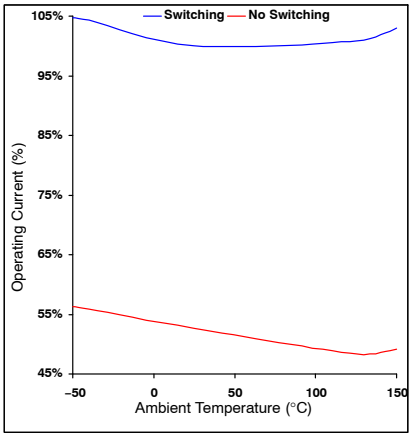


Figure 7. Operating Quiescent Current vs. Temperature

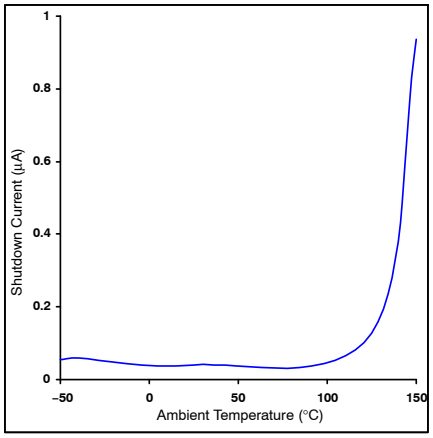


Figure 8. Sleep Mode Quiescent Current vs. Temperature

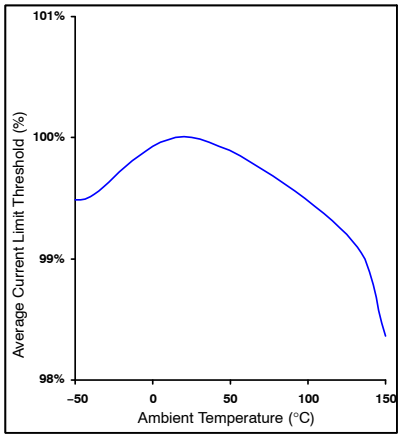


Figure 9. Average Current−Limit Threshold vs. Temperature

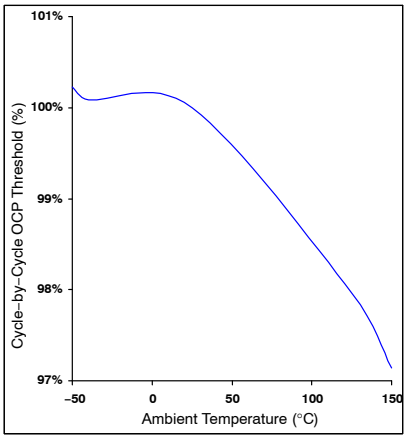


Figure 10. Cycle−by−Cycle Overcurrent Protection Threshold vs. Temperature

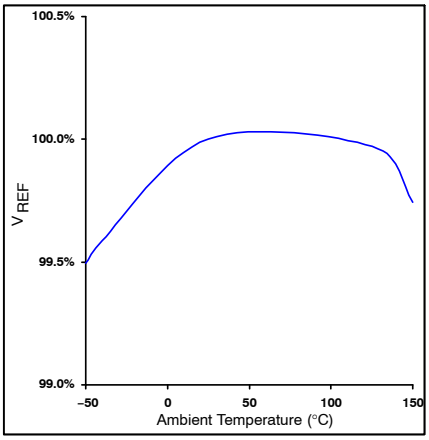


Figure 11. V_{REF} vs. Temperature

TYPICAL CHARACTERISTICS

(T_A = +25°C, V_{IN} = 13.2 V, R_{OSC} = 51.1 kΩ, unless otherwise noted)

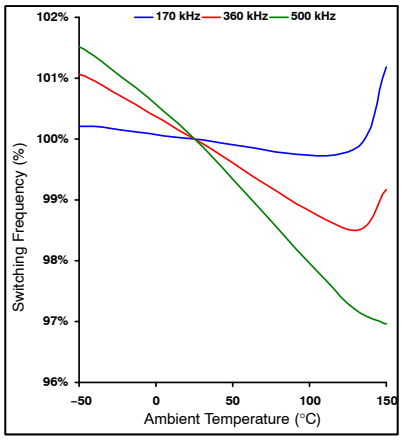


Figure 12. Oscillator Frequency vs. Temperature

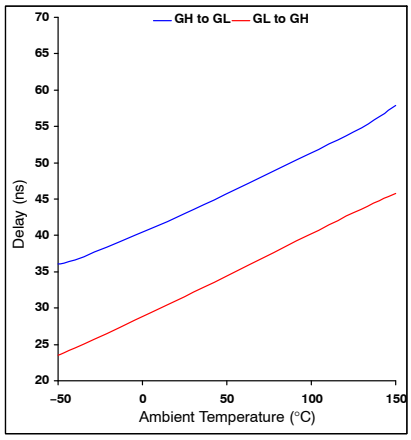


Figure 13. Non−Overlap Delay vs. Temperature

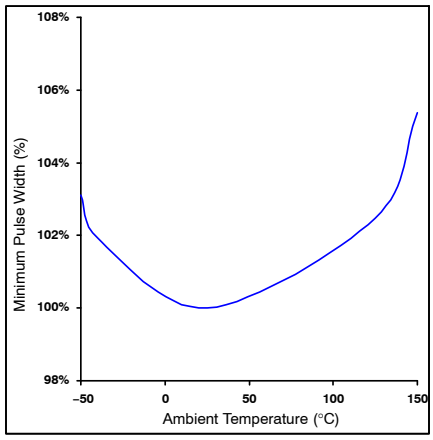


Figure 14. GH Minimum Pulse Width vs. Temperature

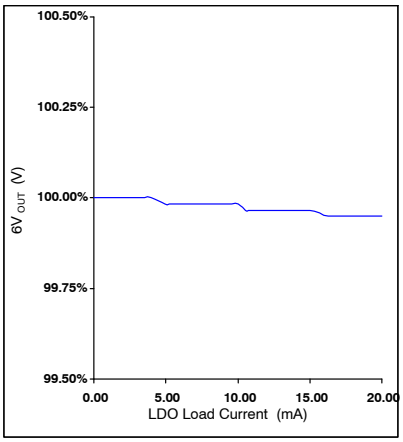


Figure 15. LDO Load Regulation

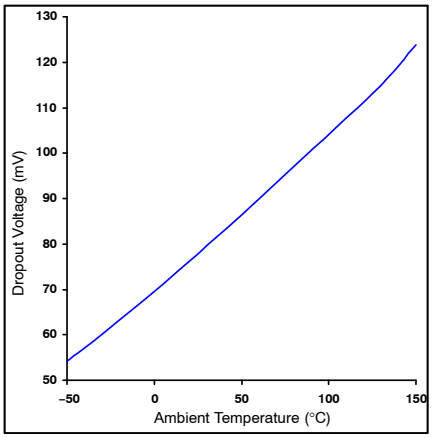


Figure 16. LDO Dropout Voltage vs. Temperature

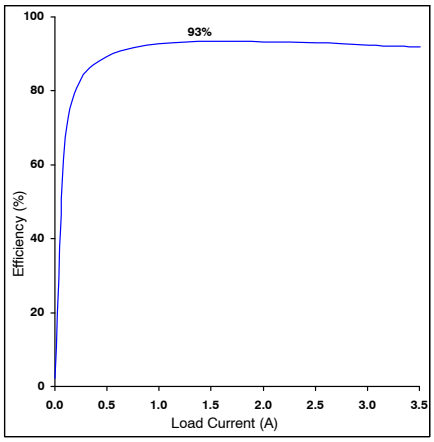


Figure 17. Efficiency vs. Load Current 5 V, 170 kHz Demo Board

DETAILED OPERATING DESCRIPTION

General

The NCV8856A is a synchronous buck controller with internal 1.5 A gate drivers designed to drive N−channel MOSFETs. The internal gate drivers simplify design, improve performance and efficiency and minimize board area. The controller has an 800 mV, 2.0% reference, allowing a wide range of precise output voltage programmability. The NCV8856A operates at a fixed frequency over a range of 170 kHz to 500 kHz set by an external resistor to ground – facilitating design tradeoffs such as efficiency versus component size and cost. An external clock signal can also be used to synchronize the NCV8856A to a higher operating frequency during operation.

To minimize the impact on the power handling components and the input power rail, inrush current during start−up is limited by an internally−controlled output voltage soft−start. Inductor current is also limited via average current limiting (ACL) and cycle−by−cycle overcurrent protection (OCP). Thermal shutdown (TSD) is also implemented to protect the device from overheating.

Average Current Mode Control

The NCV8856A employs an average current mode control (ACMC) architecture to regulate the output voltage. As implied by the name, ACMC regulates output voltage based on the average current supplied to the output, and is thereby better suited to applications sensitive to the behavior of either input or output current, such as power factor correction, LED lighting control, or operation in discontinuous conduction (DCM). As with peak current control, compensation for input voltage changes, and output current monitoring and limiting are inherent – with the additional ability of ACMC to base these functions on average current.

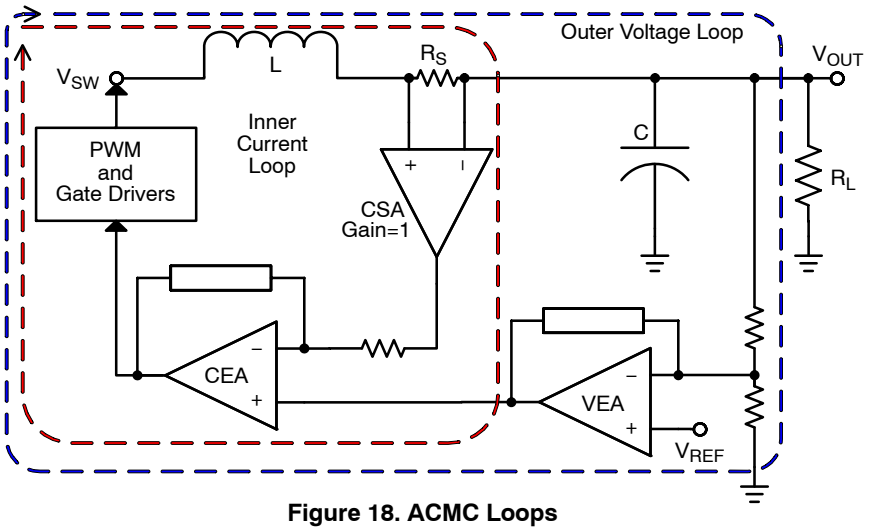


Figure 18. ACMC Loops

ACMC uses two loops, as shown in Figure 18. Through the unity gain current sense amplifier (CSA) and high−gain current error amplifier (CEA), the inner current loop controls the inductor current. The current loop reacts to input voltage changes – compensating for line transients. Using the voltage error amplifier (VEA), the outer voltage loop monitors the output voltage and reacts to output load changes – compensating for load transients.

Unlike voltage mode control (VMC) regulators – which typically require a Type−III compensation network for adequate transient response – ACMC regulators use two Type−II compensators. This simplifies the compensator design and optimization process, while offering faster transient response than a single Type−II compensation network. Type−II compensation places a zero and two poles in each of the error loops to stabilize converter operation. Each compensator requires a resistor and two capacitors (shown as complex impedances in Figure 18) in the feedback path the error amplifier. A resistor from the CSA output to the CEA scales the CEA gain at all frequencies. A pair of resistors forms a resistive attenuator from the output to set the output voltage and scale the VEA gain at all frequencies.

ENABLE

The enable pin (EN) is a TTL−compatible input used to activate internal circuitry. The NCV8856A is disabled when the EN pin voltage is below the enable input low threshold – shutting off both external FETs, and putting the part into a low quiescent current sleep mode. Once the device has been disabled, it must remain disabled for the minimum disable time. When the EN pin voltage goes above the enable input high threshold, the 6VOUT output comes up, and then the soft−start begins. The EN pin can be tied to VIN in order to automatically enable the part.

6VOUT

6VOUT is the output of a low dropout (LDO) linear regulator that regulates voltage from the VIN pin down to 6 V. A small ceramic capacitor must also be connected between 6VOUT and ground – close to the 6VOUT pin. When VIN voltage is sufficiently high, applying a high level to the EN pin activates the 6VOUT output. When the part is enabled and VIN is below the 6VOUT target voltage, the LDO is in dropout and tracks VIN. The LDO regulates its output once VIN voltage is above the 6VOUT target plus dropout voltage. The 6VOUT output directly powers the low−side gate driver, and must be externally connected through a low leakage (< 100 μA at Tmax) diode to the BST pin – charging the BST capacitor during the off−time to provide a floating voltage for the high−side driver. Since 6VOUT supplies charge to both the BST capacitor and the low−side driver, the LDO capacitor should be larger than the BST capacitor. A CLDO/CBST capacitor ratio of 10:1 is recommended along with a CLDO value of 1−4.7 μF. 6VOUT must also be connected externally to the VIN_IC pin through a small RC filter network to power internal circuits. A short to ground or overcurrent condition on the 6VOUT pin will be current limited. Use of 6VOUT output current for additional external circuits will increase internal LDO dissipation, and must not produce an overcurrent condition. Such use should be limited to PCB locations close to the NCV8856A.

VIN_IC

With the exception of the gate drivers, the NCV8856A is powered by the voltage connected to the VIN_IC pin. A small (0.1 μF recommended) ceramic capacitor should be connected between VIN_IC and ground, and close to the VIN_IC pin. A low value resistor must be connected between the VIN_IC and 6VOUT pins.

UVLO

An Undervoltage Lockout (UVLO) monitor at the VIN_IC pin ensures that unexpected behavior does not occur when VIN_IC is too low to support internal NCV8856A circuits. If enabled, the IC will start up when VIN_IC exceeds the increasing UVLO threshold (START threshold) and will shut down when VIN_IC drops below the decreasing UVLO threshold (STOP threshold).

If VIN_IC passes the UVLO threshold, but VIN remains below the VOUT setpoint after soft−start, the switcher will run at max duty cycle until VIN voltage is higher.

If EN is high and VIN_IC is below the UVLO START threshold, a totally unloaded output will slowly rise above zero volts. The high EN signal activates internal rails, allowing a small leakage current to flow out pins connecting to the output; the high side MOSFET also contributes leakage current directly from VIN. A 1k resistor connected from the power supply output to ground avoids a non−zero output voltage under these conditions.

Thermal Shutdown

The NCV8856A provides Thermal Shutdown (TSD), which monitors the die temperature and turns off the top and bottom gate drivers if an over temperature condition is detected. The internal soft−start capacitor is also discharged. A normal soft−start will occur when the die temperature falls below the TSD threshold minus TSD hysteresis.

Duty Cycle and Maximum Pulse Width Limits

In steady state operation, the duty cycle (ratio of GH time to switching period) stabilizes at an operating point roughly the ratio of output voltage to input voltage. A built in minimum GH off−time ensures that the bootstrap supply capacitor gets charged every cycle, which enforces a slightly different maximum duty cycle depending on switching frequency. The NCV8856A can achieve at least a 95% duty cycle while operating at frequencies up to 200 kHz (89% at up to 500 kHz).

Internal Soft−Start

The NCV8856A features an internal soft−start function, which reduces inrush current and output voltage overshoot. Figures 19 and 20 show a typical soft−start sequence. Soft−start is achieved by ramping up the internal soft−start voltage (VSS), which is applied to the non−inverting input of the voltage error amplifier – effectively limiting the slew rate of VOUT rising. This ramp is generated by charging an internal soft−start capacitor based on the internal oscillator, causing the soft−start time to be inversely related to the frequency set by ROSC. The internal soft−start capacitor is discharged when the part is disabled, enters TSD, or enters UVLO – ensuring a proper start−up when the part is re−enabled, leaves TSD or leaves UVLO. This sequence begins when VIN_IC passes the UVLO START threshold or when the part is enabled and the 6VOUT output has risen. After an initial delay to read internal memory, switching begins – with the output quickly rising to a low voltage followed by a controlled rise to target voltage. If VIN voltage is constant during soft−start, the duty cycle increases as VOUT climbs to the set point, or until maximum duty cycle is reached if VIN is insufficiently high.

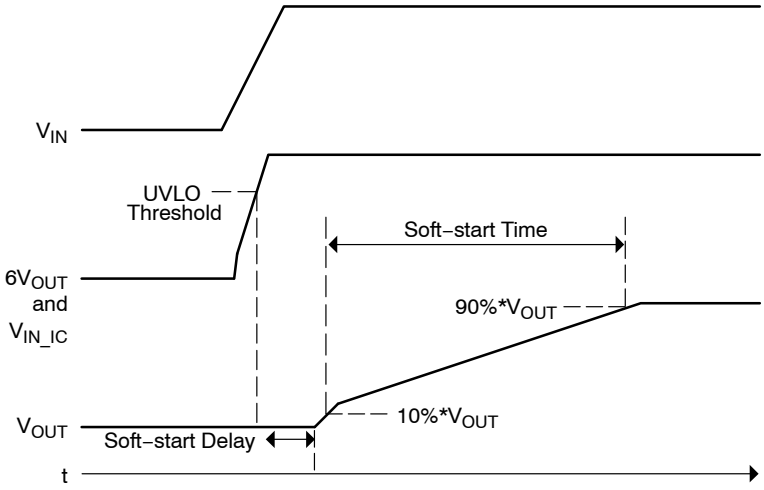


Figure 19. Normal Start−up

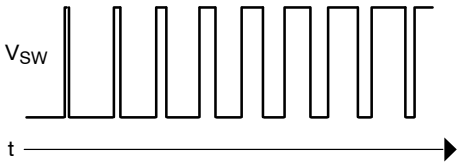


Figure 20. Switch−node in Soft−Start

Normal Shutdown Behavior and Sleep Mode

Normal shutdown occurs if the input supply drops below the UVLO STOP threshold, the part enters TSD, or the part is disabled by applying a low voltage to the EN pin. Under these conditions, GH and GL both go low to stop switching, the switch node enters a high impedance state and the output inductor and capacitors discharge through the load, and the internal soft−start capacitor is discharged. When disabled by applying a low voltage to the EN pin, the 6VOUT LDO turns off, its output capacitor is allowed to discharge, and VIN current reduces to the sleep mode quiescent current.

Gate Drivers

The NCV8856A includes 1.5 A gate drivers to switch external N−Channel MOSFETs. This allows the NCV8856A to address high−power, as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry minimizes power dissipation – increasing efficiency – by minimizing the body diode conduction time, while protecting against cross−conduction (shoot−through) of the MOSFETs. A detailed block diagram of the non−overlap and gate drive circuitry used in the chip and related external components is shown in Figure 21. A capacitor connected from VSW to BST, and a diode connected from 6VOUT to BST create a bootstrap supply at the BST pin for the floating, high−side gate driver. This ensures that the voltage on BST is about 6VOUT higher than VSW, less a diode drop – yielding a gate drive voltage high enough to enhance the high−side MOSFET. The BST capacitor supplies the charge used by the gate driver to charge the high−side MOSFET input capacitance, and is typically chosen to be at least a decade larger than the input capacitance (0.1 μF recommended). Since the BST capacitor only recharges when the low−side MOSFET is on – pulling VSW down to ground – the NCV8856A enforces a minimum GH off−time.

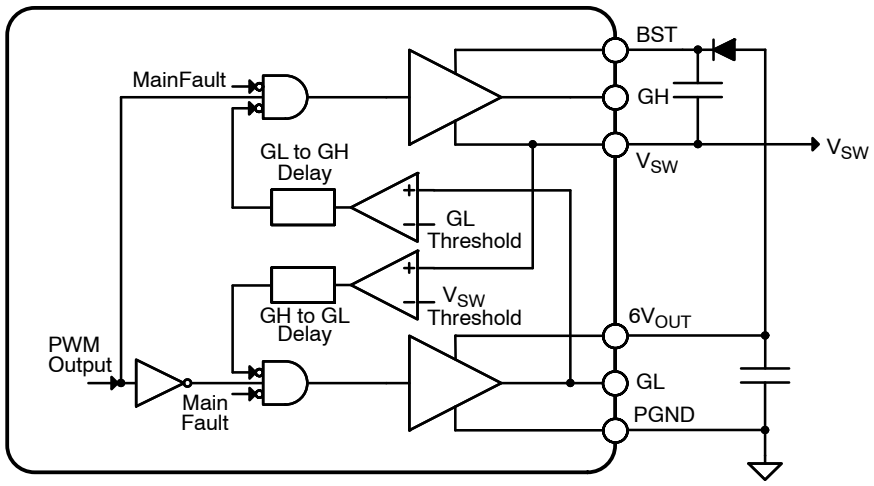


Figure 21. Gate Driver Block Diagram

Careful selection and layout of external components is required to realize the full benefit of the onboard drivers. The capacitors between 6VOUT and GND and between BST and VSW must be placed as close as possible to the IC. The current paths for the GH and GL connections must minimize parasitic resistance and inductance.

Current Limiting and Overcurrent Protection

The NCV8856A implements average current limiting (ACL) and cycle−by−cycle overcurrent protection (OCP) to protect the power switches, inductor, current sense resistor and loads. The current through the inductor also flows through a current sense resistor – developing a voltage across the resistor proportional to current that is continuously sensed at the CSP and CSN pins, is summed with a bias voltage, and appears at the output of the Current Sense Amplifier (CSA).

ACL

The current and voltage error amplifiers (CEA and VEA) make the VEA output voltage (VCOMP) equal the average CSA amplifier output voltage (CSOUT) after a small delay reflecting the averaging action of both error amplifiers. VCOMP voltage is compared to a fixed internal (ACL) voltage threshold. VCOMP is pulled down if it exceeds the threshold, and through the action of the CEA, this lower VCOMP voltage reduces the PWM pulsewidth – reducing the average current through the inductor until the average is at the ACL threshold. In steady−state operation, increasing the load while in ACL will cause the duty cycle and VOUT to decrease proportionally without jitter or skipping pulses. An advantage of this method of current limiting is that the NCV8856A will limit large transient currents yet resume normal operation on the following cycle. The current will not run away or latch the part off in case of a short, which is a characteristic of some other methods of current limiting.

OCP

If the differential plus bias voltage exceeds the OCP threshold (which is above the ACL threshold), the PWM pulse is immediately terminated and will not switch back on until the current through the inductor has dropped the instantaneous CSA output voltage below the OCP threshold. Once the inductor current is below the OCP threshold, the part will begin switching again, although current may be limited by ACL until the inductor current drops below the ACL threshold.

SYNC Feature

An external clock signal can synchronize the NCV8856A to a frequency higher than that programmed by the resistance at the ROSC pin. The rising edge of the SYNC pulse turns on the power switch after a 0.5 μs delay to start a new switching cycle, as shown in Figure 22. The SYNC threshold is TTL logic compatible, and the duty cycle of the SYNC pulses can vary from 10% to 90%. The SYNC frequency (if used) is typically chosen to meet important EMC requirements, and the Rosc controlled frequency should be set relative to that SYNC frequency (see the Switching Frequency Selection Section of the Design Methodology). The highest SYNC frequency must not exceed the SYNC Frequency Range maximum limit.

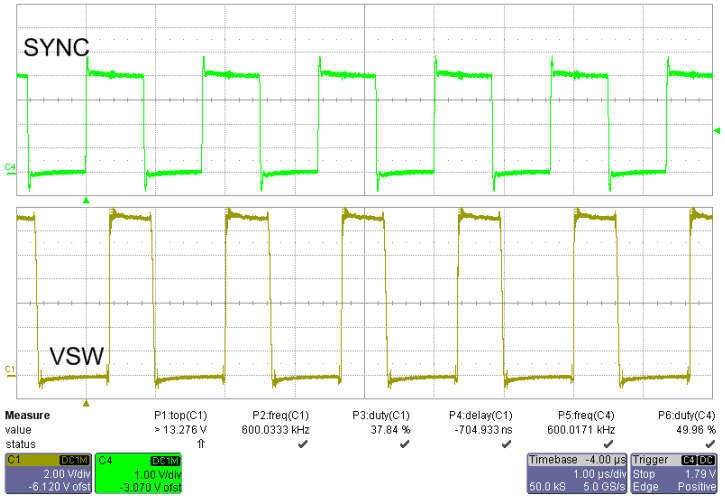


Figure 22. Synchronization from 170 kHz to an external 600 kHz signal

APPLICATIONS INFORMATION

Design Methodology

Choosing external components for the NCV8856A entails the following design process:

1. Determine operational requirements
2. Select switching frequency
3. Select current sensor
4. Select output inductor
5. Select output capacitors
6. Select input capacitors
7. Select current loop compensator components
8. Select components to set output voltage
9. Select voltage loop compensator components

(1) Operational Parameter Definition

Before selecting components, certain operational requirements must be determined. These are application−dependent and include the following:

$V_{IN(max)}$: maximum input voltage [V]
$V_{IN(typ)}$: typical input voltage [V]
$V_{IN(min)}$: minimum input voltage [V]
V_{OUT}: output voltage [V]
I_{OUT}: output current, range from minimum to maximum, and during start−up [A]
I_{CL}: desired typical current limit [A]

The following basic calculations will be used in several parts of the design process:

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(max)}} \quad \text{(eq. 1)}$$

$$D = \frac{V_{OUT}}{V_{IN(typ)}} \quad \text{(eq. 2)}$$

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(min)}} \quad \text{(eq. 3)}$$

Where:
D_{MIN}: minimum duty cycle [%]
D: typical duty cycle [%]
D_{MAX}: maximum duty cycle [%]

These are ideal duty cycles. Actual duty cycles will be marginally higher than these calculated values due to voltage drops in the MOSFETs, inductor and current sense resistor caused by the output load.

(2) Switching Frequency Selection

Determining the best switching frequency within the specified NCV8856A range should be based on several considerations:

1. The physical size or cost of the output filter components (inductor and capacitors)
2. The response speed needed for line and load transients
3. The amount of heat that can be removed from the controller and MOSFETs, or the required efficiency
4. The required minimum or maximum conversion ratio (ratio of minimum or maximum Vin, respectively, to Vout)
5. Avoiding producing EMI at frequencies that would interfere with nearby circuits

Operation at higher switching frequencies decreases the output inductor and capacitor values required to achieve acceptable current and voltage ripple. Lower value components are physically smaller and typically cost less.

Higher switching frequency improves regulator response time both by use of a lower value inductor to quickly support load current changes, and also by allowing use of a higher frequency 0dB loop gain crossover (see the Compensator Design section).

Operation at higher switching frequencies increases controller and MOSFET switching losses, which lead to higher temperatures and cooling requirements at maximum load. The decreased efficiency caused by the higher losses may be of special importance at light loads.

Besides the specified switching frequency limits, two other NCV8856A characteristics set limits on the maximum allowable switching frequency: minimum off−time and minimum on−time. These represent two different restrictions on maximum switching frequencies, as follows:

$$F_{SW(max)1} = \frac{1 - D_{MAX}}{T_{MinOff}} \quad [Hz] \quad \text{(eq. 4)}$$

$$F_{SW(max)2} = \frac{D_{MIN}}{T_{MinOn}} \quad [Hz] \quad \text{(eq. 5)}$$

Where:
$F_{SW(max)1}$: maximum switching frequency due to minimum off−time [Hz]
T_{MinOff}: minimum off−time [s]
$F_{SW(max)2}$: maximum switching frequency due to minimum on−time [Hz]
T_{MinOn}: minimum on−time [s]

Alternatively, the minimum and maximum operational input voltage can be calculated as follows:

$$V_{IN(min)} = \frac{V_{OUT}}{1 - T_{MinOff} \cdot F_{SW}} \quad [V] \quad \text{(eq. 6)}$$

$$V_{IN(max)} = \frac{V_{OUT}}{T_{MinOn} \cdot F_{SW}} \quad [V] \quad \text{(eq. 7)}$$

Where:
F_{SW}: switching frequency [Hz]

The switching frequency is programmed by selecting the resistor connected between the R_{OSC} pin and ground. The grounded side of this resistor should be directly connected to the AGND pin. Avoid running any noisy signals under the resistor, since injected noise could cause frequency jitter.

The graph in Figure 23 shows the relationship between R_{OSC} resistance and switching frequency. The following formula yields frequency programming resistance accurate to approximately 4%:

$$R_{OSC} = \frac{8300000}{F_{SW}} \quad [\Omega] \quad \text{(eq. 8)}$$

Where: R_{OSC}: frequency program resistor [Ω]
F_{SW}: switching frequency [kHz]

Some specific values for switching frequency with standard 1% resistors may be found in Table 1.

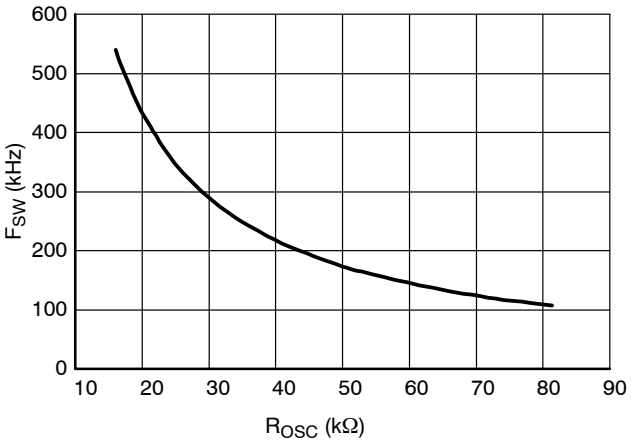


Figure 23. Frequency vs. R_{OSC}

Table 1. Frequency vs. R_{OSC}

F_{SW} (kHz)	R_{OSC} (kΩ)
170	51.1
250	34.8
300	28.7
360	23.2
500	16.2

In cases where the switching frequency is selected to avoid interfering with signals known to be sensitive to certain frequencies, R_{OSC} should program frequency to a value that avoids sensitive frequencies by a margin exceeding the f_{ROSC} tolerance.

In cases where a SYNC signal is used to avoid sensitive frequencies, the R_{OSC} resistance should be chosen such that the maximum internal oscillator frequency (f_{ROSC} plus tolerance) is no more than 6% higher than the minimum SYNC frequency.

The equation relating minimum R_{OSC} resistance to the R_{OSC} resistor tolerance and minimum SYNC frequency is:

$$R_{OSC} \geq \frac{8300 \times (1 + 1.6 \times R_{TOLERANCE})}{0.91 \times F_{SYNCmin}} \quad [k\Omega] \quad \text{(eq. 9)}$$

Where:
$R_{TOLERANCE}$ is either 0.01 for 1% resistors or 0.05 for 5% resistors
R_{OSC} is in kΩ
$F_{SYNCmin}$ is in kHz

For the 1% resistor series, this equation becomes:

$$R_{OSC} \geq \frac{7674}{F_{SYNCmin}} \quad [k\Omega] \quad \text{(eq. 10)}$$

The next−higher standard value should be chosen for the R_{OSC} resistor.

The soft−start time is a function of switching frequency and can be estimated as follows:

$$t_{SS} \approx \frac{F_0}{F_{SW}} \cdot t_{SS0} \quad [ms] \quad \text{(eq. 11)}$$

Where: t_{SS}: soft−start time [ms]
F_0: frequency condition specified for t_{SS0} [kHz]
F_{SW}: switching frequency [kHz]
t_{SS0}: specified soft−start parameter [ms]

(3) Current Sensor Selection

Current sensing for average current mode control relies on the inductor current signal. This is translated by a current sensor into a voltage, which is then measured differentially by the current sense amplifier, which produces a single−ended output for use as a control signal. The easiest means of implementing the current sensor is by use of a sense resistor in series with the output inductor. Alternative methods, such as lossless inductor current sensing, are feasible but beyond the scope of this document. A sense resistor [Ω] should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}} \quad \text{(eq. 12)}$$

Where:
V_{CL}: current limit threshold voltage [V] (either $V_{ILIM.AV}$ or V_{ILIMPK})
I_{CL}: desired current limit [A] (corresponding to either $V_{ILIM.AV}$ or V_{ILIMPK})

The size of the sense resistor should be chosen based on the power dissipated by the resistor as given by:

$$P_{RS} = \frac{V_{CL(max)}^{\ 2}}{R_S} \quad [W] \quad \text{(eq. 13)}$$

Where:
$V_{CL(max)}$: the maximum limit specified for the current limit threshold voltage $V_{ILIM.AV}$ [V]

(4) Output Inductor Selection

Inductors have many important characteristics. Among the most important for Automotive applications of the NCV8856A are:

1. Value
2. Saturation characteristic
3. DC resistance (DCR)
4. Operating Temperature range
5. Size – including height
6. Cost
7. Mounting configuration – including the ability to inspect solder joints
8. Containment of magnetic flux (shielding)

Decisions on most of these characteristics can be treated as “go/no−go” considerations.

Generally, a “shielded” inductor must be used in order to meet Automotive EMC requirements. And an inductor with “wetted flanks” should be used for easiest post−assembly inspection.

Since the inductor is often one of the largest components in the power supply, a low inductor value is preferred in space−constrained applications, since lower inductor values generally correspond to smaller physical size. Also – except for the very smallest inductors – the smaller sized inductors within a supplier’s particular technology series are typically less expensive.

The inductor Operating Temperature Range must include the full application operating ambient temperature range plus additional range on the high end for internal inductor dissipation, which is dominated by the inductor DCR loss at the frequencies used by the NCV8856A. Most inductor suppliers offer an online tool to calculate inductor internal temperature rise for any chosen ambient and maximum application load current. Internal temperature above maximum inductor operating temperature requires selecting a different inductor. A lower value inductor within the same product series will have a lower DCR and therefore less internal temperature rise. A different inductor product series might have a lower thermal resistance – and therefore lower internal temperature rise – for the same DCR.

If inductor maximum temperature is within the inductor temperature rating, the impact of inductor dissipation on efficiency may still need to be considered. If the application requires higher efficiency than the online loss calculator predicts, inductor dissipation can be lowered by selecting a different inductor with lower DCR.

Many inductor manufacturers specify saturation current at a 30% decrease in inductance. To prevent such a large value change from affecting regulator stability in normal operation, the saturation current rating should be well above the peak overload current. For the NCV8856A, this is the combined average current limit (max limit) plus half of the peak−to−peak ripple current. Saturation current varies significantly with temperature for some inductors. Inductors with ferrite and other alloy cores (sometimes called “dust” cores) may fall into this category. Unless the core material is “powdered iron”, the temperature variation of saturation current should be checked to be sure saturation current stays well above the peak current at maximum inductor temperature.

The inductor value should initially be chosen to produce a ripple current equaling 20−40% of the rated output current. If found to be necessary later in the design process in order to meet output ripple voltage or transient response requirements, this value can be increased or decreased, respectively.

The peak−to−peak ripple current [Ap−p] is given by the following equation:

$$\Delta i_L = \frac{V_{OUT} \times (1 - D)}{L \times F_{SW}} \quad [A] \qquad \text{(eq. 14)}$$

From this equation it is clear that the ripple current increases as L decreases,

The ripple current is at a maximum when the duty cycle is at a minimum value and vice versa, as follows:

$$\Delta i_{L(max)} = \frac{V_{OUT} \times (1 - D_{MIN})}{L \times F_{SW}} \quad [A] \qquad \text{(eq. 15)}$$

$$\Delta i_{L(min)} = \frac{V_{OUT} \times (1 - D_{MAX})}{L \times F_{SW}} \quad [A] \qquad \text{(eq. 16)}$$

Where:

$\Delta_{iL(max)}$: maximum inductor ripple current [Ap−p]

$\Delta_{iL(min)}$: minimum inductor ripple current [Ap−p]

The peak and valley values of the triangular current waveform are as follows:

$$i_{L(pk)} = I_{OUT} + \frac{\Delta i_L}{2} \quad [A] \qquad \text{(eq. 17)}$$

$$i_{L(vly)} = I_{OUT} - \frac{\Delta i_L}{2} \quad [A] \qquad \text{(eq. 18)}$$

Where:

$i_{L(pk)}$: peak (maximum) value of ripple current [A]

$i_{L(vly)}$: valley (minimum) value of ripple current [A]

Δ_{iL}: inductor ripple current at the input voltage of interest – usually $\Delta i_{L(max)}$ [Ap−p]

Larger inductor values decrease the speed at which inductor current can change in response to output load changes. This increases the magnitude of output voltage perturbations, since output capacitance must supply (or absorb) the load change while inductor current changes. For a given load change, lower inductance produces either less output perturbation for a given output capacitance, or the same perturbation with less output capacitance, due to the faster inductor current change capability. But unless output capacitance is increased, lower inductance increases output voltage ripple.

(5) Output Capacitor Selection

One or more multilayer ceramic capacitors (MLCC) are recommended for use due to their low equivalent series resistance (ESR) and inductance (ESL), which reduce high−frequency output voltage noise components such as ripple voltage.

A good criterion for determining the minimum amount of MLCC output capacitance is the maximum amount of output voltage ripple that is acceptable at maximum DC load. Inductor ripple current causes a 90−degree lagging output voltage ripple [Vp−p] on the output capacitance:

$$V_Q = \frac{i_L}{2 \times \pi \times C_{MLCC} \times F_{SW}} \quad [V] \qquad \text{(eq. 19)}$$

Where C_{MLCC} = total capacitance of MLCC output capacitors [F]

Also, the ripple current produces an in−phase voltage ripple [Vp−p] on the ESR of the output capacitors as follows:

$$V_{ESR} = i_L \times R_{ESR} \quad [V] \qquad \text{(eq. 20)}$$

Where:

R_{ESR}: equivalent ESR of all output capacitors in parallel (both MLCC and bulk) [Ω]

The total output voltage ripple [Vp−p] in steady−state operation is:

$$V_{RIP} \approx V_Q + V_{ESR} \quad [V] \qquad \text{(eq. 21)}$$

The very low ESL of MLCC output capacitors does not contribute to output ripple voltage when output inductance is above 1uH. But the PCB trace between the output inductor and MLCC caps can add ESL, so MLCC capacitors should always be located between the load and the output inductor.

Output capacitance is a primary determinant of power supply response to a load transient. During the first few microseconds of a load step, output capacitance supplies the incremental load current, but discharges in the process. The controller recognizes the load step and increases the duty cycle, but the current slew rate is limited by the inductor, and output voltage temporarily dips. Similarly, during a load release, the output voltage exhibits a momentary peak. Higher output capacitance decreases the magnitude of these voltage perturbations.

Providing sufficient capacitance for acceptable transient performance at an acceptable cost may require bulk capacitors to be used in addition to MLCC capacitors. If so, aluminum polymer/hybrid bulk capacitors are recommended instead of aluminum electrolytic capacitors due to their low −40°C/25°C ESR ratio. Use of bulk capacitors having a high −40°C/25°C ESR ratio may result in an ineffective output filter along with decreased stability under cold operating temperature conditions.

For a given output voltage dip caused by a given load step−up, the following minimum total capacitance is required:

$$C_{MIN} = \frac{\Delta I_{OUT} \times \left(\frac{1}{4 \times F_{CO}} + \frac{1}{F_{SW}}\right)}{2 \times \Delta V_{DIP}} \quad [F] \qquad \text{(eq. 22)}$$

Where:

ΔI_{OUT}: Load current step increase [A]

F_{CO}: Control loop 0dB gain frequency [Hz]

$\Delta V_{DIP(max)}$: Maximum allowed output voltage dip upon load step−up [V]

The worst−case output voltage peak occurs when load current initially at the current limit (with output voltage still in regulation) is released (goes to zero). The minimum capacitance for a given peak is:

$$C_{MIN} = \frac{L \cdot I_{CL}^2}{(V_{OUT} + \Delta V_{OS})^2 - V_{OUT}^2} \quad [F] \qquad \text{(eq. 23)}$$

Where:

$V_{OS(max)}$: output voltage overshoot peak on CMIN upon removal of an overload [V]

I_{CL}: average current limit [A]

The minimum output capacitance should be chosen as the larger of that needed to limit both output voltage dip and overshoot. The worst−case overshoot peak for the chosen output capacitance (C_{OUT}) is:

$$\Delta V_{OS} = \sqrt{\frac{L \cdot I_{CL}^2}{C} + V_{OUT}^2} - V_{OUT} \qquad \text{(eq. 24)}$$

During soft−start, inductor current must charge the output capacitance as well as supply the load. The sum of these currents should be no higher than the average current limit. For a given average current limit the maximum output capacitance is:

$$C_{MAX} = \frac{(I_{CL} - I_{OUT(i)}) \cdot t_{SS}}{V_{OUT}} \qquad \text{(eq. 25)}$$

Where $I_{OUT(i)}$ = highest instantaneous load current prior to output voltage reaching regulation [A]

The current needed from the input supply to charge this output capacitance during soft−start is:

$$I_{INRUSH} = \frac{C_{OUT} \cdot V_{OUT}}{t_{SS}} + D \times I_{OUT(i)} \qquad \text{(eq. 26)}$$

If the inrush current is higher than the steady−state input current with the maximum load, then the input fuse (if used) should be rated accordingly.

(6) Input Capacitor Selection

Input capacitors conduct the inductor current during the on time of the high−side MOSFET. The largest harmonic of the input capacitor ripple current is at the switching frequency, and at high loads, the RMS value of this current given by the following equation may be much higher than the inductor ripple current:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \cdot (1 - D)} \quad [A] \qquad \text{(eq. 27)}$$

The above equation reaches its maximum value with D = 0.5, where $I_{IN(RMS)} = I_{OUT}/2$. The input capacitors must be rated to handle a ripple current of one−half the maximum output current at the switching frequency. ESR is the major cause of losses in the input capacitors, so input capacitors need low ESR at the switching frequency to minimize loss, which is given by:

$$P_{CIN} = I_{IN(RMS)}^2 \cdot R_{ESR(CIN)} \quad [W] \qquad \text{(eq. 28)}$$

Where $R_{ESR(CIN)}$ = equivalent series resistance of all input capacitors in parallel

Electrolytic, polymer and/or ceramic capacitors should be used. If a tantalum must be used, it must be surge protected to prevent against capacitor failure. Ceramic capacitors are recommended in parallel with bulk input capacitors, since their lower ESR will handle most of the ripple current with minimum power loss. An additional capacitor with a value

of 0.01 μF to 0.1 μF is also recommended to be placed at the high−side MOSFET.

(7) Current Error Amplifier (CEA) Compensator Design

Compensator tuning stabilizes the converter with a minimum amount of (and minimum cost of) output capacitance.

The NCV8856A employs Average Current Mode Control (ACMC) which entails both an inductor current control feedback loop, and an output voltage control feedback loop. Separate error amplifiers are used for each loop – each with simple Type−II compensation. The Current Error Amplifier (CEA) compensation sets the characteristics of the "inner" current control loop, and the Voltage Error Amplifier (VEA) compensation sets the characteristics of the "outer" voltage control loop. "Closing" the CEA loop with inductor current feedback provides an additional gain block to the outer voltage feedback loop, without the phase lag that typically comes with such gain. The use of two amplifiers provides a large total amount of loop gain at low and mid−frequencies which allows lower output capacitance than many other control methods.

Compensator design involves determining the frequencies of zeros and poles in the CEA and VEA loops in order to stabilize the converter over the desired range of input voltage and output load. Initial compensator component values are derived from equations, and subsequently tuned through simulation, or measurement of output voltage response to line and load steps.

As shown in Figure 24, CEA compensation provides a low frequency pole (at the origin, via capacitor C_{C1}), and a mid−frequency zero − above which, CEA gain is flat. Capacitor C_{C1} and resistor R_{C1} set the zero at a frequency at least as high as the pole formed by the peak current mode sampling effect in the power stage. The flat gain is then set (typically well above 1) by selecting a value of R_{C2} that amplifies (and inverts) inductor current downslope to no greater than the upslope of the internal ramp.

A second pole realized by C_{C2} can reduce the impact of switching noise on the CEA loop if placed near the switching frequency.

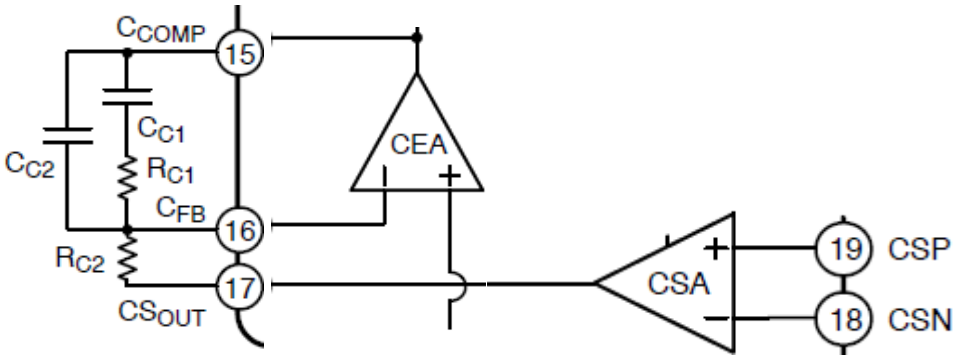


Figure 24. Current Error Amplifier (CEA) Compensation

Since standard capacitor values are spaced much further apart than standard resistor values, compensation should start by choosing a standard value for the CEA low frequency pole capacitance C_{C1} such as 2.2 nF. The CEA zero frequency is then set by resistor R_{C1} from:

$$R_{C1} = \frac{F_{SW} \times L_{MIN} \times R_{CS} \times V_{IN} \times R_L \times C_{OUT}}{1.1 \times C_{C1} \times \left(R_L \times \left(R_{CS}(0.5 \times V_{IN} - V_{OUT}) + F_{SW} \times L_{MIN} \times V_R\right) + F_{SW} \times L_{MIN} \times R_{CS} \times V_{IN}\right)} \quad [\Omega] \quad \text{(eq. 29)}$$

Where:
F_{SW}: switching frequency [Hz]
L_{MIN}: inductor value at the low tolerance limit [H]
R_{CS}: current sense resistance [Ω]
V_{IN}: minimum input voltage [V]
R_L: minimum load resistance [Ω]
C_{OUT}: total output capacitance [F]
C_{C1}: value chosen for the capacitor setting the low frequency pole [F]
V_{OUT}: output voltage [V]
V_R: minimum internal ramp voltage [V]

This sets the zero frequency at:

$$f_{ZC} = \frac{R_L \times \left(R_{CS} \times \left(0.5 \times V_{IN} - V_{OUT}\right) + F_{SW} \times L_{MIN} \times V_R\right) + R_{CS} \times V_{IN}}{2 \times \pi \times F_{SW} \times L_{MIN} \times R_{CS} \times V_{IN} \times R_L \times C_{OUT}} \quad [Hz] \quad \text{(eq. 30)}$$

The value of R_{C2} to set the overall gain of the CEA is:

$$R_{C2} = \frac{R_{CS} \times V_{OUT} \times R_{C1} \times A_{CSA}}{F_{SW} \times L_{MIN} \times V_R} \quad [\Omega] \quad \text{(eq. 31)}$$

Where:
A_{CSA}: maximum current sense amplifier gain [V/V]

Another pole placed near the switching frequency to reduce the impact of switching noise on the CEA loop can be realized by C_{C2}:

$$C_{C2} = \frac{C_{C1}}{2 \times \pi \times f_{HFPC} \times R_{C1} \times C_{C1} - 1} \quad [F] \quad \text{(eq. 32)}$$

Where:
f_{HFPC}: frequency desired for the CEA high frequency pole

(8) Setting Output Voltage

As shown in Figure 25, a resistive divider from the regulator output to the negative input of the VEA sets the output voltage. This resistive divider is composed of a resistor (R_{F1}) from the output voltage to the VEA negative input and a resistor (R_{F0}) from the VEA negative input to ground. R_{F1} is usually between 30 kΩ and 100 kΩ, and the value of R_{F0} is calculated as follows:

$$R_{F0} = \frac{R_{F1} \times V_{REF}}{V_{OUT} - V_{REF}} \quad [\Omega] \quad \text{(eq. 33)}$$

Where:
R_{F1}: [Ω]
V_{REF}: internal 0.8 V reference [V]

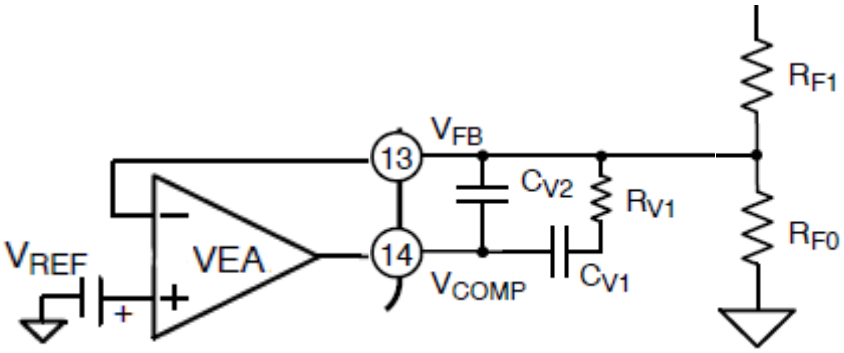


Figure 25. Voltage Error Amplifier (VEA) Compensation

(9) Voltage Error Amplifier (VEA) Compensator Design

As shown in Figure 25, Voltage Error Amplifier (VEA) compensation requires a pole (at the origin, via capacitor C_{V1}), and a mid−frequency zero that boosts phase at the 0 dB gain crossover frequency of the overall voltage−loop to assure adequate phase margin. A high frequency pole is also recommended to reduce gain at frequencies above which active regulation is not intended, and to avoid amplifying switching frequency output ripple voltage.

To set the zero, first select R_{V1} to set VEA gain such that overall voltage loop gain is 0 dB near $F_{SW}/8$ by:

$$R_{V1} = \frac{R_{F1} \times R_{CS}}{ESR_C} \quad [\Omega] \quad \text{(eq. 34)}$$

Where:
R_{CS}: current sense resistance [Ω]
ESR_C: Equivalent Series Resistance of the output capacitors

Select C_{V1} to place the VEA compensation zero half a decade below the 0 dB gain crossover frequency and produce flat VEA gain and boost phase at the crossover frequency by:

$$C_{V1} = \frac{24}{2 \times \pi \times F_{SW} \times R_{V1}} \quad [F] \quad \text{(eq. 35)}$$

Select C_{V1} to place the high frequency pole below the switching frequency to reduce the impact of switching noise on the regulation loop by:

$$C_{V2} = \frac{C_{V1}}{2 \times \pi \times f_{HFPV} \times R_{V1} \times C_{V1} - 1} \quad [F] \quad \text{(eq. 36)}$$

Where:
f_{HFPV}: frequency desired for the VEA high frequency pole

Thermal Considerations

The power dissipation of the NCV8856A varies with the MOSFETs used, the switching frequency, and V_{IN}. The average MOSFET gate current typically dominates the control IC power dissipation, which can be estimated as follows:

$$P_{IC} = V_{IN} \times I_Q + P_{TG} + P_{BG} \quad [W] \qquad \text{(eq. 37)}$$

Where:
P_{IC}: control IC power dissipation [W]
V_{IN}: Input (battery) voltage
I_Q: IC measured supply current (quiescent current) [A]
P_{TG}: high−side MOSFET gate driver loss [W]
P_{BG}: low−side MOSFET gate driver loss [W[

The high−side switching MOSFET gate driver loss is:

$$P_{TG} = Q_{TG} \times F_{SW} \times V_{IN} \qquad \text{(eq. 38)}$$

Where:
Q_{TG}: total high−side MOSFET gate charge at 6 V

The low−side synchronous rectifier MOSFET gate driver loss is:

$$P_{BG} = Q_{BG} \times F_{SW} \times V_{IN} \qquad \text{(eq. 39)}$$

Where:
Q_{BG}: total low−side MOSFET gate charge at 6 V

The junction temperature of the controller can then be estimated as follows:

$$T_J = T_A + P_{IC} \times R_{\theta JA} \qquad \text{(eq. 40)}$$

Where:
T_J = junction temperature of the IC
T_A = ambient temperature
$R_{\theta JA}$ = junction−to−ambient thermal resistance of the IC package

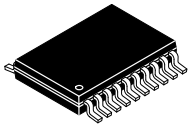
The package thermal resistance ($R_{\theta JA}$) can be obtained from the specifications section of this data sheet. It should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the IC impact the temperature of the device. These calculations may be used as a guide, but measurements should always be taken in the actual application.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

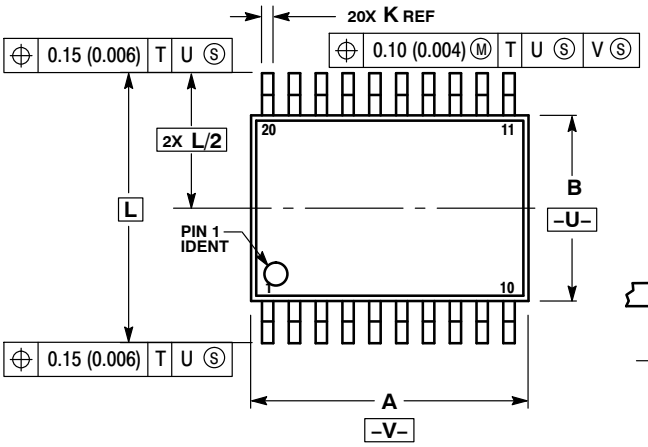
ON Semiconductor®

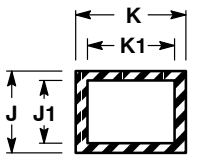
TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

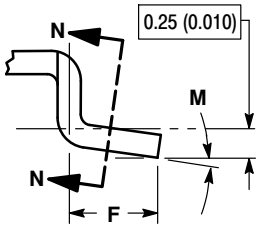


SCALE 2:1

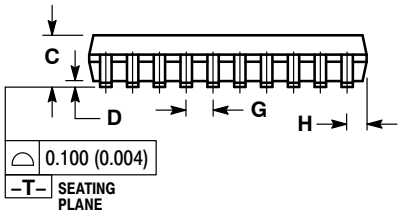


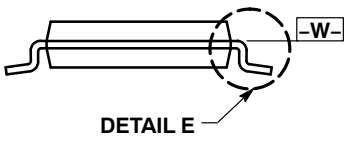


SECTION N−N



DETAIL E

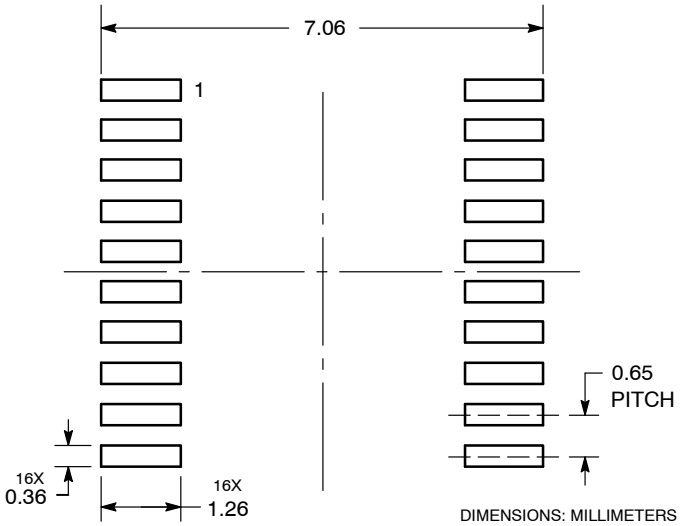




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

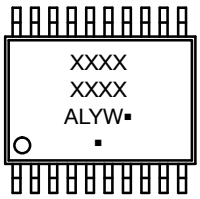
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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