NCV8445

Self Protected High Side Driver with Temperature Shutdown and Current Limit

The NCV8445 is a fully protected High−Side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids and other acuators. The device is internally protected from an overload condition by an active current limit and thermal shutdown.

A diagnostic output reports ON and OFF state open load conditions as well as thermal shutdown.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- CMOS (3.3 V / 5 V) compatible control input
- Open Load Detection in On and Off State
- Diagnostic Output
- Undervoltage and Overvoltage Shutdown
- Loss of Ground Protection
- ESD protection
- Slew Rate Control for Low EMI Switching
- Very Low Standby Current
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

ON Semiconductor®

MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751

V8445
ALYW

V8445 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS

GND	1	8 VD
IN	2	7 OUT
STAT	3	6 OUT
NC	4	5 VD
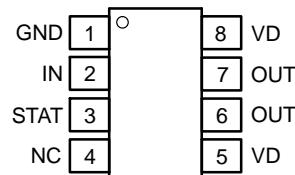
(Top View)

FEATURE SUMMARY

Operating Voltage Range	V_S	6 to 36	V
R_{DSon} (max), $T_J = 25°C$	R_{ON}	45	mΩ
Output Current Limit (min)	I_{lim}	6	A

ORDERING INFORMATION

Device	Package	Shipping[†]
NCV8445DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV8445
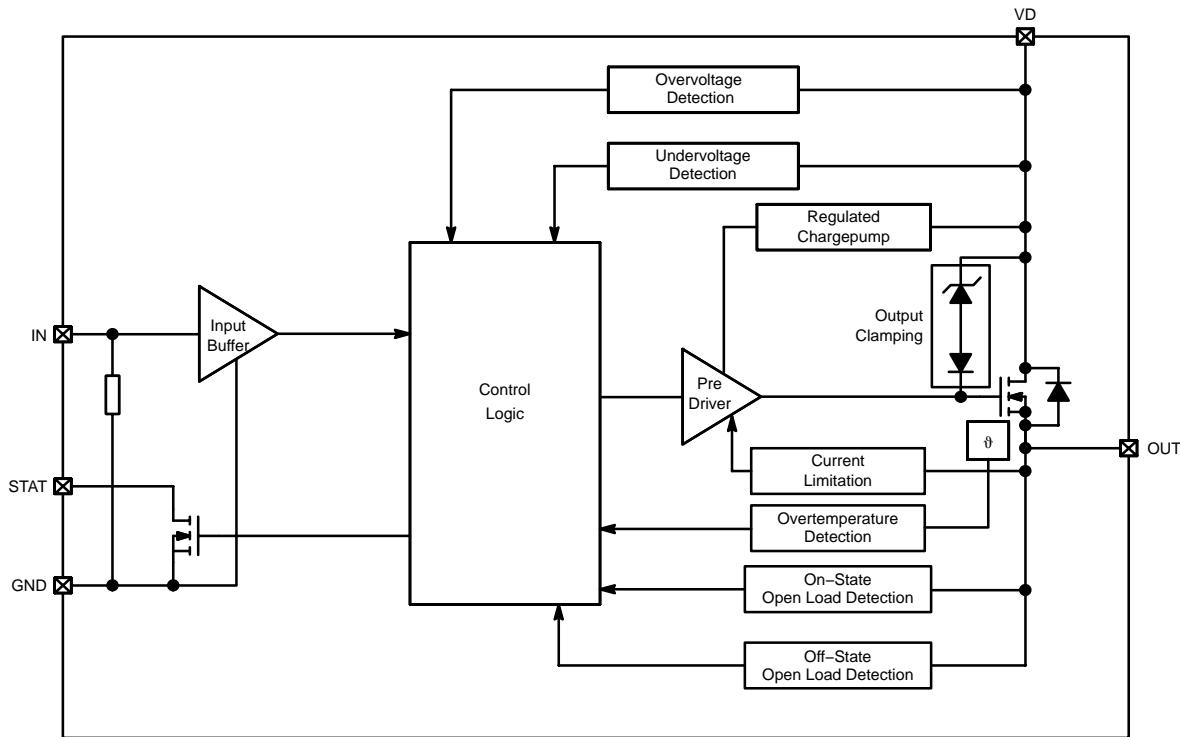
Figure 1. Block Diagram

PIN DESCRIPTION

Pin #	Symbol	Description
1	GND	Ground
2	IN	Logic Level Input
3	STAT	Status Output
4	N/C	No Connection
5	V_D	Supply Voltage
6	OUT	Output
7	OUT	Output
8	V_D	Supply Voltage

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
		Value		
DC Supply Voltage	V_D	−0.3	42	V
Peak Transient Input Voltage (Load Dump 42.5 V, V_D = 13.5 V, R_{LOAD} = 6.5 Ω, ISO7637−2 pulse 5)	V_{peak}		56	V
Input Voltage	V_{in}	−8	8	V
Input Current	I_{in}	−5	5	mA
Output Current (Note 1)	I_{out}	−6	Internally Limited	A
Negative Ground Current	$-I_{gnd}$	−200	–	mA
Status Current	I_{status}	−5	5	mA
Power Dissipation, T_A = 25°C	P_{tot}	1.183		W
Electrostatic Discharge (HBM Model 100 pF / 1500 Ω) Input Status Output V_D		4 3.5 5 5		DC kV kV kV kV
Single Pulse Inductive Load Switching Energy (Note 2) (L = 1.8 mH, V_{bat} = 13.5 V; I_L = 8.75 A, T_{Jstart} = 150°C)	E_{AS}	101.5		mJ
Operating Junction Temperature	T_J	−40	+150	°C
Storage Temperature	$T_{storage}$	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance.
2. Not subjected to production testing.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max Value	Unit
Thermal Resistance Junction−to−Lead Junction−to−Ambient (min. Pad) Junction−to−Ambient (1" square pad size, FR−4, 1 oz Cu)	$R_{\theta JL}$ $R_{\theta JA}$ $R_{\theta JA}$	30 110.8 105.6	°C/W °C/W °C/W

ELECTRICAL CHARACTERISTICS ($8 \leq V_D \leq 36$ V; $-40°C < T_J < 150°C$ unless otherwise specified)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
				Value		
Operating Supply Voltage	V_D		6	–	36	V
Undervoltage Shutdown	V_{UV}		3	5	6.5	V
Undervoltage Restart	V_{UV_Rst}				6.5	V
Overvoltage Shutdown	V_{OV}		36			V
On Resistance	R_{ON}	I_{out} = 2 A; T_J = 25°C, V_D > 8 V I_{out} = 2 A, V_D > 8 V			45 90	mΩ
Standby Current	I_D	Off State, $V_{in} = V_{out}$ = 0 V, V_D = 13.5 V On State; V_{in} = 5 V, V_D = 13.5 V, I_{out} = 0 A		10 2.0	20 4.0	μA mA
Output Leakage Current	I_L	$V_{in} = V_{out}$ = 0 V V_{in} = 0 V, V_{out} = 3.5 V $V_{in} = V_{out}$ = 0 V, V_D = 13.5 V	−12		10 5 5	μA

INPUT CHARACTERISTICS

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage – Low	V_{in_low}				1.25	V
Input Current – Low	I_{in_low}	V_{in} = 1.25 V	1			μA
Input Voltage – High	V_{in_high}		3.25			V
Input Current – High	I_{in_high}	V_{in} = 3.25 V			10	μA
Input Hysteresis Voltage	V_{hyst}		0.25			V
Input Clamp Voltage	V_{in_cl}	I_{in} = 1 mA I_{in} = −1 mA	12 −14	13 −13	14 −12	V

SWITCHING CHARACTERISTICS

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Turn–On Delay Time	t_{d_on}	to 10% V_{out}, V_D = 13.5 V, R_L = 6.5 Ω	5.0	30	55	μs
Turn–Off Delay Time	t_{d_off}	to 90% V_{out}, V_D = 13.5 V, R_L = 6.5 Ω	35	60	85	μs
Slew Rate On	dV_{out}/dt_{on}	10% to 80% V_{out}, V_D = 13.5 V, R_L = 6.5 Ω	0.1	0.4	0.8	V / μs
Slew Rate Off	dV_{out}/dt_{off}	90% to 10% V_{out}, V_D = 13.5 V, R_L = 6.5 Ω	0.1	0.5	0.8	V / μs

OUTPUT DIODE CHARACTERISTICS (Note 3)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Forward Voltage	V_F	I_{out} = −1.3 A, T_J = 150°C			0.6	V

STATUS PIN CHARACTERISTICS

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Status Output Voltage Low	V_{stat_low}	I_{stat} = 1.6 mA		0.2	0.5	V
Status Leakage Current	$I_{stat\_leakage}$	V_{stat} = 5 V		0.3	2.0	μA
Status Pin Input Capacitance	C_{stat}	V_{stat} = 5 V (Note 3)			100	pF
Status Clamp Voltage	V_{stat_cl}	I_{stat} = 1 mA I_{stat} = −1 mA	10 −2.2	11 −1.2	13 −0.6	V

PROTECTION FUNCTIONS (Note 4)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Temperature Shutdown (Note 3)	T_{SD}		150	175	200	°C
Temperature Shutdown Hysteresis (Note 3)	T_{SD_hyst}		7	15		°C
Output Current Limit	I_{lim}	8 V < V_D < 36 V	9	15	24	A
		6 V < V_D < 36 V	6	11	18	A
Status Delay in Overload (Note 3)	t_{d_stat}				20	μs
Switch Off Output Clamp Voltage	V_{clamp}	I_{out} = 2 A, V_{in} = 0 V, L = 6 mH	V_D − 43	V_D − 46	V_D − 50	V

3. Not subjected to production testing
4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles.

ELECTRICAL CHARACTERISTICS (8 ≤ V_D ≤ 36 V; −40°C < T_J < 150°C unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
DIAGNOSTICS CHARACTERISTICS						
Openload On State Detection Threshold	I_{OL}	V_{in} = 5 V	30		500	mA
Openload On State Detection Delay	$t_{d\_OL\_on}$	I_{out} = 0 A		100	200	µs
Openload Off State Detection Threshold	V_{OL}	V_{in} = 0 V	1.5	2.4	3.5	V
Openload Detection Delay at Turn Off	$t_{d\_OL\_off}$			150	350	µs

3. Not subjected to production testing
4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
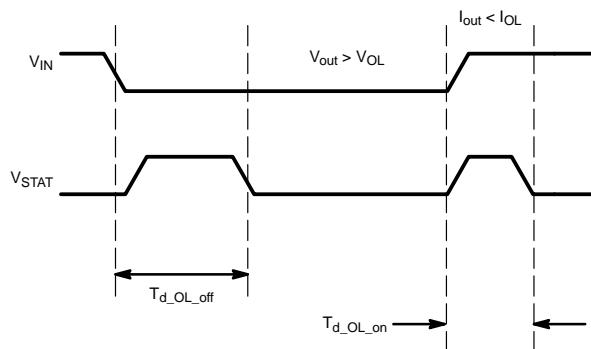
Figure 2. Open Load Status Timing (with external pull−up)
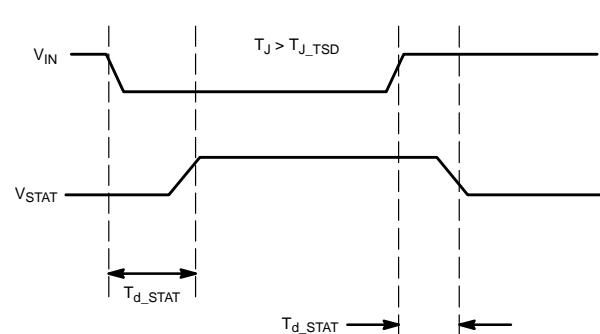
Figure 3. Overtemperature Status Timing
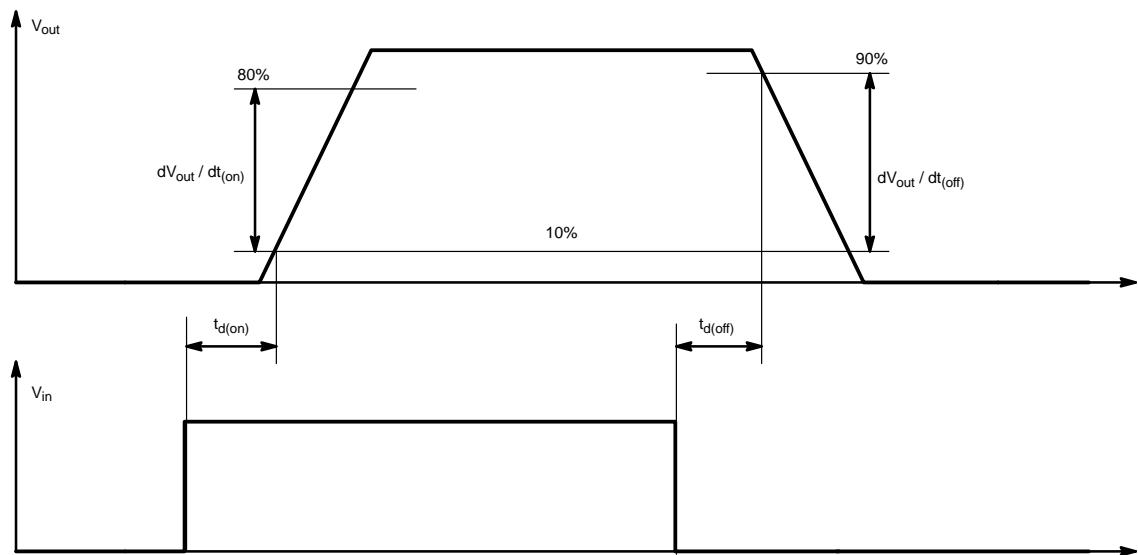
Figure 4. Switching Timing Diagram

STATUS PIN TRUTH TABLE

Conditions	Input	Output	Status
Normal Operation	L H	L H	H H
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Current Limitation	L H H	L X X	H $(T_J < T_{SD})$ H $(T_J > T_{SD})$ L
Overtemperature	L H	L L	H L
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

TYPICAL CHARACTERISTICS CURVES
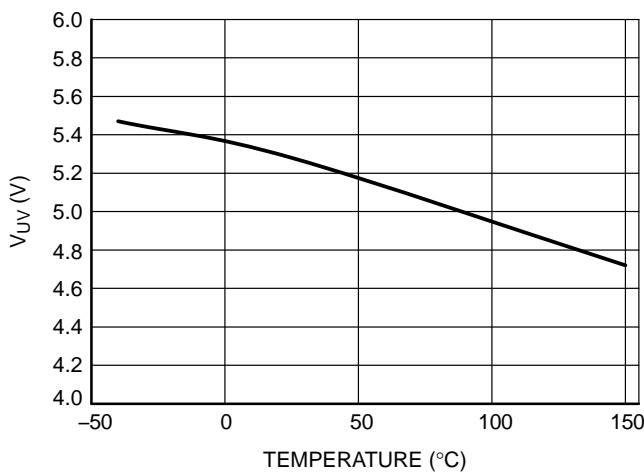
Figure 5. Undervoltage Shutdown vs. Temperature
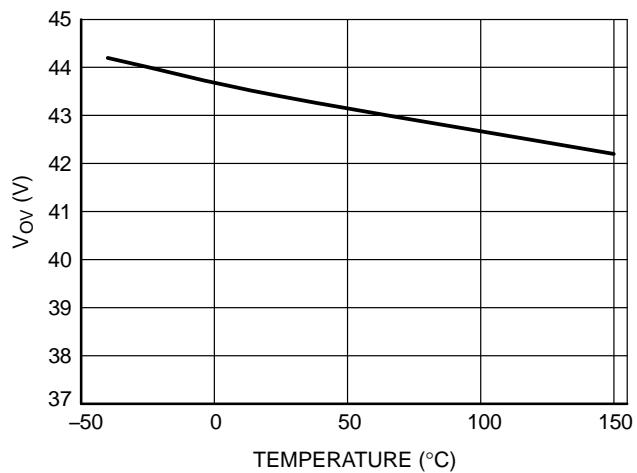
Figure 6. Overvoltage Shutdown vs. Temperature
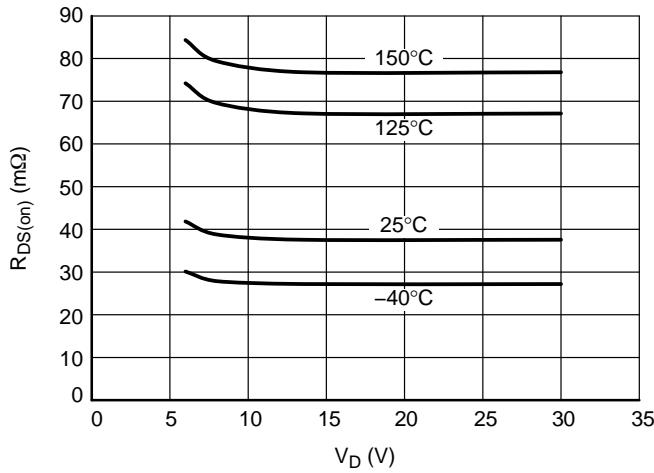
Figure 7. $R_{DS(on)}$ Over Temperature and Battery
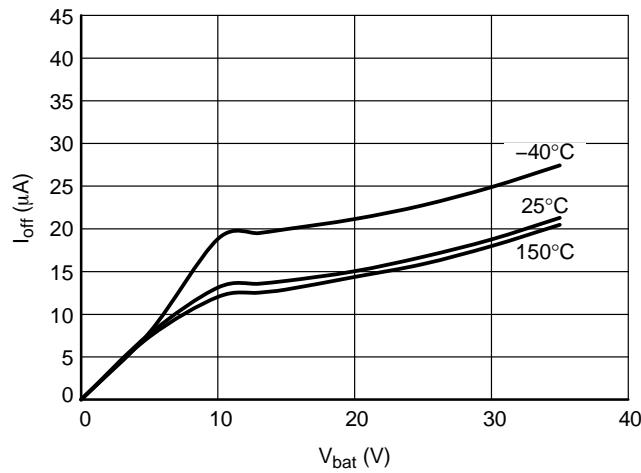
Figure 8. OFF State Standby Current Leakage vs. V_{bat} and Temperature
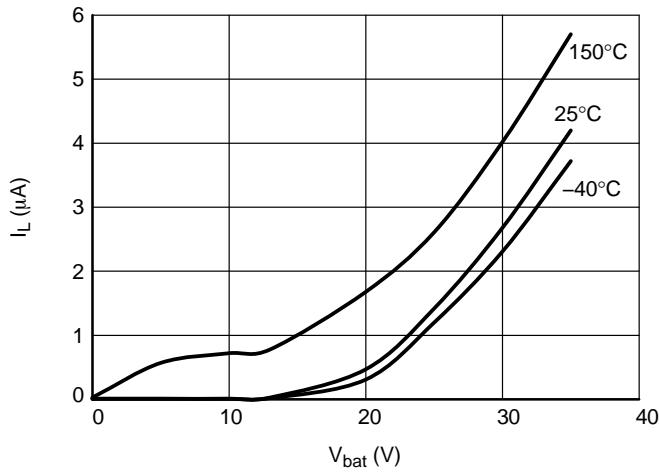
Figure 9. Output Leakage vs. V_{bat} and Temperature, V_{out} = 0 V
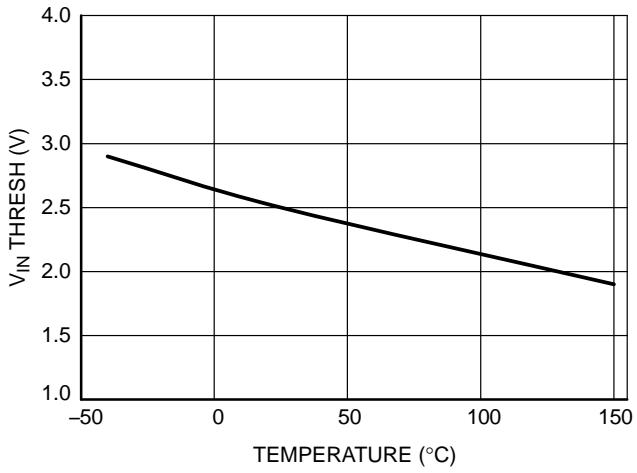
Figure 10. V_{in} Threshold High vs. Temperature

TYPICAL CHARACTERISTICS CURVES
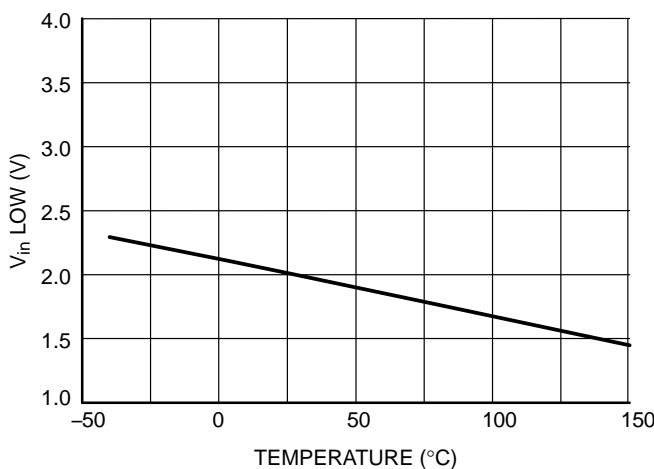
Figure 11. V_{in} Threshold Low vs. Temperature
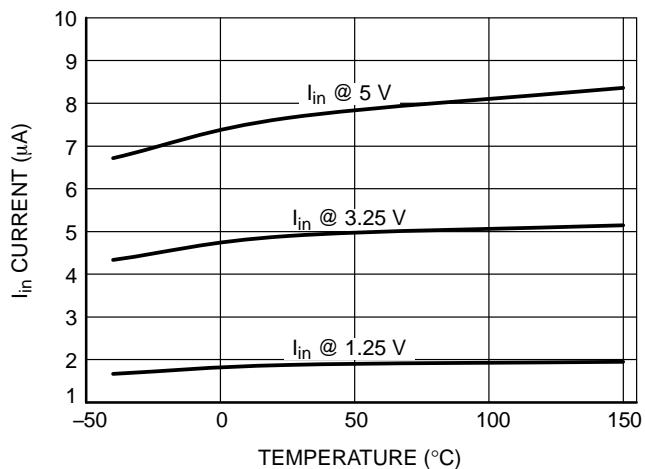
Figure 12. Input Current vs. Temperature
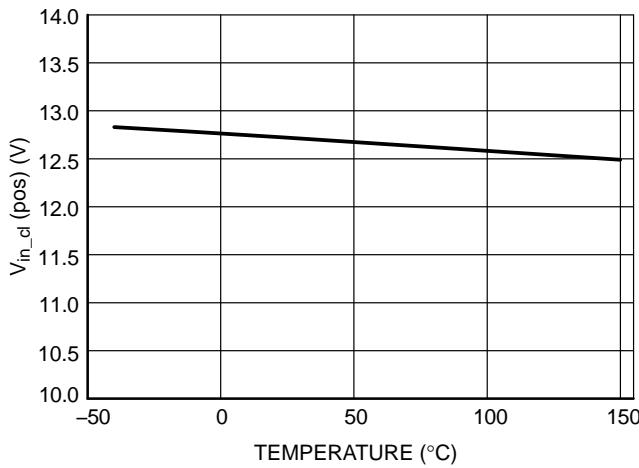
Figure 13. Input Clamp Voltage (Positive) vs. Temperature
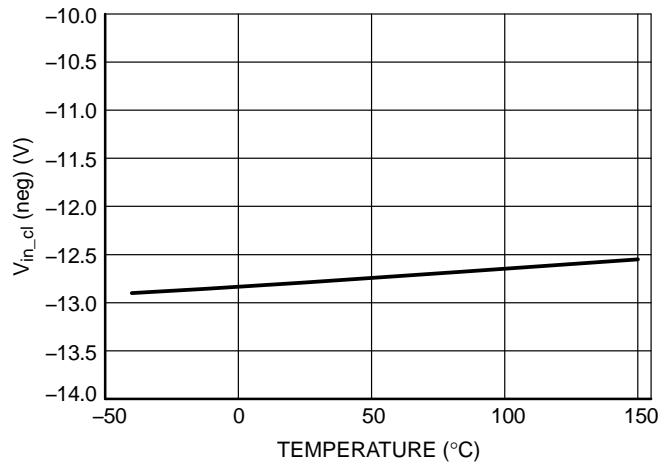
Figure 14. Input Clamp Voltage (Negative) vs. Temperature
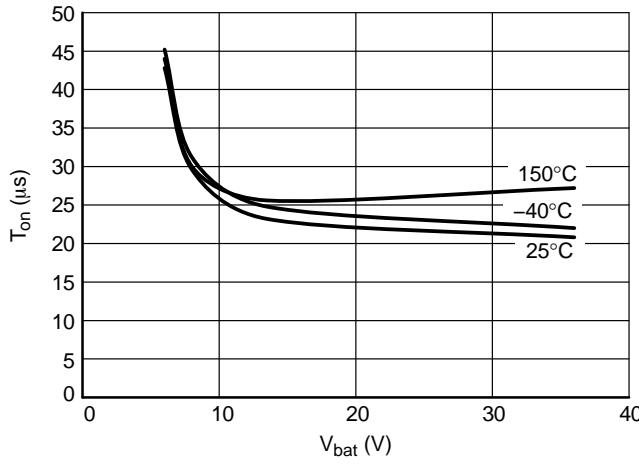
Figure 15. Turn On Delay Time vs. V_{bat} and Temperature
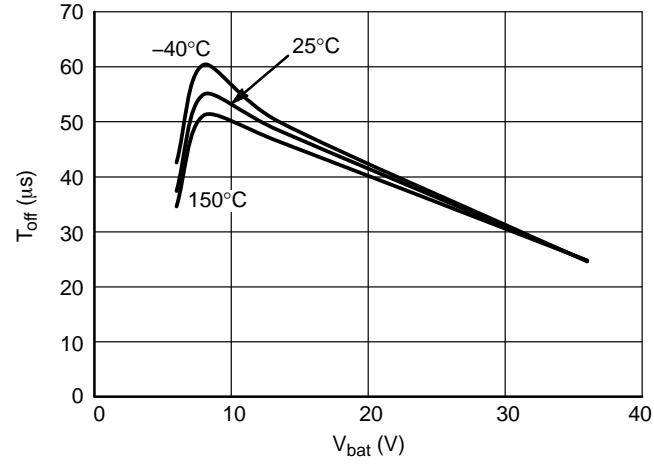
Figure 16. Turn Off Delay Time vs. V_{bat} and Temperature

TYPICAL CHARACTERISTICS CURVES
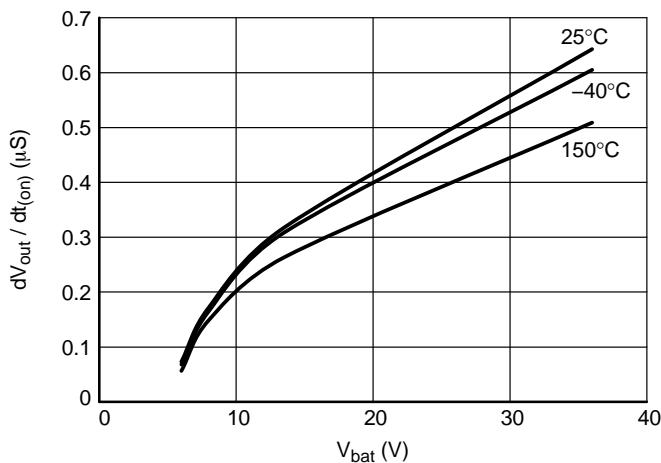
Figure 17. Slew Rate ON vs. V$_{bat}$ and Temperature
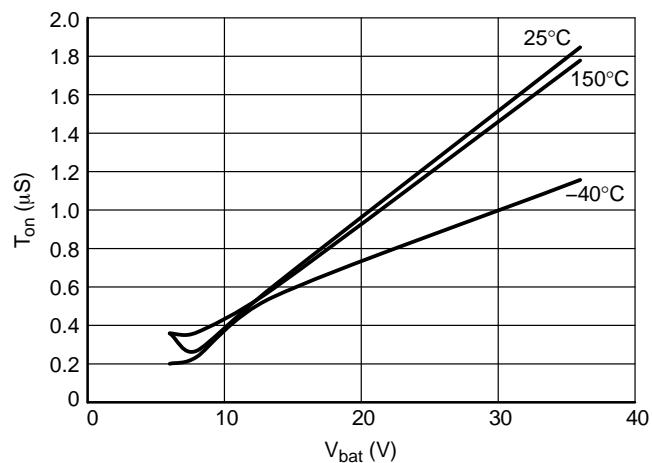
Figure 18. Slew Rate OFF vs. V$_{bat}$ and Temperature
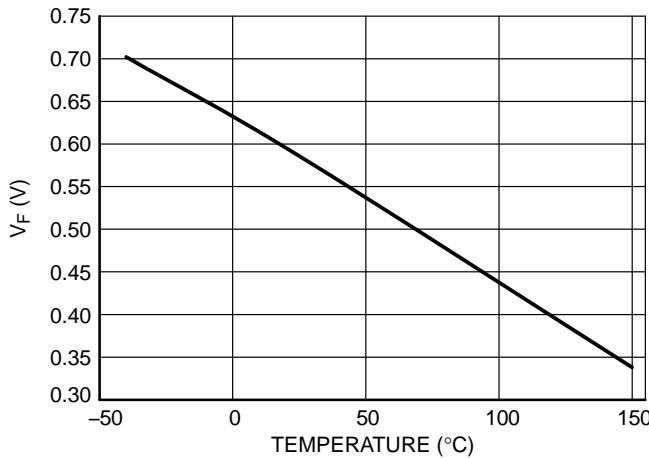
Figure 19. Forward Voltage (@ −1.3 A) vs. Temperature
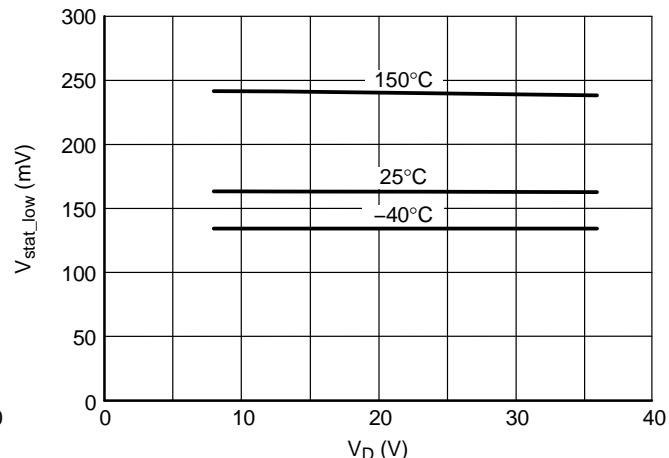
Figure 20. STAT Low Voltage vs. V$_D$
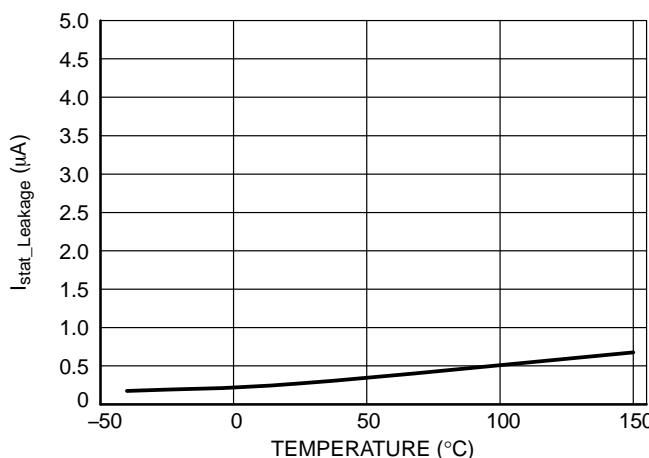
Figure 21. Status Leakage Current vs. Temperature
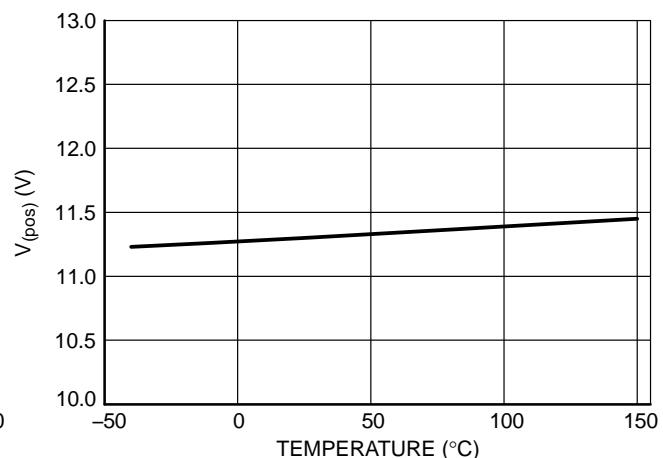
Figure 22. Status Clamp Voltage (Positive) vs. Temperature

TYPICAL CHARACTERISTICS CURVES
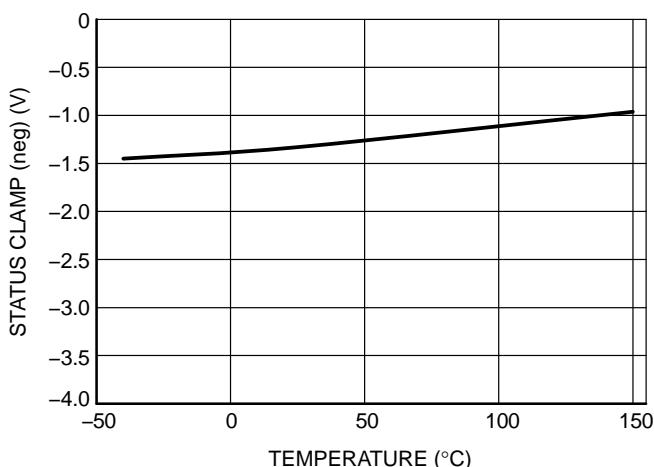
Figure 23. Status Clamp Voltage (Negative) vs. Temperature
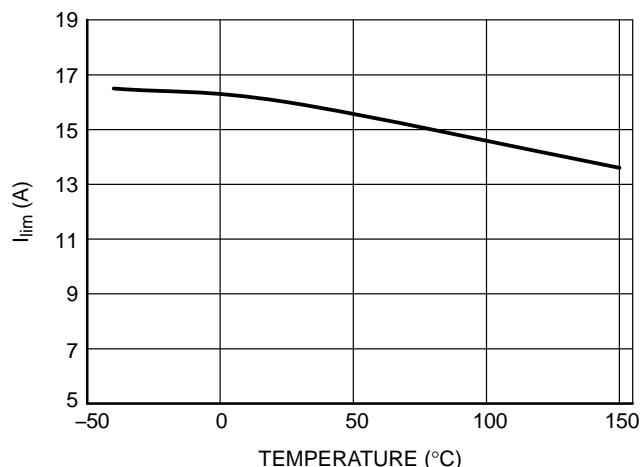
Figure 24. Current Limit vs. Temperature $V_D = 13.5$ V
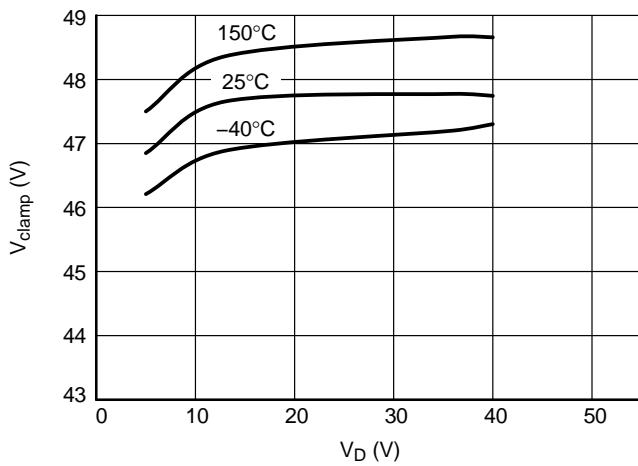
Figure 25. Turn Off Output Clamp Voltage vs. V_D and Temperature
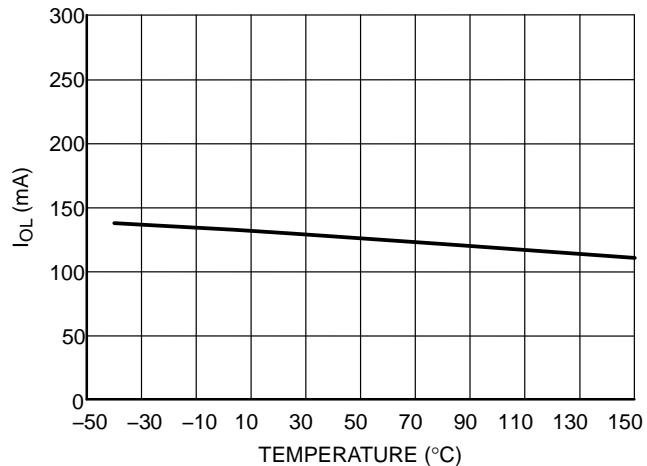
Figure 26. ON State Open Load Detection vs. Temperature $V_D = 13.5$ V
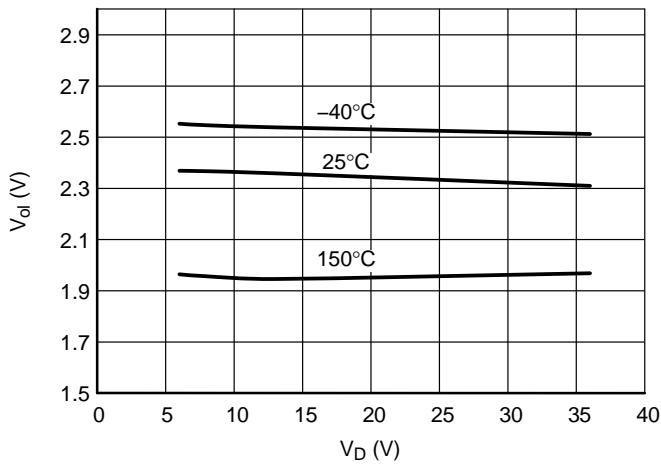
Figure 27. Off State OL Detection Threshold vs. V_D and Temperature
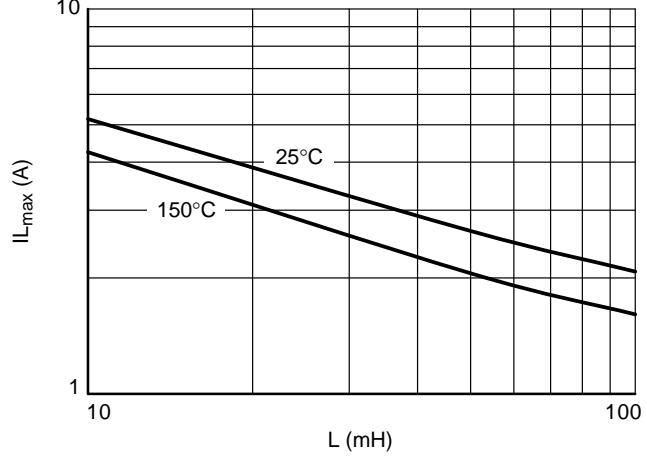
Figure 28. Single–Pulse Maximum Switch–off Current vs. Load Inductance

NCV8445

TYPICAL CHARACTERISTICS CURVES
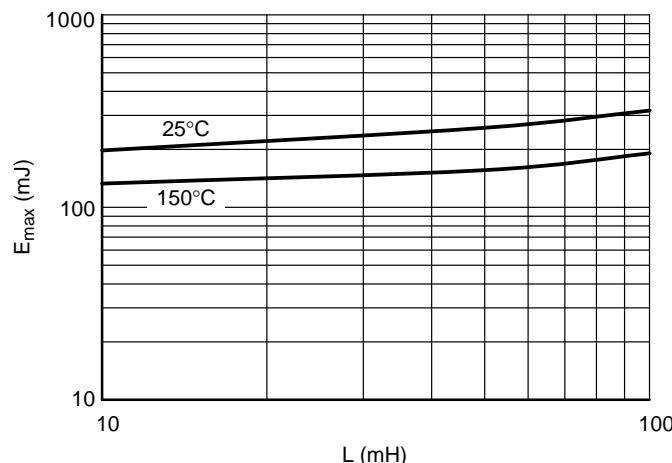
**Figure 29. Single−Pulse Maximum Switch−off
Current vs. Load Inductance**

ISO 7637−2: 2004(E) PULSE TEST RESULTS

ISO 7637−2:2004(E)	Test Levels				Delays and
Test Pulse	**I**	**II**	**III**	**IV**	**Impedance**
1	−25 V	−50 V	−75 V	−100 V	2 ms, 10 Ω
2a	+25 V	+50 V	+37 V	+50 V	0.05 ms, 10 Ω
3a	−25 V	−50 V	−112 V	−150 V	0.1 μs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs, 50 Ω
4	−4 V	−5 V	−6 V	−7 V	5 s, .01 Ω
5 (Load Dump)	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO 7637−2:2004(E)	Test Results			
Test Pulse	**I**	**II**	**III**	**IV**
1	C	C	C	C
2a	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5 (Load Dump)	C	E	E	E

| Class	Functional Status
A	All functions of a device perform as designed during and after exposure to disturbance.
B	All functions of a device perform as designed during exposure. However,one or more of
	them can go beyond specified tolerance. All functions return automatically to within normal
	limits after exposure is removed. Memory functions shall remain class A.
C	One or more functions of a device do not perform as designed during exposure but return
	automatically to normal operation after exposure is removed.
D	One or more functions of a device do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device is reset by simple
E	One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.

NCV8445
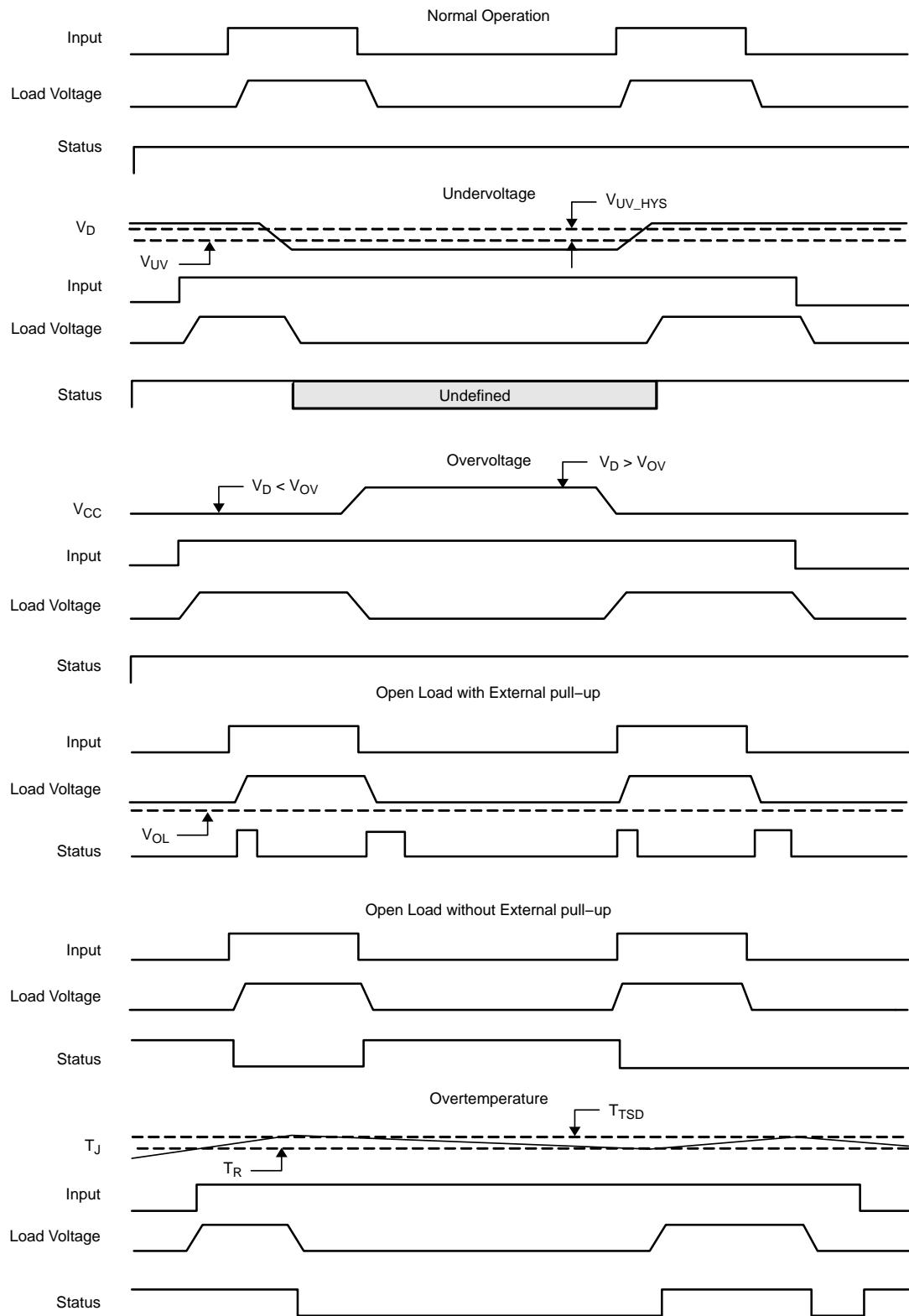
Figure 30. Waveforms

NCV8445
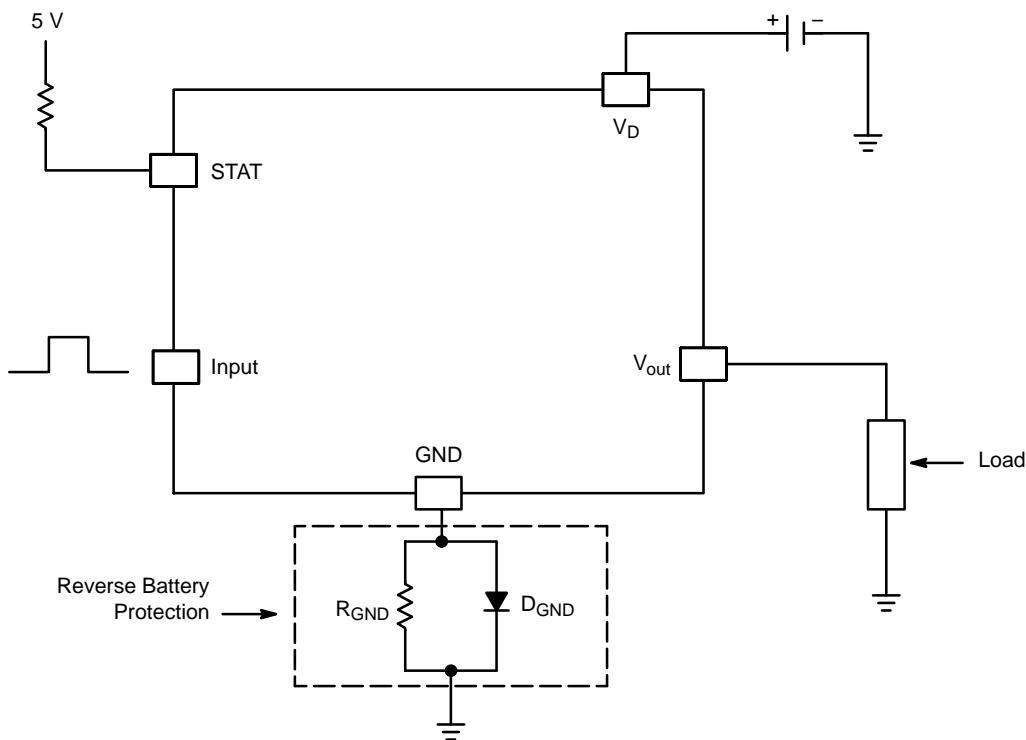
Figure 31. Application Diagram

Reverse Battery Protection

An external resistor R_{GND} is required to adequately protect the device from a Reverse Battery event. The resistor value can be calculated using the following two formulas.

1. $R_{GND} \geq 600\ mV\ /\ (I_d\ (on)\ max)$
2. $R_{GND} \geq (-V_D)\ /\ (-I_{gnd})$

Maximum $(-I_{gnd})$ current, which is the reverse GND pin current, can be found in the Maximum Ratings section. Several High Side Devices can share same the reverse battery protection resistor. Please note that the sum of $(I_d$ (on) max) of all devices should be used to calculate R_{GND} value. If the microprocessor ground is not common with the device ground, R_{GND} will produce a voltage offset ($(I_d$ (on) max) x R_{GND}) with respect to the IN and STAT pins.

This offset will be increased when more than one device shares the resistor.

Power Dissipation during a reverse battery event is equal to:

$$P_D = \left(- V_D \right)^2 / R_{GND}$$

In the case of high power dissipation due to several devices sharing R_{GND}, it is recommended to place a diode D_{GND} in the ground path as an alternate reverse battery protection method. When driving an inductive load, a 1 kΩ resistor should be placed in parallel with the D_{GND} diode. This method will also produce a voltage offset of ~600 mV with respect to the IN and STAT pins. This diode can also be shared amongst several High Side Devices. This voltage offset will vary if D_{GND} is shared by multiple devices.
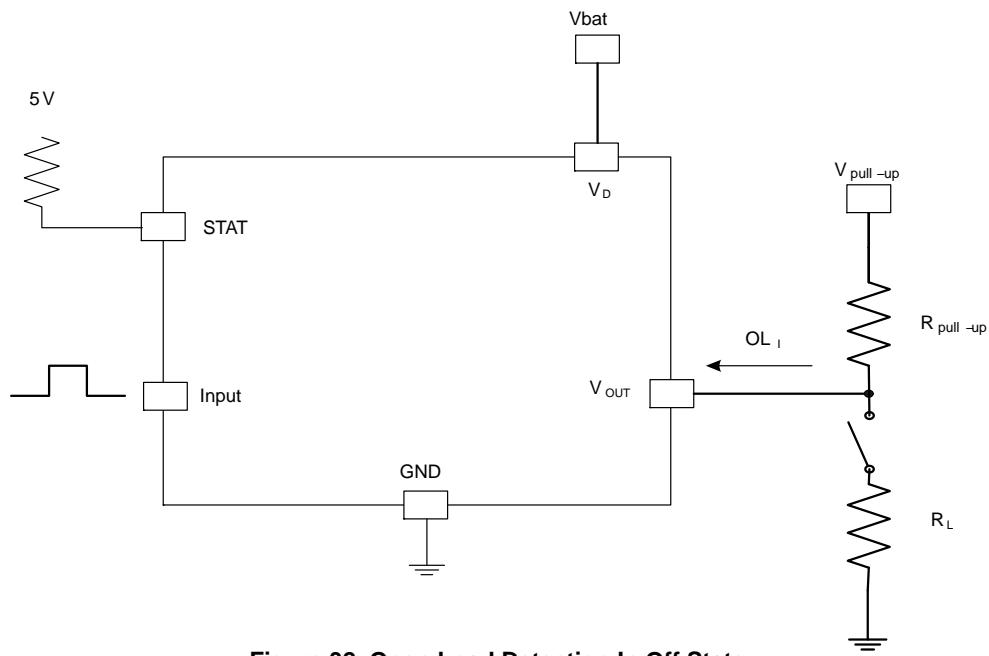
Figure 32. Open Load Detection In Off State

OFF State Open Load Detection

Off State Open Load Detection requires an external pull-up resistor ($R_{pull-up}$) connected between V_{OUT} pin and a positive supply voltage ($V_{pull-up}$).

The external $R_{pull-up}$ resistor value should be selected to ensure that a false OFF State OL condition is not detected when the load (R_L) is connected. A V_{OUT} voltage above the V_{OL_min} (Openload Off State Detection Threshold) minimum value with the load (R_L) connected needs to be avoided. The following formula shows this relationship:

$$V_{OUT} = \left(V_{pull-up}/\left(R_L + R_{pull-up}\right)\right) R_L < V_{OL\_min}$$

In addition to ensuring the selected $R_{pull-up}$ resistor value does not cause a false OFF State OL detection condition when the load is connected, the $R_{pull-up}$ must also not cause the OFF State OL to miss detecting an OL condition when the load is disconnected. A V_{OUT} voltage below the V_{OL_max} (Openload Off State Detection Threshold) maximum value with the load (R_L) disconnected needs to be avoided. The following formula shows this relationship:

$$R_{pull-up} < \left(V_{pull-up} - V_{OL\_max}\right)/OL_1$$

$$OL_1 = I_L\left(\text{Output Leakage with } V_{OUT} = 3.5 \text{ V}\right)$$

Because I_d (OFF) may significantly increase if V_{OUT} is pulled high (up to several mA), $R_{pull-up}$ resistor should be connected to a supply that is switched OFF when the module is in standby.
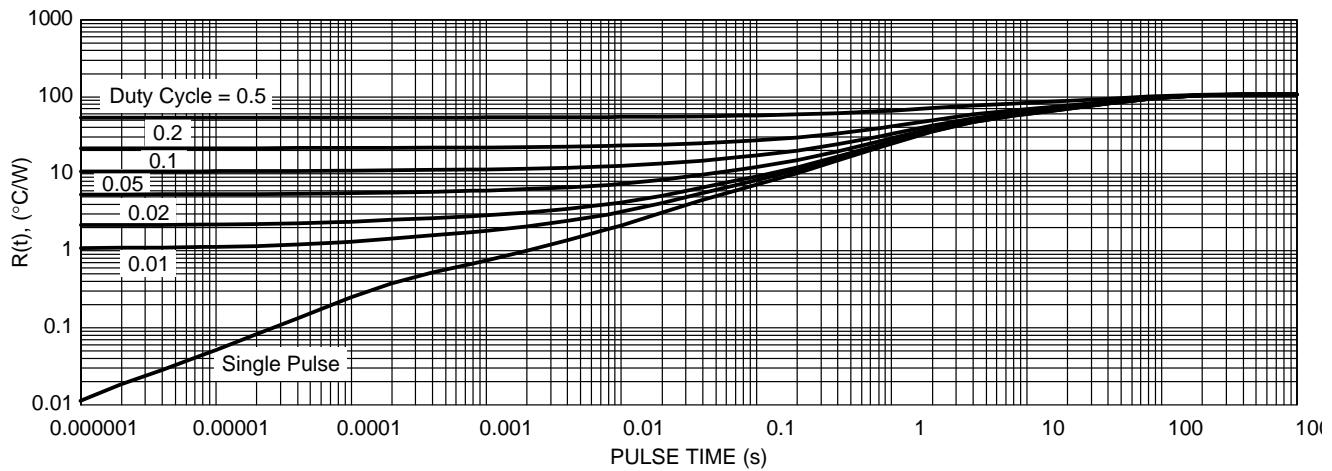
Figure 33. Transient Thermal Impedance
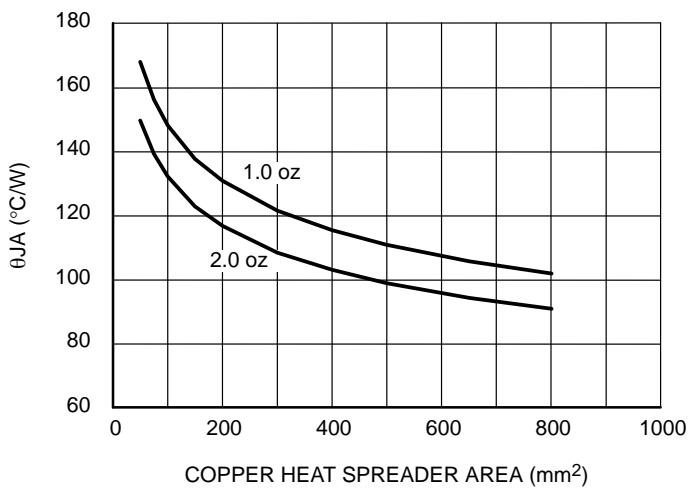
Figure 34. R$_{\theta JA}$ vs Copper Area

ON Semiconductor®

SOIC−8 NB
CASE 751−07
ISSUE AK

SCALE 1:1

8

1

DATE 16 FEB 2011

−X−

A

B

8   5

1   4

−Y−

S

⊕ | 0.25 (0.010) Ⓜ | Y Ⓜ

G

K

C

SEATING PLANE

−Z−

N X 45°

⬒ | 0.10 (0.004)

H

D

M

J

⊕ | 0.25 (0.010)Ⓜ | Z | Y Ⓢ | X Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

1.52
0.060

7.0
0.275

4.0
0.155

0.6
0.024

1.270
0.050

SCALE 6:1   (mm/inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*
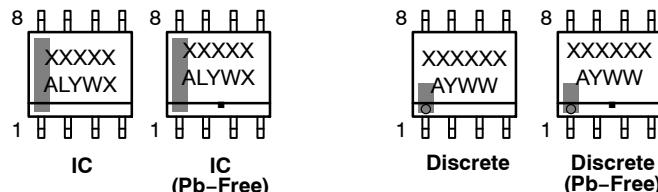
8 XXXXX ALYWX
1

IC

8 XXXXX ALYWX
1

IC (Pb−Free)

8 XXXXXX AYWW
1

Discrete

8 XXXXXX AYWW
1

Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B		
DESCRIPTION:	SOIC−8 NB		PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−8 NB		**PAGE 2 OF 2**

PUBLICATION ORDERING INFORMATION

◊

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:

  NCV8445DR2G