# Isolated High Current IGBT Gate Driver

# NCD57001F

NCD57001F is a variant of NCD57001 with reduced Soft−Turn−Off time suited to drive large IGBTs or power modules. NCD57001F is a high−current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, and soft turn−off at DESAT. NCD57001F accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCD57001F provides >5 kVrms (UL1577 rating) galvanic isolation and >1200 $V_{iorm}$ (working voltage) capabilities. NCD57001F is available in the wide−body SOIC−16 package with guaranteed 8 mm creepage distance between input and output to fulfill reinforced safety insulation requirements.

## Features
- High Current Output (+4/−6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- Active Miller Clamp to Prevent Spurious Gate Turn−on
- DESAT Protection with Programmable Delay
- Typ 550 ns Soft Turn Off during IGBT Short Circuit
- IGBT Gate Clamping during Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2
- 3.3 V to 5 V Input Supply Voltage
- 5000 V Galvanic Isolation (to meet UL1577 requirements)
- 1200 V Working Voltage (per VDE0884−10 requirements)
- High transient immunity
- High electromagnetic immunity
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant
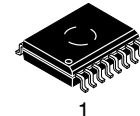
## Typical Applications
- Automotive Power Supplies
- HEV/EV Powertrain
- BSG Inverter
- PTC Heater

## ON Semiconductor®

**SOIC−16 WB**
**CASE 751G−03**

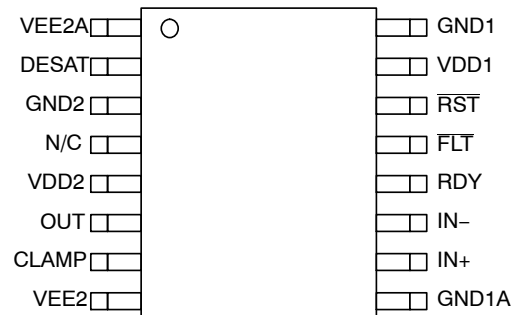## MARKING DIAGRAM

NCD57001F
DWR2G
AWLYYWWG

| | |
|---|---|
| NCD57001FDWR2G | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

## PIN CONNECTIONS

| | |
|---|---|
| VEE2A | GND1 |
| DESAT | VDD1 |
| GND2 | $\overline{RST}$ |
| N/C | $\overline{FLT}$ |
| VDD2 | RDY |
| OUT | IN− |
| CLAMP | IN+ |
| VEE2 | GND1A |

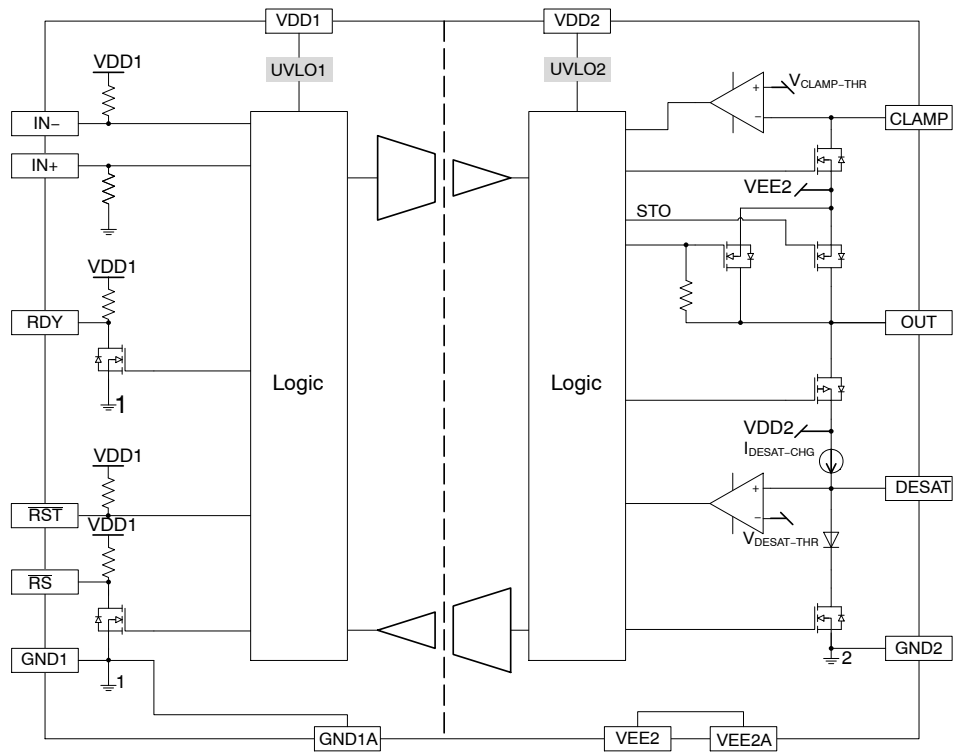## ORDERING INFORMATION

# NCD57001F



**Figure 1. Simplified Block Diagram**
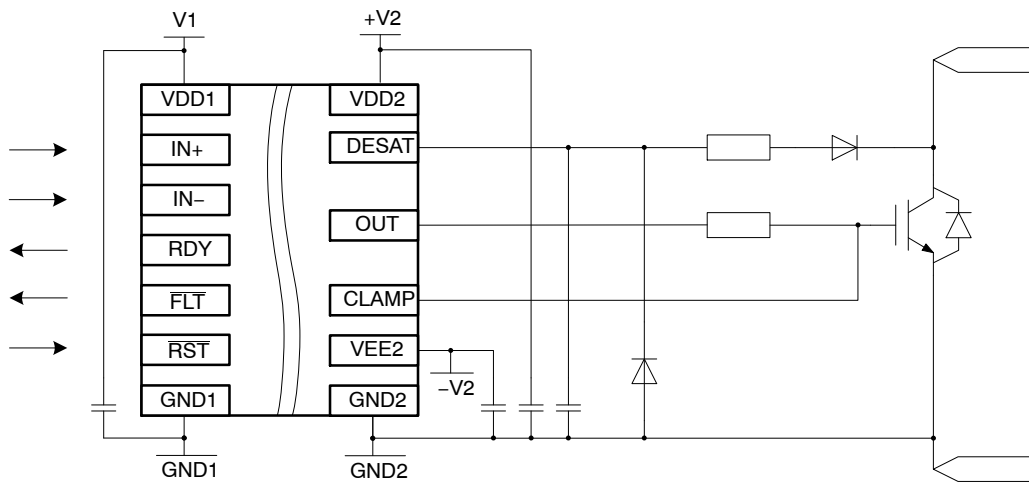


**Figure 2. Simplified Application Schematics**

## Table 1. PIN FUNCTION DESCRIPTION

| Pin Name | No. | I/O | Description |
|---|---|---|---|
| $V_{EE2A}$ | 1 | Power | Output side negative power supply. A good quality bypassing capacitor is required from these pins to GND2 and should be placed close to the pins for best results. Connect it to GND2 for unipolar supply application. |
| $V_{EE2}$ | 8 | | |
| DESAT | 2 | I/O | Input for detecting the desaturation of IGBT due to a short circuit condition. An internal constant current source $I_{DESAT-CHG}$ charging an external capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering. When the DESAT voltage goes up and reaches $V_{DESAT-THR}$, the output is driven low. Further, the $\overline{FLT}$ output is activated, please refer to Figure 5. <br><br> A 5 μs mute time apply to IN+ and IN− once DESAT occurs. |
| GND2 | 3 | Power | Output side gate drive reference connecting to IGBT emitter or FET source. |
| N/C | 4 | −− | Not connected. |
| $V_{DD2}$ | 5 | Power | Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results. |
| OUT | 6 | O | Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. OUT is actively pulled low during start−up and under Fault conditions. |
| CLAMP | 7 | I/O | Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn−on. Its internal N FET is turned on when the voltage of this pin falls below $V_{EE2} + V_{CLAMP-THR}$. It is to be tied directly to IGBT/FET gate with minimum trace length for best results. |
| GND1 | 9 | Power | Input side ground reference. |
| | 16 | | |
| IN+ | 10 | I | Non inverted gate driver input. It is internally clamped to $V_{DD1}$ and has a pull−down resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive going pulse−width is required at IN+ before OUT responds. |
| IN− | 11 | I | Inverted gate driver input. It is internally clamped to $V_{DD1}$ and has a pull−up resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum negative going pulse−width is required at IN− before OUT responds. |
| RDY | 12 | O | Power good indication output, active high when $V_{DD2}$ is good. There is an internal 50 kΩ pull−up resistor connected to this pin. Multiple of them from different drivers can be "OR"ed together. <br> If a low RDY event is triggered by UVLO2, the maximum low duration for RDY is 200 ns. <br> OUT remains low when RDY is low. Short time delay may apply. See Figure 4 for details. |
| $\overline{FLT}$ | 13 | O | Fault output (active low) that allows communication to the main controller that the driver has encountered a desaturation condition and has deactivated the output. |
| $\overline{RST}$ | 14 | I | Reset input with an internal 50 kΩ pull−up resistor, active low to reset fault latch. |
| $V_{DD1}$ | 15 | Power | Input side power supply (3.3 V to 5 V). |

## Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1) Over operating free−air temperature range unless otherwise noted

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Supply voltage, input side | $V_{DD1}-GND1$ | −0.3 | 6 | V |
| Positive Power Supply, output side | $V_{DD2}-GND2$ | −0.3 | 25 | V |
| Negative Power Supply, output side | $V_{EE2}-GND2$ | −10 | 0.3 | V |
| Differential Power Supply, output side | $V_{DD2}-V_{EE2}$ ($V_{MAX2}$) | 0 | 25 | V |
| Gate−driver output voltage | $V_{OUT}$ | $V_{EE2} - 0.3$ | $V_{DD2} + 0.3$ | V |
| Gate−driver output sourcing current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{MAX2}$ = 20 V) | $I_{PK-SRC}$ | | 7.8 | A |
| Gate−driver output sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{MAX2}$ = 20 V) | $I_{PK-SNK}$ | | 7.1 | A |
| Clamp sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{CLAMP}$ = 3 V) | $I_{PK-CLAMP}$ | | 2.5 | A |
| Maximum Short Circuit Clamping Time ($I_{OUT\_CLAMP}$ = 500 mA) | $t_{CLP}$ | | 10 | μs |
| Voltage at IN+, IN−, $\overline{RST}$, $\overline{FLT}$, RDY | $V_{LIM}-GND1$ | −0.3 | $V_{DD1} + 0.3$ | V |
| Output current of $\overline{FLT}$, RDY | $I_{LIM}-GND1$ | | 10 | mA |
| Desat Voltage | $V_{DESAT}-GND2$ | −0.3 | $V_{DD2} + 0.3$ | V |
| Clamp Voltage | $V_{CLAMP}-GND2$ | $V_{EE2} - 0.3$ | $V_{DD2} + 0.3$ | V |
| Power Dissipation SOIC−16 wide package | PD | | | mW |
| Input to Output Isolation Voltage | $V_{ISO}$ | −1200 | 1200 | V |
| Maximum Junction Temperature | TJ(max) | −40 | 150 | °C |
| Storage Temperature Range | TSTG | −65 | 150 | °C |
| ESD Capability, Human Body Model (Note 2) | ESDHBM | | ±2 | kV |
| ESD Capability, Charged Device Model (Note 2) | ESDCDM | | ±2 | kV |
| Moisture Sensitivity Level | MSL | | 1 | − |
| Lead Temperature Soldering Reflow, Pb−Free Versions (Note 3) | $T_{SLD}$ | | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 25°C.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Table 3. THERMAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| RJA | Thermal Resistance, Junction−to−Air | 100 mm$^2$, 1 oz Copper, 1 Surface Layer | 150 | °C/W |
| | | 650 mm$^2$, 1 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers | 84 | |

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm$^2$ (or 0.16 in$^2$) of 1 oz copper thickness and FR4 PCB substrate.

### Table 4. OPERATING RANGES (Note 6)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage, input side | $V_{DD1}$–GND1 | UVLO1 | 5.5 | V |
| Positive Power Supply, output side | $V_{DD2}$–GND2 | UVLO2 | 24 | V |
| Negative Power Supply, output side | $V_{EE2}$–GND2 | −10 | 0 | V |
| Differential Power Supply, output side | $V_{DD2}$–$V_{EE2}$ ($V_{MAX2}$) | 0 | 24 | V |
| Low level input voltage at IN+, IN−, $\overline{RST}$ | $V_{IL}$ | 0 | $0.3 \times V_{DD1}$ | V |
| High level input voltage at IN+, IN−, $\overline{RST}$ | $V_{IH}$ | $0.7 \times V_{DD1}$ | $V_{DD1}$ | V |
| Common Mode Transient Immunity (1500 V) | $|dV_{ISO}/dt|$ | 100 | | kV/μs |
| Ambient Temperature | $T_A$ | −40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

### Table 5. ELECTRICAL CHARACTERISTICS ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V.)

For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | | |
| UVLO1 Output Enabled | | $V_{UVLO1-OUT-ON}$ | | | 3.0 | V |
| UVLO1 Output Disabled | | $V_{UVLO1-OUT-OFF}$ | 2.4 | | | V |
| UVLO1 Hysteresis | | $V_{UVLO1-HYST}$ | 0.125 | | | V |
| UVLO2 Output Enabled | | $V_{UVLO2-OUT-ON}$ | 13.2 | 13.5 | 13.8 | V |
| UVLO2 Output Disabled | | $V_{UVLO2-OUT-OFF}$ | 12.2 | 12.5 | 12.8 | V |
| UVLO2 Hysteresis | | $V_{UVLO2-HYST}$ | | 1 | | V |
| Input Supply Quiescent Current Output Low | IN+ = Low, IN− = Low | $I_{DD1-0}$ | | 1 | 2 | mA |
| | RDY = High, $\overline{FLT}$ = High | | | | | |
| Input Supply Quiescent Current Output High | IN+ = High, IN− = Low | $I_{DD1-100}$ | | 4.8 | 6 | mA |
| | RDY = High, $\overline{FLT}$ = High | | | | | |
| Output Positive Supply Quiescent Current, Output Low | IN+ = Low, IN− = Low | $I_{DD2-0}$ | | 3.3 | 4 | mA |
| | RDY = High, $\overline{FLT}$ = High, no load | | | | | |
| Output Positive Supply Quiescent Current, Output High | IN+ = High, IN− = Low | $I_{DD2-100}$ | | 4 | 5 | mA |
| | RDY = High, $\overline{FLT}$ = High, no load | | | | | |
| Output Negative Supply Quiescent Current, Output Low | IN+ = High, IN− = Low, no load | $I_{EE2-0}$ | | 0.4 | 2 | mA |
| Output Negative Supply Quiescent Current, Output High | IN+ = High, IN− = Low, no load | $I_{EE2-100}$ | | 0.2 | 2 | mA |
| **LOGIC INPUT AND OUTPUT** | | | | | | |
| IN+, IN−, $\overline{RST}$ Low Input Voltage | | $V_{IL}$ | | | $0.3 \times V_{DD1}$ | V |
| IN+, IN−, $\overline{RST}$ High Input Voltage | | $V_{IH}$ | $0.7 \times V_{DD1}$ | | | V |
| Input Hysteresis Voltage | | $V_{IN-HYST}$ | | $0.15 \times V_{DD1}$ | | V |
| IN−, $\overline{RST}$ Input current (50 kΩ pull−up resistor) | $V_{IN-}/V_{RST}$ = 0 V | $I_{IN-L}$, $I_{RST-L}$ | | −100 | | μA |

**Table 5. ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V.) (continued)

For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LOGIC INPUT AND OUTPUT** | | | | | | |
| IN+ Input Current (50 kΩ pull−down resistor) | $V_{IN+}$ = 5 V | $I_{IN+H}$ | | 100 | | μA |
| RDY, $\overline{FLT}$ Pull−up Current (50 kΩ pull−up resistor) | $V_{RDY}/V_{FLT}$ = Low | $I_{RDY-L}$, $I_{FLT-L}$ | | 100 | | μA |
| RDY, $\overline{FLT}$ Low Level Output Voltage | $I_{RDY}/I_{FLT}$ = 5 mA | $V_{RDY-L}$, $V_{FLT-L}$ | | | 0.3 | V |
| Input Pulse Width of IN+, IN− for No Response at Output | | $t_{ON-MIN1}$ | | | 10 | ns |
| Input Pulse Width of IN+, IN− for Guaranteed Response at Output | | $t_{ON-MIN2}$ | 30 | | | ns |
| Pulse Width of $\overline{RST}$ for Resetting $\overline{FLT}$ | | $t_{RST-MIN}$ | 800 | | | ns |
| **DRIVER OUTPUT** | | | | | | |
| Output Low State ($V_{OUT}$ − $V_{EE2}$) | $I_{SINK}$ = 200 mA | $V_{OUTL1}$ | | 0.1 | 0.2 | V |
| | $I_{SINK}$ = 1.0 A, $T_A$ = 25°C | $V_{OUTL3}$ | | 0.5 | 0.8 | |
| Output High State ($V_{DD2}$ − $V_{OUT}$) | $I_{SRC}$ = 200 mA | $V_{OUTH1}$ | | 0.3 | 0.5 | V |
| | $I_{SRC}$ = 1.0 A, $T_A$ = 25°C | $V_{OUTH3}$ | | 0.8 | 1 | |
| Peak Driver Current, Sink (Note 7) | $V_{OUT}$ = 7.9 V | $I_{PK-SNK1}$ | | 7.1 | | A |
| Peak Driver Current, Source (Note 7) | $V_{OUT}$ = −5 V | $I_{PK-SRC1}$ | | 7.8 | | A |
| **MILLER CLAMP** | | | | | | |
| Clamp Voltage | $I_{CLAMP}$ = 2.5 A, $T_A$ = 25°C | $V_{CLAMP}$ | | 1.3 | 1.7 | V |
| | $I_{CLAMP}$ = 2.5 A, $T_A$ = −40°C to 125°C | | | | 2.5 | |
| Clamp Activation Threshold | | $V_{CLAMP-THR}$ | 1.5 | 2 | 2.5 | V |
| **IGBT SHORT CIRCUIT CLAMPING** | | | | | | |
| Clamping Voltage ($V_{OUT}$ − $V_{DD2}$) | IN+ = Low, IN− = High, $I_{OUT}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 μs) | $V_{CLAMP-OUT}$ | | 0.9 | 1 | V |
| Clamping Voltage, Clamp ($V_{CLAMP}$ − $V_{DD2}$) | IN+ = High, IN− = Low, $I_{CLAMP-CLAMP}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 μs) | $V_{CLAMP-CLAMP}$ | | 1.4 | 1.5 | V |
| **DESAT PROTECTION** | | | | | | |
| DESAT Threshold Voltage | | $V_{DESAT-THR}$ | 8.5 | 9 | 9.5 | V |
| Blanking Charge Current | $V_{DESAT}$ = 7 V | $I_{DESAT-CHG}$ | 0.45 | 0.5 | 0.55 | mA |
| Blanking Discharge Current | | $I_{DESAT-DIS}$ | | 50 | | mA |
| **DYNAMIC CHARACTERISTIC** | | | | | | |
| IN+, IN− to Output High Propagation Delay | $C_{LOAD}$ = 10 nF $V_{IH}$ to 10% of output change for PW > 150 ns. OUT and CLAMP pins are connected together | $t_{PD-ON}$ | 40 | 60 | 90 | ns |
| IN+, IN− to Output Low Propagation Delay | $C_{LOAD}$ = 10 nF $V_{IL}$ to 90% of output change for PW > 150 ns. OUT and CLAMP pins are connected together | $t_{PD-OFF}$ | 40 | 66 | 90 | ns |

**Table 5. ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V.) (continued)

For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTIC** | | | | | | |
| Propagation Delay Distortion (= $t_{PD-ON}$ − $t_{PD-OFF}$) | $T_A$ = 25°C, PW >150 ns | $t_{DISTORT}$ | −15 | −6 | 15 | ns |
| | $T_A$ = −40°C to 125°C, PW > 150 ns | | −25 | | 25 | |
| Prop Delay Distortion between Parts | PW > 150 ns | $t_{DISTORT\_TOT}$ | −30 | 0 | 30 | ns |
| Rise Time (see Figure 3) | $C_{LOAD}$ = 1 nF, 10% to 90% of Output Change | $t_{RISE}$ | | 14 | | ns |
| Fall Time (see Figure 3) | $C_{LOAD}$ = 1 nF, 90% to 10% of Output Change | $t_{FALL}$ | | 19 | | ns |
| DESAT Leading Edge Blanking Time (See Figure 5) | | $t_{LEB}$ | | 450 | | ns |
| DESAT Threshold Filtering Time (see Figure 5) | | $t_{FILTER}$ | | 370 | | ns |
| Soft Turn Off Time (see Figure 5) | $C_{LOAD}$ = 10 nF, $R_G$ = 10 Ω. $V_{EE2}$ = 0 V | $t_{STO}$ | | 550 | | ns |
| | $C_{LOAD}$ = 10 nF, $R_G$ = 10 Ω | | | 750 | | |
| Delay after $t_{FILTER}$ to $\overline{FLT}$ | | $t_{FLT}$ | | 450 | 1000 | ns |
| Input Mute Time after $t_{FILTER}$ | | $t_{MUTE}$ | | 5 | | μs |
| $\overline{RST}$ Rise to $\overline{FLT}$ Rise Delay | | $t_{RST}$ | | 23 | 100 | ns |
| RDY High to Output High Delays (see Figure 4) | | $t_{RDY1O}$ | | 55 | 100 | ns |
| | | $t_{RDY2O}$ | | | | |
| $V_{UVLO2-OUT-OFF}$ to RDY Low Delays (see Figure 4) | | $t_{RDY1F}$ | 6 | 8 | 15 | μs |
| | | $t_{RDY2F}$ | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Values based on design and/or characterization.
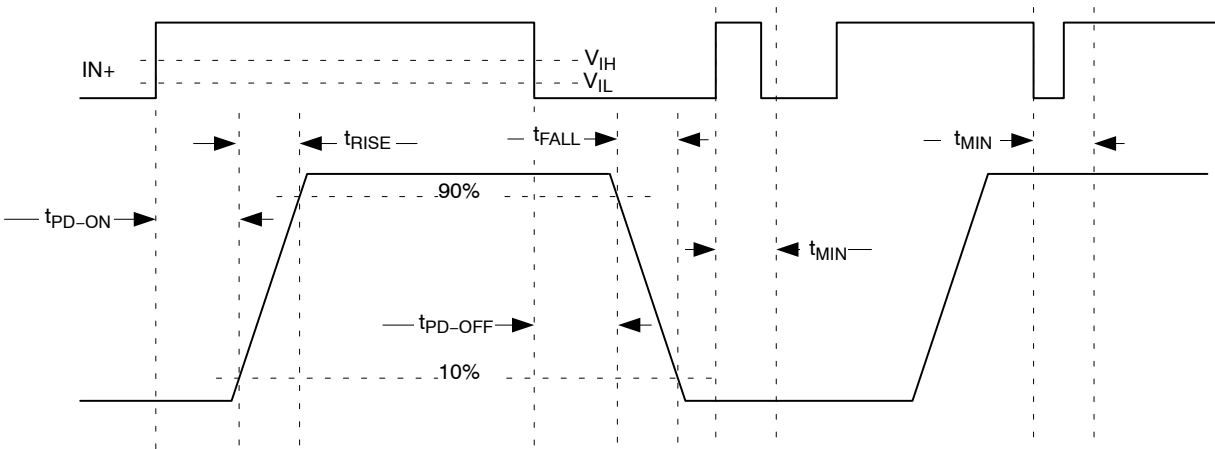
Figure 3. Simplified Block Diagram
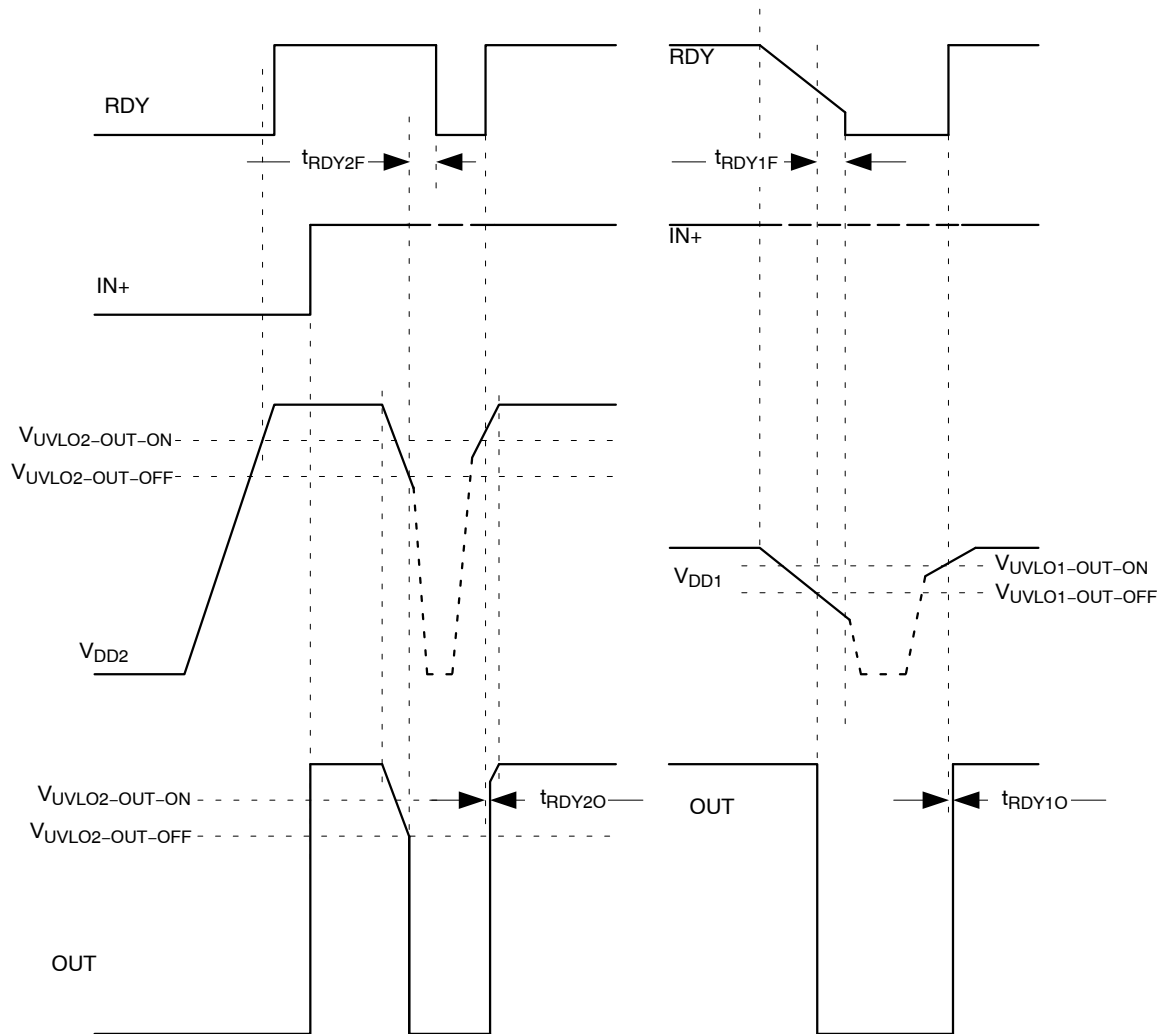


Figure 4. Simplified Block Diagram
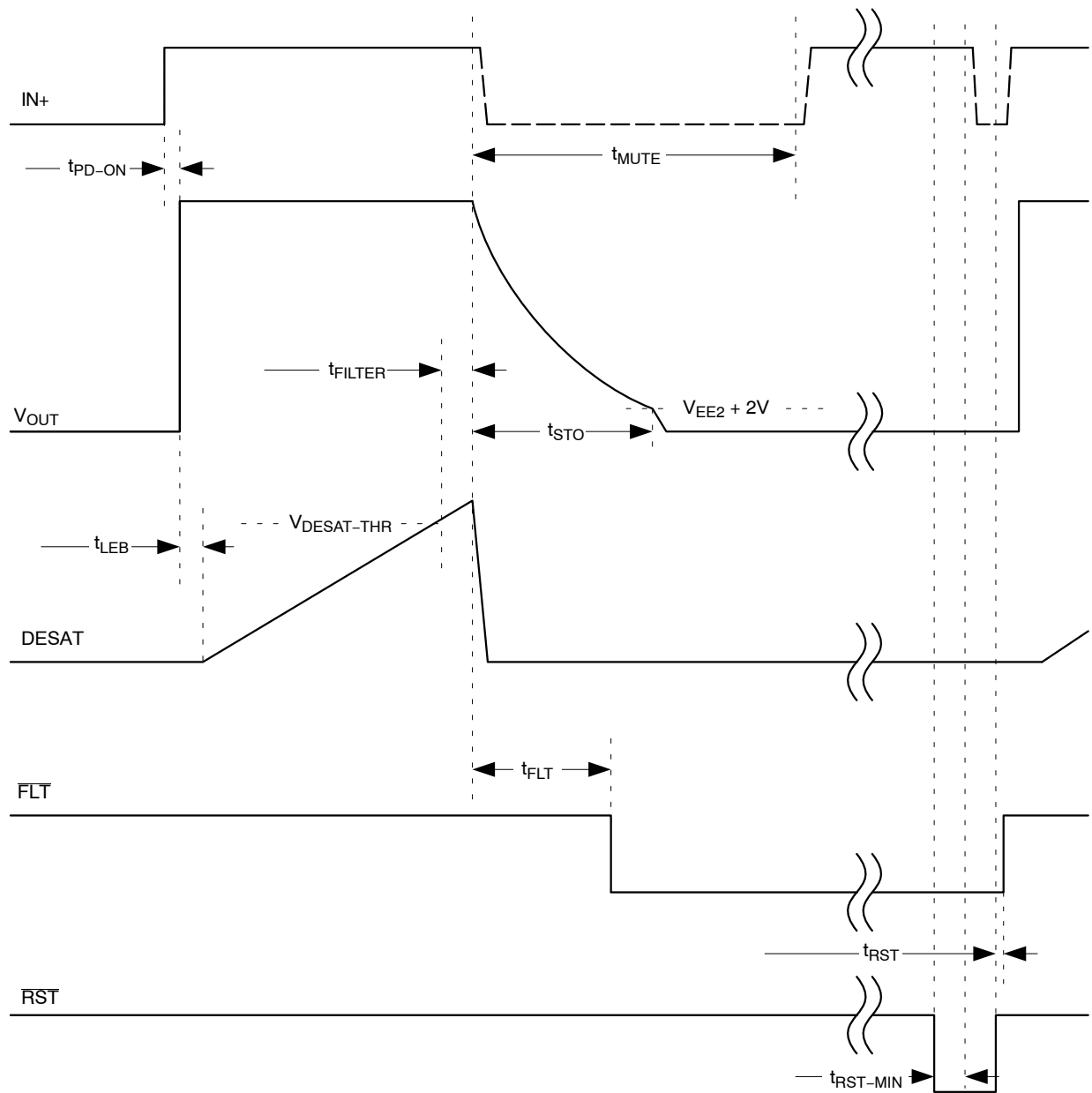
**Figure 5. UVLO Waveform**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCD57001FDWR2G | SOIC−16 Wide Body (Pb−Free) | 1,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
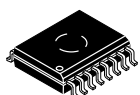
**SOIC−16 WB**
CASE 751G
ISSUE E

DATE 08 OCT 2021

**SCALE 1:1**

1

**TOP VIEW**

PIN 1 INDICATOR

16X B

16

9

1

8

D

H

E

e

**SIDE VIEW**

SEATING PLANE

T

A1

A

**END VIEW**

M

h × 45°

DETAIL A

**DETAIL A
2X SCALE**

16X

L

C
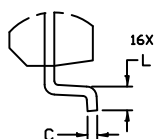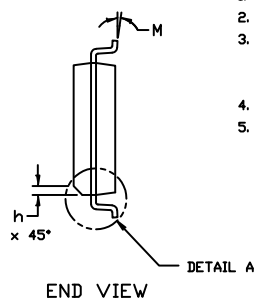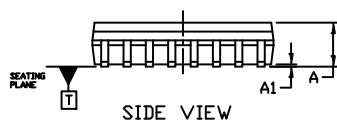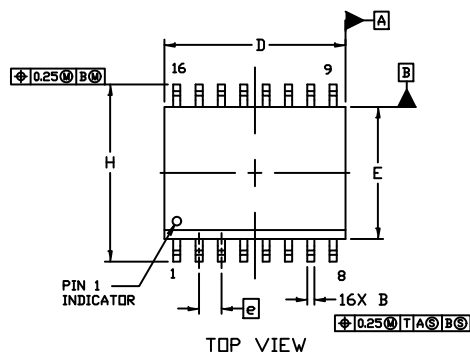
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

| DIM | MILLIMETERS | |
|-----|------|------|
| | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

**RECOMMENDED
MOUNTING FOOTPRINT**

16X 0.58

11.00

16X 1.62

1

1.27 PITCH

**GENERIC
MARKING DIAGRAM\***

16

XXXXXXXXXXX
XXXXXXXXXXX
AWLYYWWG

1
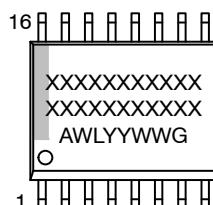
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "∎", may or may not be present. Some products may not follow the Generic Marking.
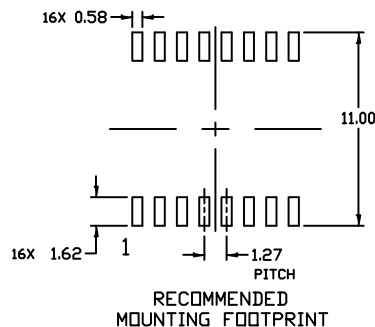
| DOCUMENT NUMBER: | 98ASB42567B | | |
|---|---|---|---|
| DESCRIPTION: | SOIC−16 WB | | PAGE 1 OF 1 |

## PUBLICATION ORDERING INFORMATION

◊

# Mouser Electronics

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