28 V / 5 A Rated OVP with Low On-resistance and Integrated TVS

FPF3381

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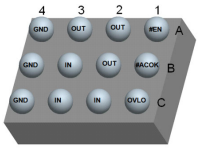


WLCSP−12
CASE 567WP

Description

FPF3381UCX is an OVP with integrated ultra−low on−resistance single channel switch. The device contains an N−MOSFET that can operate over an input voltage range of 2.8 V to 23 V and can support a maximum continuous current of 5 A.

When the input voltage exceeds the over−voltage threshold, the internal FET is turned off immediately to prevent damage to the protected downstream components.

The device has integrated ±110 V surge protection TVS base on IEC61000−4−5 standards.

FPF3381 is available in a small 12−bumps WLCSP package and operate over the free−air temperature range of −40°C to +85°C.

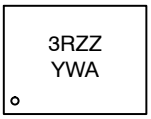
Features

- Over−voltage Protection Up to +28 V
- Integrated TVS: ±110 V for IEC61000−4−5
- Internal Low RDS(on) NMOS Transistors: Typical 15 mΩ
- Programmable Over−voltage Lockout (OVLO)
  - Externally Adjustable via OVLO Pin
- Active−low Enable Pin (OVLO) for Device
- Super−fast OVLO Response Time: Typical 40 ns
- Over Temperature Protection (Thermal Shutdown)
- Robust ESD Performance
  - ±4 kV Human Body Model (HBM)
  - ±2 kV Charged Device Model (CDM)
- System Level ESD (IEC61000−4−2)
  - ±10 kV Contact Discharge
  - ±15 kV Air Gap Discharge

Typical Applications

- Mobile Phones
- PDAs
- GPS

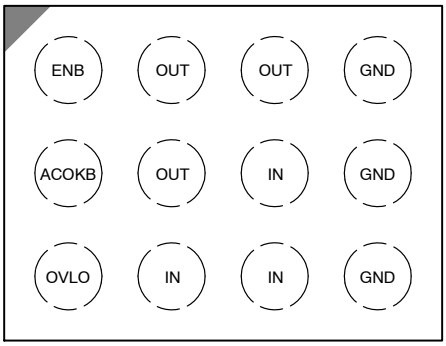
MARKING DIAGRAM



3R	= Specific Device Code
ZZ	= Assembly Lot Code
Y	= Year
W	= Work Week
A	= Assembly Location

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

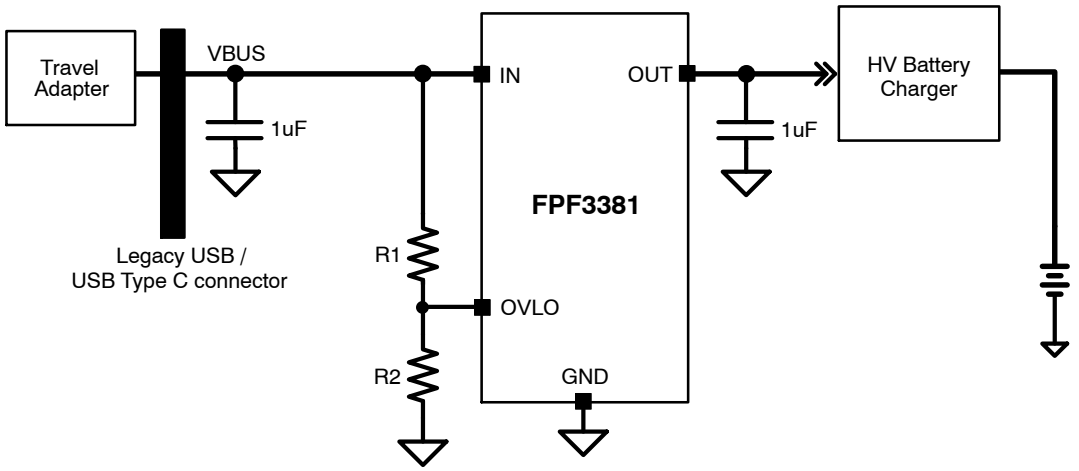


Figure 1. Application Schematic – Adjustable Option

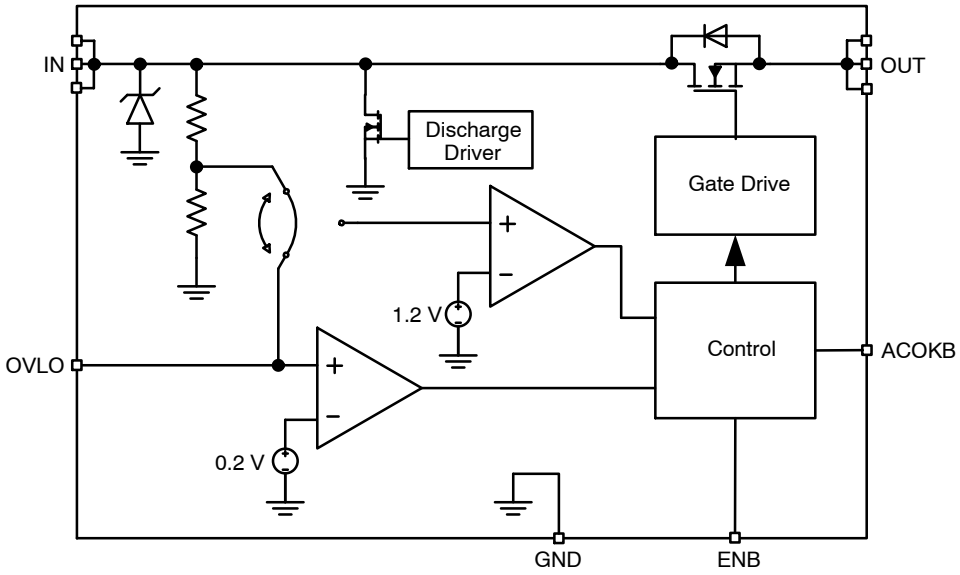


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin #	Name	Description
B3, C2, C3	IN	Power Input: Switch Input and Device Supply
A2, A3, B2	OUT	Power Output: Switch Output to Load
A1	ENB	Enable Input: Active Low. 0: Switch enabled. 1: Switch disabled. 1 MΩ Pull−down resistor integrated.
B1	ACOKB	Power Good Acknowledge Output: Open−drain output to indicate Power Good condition
C1	OVLO	OVLO Input: Over Voltage Lockout Adjustment Input
A4, B4, C4	GND	Ground

ORDERING INFORMATION

Device	Marking	Package	Shipping†
FPF3381UCX	3R	WLCSP−12L	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{in}	−0.3 to +28	V
Output Voltage Range	V_{out}	−0.3 to (V_{in} + 0.3)	V
Adjustable Input Range	V_{OVLO}	−0.3 to +24	V
Internal FET Continuous Current	I_{OUT}	0 to 6.25	A
Internal FET Peak Current (pulse width no longer than 100 μs)	I_{PEAK}	7	A
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	4	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	2	
IEC 61000−4−2 SYSTEM Level ESD	Contact	10	
	Air Gap	15	
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 2. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP−12 (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	84.1	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. Values based on 2S2P JEDEC std. PCB.

Table 3. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage on VIN	V_{in}	2.8	25	V
I/O pins	V_{OVLO}	0	5.5	V
Output Current (Note 6)	I_{out}	0	5	A
IN Capacitor	C_{in}	0.1		μF
OUT Capacitor	C_{out}	0.1		μF
Ambient Temperature	T_A	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Life time, under maximum current, > 5 years base on Temperature < 85°C and no longer than 12 hours per day.

Table 4. ELECTRICAL CHARACTERISTICS V_{IN} = 2.8 to 23 V, C_{IN} = 0.1 μF, C_{OUT} = 0.1 μF, T_A = −40 to 85°C; For typical values V_{IN} = 5.0 V, $I_{IN} \leq$ 3 A, C_{IN} = 0.1 μF, T_A = 25°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LEAKAGE AND QUIESCENT CURRENTS						
Input Quiescent Current on IN	V_{IN} = 5 V, V_{OVLO} = 0.6 V, V_{ENB} = 0 V	I_Q		90		μA
	V_{IN} = 23 V, V_{OVLO} = 0.6 V, V_{ENB} = 0 V			150		
Supply Current during Over Voltage	V_{IN} = 23 V, V_{OVLO} = 1.8 V, V_{OUT} = V_{ENB} = 0 V	I_{IN_Q}		150		μA
OVLO Input Leakage Current	V_{OVLO} = V_{OVLO_TH}	I_{OVLO}	−100		100	nA
OVER VOLTAGE AND UNDER VOLTAGE LOCKOUT, I/O						
Input Clamping Voltage	I_{IN} = 10 mA	V_{IN_CLAMP}		32		V
	I_{IN} = 30A (Note 7)			37		
Under−Voltage Rising Trip Level for VIN	V_{IN} rising, T_A = −40 to 85°C	$V_{IN\_UV\_R}$	2.4	2.55	2.7	V
Under−Voltage Falling Trip Level for VIN	V_{IN} falling, T_A = −40 to 85°C	$V_{IN\_UV\_F}$		2.45		V
Default Over−Voltage Trip Level	V_{IN} rising, V_{OVLO} = GND	V_{IN_OVLO}	13.5	14.0	14.5	V
OVLO Set Threshold	V_{OVLO} = 1.1 V to 1.3 V, the voltage of OVLO pin to trigger Over Voltage condition	V_{OVLO_TH}	1.165	1.20	1.235	V
OVLO Threshold Hysteresis		V_{HYS_OVLO}		3		%
OVLO Input Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low	 High Low	 V_{IH_OVLO} V_{IL_OVLO}	 0.2		 0.1	V
ENB Input Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low	 High Low	 V_{IH_ENB} V_{IL_ENB}	 0.9		 0.3	V
Output Low Voltage of ACOKB	I_{ACOKB} = 1 mA, Logic Low Asserted	V_{OL}			0.4	V
ACOKB Leakage Current	$V_{I/O}$ = 3.3 V, ACOKB De−asserted, V_{ENB} = 0 V	I_{ACOKB}	−0.5		0.5	uA
RESISTANCE						
On−resistance of Power FET	V_{IN} = 5 V, I_{OUT} = 200 mA, T_A = 25°C	r_{ON}		15	20	mΩ
	V_{IN} = 5 V to 23 V, I_{OUT} = 0.1 A to 5 A (Note 10)				25	
Pull−down Resistor on ENB				1		MΩ
Discharge on IN	V_{IN} = 5 V, V_{ENB} = 1.8 V			800		Ω
TIMING						
De−bounce Time of Power FET Turned On	Time from 2.5 V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 0.1 × V_{IN}	t_{SW_DEB}		15		ms
Soft−Start Time of Power FET Turned On	Time from 2.5 V < V_{IN} < V_{IN_OVLO} to V_{AOCKB} = 0.2 × $V_{I/O}$ with $V_{I/O}$ = 1.8 V and R_{PU} = 10 kΩ	t_{SS}		30		ms
Switch Turn−On Rising Time (Note 10)	V_{IN} = 5 V, R_L = 100 Ω, C_L = 22 μF, V_{OUT} from 0.1 × V_{IN} to 0.9 × V_{IN}	t_R		2		ms
Switch Turn−Off Time (Note 10)	R_L = 10 Ω, C_L = 0 μF, time from V_{IN} > V_{OVLO} to V_{OUT} = 0.9 × V_{IN} (Note 11)	t_{OVP}		40		ns
	time from V_{ENB} > V_{IH_ENB} to V_{OUT} = 0.9 × V_{IN}	t_{OFF}			2	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 10)		T_{SD}	–	130	–	°C
Thermal Shutdown Hysteresis (Note 10)		T_{SH}	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. The spec is only for surge event. Guaranteed by design and characterization.
8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Refer to the APPLICATION INFORMATION section.
10. Values based on design and/or characterization.
11. Depends on the capacitance on OVLO pin.

FUNCTION DESCRIPTION

General

FPF3381 is an OVP power switch to protect next stage system which is optimized to lower voltage working condition. The device includes ultra−low on−resistance power FET (15 mΩ) and internal TVS for surge event protection base on IEC61000−4−5. The super−fast OVP response time is only 40 ns for default OVP condition.

Power MOSFET

The FPF3381 integrates an N−type MOSFET with 15 mΩ resistance. The power FET can work under 2.8 V ~ 25 V and up to 5 A DC current capability.

Power Supply

The FPF3381 is supplied by IN.

IN will be firstly supplied by OUT when the device is working under USB On−The−Go (OTG) condition.

Enable Control

FPF3381 has an active low enable pin ENB. When ENB pin is connected to a high level, the internal FET will be turned off. When ENB pin is connected to low level, the FET will be turned on as long as V_{IN} is not higher than Over−Voltage threshold.

Under Voltage Lockout

FPF3381 power switch will be turned off when the voltage on IN is lower than the UVLO threshold $V_{IN\_UV\_F}$.

Whenever VIN voltage ramps up to higher than $V_{IN\_UV\_R}$, the power FET will be turned on automatically after t_{DEB} de−bounce time if there is no OV or OT condition.

Over Voltage Lockout

The power FET will be turned off whenever IN voltage higher than V_{IN_OVLO}. The value of V_{IN_OVLO} can be set by external resistor ladder or just be default value V_{IN_OVLO}.

When V_{OVLO} is smaller than V_{IL_OVLO}, V_{OVLO} will be decided by default value. When V_{OVLO} is larger than V_{IH_OVLO}, the power switch will be turned off once $V_{OVLO} > V_{OVLO\_TH}$. The external resistor ladder can be decided according to the following equation:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times (1 + R1/R2) \quad \text{(eq. 1)}$$

where R1 and R2 are the resistors in Figure 1.

Power OK indicator

FPF3381 has an Open−Drain output ACOKB. By implement connection to external supply through a resistor, ACOKB can indicate the status on IN (or VBUS). When VIN is between $V_{IN\_UV\_R}$ and V_{IN_OVLO} more than 30 ms, ACOKB will be pulled down to ground. If the input voltage is out of this range, ACOKB will present as a floating node and the voltage will be pulled high by external power supply.

Thermal Shutdown

When the device is in the switch mode, to protect the device from over temperature, the power switch will be turned off when the junction temperature exceeds T_{SD}. The switch will be turned on again when temperature drop below $T_{SD} - T_{SH}$.

APPLICATIONS INFORMATION

Input Decoupling (C_{in})

A ceramic or tantalum at least 0.1 μF capacitor is recommended and should be connected close to the FPF338x package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{out})

The FPF3381 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements.

Thermal Considerations

As power in the FPF3381 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the FPF3381 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the FPF3381 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 2)}$$

Since T_J is not recommended to exceed 125°C, then the FPF3381 soldered on 645 mm^2, 1 oz copper area, and the ambient temperature (T_A) is 25°C. The power dissipated by the FPF3381 can be calculated from the following equations:

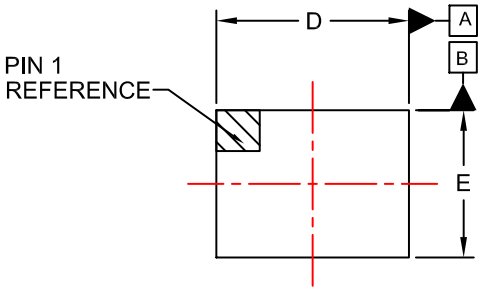
$$P_D \approx V_{in} \cdot \left(I_Q @ I_{out}\right) + {I_{out}}^2 \cdot r_{ON} \quad \text{(eq. 3)}$$

Hints

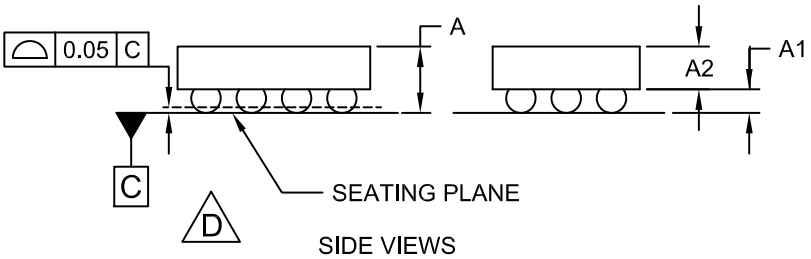
V_{in} and V_{out} printed circuit board traces should be as wide as possible. Place external components, especially the input capacitor and TVS, as close as possible to the FPF3381, and make traces as short as possible.

WLCSP12 1.828x1.288x0.574
CASE 567WP
ISSUE O

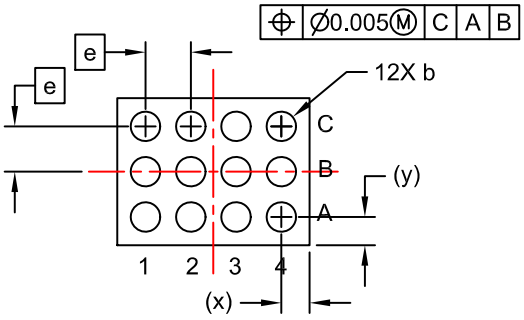
DATE 25 JUN 2018



TOP VIEW



SIDE VIEWS

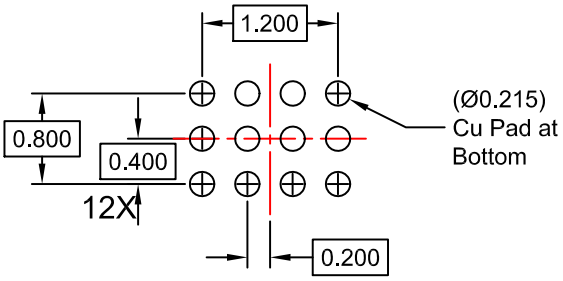


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.536	0.574	0.612
A1	0.176	0.196	0.216
A2	0.360	0.378	0.396
b	0.240	0.260	0.280
D	1.798	1.828	1.858
E	1.258	1.288	1.318
e	0.40 BSC		
x	0.299	0.314	0.329
y	0.229	0.244	0.259



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