PB_MC33774A

Product brief for 18-cell battery-cell controller IC

Rev. 3 — 25 January 2024 Product brief

1 General description

The MC33774A is a lithium-ion battery-cell controller IC designed for automotive applications, such as electric vehicles (EV) and hybrid electric vehicles (HEV). It can be used in industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The MC33774AxP1 (MC33774ATP1 for TPL isolated communication/MC33774ASP1 for SPI communication) is the premium version of the MC33774AxA1 (MC33774ATA1 for TPL isolated communication/MC33774ASA1 for SPI communication) for higher battery voltage and improved accuracy.

These devices support ISO 26262 ASIL D compliant high-precision cell voltage and temperature measurements, along with various cell-voltage balancing strategies. Aside from a SPI interface to enable direct communication with the host MCU, they alternatively provide a daisy-chain communication interface (TPL), which supports capacitive and inductive isolation between nodes.

2 Features and benefits

- AEC-Q100 grade 1 qualified: -40 °C to 125 °C ambient temperature range
- ISO 26262 ASIL D support for cell voltage and cell temperature measurements from the host microcontroller unit (MCU) to the cell
- Cell voltage measurement
  - 4 to 18 cells per device
  - Supports bus bars voltage measurement with -3 V to +5 V input voltage
  - 16-bit resolution and up to ±0.8 mV typical measurement accuracy with ultra low long-term drift
  - Integrated configurable digital filter
- External temperature and auxiliary voltage measurements
  - One analog input for absolute measurement, 5 V input range
  - Eight analog inputs configurable as absolute or ratiometric, 5 V input range
  - 16-bit resolution and ±5 mV typical measurement accuracy
  - Integrated configurable digital filter
- Internal measurement
  - Two redundant internal temperature sensors
  - Supply voltages
  - External transistor current
- Cell voltage balancing
  - 18 internal balancing field effect transistors (FET), up to 360 mA peak with 0.5 Ω R_{DSon} per channel (typ.)
  - Support for simultaneous passive balancing of all channels with automatic odd/even sequence
  - Global balancing timeout timer
  - Timer controlled balancing with individual timers with 10 s resolution and up to 45 h duration
  - Voltage controlled balancing with global and individual undervoltage thresholds
  - Temperature controlled balancing; if balancing resistors or the IC are in overtemperature, balancing is interrupted
  - Configurable pulse width modulation (PWM) duty cycle balancing
  - Automatic pause of balancing during measurement with configurable filter settling time
  - Configurable delay of the start of balancing after transition to sleep
  - Automatic discharge of the battery pack (emergency discharge)
  - Constant current cell balancing to compensate the balancing current variation because of cell voltage variation
- I^2C-bus master interface to control external devices, for example, EEPROMs and security ICs
- Configurable alarm output
- Cyclic wake-up to monitor the pack and the balancing function during sleep
- Capability to wake up the host MCU via daisy chain in case of a fault event
- Host interface supporting SPI or isolated daisy chain communication (TPL3)
  - 2 Mbit/s data rate for TPL interface
  - 4 Mbit/s data rate for SPI interface
- TPL3 daisy chain communication supports
  - Two-wire daisy chain with capacitive or inductive isolation
  - Protocol supporting up to six daisy chains and 62 nodes per chain
- Unique device ID with dynamic addressing
- Operation modes
  - Active mode FP (12 mA typ.)
  - Sleep mode LP (60 µA typ.)
  - Deep Sleep mode ULP (15 µA typ.)

3 Applications

Automotive:

- (Plug-in) hybrid electric vehicle battery management system
- Electric vehicle battery management system

Industrial:

- Stationary ESS
- UPS systems

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MC33774A	LQFP64	Plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 x 10 x 1.4 mm body	SOT1510-2

4.1 Ordering options

Table 2. Part numbers

Type number	Description
MC33774ATA1AE	Advanced version - TPL interface
MC33774ASA1AE	Advanced version - SPI interface
MC33774ATP1AE	Premium version - TPL interface
MC33774ASP1AE	Premium version - SPI interface

5 Block diagram

Figure 1 shows the general architecture of the MC33774A.

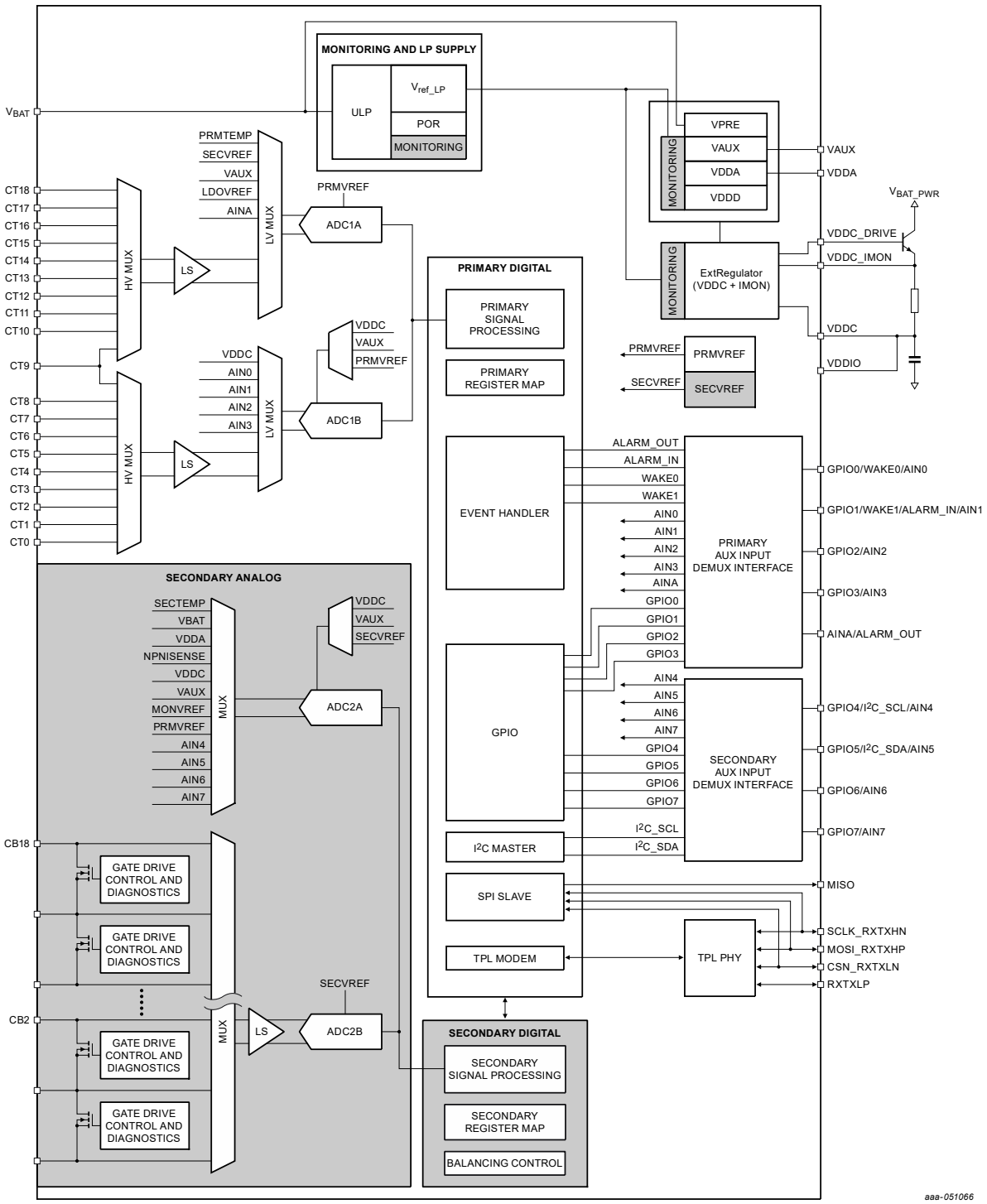


Figure 1. Simplified internal block diagram

6 Pinning information

6.1 Pinout diagram

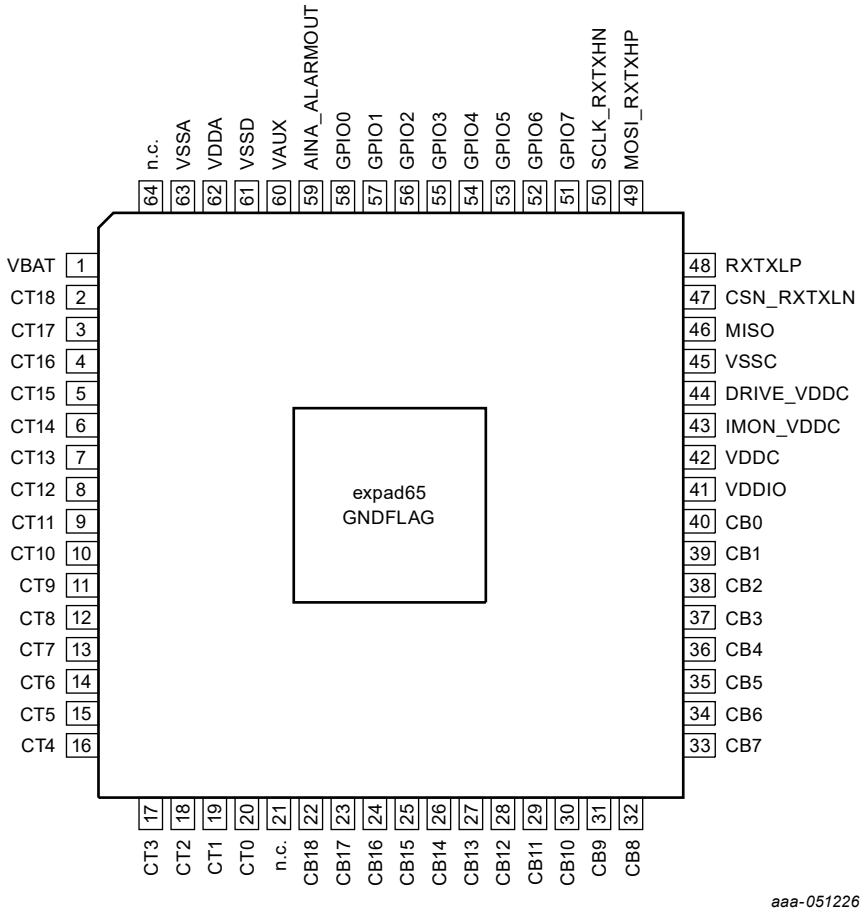


Figure 2. Pinout

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBAT	1	Supply input of the product
CT18	2	Cell terminal 18 input
CT17	3	Cell terminal 17 input
CT16	4	Cell terminal 16 input
CT15	5	Cell terminal 15 input
CT14	6	Cell terminal 14 input
CT13	7	Cell terminal 13 input
CT12	8	Cell terminal 12 input
CT11	9	Cell terminal 11 input
CT10	10	Cell terminal 10 input

Table 3. Pin description*...continued*

Symbol	Pin	Description
CT9	11	Cell terminal 9 input
CT8	12	Cell terminal 8 input
CT7	13	Cell terminal 7 input
CT6	14	Cell terminal 6 input
CT5	15	Cell terminal 5 input
CT4	16	Cell terminal 4 input
CT3	17	Cell terminal 3 input
CT2	18	Cell terminal 2 input
CT1	19	Cell terminal 1 input
CT0	20	Cell terminal 0 input
n.c.	21	Not connected
CB18	22	1. Secondary cell terminal 18 input 2. High input for cell 17 balancing
CB17	23	1. Secondary cell terminal 17 input 2. Low input for cell 17 balancing 3. High input for cell 16 balancing
CB16	24	1. Secondary cell terminal 16 input 2. Low input for cell 16 balancing 3. High input for cell 15 balancing
CB15	25	1. Secondary cell terminal 15 input 2. Low input for cell 15 balancing 3. High input for cell 14 balancing
CB14	26	1. Secondary cell terminal 14 input 2. Low input for cell 14 balancing 3. High input for cell 13 balancing
CB13	27	1. Secondary cell terminal 13 input 2. Low input for cell 13 balancing 3. High input for cell 12 balancing
CB12	28	1. Secondary cell terminal 12 input 2. Low input for cell 12 balancing 3. High input for cell 11 balancing
CB11	29	1. Secondary cell terminal 11 input 2. Low input for cell 11 balancing 3. High input for cell 10 balancing
CB10	30	1. Secondary cell terminal 10 input 2. Low input for cell 10 balancing 3. High input for cell 9 balancing
CB9	31	1. Secondary cell terminal 9 input 2. Low input for cell 9 balancing 3. High input for cell 8 balancing
CB8	32	1. Secondary cell terminal 8 input 2. Low input for cell 8 balancing 3. High input for cell 7 balancing
CB7	33	1. Secondary cell terminal 7 input 2. Low input for cell 7 balancing 3. High input for cell 6 balancing

Table 3. Pin description*...continued*

Symbol	Pin	Description
CB6	34	1. Secondary cell terminal 6 input 2. Low input for cell 6 balancing 3. High input for cell 5 balancing
CB5	35	1. Secondary cell terminal 5 input 2. Low input for cell 5 balancing 3. High input for cell 4 balancing
CB4	36	1. Secondary cell terminal 4 input 2. Low input for cell 4 balancing 3. High input for cell 3 balancing
CB3	37	1. Secondary cell terminal 3 input 2. Low input for cell 3 balancing 3. High input for cell 2 balancing
CB2	38	1. Secondary cell terminal 2 input 2. Low input for cell 2 balancing 3. High input for cell 1 balancing
CB1	39	1. Secondary cell terminal 1 input 2. Low input for cell 1 balancing 3. High input for cell 0 balancing
CB0	40	1. Secondary cell terminal 0 input 2. Low input for cell 0 balancing
VDDIO	41	External VDDIO supply input.
VDDC	42	External VDDC supply input.
IMON_VDDC	43	External NPN monitoring input.
DRIVE_VDDC	44	External NPN base output.
VSSC	45	VDDIO and VDDC ground reference.
MISO	46	SPI slave data output to master.
CSN_RXTXLN	47	1. SPI chip select input from master 2. TPLRX negative input from lower node 3. TPLTX negative output to lower node
RXTXLP	48	1. TPLRX positive input from lower node 2. TPLTX positive output to lower node
MOSI_RXTXHP	49	1. SPI slave data input from master 2. TPLRX positive input from upper node 3. TPLTX positive output to upper node
SCLK_RXTXHN	50	1. SPI clock input from master 2. TPLRX negative input from upper node 3. TPLTX negative output to upper node
GPIO7	51	1. Analog input AIN7 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN7 for absolute measurement 3. General-purpose input 7 4. General-purpose output 7
GPIO6	52	1. Analog input AIN6 for ratiometric measurement to VAUX / VDDC 2. Analog input AIN6 for absolute measurement 3. General-purpose input 6 4. General-purpose output 6

Table 3. Pin description*...continued*

Symbol	Pin	Description
GPIO5	53	1. Analog input AIN5 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN5 for absolute measurement 3. General-purpose input 5 4. General-purpose output 5 5. I2CSDA
GPIO4	54	1. Analog input AIN4 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN4 for absolute measurement 3. General-purpose input 4 4. General-purpose output 4 5. I2CSCL
GPIO3	55	1. Analog input AIN3 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN3 for absolute measurement 3. General-purpose input 3 4. General-purpose output 3
GPIO2	56	1. Analog input AIN2 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN2 for absolute measurement 3. General-purpose input 2 4. General-purpose output 2
GPIO1	57	1. Analog input AIN1 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN1 for absolute measurement 3. General-purpose input 1 4. General-purpose output 1 5. Wake-up input 1 6. Alarm input
GPIO0	58	1. Analog input AIN0 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN0 for absolute measurement 3. General-purpose input 0 4. General-purpose output 0 5. Wake-up input 0
AINA_ALARMOUT	59	1. Analog input AINA for absolute measurement 2. Alarm output
VAUX	60	Supply output for external sensors.
VSSD	61	Digital ground.
VDDA	62	Internal analog supply. Should be connected to a 100 nF capacitor. Should not be used for application.
VSSA	63	Analog ground.
n.c.	64	Not connected.
GNDFLAG	Expad 65	Grounded exposed pad.

7 Limiting values

7.1 MC33774AxA1 limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	VBAT voltage		-0.3	-	84	V

7.2 MC33774AxP1 limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	VBAT voltage		-0.3	-	94	V

7.3 MC33774A common limiting values

Table 6. Common limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{dif(CT)}$	Cell terminal input differential voltage		-5	-	10	V
$I_{i(CTn)}$	cell terminal input current	open load detection disabled	-500	-	500	nA
$V_{i(dif)bal}$	balancing input differential voltage		-4.5	-	12.5	V
$I_{i(bal)}$	input current on balancing pins		-	-	330	mA
V_{DDC}	VDDC voltage		-0.3	-	5.5	V
V_{DDIO}	VDDIO voltage		-0.3	-	5.5	V
V_{AUX}	VAUX voltage		-0.3	-	4	V
V_{GPIOx}	GPIOx voltage		-0.3	-	VDDC + 0.5	V
V_{AINA}	AINA and $ALARM_{OUT}$ voltage		-0.3	-	VDDC + 0.5	V
$V_{bus(TPL)}$	voltage on TPL communication bus pins	Relative to VSSC	-27	-	40	V
Thermal maximum ratings						
T_j	junction temperature		-40	-	165	°C
T_{stg}	storage temperature		-55	-	150	°C

8 Electrical characteristics

8.1 MC33774AxA1 electrical characteristics

Table 7. Electrical characteristics

Vbat = 9 V to 81 V; Ta = -40 °C to 125 °C; Tj = -40 °C to 150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT						
V_{BAT}	VBAT operating range		9	-	81	V
$V_{BAT(th)ov}$	VBAT overvoltage threshold		81	-	83	V
Cell voltage measurement accuracy for primary measurement - begin of life						
$V_{err(meas)(LPF1)}$	Measurement error voltage (LFP1)	VC_x = 0 V to 3.7 V; T_j = −40 °C to 105 °C	-1	-	1	mV
$V_{err(meas)(NMC1)}$	Measurement error voltage (NMC1)	VC_x = 0 V to 4.5 V; T_j = −40 °C to 105 °C	-1.3	-	1.3	mV
Cell voltage measurement accuracy for primary measurement - end of life						
$V_{err(meas)(LFP3)}$	Measurement error voltage (LFP3)	VC_x = 0 V to 3.7 V; T_j = −40 °C to 125 °C	−1.5	-	1.5	mV
$V_{err(meas)(NMC3)}$	Measurement error voltage (NMC3)	VC_x = 0 V to 4.5 V; T_j = −40 °C to 125 °C	−2.0	-	2.0	mV
TPL current						
$I_{VDDC(TPL)wait}$	TPL current on VDDC, device in waiting state	2 RX ON,No TX	-	-	1.4	mA
$I_{VDDC(TPL)forward}$	TPL current on VDDC, device in forward state	1 RX ON,1 TX ON(TX averaged on bit period)	-	-	9.2	mA
$I_{VDDC(TPL)respond}$	TPL current on VDDC, device in responding state	NO RX, 2 TX ON(TX averaged on bit period)	-	-	17	mA

8.2 MC33774AxP1 electrical characteristics

Table 8. Electrical characteristics

Vbat = 9 V to 90 V; Ta = -40 °C to 125 °C; Tj = -40 °C to 150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT						
V_{BAT}	VBAT operating range		9	-	90	V
$V_{BAT(th)ov}$	VBAT overvoltage threshold		90	-	93	V
Cell voltage measurement accuracy for primary measurement - begin of life						
$V_{err(meas)(A)(CTx)}$	Cell voltage measurement error CTx, range A. (LFP)	Vcell = 0 V..3.7 V, Tj = -40 °C.. 115 °C, VBAT = 9 V.. 81 V	-0.8	-	0.8	mV
$V_{err(meas)(B)(CTx)}$	Cell voltage measurement error CTx, range B. (NMC)	Vcell = 0 V..4.5 V, Tj = -40 °C.. 115 °C, VBAT = 9 V.. 81 V	-1	-	1	mV
Cell voltage measurement accuracy for primary measurement - end of life						
$V_{err(meas)(E)(CTx)}$	Cell voltage measurement error CTx, range E. (LFP cells)	Vcell = 0 V..3.7 V, Tj = -40 °C.. 115 °C, VBAT = 9 V.. 81 V	-1.2	-	1.2	mV
$V_{err(meas)(F)(CTx)}$	Cell voltage measurement error CTx, range F. (NMC cells)	Vcell = 0 V..4.5 V, Tj = -40 °C.. 115 °C, VBAT = 9 V.. 81 V	-1.5	-	1.5	mV

Table 8. Electrical characteristics*...continued*

Vbat = 9 V to 90 V; Ta = -40 °C to 125 °C; Tj = -40 °C to 150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TPL current						
$I_{VDDC(TPL)wait}$	TPL current on VDDC, device in waiting state	2 RX ON,No TX	-	-	1.4	mA
$I_{VDDC(TPL)forward}$	TPL current on VDDC, device in forward state	1 RX ON,1 TX ON(TX averaged on bit period)	-	-	11.2	mA
$I_{VDDC(TPL)respond}$	TPL current on VDDC, device in responding state	NO RX, 2 TX ON(TX averaged on bit period)	-	-	21	mA

8.3 MC33774A common electrical characteristics

Table 9. Characteristics

Vbat = 9 V to 81 V (MC33774AxA1) / 90V (MC33774AxP1); Ta = -40 °C to 125 °C; Tj = -40 °C to 150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT						
$V_{BAT(th)uv}$	VBAT undervoltage threshold		7	8	9	V
$V_{BAT(th)lv}$	VBAT low-voltage (LV) threshold	FP and FPC modes and LP mode with cell balancing	10.5	12	13.5	V
$\Delta V_{max1(VBAT-upperCT)}$	Maximum voltage difference 1 between battery supply voltage and pin CT18 or highest CTn	V_{bat} = 35 V to maximum supply voltage	-2.1	-	2.5	V
$\Delta V_{max2(VBAT-upperCT)}$	Maximum voltage difference between battery supply voltage and pin CT18 or highest CTn	V_{bat} = 9 V +1.5 V to 35 V	-1.5	-	2	V
$\Delta V_{bal(VBAT-upperCB)}$	Maximum voltage difference between battery supply voltage and pin CB18 or highest CBn	T_j = -40 °C to 150 °C, V_{bat} = 9 V to 81V, V_{cell} = -5 V to 5 V	-0.4	-	0.4	V
Current consumption						
$I_{BAT(ULP)}$	IBAT current in Deep Sleep mode	Tj= -40 °C...85 °C	-	-	19	µA
$I_{BAT(LP)}$	IBAT current in Sleep mode	Tj= -40 °C...125 °C	-	-	115	µA
$I_{BAT(add)LP}$	Additional IBAT current in Sleep mode in sleep mode due to balancing	sleep mode with balancing enabled	-	-	2.9	mA
$I_{BAT(FP)}$	Full Power mode current consumption measuring all cell voltages and auxiliary inputs.	No external load. No cell balancing.	-	-	14.9	mA
$I_{BAT(FPC)2}$	Cyclic mode current consumption measuring all cell voltages, primary auxiliary inputs, and module voltage.	No secondary measurement. No balancing. No external current consumption. No communication.	-	-	12.3	mA
$I_{BATCB(FPC)}$	IBAT additional current in FP or FPC mode when all CB enable	All cell balancing enabled.	-	-	700	uA
$\Delta I_{BAT(FP)}$	IC to IC operating current imbalance	Ta = -40 °C to 125 °C, Vbat = 45 V, Ta and Vbat are the same for both ICs, Active mode/all ADCs running/No balancing operation/ No communication/No external load	-	-	400	µA

Table 9. Characteristics*...continued*

Vbat = 9 V to 81 V (MC33774AxA1) / 90V (MC33774AxP1); Ta = -40 °C to 125 °C; Tj = -40 °C to 150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VAUX						
V_{AUX}	VAUX output voltage		3.19	3.3	3.41	V
I_{VAUX}	VAUX external current capability		-	-	5	mA
VDDC						
V_{DDC}	VDDC output voltage		4.85	5.0	5.15	V
I_{VDDC}	External VDDC current drive capability	Ta = -40 °C to 125 °C	-	-	15	mA
Internal temperature measurement						
$T_{j(meas)}$	IC temperature measurement range		-45	-	155	°C
$\Delta T_{j(meas)}$	IC temperature measurement error	Range to be measured is -40 °C to 150 °C	-3	-	3	°C
Overtemperature protection						
$T_{sd(th)}$	Shutdown temperature threshold	Of VPRE regulator	160	-	175	°C
Measurement resolution						
$V_{meas(res)VBAT}$	Measured voltage resolution		-	3.128	-	mV/LSB
$V_{meas(res)}$	Measured voltage resolution		-	154	-	µV/LSB
$T_{meas(res)}$	Primary and secondary measured temperature resolution		-	32.4	-	mK/LSB
$V_{meas(res)(supply)}$	Supply voltage measurement resolution (VAUX, VDDC)		-	308	-	uV/LSB
$V_{meas(res)(vdda)}$	Supply voltage measurement resolution (VDDA)		-	154	-	uV/LSB
Measurement acquisition						
$N_{s(PI)}$	Number of periodic integrator samples		16	-	511	
$N_{s(AI)}$	Number of application integrator samples		16	-	65534	
VBAT measurement accuracy						
$V_{I(acc)VBAT}$	Measured voltage minimum accuracy	Tj = -40 °C to 115 °C, VBAT ≥ 17 V at pin VBAT (wo Rvbat)	-50	-	50	mV
$\Delta V_{I(meas)VBAT}$	Measured Voltage Max Relative Error	Tj = -40 °C to 115 °C, VBAT ≥ 17 V at pin VBAT (wo Rvbat)	-	-	0.3	%
Balancing						
I_{bal2}	Balancing current	T_j = -40 °C to 125 °C, R_{bal} = 10 to 450 Ω, no external load current, 50 % duty cycle max	0	-	360	mA
$I_{lim(bal)2}$	Balancing current limit	Tj = -40 °C to 125 °C	360	-	800	mA
$R_{sw(bal)}$	Balancing switch resistance	T_j = -40 °C to 150 °C, V_{bat} = 9 V to 81 V, 4 to 18 cells	-	-	1.1	Ω
Analog inputs						
$V_{meas(aux)(abs)}$	Auxiliary input measured voltage (absolute value)		0	-	5	V
$E_{G(abs)1}$	Absolute gain error 1	T_j = -40 °C to 115 °C	-0.08	-	0.08	%

Table 9. Characteristics*...continued*

Vbat = 9 V to 81 V (MC33774AxA1) / 90V (MC33774AxP1); Ta = -40 °C to 125 °C; Tj = -40 °C to 150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

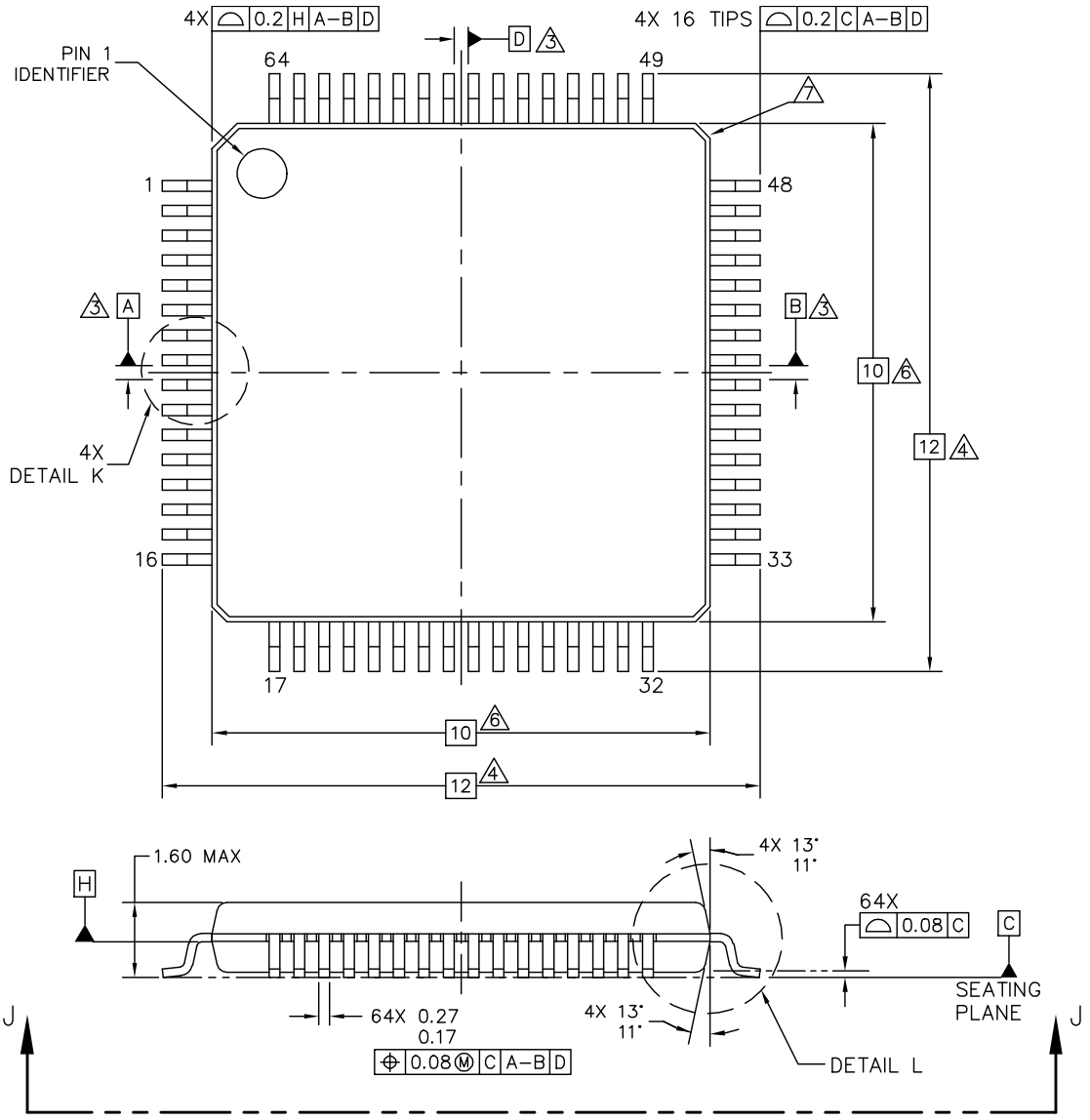
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$E_{G(abs)2}$	Absolute gain error 2	T_j = -40 °C to 150 °C	-0.12	-	0.12	%
$V_{err(offset)(abs)}$	Absolute offset error voltage	T_j = -40 °C to 150 °C	-3	-	3	mV
$E_{T(meas)ratiom1}$	Ratiometric measurement total error 1	T_j = -40 °C to 115 °C	-0.006 - 0.15 % * V_{AINx}	-	0.006 + 0.15 % * V_{AINx}	V
$E_{T(meas)ratiom2}$	Ratiometric measurement total error 2	T_j = -40 °C to 150 °C	-0.006 - 0.25 % * V_{AINx}	-	0.006 + 0.25 % * V_{AINx}	V
$V_{meas(res)(abs)}$	Measured voltage resolution	Absolute measurement (absolute reference voltage)	-	154	-	µV/LSB
$V_{meas(res)(ratiom)}$	Measured voltage resolution	Ratiometric measurement (VAUX or VDDC)	-	3.05176×10^{-3}	-	% / LSB
GPIO						
$V_{OH(GPIO)}$	Output logic high voltage on GPIO pins	I_{GPIO} = 1 mA Including routing and all GPIOs / I^2C driving at the same time.	V_{VDDC} - 0.4V	-	V_{VDDC}	-
$V_{OL(GPIO)}$	Output logic low voltage on GPIO pins	I_{GPIO} = 1 mA Including routing and all GPIOs / I^2C driving at the same time.	-	-	0.4	V
$I_{OH(tot)GPIO}$	Total high-level output current on GPIO pins		-	-	8	mA
$I_{OL(tot)GPIO}$	Total low-level output current on GPIO pins		-	-	20	mA

9 Package information

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 10. Package outline

Package	Suffix	Package outline drawing number
64-pin LQFP-EP	AE	98ASA10763D



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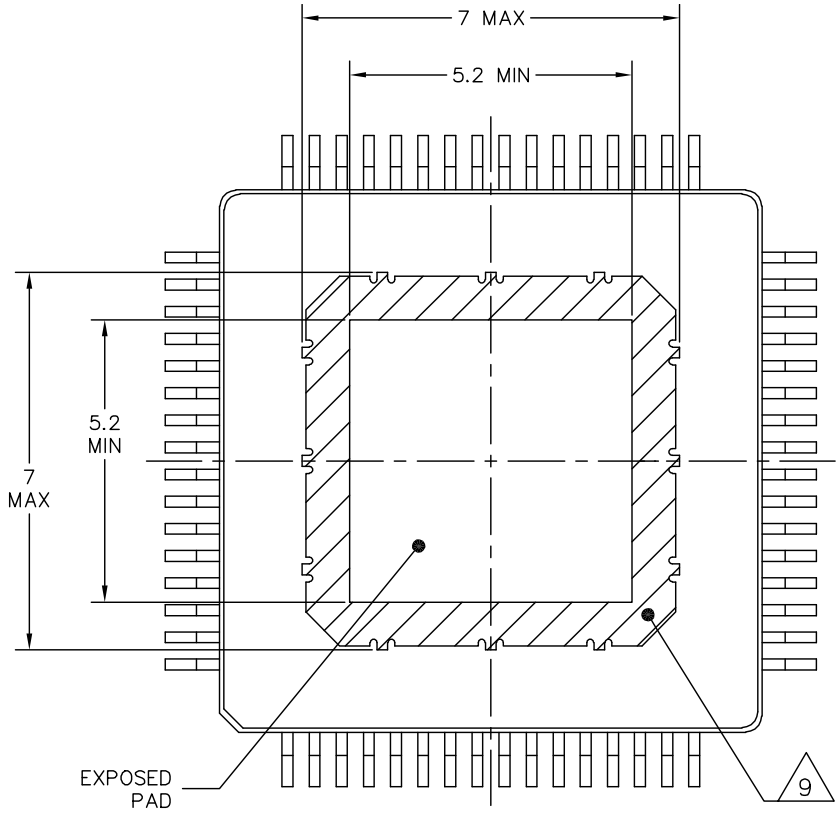
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018



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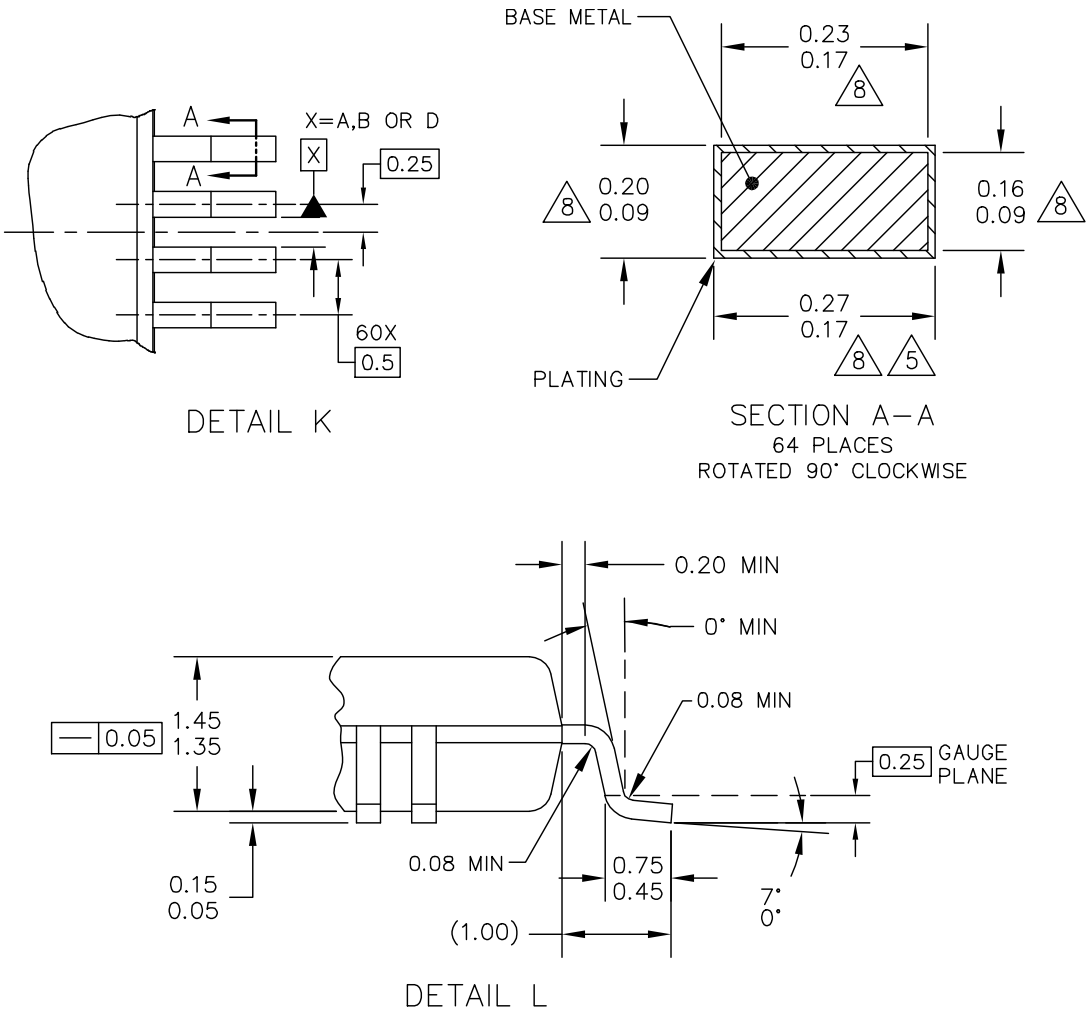

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TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.
10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (EG. TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

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TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

10 Revision history

Revision history

Revision	Date	Description
v.3	25 January 2024	• Updated Figure 1.
v.2	11 December 2023	• Added MC33774AxP product description and characteristics in addition to the MC33774AxA single product initially described in the MC33774A v.1 product brief. As a consequence, the following changes have been done: • General description: Updated text • Features and benefits: Changed bullet item to " … up to 360 mA peak with 0.5 Ω R_{DSon} per channel (typ.)" from "… up to 150 mA average with 0.5 Ω R_{DSon} per channel (typ.)" • Ordering information: Updated Oredering information and Ordering options • Section 7: Reorganized with MC33774AxA1 limiting values table, MC33774 AxP1 limiting values table, MC33774A common limiting values table • Electrical characteristics: Reorganized with MC33774AxA1 limiting values table, MC33774AxP1 limiting values table, MC33774A common limiting values table • Package information: Updated figures to most recent versions • Revision history: Updated to align with NXP style
v.1	03 March 2023	Initial version

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