MCX W23

Ultra-low power, small footprint Bluetooth Low Energy solution with integrated flash and security for IoT

Rev. 2.0 — 20 June 2025 Product data sheet

1 General description

The MCX W23 constitutes a highly integrated, single chip ultra-low power Bluetooth Low Energy 5.3 wireless transceiver with embedded microcontroller and flash, targeted at Internet of things (IoT) applications.

Because of the integrated ultra-low power radio and flash, the MCX W23 provides an extended battery lifetime.

The MCX W23 provides a cost-effective solution within a small solution area required for body-worn sensors and actuators application. The MCX W23 chip integrates the following key functionality:

- An Arm Cortex-M33 with floating point unit (FPU) and memory protection unit (MPU) for application control and Bluetooth Low Energy host stack
- The Arm Cortex-M33 provides a security foundation, offering isolation to protect valuable software IP and data with TrustZone-M technology.
- To support safety and security requirements, the MCX W23 also offers support for SHA-1, SHA2-256, AES, RSA, error code correction, UUID, dynamic encryption and decryption of embedded flash memory with the PRINCE engine, secure boot, protected flash regions, physical unclonable function (PUF) for key store protection and debug authentication.
- A 2.4 GHz RF transceiver supporting Bluetooth Low Energy 5.3
- A low-power 32 MHz crystal oscillator
- 32-bit real-time clock (RTC) with 1 s resolution running in the always-on power domain. Another timer in the RTC can be used for wake-up from all low-power modes, including deep power-down, with 1 ms resolution. The 32.768 kHz free running oscillator (FRO_32k) or a 32.768 kHz external crystal clocks the RTC.
- Integrated flash memory with error code correction, which enables autonomous operation or operation with a host microcontroller.
- Multiple interfaces for control, data, debug, and test
- SPIFI with execute-in-place (XIP) feature uses up to four data lines to access off-chip SPI/DSPI/QSPI flash memory at a higher rate than standard SPI interfaces.
- Flexible power management:
  - MXCW23xB
    - High-voltage supply mode (HV_SM) for 3 V battery support using integrated buck DC-DC converter
    - External regulated supply mode (XR_SM) for PMIC support (bypassing the integrated DC-DC converter)
- High integration, which enables a small solution size

The MCX W23 is offered in a WLCSP37 or QFN40 package.

CAUTION

Semiconductors devices are sensitive to light. Exposure to light sources might cause the WLCSP package variant of the MCX W23 to malfunction.

The MCX W23 WLCSP needs protection from all sides against light.

2 Features and benefits

- Arm Cortex-M33
  - up to 32 MHz
  - TrustZone-M® enabled
  - Floating point unit (FPU)
  - Memory protection unit (MPU)
  - Serial wire debug (SWD) with eight break points and four watch points
- Controller subsystem memories:
  - up to 1 MB of flash with cache and error code correction management, including single bit correction and double bit fault detection
  - up to 128 KB RAM
  - Dedicated packet RAM buffer for radio subsystem: 16 KB data RAM and 512 bytes sequencer RAM
  - 256 KB of ROM
- ROM bootloader supports:
  - Booting of images from an on-chip flash
  - Supports CRC32 image integrity checking
  - Supports flash programming through in-system programming (ISP) commands over the following interfaces: SPI slave interfaces (Flexcomm 0) using mode 3 (CPOL = 1 and CPHA = 1), I2C slave interface (Flexcomm 1), and UART interface (Flexcomm 2) with autobaud. ROM API functions: Flash programming API, MBED TLS API, and secure firmware update API using NXP secure boot file format, version 2.1 (SB2 files)
  - Supports preloading a TrustZone-M® configuration before the application boots
  - Supports booting of images from PRINCE encrypted flash regions
  - Supports NXP Debug Authentication Protocol version 1.0 (RSA-2048) and 1.1 (RSA-4096)
  - Supports setting a sealed part to fault analysis mode through debug authentication
  - Supports boot seed as described in the Arm platform security architecture specification
  - Supports OEM key provisioning during device manufacturing
- Secure boot support:
  - Uses RSASSA-PKCS1-v1_5 signature of SHA256 digest as cryptographic signature verification.
  - Supports RSA-2048 bit public keys (2048-bit modulus, 32-bit exponent).
  - Supports RSA-4096 bit public keys (4096-bit modulus, 32-bit exponent).
  - Uses a x509 certificate format to validate image public keys.
  - Supports up to four revocable root of trust (RoT) or certificate authority keys, root of trust (RoT) establishment by storing the SHA-256 hash digest of the SHA-256 hashes of four RoT public keys in a protected flash region (PFR).
  - Supports an antirollback feature using image key revocation and supports up to 16 image key certificates revocations using the serial number field in the x509 certificate.
- Two flexible DMA engines
- Control/data interfaces
  - Three FlexComm: Each FlexComm can be configured as an SPI, UART, or I^2C interface
  - SPIFI: Quad SPI interface for external serial flash support with execute-in-place (XIP)
  - Up to 23 GPIO
- Security features
  - Arm TrustZone-M® enabled.
  - AES-256 encryption/decryption engine with keys fed directly from PUF or a software-supplied key.
  - Secure hash algorithm (SHA1 and SHA2-256) module supports secure boot with a dedicated DMA controller.

- Physical unclonable function (PUF) using dedicated SRAM for silicon fingerprint; PUF can generate, store, and reconstruct key sizes from 64 bits to 4096 bits. Includes hardware for key extraction.
- True random number generator (TRNG) compliant to NIST SP 800-90B, NIST SP 800-22.
- 128-bit unique device serial number for identification (universal unique identifier: UUID).
- Secure GPIO.
- To enable hardware acceleration for various functions required for certain asymmetric cryptographic algorithms, such as elliptic curve cryptography (ECC) or RSA, a public key coprocessor (PKC) is provided.
- PRINCE module for real-time encryption of data written to on-chip flash and decryption of encrypted flash data during read to allow asset protection, such as securing application code, and enabling secure flash update.
- Protected flash region (PFR) is available to configure secure boot, debug authentication, read UUID, store PUF in a key store area, and user-defined fields available for specific data storage.

- The MCX W23 is compatible with the Bluetooth Low Energy 5.3 specification:
  - Bluetooth Low Energy 5.3 controller subsystem (QDID 200592)
  - Bluetooth Low Energy 5.3 host subsystem (QDID 226395)
  - Includes a 48-bit unique Bluetooth device address
  - Up to 4 simultaneous connections supported
- The MCX W23 supports the following Bluetooth Low Energy features:
  - Device privacy and network privacy modes (Version 5.0)
  - Advertising extension PDUs (Version 5.0)
  - Anonymous device address type (Version 5.0)
  - Up to 2 Mbps data rate (Version 5.0)
  - Long range (Version 5.0)
  - High-duty cycle, non-connectable advertising (Version 5.0)
  - Channel selection algorithm #2 (Version 5.0)
  - High output power (Version 5.0)
  - Advertising Channel Index (Version 5.1)
  - Periodic Advertising Sync Transfer (PAST) (Version 5.1)
  - Supports LE power control feature (Version 5.2)
- RF antenna: 50 Ω single-ended
- RF receiver characteristics
  - Sensitivity −94 dBm in Bluetooth Low Energy 2 Mbps
  - Sensitivity −97 dBm in Bluetooth Low Energy 1 Mbps
  - Sensitivity −100 dBm in Bluetooth Low Energy 500 kbps
  - Sensitivity −102 dBm in Bluetooth Low Energy 125 kbps
  - Accurate RSSI measurement with ±3 dB accuracy
- Flexible RF transmitter level configurability:
  - TX mode 1 (TXM1): Range from −31 dBm to +2 dBm when V_{DD_RF} exceeds 1.1 V
  - TX mode 2 (TXM2): Range from −28 dBm to +6 dBm when V_{DD_RF} exceeds 1.7 V
- Flexible boot modes:
  - Autonomous boot from flash
  - In-system programming (ISP)
  - Secure bootloader, which enables OEM key provisioning by creating a root of trust for execution of authenticated and encrypted application images (SB2.1 format).
- Flexible power management:
  - MXCW23xB
    - High-voltage supply mode (HV_SM) for 3 V battery support using integrated buck DC-DC converter

    - External regulated supply mode (XR_SM) for PMIC support (bypassing the integrated DC-DC converter)
- Low current consumption at room temperature (T_{amb} = 25°C):
  - MCX W23xB in XR_SM mode (1.8 V)
    - Power-off current: 80 nA with PIO0_21 pin wake-up
    - Deep power-down current: 650 nA with RTC FRO_32k wake-up
    - Deep power-down current: 695 nA with RTC XO_32k wake-up
    - Power-down current: 1.18 µA (16 kB RAM retention) with RTC FRO_32k wake-up
    - Deep-sleep current: 4.50 µA (full RAM retention) with RTC FRO_32k wake-up
    - Bluetooth Low Energy current during radio RX packet phase: 6.64 mA
    - Bluetooth Low Energy current during radio TX packet phase: 9.68 mA (0 dBm output power)
  - MCX W23xB in HV_SM mode (3.0 V)
    - Power-off current: 25 nA with PIO0_21 pin wake-up
    - Deep power-down current: 645 nA with RTC FRO_32k wake-up
    - Deep power-down current: 690 nA with RTC XO_32k wake-up
    - Power-down current: 1.23 µA (16 kB RAM retention) with RTC FRO_32k wake-up
    - Deep-sleep current: 4.61 µA (full RAM retention) with RTC FRO_32k wake-up
    - Bluetooth Low Energy current during radio RX packet phase : 3.33 mA
    - Bluetooth Low Energy current during radio TX packet phase : 4.83 mA (0 dBm output power)
- Clock generation:
  - Integrated low-power high-frequency free running oscillator (FRO) providing a set of selectable outputs, 32 MHz, 24 MHz, and 12 MHz
  - Crystal oscillator for a 32 MHz crystal required for radio functionality (XO_32M)
  - Integrated 32.768 kHz ultra-low power free running oscillator (FRO_32k)
  - Crystal oscillator for a 32.768 kHz crystal (XO_32k)
  - Integrated 1 MHz ultra-low power free running oscillator (FRO_1M)
- Timers:
  - 5 Standard timer/counters (CTIMER)
  - Windowed watchdog timer (WWDT)
  - Real-time clock (RTC)
  - Multirate timer (MRT)
  - Microtick timer (UTICK)
  - SCTimer/PWM
  - 42-bit free running OS Timer
- Packaging:
  - WLCSP package: 6.56 mm^2 with 37 bumps
  - QFN package: 5 mm × 5 mm with 40 pins
- Easy development:
  - EVK board containing MCX W23 with support interfaces for SW development
  - MCUXpresso integrated development environment (IDE) brings developers an easy-to-use Eclipse-based development environment
  - Source code for the peripheral drivers
  - Bluetooth Low Energy host stack
- Low number of external passive components
- Operating temperature: −40 °C to +85 °C
- Pb-free and compliant with RoHS Directive EU 2015/863 (RoHS 3)

3 Applications

The main application targets of the MCX W23 are Internet of things (IoT) applications running directly from a coin battery in a small body-worn device.

The MCX W23 family supports the following supply configurations:

- MCX W23xB is used with 3 V battery (for example, Li coincell) attached to the VBAT_HV pin. The DC-DC converter gets configured as a buck converter and generates a 1.2 V output supply on VBAT_LV pin for the internal logic, the external sensors, and the radio subsystem. This mode is called high-voltage supply mode (HV_SM).
- MCX W23xB can also be used in a system with external PMIC. The integrated DC-DC converter can be disabled. To reduce system costs, no inductor is necessary. This mode is called external regulated supply mode (XR_SM).

The integrated Arm Cortex-M33 provides a flexible, secure, and high-performance environment for developing sensor and actuator applications.

The system supports optional features, for example:

- An external SPI flash for data logging applications and execute-in-place (XIP)

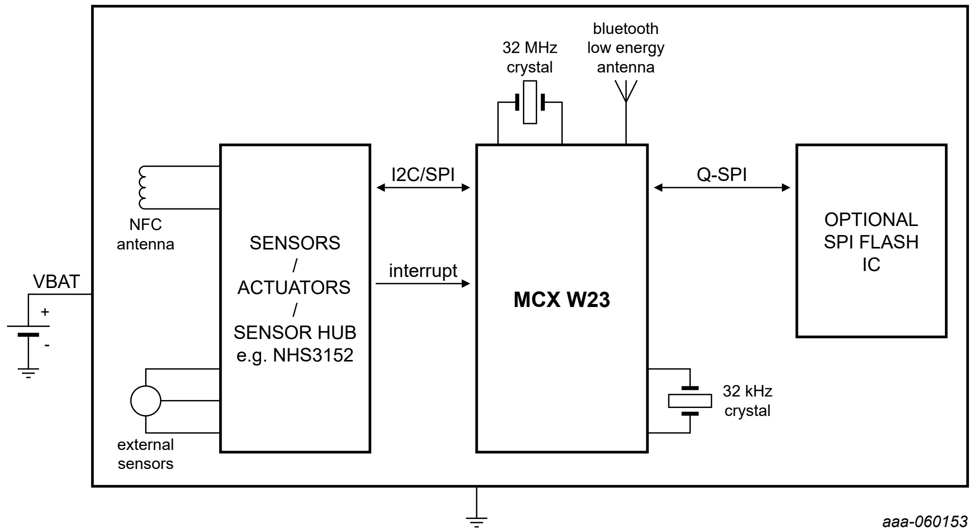

Figure 1. Typical application diagram of the MCX W23

4 Ordering information

Table 1. Ordering information

Type number	Flash (KB)	RAM (KB)	DCDC	Package	Package Reference
MCXW236BIUKAR	1024	128	Supports HV_SM (Buck) and XR_SM (PMIC) mode	WLCSP37	SOT2173-1
MCXW236BIHNAR	1024	128	Supports HV_SM (Buck) and XR_SM (PMIC) mode	HVQFN40	SOT1369-5
MCXW235BIUKAR	640	96	Supports HV_SM (Buck) and XR_SM (PMIC) mode	WLCSP37	SOT2173-1
MCXW235BIHNAR	640	96	Supports HV_SM (Buck) and XR_SM (PMIC) mode	HVQFN40	SOT1369-5

5 Block diagram

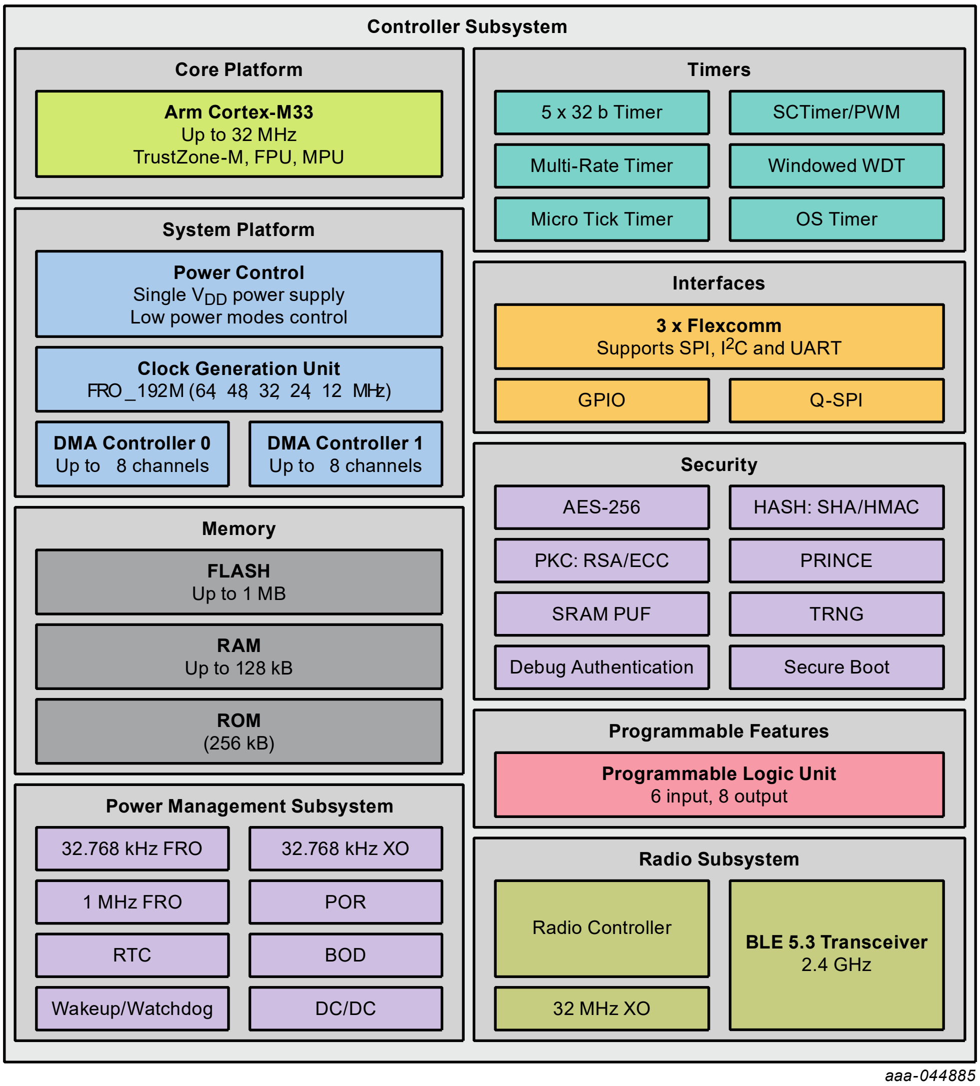

Figure 2. MCX W23 block diagram

6 Package and pinning information

This section gives an overview of the package and pinning of the MCX W23.

6.1 WLCSP package

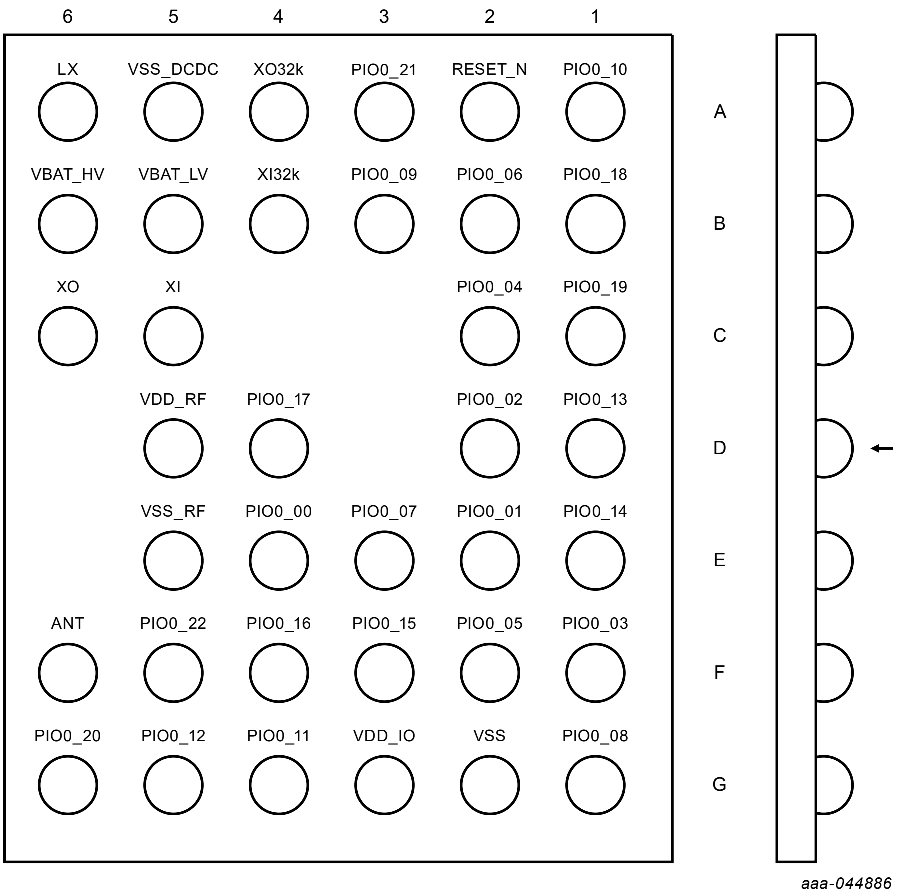

Figure 3. MCX W23 WLCSP - Bump configuration (bottom view of package) - 7 × 6 grid: 37 bumps

Figure 3 show the MCX W23 WLCSP bump layout.

To optimize radio performance, bumps D6 and E6 are depopulated.

To provide space for vias, bumps D3, C3, and C4 are depopulated.

6.2 QFN package

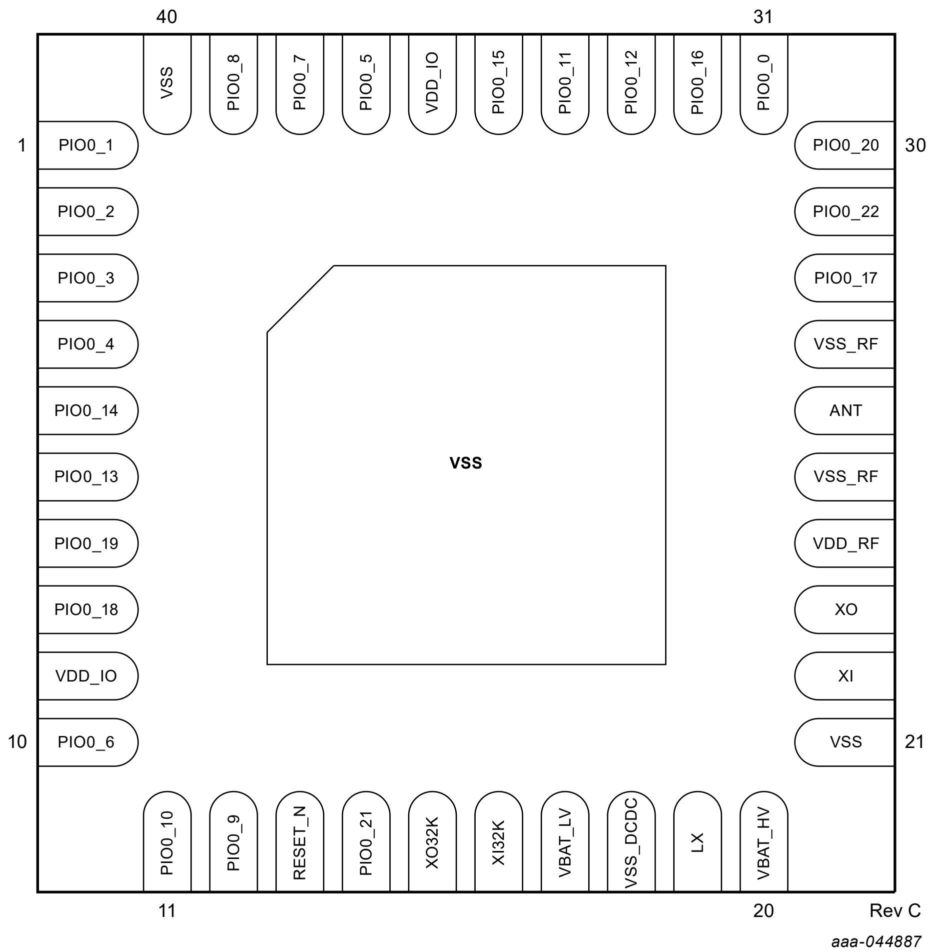

Figure 4. QFN40 - Pad configuration (transparent top view of package) - 40 pads

6.3 Pin description

Table 2 lists the description of all the pins of the MCX W23. It provides the assignment of these pins to the different supported packages and associated pin type.

The different types are:

- PWR: supply pin
- GND: ground pin
- RF: RF signal pin
- A: analog pin
- AI: analog input pin
- DIO: digital IO pin

When the part is in boundary scan mode, the hardware selects the JTAG functions, TCK functions, TMS functions, TDI functions, and TDO functions on pins PIO0_14 to PIO0_17.

Table 2. MCX W23 pin description

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
B6	20	-	VBAT_HV	PWR		For MCX W23xB in high-voltage supply mode (HV_SM), input supply connected to 3 V battery (input to DC-DC converter in buck mode). For MCX W23xB in external regulated supply mode (XR_SM), input supply for internal flash memory.
B5	17	-	VBAT_LV	PWR		For MCX W23xB in high-voltage supply mode (HV_SM), output connected to buffer capacitor (output of DC-DC converter buck mode) For MCX W23xB in external regulated supply mode (XR_SM), input supply for analog and digital subsystem.
G3	9; 36	-	VDD_IO	PWR		input supply for digital IO
D5	24	-	VDD_RF	PWR		input supply for RF subsystem
E5	25; 27	-	VSS_RF	GND		RF ground ***Note:*** *In the HVQFN package these pins are shorted to the VSS pins inside the package*
A5	18	-	VSS_DCDC	GND		DC-DC converter ground
G2	21; 40	-	VSS	GND		digital and IO ground ***Note:*** *HVQFN exposed die attach pad is connected to pins 21 and 40 inside the HVQFN package. They must share ground plane on the PCB.*
A6	19	-	LX	PWR		terminal for external inductor the integrated DC-DC converter uses For the MCX W23 in XR_SM mode, this pin can be left open or connected through a resistor of at least 250 Ω to ground
C5	22	-	XI_32M	AI		32 MHz crystal oscillator input
C6	23	-	XO_32M	A		32 MHz crystal oscillator output
B4	16	-	XI_32K	AI		32.768 kHz crystal oscillator input
A4	15	-	XO_32K	A		32.768 kHz crystal oscillator output
F6	26	-	ANT	RF		antenna pin
A2	13	PU	RESET_N	AI		External reset input A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. The pin is internally pulled up high on-chip to V_{DD_IO}.

Table 2. MCX W23 pin description...*continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
E4	31	Z	PIO0_0 [2]	DIO	0	PIO0_0 GPIO - general-purpose digital input/ output pin
					1	FC0_CTS_SDA_SSEL0 - Flexcomm 0 USART clear-to-send, I^2C data I/O, SPI slave select 0
					2	FC1_RTS_SCL_SSEL1 - Flexcomm 1 USART request-to-send, I^2C clock, SPI slave select 1
					7	SEC_PIO0_0 - secure GPIO pin
					9	CTIMER0_MAT0 - 32-bit CTIMER 0 match output 0
					10	CTIMER_INP0 - capture input 0 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 0 SPI SSEL0 function.*
E2	1	Z	PIO0_1 [2]	DIO	0	PIO0_1 GPIO - general-purpose digital input/ output pin
					1	FC0_RTS_SCL_SSEL1 - Flexcomm 0 USART request-to-send, I^2C clock, SPI slave select 1
					2	FC2_SCK - Flexcomm 2 USART, SPI, or I^2C clock
					6	PLU_CLKIN - PLU clock input
					7	SEC_PIO0_1 - secure GPIO pin
					9	CTIMER0_MAT1 - 32-bit CTIMER 0 match output 1
					10	CTIMER_INP1 - capture input 1 to CTIMER input multiplexers
D2	2	Z	PIO0_2 [2]	DIO	0	PIO0_2 GPIO - general-purpose digital input/ output pin
					1	FC0_RXD_SDA_MOSI - Flexcomm 0 USART receiver, I^2C data I/O, SPI master-out/slave-in data
					3	SCT_OUT9 - SCTimer/PWM output 9
					7	SEC_PIO0_2 - secure GPIO pin
					9	CTIMER0_MAT2 - 32-bit CTIMER 0 match output 2
					10	CTIMER_INP2 - capture input 2 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 0 SPI MOSI function.*

Table 2. MCX W23 pin description*...continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
F1	3	Z	PIO0_3 [2]	DIO	0	PIO0_3 GPIO - general-purpose digital input/ output pin
					1	FC0_TXD_SCL_MISO - Flexcomm 0 USART transmitter, I^2C clock, SPI master-in/slave-out data
					3	SCT_OUT8 - SCTimer/PWM output 8
					4	FREQME_GPIO_3 - frequency measure pin 3 clock input
					7	SEC_PIO0_3 - secure GPIO pin
					9	CTIMER0_MAT3 - 32-bit CTIMER 0 match output 3
					10	CTIMER_INP3 - capture input 3 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 0 SPI MISO function.*
C2	4	Z	PIO0_4 [2]	DIO	0	PIO0_4 GPIO - general-purpose digital input/ output pin
					1	FC0_SCK - Flexcomm 0 USART, SPI, or I^2C clock
					3	SCT_OUT7 - SCTimer/PWM output 7
					7	SEC_PIO0_4 - secure GPIO pin
					9	CTIMER1_MAT0 - 32-bit CTIMER 1 match output 0
					10	CTIMER_INP4 - capture input 4 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 0 SPI SCL function*

Table 2. MCX W23 pin description...*continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
F2	37	Z	PIO0_5[2]	DIO	0	PIO0_5 GPIO - general-purpose digital input/ output pin
					2	FC2_CTS_SDA_SSEL0 - Flexcomm 2 USART clear-to-send, I^2C data I/O, SPI slave select 0
					3	SCT_OUT6 - SCTimer/PWM output 6
					5	UTICK_CAP0 - Microtick timer capture input 0
					6	PLU_IN0 - PLU input 0
					7	SEC_PIO0_5 - secure GPIO pin
					8	SPIFI_CSN - Quad-SPI chip select
					9	CTIMER1_MAT1 - 32-bit CTIMER 1 match output 1
					10	CTIMER_INP5 - capture input 5 to CTIMER input multiplexers
B2	10	Z	PIO0_6 [2]	DIO	0	PIO0_6 GPIO - general-purpose digital input/ output pin
					2	FC2_RXD_SDA_MOSI - Flexcomm 2 USART receiver, I^2C data I/O, SPI master-out/slave-in data
					3	SCT_OUT5 - SCTimer/PWM output 5
					5	UTICK_CAP1 - microtick timer capture input 1
					6	PLU_IN1 - PLU input 1
					7	SEC_PIO0_6 - Secure GPIO pin
					8	SPIFI_IO0 - Quad-SPI data I/O 0
					9	CTIMER1_MAT2 - 32-bit CTIMER 1 match output 2
					10	CTIMER_INP6 - Capture input 6 to CTIMER input multiplexers
E3	38	Z	PIO0_7 [2]	DIO	0	PIO0_7 GPIO - general-purpose digital input/ output pin
					2	FC2_TXD_SCL_MISO - Flexcomm 2 USART transmitter, I^2C clock, SPI master-in/slave-out data
					3	SCT_OUT4 - SCTimer/PWM output 4
					5	UTICK_CAP2 - microtick timer capture input 2
					6	PLU_IN2 - PLU input 2
					7	SEC_PIO0_7 - secure GPIO pin

Table 2. MCX W23 pin description...*continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
					8	SPIFI_IO1 - quad-SPI data I/O 0
					9	CTIMER1_MAT3 - 32-bit CTIMER 1 match output 3
					10	CTIMER_INP7 - capture input 7 to CTIMER input multiplexers
G1	39	Z	PIO0_8 [2]	DIO	0	PIO0_8 GPIO - general-purpose digital input/ output pin
					2	FC2_RTS_SCL_SSEL1 - Flexcomm 2 USART request-to-send, I^2C clock, SPI slave select 1
					3	SCT_GPI7 - pin input 7 to SCTimer/PWM
					5	UTICK_CAP3 - microtick timer capture input 3
					6	PLU_IN3 - PLU input 3
					7	SEC_PIO0_8 - secure GPIO pin
					8	SPIFI_IO2 - quad-SPI data I/O 2
					9	CTIMER2_MAT0 - 32-bit CTIMER 2-match output 0
					10	CTIMER_INP8 - capture input 8 to CTIMER input multiplexers
B3	12	Z	PIO0_9 [2]	DIO	0	PIO0_9 GPIO - general-purpose digital input/ output pin
					3	SCT_GPI6 - pin input 6 to SCTimer/PWM
					4	CLKOUT - output of the CLKOUT function
					6	PLU_IN4 - PLU input 4
					7	SEC_PIO0_9 - secure GPIO pin
					8	SPIFI_IO3 - quad-SPI data I/O 3
					9	CTIMER2_MAT1 - 32-bit CTIMER 2-match output 1
					10	CTIMER_INP9 - capture input 9 to CTIMER input multiplexers
A1	11	Z	PIO0_10 [2]	DIO	0	PIO0_10 GPIO - general-purpose digital input/ output pin
					2	FC2_SCK - Flexcomm 2 USART, SPI, or I^2C clock
					3	SCT_GPI5 - pin input 5 to SCTimer/PWM
					6	PLU_IN5 - PLU input 5
					7	SEC_PIO0_10 - secure GPIO pin

Table 2. MCX W23 pin description...*continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
					8	SPIFI_CLK - quad-SPI clock
					9	CTIMER2_MAT2 - 32-bit CTIMER 2-match output 2
					10	CTIMER_INP10 - capture input 10 to CTIMER input multiplexers
G4	34	PD	PIO0_11[2]	DIO	0	PIO0_11 GPIO - general-purpose digital input/ output pin
					1	SWCLK - serial wire debug (SWD) clock. The default function after booting
					2	FC1_CTS_SDA_SSEL0 - Flexcomm 1 USART clear-to-send, I^2C data I/O, SPI slave select 0
					3	SCT_GPI4 - pin input 4 to SCTimer/PWM
					4	FREQME_GPIO_11 - frequency measure pin 11 clock input
					5	UTICK_CAP0 - microtick timer capture input 0
					6	PLU_CLKIN - PLU clock input
					7	CTIMER2_MAT3 - 32-bit CTIMER 2-match output 3
					9	CTIMER_INP11 - capture input 11 to CTIMER input multiplexers
					10	SEC_PIO0_11 - secure GPIO pin
						Note: *To enter the boundary scan mode, this pin must be pulled high at start-up.*
G5	33	PU	PIO0_12 [2]	DIO	0	PIO0_12 GPIO - general-purpose digital input/ output pin
					1	SWDIO - serial wire debug (SWD) I/O. The default function after booting
					2	FC1_RTS_SCL_SSEL1 - Flexcomm 1 USART request-to-send, I^2C clock, SPI slave select 1
					3	SCT_OUT3 - SCTimer/PWM output 3
					4	FREQME_GPIO_12 - frequency measure pin 12 clock input
					5	UTICK_CAP1 - microtick timer capture input 1
					6	PLU_OUT0 - PLU output 0
					7	SEC_PIO0_12 - secure GPIO pin
					9	CTIMER3_MAT0 - 32-bit CTIMER 3-match output 0

Table 2. MCX W23 pin description...*continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
					10	CTIMER_INP12 - capture input 12 to CTIMER input multiplexers
						Note: *To enter the boundary scan mode, this pin must be pulled low at start-up.*
D1	6	Z	PIO0_13[3]	DIO	0	PIO0_13 GPIO - general-purpose digital input/ output pin
					1	FC1_RXD_SDA_MOSI - Flexcomm 1 USART receiver, I^2C data I/O, SPI master-out/slave-in data
					2	FC2_CTS_SDA_SSEL0 - Flexcomm 2 USART clear-to-send, I^2C data I/O, SPI slave select 0
					3	SCT_OUT2 - SCTimer/PWM output 2
					5	UTICK_CAP2 - microtick timer capture input 2
					6	PLU_OUT1 - PLU output 1
					7	SEC_PIO0_13 - secure GPIO pin
					9	CTIMER3_MAT1 - 32-bit CTIMER 3-match output 1
					10	CTIMER_INP13 - capture input 13 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 1 SDA function.*
E1	5	Z	PIO0_14 [3]	DIO	0	PIO0_14 GPIO - general-purpose digital input/ output pin
					1	FC1_TXD_SCL_MISO - Flexcomm 1 USART transmitter, I^2C clock, SPI master-in/slave-out data
					2	FC2_RTS_SCL_SSEL1 - Flexcomm 2 USART request-to-send, I^2C clock, SPI slave select 1
					3	SCT_OUT1 - SCTimer/PWM output 1
					4	FREQME_GPIO_14 - frequency measure pin 14 clock input
					5	UTICK_CAP3 - microtick timer capture input 3
					6	PLU_OUT2 - PLU output 2
					7	SEC_PIO0_14 - secure GPIO pin
					9	CTIMER3_MAT2 - 32-bit CTIMER 3-match output 2
					10	CTIMER_INP14 - capture input 14 to CTIMER input multiplexers

Table 2. MCX W23 pin description*...continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
						Note: *In ISP mode, this pin is set to the Flexcomm 1 SCL CLK function.* ***Note:*** *In boundary scan mode, this pin is test-data-in (TDI).*
F3	35	Z	PIO0_15 [2]	DIO	0	PIO0_15 GPIO - general-purpose digital input/ output pin
					1	SWO - serial wire debug (SWD) trace output
					2	FC1_CTS_SDA_SSEL0 - Flexcomm 1 USART clear-to-send, I^2C data I/O, SPI slave select 0
					3	SCT_OUT0 - SCTimer/PWM output 0
					6	PLU_OUT3 - PLU output 3
					7	SEC_PIO0_15 - secure GPIO pin
					9	CTIMER3_MAT3 - 32-bit CTIMER 3-match output 3
					10	CTIMER_INP15 - capture input 15 to CTIMER input multiplexers
						Note: *In boundary scan mode, this pin is test mode select (TMS).*
F4	32	Z	PIO0_16 [2]	DIO	0	PIO0_16 GPIO - general-purpose digital input/ output pin
					2	FC1_SCK - Flexcomm 1 USART, SPI, or I^2C clock
					3	SCT_GPI3 - SCTimer/PWM input 3
					6	PLU_OUT4 - PLU output 4
					7	SEC_PIO0_16 - secure GPIO pin
					9	CTIMER4_MAT0 - 32-bit CTIMER 4-match output 0
					10	CTIMER_INP16 - capture input 16 to CTIMER input multiplexers
						Note: *In boundary scan mode, this pin is test-clock-in (TCK)*

Table 2. MCX W23 pin description...continued

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
D4	28	Z	PIO0_17 [2]	DIO	0	PIO0_17 GPIO - general-purpose digital input/ output pin
					1	SWO - serial wire debug (SWD) trace output
					2	FC0_CTS_SDA_SSEL0 - Flexcomm 0 USART clear-to-send, I^2C data I/O, SPI slave select 0
					3	SCT_GPI2 - SCTimer/PWM input 2
					6	PLU_OUT5 - PLU output 5
					7	SEC_PIO0_17 - secure GPIO pin
					9	CTIMER4_MAT1 - 32-bit CTIMER 4-match output 1
					10	CTIMER_INP17 - capture input 17 to CTIMER input multiplexers
						Note: *In boundary scan mode, this pin is test-data-out (TDO).*
B1	8	Z	PIO0_18 [4]	DIO	0	PIO0_18 GPIO - general-purpose digital input/ output pin
					1	FC2_RXD_SDA_MOSI - Flexcomm 2 USART receiver, I^2C data I/O, SPI master-out/slave-in data
					3	SCT_GPI1 - SCTimer/PWM input 1
					4	CLKOUT - output of the CLKOUT function
					6	PLU_OUT6 - PLU output 6
					7	SEC_PIO0_18 - secure GPIO pin
					9	CTIMER4_MAT2 - 32-bit CTIMER 4-match output 2
					10	CTIMER_INP18 - capture input 18 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 2 RXD function.*

Table 2. MCX W23 pin description...*continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
C1	7	Z	PIO0_19[4]	DIO	0	PIO0_19 GPIO - general-purpose digital input/ output pin
					1	FC2_TXD_SCL_MISO - Flexcomm 2 USART transmitter, I^2C clock, SPI master-in/slave-out data
					3	SCT_GPI0 - SCTimer/PWM input 0
					6	PLU_OUT7 - PLU output 7
					7	SEC_PIO0_19 - secure GPIO pin
					9	CTIMER4_MAT3 - 32-bit CTIMER 4-match output 3
					10	CTIMER_INP19 - capture input 19 to CTIMER input multiplexers
						Note: *In ISP mode, this pin is set to the Flexcomm 2 TXD function.*
G6	30	PU	PIO0_20[2]	DIO	0	PIO0_20 GPIO - general-purpose digital input/ output pin
					7	SEC_PIO0_20 - secure GPIO pin
					10	CTIMER_INP20 - capture input 20 to CTIMER input multiplexers
						Note: *The state of this pin at reset determines the boot mode for the part. If it is pulled down, the ISP mode is invoked.* ***Note:*** *To enter the boundary scan mode, this pin must be pulled low at start-up.*
A3	14	Z	PIO0_21[2]	DIO	0	PIO0_21 GPIO - general-purpose digital input/ output pin
					1	WAKEUP_INTERRUPT The WAKEUP pin can be configured with a PU or PD level. This pin can trigger a wake-up from low-power modes.
					7	SEC_PIO0_21 - secure GPIO pin
					10	CTIMER_INP21 - capture input 21 to CTIMER input multiplexers

Table 2. MCX W23 pin description*...continued*

WLCSP	QFN40 pin	Reset state[1]	Symbol	Type	Function #	Pin description
F5	29	PD	PIO0_22[2]	DIO	0	PIO0_22 GPIO - general-purpose digital input/output pin
					7	SEC_PIO0_22 - secure GPIO pin
					10	CTIMER_INP22 - capture input 22 to CTIMER input multiplexers
						Note: *To enter the boundary scan mode, this pin must be pulled high at start-up.*

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin toward VDD). PD = input mode, pull-down enabled (pull-down resistor pulls down pin toward VSS). Z = high impedance; pull-up, pull-down, and input disabled. AI = analog input. I = input. O = output. I/O = input/output. Reset state reflects the pin state at reset without boot code operation.

[2] Pad with programmable glitch filter; provides digital I/O functions with TTL levels and hysteresis; normal drive strength. Pulse width of spikes or glitches suppressed by an input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C fast mode, and I^2C fast mode plus. To provide output functionality, the pin requires an external pull-up. When power is switched off, this pin is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[4] Pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled.

7 Functional description

7.1 Controller subsystem

Figure 5 shows the block diagram of the microcontroller subsystem.

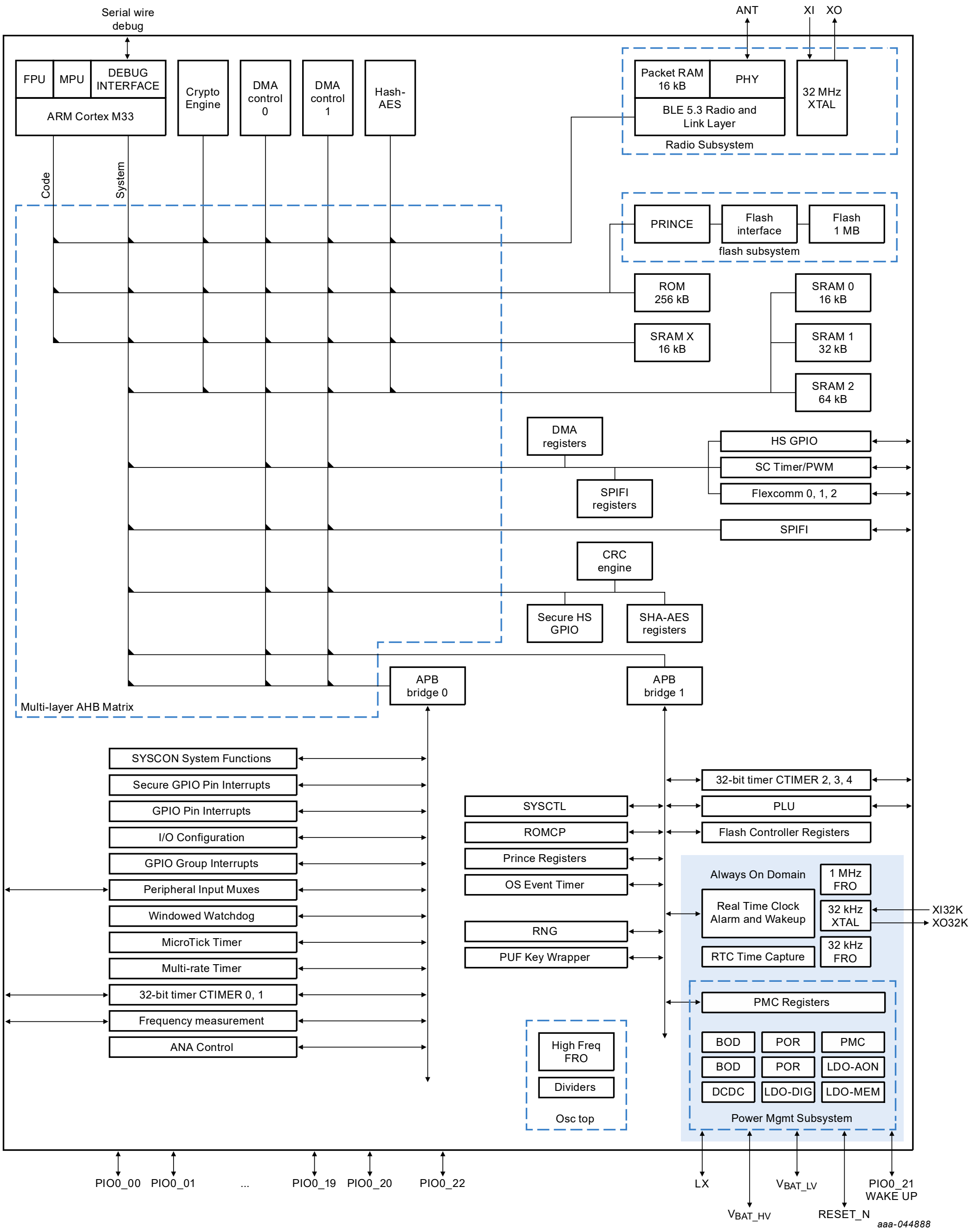

Figure 5. Microcontroller block diagram

Some main components are described in the subsequent subsections.

7.1.1 Architectural overview

The Arm Cortex M33 includes two AHB-Lite buses, one system bus, and one code bus. The code-AHB (C-AHB) interface is used for any instruction fetch and data access to the code region of the ARMv8-M memory map ([0x00000000 to 0x1FFFFFFF]). The system-AHB (S-AHB) interface is used for instruction fetch and data access to all other regions of the ARMv8-M memory map ([0x20000000 to 0xFFFFFFFF]).

To connect the Arm Cortex-M33 buses and other bus masters to peripherals in a flexible manner, the MCX W23 uses a multilayer AHB matrix. It optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters. Figure 5 shows the available matrix connections.

7.1.2 Arm Cortex-M33 processor

The Arm Cortex-M33 is a general-purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The Arm Cortex M33 offers many features, including:

- A Thumb-2 instruction set
- Low interrupt latency
- Hardware multiply and divide
- Interruptable/continuable multiple load and store instructions
- Automatic state save and restore for interrupts
- Tightly integrated interrupt controller with wake-up interrupt controller
- Multiple core buses capable of simultaneous accesses

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is executed, its successor is decoded, and a third instruction is fetched from memory.

The Arm Cortex-M33 provides a security foundation, offering isolation to protect valuable IP and data with TrustZone technology. It simplifies the design and software development of digital signal control systems with the integrated digital signal processing (DSP) instructions.

The Arm Cortex-M33 core includes a SysTick timer that is intended to generate a dedicated SYSTICK exception.

On the MCX W23, the Cortex-M33 is augmented with a hardware public key coprocessor (PKC) providing accelerated support for cryptography.

7.1.3 Arm Cortex-M33 integrated floating-point unit

The floating-point unit (FPU) fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.1.4 Memories

7.1.4.1 On-chip flash

Support for up to 1 MB (main flash array) + 32 KB (information flash region) of on-chip flash memory. Each 16-byte phrase in flash is protected by a 9-bit error correction code, which allows the correction of single-bit faults and detects double bit faults.

The protected flash region (PFR) is 40 KB. It is mapped on the information flash region (32 KB) and the last sector (8 KB) of the main flash array.

The protected flash region is available to configure secure boot, debug authentication, read UUID, store PUF in a key store area, and user-defined fields available for specific data storage.

7.1.4.2 On-chip static RAM

The on-chip static RAM supports up to 128 KB SRAM (divided into 4 physical blocks) with a separate bus master access for higher throughput and individual power control for low-power operation. The 16 KB SRAM is on the Arm C-bus (SRAMX). The remaining 112 KB is on the Arm S-bus split into 3 physical blocks (1 block of 16 KB - SRAM0, 1 block of 32 KB -SRAM1, and 1 block of 64 KB - SRAM2).

SRAM memory is also dedicated for the Bluetooth Low Energy radio. The Bluetooth Low Energy radio has 16 KB data SRAM and 512 bytes sequencer SRAM.

7.1.4.3 On-chip ROM

The on-chip ROM contains the bootloader and the following features:

- Booting of images from the on-chip flash
- Supports CRC32 image integrity checking
- Supports flash programming through in-system programming (ISP) commands over the following interfaces: UART interface (Flexcomm 2) with autobaud, SPI slave interfaces (Flexcomm 0) using mode 3 (CPOL = 1 and CPHA = 1), and I^2C slave interface (Flexcomm 1)
- ROM API functions: Flash programming API, the power control API, and the secure firmware update API using NXP Secure Boot file format, version 2.1 (SB2 files)
- Supports booting of images from PRINCE encrypted flash region
- Supports NXP Debug Authentication Protocol version 1.0 (RSA-2048) and 1.1 (RSA-4096)
- Supports setting a sealed part to fault analysis mode via debug authentication
- Supports recovery boot from external flash using Flexcomm 2

The on-chip ROM supports a secure boot based on the RSA public key signature.

- Uses RSASSA-PKCS1-v1_5 signature of SHA256 digest as cryptographic signature verification.
- Supports RSA-2048 bit public keys (2048-bit modulus, 32-bit exponent).
- Supports RSA-4096 bit public keys (4096-bit modulus, 32-bit exponent).
- Uses x509 certificate format to validate image public keys.
- Supports up to four revocable root of trust (RoT) or certificate authority keys. Root of trust establishment by storing the SHA-256 hash digest of the SHA-256 hashes of four RoT public keys in the protected flash region (PFR).
- Supports an antirollback feature using image key revocation and supports up to 16 image key certificate revocations using a serial number field in an x509 certificate.

7.1.5 DMA controller

The DMA controller allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

Two DMA controllers are included, for a secure DMA or a non-secure DMA.

7.1.5.1 Features

- The DMA controller has two instances. DMA0 is intended for non-secure use. DMA1 is intended for secure use.
- DMA0: 8 channels. They come from the Flexcomm interfaces (0, 1, and 2), the SPIFI interface, AES, and the SHA interfaces. 21 trigger sources are available.
- DMA1: 8 channels. They come from the Flexcomm Interfaces (0, 1, and 2), the SPIFI interface, AES, and the SHA interfaces. 15 trigger sources are available.
- On-chip or off-chip events can trigger DMA operations.
- Priority is user-selectable for each channel (up to eight priority levels).
- Continuous priority arbitration.
- Address cache with four entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.1.6 Flexcomm serial communication interface

A Flexcomm interface provides a choice of serial communication peripheral functions, one of which the user must choose before the function can be configured and used.

Supported functions:

- USART with asynchronous operation or synchronous master or slave operation
- SPI master or slave with up to 2 slave selects
- I^2C, including separate master, slave, and monitor functions

The MCX W23 contains three independent Flexcomm interfaces.

7.1.6.1 Flexcomm SPI

Features

- The maximum supported bit rate for SPI master and slave (transmit/receive) mode is 18 Mbit/s over the full VDD_IO range (VBAT_LV supply range).
  If VDD_IO exceeds 1.7 V (VBAT_HV supply range), the maximum supported bit rate for SPI slave mode can be increased up to 24 Mbit/s.
- Master and slave operation.
- Data frames of 4 bits to 16 bits supported directly. Software supports larger frames.
- The SPI function supports separate transmit and receive FIFOs with eight entries each.
- Supports DMA transfers: SPI transmit and receive functions can be operated with the system DMA controller.
- Data can be transmitted to a slave without the necessity to read incoming data, which can be useful while setting up an SPI memory.
- Up to two slave-select input/outputs with selectable polarity and flexible usage.

7.1.6.2 Flexcomm I^2C

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in master mode or slave mode, depending on if the chip must initiate a data transfer or is only addressed. The I^2C is a multimaster bus. More than one bus master connected to it can control it.

Features

- Supports standard (100 kbps), fast mode (400 kbps), and fast mode Plus (specific I^2C pins) with data rates of up to 1 Mbit/s.
- Supports high-speed mode with data rates up to 3.4 Mbit/s (specific I^2C pins when VDD_IO at 1.8 V or higher).
- Independent master, slave, and monitor functions.
- Supports multimaster and multimaster with slave functions.
- Multiple I^2C slave addresses supported in hardware.
- To respond to multiple I^2C-bus addresses, one slave address can be selectively qualified with a bit mask or an address range.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Separate DMA requests for master, slave, and monitor functions.
- No chip clocks are required to receive and compare an address as a slave. So, this event can wake up the device from deep-sleep mode.
- Automatic modes optionally allow less software overhead for some use cases.

7.1.6.3 Flexcomm UART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection.
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in baud rate generator with autobaud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for receiver ready, transmitter ready, receiver idle, change in receiver break detect, framing error, parity error, overrun, underrun, delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.

- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep and, when a character is received, can wake up the device.
- USART transmit and receive functions work with the system DMA controller.
- The USART function supports separate transmit and receive FIFO with 16 entries each.

7.1.7 SPI flash interface (SPIFI)

The SPI flash interface (SPIFI) allows low pin-count serial flash memories to be connected to the MCX W23 with little performance penalty compared to higher pin-count parallel flash memories. It implements basic, dual, and quad SPI in half-duplex mode and allows for memory-mapped access. The SPIFI also includes a cache to reduce access power by caching recently accessed code or data.

The maximum supported bit rate for the SPIFI interface is 32 Mbit/s over the full VDD_IO range.

This maximum supported bit rate for the SPIFI interface can be increased up to 64 Mbit/s if VDD_IO is above 1.7 V.

7.1.8 General-purpose I/O

The MCX W23 provides one GPIO port with a total of 23 GPIO pins.

The GPIO registers control device pins that are not connected to a specific peripheral function. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

To achieve the fastest possible I/O timing, GPIO registers are located on the AHB.

7.1.9 Timers

The MCX W23 contains the following timers, available for use with application software:

- Standard timer/counters:
  The MCX W23 includes five general-purpose 32-bit timer/counters. The timer/counter is designed to count the cycles of the system-derived clock or an externally supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers.
- Windowed watchdog timer (WWDT):
  The WWDT enables the resetting or interrupting of the microcontroller within a programmable time if it enters an erroneous state.
- Real-time clock (RTC):
  The RTC block is used to count seconds and generate an alarm interrupt to the processor whenever the counter value equals the value programmed into the associated 32-bit match register.
- Multirate timer (MRT):
  The MRT provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval. Each channel operates independently from the other channels.
- Microtick timer (UTICK):
  The ultralow power microtick timer can be used to wake up the device from low-power modes.
- SCTimer/PWM subsystem (SCT):
  The SCTimer/PWM is a flexible timer module, which can create complex PWM waveforms and perform other advanced timing and control operations with minimal or no CPU intervention.

- 42-bit free running OS timer as a continuous timebase for the system, available in any of the reduced power modes. It runs on a 32.768 kHz clock source, allowing a count period of more than 4 years.

7.1.10 CRC engine

The cyclic redundancy check (CRC) generator with programmable polynomial settings supports several CRC standards that are commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.1.10.1 Features

- Supports three common polynomials: CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: x16 + x12 + x5 + 1
  - CRC-16: x16 + x15 + x2 + 1
  - CRC-32: x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8-bit, 16-bit, or 32-bit.
  - 8-bit write: 1-cycle operation
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle)
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle)

7.1.11 Emulation and debugging

Debug and trace functions are integrated into the Arm Cortex-M33. Serial wire debug and trace function (serial wire output) are supported. Eight breakpoints and four watch points are supported. In addition, a JTAG boundary scan mode is provided.

The Arm SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins PIO0_11 and PIO0_12 assume the SWD functions by default (SWCLK and SWDIO).

7.1.12 Security features

- Arm TrustZone-M® enabled.
- AES-256 encryption/decryption engine with keys fed directly from PUF or a software-supplied key.
- Secure hash algorithm (SHA2) module supports secure boot with a dedicated DMA controller.
- Physical unclonable function (PUF) using dedicated SRAM for silicon fingerprint. PUF can generate, store, and reconstruct key sizes from 64 bits to 4096 bits. Includes hardware for key extraction.
- True random number generator (TRNG) compliant to NIST SP 800-90B, NIST SP 800-22.
- 128-bit unique device serial number for identification (UUID).
- Secure GPIO.
- Public key coprocessor is provided to enable hardware acceleration for various functions required for certain asymmetric cryptographic algorithms, such as elliptic curve cryptography (ECC).
- PRINCE module for real-time encryption of data written to on-chip flash and decryption of encrypted flash data during read to allow asset protection, such as securing application code and enabling secure flash update.
- Hash-based message authentication code (HMAC) using SHA2.
- Cipher-based message authentication code (CMAC) using AES.

- Protected flash region (PFR) is available to configure secure boot, debug authentication, read UUID, store PUF in a key store area, and user-defined fields available for specific data storage.

7.2 Radio subsystem

The Bluetooth Low Energy link layer is compatible with the Bluetooth Low Energy 5.3 specification:

- Bluetooth Low Energy 5.3 controller subsystem (QDID 200592)
- Bluetooth Low Energy 5.3 host subsystem (QDID 226395)
- Includes a 48-bit unique bluetooth device address

The MCX W23 supports the following features:

- Device privacy and network privacy modes (Version 5.0)
- Advertising extension PDUs (Version 5.0)
- Anonymous device address type (Version 5.0)
- Up to 2 Mbps data rate (Version 5.0)
- Long range (Version 5.0)
- High-duty cycle, non-connectable advertising (Version 5.0)
- Channel selection algorithm #2 (Version 5.0)
- High output power (Version 5.0)
- Advertising Channel Index (Version 5.1)
- Periodic Advertising Sync Transfer (PAST) (Version 5.1)
- Supports LE power control feature (Version 5.2)

All roles specified by the Bluetooth specification are supported:

- Broadcaster
- Observer
- Peripheral
- Central

Further supported functionality:

- Up to 4 simultaneous connections in any role.
- Device filtering through the programmable size of the accept lists.

The Bluetooth Low Energy link layer supports the following operation modes:

- Functional mode, Bluetooth Low Energy link layer controlled through logical HCI commands from the Bluetooth Low Energy host stack.
- 'Black box' operation mode controlled over the UART HCI, which can be used for Bluetooth Low Energy qualification.
  - Includes direct test mode configurable through the UART HCI.
  - Additional API functions are included to enable:
    - Transmitting in continuous wave mode
    - RSSI measurements
  - This mode can only run in active power mode and sleep power mode (low-power modes are not supported).

The MCX W23 comes with an integrated Bluetooth Low Energy host stack library, compatible with Bluetooth Low Energy version 5.3.

7.2.1 Transceiver

The RF radio transceiver implements the complete physical layer of a 2.4 GHz ultralow power RF wireless link. It includes:

- RF functionality including its own optimized power management and timing management.
- Integrated analog RF front-end including matching network and Rx/Tx switch.
- Symbol demodulation and timing/frequency recovery blocks.
- Gaussian frequency shift keying (GFSK) with variable modulation modes:
  - Bluetooth Low Energy 2 Mbps mode
  - Bluetooth Low Energy 1 Mbps mode
  - Bluetooth Low Energy 500 kbps mode
  - Bluetooth Low Energy 125 kbps mode
- Accurate received signal strength indicator (RSSI)
- Integrated frequency synthesizer
- Automatic gain control
- Flexible RF transmitter level configurability:
  - TX Mode 1 (TXM1): Range from −31 dBm to +2 dBm when VDD_RF exceeds 1.1 V
  - TX Mode 2 (TXM2): Range from −28 dBm to +6 dBm when VDD_RF exceeds 1.7 V
- Trimming and calibration during chip production removing the necessity for trimming in the application to achieve Bluetooth Low Energy compliance.
- Continuous wave transmit for test mode.

7.2.2 Radio controller

The radio controller enables:

- Radio controller supports the link-layer coprocessor.
- Support of ACL links with support for multimaster and multislave connections.
  - Up to 4 channels with a mix of master ACL connections, slave ACL connections, advertisement and/or scanning channels.

7.2.3 Radio crystal oscillator

To generate a clock for the MCX W23, an external 32 MHz crystal must be connected to the crystal oscillator pins (XIN_32M, XOUT_32M).

The crystal oscillator is not enabled until the Cortex boots up. The control of the crystal remains under control of the firmware.

7.3 Power management subsystem

This section describes the power management and clocking options of the MCX W23.

7.3.1 General power management

Figure 6 shows the different states in of the MCX W23 which can be used to optimize the power consumption.

The MCX W23 has the following supply mode configurations:

- High-voltage supply mode (HV_SM) for MCX W23xB only.
  The device is supplied from a 3 V coincell on the VBAT_HV pin. The DC-DC converter is in buck mode.
- External regulated supply mode (XR_SM) for MCX W23xB only.
  An external PMIC supplies the VBAT_LV and the VBAT_HV pins. The DC-DC converter is disabled.

For more information, see Section 7.3.2.

In active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are five special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, power-down mode, deep power-down mode, and power-off mode. The API functions to configure the different power modes are documented in the MCX W23 user manual.

The in-system programming (ISP) state enables the programming of the on-chip flash. Section 7.1.4.3 describes the supported interface in ISP mode. After a reset, the chip can be forced in this mode with the ISP pin. If no image or an invalid image is detected in the on-chip flash, the chip enters the ISP mode automatically. The DEFAULT_ISP_MODE can be configured in the PFR region of the flash.

The chip can be reset by asserting the RESET_N pin. The external application can keep the RESET_N low for an extended time. Only when the RESET_N goes high, the MCX W23 starts its power-up sequence.

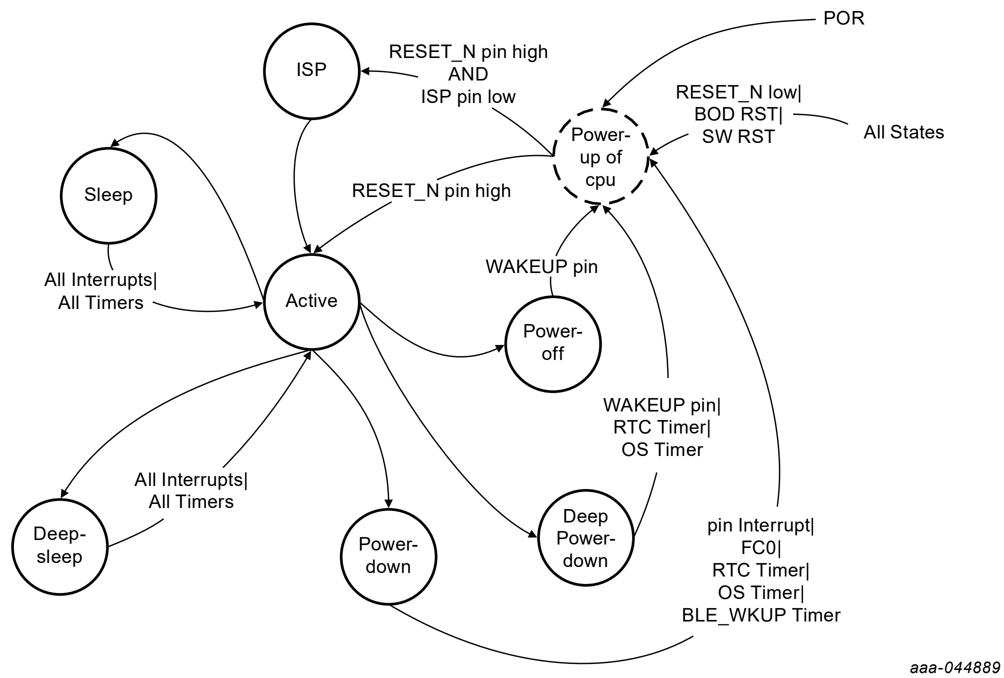

Figure 6. MCX W23 state diagram

Table 3 provides an overview of the different MCX W23 subsystems and functions during the different power modes.

Table 3. Operating states of the MCX W23 subsystems and functions for the different power modes

MCX W23 power modes	pin WAKEUP[1]	RTC timer/ OS timer	BOD1/ BOD2	DC-DC[2]	RAM[3]	System domain[4]/ Low Energy wake-up timer	Core domain[5] Other timers[6]	Radio subsystem[7]
power-off	on	off	off	**off**/bypass	off	off	off	off
deep power-down	on	off/XO_32k/ FRO_32k	on/off	**off**/bypass/on	off	off	off	off
power-down	GPIO	off/XO_32k/ FRO_32k	on/off	**off**/bypass/on	ret/off	on	off	off
deep-sleep	GPIO	off/XO_32k/ FRO_32k	on/off	**off**/bypass/on	ret/off	on	ret	ret/off
sleep	GPIO	off/XO_32k/ FRO_32k	on/off	off/bypass/**on**	on/off	on	WFI	on/ret/off
active	GPIO	off/XO_32k/ FRO_32k	on/off	off/bypass/**on**	on/off	on	on	on/ret/off

[1] WAKEUP pin functionality depends on the power mode:
- On: The WAKEUP pin is used to trigger activation to go to active mode.
- GPIO: The application can configure the WAKEUP pin as a generic GPIO pin.

[2] The DC-DC converter can be put in on mode, bypass mode, or off mode. The **bold** value is the default state used in the corresponding power mode. Bypass mode is only applicable in HV_SM on MCX W23xB.

[3] To optimize power consumption, a configurable number of RAM instances can be turned off. For the deep sleep and the power-down modes, the RAM instance in on-mode is automatically configured in retention mode.

[4] The system domain is part of the digital logic, which manages the wake-up sequences of the power modes.

[5] The core domain is part of the digital logic where the Arm controller is running. Depending on the selected power mode, the Arm can be active, WFI, retention, or off-mode.
- On: Active mode (powered and clocked)
- WFI: Wait for interrupt (powered, clock gated, waiting for activation)
- Ret: Retention mode (powered but not clocked)
- Off: subsystem not powered

[6] The other timers are active in the sleep and deep-sleep modes. These timers are:
- CTimers
- WWDT
- MRT
- SCTimer
- UTICK

[7] The core domain is part of the digital logic where the Arm controller is running. Depending on the selected power mode, the Arm can be active, WFI, retention, or off mode.
- On: Active mode (powered and clocked)
- Ret: Retention mode (powered but not clocked)
- Off: subsystem not powered

For short radio intervals, the MCX W23 enters the deep-sleep mode. The Bluetooth Low Energy wake-up timer manages protocol timing during Deep-sleep. The state is retained in the radio subsystem for a fast wake-up.

For long radio intervals, the MCX W23 enters the power-down mode. The Bluetooth Low Energy wake-up timer manages the protocol timing during the power-down mode. Before entering the power-down mode, the state of the radio subsystem must be stored to RAM. After wake-up, the state of the radio subsystem must be reinitialized.

The Bluetooth Low Energy radio can be configured to three modes with a different maximum transmit level.

For more information on the radio supply options, see Section 7.3.3.

7.3.1.1 Active mode

In active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption.

7.3.1.2 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until a reset or an interrupt occurs. Peripheral functions (like the radio subsystem), if selected to be clocked, can continue operation during sleep mode. They may generate interrupts that cause the processor to resume execution. Sleep mode eliminates the dynamic power the processor itself, the memory systems and related controllers, the internal buses, and the unused peripherals use.

7.3.1.3 Deep-sleep mode

In deep-sleep mode, the flash is powered down. The system clock to the CPU is stopped and, if not configured, the peripherals receive no clocks. Through the power profiles API, selected peripherals, such as Flexcomm interfaces 0 to 2 (SPI, I2C, USART), microtick, WWDT, RTC, OS timer, standard timers, Bluetooth Low Energy sleep timer, and BOD, can be left running in deep-sleep mode. Clock sources, such as FRO 32 MHz, FRO 1 MHz, FRO 32 kHz, the 32.768 kHz RTC clock, and the external oscillator, can be enabled or disabled via software.

The MCX W23 can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block and group interrupt block, OS timer, standard timers, microtick, RTC alarm, a watchdog timer interrupt/reset, BOD interrupt/reset, SPI, I^2C, USART, Bluetooth Low Energy sleep timer, and PLU.

In deep-sleep mode, all SRAM, logic state, and registers maintain their internal states. All SRAM instances that are active enter the retention state, other SRAM instances (not enabled in active) remain switched off. Deep-sleep mode allows for very low quiescent power and fast wake-up options.

7.3.1.4 Power-down mode

In power-down mode, nearly all on-chip power consumption is turned off by shutting down the internal DC-DC converter. The flash is powered down. The system clock to the CPU is stopped and, if not configured, the peripherals receive no clocks. Through the power profiles API, selected peripherals, such as Flexcomm interface 0 (SPI, I2C, USART), RTC, Bluetooth Low Energy sleep timer, and OS timer, can be left running in power-down mode. Clock sources, such as FRO 32 kHz and the 32.768 kHz RTC clock, can be enabled or disabled via software.

The MCX W23 can wake up from power-down mode via a reset, digital pins selected as inputs to the group interrupt block, the OS timer, the RTC alarm, and an interrupt from the Flexcomm interface 0 (SPI, I2C, USART).

In power-down mode, the CPU processor is power-gated and looses internal states. All SRAM instances that are active enter the retention state, other SRAM instances (not enabled in active) remain switched off.

A special mode (power-down mode with CPU retention) is supported where the CPU state is stored in RAM and automatically restored upon wake-up. It allows a fast CPU restart without the need to go through the complete boot process.

7.3.1.5 Deep-power-down mode

In deep-power-down mode, power is shut off to the entire chip except for the power management subsystem (which includes the RTC, the RESET_N pin, the WAKEUP pin, and the OS timer, if enabled. Clock sources such as LF 32 kHz and the 32.768 kHz RTC clock can be enabled or disabled via software.

The MCX W23 can wake up from deep-power-down mode via the RESET_N pin, the RTC alarm, the special wake-up pin, or by using the timeout of the OS timer. The ALARM1HZ flag in the RTC control register generates an RTC wake-up interrupt request, which can wake up the part. SRAM instances are power-gated and losing internal states.

In deep-power-down mode, all functional pins are in tri-state.

When the MCX W23 is used in the HV_SM mode, the supply voltage on the VBAT_HV pin must be 2.5 V or higher to be able to exit Deep-power-down mode.

7.3.1.6 Power-off mode

In power-off mode, power is shut off to the entire chip except for the RESET_N pin and the WAKEUP pin. No clock sources are active on-chip.

The MCX W23 can wake up from power-off mode via the RESET_N pin or the special WAKEUP pin. SRAM instances are power-gated and losing internal states.

The external application can keep the RESET_N low for an extended time. Only when the RESET_N goes high, the MCX W23 starts its power-up sequence.

In power-off mode, all functional pins are in tri-state.

When the MCX W23 is used in the HV_SM mode, the supply voltage on the VBAT_HV pin must be 2.5 V or higher to be able to exit Power-off mode.

7.3.2 Supply mode configurations

The MCX W23 family has the following supply mode configurations:

- High-voltage supply mode (HV_SM):
  The device receives a supply on pin VBAT_HV (V_{BAT_LV} is not supplied). For example, a dual silver-oxide or Li coincell.
- External regulated supply mode (XR_SM):
  An external PMIC supplies pin VBAT_LV and pin VBAT_HV. For example, an external PMIC supplies 1.2 V on VBAT_LV and 1.8 V on VBAT_HV.

To configure for these supply modes, different PCB level interconnects are required.

- In HV_SM and XR_SM configurations, the MCX W23xB is used

Figure 7 shows the HV_SM configuration.

In HV_SM, the battery supply is connected to the VBAT_HV pin. The integrated PMU detects this supply and configures the DC-DC converter in buck mode. To power up correctly and have the internal DC-DC to start automatically in buck mode, a minimum supply voltage of 2.5 V is required. The DC-DC converter generates the 1.2 V supply to the VBAT_LV pin, which is decoupled with an external output capacitor.

External sensors and/or actuators can be connected directly to the battery supply.

In this example, the supply of the IO (VDD_IO) is connected to the VBAT_HV pin. So, the MCX W23 can interface to the connected sensors and/or actuators.

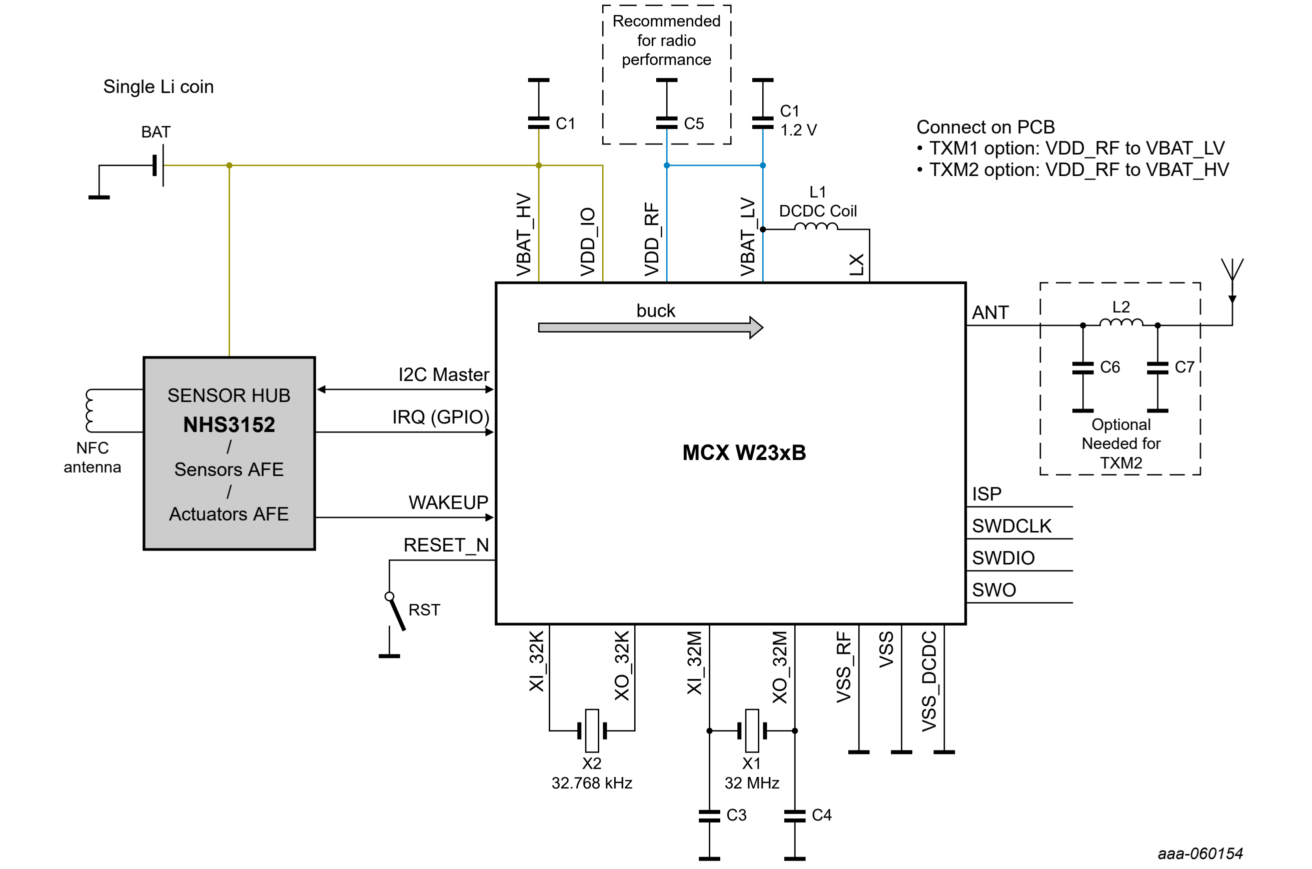

Figure 7. High-voltage supply mode (HV_SM) - MCX W23xB

Figure 8 shows the MCX W23 with a PMIC with charging capabilities. The integrated DC-DC converter of the MCX W23 is not used. The external inductor is not required.

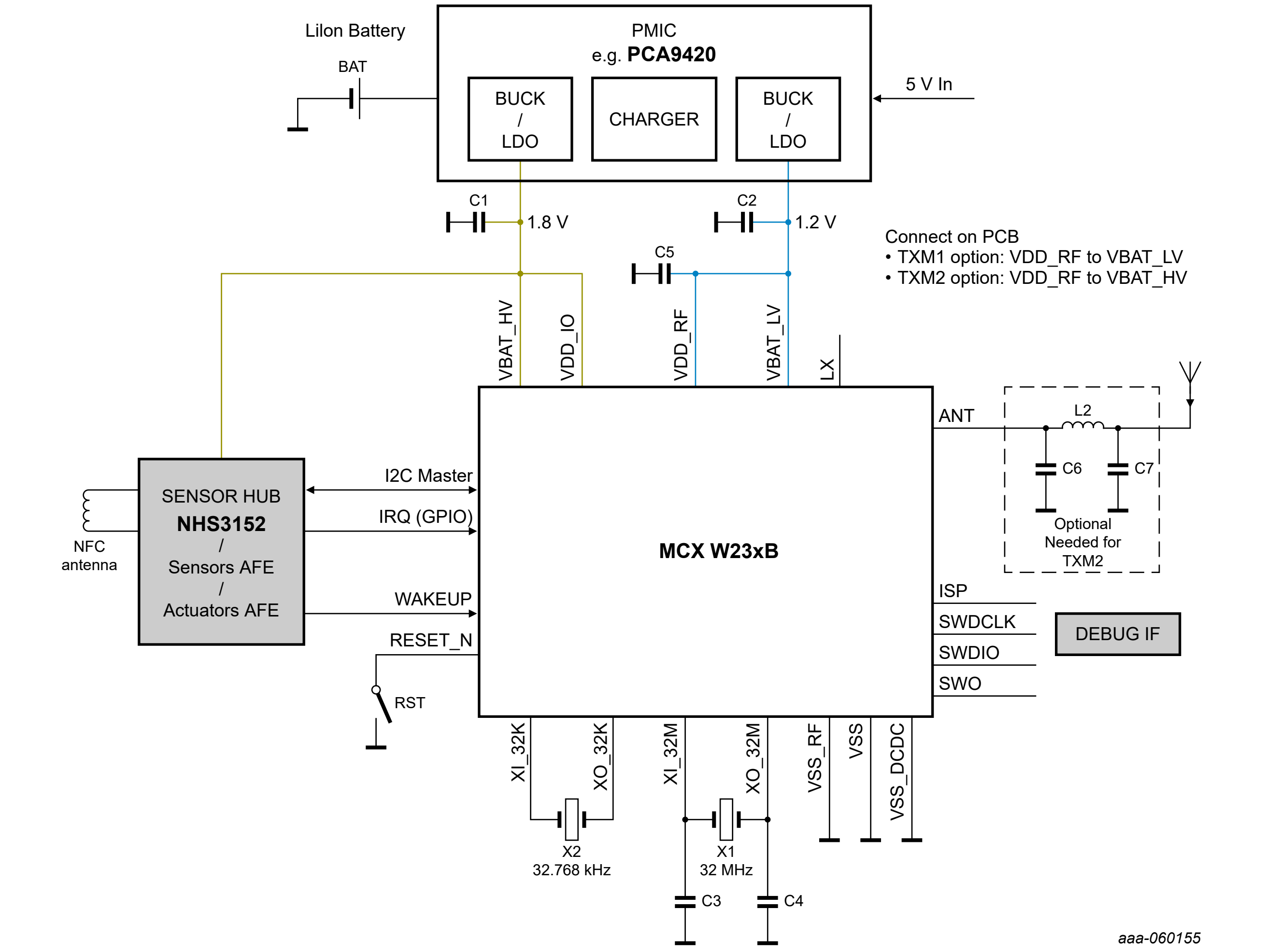

Figure 8. PMIC-based external regulated supply mode (XR_SM) - MCX W23xB

7.3.3 Radio supply configurations

The Bluetooth Low Energy radio can be configured to two modes with a different maximum transmit level:

- TX mode 1 (TXM1): Range from −31 dBm to +2 dBm when V_{DD_RF} exceeds 1.1 V
- TX mode 2 (TXM2): Range from −28 dBm to +6 dBm when V_{DD_RF} exceeds 1.7 V

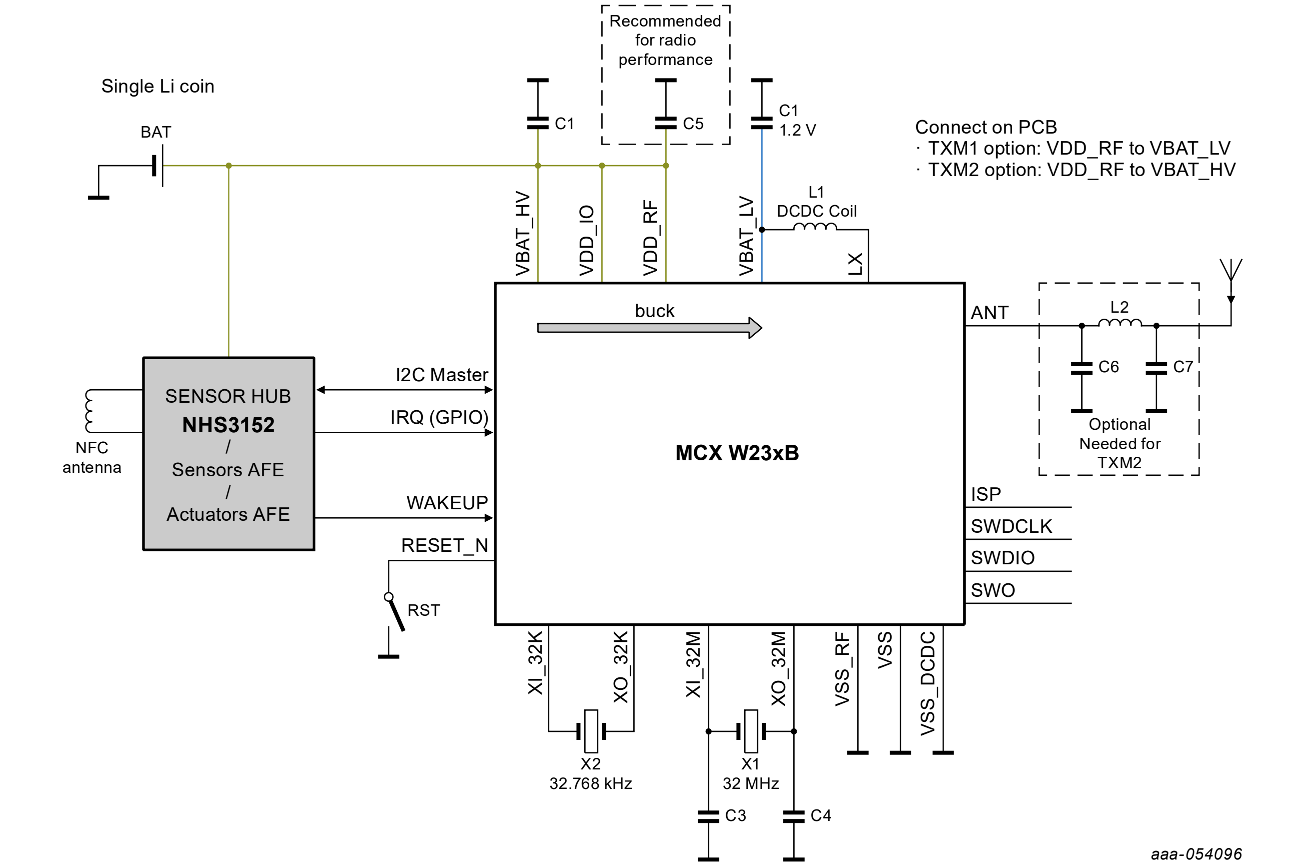

Figure 9. MCX W23xB Application diagram HV_SM in TXM2 mode

7.3.4 Clock sources

The MCX W23 supports 2 external and 3 internal clock sources:

- FRO_192M: Internal high-frequency free-running oscillator.
  This oscillator provides a set of selectable outputs:
  – A 32 MHz output provides the highest clock speed for the system clock. Shortly after the supply pins reach operating voltage, it provides the default clock at reset. The FRO_32M clock is trimmed to ± 3 % accuracy over the entire voltage and temperature range.
  – A 12 MHz output, which can be selected to run the system at lower clock speeds (consuming less power). It can be set to the default clock at start-up by programming the BOOT_SPEED field in the CMPA register.
  – A 24 MHz output, which can be selected to run the system or to be used by specific peripherals
  – A 48 MHz and a 64 MHz output provide the clock for the SPIFI interface.
- FRO_32k:
  32.768 kHz internal free-running oscillator. The FRO_32k clock is trimmed to ± 2 % accuracy over the entire voltage and temperature range.
- FRO_1M:
  Internal low-power oscillator of 1 MHz. The FRO_1M clock is trimmed to ± 15 % accuracy over the entire voltage and temperature range.
- XO_32M:
  Crystal oscillator with an operating frequency of 32 MHz (XO_32M).
- XO_32k:
  Crystal oscillator with 32.768 kHz operating frequency (XO_32k).

All FRO sources can be runtime calibrated against the XO_32M.

7.3.5 Clock generation

The system control block facilitates the clock generation. Many clocking variations are possible. Figure 10 gives an overview of potential clock options. Table 4 describes the signals on the clocking diagram. The maximum clock frequency for the Arm and system bus is 32 MHz.

Note: *The indicated clock multiplexers shown in Figure 10 are synchronized.*

To operate, the currently selected clock must be running and the clock to be switched to must also be running. The clock must be running so that the multiplexer can gracefully switch between the two clocks without glitches. Other clock multiplexers are not synchronized. If a glitch-free output is required, the output divider can be stopped and restarted gracefully during switching.

Table 4. Signals on the clocking diagram

Clock names	Description
xtal32k	32.768 kHz crystal oscillator (XO_32k) output clock
fro32k	32.768 kHz FRO (FRO_32k) output clock
32k_osc	The 32.768 kHz output of the RTC clock selector (xtal32k or fro32k). The clock must be enabled in the RTCOSCCTRL register.
clk_in	The internal clock that comes from the main 32 MHz crystal oscillator (XO_32M).
fro_1m	The output clock of the low-power oscillator (FRO_1M)
fro_12m	12 MHz divided down from the high-speed FRO clock
fro_24m	24 MHz divided down from the high-speed FRO clock
fro_32m	32 MHz divided down from the high-speed FRO clock
fro_32m_div	The output clock of the high-speed FRO divider

Table 4. Signals on the clocking diagram...*continued*

Clock names	Description
main_clk	The clock that the CPU and AHB (optionally divided), and potentially many others, use. The main clock and its source selection are shown in the diagram.
main_clk_div	The output clock of the main_clk divider
none	A tied-off source that must be selected to save power when the output of the related multiplexer is not used

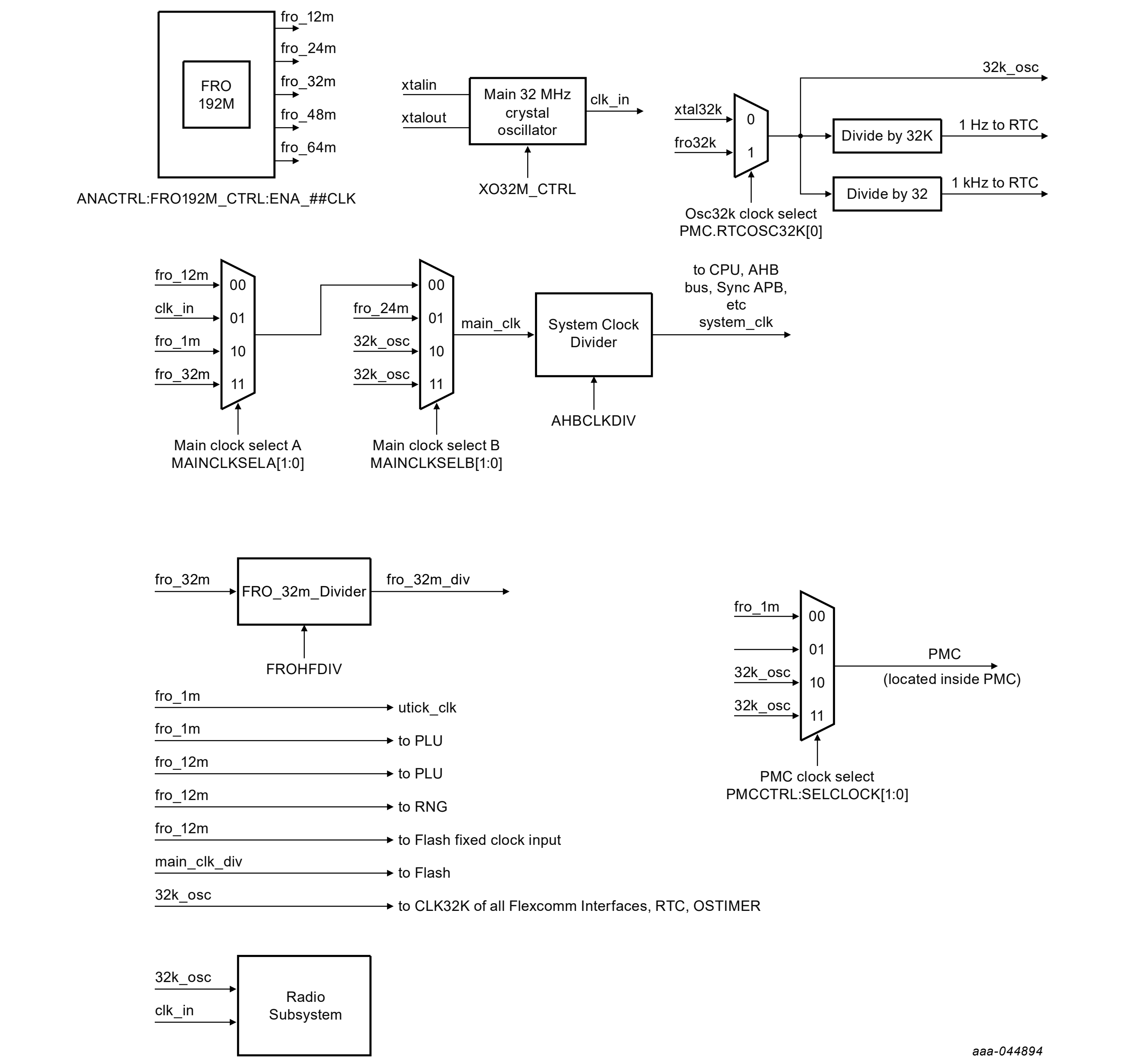

Figure 10. Clock Generation: Part 1

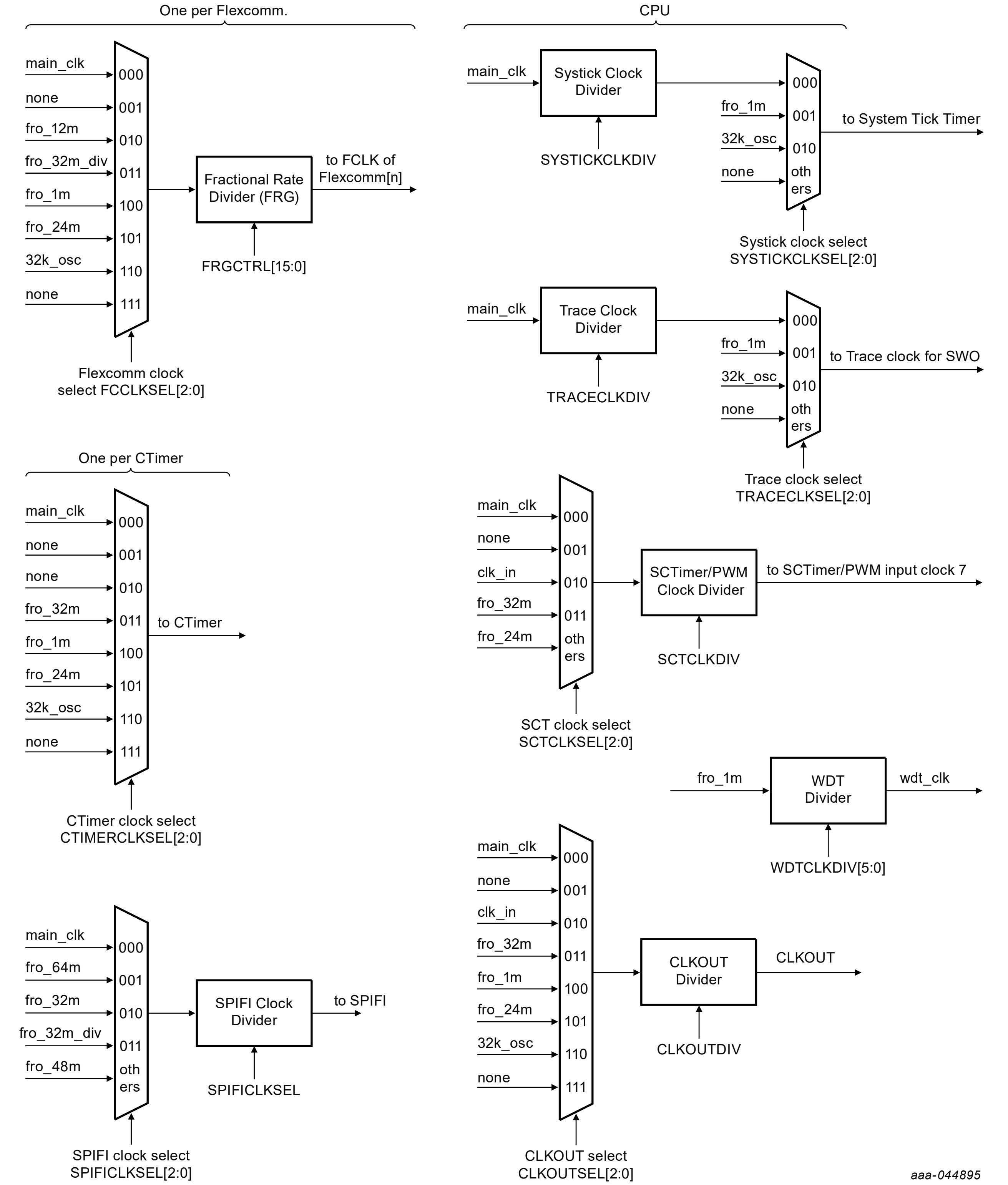

Figure 11. Clock Generation: Part 2

7.3.6 Power-on reset (POR)

The MCX W23 contains a POR circuit:

- On the MCX W23xB, the POR monitors V_{BAT_HV}.

After initial power-up, the POR circuit is disabled to save power. If the application must be protected against supply voltage dips, it must enable one of the brownout detection modules with reset generation on. When the supply voltage drops below the programmed BOD threshold level, it allows the reset of the device.

7.3.7 Brownout detection (BOD)

The MCX W23 includes two BOD detectors. The BOD detectors monitor the voltage level on the selected supply pin.

If this voltage drops to below a configurable threshold level, the BOD sets a flag that can be polled or causes an interrupt. The BOD configure API can be used to configure the threshold level.

The BOD can also be configured to reset the device over the configuration API.

8 Limiting values

Table 5. Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(VBAT\_LV)}$	supply voltage on VBAT_LV pin		−0.3	+3.6	V
$V_{DD(VBAT\_HV)}$	supply voltage on VBAT_HV pin		−0.3	+3.6	V
$V_{DD(VDD\_RF)}$	supply voltage on VDD_RF pin		−0.3	+3.6	V
$V_{DD(VDD\_IO)}$	supply voltage on VDD_IO pin		−0.3	+3.6	V
$P_{i(RF)}$	RF input power		-	10	dBm
P_{tot}	total power consumption		-	1	W
T_j	junction temperature		−40	125	°C
T_{stg}	storage temperature		−55	150	°C
RH	relative humidity	[1]	-	95	%
V_{ESD}	electrostatic discharge voltage	HBM; all pins [2]	-	2000[3]	V
		CDM; all pins, HVQFN40 package [4]	-	500[5]	V
		CDM; all pins, WLCSP37 package [4]	-	350[6]	V

[1] MSL – moisture sensitivity level – JEDEC J-STD-20D – max level 3 (168 hrs floor life at ≤ 30 °C/60 % relative humidity).
[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor (human body model) compliant with the JS-001-2014 norm.
[3] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
[4] Charge device model. Compliant with the JESD22-C101F norm.
[5] Classification Level C2a according to ANSI/ESDA/JEDEC JS-002-2022
[6] Classification Level C1 according to ANSI/ESDA/JEDEC JS-002-2022

9 Characteristics

Unless otherwise specified:

- Typical values are informative only. Characterized through bench measurements using typical samples and recommended components as defined in "Hardware Design Considerations for MCX W23 application note.
  - 1.8 V at V_{BAT_LV} and 1.8 V at V_{BAT_HV} for XR_SM on MCX W23xB.
  - 3.0 V at V_{BAT_HV} for HV_SM on MCX W23xB. Default buck mode is enabled.
- Min/Max values are valid over the operating temperature and the voltage range as specified in Table 6.

9.1 General operating conditions

Table 6. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	Ambient temperature		−40	+25	+85	°C
f_{clk}	clock frequency	internal CPU/system clock	-	-	32	MHz
$V_{BAT(lv)}$	low-voltage battery supply voltage	pin VBAT_LV in XR_SM mode	1.1	1.2	$V_{BAT(hv)}$	V
$V_{BAT(hv)}$	high-voltage battery supply voltage	pin VBAT_HV in HV_SM mode [1] [2]	1.7	3.0	3.3	V
		pin VBAT_HV in XR_SM mode. Only used for internal flash access. [2]	1.7	1.8	3.3	V
$V_{DD(N)ext(p-p)}$	peak-to-peak external noise supply voltage	on VBAT_LV pin up to 100 kHz; VDD_RF pin connected to VBAT_LV pin at nominal supply 1.2 V [3] [4]	-	-	50	mVpp
		on VBAT_HV pin up to 100 kHz; VDD_RF pin connected to VBAT_HV pin at nominal supply 3.0 V [3] [4]	-	-	50	mVpp
$V_{DD(IO)}$	input/output supply voltage	IO domain supply voltage on pin VDD_IO	1.1	1.5	3.3	V
$V_{DD(RF)}$	RF analog supply voltage	radio voltage supply (on VDD_RF pin) in TXM1: TX up to +2 dBm	1.1	-	3.3	V
		radio voltage supply (on VDD_RF pin) in TXM2: TX up to +6 dBm	1.7	-	3.3	V
$V_{i(XI\_32M)}$	input voltage on pin XI_32M	voltage amplitude on XI_32M pin when connected to a crystal; Any input common mode is acceptable as there is an AC coupling capacitor inside.	200	-	-	mVp
$V_{i(XI\_32K)}$	input voltage on pin XI_32K	voltage amplitude on XI_32K pin when connected to a crystal	200	-	350	mVpp
		voltage on XI_32K pin with cap_osc_in set to 0	0	-	500	mV

Table 6. General operating conditions...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{r(VBAT\_HV)}$	rise time of VBAT_HV supply	Ramp on VBAT_HV pin from 0V to $V_{BAT(hv)}$	0.1	-	10 x $V_{BAT(hv)}$	ms
$t_{r(VBAT\_LV)}$	rise time of VBAT_LV supply	Ramp on VBAT_LV pin from 0V to $V_{BAT(lv)}$in XR_SM mode	0.1	-	10 x $V_{BAT(lv)}$	ms

[1] Power-up in HV_SM mode requires a minimum supply voltage of 2.5 V to allow internal DC-DC to start up in buck mode.
[2] When powering up the silicon, the high-voltage battery supply voltage must be below 250 mV or above 350 mV.
[3] Measured on the chip pins of the RDM module
[4] 100 kHz is the maximum frequency that the ripple measurement setup used during silicon validation supports.

9.2 CoreMark data

Table 7. CoreMark score

Parameter	Conditions	Typ [1]	Unit
CoreMark score; SRAM	CoreMark coded executed from SRAM; main_clk_div = 32 MHz	3.75	(Iterations/s)/MHz
CoreMark score; internal flash	CoreMark coded executed from internal flash; main_clk_div = 32 MHz	3.66	(Iterations/s)/MHz
CoreMark score; external QSPI flash	CoreMark coded executed from external flash; main_clk_div = 32 MHz; QSPI at 64 MHz	1.47	(Iterations/s)/MHz

[1] Compiler settings: Keil µVision v.5.36; optimization level 3; optimized for time ON.

9.3 Power consumption controller subsystem

Power measurements in active, sleep, and deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the SWM block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.
- XTAL disabled.
- Radio subsystem initialized and in sleep

9.3.1 Power consumption in active and sleep modes

The current is measured on the different supply pins. Current consumption on VDD_RF pin is not included. VDD_RF current consumption is reported separately in Section 11

- For MCX W23xB in XR_SM mode, it is measured on VBAT_HV, VBAT_LV and VDD_IO pins. All pins are supplied with 1.8 V. The sum of the currents is provided in the table.
- For MCX W23xB in HV_SM mode, it is measured on VBAT_HV and VDD_IO pin. VBAT_HV and VDD_IO pins are supplied with 3.0 V. The output of the DC-DC is set to 1.2 V. The sum of the currents is provided in the table.

Table 8. Static characteristics: Power consumption in active and sleep mode for XR_SM (MCX W23xB only)

T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	CoreMark code executed from SRAMX				
		CCLK = 12 MHz [1][2][3][4]	-	0.961	-	mA
		CCLK = 32 MHz [1][2][3][4]	-	2.03	-	mA
		CoreMark code executed from flash				
		CCLK = 12 MHz [1][2][3][5]	-	1.23	-	mA
		CCLK = 32 MHz [1][2][3][5]	-	2.75	-	mA
		CPU in sleep mode with CCLK = 12 MHz	-	0.49	-	mA
		CPU in sleep mode with CCLK = 32 MHz	-	0.84	-	mA

[1] Clock source FRO.
[2] Characterized through bench measurements using typical samples.
[3] Compiler settings: Keil µVision v.5.36; optimization level 3; optimized for time ON.
[4] Flash is powered down.
[5] See the FLASHCFG register in the MCX W23 user manual for system clock flash access time settings.

Table 9. Static characteristics: Power consumption in active and sleep mode for HV_SM (MCX W23xB only)

T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	CoreMark code executed from SRAMX				
		CCLK = 12 MHz [1] [2] [3] [4]	-	0.51	-	mA
		CCLK = 32 MHz [1] [2] [3] [4]	-	1.05	-	mA
		CoreMark code executed from flash				
		CCLK = 12 MHz [1] [2] [3] [5]	-	0.65	-	mA
		CCLK = 32 MHz [1] [2] [3] [5]	-	1.42	-	mA
		CPU in sleep mode with CCLK = 12 MHz	-	0.28	-	mA
		CPU in sleep mode with CCLK = 32 MHz	-	0.46	-	mA

[1] Clock source FRO.
[2] Characterized through bench measurements using typical samples.
[3] Compiler settings: Keil µVision v.5.36; optimization level 3; optimized for time ON.
[4] Flash is powered down.
[5] See the FLASHCFG register in the MCX W23 user manual for system clock flash access time settings.

9.3.2 Power consumption in deep-sleep, power-down, deep power-down, and power-off modes

The current is measured on the different supply pins. Current consumption on VDD_RF pin is not included. VDD_RF current consumption is reported separately in Section 11

- For MCX W23xB in XR_SM mode, it is measured on VBAT_HV, VBAT_LV and VDD_IO pins. All pins are supplied with 1.8 V. The sum of the currents is provided in the table.
- For MCX W23xB in HV_SM mode, it is measured on VBAT_HV and VDD_IO pin. VBAT_HV and VDD_IO pins are supplied with 3.0 V. The output of the DC-DC is set to 1.2 V. The sum of the currents is provided in the table.

Table 10. Static characteristics: Power consumption in deep-sleep, power-down, deep power-down, and power-off modes for XR_SM (MCX W23xB only)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Deep-Sleep mode with FRO_32K and RTC timer running. External regulated supply mode (1.8 V)						
I_{DD}	supply current	SRAM0 (16 KB) powered; T_{amb} = 25 °C	-	3.84	-	µA
		SRAM0 (16 KB) powered; T_{amb} = 85 °C	-	35.65	-	µA
		full RAM powered; T_{amb} = 25 °C	-	4.50	5.30	µA
		full RAM powered; T_{amb} = 85 °C	-	45.10	-	µA
Power-down with FRO_32K and RTC timer running. External regulated supply mode (1.8 V)						
I_{DD}	supply current	SRAM0 (16 KB) powered; T_{amb} = 25 °C	-	1180	1900	nA
		SRAM0 (16 KB) powered; T_{amb} = 85 °C	-	7860	-	nA
Deep power-down with 32.768 kHz clock and RTC timer running. External regulated supply mode (1.8 V)						
I_{DD}	supply current	WAKEUP pin active; RTC with XO_32k active; T_{amb} = 25 °C	-	695	1250	nA
		WAKEUP pin active; RTC with XO_32k active; T_{amb} = 85 °C	-	2560	-	nA
		WAKEUP pin active; RTC with FRO_32k active; T_{amb} = 25 °C	-	650	1200	nA
		WAKEUP pin active; RTC with FRO_32k active; T_{amb} = 85 °C	-	2510	-	nA
Power-off with WAKEUP pin. External regulated supply mode (1.8 V)						
I_{DD}	supply current	WAKEUP pin active;	-	80	185	nA

Table 10. Static characteristics: Power consumption in deep-sleep, power-down, deep power-down, and power-off modes for XR_SM (MCX W23xB only)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		T_{amb} = 25 °C				
		WAKEUP pin active; T_{amb} = 85 °C	-	1000	-	nA

Table 11. Static characteristics: Power consumption in deep-sleep, power-down, and deep power-down and power-off modes for HV_SM (MCX W23xB only)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Deep-Sleep mode with FRO_32K and RTC timer running. High-voltage battery supply mode (3.0 V)						
I_{DD}	supply current	SRAM0 (16 KB) powered; T_{amb} = 25 °C	-	4.01	-	μA
		SRAM0 (16 KB) powered; T_{amb} = 85 °C	-	33.06	-	μA
		full RAM powered; T_{amb} = 25 °C	-	4.61	5.30	μA
		full RAM powered; T_{amb} = 85 °C	-	42.34	-	μA
Power-down with FRO_32K and RTC timer running. High-voltage battery supply mode (3.0 V)						
I_{DD}	supply current	SRAM0 (16 KB) powered; T_{amb} = 25 °C	-	1230	1700	nA
		SRAM0 (16 KB) powered; T_{amb} = 85 °C	-	7740	-	nA
Deep power-down with 32.768 kHz clock and RTC timer running. High-voltage battery supply mode (3.0 V)						
I_{DD}	supply current	WAKEUP pin active; RTC with XO_32k active; T_{amb} = 25 °C	-	690	1200	nA
		WAKEUP pin active; RTC with XO_32k active; T_{amb} = 85 °C	-	3050	-	nA
		WAKEUP pin active; RTC with FRO_32k active; T_{amb} = 25 °C	-	645	1150	nA
		WAKEUP pin active; RTC with FRO_32k active; T_{amb} = 85 °C	-	2960	-	nA
Power-off with WAKEUP pin. High-voltage battery supply mode (3.0 V)						
I_{DD}	supply current	T_{amb} = 25 °C	-	25	50	nA
		T_{amb} = 85 °C	-	745	-	nA

9.3.3 Peripheral power consumption

Table 12 shows the peripheral power consumption measured on a typical sample at T_{amb} = 25 °C. The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using AHB clock control and PDRUNCFG registers. All other blocks are disabled and no code accessing the peripheral is executed.

Table 12. Typical peripheral power consumption

T_{amb} = 25 °C

Peripheral	I_{DD} in XR_SM mode at 1.8 V	I_{DD} in HV_SM mode at 3.0 V	Unit
FRO HF (12 MHz)	58	58	µA
FRO (1 MHz)	1.9	1.85	µA
FRO (32.768 kHz)	0.21	0.23	µA
XTAL OSC (32 MHz)	230	260	µA
XTAL OSC (32.768 kHz)	0.24	0.27	µA
BOD1	0.25	0.50	µA
BOD2	0.25	0.50	µA
SRAM X	16	8	µA
SRAM 0	6	3	µA
SRAM 1	6	3	µA
SRAM 2	8	4	µA

9.4 Power consumption radio subsystem

Table 13 shows the typical radio power consumption measured on a typical sample at T_{amb} = 25 °C.

In HV_SM mode, the current is measured on the VBAT_HV pin with VDD_RF pin connected to the VBAT_LV pin (output of the DC-DC). The output voltage of the DC-DC on the VBAT_LV pin is configured to 1.2 V.

In XR_SM mode, the current reported is the sum of all currents on all supply pins at 1.8 V (VBAT_HV, VBAT_LV, VDD_RF).

The average power consumption during the different phases when advertising is shown in Figure 12 and Figure 13. A more detailed description can be found in the "MCX W23 Power Consumption Analysis" application note
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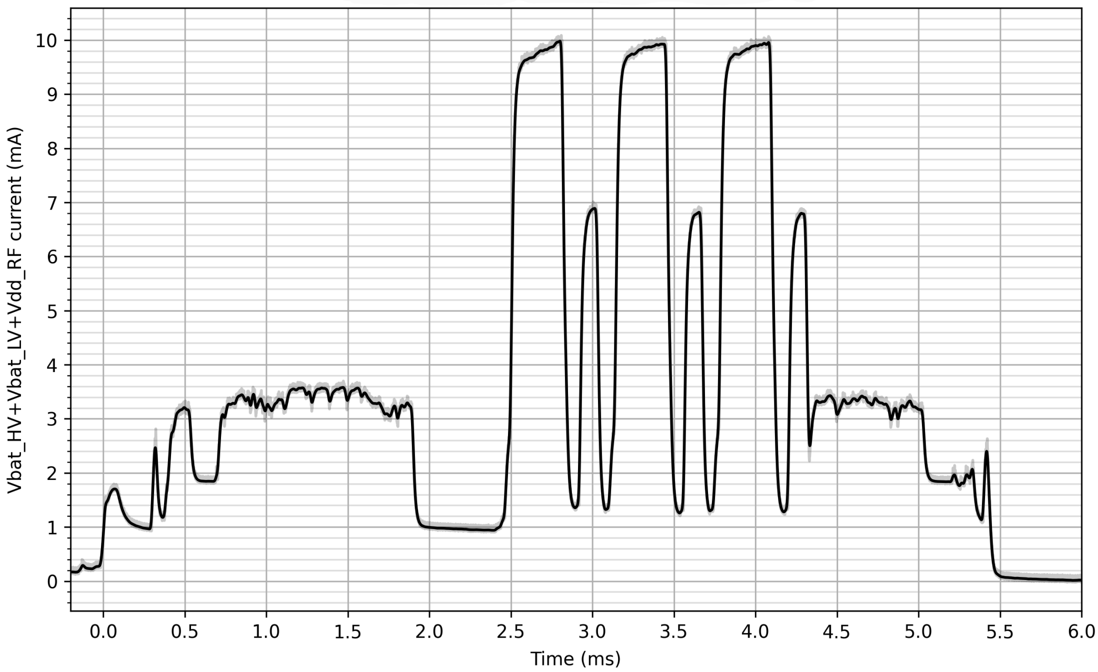


Figure 12. Power consumption during Bluetooth Low Energy advertising during XR_SM mode with VBAT_HV = VBAT_LV = VDD_RF = 1.8V

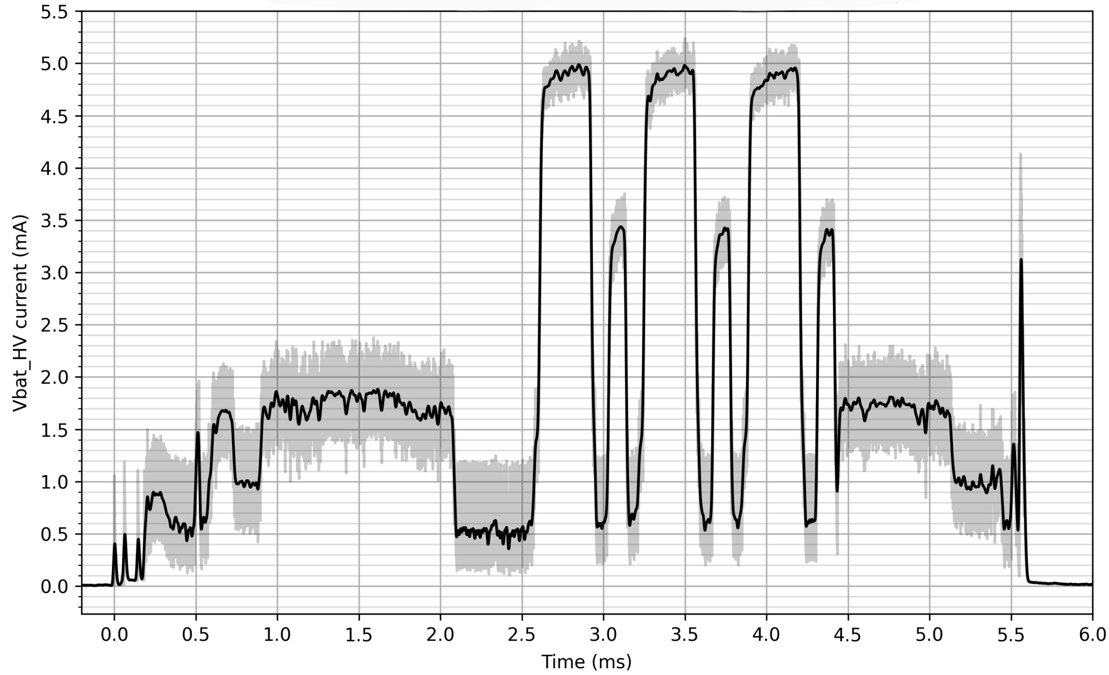


Figure 13. Power consumption during Bluetooth Low Energy advertising during HV_SM mode with VBAT_HV = 3 V, VBAT_LV = 1.2V and VDD_RF = VBAT_LV

Table 13. Static characteristics: Power consumption during Bluetooth Low Energy advertising in XR_SM and HV_SM

Radio mode	Condition	I_{DD} in XR_SM	I_{DD} in HV_SM	Unit
radio RX packet phase		6.64	3.33	mA
radio TX packet phase	TXM1 - 0 dBm output power	9.68	4.83	mA

See Section 11 for more power consumption numbers on the VDD_RF pin of the radio transceiver under different supply levels and radio output power.

9.5 Pin characteristics

Table 14. Static characteristics: pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RESET pin						
Input characteristics						
V_I	input voltage		0	-	V_{DD_IO}	V
V_{IH}	HIGH-level input voltage		0.7	-	V_{DD_IO}	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3	V
Standard I/O pins						
Input characteristics						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	2	200	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD\_IO}$; on-chip pull-down resistor disabled	-	2	200	nA
V_I	input voltage	pin configured to provide a digital function	0	-	V_{DD_IO}	V
V_{IH}	HIGH-level input voltage		0.7 × V_{DD_IO}	-	V_{DD_IO}	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3 × V_{DD_IO}	V
V_{hys}	hysteresis voltage		-	0.4	-	V
Output characteristics						
I_{OH}	Static output high current	At $V_{OH} = V_{DD\_IO}$ - 0.2V; with V_{DD_IO} = 1.2 V	2	-	-	mA
		At $V_{OH} = V_{DD\_IO}$ - 0.2V; with V_{DD_IO} = 1.8 V	7.0	-	-	mA
		At $V_{OH} = V_{DD\_IO}$ - 0.2V; with V_{DD_IO} = 3.3 V	13.6	-	-	mA
I_{OL}	Static output low current	At V_{OL} = 0.2V; with V_{DD_IO} = 1.2 V	2	-	-	mA
		At V_{OL} = 0.4V; with V_{DD_IO} = 1.8 V	7.3	-	-	mA
		At V_{OL} = 0.4V; with V_{DD_IO} = 3.3 V	13.5	-	-	mA
Weak input pull-up/pull-down characteristics						
R_{pd}	pull-down resistance	V_I = 0 V	40	50	62	kΩ
R_{pu}	pull-up resistance	$V_I = V_{DD\_IO}$	40	50	62	kΩ
Pin capacitance						
C_{IO}	input/output capacitance	I^2C-bus pins	-	-	7	pF
		pins with digital functions only	-	-	2.4	pF

Table 15. Dynamic characteristics: I/O pins

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Condition		Min	Typ	Max	Unit
1.8 V < V_{DD} < 3.6 V							
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1	[1] [2]	0.65	-	1.20	ns
		pin configured as output; SLEW = 0	[1] [2]	1.78	-	3.00	ns
t_f	fall time	pin configured as output; SLEW = 1	[1] [2]	0.70	-	1.22	ns
		pin configured as output; SLEW = 0	[1] [2]	1.72	-	3.00	ns
I^2C I/O pins - normal drive strength							
t_r	rise time	pin configured as output; internal pull-up enabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF	[1] [2]	11.0	-	26.0	ns
		pin configured as output; internal pull-up disabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF	[1] [2]	16.5	-	72.0	ns
t_f	fall time	pin configured as output; internal pull-up enabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF	[1] [2]	13.0	-	22.0	ns
		pin configured as output; internal pull-up disabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF	[1] [2]	12.5	-	22.0	ns
1.1 V < V_{DD} < 1.8 V							
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1	[1] [2]	1.8	-	4.3	ns
		pin configured as output; SLEW = 0	[1] [2]	3.8	-	8.2	ns
t_f	fall time	pin configured as output; SLEW = 1	[1] [2]	1.65	-	4.3	ns
		pin configured as output; SLEW = 0	[1] [2]	3.5	-	7.4	ns

Table 15. Dynamic characteristics: I/O pins*...continued*

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I^2C I/O pins - normal drive strength						
t_r	rise time	pin configured as output; internal pull-up enabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF [1] [2]	15	-	59	ns
		pin configured as output; internal pull-up disabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF [1] [2]	16	-	72	ns
t_f	fall time	pin configured as output; internal pull-up enabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF [1] [2]	19	-	44	ns
		pin configured as output; internal pull-up disabled; external resistive pull-up and capacitance from 1.3 kΩ/10 pF to 0.8 kΩ/100 pF [1] [2]	19	-	44	ns

[1] Rise times and fall times measured between 90 % and 10 % of the full input signal level.

[2] The slew rate is configured in the IOCON block of the SLEW bit (see the MCX W23 user manual).

9.6 Flash memory

Table 16. Flash characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	flash size		-	1 M	-	bytes
	flash sector	smallest portion of the flash memory that can be erased in one operation	-	8 k	-	bytes
	flash page	largest portion of the flash memory that can be programmed in one operation	-	128	-	bytes
	flash phrase	smallest portion of the flash memory that can be programmed in one operation	-	16	-	bytes
N_{endu}	endurance	Page erase/program; page in a sector	10 k	-	-	cycles
t_{ret}	retention time	powered/unpowered after up to 10 k cycles at 85 °C	5	-	-	years
$t_{er(sect)}$	sector erase time	1 sector - 8 kB	-	2	4	ms
$t_{er(all)}$	all erase time	full main array - 1 MB	-	-	2800	ms
$t_{prog(phrase)}$	programming time	one phrase (= 16 bytes) from RAM to flash	-	135	375	us
$t_{prog(page)}$	programming time	one page (= 128 bytes) from RAM to flash	-	450	1000	us

Table 17. Flash characteristics: program/erase current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{er(AV)}$	average erase current	current at VBAT_HV pin in HV_SM [1]	-	1685	-	µA
$I_{prog(AV)}$	average program current	current at VBAT_HV pin in HV_SM [1]	-	2265	-	µA
$I_{er(peak)}$	peak erase current	current at VBAT_HV pin in HV_SM [2]	-	1970	-	µA
$I_{prog(peak)}$	peak program current	current at VBAT_HV pin in HV_SM [2]	-	2448	-	µA

[1] Average of full cycle.
[2] Maximum of 10 µs moving average.

9.7 Device reset

Table 18. POR

Symbol	Parameter	Conditions	min	typ	max	unit
$t_{(RESET\_N)}$	RESET_N pulse width		5	-	-	µs

Table 19. Dynamic characteristics: Typical start-up times after reset

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup(por)}$	power-on reset start-up time	triggered by POR [1]	-	17.5	-	ms
$t_{startup}$	start-up time	triggered by a cold reset (RESET_N pin asserted) [1]	-	15	-	ms
		triggered by a warm reset (writing to SWR_RESET register in SYSCON module)	-	15	-	ms

[1] The wake-up time measured is the time between the triggering of the reset event to wake up the device and the setting of a GPIO output pin in the reset handler.

9.8 Wake-up process

Table 20. Dynamic characteristics: Typical wake-up times from low-power modes in XR_SM (MCX W23xB only)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wake(lpm)}$	low-power mode wake-up time	from sleep mode; 32 MHz [1] [2]	-	15.5	-	µs
		from deep-sleep mode [1] [3]	-	400	-	µs
		from power-down mode [1] [3]	-	1345	-	µs
		from deep power-down mode [1] [3]	-	15.4	-	ms
		from power-off mode [1] [4]	-	16	-	ms
$t_{cy(min)lpm}$	low-power mode minimum cycle time	minimum time required from active mode to deep-sleep mode and back to active mode [3]	-	460	-	µs
		minimum time required from active mode to power-down mode and back to active mode using CPU retention [3]	-	620	-	µs

[1] The wake-up time measured is the time between the triggering of the WAKEUP input pin to wake up the device from the low-power modes and the setting of a GPIO output pin in the interrupt handler (ISR) wake-up handler.
[2] FRO is enabled; all peripherals are off.
[3] FRO_32k is enabled; all peripherals are off.
[4] FRO_32k is disabled; all peripherals are off.

Table 21. Dynamic characteristics: Typical wake-up times from low-power modes in HV_SM (MCX W23xB only)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{wake(lpm)}$	low-power mode wake-up time	from sleep mode; 32 MHz	[1] [2]	-	15.5	-	µs
		from deep-sleep mode	[1] [3]	-	400	-	µs
		from power-down mode	[1] [3]	-	1345	-	µs
		from deep power-down mode	[1] [3]	-	15.4	-	ms
		from power-off mode	[1] [4]	-	16	-	ms
$t_{cy(min)lpm}$	low-power mode minimum cycle time	minimum time required from active mode to deep-sleep mode and back to active mode	[3]	-	460	-	µs
		minimum time required from active mode to power-down mode and back to active mode using CPU retention	[3]	-	620	-	µs

[1] The wake-up time measured is the time between the triggering of the WAKEUP input pin to wake up the device from the low-power modes and the setting of a GPIO output pin in the interrupt handler (ISR) wake-up handler.
[2] FRO is enabled; all peripherals are off.
[3] FRO_32k is enabled; all peripherals are off.
[4] FRO_32k is disabled; all peripherals are off.

9.9 FRO (64 MHz/48 MHz/32 MHz/12 MHz)

Table 22. FRO start-up time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	FRO start-up time	-	5	15	µs

Table 23. FRO oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	32 MHz free running oscillator	-	32	-	MHz
f_{acc}	frequency accuracy	FRO_32M accuracy	-	-	±3	%
		FRO_32M accuracy; at room temperature	-	-	±2	%
		FRO_32M tuning range	±20	-	-	%

9.10 FRO_1M (1 MHz)

Table 24. FRO_1M start-up time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	FRO_1M start-up time	-	15	25	µs

Table 25. FRO oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	1 MHz free running oscillator	-	1	-	MHz
f_{acc}	frequency accuracy	FRO_1M accuracy	-	-	±25	%
		FRO_1M accuracy; at room temperature with no retrim in application	-	-	±3	%
		FRO_1M accuracy; at room temperature after retrim in application	-	-	±1	%
		FRO_1M tuning range	±50	-	-	%

9.11 FRO_32k (32.768 kHz)

Table 26. FRO_32k start-up time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	FRO_32K start-up time	-	40	100	µs

Table 27. FRO_32k oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	32.768 kHz free running oscillator	-	32.768	-	kHz
f_{acc}	frequency accuracy	FRO_32k accuracy	-	-	±3	%
		FRO_32k accuracy; at room temperature after trim in application	-	-	±0.4	%
		FRO_32k tuning range	±20	-	-	%

9.12 XTAL oscillator 32 MHz

Spec from SNPS. The start-up time is updated after measurements done by the validation team.

Table 28. 32 MHz crystal oscillator characteristics

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency		-	32	-	MHz
Δf_{xtal}	crystal frequency tolerance		−30	-	+30	ppm
ESR_{xtal}	crystal equivalent series resistance		33	-	150	Ω
C_L	load capacitance		6	-	18	pF

Table 28. 32 MHz crystal oscillator characteristics*...continued*

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
C_0	shunt capacitance		-	-	4	pF
$t_{startup(osc)}$	oscillator start-up time	to achieve specifications, proper PCB layout procedures must be followed.	-	209	270	µs

9.13 XTAL oscillator 32.768 kHz

Table 29. 32.768 kHz crystal oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	unit
f_{xtal}	crystal frequency		-	32.768	-	kHz
Δf_{xtal}	crystal frequency tolerance		-20	-	+20	ppm
C_L	load capacitance		4	-	12.5	pF
C_1	motional capacitance		-	-	6.3	fF
C_0	static capacitance		-	1.4	2	pF
$R_{s(xtal)}$	crystal series resistance	32.768 kHz crystal series resistance	-	-	90	kΩ
t_s	settling time	32.768 kHz crystal oscillator settling time	-	500	2000	ms

9.14 I²C characteristics

Table 30. Dynamic characteristics: I²C pins[1]

t_{amb} = −40 °C to +85 °C;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1.1 V < V_{DD} < 3.6 V[2]						
f_{SCL}	SCL clock frequency	standard mode	0	-	100	kHz
		fast mode	0	-	400	kHz
		fast mode plus	0	-	1	MHz
t_f	fall time	SDA and SCL signals [3] [4] [5] [6]				
		standard mode	-	-	300	ns
		fast mode	20 + 0.1 × C_b		300	ns
		fast mode plus	-	-	120	ns
t_{LOW}	LOW period of the SCL clock	standard mode	4.7	-	-	μs
		fast mode	1.3	-	-	μs
		fast mode plus	0.5	-	-	μs
t_{HIGH}	HIGH period of the SCL clock	standard mode	4.0	-	-	ns
		fast mode	0.6	-	-	μs
		fast mode plus	0.26	-	-	μs
$t_{HD;DAT}$	data hold time	standard mode [7] [3] [8]	0	-	-	ns
		fast mode [7] [3] [8]	0	-	-	ns
		fast mode plus [7] [3] [8]	0	-	-	ns
$t_{SU;DAT}$	data set-up time	standard mode [9] [10]	250	-	-	ns
		fast mode [9] [10]	100	-	-	ns
		fast mode plus [9] [10]	50	-	-	ns

[1] Guaranteed by design. Not tested in production.
[2] Parameters are valid over the operating temperature range unless otherwise specified (For more information, see the I²C-bus specification user manual.
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (regarding the $V_{IH(min)}$of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.
[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. It allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[6] In fast mode plus, the fall time is specified in the same way for the output stage and the bus timing. If series resistors are used, designers must allow for it when considering bus timing.
[7] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL. It applies to data in transmission and the acknowledge.
[8] The maximum $t_{HD;DAT}$ can be 3.45 μs and 0.9 μs for Standard mode and Fast mode. However, it must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid x ns before it releases the SCL clock (where x is the setup time).
[9] $t_{SU;DAT}$ is the data setup time that is measured with regarding the rising edge of SCL. It applies to data in transmission and the acknowledge.

[10] A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. It is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I2C-bus specification) before the SCL line is released. Also, the acknowledge timing must meet this setup time.

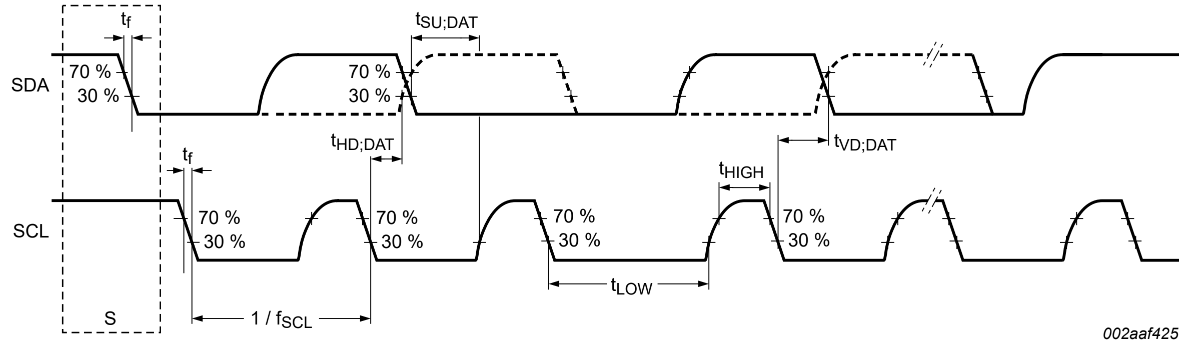


Figure 14. I²C-bus pins clock timing

9.15 SPI characteristics

The actual SPI bit rate depends on the delays that the internal trace introduces, the external device, the system clock (CCLK), and the capacitive load.

Excluding delays, the external device, and the PCB introduce, the maximum supported bit rate for SPI master and slave mode (transmit/receive) is 18 Mbit/s if VDD_IO is below 1.8 V.

This maximum supported bit rate for SPI master and slave mode (transmit/receive) can be increased up to 24 Mbit/s if VDD_IO is 1.8 V or above.

Table 31. Dynamic characteristics: SPI[1]

t_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1.8 V < V_{DD} < 3.6 V [1]						
SPI master						
$t_{su(D)}$	data set-up time		2.8	-	-	ns
$t_{h(D)}$	data hold time		5.7	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	4.0	ns
SPI slave						
$t_{su(D)}$	data set-up time		4.0	-	-	ns
$t_{h(D)}$	data hold time		3.7	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	11.4	ns
1.1 V < V_{DD} < 1.8 V[1]						
SPI master						
$t_{su(D)}$	data set-up time		2.8	-	-	ns
$t_{h(D)}$	data hold time		5.7	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	5.6	ns
SPI slave						
$t_{su(D)}$	data set-up time		4.0	-	-	ns
$t_{h(D)}$	data hold time		3.7	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	27	ns

[1] C_L = 10 pF balanced loading on all pins; input slew = 1 ns; SLEW setting = fast mode for all pins; parameters sampled at the 50 % level of the rising or falling edge.

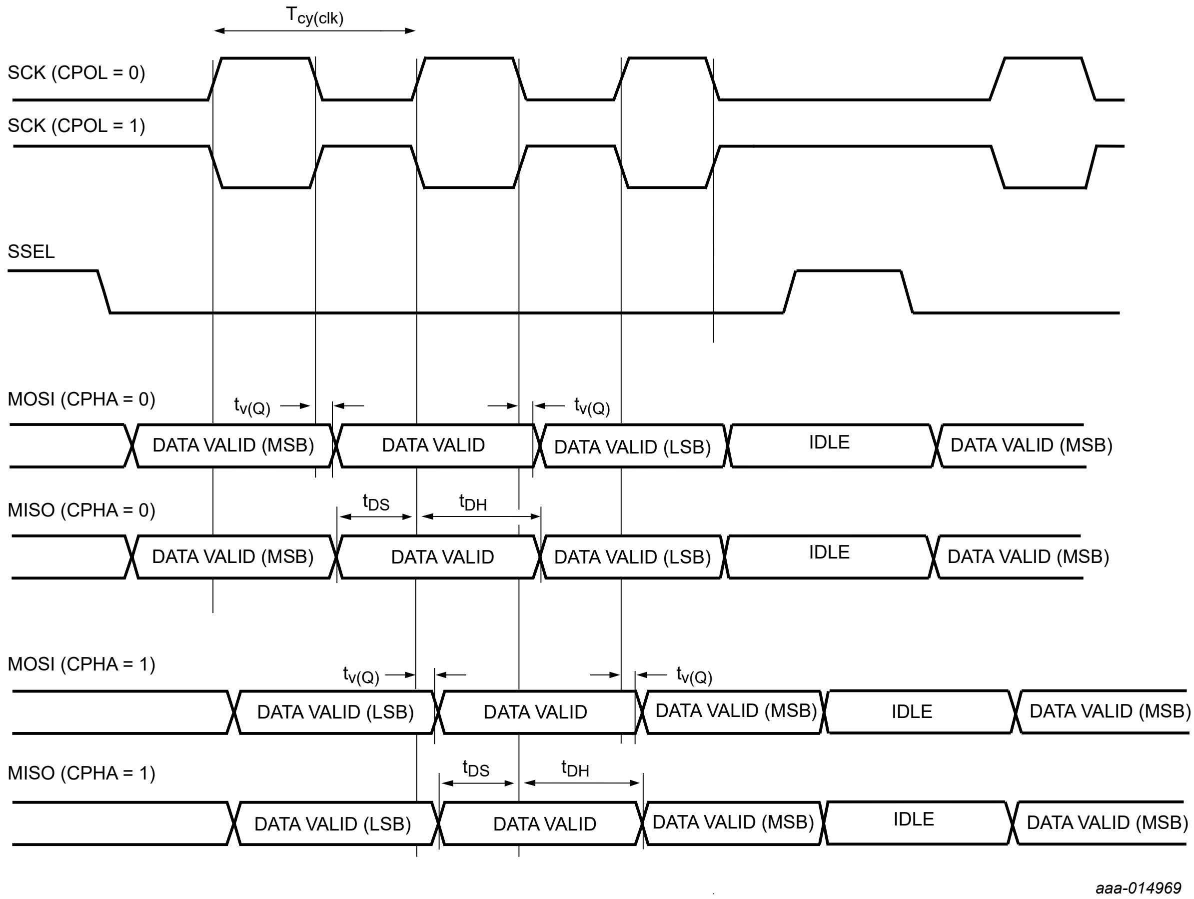


Figure 15. SPI pins clock timing

9.16 USART characteristics

The actual USART bit rate depends on the delays the external trace, the external device, the system clock (CCLK), and the capacitive load introduce.

Excluding delays the external device and the PCB introduce, the maximum supported bit rate for USART master and slave synchronous mode is 10 Mbit/s.

Excluding delays the external device and the PCB introduce, the maximum supported bit rate for USART master and slave asynchronous mode is 6.25 Mbit/s.

Table 32. Dynamic characteristics: USART pins[1]

t_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1.1 V < V_{DD} < 3.6 V[2]						
USART master (in synchronous mode)						
$t_{su(D)}$	data input set-up time		6	-	-	ns
$t_{h(D)}$	data input hold time		0	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	12.4	ns
USART slave (in synchronous mode)						
$t_{su(D)}$	data input set-up time		7.6	-	-	ns
$t_{h(D)}$	data input hold time		3.2	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	28	ns

[1] Based on simulated values. Not tested in production.
[2] C_L = 10 pF balanced loading on all pins; input slew = 1 ns, SLEW setting = fast mode for all pins; parameters sampled at the 50 % level of the rising or falling edge.

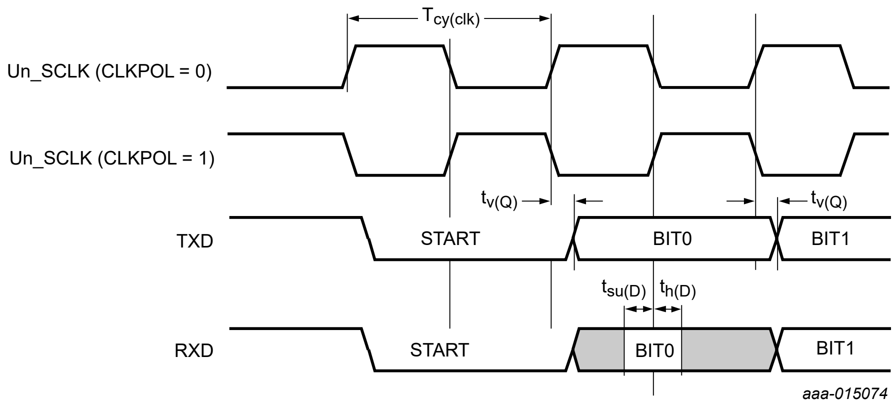


Figure 16. USART timing

9.17 SPIFI characteristics

The actual SPIFI bit rate depends on the delays the external trace, the external device, the system clock (CCLK), and the capacitive load introduce.

Excluding delays, the external device, and the PCB introduce, the maximum supported bit rate for SPIFI mode is 128 Mbit/s when operating in quad mode with a VDD_IO below 1.8 V. Excluding delays, the external device, and the PCB introduce, the maximum supported bit rate for SPIFI mode is 32 Mbit/s when operating in single-bit mode with a VDD_IO below 1.8 V.

Excluding delays, the external device, and the PCB introduce, the maximum supported bit rate for SPIFI mode is 256 Mbit/s when operating in quad mode with a VDD_IO at 1.8 V or above. Excluding delays, the external device, and the PCB introduce, the maximum supported bit rate for SPIFI mode is 64 Mbit/s when operating in single-bit mode with a VDD_IO at 1.8 V or above.

Table 33. Dynamic characteristics: SPIFI[1]

t_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1.8 V < V_{DD} < 3.6 V[2]						
$t_{su(D)}$	data set-up time	[3]	5	-	-	ns
$t_{h(D)}$	data hold time	[3]	3	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	5.5	ns
1.1 V < V_{DD} < 1.8 V[2]						
$t_{su(D)}$	data set-up time	[3]	6	-	-	ns
$t_{h(D)}$	data hold time	[3]	3	-	-	ns
$t_{v(Q)}$	data output valid time		-	-	6.5	ns

[1] Based on simulated values. Not tested in production.

[2] C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = fast mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

[3] $t_{su(D)}$ and $t_{h(D)}$ above are the same for RFCLK = 0 or RFCLK = 1 (data latched on SPIFI_CLK rising or falling edge).

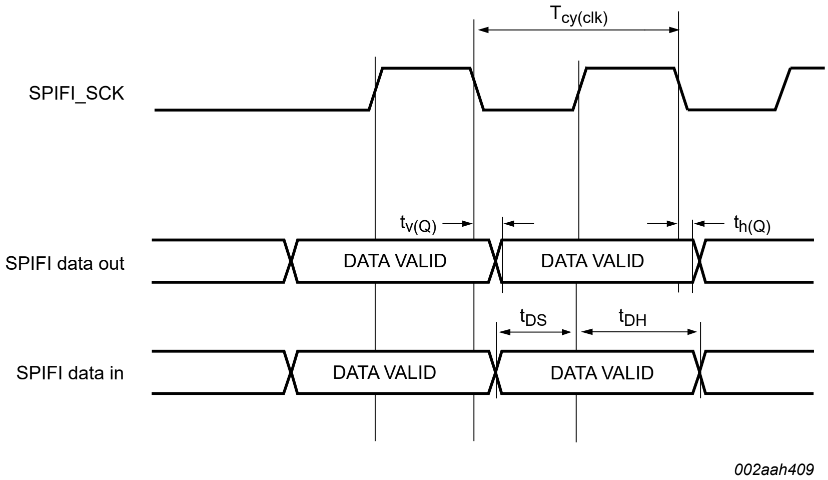


Figure 17. SPIFI timing

10 Analog characteristics

10.1 Power-on reset (POR)

More information on the characteristics can be found in Section 7.3.6

Table 34. POR

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(por)}$	power-on reset detection rising edge threshold voltage	On VBAT_HV pin for MCX W23xB; ***Note:*** *The POR circuit is automatically turned off when the voltage rises above $V_{th(por)}$ during power-up. If the supply drops below 0.2V, it turns on again.*	1.305	1.45	1.595	V

10.2 Brownout detection (BOD)

Table 35. BOD for MCX W23xB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(bod)}$	brownout detection threshold voltage	The BOD monitors the VBAT_HV pin.	1.55	-	3.1	V
$\Delta V_{th(acc)}$	brownout detection threshold voltage accuracy	Percentage of the set point voltage level for a temperature range between 0 °C and 85 °C and a threshold level of 1.7 V (after applying trim)	−2.5	-	+2.5	%
		Percentage of the set point voltage level for untrimmed BOD	−7.5	-	+7.5	%

10.3 DC-DC converter buck mode (MCX W23xB only)

The DC-DC converter in buck mode takes the input from the VBAT_HV pin and supplies an output on the VBAT_LV pin.

Table 36. DC-DC converter buck mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(DCDC)}$	DC-DC output voltage	buck DC-DC output default level on VBAT_LV pin; for input supply range, see $V_{BAT(hv)}$ [1]	1.14	1.2	1.26	V
$\Delta V_{O(dcdc)}$	DC-DC output configuration range	[2] buck DC-DC output configuration range; configurable by application software in 8 steps of 100 mV; output level on VBAT_LV pin; for input supply range, see $V_{BAT(hv)}$.	1.1	-	1.8	V
$I_{O(dcdc)buck(max)}$	maximum buck DC-DC output current	for 1.2 V output voltage at the VBAT_LV pin	20	-	-	mA

[1] The DC-DC output voltage remains accurate within ± 5% of the programmed DC-DC output voltage level.
[2] The programmed DC-DC output voltage must be at least 400mV lower than the DC-DC input voltage

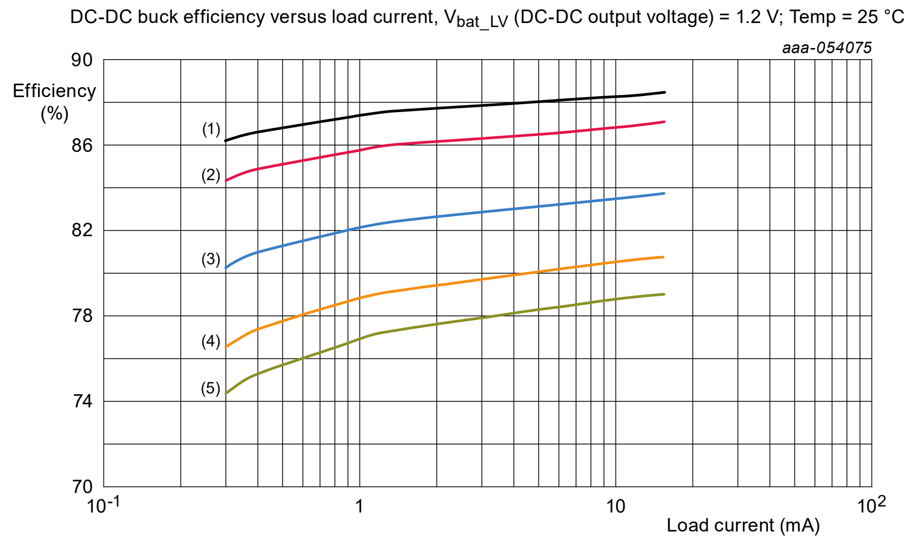


Figure 18. DC-DC efficiency - buck

(1) Vbat_HV = 1.8 V
(2) Vbat_HV = 2.0 V
(3) Vbat_HV = 2.5 V
(4) Vbat_HV = 3.0 V
(5) Vbat_HV = 3.3 V

11 Bluetooth Low Energy radio characteristics

The specifications are guaranteed on the MCX W23 reference board schematics and layout. All parameters are referred to the chip antenna pin.

11.1 RF transceiver specification

Table 37. 2.4 GHz radio transceiver specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD_RF}	RF supply voltage		1.1	1.2	3.3	V
$f_{i(RF)}$	RF input frequency		2.400	-	2.484	GHz
$f_{o(RF)}$	RF output frequency		2.400	-	2.484	GHz
$f_{ref(osc)xtal}$	crystal oscillator reference frequency		-	32	-	MHz
f_{tol}	frequency tolerance		-	±40	-	ppm
$t_{T(RX\_TX)}$	RX-TX turnaround time		-	150	-	μs
$I_{DD(pd)}$	power-down supply current	measured on VDD_RF pin; 1.2 V supplied at the VDD_RF pin	-	12	-	nA
		measured on VDD_RF pin; 1.8 V supplied at the VDD_RF pin	-	18	-	nA
		measured on VDD_RF pin; 3.0 V supplied at the VDD_RF pin	-	25	-	nA

11.2 RF transmitter specifications

Table 38. Transmitter generic specifications: Part 1

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$P_{o(tol)}$	output power tolerance	at 2 dBm in TXM1 mode	-	±1.5	-	dB
$Z_{o(se)}$	single-ended output impedance		-	50	-	Ω
$\alpha_{emi(sp)}$	spurious emissions	all TX output levels and all rates Complies with: • EN 300 328 V2.2.2 • FCC CFR 47 part 15 • ARIB STD-66 • RSS-210				
		range: 30 MHz to 1000 MHz	-	-	−36	dBm/100 kHz
		range: 1 GHz to 12.75 GHz	-	-	−30	dBm/1 MHz
		range: 47 MHz to 74 MHz	-	-	−56	dBm/100 kHz
		range: 87.5 MHz to 118 MHz	-	-	−54	dBm/100 kHz
		range: 174 MHz to 230 MHz	-	-	−54	dBm/100 kHz
		range: 470 MHz to 694 MHz	-	-	−54	dBm/100 kHz
$\alpha_{emi(sp)}$	spurious emissions	at P_{out} < 0 dBm; range: 2.0 GHz to 3.0 GHz	-	−60	−45	dBm/1 MHz

Table 39. Transmitter generic specifications: Part 2

Symbol	Parameter	Condition[1]	Min	Typ	Max	Unit
$I_{DD(RF)}$	supply current from VDD_RF pin	P_{RF} = 6 dBm (TXM2 mode); continuous wave mode measured on the VDD_RF pin; 3.0 V supplied at the VDD_RF pin	-	12.6	-	mA
		P_{RF} = 6 dBm (TXM2 mode); continuous wave mode measured on the VDD_RF pin; 1.8 V supplied at the VDD_RF pin	-	12.6	-	mA
		P_{RF} = 2 dBm (TXM1 mode); continuous wave mode measured on the VDD_RF pin; 3.0 V supplied at the VDD_RF pin	-	10.4	-	mA
		P_{RF} = 2 dBm (TXM1 mode); continuous wave mode measured on the VDD_RF pin; 1.8 V supplied at the VDD_RF pin	-	10.2	-	mA
		P_{RF} = 2 dBm (TXM1 mode); continuous wave mode measured on the VDD_RF pin; 1.2 V supplied at the VDD_RF pin	-	10.2	-	mA
		P_{RF} = 0 dBm (TXM1 mode); continuous wave mode measured on the VDD_RF pin; 3.0 V supplied at the VDD_RF pin	-	9.2	-	mA
		P_{RF} = 0 dBm (TXM1 mode); continuous wave mode measured on the VDD_RF pin; 1.8 V supplied at the VDD_RF pin	-	9.0	-	mA
		P_{RF} = 0 dBm (TXM1 mode); continuous wave mode measured on the VDD_RF pin; 1.2 V supplied at the VDD_RF pin	-	9.0	-	mA
$P_{o(RF)}$	RF output power	1.8 V supplied at the VDD_RF pin [2] [3]	-28	-	6	dBm
		1.2 V supplied at the VDD_RF pin [2]	-31	-	2	dBm
$f_{drift(max)}$	maximum frequency drift	frequency drift during any packet	-	-	±50	kHz
BW_{1M}	Bandwidth	20 dB bandwidth; TX output spectrum for Bluetooth Low Energy data rate of 1 Mbps	-	1.1	-	MHz
BW_{2M}	Bandwidth	20 dB bandwidth; TX output spectrum for Bluetooth Low Energy data rate of 2 Mbps	-	2.2	-	MHz
$ACPR_{2M}$	adjacent channel power ratio (2 MHz)	adjacent channel transmit power at 2 MHz offset for Bluetooth Low Energy data rate at 1 Mbps and 0 dBm transmit output power.	-	−50	−40	dBc

Table 39. Transmitter generic specifications: Part 2...*continued*

Symbol	Parameter	Condition[1]	Min	Typ	Max	Unit
$ACPR_{3M}$	adjacent channel power ratio (≥ 3 MHz)	Adjacent channel transmit power at ≥ 3 MHz offset for Bluetooth Low Energy data rate at 1 Mbps and 0 dBm transmit output power.	-	−54	−50	dBc
$ACPR_{4M}$	adjacent channel power ratio (4 MHz)	adjacent channel transmit power at 4 MHz offset for Bluetooth Low Energy data rate at 2 Mbps and 0 dBm transmit output power.	-	−55	−50	dBc
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	Adjacent channel transmit power at ≥ 5 MHz offset for Bluetooth Low Energy data rate at 2 Mbps and 0 dBm transmit output power.	-	−57	−50	dBc
$ACPR_{6M}$	adjacent channel power ratio (≥ 6 MHz)	Adjacent channel transmit power at ≥ 6 MHz offset for Bluetooth Low Energy data rate at 2 Mbps and 0 dBm transmit output power.	-	−59	−50	dBc
α_{2H}	second harmonic level	Power in second harmonic of transmit carrier frequency with P_o = 0 dBm in TXM1	-	-	−42	dBc
α_{3H}	third harmonic level	Power in the third harmonic of transmit carrier frequency with P_o = 0 dBm in TXM1	-	-	−42	dBc
$\alpha_{emi(oob)}$	out-of-band emission	at maximum output power excluding harmonics	-	-	−45	dBm
$\alpha_{emi(sp)ib}$	in-band spurious emission	at 2 MHz offset for all TX output levels and all rates	-	-	−20	dBm
		at ≥ 3 MHz offset for all TX output levels and all rates	-	-	−30	dBm

[1] All TX parameters are measured at a test hardware SMA connector and referred to the chip antenna pin.
[2] Min/Max values exclude $P_{o(tol)}$ output power tolerance number.
[3] For the WLCSP37 package, channels 15 (2432 MHz) and 31 (2464 MHz) are limited to +2 dBm to safeguard regulatory requirements. This is further explained in the Errata document.

11.3 RF receiver specifications

The tables below contain the detailed specifications of the RF radio receiver.

The following conventions are chosen:

- Maximum input power $P_{i(max)}$ is given for a 10-3 BER.
- RX sensitivity $P_{RX,*}$ is defined for a 10-3 BER for all modes.

A 10-3 BER corresponds to a 30.8 % PER, since a 37-byte PDU length is used according to the Bluetooth Low Energy RF PHY test specification:

- Cochannel interference (CC_{interf}) and adjacent channel interference (AC_{interf}) are measured with a wanted signal 3 dB over the Bluetooth Low Energy specification reference sensitivity level. One interferer has the same modulation as the wanted signal. The measurement is done according to the Bluetooth Low Energy RF PHY test spec for all different modes.
- IMD is measured with a wanted signal at −64 dBm and 2 interferers that have the same power. The closest interferer is a CW signal. The other interferer has the same modulation as the wanted signal. The largest

power of the interfering signals for which the wanted signal fulfills the sensitivity criterion is reported. The measurement is done according to the Bluetooth Low Energy RF PHY test spec for all different modes.

Table 40. Receiver generic specifications: Part 1

Symbol	Parameter		Min	Typ	Max	Unit
$P_{i(max)}$	Maximum input power		-	-	−10	dBm
LO_{leak}	LO leakage		-	−70	-	dBm
$\alpha_{oob(block)}$	out-of-band blocking	As defined by the Bluetooth Low Energy standard (Bluetooth spec 4.0 – Volume 6 – Part A – section 4.3);				
		range: 30 MHz to 2000 MHz	−30	2	-	dBm
		range: 2003 MHz to 2399 MHz	−35	−20	-	dBm
		range: 2484 MHz to 2997 MHz	−35	0	-	dBm
		range: 3000 MHz to 12.75 GHz	−30	+2	-	dBm
$\alpha_{emi(sp)RX}$	RX spurious emissions	range: 30 MHz to 1 GHz	-	-	−57	dBm/100 kHz
		exceeding 1 GHz	-	-	−47	dBm/1 MHz
Z_i	input impedance		-	50	-	Ω

Table 41. 2.4 GHz radio receiver specifications: Part 2

Symbol	Parameters	Conditions[1]	Min	Typ	Max	Unit
$I_{DD(RF)}$	supply current from VDD_RF pin	continuous wave mode measured on the VDD_RF pin; 3.0 V supplied at the VDD_RF pin; applicable for all PHY modes	-	5.8	-	mA
		continuous wave mode measured on the VDD_RF pin; 1.8 V supplied at the VDD_RF pin; applicable for all PHY modes	-	5.7	-	mA
		continuous wave mode measured on the VDD_RF pin; 1.2 V supplied at the VDD_RF pin; applicable for all PHY modes	-	5.7	-	mA
S_{RX}	RX sensitivity	Bluetooth Low Energy long range RX sensitivity at 125 kbps [2]	-	−102	-	dBm
		Bluetooth Low Energy long range RX sensitivity at 500 kbps [2]	-	−100	-	dBm
		Bluetooth Low Energy legacy RX sensitivity at 1 Mbps [2]	-	−97	-	dBm
		Bluetooth Low Energy long range RX sensitivity at 2 Mbps [2]	-	−94	-	dBm
$\alpha_{RSSI(range)}$	RSSI range		-100	-	-30	dBm
$\alpha_{RSSI(res)}$	RSSI resolution		-	1	-	dB
$\alpha_{RSSI(acc)}$	RSSI accuracy	−35 dBm > signals ≥ −50 dBm	−3	-	+3	dB
		−50 dBm > signals ≥ −85 dBm	−6	-	+6	dB

Table 41. 2.4 GHz radio receiver specifications: Part 2*...continued*

Symbol	Parameters	Conditions[1]	Min	Typ	Max	Unit
IRR	Image rejection ratio	Bluetooth Low Energy image frequency interference (wanted signal at −67 dBm, BER < 0.1 %; measurement resolution = 1 MHz)				
		in Bluetooth Low Energy = 1 Mbps, LR = 500 kbps, and LR = 250 kbps modes; C/I	-	−21	−9	dB
		in Bluetooth Low Energy = 2 Mbps mode; C/I	-	−21	−9	dB
CC_{interf}	cochannel interference	wanted signal 3 dB over reference sensitivity level); C/I	-	8	10	dB

[1] All the RX parameters are measured at the test hardware SMA connector and referred to the chip antenna pin.
[2] Packet error rate of 30 %.

Table 42. 2.4 GHz radio receiver specifications: Part 3

Symbol	Parameters	Conditions[1]	Min	Typ	Max	Unit
Adjacent/alternate channel performance						
$AC_{interf(1M)}$	adjacent channel interference offset at 1 MHz	Wanted signal at −67 dBm; BER < 0.1 %; measurement resolution = 1 MHz; in Bluetooth Low Energy = 1 Mbps, LR = 500 kbps, and LR = 250 kbps modes; C/I				
		−1 MHz	-	−4	15	dB
		+1 MHz	-	1	15	dB
$AC_{interf(2M)}$	adjacent channel interference offset at 2 MHz	wanted signal at −67 dBm; BER < 0.1 %; measurement resolution = 1 MHz; in Bluetooth Low Energy = 1 Mbps, LR = 500 kbps, and LR = 250 kbps modes; C/I				
		−2 MHz	-	−21	−9	dB
		+2 MHz	-	−35	−17	dB
		in Bluetooth Low Energy = 2 Mbps mode; C/I				
		−2 MHz	-	−4	15	dB
		+2 MHz	-	1	15	dB
$AC_{interf(3M)}$	adjacent channel interference offset at 3 MHz	wanted signal at −67 dBm; BER < 0.1 %; measurement resolution = 1 MHz; in Bluetooth Low Energy = 1 Mbps, LR = 500 kbps, and LR = 250 kbps modes; C/I				
		−3 MHz	-	−27	−15	dB
		+3 MHz	-	−40	−27	dB

Table 42. 2.4 GHz radio receiver specifications: Part 3*...continued*

Symbol	Parameters	Conditions[1]	Min	Typ	Max	Unit
$AC_{interf(4M)}$	adjacent channel interference offset at 4 MHz	wanted signal at −67 dBm; BER < 0.1 %; measurement resolution = 1 MHz; in Bluetooth Low Energy = 1 Mbps, LR = 500 kbps, and LR = 250 kbps modes; C/I				
		−4 MHz	-	−40	−27	dB
		+4 MHz	-	−40	−27	dB
		in Bluetooth Low Energy = 2 Mbps mode; C/I				
		−4 MHz	-	−21	−9	dB
		+4 MHz	-	−35	−17	dB
$AC_{interf(3M)}$	adjacent channel interference offset at 6 MHz	wanted signal at −67 dBm; BER < 0.1 %; measurement resolution = 1 MHz; in Bluetooth Low Energy = 2 Mbps mode; C/I				
		−6 MHz	-	−27	−15	dB
		+6 MHz	-	−40	−27	dB
$AC_{interf(3M)}$	adjacent channel interference offset at 8 MHz	wanted signal at −67 dBm; BER < 0.1 %; measurement resolution = 1 MHz; in Bluetooth Low Energy = 2 Mbps mode; C/I				
		−8 MHz	-	−40	−27	dB
		+8 MHz	-	−40	−27	dB
Intermodulation performance						
	Bluetooth Low Energy intermodulation with continuous wave interferer at +3 MHz and modulated interferer is at +6 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 1 Mbps mode	−50	−30	-	dBm
	Bluetooth Low Energy intermodulation with continuous wave interferer at −3 MHz and modulated interferer is at −6 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 1 Mbps mode	−50	−35	-	dBm
	Bluetooth Low Energy intermodulation with continuous wave interferer at +5 MHz and modulated interferer is at +10 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 1 Mbps mode	−50	−30	-	dBm
	Bluetooth Low Energy intermodulation with continuous wave interferer at −5 MHz and modulated interferer is at −10 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 1 Mbps mode	−50	−30	-	dBm
	Bluetooth Low Energy intermodulation with modulated interferer is at +6 MHz and modulated interferer is at +12 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 2 Mbps mode	−50	−33	-	dBm
	Bluetooth Low Energy intermodulation with modulated interferer is at -6 MHz and modulated interferer is at -12 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 2 Mbps mode	−50	−38	-	dBm
	Bluetooth Low Energy intermodulation with modulated interferer is at +10 MHz and modulated interferer is at +20 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 2 Mbps mode	−50	−33	-	dBm

Table 42. 2.4 GHz radio receiver specifications: Part 3*...continued*

Symbol	Parameters	Conditions[1]	Min	Typ	Max	Unit
	Bluetooth Low Energy intermodulation with modulated interferer is at −10 MHz and modulated interferer is at −20 MHz	wanted signal at −64 dBm; BER < 0.1 %; in Bluetooth Low Energy = 2 Mbps mode	−50	−33	-	dBm

[1] All the RX parameters are measured at the RF pins.

12 Application information

The radio daughter module (RDM) is used for radio performance measurements. The RDM can be configured in all supply modes (HV_SM and XR_SM).

The configuration of VDD_IO and VDD_RF can be made with solder jumpers to VBAT_HV, VBAT_LV or an external supply.

The RDM with the recommended component list is aligned for the application diagrams:

- Application diagram for HV_SM using MCX W23xB: Figure 7

More details on the RDM boards (including recommended BoM) can be found in the Hardware Design Considerations for MCX W23" application note[Ref.8].

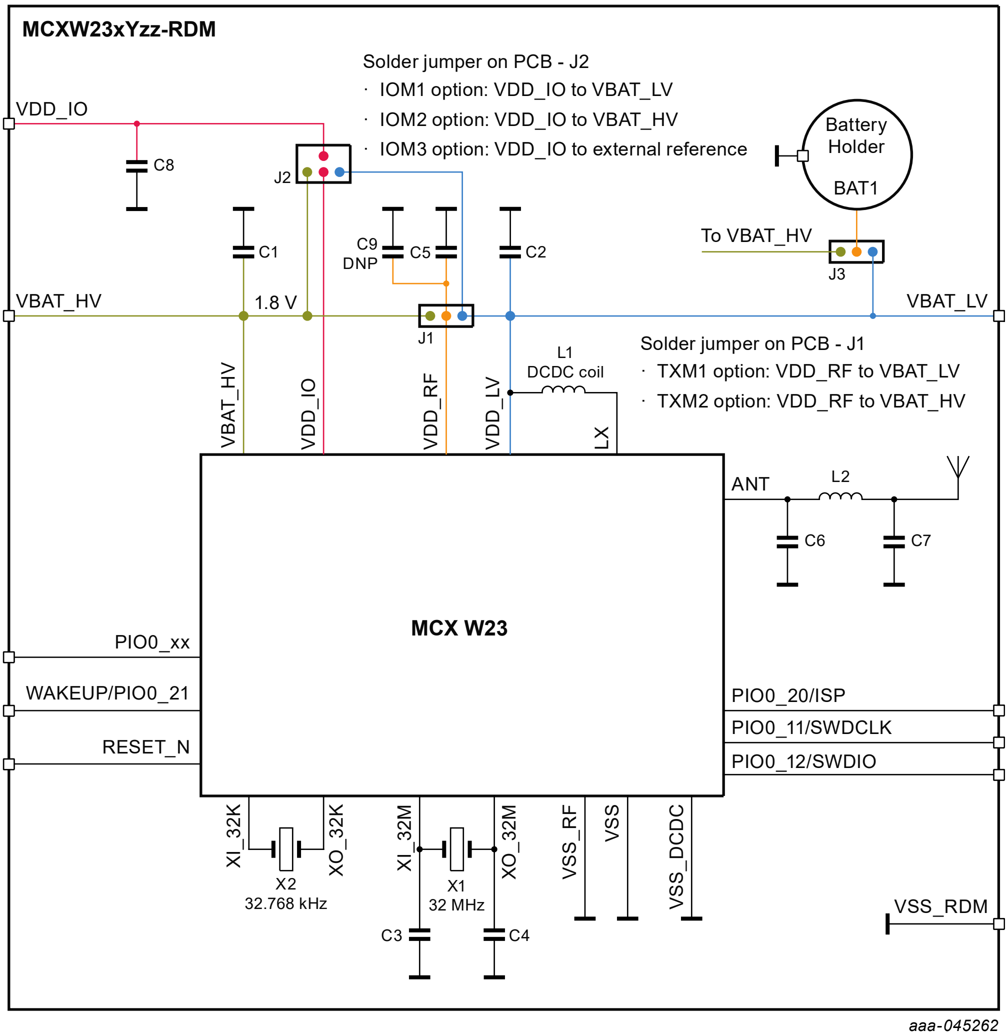


Figure 19. Radio daughter module

Table 43. Reference components

Symbol	Component	Value WLCP	Value QFN	Package
Mandatory				
X1	32 MHz crystal; ±20 ppm	Load capacitance = 6 pF	Load capacitance = 6 pF	TST; TZ3525A; 1.2 mm × 1.0 mm × 0.25 mm
ANT	Bluetooth Low Energy antenna	-	-	-
C1	voltage-decoupling capacitor for VBAT_HV	10 μF; 6.3 V; X5R/ X7R[1][2]	10 μF; 6.3 V; X5R/ X7R[1][2]	0603; 1.6 mm × 0.8 mm × 0.8 mm TDK: MLW1608A2R2WT000
C2	voltage-decoupling capacitor for VBAT_LV	10 μF; 6.3 V; X5R/ X7R[1][2]	10 μF; 6.3 V; X5R/ X7R[1][2]	0402; 1.0 mm × 0.5 mm × 0.5 mm Murata: GRM188R60J106
L1	DC-DC converter inductor	2.2 μH ± 20 %[3][4]	2.2 μH ± 20 %[3][4]	0603; 1.6 mm × 0.8 mm × 0.8 mm TDK: MLW1608A2R2WT000
C5	RF supply-decoupling capacitor	470nF	470nF	0201; 0.6 mm × 0.3 mm × 0.3 mm
C3	capacitor XTAL[5]	9pF	7.2pF	0201; 0.6 mm × 0.3 mm × 0.3 mm
C4	capacitor XTAL[5]	9pF	7.2pF	0201; 0.6 mm × 0.3 mm × 0.3 mm
L2	inductor pi filter[5]	3.4nH	2.5nH	0402; 1.0 mm × 0.5 mm × 0.5 mm
C6	capacitor pi filter[5]	1.5pF	1.6pF	0402; 1.0 mm × 0.5 mm × 0.5 mm
C7	capacitor pi filter[5]	1.5pF	1.6pF	0402; 1.0 mm × 0.5 mm × 0.5 mm
X2[5]	32.768 kHz crystal for real-time clock function	Load capacitance = 6 pF	Load capacitance = 6 pF	CM9V0T1A; 1.6mm x 0.3 mm x 0.5 mm
Optional				
BAT1	single silver-oxide coin-cell	high-drain	high-drain	diameter = 9.5 mm; height = 2.7 mm; Seizaiken: SR927W
C8	VDDIO decouple capacitor	100 nF	100 nF	0201; 0.6 mm × 0.3 mm × 0.3 mm
C9	additional RF supply decoupling capacitor	10pF (do not populate)	10pF (do not populate)	0201; 0.6 mm × 0.3 mm × 0.3 mm
C10	additional VDDIO decouple capacitor	-	10 nF (do not populate)	0402; 1.0 mm × 0.5 mm × 0.5 mm

[1] Capacitor minimum value of 5 μF after taking into account tolerances and derating conform to application conditions: temperature, operating voltage, lifetime, and so on

[2] ESR<10 mΩ maximum; smaller ESR values improve supply noise and radio performance

[3] Rated current (L change; maximum = 130 mA (50 % down).

[4] DC resistance (typical) = 250 mΩ.

[5] The values need to be tuned depending on the integration. For more information, see Hardware Design Considerations for MCX W23 in Section 17.

13 Package outline

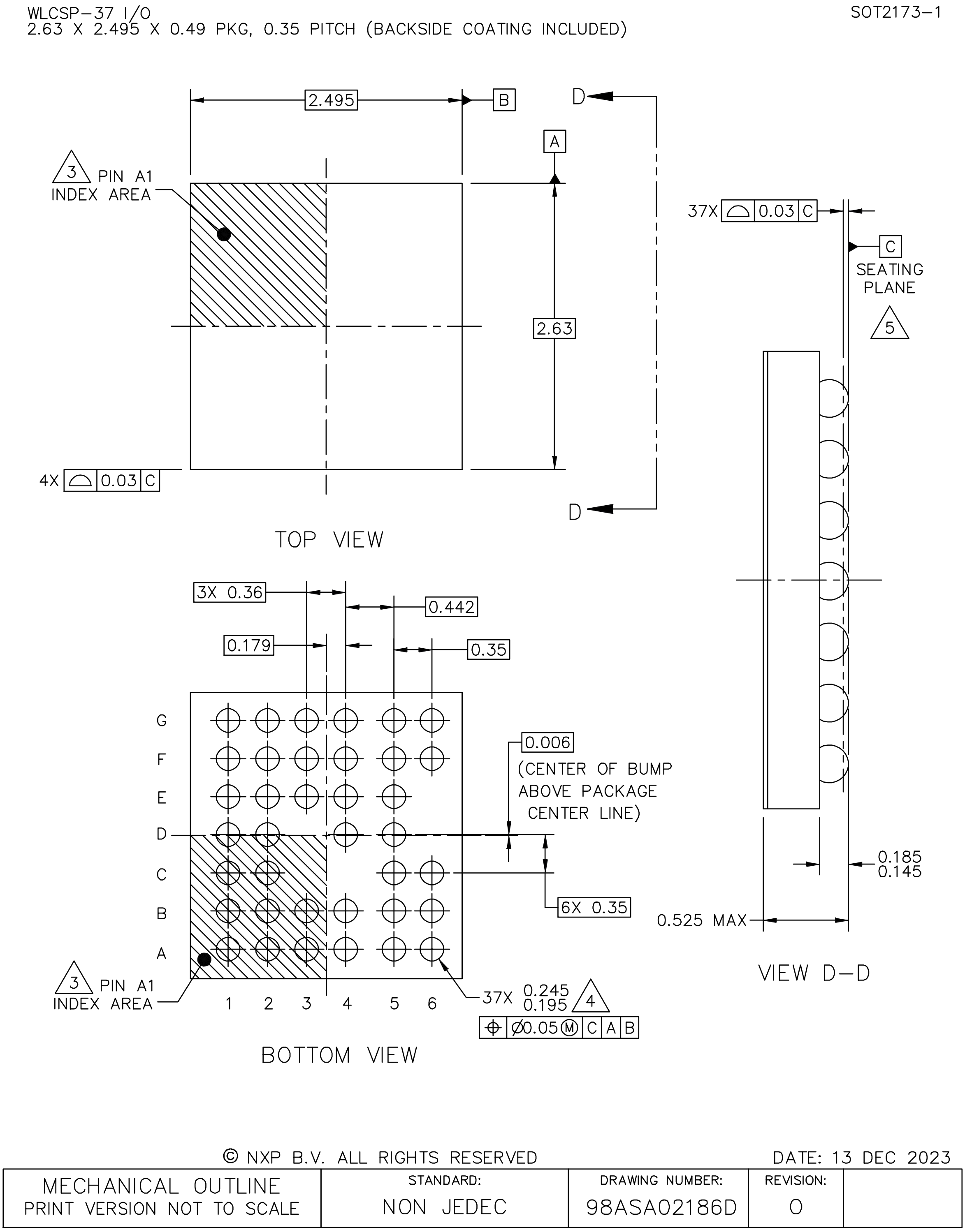


Figure 20. MCX W23 WLCSP37 – package outline part 1

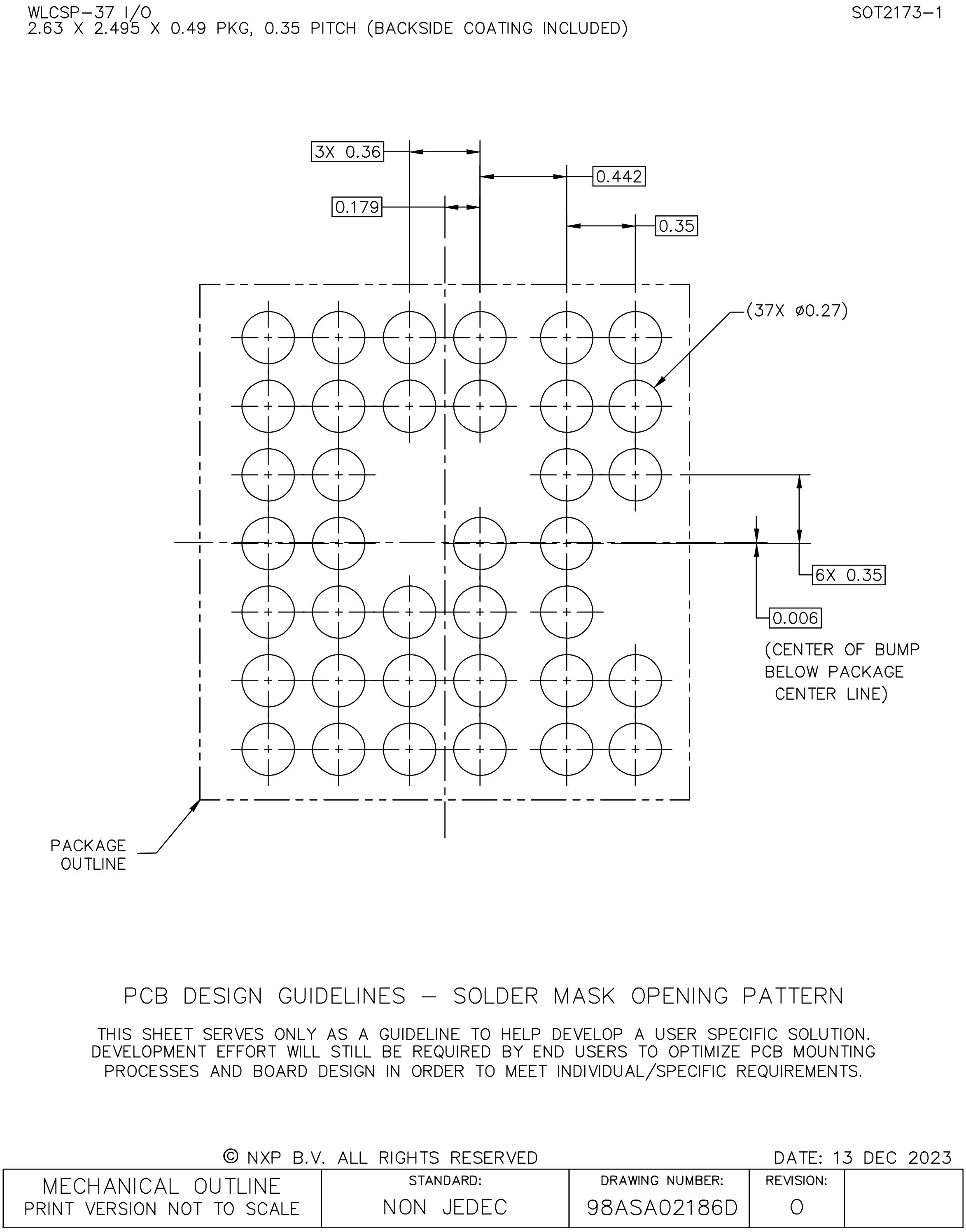
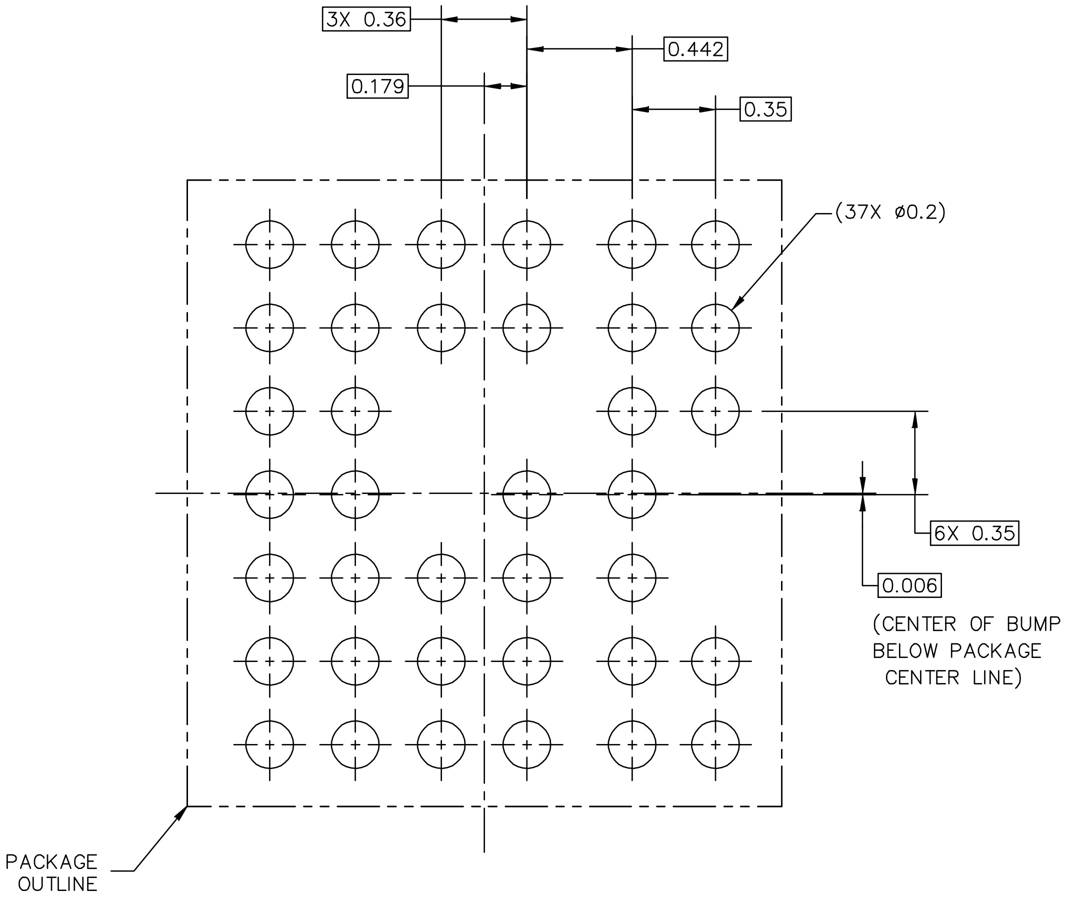


Figure 21. MCX W23 WLCSP37 – package outline part 2

WLCSP–37 I/O
2.63 X 2.495 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2173–1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

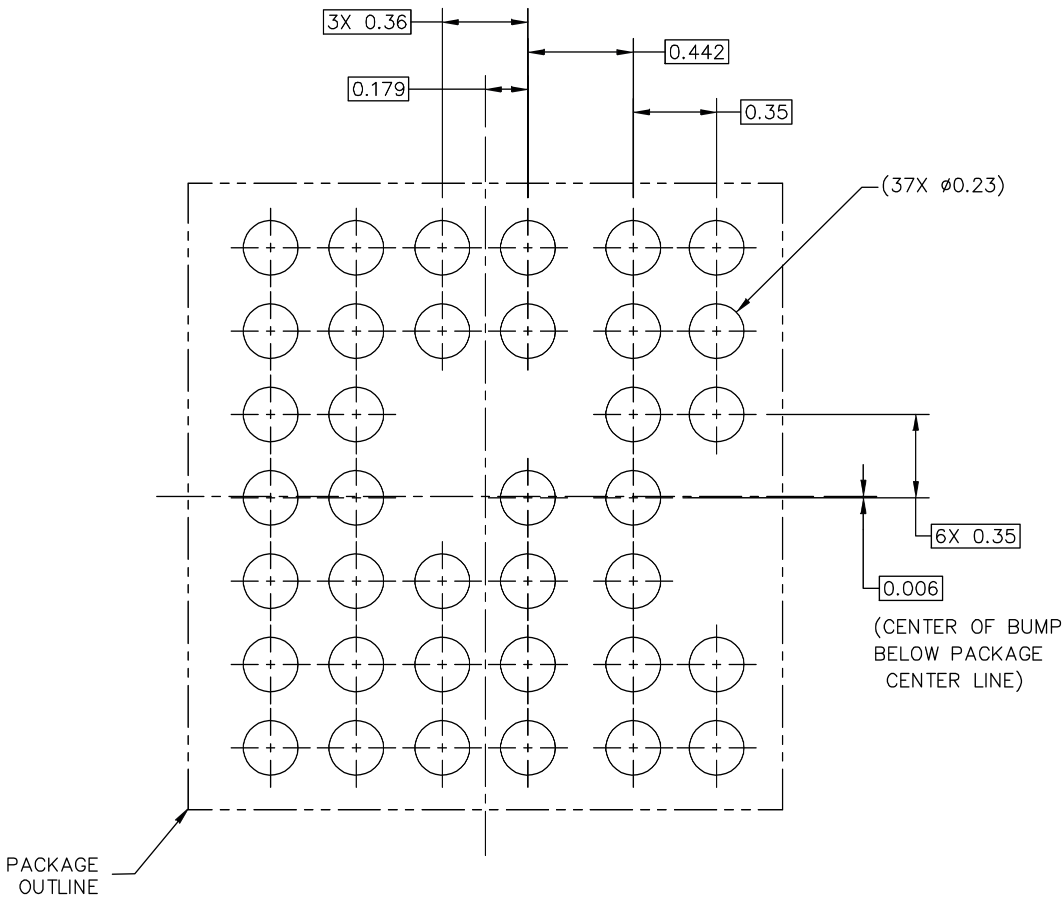
DATE: 13 DEC 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02186D	REVISION: O	

Figure 22. MCX W23 WLCSP37 – package outline part 3

WLCSP–37 I/O
2.63 X 2.495 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2173–1



RECOMMENDED STENCIL THICKNESS 0.08

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02186D	REVISION: O	

Figure 23. MCX W23 WLCSP37 – package outline part 4

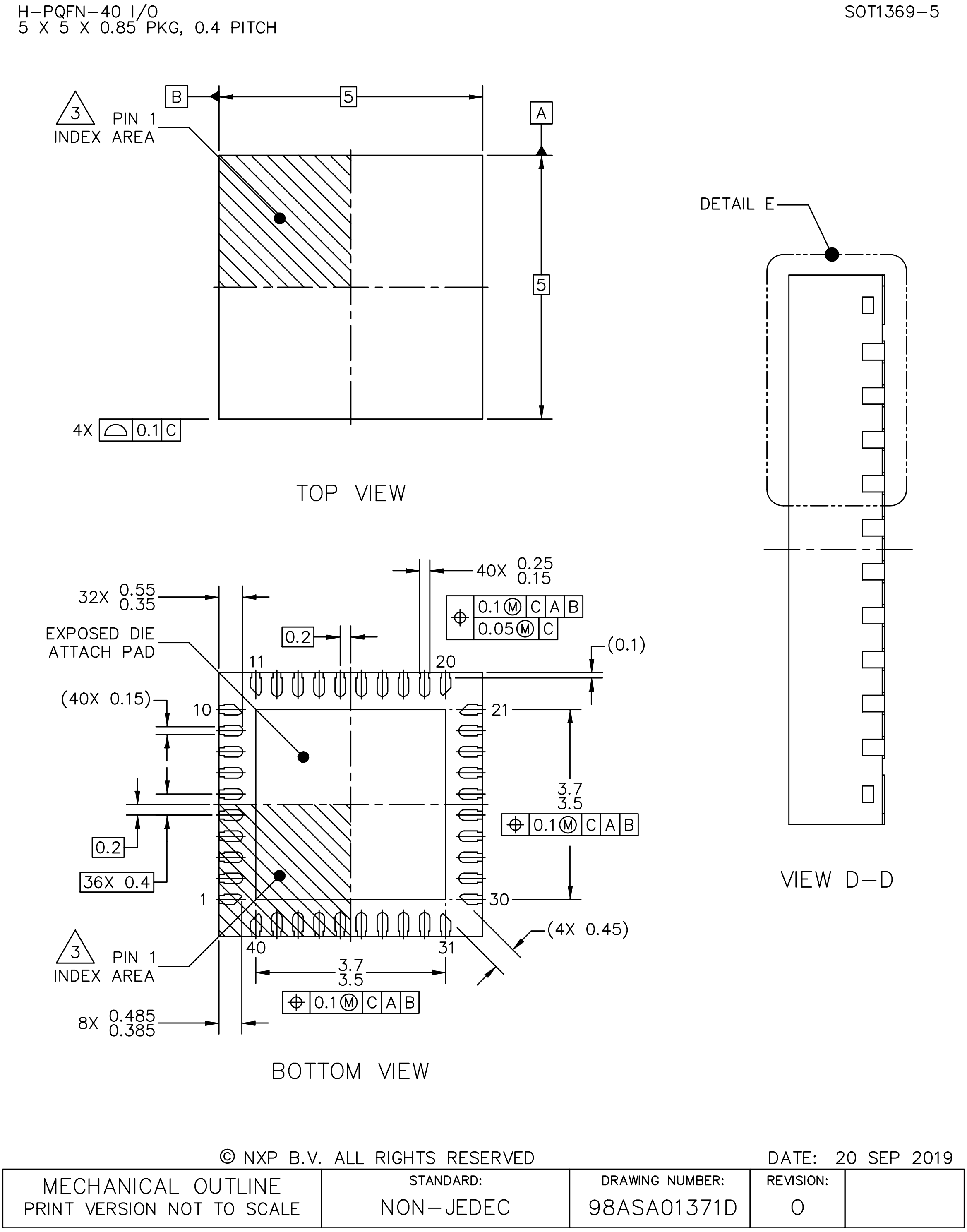
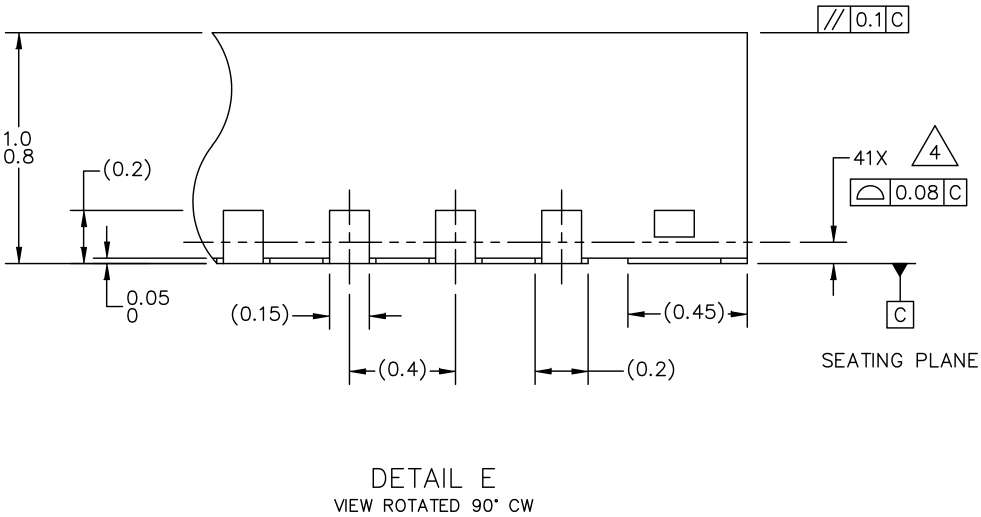


Figure 24. MCX W23 QFN40 – Package outline part 1

H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-5



DATE: 20 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01371D	REVISION: O	

Figure 25. MCX W23 QFN40 – Package outline part 2

14 Handling information

The shelf life and shipping age limits for NXP products have been described in the "NXP Shelf Life Policy" document.

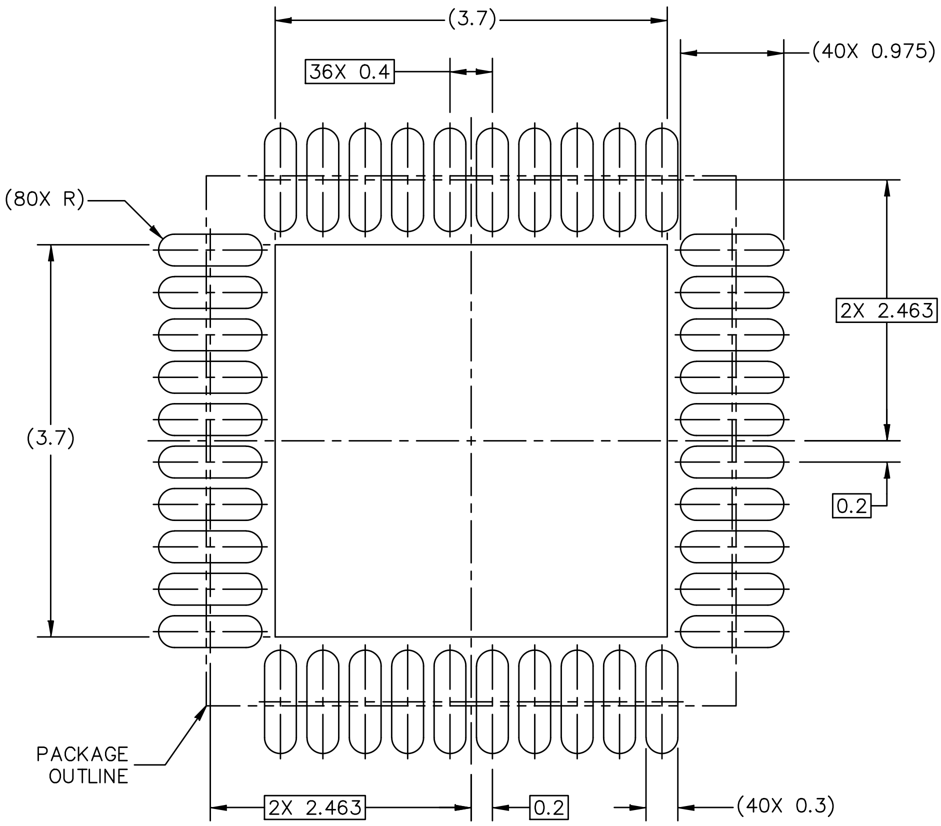
A more in-depth account of soldering WLCSP (Wafer level chip-size packages) can be found in the "Wafer level chip size package" application note and in the "Surface mount reflow soldering" application note. Wave soldering is not suitable for this package. All NXP WLCSP packages are lead-free.

More details on how to handle QFN packages can be found in the "Assembly guidelines for QFN and SON packages" application note.

Figure 26, Figure 27, and Figure 28 show the soldering footprint for the MCX W23 QFN40 devices.

H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-5



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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DATE: 20 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01371D	REVISION: O	

Figure 26. MCX W23 QFN40 – Soldering footprint part 1

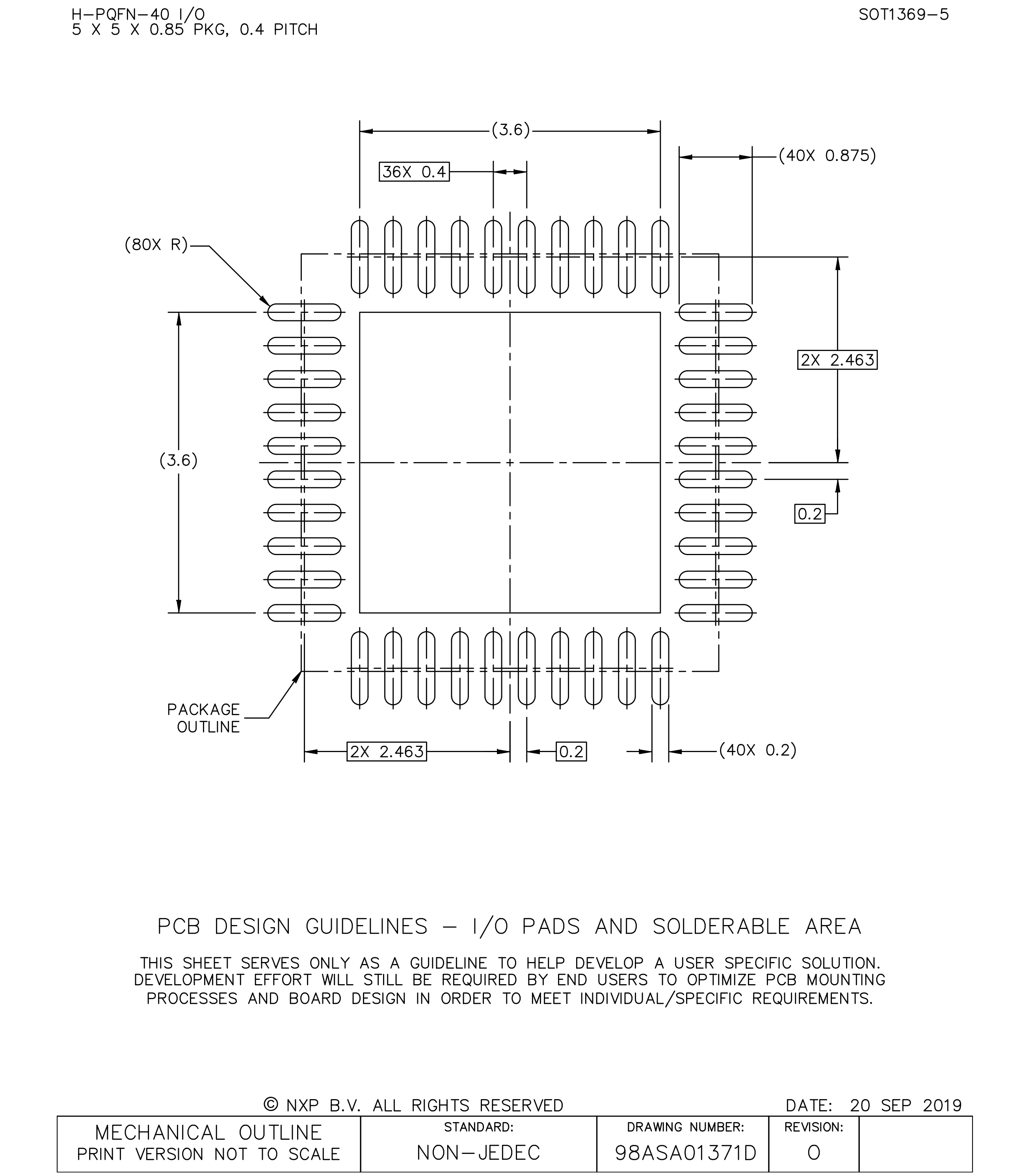
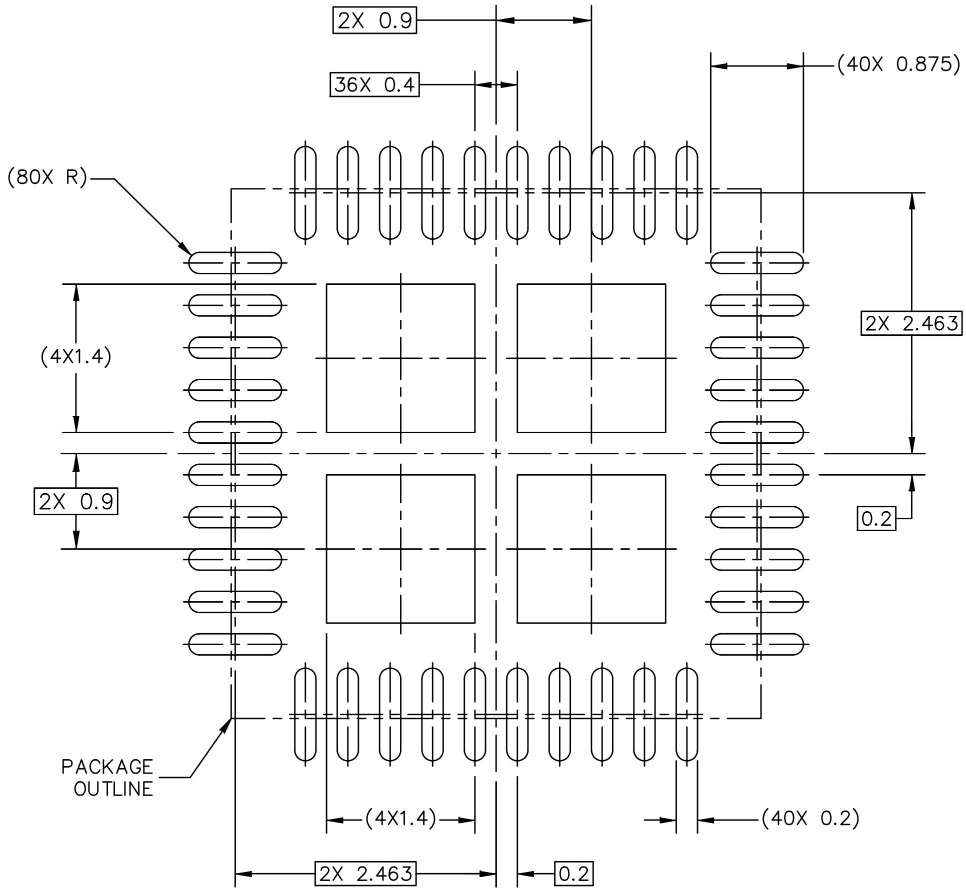


Figure 27. MCX W23 QFN40 – Soldering footprint part 2

H−PQFN−40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369−5



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES − SOLDER PASTE STENCIL

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DATE: 20 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON−JEDEC	DRAWING NUMBER: 98ASA01371D	REVISION: O	

Figure 28. MCX W23 QFN40 – Soldering footprint part 3

15 Packing information

Default packing for the MCX W23 UK devices is tape and reel with bump 1 in quadrant Q1 (top-left). The taping orientation is shown in Figure 30.

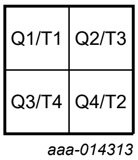

Figure 29. The four tape pocket quadrants

Number of MCX W23 UK samples per tape and reel: 8000 pcs in 13” reel with 4” hub

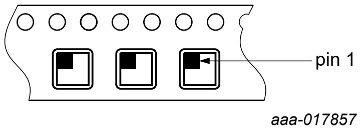

Figure 30. MCX W23UK Tape and reel product orientation

Default packing for the MCX W23 HN devices is tape and reel with pin 1 in quadrant Q2 (top-right). The taping orientation is shown in Figure 31.

Number of MCX W23 HN samples per tape and reel: 6000 pcs in 13” reel with 4” hub

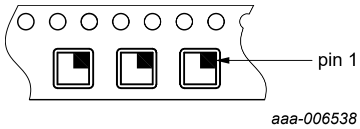

Figure 31. MCX W23HN Tape and reel product orientation

16 Abbreviations

Table 44. Abbreviations

Acronym	Description
AES	advanced encryption standard
BOD	brownout detect
CDM	charged device model
CSP	chip scale package
ESD	electrostatic discharge
GFSK	gaussian frequency shift keying
HBM	human body model
IoT	internet of things
PMC	power management controller
PMU	power management unit
POR	power-on reset
RSSI	received signal strength indication
RX	receiver
SCK	serial clock
SSO	simultaneously switching outputs
TX	transmit
UUID	universal unique identifier
XIP	execute in place
WDT	watchdog timer
WWDT	windowed watchdog timer
HV_SM	high-voltage supply mode
XR_SM	external regulated supply mode

17 References

[1] **UM12312 user manual** — MCX W23 user manual; 2025, NXP Semiconductors

[2] **98ENG06256D_X0_Ext** — SOT2173; WLCSP37, wafer level chip-size package, 37 terminals, 0.35 mm pitch, 2.63 mm x 2.495 mm x 0.49 mm body, 2022, NXP Semiconductors

[3] **SOT1369-5** — HVQFN40, plastic, thermally enhanced very thin quad flat, non-leaded package; 40 terminals; 0.4mm pitch; 5 mm x 5 mm x 0.85 mm body, 8 October 2019, NXP Semiconductors

[4] **AN10439 application note** — Wafer-level chip-scale and fan-out wafer-level package; 2022, NXP Semiconductors

[5] **AN10365 application note** — Surface mount reflow soldering; 2021, NXP Semiconductors

[6] **AN1902 application note** — Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages; 2021, NXP Semiconductors

[7] **UM10204** — I^2C-bus specification and user manual; 1 October 2021, NXP Semiconductors

[8] **AN14658** — Hardware Design Considerations for MCX W23, rev1.0; 2025, NXP Semiconductors

[9] **AN14659** — MCX W23 Power Consumption Analysis, rev1.0; 2025; NXP Semiconductors

[10] **Shelf life policy** — NXP Policy on shelf life; August 2020, NXP Semiconductors (https://www.nxp.com/docs/en/supporting-information/NXP-Shelf-Life-Policy-2020.pdf)

18 Revision history

Table 45. Revision history

Document ID	Release date	Description
MCX W23 v.2.0	20 June 2025	Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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