K32W1480

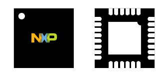
K32W14x Product Family

Ultra-low-power, Highly Secure, Multiprotocol Wireless MCU

Rev. 3 — 12/2022

Data Sheet: Technical Data

K32W1480VFTBT
K32W1480VFTBR



48HVQFN

7 x 7 x 0.85 mm; Pitch 0.5 mm

The K32W14x product family is a low-power, highly secure, single chip multiprotocol wireless MCU that integrates a high performance Bluetooth Low Energy version 5.3 radio and an IEEE 802.15.4 radio supporting Thread, Matter and Zigbee. The K32W14x implements a tri-core architecture to isolate the connectivity, computing and security capabilities.

The multiprotocol radio is energy efficient, supports full simultaneous dual-PAN to enable Thread and Zigbee, and designed for Wi-Fi coexistence. The radio is supported with tested software stacks for Matter, Thread, Zigbee and Bluetooth Low Energy for standalone and hosted applications to enable a range of IoT and industrial applications.

The K32W14x integrates a state-of-the-art, scalable security architecture including Arm® TrustZone®-M, a resource domain controller and an isolated EdgeLock™ Secure Enclave supporting hardware cryptographic accelerators, random number generators, key generation, storage and management, and secure debug. Flash memory contents can optionally be stored as encrypted data and then decrypted on-the-fly enabling protection of sensitive data and algorithms.

The K32W14x implements a flexible power efficient architecture to extend battery life and reduce energy footprint in IoT devices

Application core

- Up to 96 MHz Arm Cortex®-M33 core
- TrustZone-M, IEEE 754 FPU, DSP, MPU, NVIC, SysTick
- 8 KB Code Cache to improve performance and efficiency
- 1 MB flash memory
- 128 KB SRAM
- Secure Boot ROM
- Bluetooth LE Controller stack and transceiver drivers contained in on-chip radio memory, preserving more on-chip system memory for host stack and application space

Target applications

- Smart Home IoT
  - Smart Home environmental, occupancy, and security sensors
  - Home Gateways and Bridges
  - Smart Lighting

EdgeLock Secure Enclave

- Secure boot and debug
- Trusted resource domain controller (TRDC) providing programmable control mechanisms for independent processing domains including embedded memory and peripherals
  - Privilege/user
  - Data only
  - Execute only
  - Read-only access
  - Secure/Non-secure
- Advanced flash access protection
  - Write/Erase protection, Execute only, Data only access control
  - Optional encryption and on-the-fly decryption using a PRINCE XEX block cipher mode
- Hardware encryption and decryption

Table continues on the next page...

- Smart Plugs
  - Access Control
  - HVACs and Thermostats
  - Window Shades
- Industrial/IoT
  - Positioning/Localization
  - Building Control and Monitoring
  - Building HVAC Control
  - Fire and Security
  - Smart Lighting
  - Access Control

Narrow Band Radio Unit

- Dedicated CM3 core running at up to 64 MHz
- 256 kB Flash supporting upgradable software radio
- 88 KB SRAM optimized for link layer support
- IEEE 802.15.4 Radio
  - IEEE 802.15.4–2015 compliant radio
  - –103 dBm 250 kbps Receive Sensitivity
  - Programmable Transmit Output Power up to +10 dBm
  - Improved Enhanced ACK timing support in the 802.15.4 hardware which enables synchronized broadcasts to a larger number of sleepy end devices – for example, synchronous window blinds actuation
  - Supports Dual PAN which allows a single radio to participate in two 802.15.4 Personal Area Networks
  - Modulation Types: 2 Level FSK, GFSK, MSK, GMSK
  - Single ended bidirectional RF port
  - Low external component counts for low cost, small form-factor designs
- Bluetooth Low Energy radio core
  - Up to 24 simultaneous connections
  - –106 dBm 125 kbps Long Range Receive Sensitivity
  - –102 dBm 500 kbps Long Range Receive Sensitivity

- Symmetric Key Encryption
  - AES-128/192/256
  - ECB, CBC, CFB, OFB, CTR, GCM, CMAC, and CCM Modes
  - ChaCha20
- Asymmetric Key Encryption
  - RSA-2048/3072/4096
  - ECC NIST P–192/224/256/384/521
  - Curve25519
- Key Exchange Algorithms
  - ECDH(E)
  - SPAKE2+
  - JPAKE
- Digital Signature Algorithms
  - ECDSA
  - Ed25519
- Hash Algorithms
  - SHA2-224/256/384/512
  - Poly1305

- Secure key generation, storage, and management
- Pseudo (PRNG) and True Random Number Generator (TRNG) with 512-bits entropy supporting NIST SP 800-90A and SP 800-90B
- Support for secure over-the-air (OTA) firmware updates
- Four digital tamper pins with optional interrupt and seconds timestamp upon trigger
- Universally Unique ID (UUID) programmed by NXP during factory programming
- 24-bit unique IEEE media access control (MAC) subaddress
- Factory Root of Trust programming

Low-power consumption (DCDC 3.6 V, 25 ºC)

- Typical active core current: < 5.3 mA at 96 MHz (< 55 µA/MHz)
- Transceiver current (DC-DC buck mode, 3.3 V supply)
  - Typical RX: 4.7 mA
  - Typical TX at 0 dBm: 4.6 mA

Table continues on the next page...

- — –97.5 dBm 1 Mbps Receive Sensitivity
- — –95 dBm 2 Mbps Receiver Sensitivity
- — Programmable Transmit Output Power up to +10 dBm
- — Data Rates: 125 kbps, 500 kbps, 1 Mbps, and 2 Mbps
- — Modulation Types: 2 Level FSK, GFSK, MSK, GMSK
- — Integrated memories in radio containing Bluetooth LE Controller Stack and radio drivers
- — On-chip balun with single ended bidirectional RF port
- — Low external component counts for low cost, small form-factor designs

Safety

- Memory Protection Unit (MPU)
- Register write protection
- Illegal memory access
- Flash area protection
- SRAM Error Correction Code (ECC) and SRAM parity error check
- Clock Frequency Accuracy Measurement Circuit (CAC) using Signal Frequency Analyzer (SFA) module
- Cyclic Redundancy Check (CRC) calculator
- Two internal, independent, and one external watchdog timers
- Clock loss detection
- Main oscillator stop detection (Loss of lock detection)
- Low voltage / high voltage detection

System peripherals

- DC/DC converter supporting buck and bypass operating modes
- Asynchronous DMA controller with per channel access permissions (secure/non-secure)
- Two internal and one external watchdog monitors
- Nested vectored interrupt controller
- Wakeup unit for power down modes

Analog modules

- — Typical TX at 10 dBm: 18.7 mA
- Less than 3 µA in Power-down mode with real-time clock (RTC) active and 32 KB SRAM retention
- Less than 1.5 µA in Deep Power-down mode with RTC active
- Multiple power-down modes supporting currents as low as 300 nA
- Ultra-low leakage Smart Power Switch with less than 100 nA sleep current with exit from internal timer or GPIO.

Clocks

- 32 MHz RF crystal oscillator
- 32.768 kHz crystal oscillator
- Internal 192 MHz high frequency free running oscillator providing 48/64/96 MHz clock
- Internal low frequency free running oscillator providing 6 MHz clock
- Internal low-power free running oscillator providing 32 kHz clock

Communication interfaces

- Two Low Power UART (LPUART) modules
- Two Low Power SPI modules and one MIPI-I3C module
- Two Low Power I2C (LPI2C) modules supporting the System Management Bus (SMBus) Specification, version 2
- One programmable FlexIO module supporting emulation of UART, I2C, I2S, SPI, Camera IF, LCD RGB, PWM/ Waveform generation

Timers

- One 2-channel 32-bit timers (LPTPM)
- Two 6-channel 32-bit timers (LPTPM) with PWM capability and DMA support
- Two 32-bit low-power timers (LPTMR) or pulse counters with compare features
- 4-channel 32-bit low-power periodic interrupt timer (LPIT) with DMA support
- One 56-bit timestamp timer
- 32-bit seconds real time counter (RTC) with 32-bit alarm and independent power supply
- Signal frequency analyzer (SFA) provides facilities for measurement of clock period/frequency as well as time between triggers

Table continues on the next page...

- 16-bit single ended SAR Analog-to-digital converter (ADC) up to 2 Msps
- Two 6-bit High-speed analog comparators (CMP) with 8-bit digital-to-analog converter (DAC)
- 1.0 V to 2.1 V Voltage Reference (Vref)

Operating characteristics

- Temperature range (ambient): –40 °C to 105 °C
- Temperature range (junction): –40 °C to 125 °C
- DC/DC voltage range: 1.71 V to 3.6 V
- Bypass voltage range: 1.71 V to 3.6 V

Input supply voltage options:

- Integrated DCDC regulator 1.71 V–3.6 V providing power to Core_LDO regulator, SYS_LDO regulators, and Radio
- Integrated Core_LDO regulator 1.2 V–3.6 V powering the core digital domain
- Integrated SYS_LDO regulator 1.71 V to 3.6 V powering the SYS domain
- DCDC and Core_LDO regulators can support bypass modes
- Radio Analog: 1.2 V–3.6 V
- Radio PA: 0.9 V–2.4 V

Human Machine Interface modules

- General-purpose input/output (GPIO)

Table 1. Ordering Information

Part Number	Packaging Type	Protocol	Memory (Flash/ RAM)	Packages	Qualification
K32W1480VFTBT	Tray	Bluetooth LE 5.3, Thread, Zigbee, Matter	1 MB/128 KB	7x7 48-pin HVQFN	Industrial –40 °C to + 105 °C (T_A)
K32W1480VFTBR	Tray and Reel				

Table 2. Device Revision Number

Device Mask Set Number	SIM_SDID[REVID]
P43C	0b10

Table 3. Related Resources

Type	Description	Resource
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K32W1480RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KW45_K32W1_2P43C
Package drawing	Package dimensions are provided in package drawings.	• 48 HVQFN:SOT619-17(D)

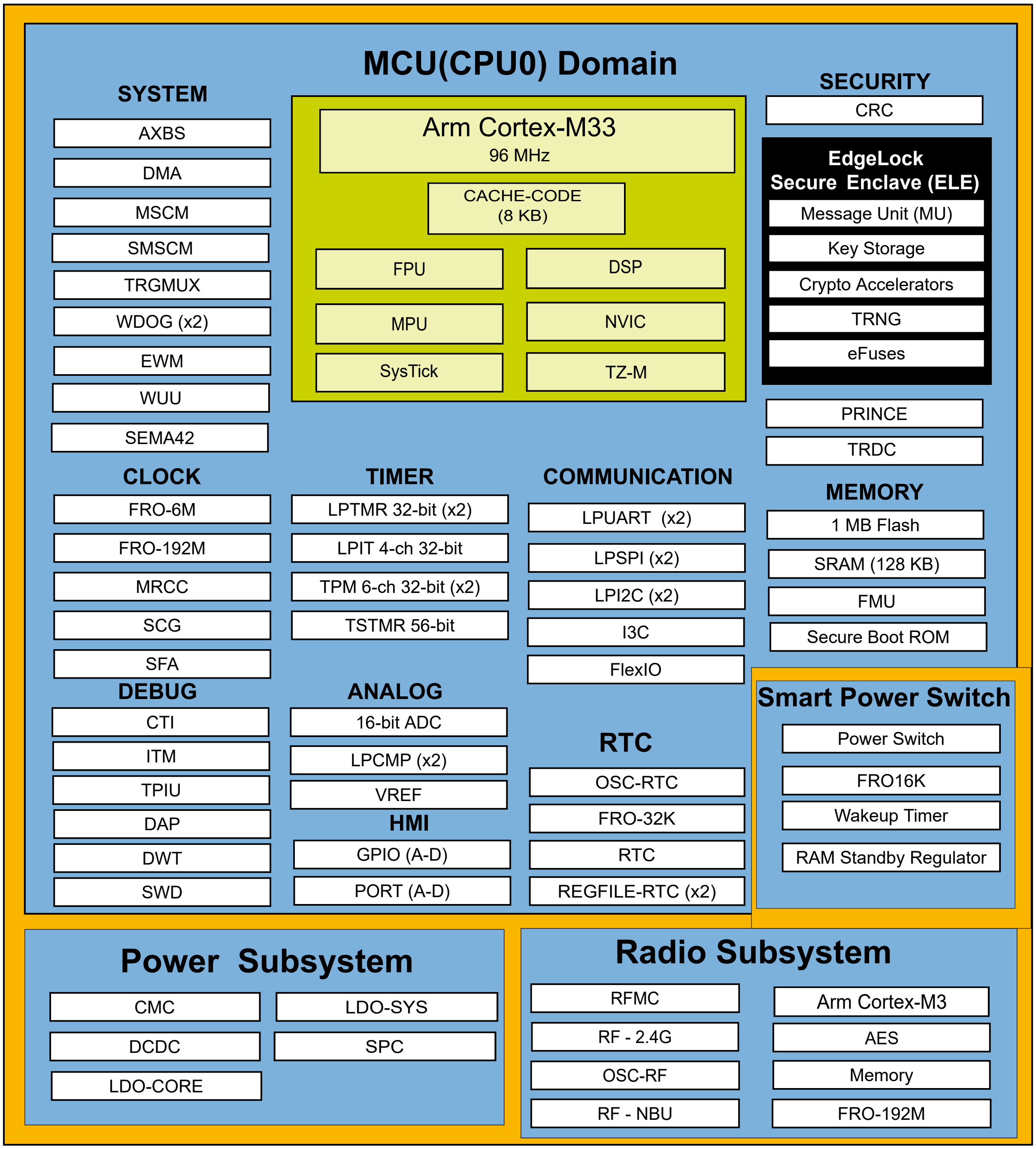


Figure 1. K32W1480 block diagram

Contents

1 Ratings

1.1 Thermal handling ratings

Table 4. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 5. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD and Latch-Up Ratings

Table 6. ESD and Latch-Up Ratings

Description	Rating	Notes
Electrostatic discharge voltage, human body model	±2000 V	1
Electrostatic discharge voltage, charged-device model (corner pins and antenna pin excluded)	±500 V	2
Electrostatic discharge voltage, charged-device model (corner pins)	±750 V	
Electrostatic discharge voltage, charged-device model (antenna pin)	±250 V	
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	3

1. Determined according to JEDEC Standard JS-001-2017, *For Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBM) - Component Level*.
2. Determined according to JEDEC Standard JS-002-2018, *For Electrostatic Discharge (ESD) Sensitivity Testing, Charged-Device Model (CDM) - Device Level* .
3. Determined according to JEDEC Standard JESD78F, *IC Latch-Up Test*.

1.4 Voltage and current maximum ratings

Table 7. Voltage and current maximum ratings

Symbol	Description	Min.	Max.	Unit
VDD_CORE	Supply voltage for most digital domains	–0.3	1.26	V
VDD_SYS	Supply voltage for PMC, EFUSE, SRTC, and FROs	–0.3	1.98 [1]	V

Table continues on the next page...

Table 7. Voltage and current maximum ratings (continued)

Symbol	Description	Min.	Max.	Unit
VDD_DCDC	Supply voltage for DCDC regulator	–0.3	3.63	V
VDD_IO_D	Supply voltage for LDO_SYS regulator, and PortD	–0.3	3.63	V
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	–0.3	3.63	V
VDD_RF	Supply voltage for OSC and radio analog	–0.3	3.6	V
VPA_2P4GHZ	Supply voltage for 2.4 GHz radio power amplifier	–0.3	2.8	V
VDD_IO_ABC	Supply voltage for Port A, Port B, Port C, Flash and CMP0/1	–0.3	3.63	V
VDD_ANA	Supply voltage for ADC, DAC, and VREF	–0.3	3.63	V
V_{IN}	Port input voltage	–0.3	3.63 [2]	V
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA

1. The part supports 2.75 V for up to 20 s over lifetime to allow fuse programming
2. The Max. of the V_{IN} cannot be greater than the voltage applied to the VDD_IO_*x*.

1.5 Required Power-On-Reset (POR) Sequencing

When VDD_CORE is supplied by one of the internal regulators, VDD supply inputs can be powered up in any order. VDD supply inputs on power-up must not exceed VDD voltage maximums.

When powering VDD_CORE with an external supply, VDD_CORE must not be enabled until VDD_IO_ABC ≥ 1.65 V, as shown below.

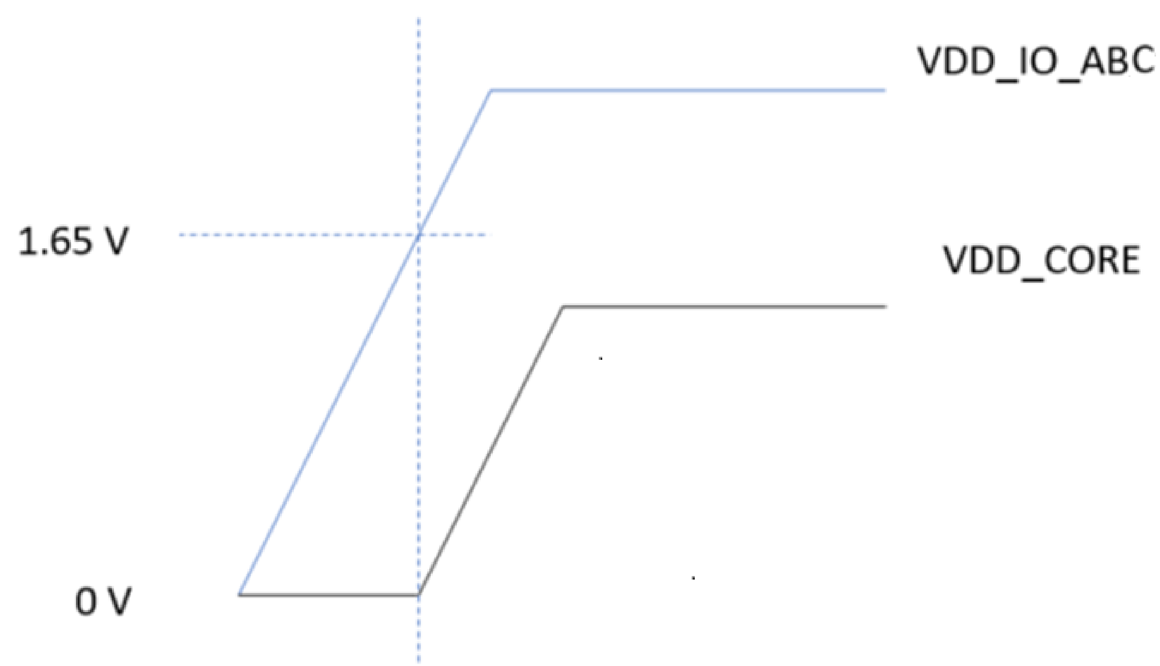


Figure 2. VDD_CORE/VDD_IO_ABC Powering Sequence

1.6 Power Sequence

Table 8. Power Sequence

Symbol	Description	Order in sequence	Notes
VDD_SWITCH	Smart Power Switch input	1	1
VDD_DCDC/ VDD_IO_D	DCDC / PORT D / LDO_SYS regulator input	2	1
VDD_IO_ABC	Ports A, B, and C power rail input	2	1
VDD_ANA	Analog source input	2	1
VDD_LDO_CORE	Core power rail input	2	1
VDD_RF	RF power rail input	3	1
VPA_2P4GHz	RF PA voltage input	4	1

1. All domains can be powered at the same time. If external sources are used, make sure they start at the same time or they follow the order in the sequence.

2 General

2.1 AC electrical characteristics

Unless specified, propagation delays are measured from the 50 % to the 50 % point, and rise and fall times are measured at the 20 % and 80 % points, as shown in the following figure.

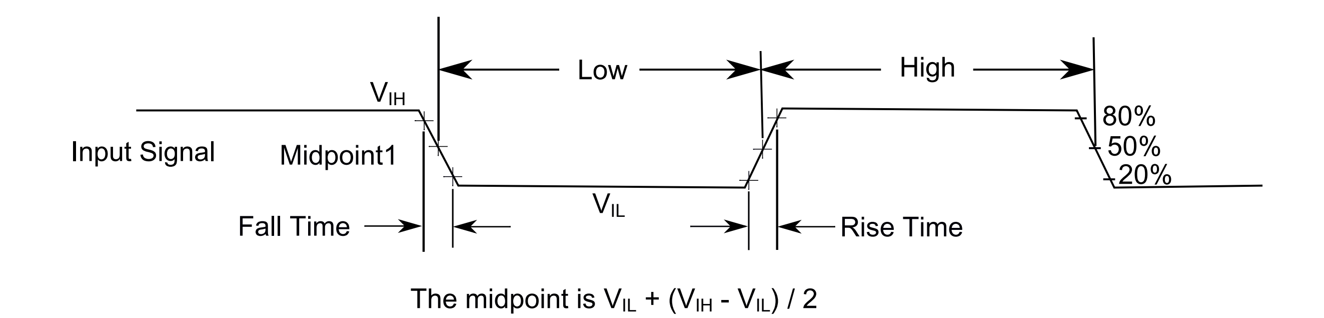


Figure 3. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 9. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
VDD_CORE	VDD_CORE input supply voltage			V	
	Mid Drive (1.0 V) Operation	1.0	1.1		

Table continues on the next page...

Table 9. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Normal Drive (1.1 V) Operation	1.04	1.21		
	Safe-Mode Voltage (1.15 V) Operation	1.04	1.21		
VDD_SYS	Supply voltage for System Voltage Domain • Normal mode • Fuse Programming	1.8 2.25	1.98 2.75	V	
VDD_DCDC	Supply voltage DCDC regulator	1.8	3.6	V	1
VDD_IO_D	Supply voltage for LDO_SYS regulator, PortD	1.86	3.6	V	2
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	1.25	3.6	V	
VDD_RF	Supply voltage for OSC and radio analog	1.175	3.6	V	
VPA_2P4GHz	Supply voltage for 2.4 GHz radio power amplifier	0.9	2.4	V	
VDD_IO_ABC	Supply voltage for PortA, PortB, Port C, and CMPs	1.71	3.6	V	3
VDD_ANA	Supply voltage for ADC, DAC, and VREF	1.71	3.6	V	
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 1.71 V ≤ VDD_IO_ABC ≤ 3.6 V • 1.86 V ≤ VDD_IO_D ≤ 3.6 V	0.7 × VDD_IO_ABC 0.7 × VDD_IO_D	— —	V	4
V_{IL}	Input low voltage • 1.71 V ≤ VDD_IO_ABC ≤ 3.6 V • 1.86 V ≤ VDD_IO_D ≤ 3.6 V	— —	0.3 × VDD_IO_ABC 0.3 × VDD_IO_D	V	4
V_{HYS}	Input hysteresis	0.1 × VDD_IO_*X*	—	V	
I_{ICIO}	IO pin DC injection current — single pin • V_{IN} < VSS – 0.3 V (negative current injection) • V_{IN} > VDD + 0.3 V (positive current injection)	0 —	— 0	mA	5, 6
V_{ODPU}	Open drain pullup voltage level	VDD_IO_*X*	VDD_IO_*X*	V	7

1. If DCDC is unused, then input supply should be tied to GND through a 10 kΩ resistor.
2. When LDO_SYS is bypassed, the input supply voltage is 1.8 V to 1.98 V and VDD_IO_D must be externally connected to VDD_SYS
3. If none of the PortA, PortB, and PortC pins are being used, then the VDD_IO_ABC can be left floating.
4. VIH and VIL for PTD0 are based of VDD_SYS instead of VDD_IO_D

5. All I/O pins are internally clamped to VSS and VDD_IO_*x* through an ESD protection diode. If V_{IN} is greater than VDD_IO_x_MIN(= VSS – 0.3 V) or is less than VDD_IO_x_MAX(= VDD + 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
6. This device does not allow pin injection current. User must ensure that VIN is kept within the Voltage Maximum Ratings.
7. Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD_IO_*X* as appropriate.

2.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD_IO_ABC
- VDD_CORE
- VDD_SYS

For VDD_SYS, it has Power-on-reset (POR) power supervisor circuits.

Table 10. VDD_IO_ABC supply HVD, LVD, and POR Operating Ratings

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{HVDH\_IO\_ABC}$	VDD_IO_ABC Rising high-voltage detect threshold	3.730	3.810	3.890	V	
$V_{HVDH\_HYS\_IO\_ABC}$	VDD_IO_ABC High-voltage inhibit reset/recover hysteresis	—	38	—	mV	
$V_{LVDH\_IO\_ABC}$	VDD_IO_ABC Falling low-voltage detect threshold - high range	2.567	2.619	2.673	V	
$V_{LVDH\_HYS\_IO\_ABC}$	VDD_IO_ABC Low-voltage inhibit reset/recover hysteresis - high range	—	27	—	mV	
$V_{LVDL\_IO\_ABC}$	VDD_IO_ABC Falling low-voltage detect threshold - low range	1.618	1.651	1.684	V	
$V_{LVDV\_HYS\_IO\_ABC}$	VDD_IO_ABC Low-voltage inhibit reset/recover hysteresis - low range	—	20	—	mV	

Table 11. VDD_CORE supply HVD and LVD Operating Ratings

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVD_CORE}	VDD_CORE Rising high-voltage detect threshold (HVD assertion) Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.15 V (safe mode LVD)	1.230	1.257	1.285	V	1
$V_{HVD\_HYS\_CORE}$	VDD_CORE High-voltage inhibit reset/recover hysteresis Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.15 V (safe mode LVD)	—	14	—	mV	1

Table continues on the next page...

Table 11. VDD_CORE supply HVD and LVD Operating Ratings (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVD_CORE}	VDD_CORE Falling low-voltage detect threshold (LVD assertion) Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.15 V (safe mode LVD)	0.944 0.989 1.043	0.963 1.009 1.064	0.983 1.029 1.086	V	
$V_{LVD\_HYS\_CORE}$	VDD_CORE Low-voltage inhibit reset/ recover hysteresis Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.15 V (safe mode LVD)	— — —	14 14 17	— — —	mV	

1. Same value applies to all conditions.

Table 12. VDD_SYS supply HVD and LVD Operating Ratings

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVD_SYS}	VDD_SYS Rising high-voltage detect threshold (HVD assertion) Target VDD_SYS = 1.8 V Target VDD_SYS = 1.9 V (safe mode LVD)	2.035 2.035	2.077 2.077	2.120 2.120	V	1
$V_{HVD\_HYS\_SYS}$	VDD_SYS High-voltage inhibit reset/recover hysteresis	—	22	—	mV	
V_{POR_SYS}	Falling VDD_SYS POR detect voltage (POR assertion)	0.8	1.0	1.5	V	
V_{LVD_SYS}	VDD_SYS Falling low-voltage detect threshold (LVD assertion) Target VDD_SYS = 1.8 V Target VDD_SYS = 1.9 V (safe mode LVD)	1.616 1.700	1.649 1.735	1.683 1.770	V	
$V_{LVD\_HYS\_SYS}$	VDD_SYS Low-voltage inhibit reset/recover hysteresis	—	19	—	mV	
V_{BG}	Bandgap voltage reference voltage	—	1.0	—	V	

1. When fuses are being programmed VDD_SYS is raised to 2.5 V nominal. This is outside the HVD bounds, so HVD detection for VDD_SYS must be disabled when programming fuses

2.2.3 Voltage and current operating behaviors

Table 13. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive strength					1

Table continues on the next page...

Table 13. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OH} = 4 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OH} = 2.5 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OH} = 2.5 mA	VDD_IO_*X* – 0.5	—	—	V	
V_{OH}	Output high voltage — High drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OH} = 6 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OH} = 3.75 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OH} = 3.75 mA	VDD_IO_*X* – 0.5	—	—	V	1,2
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — Normal drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OL} = 4 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OL} = 2.5 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OH} = 2.5 mA	—	—	0.5	V	1,3
V_{OL}	Output low voltage — High drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OL} = 6 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OL} = 3.75 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OL} = 3.75 mA	—	—	0.5	V	1,3,2
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	—	1	μA	4
I_{IN}	Input leakage current (per pin) at 25 °C	—	—	0.025	μA	4
I_{IN}	Input leakage current (total all pins) for full temperature range	—	—	41	μA	4
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	1	μA	
R_{PU}	Internal pullup resistors	33	50	75	kΩ	
R_{PU} (I3C)	Internal pullup resistors	1.1	2	2.833	kΩ	5
R_{PD}	Internal pulldown resistors	33	50	75	kΩ	
R_{HPU}	High-resistance pullup option (PORTx_PCRy[PV] = 1)	0.67	—	1.5	MΩ	6
R_{HPD}	High-resistance pulldown option (PORTx_PCRy[PV] = 1)	0.67	—	1.5	MΩ	6

1. When setting DSE1=1, the same VOH / VOL is met with IOH / IOL doubled.
2. RTC signals are always configured in high drive mode
3. Open drain outputs must be pulled to VDD_IO_*X*.
4. Measured at VDD_IO_*X* = 3.6 V.
5. Only I3C pins support this option
6. Only Port D pins support this option.

2.2.4 On-chip regulator electrical specifications

2.2.4.1 DCDC converter specifications

Table 14. DCDC Converter Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD_DCDC}	DCDC input voltage	1.71	—	3.6	V	
V_{OUT_DCDC}	DCDC output voltage	1.25	—	2.5	V	1, 2
I_{LOAD}	DCDC load current • Normal drive strength • Low drive strength • SPC_DCD_CFG[FREQ_CNTRL_ON]=1	 — — —	 — — —	 105 15 45	 mA mA mA	1, 3
LX	DCDC inductor value	0.47	1	2.2	µH	4
ESR	External inductor equivalent series resistance	—	110	—	mΩ	5
C_{OUT}	DCDC capacitance value	6	22	30	µF	6
V_{RIPPLE}	DCDC voltage ripple • In normal drive strength • In low drive strength	 — —	 1 25	 — —	 % mV	
f_{burst}	DCDC burst frequency	3	5	8	MHz	7
f_{burst_acc}	DCDC burst frequency accuracy	—	10	—	%	7

1. The system DCDC converter generates 1.8 V at DCDC_LX by default. The DCDC can be used to power VDD_RF, VDD_LDO_CORE, and external components as long as the max I_{LOAD} is not exceeded.
2. The VDD_DCDC input supply to DCDC must be at least 500 mV higher than the desired output at DCDC_LX.
3. The maximum load current during boot up shall not exceed 60 mA.
4. Recommended inductor value is 1 µH to 1.5 µH. If the inductor is < 1 µH, the DCDC efficiency is not guaranteed
5. The maximum recommended ESR is 250 mΩ (not a hard limit).
6. The variation in capacitance of the capacitor at DCDC_LX due to aging, temperature, and voltage degradation must not exceed the Min./Max. values.
7. FREQ_CNTRL_ON = 1.

DCDC Efficiency plots

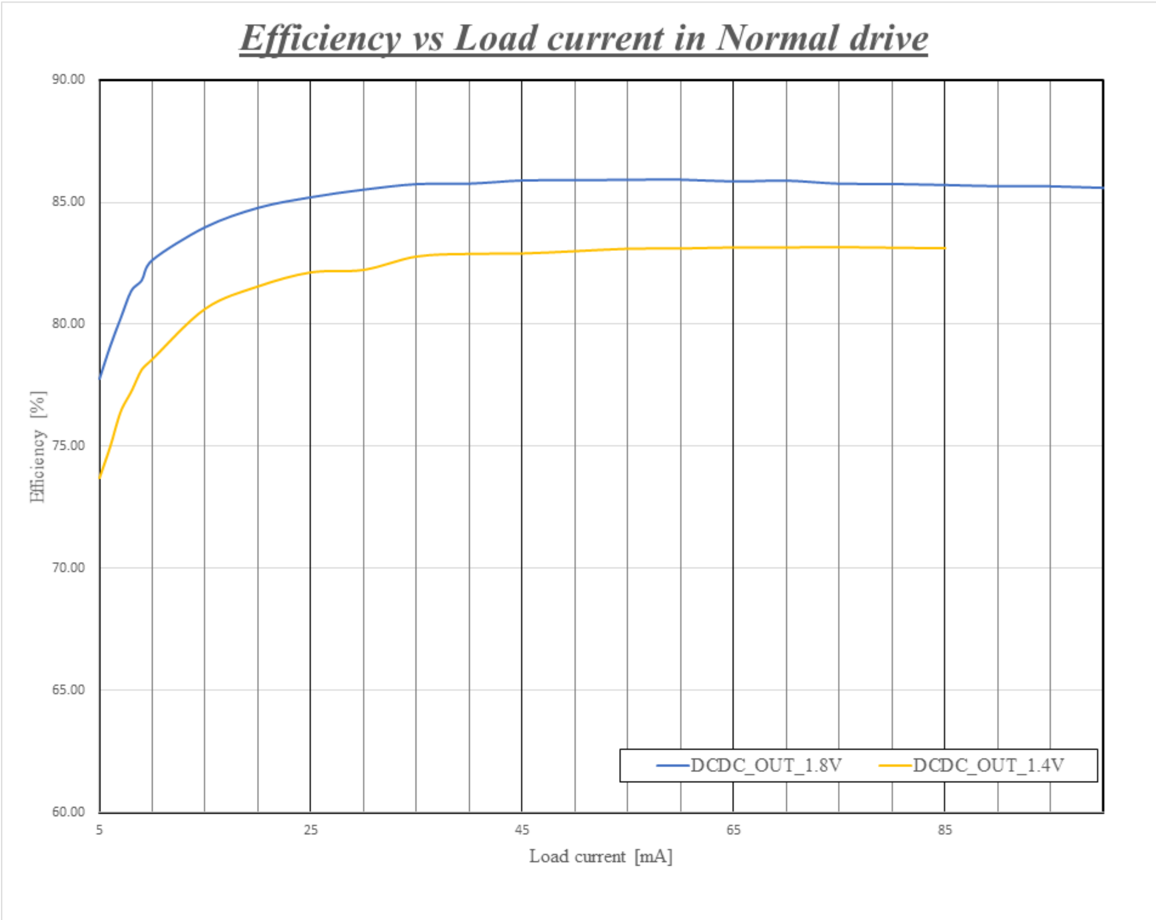


Figure 4. Efficiency vs Load current in Normal drive

Figure 5. Efficiency vs Load current in Low-power drive

2.2.4.2 LDO_SYS electrical specifications

Table 15. LDO_SYS electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_IO_D	LDO_SYS input supply voltage • LDO_SYS input supply voltage (Regulation mode) • LDO_SYS input supply voltage (Bypass mode) • Fuse programming mode	 1.86 1.8 2.75	 — — —	 3.6 1.98 3.6	V	1
VOUT_SYS	LDO_SYS regulator output voltage • Normal drive mode • Fuse Programming mode	 1.71 2.25	 1.8 2.5	 1.98 2.75	V	2,3,4,5
I_{LOAD}	LDO_SYS maximum load current					

Table continues on the next page...

Table 15. LDO_SYS electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• Normal drive mode • Low drive mode • Fuse programming mode	— — —	— — —	50 2 40	mA mA mA	
I_{DD}	LDO_SYS power consumption • Normal drive mode • Low drive mode	 — —	 100 70	 — —	 µA nA	6
C_{OUT}	External output capacitor	—	1.5	10	µF	
C_{DEC}	External output decoupling capacitor	—	0.1	—	µF	
ESR	External output capacitor equivalent series resistance	—	30	—	mΩ	
I_{INRUSH}	LDO_SYS inrush current	—	—	120	mA	7

1. Regulator will automatically switch to passthrough (means the regulator driver is fully ON) with the supply is below 1.95 V.
2. The LDO_SYS converter generates 1.8 V by default at VOUT_SYS. VOUT_SYS can be used to power VDD_SYS, VDD_RF, VDD_IO_*X*, VDD_ANA, and external components as long as the max I_{LOAD} is not exceeded.
3. VOUT_SYS and VDD_SYS are connected together.
4. VDD_IO_D must be at least 150 mV higher than the desired VOUT_SYS.
5. LDO_SYS can be used to program efuse and in this configuration the output voltage can range between 2.25 V and 2.75 V
6. In normal drive strength, LDO_SYS draws ~100 µA for every 20 mA of load current.
7. This is for 1.5 µF external output capacitor. If the capacitor has 10 µF value, this value should be 300 mA instead.

2.2.4.3 LDO_CORE electrical specifications

Table 16. LDO_CORE electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_LDO_CORE	LDO_CORE input supply voltage	1.25	—	3.6	V	1, 2
VOUT_CORE	LDO_CORE regulator output voltage • Normal drive strength • Low drive strength	1.0 1.0	— —	1.15 1.15	V	
I_{LOAD}	LDO_CORE max load current • Normal mode - VDD_LDO_CORE ≥ 1.5 V • Normal mode - VDD_LDO_CORE < 1.5 V • Low-power mode - VDD_LDO_CORE ≥ 1.5 V • Low-power mode - VDD_LDO_CORE < 1.5 V	 — — — —	 — — — —	 60 30 5 5	mA	

Table continues on the next page...

Table 16. LDO_CORE electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD}	LDO_CORE current consumption				µA	3
	• Normal drive strength - VDD_LDO_CORE ≥ 1.5 V	—	—	150		
	• Normal drive strength - VDD_LDO_CORE < 1.5 V	—	—	75		
	• Low drive strength - VDD_LDO_CORE ≥ 1.5 V	—	—	0.05		
	• Low drive strength - VDD_LDO_CORE < 1.5 V	—	—	0.05		
I_{INRUSH}	LDO_CORE inrush current	—	—	5 x I_{LOAD}	mA	

1. To bypass LDO_CORE, tie VDD_LDO_CORE to VDD_CORE
2. The VDD_LDO_CORE input supply must also be at least 250 mV higher than the desired output at VOUT_CORE.
3. In normal drive strength, LDO_CORE draws ~40 µA for every 20 mA of load current. In low drive strength, LDO_CORE draws ~50 nA for every 100 µA of load current.

Table 17. LDO_CORE external device electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_{OUT}	External output capacitor	3.7	4.7	10	µF	
C_{DEC}	External output decoupling capacitor	—	0.1	—	µF	
ESR	External output capacitor equivalent series resistance	—	10	—	mΩ	

2.2.5 Smart power switch

NOTE

SWITCH_WAKEUP_B pad is internally pulled up to the switch input through a resistor, it can be pulled down to wake up the smart power switch. To generate a valid internal wake-up signal successfully, maximum value of SWITCH_WAKEUP_B pulldown voltage is 0.7 V, duration time should be larger than 1 µs.

Table 18. Smart power switch

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{supply}	Input voltage (VDD_SWITCH)	1.9	—	3.6	V	
R_{ON}	Switch resistor at 'on' state	—	—	3	Ω	
I_{load}	Load current	—	—	40	mA	
$I_{leakage1}$	Typical leakage current when Vsupply = 2.7 V, 25 °C	—	4	—	nA	
$I_{leakage2}$	Maximum leakage current when Vsupply = 3.3 V	—	—	1	µA	

NOTE

If battery (with peak current limitation) is used to power VDD_SWITCH which power rest of chip supplies, it is not recommended to go to deep-power-down mode constantly. Because DCDC startup will introduce big peak current when wakeup.

2.2.6 Power mode transition operating behaviors

All specifications in the following table assume that the default clock configuration will be 96 MHz CPU_CLK/BUS_CLK and 24 MHz slow clock.

Table 19. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{SLEEP}	SLEEP → ACTIVE	—	8.95	9.4	μs	
t_{DSLEEP}	DEEP SLEEP → ACTIVE	—	9.6	10.1	μs	
t_{PWDN}	POWER DOWN → ACTIVE	233.86	234.33	234.59	μs	
t_{DPWDN}	Deep Power DOWN → ACTIVE	747.59	816.12	835.00	μs	

2.2.7 Power consumption operating behaviors

The K32W device has multiple power supplies that can be connected in different configurations, where the total current consumption of the device is the accumulative result of each individual power supply's current consumption. All current consumption specifications are measured with a bench power supply that provides externally the different voltage levels required by each power domain in the corresponding KW45 power mode configuration.

When calculating the total MCU current consumption, the following considerations should be made:

- Specifications below only include power for the MCU itself
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered
- Efficiency of regulators (on-chip or off-chip) used to generate supply voltages should be considered

The maximum values stated in the following sections represent characterized results equivalent to the mean plus three times the standard deviation (mean + 6 sigma).

2.2.7.1 Power Consumption Operating Behaviors

Table 20. Power Consumption Operating Behaviors

	DCDC Power Configuration						
Mode#	Symbol	Description	Temp	Typ	Max	Unit	Notes
IDD_ACT 8	IDD_ACT1	Active 1 mode current - DCDC in low strength, Core voltage = 1.0 V, all peripherals disabled, executing while(1) from FLASH in both CM33 at 48 MHz and NBU at 32 MHz	–40 °C	4.9	–	mA	1,2
			25 °C	5.1	–		
			85 °C	5.4	–		
			105 °C	5.8	–		

Table continues on the next page...

Table 20. Power Consumption Operating Behaviors (continued)

IDD_ACT 15	IDD_ACT2	Active 2 mode current - DCDC in normal strength, Core voltage = 1.1 V, all peripherals enabled, executing while(1) from FLASH in both CM33 at 48 MHz and NBU at 32 MHz	25 °C	5.5	–		2,3
IDD_ACT 16	IDD_ACT3	Active 3 mode current - DCDC in normal strength, Core voltage = 1.1 V, all peripherals enabled, executing while(1) from FLASH in both CM33 at 48 MHz and NBU at 32 MHz	25 °C	8.8	–		2,3
IDD_ACT 17	IDD_ACT4	Active 4 mode current - DCDC in normal strength, Core voltage = 1.1 V, all peripherals disabled, executing while(1) from FLASH in both CM33 at 96 MHz and NBU at 32 MHz	25 °C	5.4	–		2,3
IDD_CM 1	IDD_CM1	CoreMark 1 mode current - DCDC in normal strength, Core voltage = 1.1 V, all peripherals disabled, executing CoreMark® code from FLASH in CM33 at 96MHz, NBU in sleep mode.	–40 °C	6.0	–	mA	2,3
			25 °C	6.2	–		
			85 °C	6.4	–		
			105 °C	7.7	–		
IDD_CM 22	IDD_CM2	CoreMark 2 mode current - DCDC in low strength, Core voltage = 1.0 V, all peripherals disabled, executing CoreMark® code from FLASH in	25 °C	4.6	–		1,2

Table continues on the next page...

Table 20. Power Consumption Operating Behaviors (continued)

		CM33 at 48MHz, NBU in sleep mode.					
IDD_DS1	IDD_DS1	Deep Sleep 1 mode current - All regulators in low-power mode, all RAM retained, all peripherals, NBU, and EdgeLock disabled, OSC32K enabled	–40 °C	3.0	–	µA	4
			25 °C	2.8	–		
			85 °C	12.5	–		
			105 °C	26.2	–		
IDD_DS2	IDD_DS2	Deep Sleep 2 mode current - All regulators in low power, 16 KB of RAM retained, all radio RAM retained, all peripherals, NBU, and Edge Lock disabled, OSC32K enabled	–40 °C	2.9	–	µA	4
			25 °C	2.5	–		
			85 °C	9.2	–		
			105 °C	18.4	–		
IDD_PD2	IDD_PD1	Power Down 1 mode current - All regulators in low power, 16 KB of RAM retained, all radio RAM retained, all peripherals, NBU, and Edge Lock disabled, FRO32K enabled	–40 °C	3.8	–	µA	4
			25 °C	3.4	–		
			85 °C	9.8	–		
			105 °C	18.3	–		
IDD_DPD2	IDD_DPD1	Deep Power Down 1 mode current - LDO_CORE and DCDC off, LDO_SYS in low power, no RAM retained, no radio RAM retained, all peripherals, NBU, and EdgeLock disabled, FRO32K enabled	–40 °C	1.70	–	µA	4
			25 °C	1.2	–		
			85 °C	3.7	–		
			105 °C	7.2	–		
	PMIC Power Configuration						
Mode	**Symbol**	**Description**	**Temp**	**Typ**	**Max**	**Unit**	**Notes**
IDD_ACT14	IDD_ACT5	Active 5 mode current - Core	–40 °C	6.9	–	mA	2,5
			25 °C	7.0	–		

Table continues on the next page...

Table 20. Power Consumption Operating Behaviors (continued)

		voltage = 1.0 V, all peripherals disabled, executing while(1) from FLASH in both CM33 at 48 MHz and NBU at 32 MHz	85 °C	7.7	–		
			105 °C	8.4	–		
IDD_ACT 18	IDD_ACT6	Active 6 mode current - Core voltage = 1.1 V, all peripherals enabled, executing while(1) from FLASH in both CM33 at 48 MHz and NBU at 32 MHz	25 °C	10	–	mA	2, 6
IDD_ACT 19	IDD_ACT7	Active 7 mode current - Core voltage = 1.1 V, all peripherals enabled, executing while(1) from FLASH in both CM33 at 96 MHz and NBU at 32 MHz	25 °C	17	–	mA	2,6
IDD_ACT 20	IDD_ACT8	Active 8 mode current - Core voltage = 1.1 V, all peripherals disabled, executing while(1) from FLASH in both CM33 at 96 MHz and NBU at 32 MHz	25 °C	9.9	–	mA	2,6
IDD_CM 13	IDD_CM3	CoreMark 3 mode current - Core voltage = 1.1 V, all peripherals disabled, executing CoreMark® code from FLASH in CM33 at 96 MHz, NBU in sleep mode.	–40 °C	10.7	–	mA	2,6
			25 °C	10.8	–		
			85 °C	11.9	–		
			105 °C	12.7	–		
IDD_CM 23	IDD_CM4	CoreMark 4 mode current - Core voltage = 1.0 V, all peripherals disabled, executing CoreMark® code from FLASH in	25 °C	6.9	–	mA	2,5

Table continues on the next page...

Table 20. Power Consumption Operating Behaviors (continued)

		CM33 at 48MHz, NBU in sleep mode.					
IDD_DS5	IDD_DS3	DeepSleep 3 mode current - all RAM retained, all peripherals, NBU, and EdgeLock disabled, OSC32K enabled	–40 °C	7.1	–	µA	[5]
			25 °C	5.4	–		
			85 °C	24.9	–		
			105 °C	53.2	–		
IDD_DS6	IDD_DS4	DeepSleep 4 mode current - 16 KB of RAM retained, all radio RAM retained, all peripherals, NBU, and Edge Lock disabled, OSC32K enabled	–40 °C	5.4	–	µA	[5]
			25 °C	4.5	–		
			85 °C	17.3	–		
			105 °C	34.9	–		
IDD_PD6	IDD_PD2	PowerDown 2 mode current - 16 KB of RAM retained, all radio RAM retained, all peripherals, NBU, and Edge Lock disabled, FRO32K enabled	–40 °C	12.0	–	µA	[5]
			25 °C	6.5	–		
			85 °C	18.9	–		
			105 °C	34.8	–		
IDD_DPD4	IDD_DPD2	DeepPowerDown 2 mode current - no RAM retained, no radio RAM retained, all peripherals, NBU, and EdgeLock disabled, FRO32K enabled	–40 °C	9.7	–	µA	[5]
			25 °C	2.9	–		
			85 °C	5.8	–		
			105 °C	9.5	–		
	Smart Power Switch						
Mode	**Symbol**	**Description**	**Temp**	**Typ**	**Max**	**Unit**	**Notes**
IDD_SW_DPD2	IDD_SW_DPD1	Smart Power Switch Deep Power Down 2 mode current - All regulators off, 8 KB RAM retained, no radio RAM retained, all peripherals, NBU, and EdgeLock disabled, FRO16K enabled	–40 °C	0.3	–	µA	[7,8]
			25 °C	0.4	–		
			85 °C	2.2	–		
			105 °C	3.3	–		

1. All regulators enabled, 3.3 V supply upstream from the DCDC. DCDC output is 1.8 V, VDD_CORE =1.0. SYS_LDO input=3.3, output = 1.8 V.
2. FRO-192M as clock source

3. All regulators enabled, 3.3 V supply upstream from the DCDC. DCDC output is 1.35V, VDD_CORE =1.1. SYS_LDO input=3.3, output = 1.8 V.
4. All regulators enabled, 3.3 V supply upstream from the DCDC. DCDC output is 1.25V, VDD_CORE =1.0. SYS_LDO input=3.3, output = 1.8V.
5. All regulators are disabled. Voltages are come from external supplies. External 3.3V supply for VDD_SWITCH, VDD_ANA, VDD_IO_ABC and VDD_IO_D/DCDC_IN. External 1.8V supply for VDD_SYS and VDD_RF. External 1.0V supply for VDD_CORE.
6. All regulators are disabled. Voltages are come from external supplies. External 3.3V supply for VDD_SWITCH, VDD_ANA, VDD_IO_ABC and VDD_IO_D/DCDC_IN. External 1.8V supply for VDD_SYS and VDD_RF. External 1.1V supply for VDD_CORE.
7. 8 KB of retained RAM correspond to the last RAM block and is powered by the standby LDO in smart power switch domain
8. External 3.3 V supply to Smart Power Switch. Power switch output connected to DCDC_IN, LDO_SYS, VDD_ANA, VDD_IO_D and VDD_IO_ABC; DCDC output connected to LDO_CORE, VDD_RF

2.2.7.2 SoC Power Consumption

SoC Power Consumption table is as follows:

Table 21. SoC POwer Consumption

CM33	Radio state	DCDC state	Typical Average IC current	Unit
Deep Sleep 2	Rx	Buck (Vdcdc_in =3.3 V)	6.6	mA
Deep Sleep 2	Rx (scan)	Buck (Vdcdc_in =3.3 V)	4.1	mA
Deep Sleep 2	Tx (+0 dBm)	Buck (Vdcdc_in =3.3 V)	5.2	mA
Deep Sleep 2	Tx (+4 dBm)	Buck (Vdcdc_in =3.3 V)	8.7	mA
Deep Sleep 2	Tx (+7 dBm)	Buck (Vdcdc_in =3.3 V)	12.5	mA
Deep Sleep 2	Tx (+10 dBm)	Buck (Vdcdc_in =3.3 V)	19.7	mA
Deep Sleep 2	Rx	Disabled/Bypass	8.7	mA
Deep Sleep 2	Rx (scan)	Disabled/Bypass	6.5	mA
Deep Sleep 2	Tx (+0 dBm)	Disabled/Bypass	11.4	mA
Deep Sleep 2	Tx (+4 dBm)	Disabled/Bypass	13.6	mA
Deep Sleep 2	Tx (+7 dBm)	Disabled/Bypass	19.0	mA
Deep Sleep 2	Tx (+10 dBm)	Disabled/Bypass	22.4	mA

2.2.7.3 Typical power-down mode RAM current adders

The table below shows typical current consumption adders on the VDD_CORE domain for different SRAM configurations. All currents are measured in power-down mode, but RAM adder should be similar for other modes.

Table 22. Typical power-down mode RAM current adders

SRAM array	Non-Secure Start Address	Non-Secure End Address	Size	-40 °C	25 °C	85 °C	105 °C	Unit
CTCM0	0x40000000	0x40001FFF	8 KB	0.061	0.070	1.49	2.44	μA
CTCM1	0x40002000	0x40003FFF	8 KB	0.020	0.026	1.80	2.70	μA
STCM0	0x20000000	0x20003FFF	16 KB	0.142	0.151	2.95	4.68	μA

Table continues on the next page...

Table 22. Typical power-down mode RAM current adders (continued)

SRAM array	Non-Secure Start Address	Non-Secure End Address	Size	-40 °C	25 °C	85 °C	105 °C	Unit
STCM1	0x20004000	0x20007FFF	16 KB	0.176	0.186	3.06	5.02	µA
STCM2	0x20008000	0x2000FFFF	32 KB	0.321	0.362	4.92	8.93	µA
STCM3	0x20010000	0x20017FFF	32 KB	0.207	0.215	3.76	6.17	µA
STCM4	0x20018000	0x20019FFF	8 KB	0.045	0.046	2.02	2.33	µA
STCM5	0x2001A000	0x2001BFFF	8 KB	1.12	1.16	1.33	1.38	µA

2.2.7.4 Low power mode peripheral power consumption adders

The following measurements were performed in DCDC mode with low drive strength configured at 1.25 V. Supply voltage is at 3.3 V

Table 23. Low power mode peripheral power consumption adders

Symbol	Description	Temperature	Unit
		25 °C	
LPTMR	LPTMR peripheral adder measured by placing the device in Deep Power-down mode using the FRO-32K configured for 1 second prescaler with 1 minute match. Include the FRO-32K power consumption.	252.9	nA
LPIT	LPIT peripheral adder measured by placing the device in Sleep mode with Wake Domain place in Sleep. Using FRO6M, configured for a 1 minute match. Does not include selected clock source power consumption.	3.2	µA
TSTMR	TSTMR peripheral adder measured by placing the device in Power-down mode with Wake Domain place in Sleep. Incrementing on the 1MHz clock output from the FRO6M. Does not include the selected clock source power consumption.	4.0	µA
TPM0	TPM0 peripheral adder measured by placing the device in Power-down mode with Wake Domain	4.1	µA

Table continues on the next page...

Table 23. Low power mode peripheral power consumption adders (continued)

	place in Sleep. Using FRO32K configured for output compare generating a 10Hz clock signal. No load is placed on the I/O pin generating the clock signal. Includes the clock source power consumption		
RTC	RTC peripheral adder measured with external 32 kHz OSC enabled with an alarm of 1 minute, by placing the device in Deep Power-down mode. Includes OSC-RTC (32 kHz external crystal) power consumption.	210.7	nA
LPUART1	LPUART1 peripheral adder measured by placing the device in Sleep mode with Wake Domain Sleep. Selected clock source FRO6M as clock source waiting for Rx data at 115200 BR, configuring CC=10b for MRCC_LPUART1. Does not include selected clock source power consumption.	4.2	µA
LPI2C1	LPI2C1 peripheral adder measured by placing the device in Sleep mode configured as Slave with digital glitch filter disabled. Does not include selected clock source power consumption.	3.2	µA
I3C	LPI3C peripheral adder measured by placing the device in Sleep mode with Wake Domain place in Sleep, while configured as slave. Does not include the clock source power	3.3	µA
LPSPI0	LPSPI0 peripheral adder measured by placing the device in Sleep mode with Wake Domain place in Sleep, while configured as Slave in SPI. Does not include	4.0	µA

Table continues on the next page...

Table 23. Low power mode peripheral power consumption adders (continued)

	the clock source power consumption.		
FlexIO	FlexIO peripheral adder measured by placing the device in Sleep mode with Wake Domain Sleep, while Using FRO6M, emulating UART waiting for RX data at 115200 baudrate. Does not include selected clock source power consumption.	3.3	µA
ADC	ADC peripheral adder by placing the device in Sleep mode with Wake Domain place in Sleep. ADC in low power single ended mode using the FRO6M and 10Ksps continuous conversion. Does not include selected clock source power consumption.	4.1	µA
CMP	CMP peripheral adder measured with CMP enabled 8-bit DAC and single input for compare. The device is placed in Sleep mode with Wake Domain place in Sleep. Does not include 6-bit DAC power consumption	3.3	µA
VREF	VREF peripheral adder measured by placing the device in Sleep mode with Wake Domain place in Sleep. Generating a 1.2V reference output voltage	3.9	µA
WDOG	WDOG peripheral adder measured by placing the device in Sleep mode with Wake Domain place in Sleep. The peripheral is configured Using OSC-RTC (External 32kHz) using the longest timeout period possible. Includes the OSC_RTC current consumption	2.8	µA

2.2.8 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

2.2.9 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to https://www.nxp.com/.
2. Perform a keyword search for “EMC design”.

2.2.10 Capacitance attributes

Table 24. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 25. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
VDD_CORE = 1.1 V					
f_{CPU}	CPU clock (CPU_CLK)	—	96	MHz	
f_{BUS}	Bus clock (BUS_CLK)	—	96	MHz	
f_{SLOW}	Slow clock (SLOW_CLK)	—	24	MHz	
VDD_CORE = 1.0 V					
f_{CPU}	CPU clock (CPU_CLK)	—	48	MHz	
f_{BUS}	Bus clock (BUS_CLK)	—	48	MHz	
f_{SLOW}	Slow clock (SLOW_CLK)	—	24	MHz	

NOTE

By default, VDD_CORE = 1.0 V, f_{CPU_CLK}/f_{BUS_CLK} = 32 MHz, f_{SLOW_CLK} = 16 MHz.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPTMR, TPM, LPI2C, LPI3C, LPSPI, or FlexIO functions.

Table 26. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	150	—	ns	

Table continues on the next page...

Table 26. General switching specifications (continued)

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	
External RESET and NMI pin interrupt pulse width — Asynchronous path	330	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise/fall time				
Normal I/O pins				3
• 2.7 ≤ VDD_IO_*x* ≤ 3.6 V				
— Fast slew rate (SRE = 0; DSE = 0)	2.9	7	ns	
— Slow slew rate (SRE = 1; DSE = 0)	6	15	ns	
• 1.71 ≤ VDD_IO_*x* < 2.7 V				
— Fast slew rate (SRE = 0; DSE = 1)	2.4	7	ns	
— Slow slew rate (SRE = 1; DSE = 1)	6.1	20	ns	
I2C/I3C I/O pins				4
• 2.7 ≤ VDD_IO_*x* ≤ 3.6 V				
— Normal drive, fast slew rate (SRE = 0; DSE =)	3	7	ns	
— Normal drive, slow slew rate (SRE = 1; DSE = 0)	6.1	15	ns	
— High drive, fast slew rate (SRE = 0; DSE = 1)	2.8	7	ns	
— High drive, slow slew rate (SRE = 1; DSE = 1)	5.6	15	ns	
• 1.71 ≤ VDD_IO_*x* < 2.7 V				
— Normal drive, fast slew rate (SRE = 0; DSE = 0)	2.8	7	ns	
— Normal drive, slow slew rate (SRE = 1; DSE = 0)	6.4	20	ns	
— High drive, fast slew rate (SRE = 0; DSE = 1)	2.3	7	ns	
— High drive, slow slew rate (SRE = 1; DSE = 1)	5.7	20	ns	
Reset and NMI pins				5
• 2.7 ≤ VDD_IO_*x* ≤ 3.6 V	3.3	6.7	ns	
• 1.71 ≤ VDD_IO_*x* < 2.7 V	4.3	20	ns	

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. Load is 25 pF. Drive strength and slew rate are configured using PORTx_PCRn[DSE] and PORTx_PCRn[SRE].
4. Load is 25 pF for DSE=0 or DSE=1. Load is 50 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].
5. Load is 25 pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 27. Thermal operating requirements

Symbol	Description	Min.	Typical	Max.	Unit	Notes
T_J	Die junction temperature	–40	25	125	°C	
T_A	Ambient temperature	–40	25	105	°C	

2.4.2 Thermal attributes

Table 28. Thermal attributes

Board type	Symbol	Description	48 QFN	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	26	°C/W	
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	1

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 29. SWD timing

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation	—	25	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	20	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
S7	SWD_CLK high to SWD_DIO data valid	—	25	ns
S8	SWD_CLK high to SWD_DIO high-Z	5	—	ns

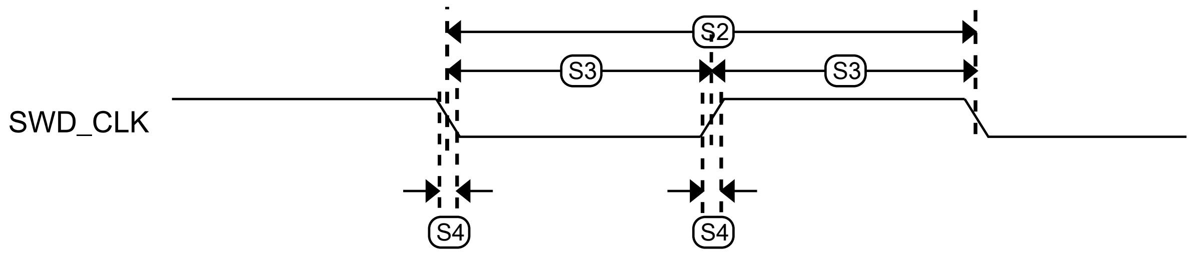


Figure 6. Serial wire clock input timing

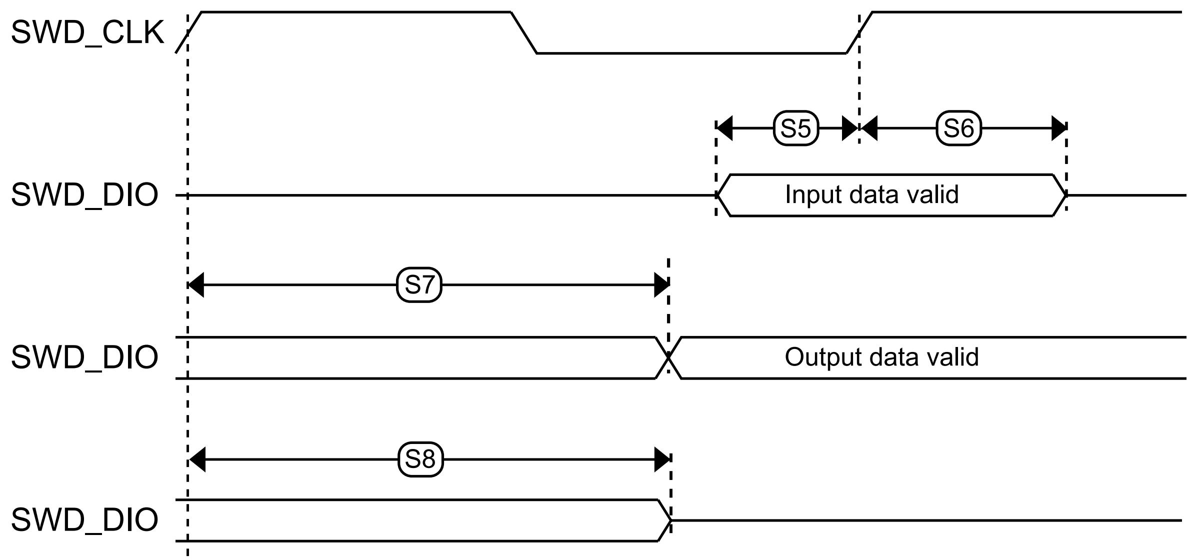


Figure 7. Serial wire data timing

3.2 Clock modules

3.2.1 Reference oscillator specification

This chip is designed to meet targeted specifications with a ±40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

Table 30. Reference Crystal Specification

Symbol	Description	F0 = 32.0 MHz			Unit	Notes
		Min	Typ	Max		
T_A	Operating Temperature	–40	—	105	°C	1
	Crystal frequency tolerance over Aging and Temperature	–33	—	30	ppm	2,3

Table continues on the next page...

Table 30. Reference Crystal Specification (continued)

Symbol	Description	F0 = 32.0 MHz			Unit	Notes
		Min	Typ	Max		
	Oscillator variation	–17	—	20	ppm	4
	Total reference oscillator tolerance for Bluetooth LE applications	–50	—	50	ppm	5
	Total reference oscillator tolerance for IEEE 802.15.4 applications	–40	—	40	ppm	5
C_L	Load capacitance	6	8	10	pF	2,6
C_0	Shunt capacitance	0.469	0.67	0.871	pF	2,6
Cm1	Motional capacitance	1.435	2.05	2.665	fF	2, 6
Lm1	Motional inductance	8.47	12.1	15.73	mH	2,6
Rm1	Motional resistance	—	25	50	Ohms	2
ESR	Equivalent series resistance	—	50	60	Ohms	2, 7
P_d	Maximum crystal drive	—	—	200	µW	2
T_S	Trim sensitivity	6.30	9.00	11.70	ppm/pF	2,6
T_{OSC}	Oscillator Startup Time	—	500	—	µs	8

1. Full temperature range of this device. A reduced range can be chosen to meet application needs.
2. Recommended crystal specification.
3. Combination of frequency stability variation over desired temperature range and frequency variation due to aging over desired lifetime of system.
4. Variation due to temperature, process, and aging of MCU.
5. Sum of crystal initial frequency tolerance, crystal frequency stability and aging, oscillator variation, and PCB manufacturing variation must not exceed this value.
6. Typical is target. 30 % tolerances shown.
7. ESR = Rm1 * (1 + [C_0/C_L])^2.
8. Time from oscillator enables to clock ready. Dependent on the complete hardware configuration of the oscillator.

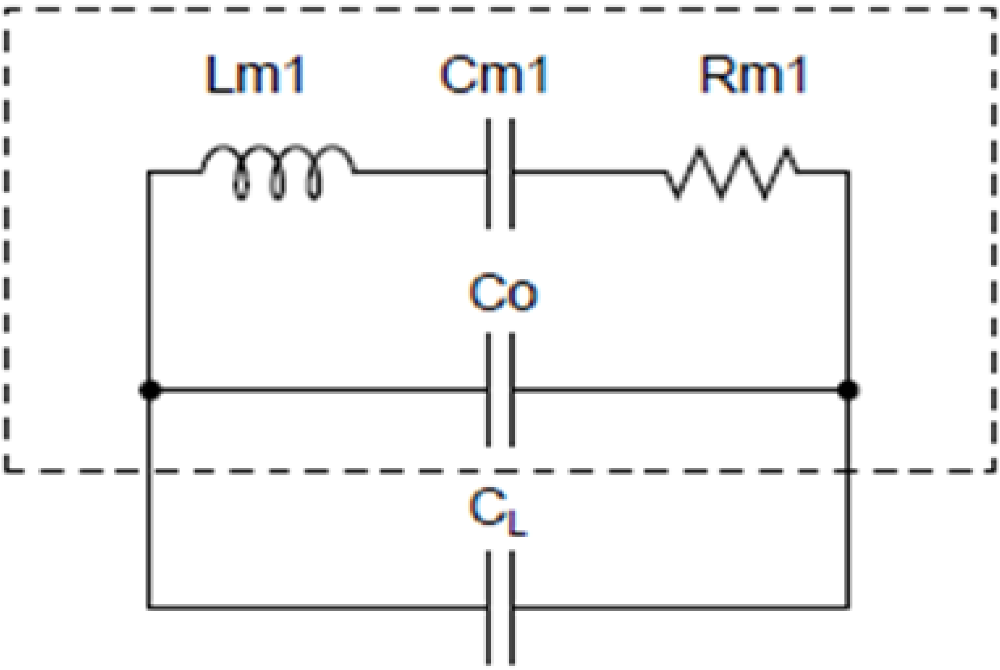


Figure 8. Crystal Electrical Block Diagram

3.2.2 32 kHz oscillator electrical specifications

Table 31. 32 kHz oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_32k}	Crystal frequency	—	32.768	—	kHz	
Tol	Frequency tolerance	—	±100	—	ppm	
Jit_{osc}	Jitter • Period jitter (RMS) • Accumulated jitter over 1 ms (RMS)	 — —	 10 50	 — —	ns	
ESR	Crystal equivalent series resistance	—	—	80/150	kΩ	1
C_{para}	Parasitic capacitance of EXTAL32 and XTAL32	—	1	2	pF	
t_{start}	Crystal start-up time	—	1000	8000	ms	2
I_{OSC_32k}	Current consumption • OFF mode • ON mode	 — —	 0.5 100	 — —	 nA	
V_{pp}	Peak-to-peak amplitude of oscillation	—	0.2	—	V	3

Table continues on the next page...

Table 31. 32 kHz oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	4
$v_{ec\_extal32}$	Externally provided input clock amplitude	—	VDD_SYS	—	mV	4, 5
$C_{extal/xtal}$	EXTAL, XTAL Load Capacitance	0	—	30	pF	6

1. Maximum value is 80 kOhms for parasitic capacitances higher than 1 pF, and 150 kOhms for parasitic capacitances around 1 pF.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.
4. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
5. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to $V_{DD\_IO\_D}$.
6. With 2 pF steps.

NOTE

It is recommended that the oscillator margin be measured on the actual application PCB with the target crystal.

3.2.3 Free-running oscillator FRO-192M specifications

Table 32. FRO-192M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$f_{fro192m}$	FRO-192M frequency (nominal)		96/192		MHz	
$\Delta f_{fro192m}$	Frequency deviation (–40 °C – 125 °C) • Open loop • Closed loop (using accurate clock source as reference)	 — —	 — —	 ±3 ±0.25	 % %	
$t_{startup}$	Start-up time • Oscillation time with initial accuracy of ±20 % to ±2 % of enable signal assertion • Oscillation time within ±2 % from enable signal assertion	 — —	 2 10	 — —	 μs μs	
f_{os}	Frequency overshoot during startup	—	—	2	%	
jit_{per}	• Period jitter RMS [1] • Accumulated jitter over 1 μs	— —	50 375	— —	ps	
jit_{cyc}	Cycle to Cycle jitter RMS	—	60	—	ps	
$I_{fro192m}$	Current consumption	—	40	100	μA	

1. Reference clock = 192 MHz.

3.2.4 Free-running oscillator FRO-6M specifications

Table 33. FRO-6M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{fro6m}	FRO-6M frequency (nominal)	—	6	—	MHz	
Δf_{fro6m}	Frequency deviation • open loop • closed loop (using accurate clock source as reference)	— —	— —	±3 ±0.6	% %	
$t_{startup}$	Start-up time • Oscillation time with initial accuracy of -20 % to +2 % of enable signal assertion • Oscillation time within ± 2 % from enable signal assertion	— —	5 10	— —	μs μs	
f_{os}	Frequency overshoot during startup	—	10	—	%	
I_{fro6m}	Current consumption	—	—	4	μA	

3.2.5 Free-running oscillator FRO-32K specifications

Table 34. FRO-32K specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{fro32k}	FRO-32K frequency (nominal)	—	32.768	—	kHz	
Δf_{fro32k}	Frequency deviation • open loop	—	—	±2	%	
$TRIM_{step}$	Trimming step	—	0.03	—	%	
$t_{startup}$	Start-up time	—	—	120	μs	
f_{os}	Frequency overshoot during startup • Trimmed	—	10	—	%	
I_{fro32k}	Current consumption	—	350	—	nA	

3.2.6 Free-running oscillator FRO-16K specifications

Table 35. FRO-16K specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V_{BAT}	Supply voltage operating range	1.9	2.7	3.6	V	1
Temp	Temperature range	–40	25	125	°C	
f_{fro16K}	FRO-16K frequency (nominal)	—	16.384	—	kHz	
Δf_{fro16K}	Frequency deviation • Over –40 °C~125 °C temperature range	—	—	±6	%	

Table continues on the next page...

Table 35. FRO-16K specifications (continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
TRIMstep	Frequency trimming step	—	1.5	—	%	
I_{fro16k}	Current consumption	—	50	—	nA	2
I_{por}	Current consumption	—	26	—	nA	

1. FRO-16K is in Power Switch block, which is powered by min 1.9 V VDD_SWITCH
2. The Typical value (70 nA) of current consumption includes 20 nA POR current consumption in stable running period.

3.3 Memories and memory interfaces

3.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.3.1.1 Flash Read wait state control specifications

FCTRL[RWSC] defines the number of read wait-states in the flash module for FMC read access to the flash array during full power and low-power modes. The following requirements must be met.

Table 36. Recommend RWSC settings on K32W (for MCU flash and Radio Flash)

Mode	Typical Frequency (MHz)	FCTRL[RWSC]
SD – 1.1 V	96	0010b
SD – 1.1 V	64	0001b
SD – 1.1 V	48	0001b
MD – 1.0 V	48	0001b
MD – 1.0 V	32	0000b

3.3.1.2 Flash timing specifications

The following command times assume a flash bus clock frequency of 24 MHz.This clock come from SLOW_CLK. Command times will be increased by up to 10 μs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

Table 37. Flash command time specifications

Symbol	Description	Typ.	Max.	Unit	Notes
$t_{rd1all1024k}$	Read 1s All execution time (1024 KB)	—	6200	μs	
$t_{rd1blk1024k}$	Read 1s Block execution time (1024 KB)	—	6000	μs	
t_{rd1scr}	Read 1s Sector execution time	—	50	μs	1
t_{rd1pg}	Read 1s Page execution time	—	4.4	μs	1
$t_{rd1pglv}$	Read 1s Page at low voltage execution time	—	5.8	μs	1
$t_{rd1phrlv}$	Read 1s Phrase at low voltage execution time	—	4.8	μs	1
$t_{rd1ipglv}$	Read 1s IFR Page at low voltage execution time	—	5.8	μs	1
$t_{rd1iphrlv}$	Read 1s IFR Phrase at low voltage execution time	—	4.8	μs	1

Table continues on the next page...

Table 37. Flash command time specifications (continued)

Symbol	Description	Typ.	Max.	Unit	Notes
t_{rd1phr}	Read 1s Phrase execution time	—	3.8	μs	1
$t_{rdmisr8k}$	Read into MISR (8 KB)	—	50	μs	1
$t_{rdmisr1024k}$	Read into MISR (1024 KB)	—	6000	μs	1
$t_{rd1iscr}$	Read 1s IFR Sector execution time	—	50	μs	1
t_{rd1ipg}	Read 1s IFR Page execution time	—	4.4	us	1
$t_{rd1iphr}$	Read 1s IFR Phrase execution time	—	3.8	μs	1
$t_{rdimisr8k}$	Read IFR into MISR (8 KB)	—	50	μs	1
$t_{rdimisr32k}$	Read IFR into MISR (32 KB)	—	190	μs	1
t_{pgmpg}	Program Page execution time	450	1000	μs	2
t_{pgmphr}	Program Phrase execution time	135	375	μs	2
$t_{ersall1024k}$	Erase All execution time (1024 KB)	—	2800	ms	
$t_{masers1024k}$	Mass Erase execution time (1024 KB)	—	2800	ms	
t_{ersscr}	Erase Sector execution time	2	22	ms	2

1. Time to abort the command may significantly impact the time to execute the command.
2. Measured from the time PERDY is cleared.

3.3.1.3 Flash high voltage current behavior

Table 38. Flash high voltage current behavior

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD\_IO\_PGM}$	Average current adder to VDD_IO_x during flash programming operation	—	—	6	mA	1
$I_{DD\_IO\_ERS}$	Average current adder to VDD_IO_x during flash erase operation	—	—	4	mA	1

1. See the Power Management chapter in the reference manual for the specific VDD_IO_x voltage supply powering the flash array.

3.3.1.4 Flash reliability specifications

Table 39. Flash reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	10	50	—	years	
$n_{nvmcycscr}$	Sector cycling endurance	10 K	500 K	—	cycles	2
$T_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$T_{nvmretp100k}$	Data retention after up to 100 K cycles	5	50	—	years	

Table continues on the next page...

Table 39. Flash reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$N_{nvmcyc256k}$	Sector cycling endurance for 256 KB per array block	100 K	500 K	—	cycles	3

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile.
2. Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40 °C ≤ T_j ≤ 125 °C.
3. For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory.

3.4 Radio modules

3.4.1 2.4 GHz radio transceiver electrical specification

Table 40. 2.4 GHz radio transceiver specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VDD_RF	RF supply voltage	1.175	1.2	3.6	V	
VPA_2P4 GHZ	Supply voltage for 2.4 GHz radio power amplifier	0.9	—	2.4	V	1, 2
f_{in}	Input RF frequency	2.360	—	2.4835	GHz	
f_c	Output RF frequency	2.360	—	2.4835	GHz	
P_{max}	RF input power	—	—	10	dBm	
f_{ref}	Crystal reference oscillator frequency	—	32	—	MHz	
f_{tol}	Frequency tolerance	—	±50	—	ppm	
T_{rx_tx}	Rx - Tx turnaround time	—	150	—	µs	3

1. Voltage required at this rail depends on the desired output power. See Transmit and PLL Feature Summary for the required voltages.
2. VPA_2P4GHZ is internally connected to the VDD_RF pin. When not powered externally, VPA_2P4GHZ = VDD_RF - 0.275 V. An internal regulator prevents VPA_2P4GHZ from going above 2.4 V when powered through the VDD_RF pin.
3. Bluetooth LE. Other modes have different requirements

3.4.2 Receiver Feature Summary

Table 41. Top-level Receiver Specifications (T_A = 25 °C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Receiver Active Power Consumption					
Supply current Rx On with DC-DC converter enable (Buck; VDD_DCDC =3.3 V, VDD_RF=VDD_LDO_CORE = 1.25 V) [2]	I_{Rxon}	—	4.68	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3. V) [2]	I_{Rxon}	—	10.01	—	mA

Table continues on the next page...

Table 41. Top-level Receiver Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current Rx On with DC-DC converter disabled (Buck, VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.25 V) for IEEE802.15.4[2]	$I_{Rxon15.4}$	—	3.69	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3. V) [2]	$I_{Rxon15.4}$	—	7.9	—	mA
Receiver General Specifications					
Input RF Frequency	F_{in}	2.360	—	2.4835	GHz
GFSK Rx Sensitivity(250 kbps GFSK-BT = 0.5, h = 0.5)[3]	$SENS_{GFSK}$	—	–103	—	dBm
Max RX RF Input Signal Level	RF_{inMax}	—	—	10	dBm
Noise Figure for maximum gain mode @ typical sensitivity[4]	NF_{HG}	—	6.5	—	dB
Receiver Signal Strength Indicator Range[5]	$RSSI_{Range}$	-100	—	0[6]	dBm
Receiver Signal Strength Indicator Resolution	$RSSI_{Res}$	—	1	—	dB
Typical RSSI variation over frequency		–2	—	2	dB
Typical RSSI variation over temperature		–2	—	2	dB
Narrowband RSSI accuracy[7]	$RSSI_{Acc}$	–3	—	3	dB
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc| < 1.6 MHz	—	—	–54	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc| > 2.5 MHz[8]	—	—	–70	—	dBc
Bluetooth LE coded 125 kbps (Long Range, 8x Spreading)					
Bluetooth LE LR 125 kbps Sensitivity[9,3]	$SENS_{BLELR125}$	—	–106	—	dBm
Bluetooth LE LR 125 kbps Co-channel Interference (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz).	$COSEL_{BLELR125}$		–2		dB
Adjacent/Alternate Channel Performance[10]					
Bluetooth LE LR 125 kbps Adjacent ±1 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLELR125,\ 1\ MHz}$	—	8	—	dB
Bluetooth LE LR 125 kbps Adjacent ± 2 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLELR125,\ 2\ MHz}$	—	50/35	—	dB

Table continues on the next page...

Table 41. Top-level Receiver Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Bluetooth LE LR 125 kbps Alternate ±3 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLELR125, 3 MHz}$	—	55/45	—	dB
Bluetooth LE LR 125 kbps Alternate ≥ ±4 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)[11]	$SEL_{BLELR125, 4+ MHz}$	—	55	—	dB
Bluetooth LE coded 500 kbps (Long Range, 2x Spreading)					
Bluetooth LE LR 500 kbps Sensitivity[9,3]	$SENS_{BLELR500}$	—	–102	—	dBm
Bluetooth LE LR 500 kbps Co-channel Interference (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz).	$COSEL_{BLELR500}$		–3		dB
Adjacent/Alternate Channel Performance[10]					
Bluetooth LE LR 500 kbps Adjacent ±1 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLELR500, 1 MHz}$	—	8	—	dB
Bluetooth LE LR 500 kbps Adjacent ±2 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLELR500, 2 MHz}$	—	50/35	—	dB
Bluetooth LE LR 500 kbps Alternate ±3 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLELR500, 3 MHz}$	—	55/45	—	dB
Bluetooth LE LR 500 kbps Alternate ≥ ±4 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)[11]	$SEL_{BLELR500, 4+ MHz}$	—	52	—	dB
Bluetooth LE un-coded 1 Mbps					
Bluetooth LE 1 Mbps Sensitivity[9,3]	$SENS_{BLE1M}$	—	–97.5	—	dBm
Bluetooth LE 1 Mbps Co-channel Interference (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz).	$COSEL_{BLE1M}$		–6		dB
Adjacent/Alternate Channel Selectivity Performance[10]					
Bluetooth LE 1 Mbps Selectivity ±1 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLE1M, 1 MHz}$	—	0	—	dB
Bluetooth LE 1 Mbps Adjacent ±2 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLE1M, 2 MHz}$	—	45/35	—	dB
Bluetooth LE 1 Mbps Selectivity ±3 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLE1M, 3 MHz}$	—	53/45	—	dB

Table continues on the next page...

Table 41. Top-level Receiver Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps Alternate ≥ ±4 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)[11]	$SEL_{BLE1M, 4+ MHz}$	—	52	—	dB
Intermodulation Performance					
Bluetooth LE 1 Mbps Intermodulation with continuous wave interferer at ±3 MHz and modulated interferer is at ±6 MHz (or ±8 MHz) – Wanted signal at –67 dBm, BER < 0.1 %.	$IM3\text{-}6_{BLE1M}$ $IM4\text{-}8_{BLE1M}$	—	–27	—	dBm
Bluetooth LE 1 Mbps Intermodulation with continuous wave interferer at ±5 MHz and modulated interferer is at ±10 MHz – Wanted signal at –67 dBm, BER < 0.1 %.	$IM5\text{-}10_{BLE1M}$	—	–28	—	dBm
Blocking Performance					
Bluetooth LE 1 Mbps Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[12]	—	–2	—	—	dBm
Bluetooth LE 1 Mbps Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)	—	–10	—	—	dBm
Bluetooth LE 1 Mbps Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[13]	—	–10	—	—	dBm
Bluetooth LE 1 Mbps Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at –67 dBm, BER < 0. 1 %. Interferer continuous wave signal.)[13]	—	2	10	—	dBm
Bluetooth LE un-coded 2 Mbps (High Speed)					
Bluetooth LE 2 Mbps Sensitivity[9,3]	$SENS_{BLE2M}$	—	–95	—	dBm
Bluetooth LE 2 Mbps Co-channel Interference (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz).	$COSEL_{BLE2M}$		–7		dB
Adjacent/Alternate Channel Performance[10]					
Bluetooth LE 2 Mbps Adjacent ±2 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)	$SEL_{BLE2M, 2 MHz}$	—	5	—	dB
Bluetooth LE 2 Mbps Alternate ±4 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 2 MHz.)	$SEL_{BLE2M, 4 MHz}$	—	42/30	—	dB
Bluetooth LE 2 Mbps Selectivity ±6 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 4 MHz.)	$SEL_{BLE2M, 6 MHz}$	—	50	—	dB

Table continues on the next page...

Table 41. Top-level Receiver Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Bluetooth LE 2 Mbps Selectivity ≥±8 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %. Measurement resolution 1 MHz.)[11]	$SEL_{BLE2M, 8+ MHz}$	—	52	—	dB
Intermodulation Performance					
Bluetooth LE 2 Mbps Intermodulation with continuous wave interferer at ±6 MHz and modulated interferer is at ±12 MHz (or ±16 MHz) -- Wanted signal at –67 dBm, BER < 0.1 %.	$IM3\text{-}6_{BLE2M}$	—	–28	—	dBm
Bluetooth LE 2 Mbps Intermodulation with continuous wave interferer at ±8 MHz (±10 MHz) and modulated interferer is at ±16 MHz (or ±20 MHz) – Wanted signal at –67 dBm, BER < 0.1 %.)	$IM4\text{-}8_{BLE2M}$ $IM4\text{-}10_{BLE2M}$	—	–32	—	dBm
Blocking Performance					
Bluetooth LE 2 Mbps Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[12]	—	–4	—	—	dBm
Bluetooth LE 2 Mbps Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)	—	–10	—	—	dBm
Bluetooth LE 2 Mbps Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[13]	—	–10	—	—	dBm
Bluetooth LE 2 Mbps Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[13]	—	2	10	—	dBm
IEEE 802.15.4					
IEEE 802.15.4 1 % PER Sensitivity	SENS15.4	—	-103	—	dBm
IEEE 802.15.4 Co-channel Interference (Wanted signal at 3 dBm above sensitivity, PER 1 %).	COSEL15.4	—	-4	—	dB
WIFI rejection. 1 % PER, with wanted signal IEEE802.15.4 –75 dBm 2470 MHz, WIFI signal IEEE 802.11n 2447 MHz (20 MHz mode). Frequency offset > 23 MHz	RejWIFI15.4	—	-46	—	dBc
Adjacent/Alternate Channel Performance9[10]					
IEEE 802.15.4 Adjacent ±5 MHz interference offset (Wanted signal 3 dB over reference sensitivity level, PER <1 %)	SEL15.4, 5 MHz	—	35	—	dB

Table continues on the next page...

Table 41. Top-level Receiver Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
IEEE 802.15.4 Alternate ±10 MHz interference offset (Wanted signal 3 dB over reference sensitivity level, PER <1 %.)	SEL15.4, 10 MHz	—	45	—	dB
IEEE 802.15.4 Alternate ≥ ±15 MHz interference offset (Wanted signal 3 dB over reference sensitivity level, PER <1 %.)	SEL15.4, 15 MHz	—	52	—	dB
Blocking Performance					
IEEE 802.15.4 out of band blocking for frequency offsets > 10 MHz and <= 80 MHz(Wanted signal 3 dB over reference sensitivity level, PER <1 %. Interferer continuous wave signal.)[14]	—	—	–20	—	dBm
IEEE 802.15.4 out of band blocking from carrier frequencies in 1 GHz to 4 GHz range excluding frequency offsets < ±80 MHz (Wanted signal 3 dB over reference sensitivity level, PER <1 %. Interferer continuous wave signal.)	—	—	–10	—	dBm
IEEE 802.15.4 out of band blocking frequency from fc < 1 GHz or 4 GHz < fc < 5 GHz or fc > 6 GHz (Wanted signal 3 dB over reference sensitivity level, PER <1 %. Interferer continuous wave signal..11	—	—	-1	—	dBm
IEEE 802.15.4 out of band blocking frequency from 5 GHz < fc < 6 GHz (Wanted signal 3 dB over reference sensitivity level, PER <1%. Interferer continuous wave signal..11	—	—	-17	—	dBm

1. All the RX parameters are measured at the RF pins.
2. Transceiver power consumption.
3. Variation across temperature (-40 °C to 105 °C) is up to 3 dB.
4. Receiver noise Figure is computed from RF pin to composite (I+jQ) ADC output
5. Narrow-band RSSI mode.
6. With RSSI_CTRL_0.RSSI_ADJ field calibrated to account for antenna to RF input losses.
7. With one point calibration over frequency and temperature.
8. Exceptions allowed for twice the reference clock frequency(fref) multiples.
9. Measured at 0.1 % BER using 37 byte long packets in maximum gain mode and nominal conditions.
10. Bluetooth LE adjacent and alternate selectivity performance is measured with modulated interference signals.
11. Exceptions allowed for multiple of XTAL frequency
12. Exceptions allowed for carrier frequency sub harmonics.
13. Exceptions allowed for carrier frequency harmonics.
14. Exception to the 10 MHz > freq offset ≤ 80 MHz out-of-band blocking limit allowed for frequency offsets of twice the reference frequency(fref)

Table 42. Receiver Specifications with Generic FSK Modulations

				Adjacent/Alternate channel selectivity (dB)[1]					
Modulation type	Data rate (kb/s)	Channel BW (kHz)	Typical sensitivity (dBm)[2]	Desired signal level (dBm)	Interferer at ±1* channel BW offset	Interferer at ±2* channel BW offset	Interferer at ±3* channel BW offset	Interferer at ±4* channel BW offset	Co-channel
GFSK BT = 0.5, h = 0.5	2000	4000	-95	-67	5	45/35	52	55	7
	1000	2000	-98	-67	0	42/32	52/42	55	7
	500	1000	-101	-85	40	50/35	55	55	6
	250	500	-103	-85	38	48	52	55/35	6

1. Selectivity measured with an unmodulated blocker.
2. Variation across temperature (-40 °C to 105 °C) is up to 3 dB.

3.4.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM frequency band.
- Fast PLL Lock time: < 25 µs
- Reference Frequency:
  - — 32 MHz crystals supported for Bluetooth LE and Generic FSK modes

Table 43. Top-level Transmitter Specifications (T_A = 25 °C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Transmitter Active Power Specifications					
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.25 V) [2]	I_{TX0dBm}	—	4.60	—	mA
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V) [2]	$I_{TX0dBmb}$	—	9.83	—	mA
Supply current Tx On with P_{RF} = +4 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.25 V) [2]	I_{TX4dBm}	—	7.63	—	mA
Supply current Tx On with P_{RF} = +4 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V) [2]	I_{TX4dBm}	—	11.89	—	mA
Supply current Tx On with P_{RF} = +7 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.8 V) [2]	I_{TX7dBm}	—	10.79	—	mA
Supply current Tx On with P_{RF} = +7 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V, LDO_ANT ≥ 1.61 V)[2]	$I_{TX7dBmb}$	—	16.81	—	mA

Table continues on the next page...

Table 43. Top-level Transmitter Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current Tx On with P_{RF} = +10 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = LDO_ANT = 2.4 V)[2]	$I_{TX10dBm}$	—	18.71	—	mA
Supply current Tx On with P_{RF} = +10 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V, LDO_ANT ≥ 2.21 V)[2]	$I_{TX10dBmb}$	—	20.99	—	mA
Supply current Tx On in IEEE 802.15.4 with P_{RF} = 0 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.25 V)[2,3]	$I_{TX0dBm15.4}$	—	3.75	—	mA
Supply current Tx On in IEEE 802.15.4 with P_{RF} = 0 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V)[2,3]	$I_{TX0dBm15.4}$	—	8.02	—	mA
Supply current Tx On in IEEE 802.15.4 with P_{RF} = +10 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.25 V)[2,3]	$I_{TX0dBm15.4}$	—	17.10	—	mA
Supply current Tx On in IEEE 802.15.4 with P_{RF} = +10 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V)[2,3]	$I_{TX0dBm15.4}$	—	19.19	—	mA
Transmitter General Specifications					
Output RF Frequency	f_{RFout}	2.360	—	2.4835	GHz
Maximum RF Output Power; 10 dBm configuration [4,5]	$P_{RF,maxV}$	—	10	—	dBm
Minimum RF Output power [6,5]	$P_{RF,minn}$	—	-30	—	dBm
RF Output power control range (nominal power supply)	P_{RFCR}	—	32	—	dB
Bluetooth LE Maximum Deviation of the Carrier Frequency[7]	$F_{cdev,BLE}$	—	±3	—	kHz
Bluetooth LE Frequency Hopping Support			YES		
2^{nd} Harmonic of Transmit Carrier Frequency (P_{out} = $P_{RF,max}$)[8,9]	TXH2	—	–53	—	dBm/MHz
3^{rd} Harmonic of Transmit Carrier Frequency (P_{out} = $P_{RF,max}$)[9]	TXH3	—	–50	—	dBm/MHz
Bluetooth LE un-coded 1 Mbps/coded 125 kbps/coded 500 kbps					
Bluetooth LE 1 Mbps TX Output Spectrum 20 dB BW	$TXBW_{BLE1M}$	1.0		—	MHz
Bluetooth LE 1 Mbps average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE1M}$		250		kHz
Bluetooth LE 1 Mbps average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE1M}$		220		kHz
Bluetooth LE 1 Mbps RMS FSK Error	$FSK_{err,BLE1M}$		3%		
Bluetooth LE 1 Mbps Adjacent Channel Transmit Power at 2 MHz offset[9]	$P_{RF2MHz,BLE1M}$	—	—	-55	dBc

Table continues on the next page...

Table 43. Top-level Transmitter Specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps Adjacent Channel Transmit Power at ≥ 3 MHz offset[9]	$P_{RF3MHz,BLE1M}$	—	—	-59	dBc
Bluetooth LE un-coded 2 Mbps					
Bluetooth LE 2 Mbps TX Output Spectrum 20 dB BW	$TXBW_{BLE2M}$	2.0		—	MHz
Bluetooth LE 2 Mbps average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE2M}$	—	500	—	kHz
Bluetooth LE 2 Mbps average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE2M}$	—	440	—	kHz
Bluetooth LE 2 Mbps RMS FSK Error	$FSK_{err,BLE2M}$	—	4%	—	
Bluetooth LE 2 Mbps Adjacent Channel Transmit Power at 4 MHz offset[9]	$P_{RF4MHz,BLE2M}$	—	—	-55	dBc
Bluetooth LE 2 Mbps Adjacent Channel Transmit Power at ≥ 6 MHz offset[9]	$P_{RF6MHz,BLE2M}$	—	—	-60	dBc
IEEE 802.15.4					
IEEE 802.15.4 Peak Frequency Deviation	$Fdev_{15.4}$	—	±500	—	kHz
IEEE 802.15.4 Error Vector Magnitude[10]	$EVM_{15.4}$	—	5	8	%
IEEE 802.15.4 Offset Error Vector Magnitude[11]	$OEVM_{15.4}$	—	0.5	—	%
IEEE 802.15.4 TX spectrum level at 3.5 MHz offset[10,12]	$TXPSD_{15.4}$	—	—	–36	dBc
Transmitter spurious emissions					
30 MHz to 1 GHz, Peak detector, RBW=100 kHz	—	—	—	–60	dBm
1 GHz to 26 GHz, Peak detector, RBW = 1 MHz, based on FCC 15.247 at +10 dBm	—	—	—	–42	dBm
1 GHz to 2.36 GHz and 2.483 to 12.75 GHz, Peak detector, RBW = 1 MHz, based on ETSI EN 300 328 at +10 dBm	—	—	—	–37	dBm
2.36 GHz to 2.4 GHz and 2.4 GHz to 2.483 GHz, Peak detector RBW 1 MHz, ETSI EN 300 328 at +10dBm	—	—	—	–42	dBm

1. All the TX parameters are measured at test hardware SMA connector.
2. Transceiver power consumption. NBU running at @16 MHz.
3. To obtain current consumption at higher output power use the formula $I_{TXndBm15.4}=I_{TXndBm15.4}+(I_{TXndBm}-I_{TX0dBm})$ where n is the desired output power (+4 or +7)
4. Measured at RF pins, with V_{PA_2P4GHz} ≥ 2.4 V.
5. Variation across temperature (-40 °C to 105 °C) is up to 3 dB.
6. Measured at the RF pins single supply configuration VDD_RF = VDD_LDO_CORE = 1.25V
7. Maximum drift of carrier frequency of the PLL during a Bluetooth LE packet with a nominal 32 MHz reference crystal.
8. Harmonic levels based on recommended 2 component match for TX output power ≤ 5 dBm. Transmit harmonic levels depend on the quality of matching components. Additional harmonic margin using a 3rd matching component (1x shunt capacitor) is possible.
9. Measured at P_{out} > 5 dBm and recommended high-power TX match.
10. Measured as per IEEE Standard 802.15.4
11. Offset EVM is computed at one point per symbol, by combining the I value from the beginning of each symbol and the Q value from the middle of each symbol into a single complex value for EVM computations
12. Measured at PRF, Max and recommended TX match.

Transmit PA driver output as a function of the TX-PA_POWER[5:0] field when measured at the IC pins is as follows:

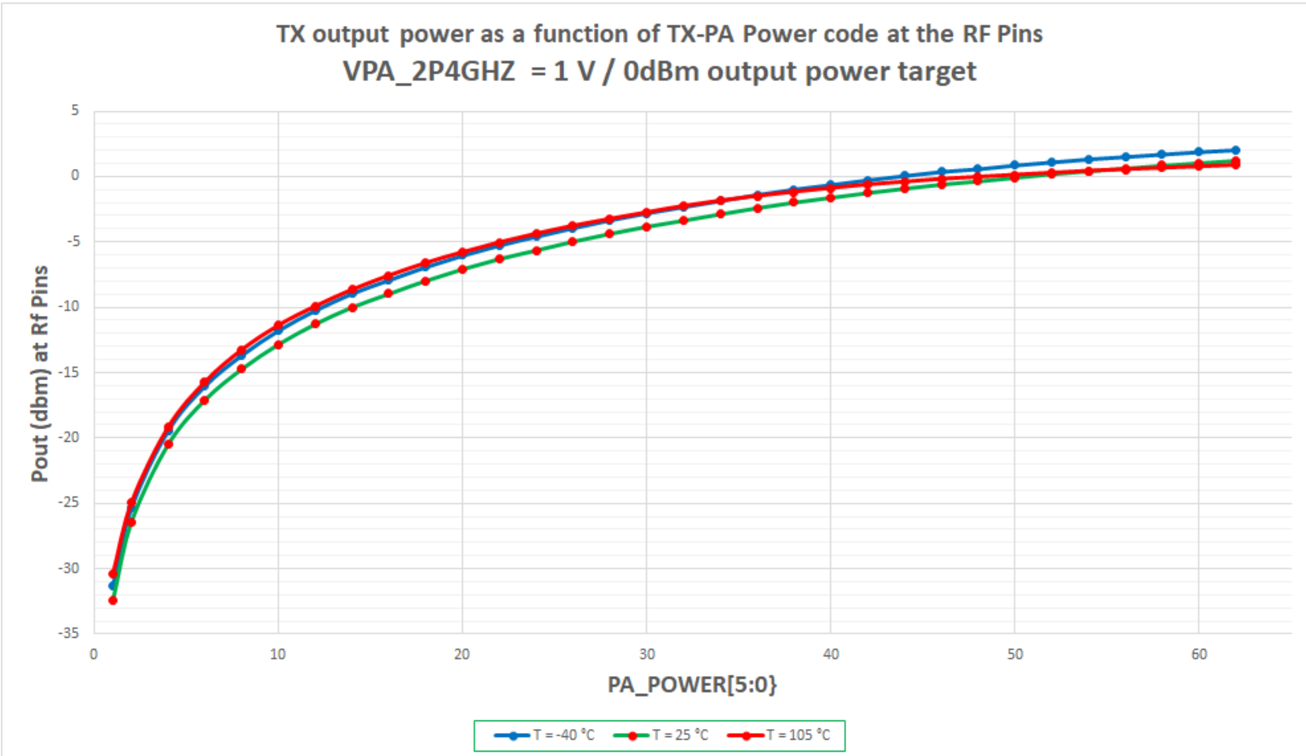


Figure 9. TX Pout (dBm) as function TX-PA Power Code at RF pins

Table 44. Transmit Output Power as a function of PA_POWER VPA_2P4GHZ = 1 V / 0 dBm output power target

TX Pout (dBm)				
PA_POWER	LDO ANT	T = –40 °C	T = 25 °C	T = 105 °C
1	2	–31.27	–32.44	–30.36
2	2	–25.34	–26.44	–24.92
4	2	–19.42	–20.5	–19.15
6	2	–16.01	–17.09	–15.7
8	2	–13.67	–14.73	–13.24
10	2	–11.77	–12.83	–11.36
12	2	–10.24	–11.28	–9.91
14	2	–8.94	–10	–8.65
16	2	–7.92	–8.97	–7.57
18	2	–6.92	–7.97	–6.61
20	2	–6.04	–7.08	–5.79
22	2	–5.26	–6.3	–5.04
24	2	–4.59	–5.64	–4.38

Table continues on the next page...

Table 44. Transmit Output Power as a function of PA_POWER VPA_2P4GHZ = 1 V / 0 dBm output power target (continued)

TX Pout (dBm)				
PA_POWER	LDO ANT	T = –40 °C	T = 25 °C	T = 105 °C
26	2	–3.94	–4.97	–3.77
28	2	–3.34	–4.37	–3.25
30	2	–2.8	–3.83	–2.75
32	2	–2.33	–3.36	–2.26
34	2	–1.86	–2.87	–1.85
36	2	–1.4	–2.4	–1.5
38	2	–0.99	–1.98	–1.18
40	2	–0.64	–1.61	–0.89
42	2	–0.28	–1.25	–0.63
44	2	0.05	–0.91	–0.41
46	2	0.36	–0.6	–0.2
48	2	0.57	–0.36	–0.04
50	2	0.85	–0.08	0.12
52	2	1.09	0.19	0.27
54	2	1.32	0.42	0.42
56	2	1.5	0.63	0.54
58	2	1.69	0.85	0.65
60	2	1.87	1.04	0.75
62	2	2.02	1.22	0.86

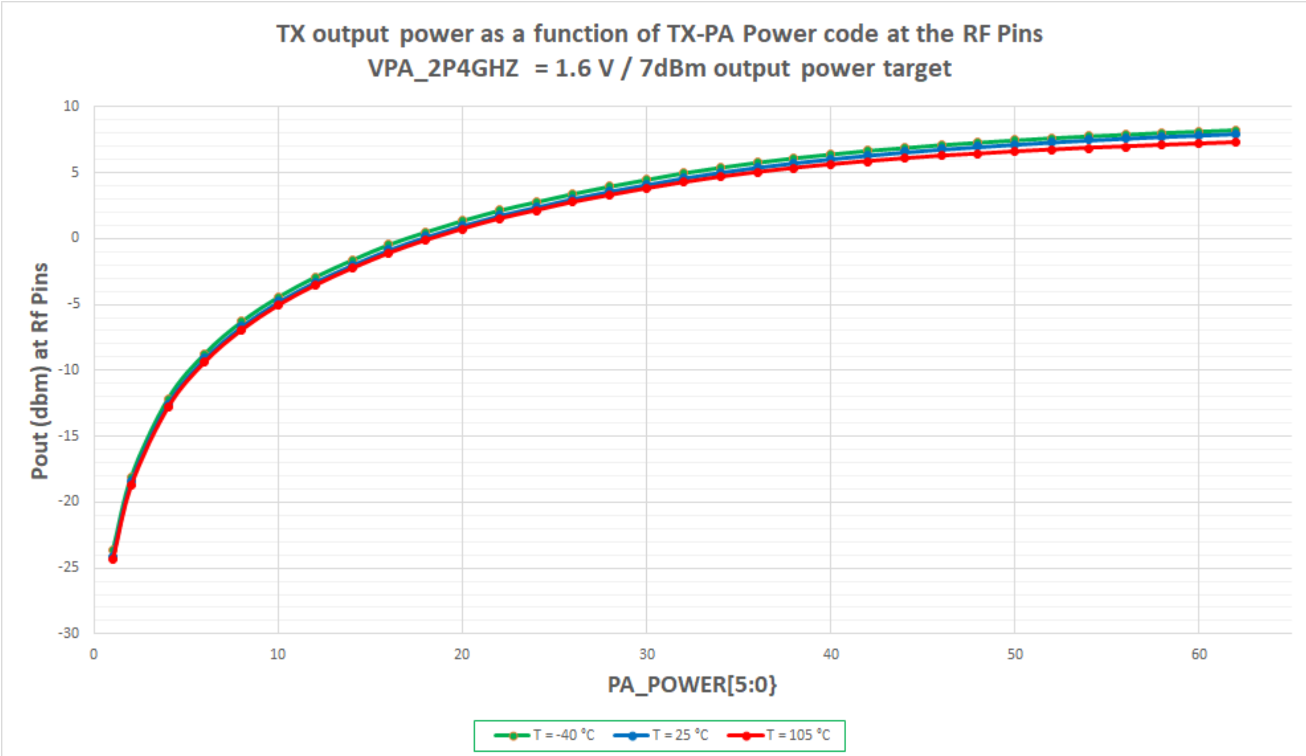


Figure 10. TX Pout (dBm) as function TX-PA Power Code at 7 dBm

Table 45. Transmit Output Power as a function of PA_POWER VPA_2P4GHZ = 1.6 V / 7 dBm output power target

TX Pout (dBm)				
PA_POWER	LDO_ANT	T =–40 °C	T = 25 °C	T =105 °C
1	8	–23.66	–24.11	–24.37
2	8	–18.06	–18.45	–18.72
4	8	–12.13	–12.54	–12.81
6	8	–8.72	–9.11	–9.38
8	8	–6.29	–6.68	–6.96
10	8	–4.42	–4.79	–5.07
12	8	–2.9	–3.29	–3.56
14	8	–1.62	–2.01	–2.28
16	8	–0.45	–0.85	–1.12
18	8	0.51	0.13	–0.14
20	8	1.38	0.99	0.72
22	8	2.15	1.75	1.49
24	8	2.79	2.39	2.12
26	8	3.42	3.03	2.75

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Table 45. Transmit Output Power as a function of PA_POWER VPA_2P4GHZ = 1.6 V / 7 dBm output power target (continued)

TX Pout (dBm)				
PA_POWER	LDO_ANT	T =–40 °C	T = 25 °C	T =105 °C
28	8	3.98	3.59	3.28
30	8	4.49	4.1	3.78
32	8	4.99	4.6	4.25
34	8	5.41	5.03	4.66
36	8	5.79	5.41	5.01
38	8	6.13	5.75	5.33
40	8	6.42	6.05	5.6
42	8	6.69	6.32	5.85
44	8	6.91	6.57	6.06
46	8	7.13	6.79	6.26
48	8	7.31	6.97	6.41
50	8	7.49	7.15	6.58
52	8	7.65	7.33	6.72
54	8	7.8	7.48	6.86
56	8	7.91	7.61	6.96
58	8	8.05	7.74	7.08
60	8	8.15	7.85	7.18
62	8	8.26	7.96	7.27

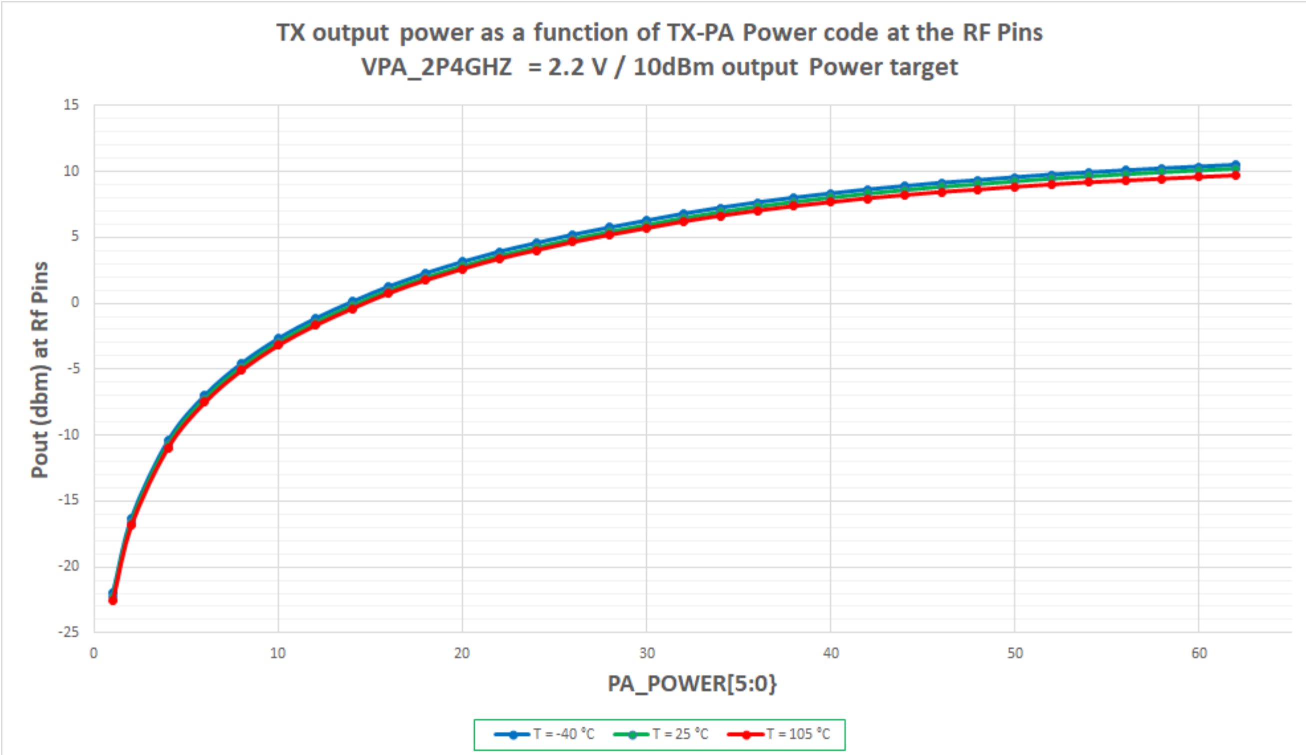

Figure 11. TX Pout (dBm) as function TX-PA Power Code at 10 dBm

Table 46. Transmit Output Power as a function of PA_POWER VPA_2P4GHZ = 2.2 V / 10 dBm output

TX Pout (dBm)				
PA_POWER	LDO_ANT	T = -40 °C	T = 25 °C	T = 105 °C
1	12	–21.93	–22.25	–22.52
2	12	–16.29	–16.59	–16.86
4	12	–10.39	–10.67	–10.95
6	12	–6.97	–7.24	–7.52
8	12	–4.55	–4.82	–5.09
10	12	–2.66	–2.93	–3.19
12	12	–1.16	–1.43	–1.69
14	12	0.11	–0.16	–0.42
16	12	1.27	1.01	0.76
18	12	2.27	1.99	1.74
20	12	3.13	2.85	2.6
22	12	3.9	3.62	3.37
24	12	4.55	4.26	4.01
26	12	5.19	4.9	4.63

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Table 46. Transmit Output Power as a function of PA_POWER VPA_2P4GHZ = 2.2 V / 10 dBm output (continued)

TX Pout (dBm)				
PA_POWER	LDO_ANT	T = -40 °C	T = 25 °C	T = 105 °C
28	12	5.74	5.46	5.18
30	12	6.26	5.97	5.68
32	12	6.78	6.5	6.19
34	12	7.23	6.95	6.62
36	12	7.63	7.36	7
38	12	7.99	7.72	7.35
40	12	8.31	8.05	7.65
42	12	8.61	8.35	7.94
44	12	8.87	8.62	8.18
46	12	9.12	8.87	8.42
48	12	9.32	9.07	8.6
50	12	9.54	9.29	8.81
52	12	9.74	9.49	8.99
54	12	9.91	9.66	9.15
56	12	10.06	9.82	9.28
58	12	10.21	9.98	9.42
60	12	10.34	10.11	9.55
62	12	10.47	10.24	9.67

3.5 Analog

3.5.1 ADC electrical specifications

3.5.1.1 16-bit ADC operating conditions

Table 47. 16-bit ADC operating conditions

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{DD_ANA}	Supply voltage	1.71	—	3.6	V	
ΔV_{DD_ANA}	Supply voltage delta to V_{DD} ($V_{DD} - V_{DD\_ANA}$)	–0.1	0	+0.1	mV	2
ΔV_{SS_ANA}	Ground voltage delta to V_{SS} ($V_{SS} - V_{SS\_ANA}$)	–0.1	0	+0.1	mV	2
V_{REFH}	ADC reference voltage high	0.99	V_{DD_ANA}	V_{DD_ANA}	V	
V_{REFL}	ADC reference voltage low	V_{SS_ANA}	V_{SS_ANA}	V_{SS_ANA}	V	3
V_{ADIN}	Input voltage	V_{REFL}	—	V_{REFH}	V	3, 4,5

Table continues on the next page...

Table 47. 16-bit ADC operating conditions (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
f_{ADCK}	ADC input clock frequency • Low-power mode (PWRSEL=00) • High-speed 16b mode (PWRSEL = 10) • High-speed 12b mode (PWRSEL = 10)	6 6 6	— — —	20 48 60	MHz MHz MHz	
C_{ADIN}	Input capacitance	—	3.7	4.63	pF	
C_p	Parasitic Cap of pad /package	—	2	3	pF	
R_{AS}	Analog source resistance (external)	—	—	5	kΩ	[6]
R_{ADIN}	• High-speed dedicated input channel (CH0:3) — $V_{DD\_ANA} \geq 1.71$ V — $V_{DD\_ANA} \geq 2.1$ V — $V_{DD\_ANA} \geq 2.5$ V • Standard external input channel (Ch4:7) — $V_{DD\_ANA} \geq 1.71$ V — $V_{DD\_ANA} \geq 2.1$ V — $V_{DD\_ANA} \geq 2.5$ V • Standard muxed input channel (Ch4:11) — $V_{DD\_ANA} \geq 1.71$ V — $V_{DD\_ANA} \geq 2.1$ V — $V_{DD\_ANA} \geq 2.5$ V	 — — — — — — — — —	 0.95 0.95 0.95 1.35 1.35 1.35 1.65 1.65 1.65	 1.7 1.6 1.4 3.25 2.15 1.75 7.25 3.05 2.35	kΩ	[7,8]

1. Typical values assume V_{DD_ANA}= 3.0 V, Temp = 25 °C, f_{ADCK} = 24 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
4. If V_{REFH} is less than V_{DD_ANA}, then voltage inputs greater than V_{REFH} but less than V_{DD_ANA} are allowed but result in a full scale conversion result
5. ADC selected inputs and unselected dedicated inputs must not exceed V_{DD_ANA} during an ADC conversion. Unselected muxed inputs may exceed V_{DD_ANA} but must not exceed the IO supply associated with the inputs (VDD_IO_X) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
6. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
7. There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual
8. If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

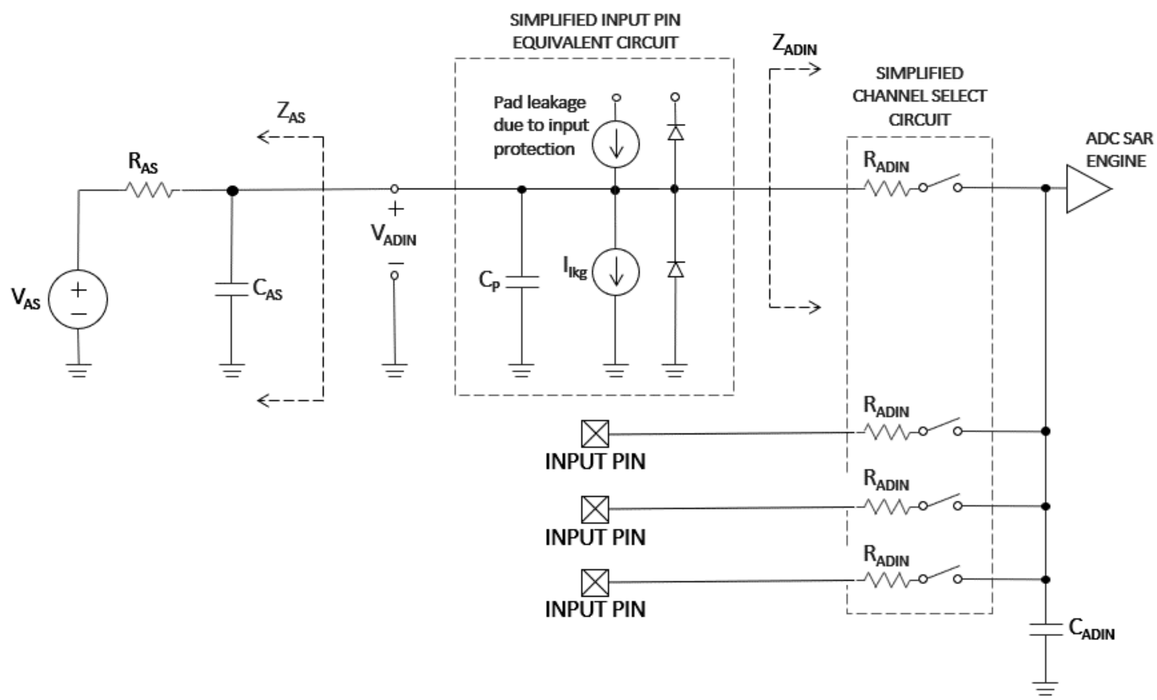


Figure 12. ADC input impedance equivalency diagram

3.5.1.2 16-bit ADC electrical characteristics

Table 48. 16-bit ADC characteristics (VREFH = VDD_ANA, VREFL = VSS_ANA)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDA}	Supply current					2
	• PWREN=0, Conversions triggered at 1 kS/s	—	2.2	—	µA	
	• PWREN=1, No Conversions	—	160	215	µA	
	• Low-power, single-ended mode, 6 MHz	—	340	440	µA	
	• Low-power, or dual-SE mode, 6 MHz	—	500	640	µA	
	• Low-power, single-ended mode, 24 MHz	—	415	530	µA	
	• Low-power, or dual-SE mode, 24 MHz	—	580	750	µA	
	• High-speed, single-ended mode, 48 MHz	—	940	1200	µA	
	• High-speed, or dual-SE mode, 48 MHz	—	1500	1950	µA	
I_{TS}	Temp Sensor Current Adder	—	40	50	µA	
C_{SMP}	ADC Sample cycles	3.5	—	131.5	cycles	3
C_{CONV}	ADC conversion cycles	24	—	152	cycles	
C_{RATE}	ADC conversion rate	—	—	0.857	MS/s	4

Table continues on the next page...

Table 48. 16-bit ADC characteristics (VREFH = VDD_ANA, VREFL = VSS_ANA) (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	• Low-power mode • High-speed mode (16-bits) • High-speed mode (12-bits)	— —	— —	2 3.16		
T_{SMP_REQ}	Required Sample Time	See equation	—	—	ns	[5]
T_{AZ_REQ}	Required Auto-zero Time • Low-power mode • High-power mode (16-bits) • High-power mode (12-bits)	291.7 72.9 58.3	— — —	— — —	ns	[5]
T_{SMP}	Sample Time External inputs	See equation	—	—	ns	[5]
T_{SMP_INT}	Internal channel sample time	1.5	—	—	µs	[6]
DNL	Differential non-linearity	—	±0.7	+1.4/–0.95	LSB[7]	[8]
INL	Integral non-linearity	—	±2.0	+4.0/–2.0	LSB[7]	[8]
Z_{SE}	Zero-scale error (V_{ADIN} = V_{REFL})	—	±1.0	±2.0	LSB[7]	[8]
F_{SE}	Full-scale error (V_{ADIN}=V_{REFH})	—	±2.0	+2.0/–8.0	LSB[7]	[8]
TUE	Total unadjusted error	—	±4.0	±10.0	LSB[7]	[8]
ENOB	Effective number of bits • Differential mode — 0.5 MS/s — 2 MS/s • Single-ended mode — 0.5 MS/s — 2 MS/s	12.7 12.0 12.4 11.5	13.5 12.7 13.1 12.2	— — — —	bits	[8,9]
SINAD	Signal-to-noise plus distortion • Differential mode — 0.5 MS/s — 2 MS/s • Single-ended mode — 0.5 MS/s — 2 MS/s	80 75 77 71	86 79 81 75	— — — —	dB	[8,9]
THD	Total harmonic distortion	85	92	—	dB	[8,10]
SFDR	Spurious free dynamic range	86	94	—	dB	[8,10]

Table continues on the next page...

Table 48. 16-bit ADC characteristics (VREFH = VDD_ANA, VREFL = VSS_ANA) (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
T_{SU}	ADC/VREF start-up time	5	—	—	µs	11
E_{IL}	Input leakage error	—	$I_{lkg} \times R_{AS}$	—	mV	12
E_{TS}	Temperature sensor error • T=–40 °C to 105 °C • T=–40 °C to 125 °C	— —	±1 ±1.5	±3 ±4	°C	13

1. Typical values assume V_{DD_ANA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 24 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The ADC supply current depends on the ADC conversion clock speed, conversion rate and power mode. Typical value show is at 6 MHz, 24 MHz, and 48 MHz. For lowest power operation, PWRSEL should be set to 00.
3. Must meet minimum TSMP requirement.
4. Maximum conversion rate for high-speed mode is with F_{ADCK} = 48 MHz. Maximum conversion rate for low-power mode is F_{ADCK} = 24 MHz and 7.5 sample cycles (to meet the minimum auto-zero time requirement).
5. Required sample time is dictated by external components R_{AS}, C_{AS}, internal components R_{ADIN}, C_{ADIN}, C_P, and desired sample accuracy in bits. Calculated it with formula: $T_{SMP\_REQ} = B*IN(2)*[R_{AS}*(C_{AS}*C_P)+ (R_{AS} + R_{ADIN})* C_{ADIN(typ)}$. Required auto-zero time is for ADC comparator offset cancellation. The chosen sample time should be no less than maximum of the two: $T_{SMP} = max(T_{SMP\_REQ},T_{AZ\_REQ})$.
6. Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
7. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$ (N=14 bits), for 16-bit specifications, multiply by 4.
8. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DD\_ANA}$ and using a high-speed dedicated input channel.
9. Dynamic results assume F_{in} = 1 kHz sinewave, AVGS = 0 for 2 MS/s, AVGS = 4 for 0.5 MS/s.
10. Dynamic results assume F_{in} = 1 kHz sinewave, no averaging.
11. Set the power up delay (PUDLY) according to the ADC start-up time if PWREN=0.
12. I_{lkg} = leakage current (Refer to pin leakage specification in the packaged device's voltage and current operating ratings).
13. The temperature sensor can be calibrated to a ± 0.5% precision after board assembly by using a 3 temperature calibration flow with accurate ± 0.15 % temperature chamber.

3.5.2 CMP and 8-bit DAC electrical specifications

Table 49. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_IO_ABC	Supply voltage	1.71	—	3.6	V	
VREFH	8-bit DAC reference voltage high	0.97	—	VDD_IO_ABC	V	
I_{DD_CMP}	Supply current • High-speed mode (EN=1, HPMD=1) • Normal mode (EN=1, HPMD=0, NPMD=0) • Nano mode (EN=1, HPMD=0, NPMD=1)	— — —	200 10 400	— — —	µA µA nA	
V_{AIN}	Analog input voltage	VSS_ANA	—	VDD_ANA	V	1
V_{AIO}	Analog input offset voltage • High-speed mode • Normal mode	— —	— —	20 20	mV mV	

Table continues on the next page...

Table 49. Comparator and 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• Nano mode	—	—	40	mV	
V_H	Analog comparator hysteresis • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	— — — —	0 10 20 30	— — — —	mV mV mV mV	2
t_D	Propagation delay • High-speed mode, 100 mV overdrive, power > 1.71 V • High-speed mode, 30 mV overdrive, power > 1.71 V • Normal mode, 30 mV overdrive, power > 1.71 V • Nano mode, 30 mV overdrive, power > 1.71 V	— — — —	— — — —	25 50 600 5	ns ns ns μs	3
t_{init}	Analog comparator initialization delay	—	—	40	μs	4
I_{DAC8b}	8-bit DAC current adder (enabled) • High-power mode (EN=1, PMODE=1) • Low-power mode (EN=1, PMODE=0)	— —	10 1	— —	μA μA	
INL	8-bit DAC integral non-linearity • Low/High power mode, supply power > 1.71 V	–1.0	—	+1.0	LSB	5
DNL	8-bit DAC differential non-linearity • Low/High power mode, power > 1.71 V	–1.0	—	+1.0	LSB	5

1. For devices that do not have a dedicated VSS_ANA pin, VSS_ANA is tied to VSS internally.
2. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
3. Overdrive does not include input offset voltage or hysteresis.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]), and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}$/256.

Typical hysteresis

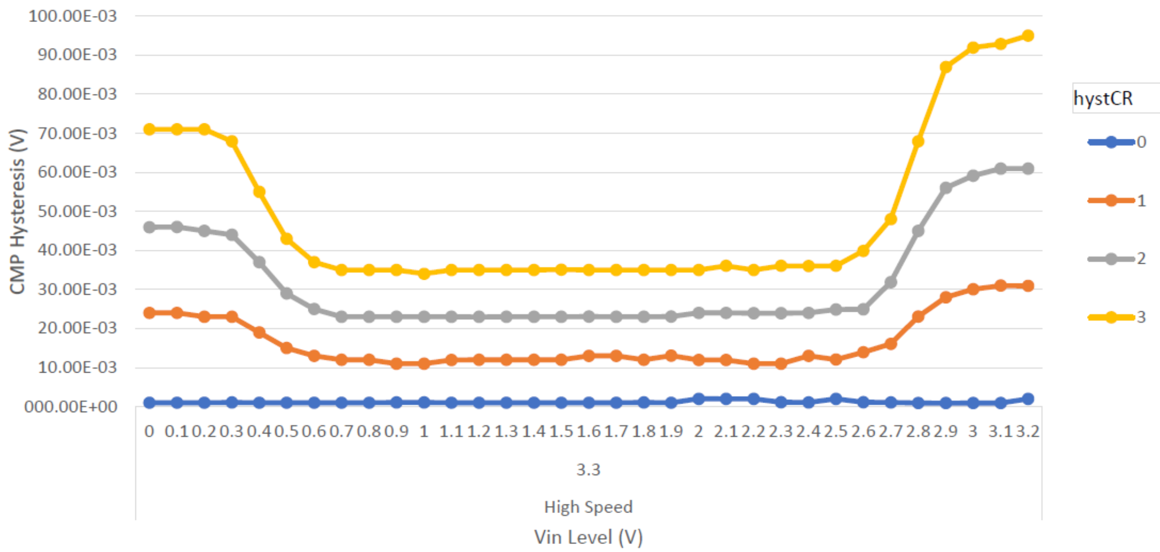


Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

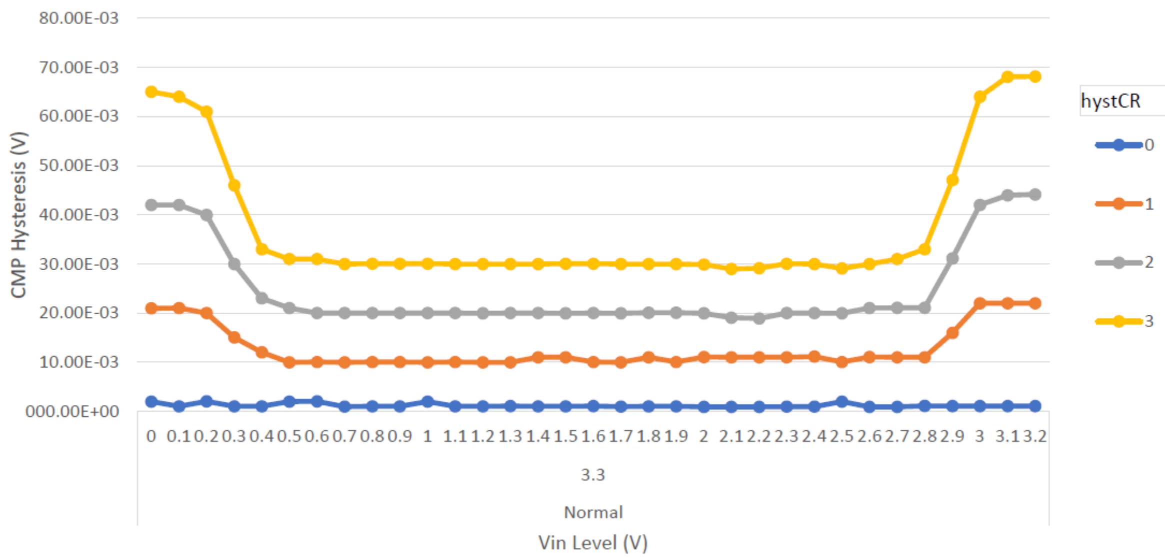


Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

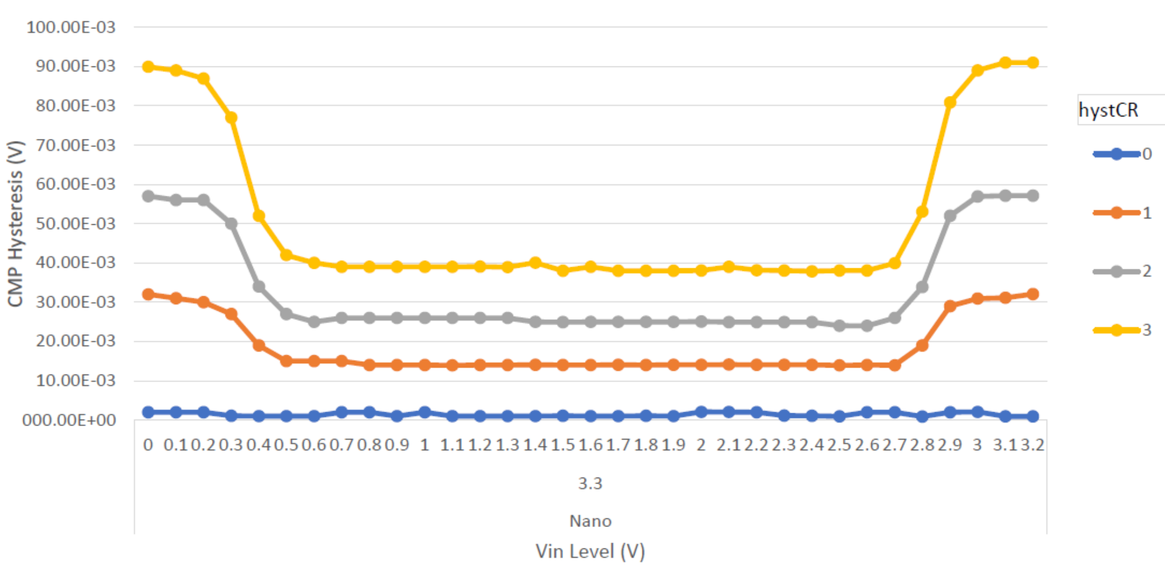


Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1)

3.5.3 Voltage reference electrical specifications

Table 50. VREF operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_ANA	Supply voltage	1.71	3.0	3.6	V	
C_L	Output load capacitance	130	220	470	nF	1

1. C_L must be connected to VREFO if the VREFO functionality is being used for either an internal or external reference.

Table 51. VREF operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
1.0 V low-power reference voltage						
V_{vrefo_lpbg}	Voltage reference output 1.0 V - LP bandgap	1.0	—	1.1	V	1
I_{q_lpbg}	Quiescent current - LP bandgap	—	16	—	μA	
I_{out_lpbg}	Output current - LP bandgap	—	10	—	μA	
t_{st_lpbg}	Start-up time - LP bandgap	—	6	20	μs	
$\Delta V/V_{refo\_lpbg}$	Voltage variation - LP bandgap	—	±5	—	%	
High precision reference voltage						
V_{vrefo}	Voltage reference output 2.0 V	1.0	—	2.1	V	2,1
V_{step}	Fine trim step	—	0.5 x V_{refo}	—	mV	
I_q	Quiescent current	—	750	—	μA	

Table continues on the next page...

Table 51. VREF operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{out}	Output current	±1	—	—	mA	
t_{st_lpbg}	Start-up time	—	—	400	μs	
ΔV_{LOAD}	Load regulation	—	100	200	μV/mA	3
V_{acc}	Absolute voltage accuracy (room temp)	—	±1.5	±6.5	mV	
V_{dev}	Voltage deviation over temperature	—	15	—	ppm/°C	

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. V_{vrefo} max is also ≤ VDD_ANA - 600 mV.
3. Load regulation voltage is the difference between the VREFO voltage with no load vs. voltage with defined load.

3.6 Timers

See General switching specifications.

3.7 Communication interfaces

3.7.1 LPUART

See General switching specifications.

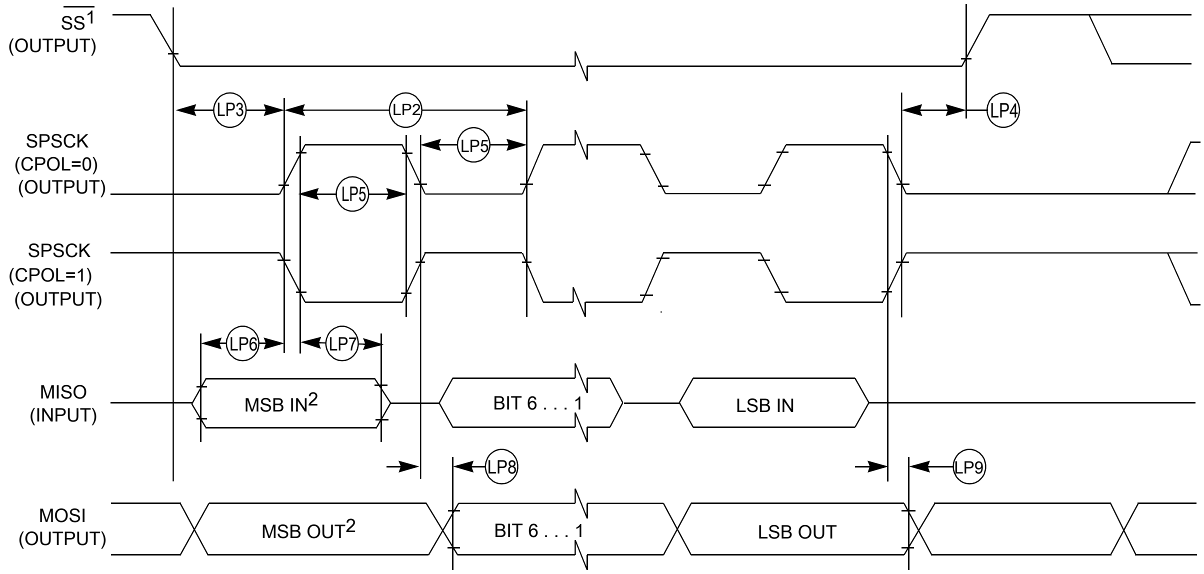
3.7.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

Table 52. LPSPI master mode timing

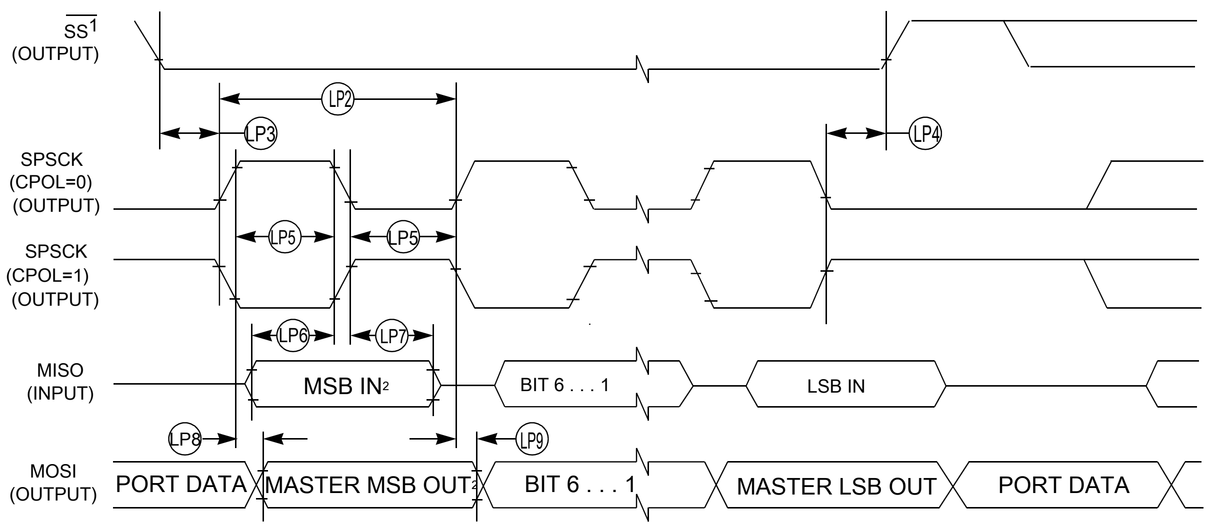
Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation • LPSPI0 • LPSPI1	— —	12 24	MHz MHz	1
LP2	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
LP3	Enable lead time	1/2	—	t_{periph}	2
LP4	Enable lag time	1/2	—	t_{periph}	2
LP5	Clock (SPSCK) high or low time	$t_{SPSCK}/2 - 3$	$t_{SPSCK}/2$	ns	—
LP6	Data setup time (inputs)	8	—	ns	—
LP7	Data hold time (inputs)	0	—	ns	—
LP8	Data valid (after SPSCK edge)	—	6	ns	—
LP9	Data hold time (outputs)	2	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/2$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. LPSPI master mode timing (CPHA = 1)

Table 53. LPSPI slave mode timing

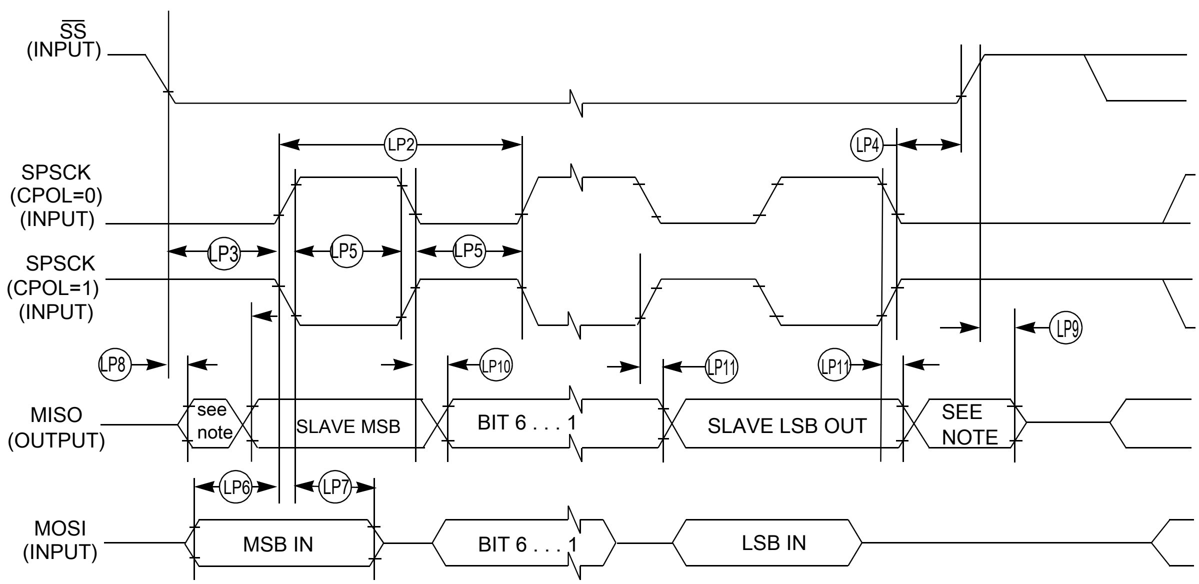
Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation • LPSPI0-LPSPI1	—	12	MHz	1
LP2	SPSCK period	4 x t_{periph}	2048 x t_{periph}	ns	2

Table continues on the next page...

Table 53. LPSPI slave mode timing (continued)

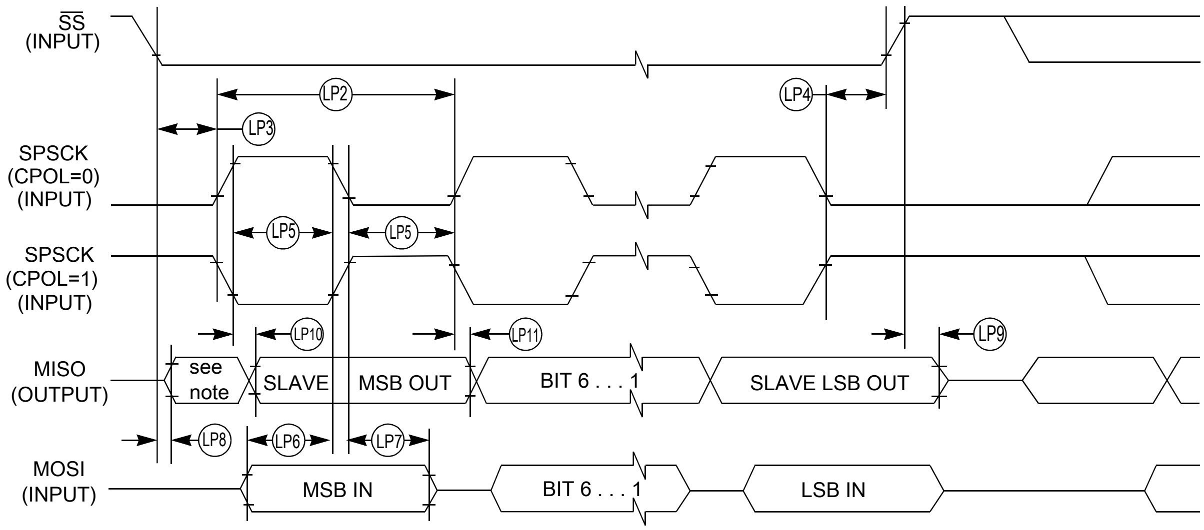
Symbol	Description	Min.	Max.	Unit	Notes
LP3	Enable lead time	1	—	t_{periph}	2
LP4	Enable lag time	1	—	t_{periph}	2
LP5	Clock (SPSCK) high or low time	$t_{SPSCK}/2 - 5$	$t_{SPSCK}/2$	ns	—
LP6	Data setup time (inputs)		—	ns	—
LP7	Data hold time (inputs)	1	—	ns	—
LP8	Slave access time	—	t_{periph}	ns	2,3
LP9	Slave MISO disable time	—	t_{periph}	ns	2,4
LP10	Data valid (after SPSCK edge)	—	28	ns	—
LP11	Data hold time (outputs)	1	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/4$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$.
3. Time to data active from high-impedance stat.
4. Hold time to high-impedance state.



NOTE: Not defined

Figure 18. LPSPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 19. LPSPI slave mode timing (CPHA = 1)

3.7.3 Inter-Integrated Circuit Interface (I^{2}C) specifications

Table 54. I^{2}C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^{2}C bus devices	t_{HD}; DAT	0[1,2]	3.45[3]	0[4,2]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3,6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^{2}C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 55. I^2C 1 Mbps timing

Characteristic	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	$20 + 0.1C_b$ [1]	120	ns
Fall time of SDA and SCL signals	t_f	$20 + 0.1C_b$[1]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. C_b = total capacitance of the one bus line in pF. The max Cb value is 50 pF.

Table 56. I2C HS mode timing[1]

Parameter	Symbol	Min	Max	Units
SCL Clock Frequency	f_{SCL}	0	3.4	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	–	µs
LOW period of the SCL clock	t_{LOW}	0.5	–	µs
High period of the SCL clock	t_{HIGH}	0.26	–	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	–	µs
Data hold time for I2C bus devices	t_{HD}; DAT	0[2]	–	µs
Data setup time	t_{SU}; DAT	34	_	ns
Rise time of SDA and SCL signals	t_r	20 +0.1Cb[3]	120	ns

Table continues on the next page...

Table 56. I2C HS mode timing[1] (continued)

Fall time of SDA and SCL signals	t_f	20 +0.1Cb[3]	120	ns
Setup time for STOP condition	t_{SU}; STO	0.26	_	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	_	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. Only PTB4/5, PTA18/19, PTC0/1, PTC4/5 pin can support Fast+ (3 MHz) mode.
2. A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.
3. Cb = total capacitance of the one bus line in pF. The max Cb value is 50 pF.

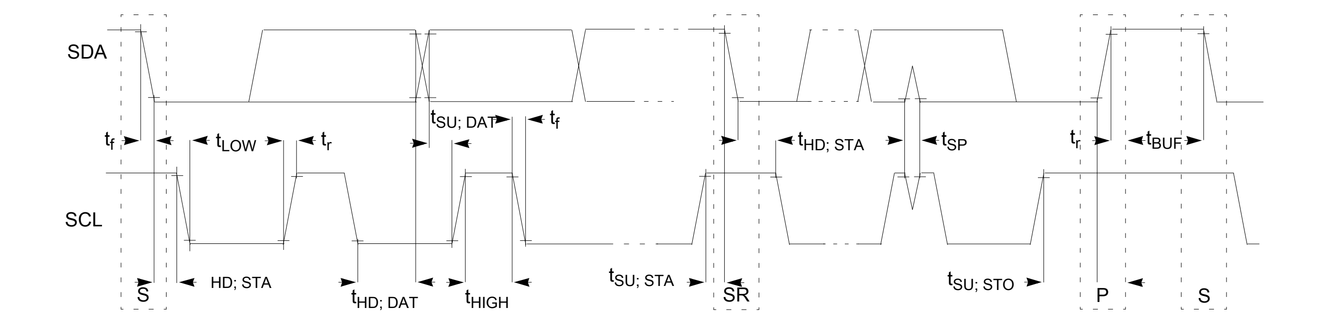


Figure 20. Timing definition for devices on the I2C bus

3.7.4 Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications

Unless otherwise specified, MIPI-I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

Table 57. MIPI-I3C specifications when communicating with legacy I2C devices

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1.0	MHz
t_{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
t_{HD_STA}	Hold time (repeated START condition)	600	—	260	—	ns
t_{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t_{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t_{SU_DAT}	Data set-up time	100	—	50	—	ns
t_{HD_DAT}	Data hold time for I2C bus devices	0	—	0	—	ns
t_f	Fall time of SDA and SCL signals	20 + 0.1C_b[1]	300	20 + 0.1C_b[1]	120	ns
t_r	Rise time of SDA and SCL signals	20 + 0.1C_b[1]	300	20 + 0.1C_b[1]	120	ns
t_{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns

Table continues on the next page...

Table 57. MIPI-I3C specifications when communicating with legacy I^2C devices (continued)

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

1. C_b = total capacitance of the one bus line in pF.

Table 58. MIPI-I3C open drain mode specifications

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{LOW_OD}	LOW period of the SCL clock	200	—	ns	
$t_{DIG\_OD\_L}$		t_{LOW_OD} + t_{fDA_OD} (min)	—	ns	
t_{HIGH}	HIGH period of the SCL clock	t_{CF}	12	ns	
t_{fDA_OD}	Fall time of SDA signal	20 +0.1C_b	120	ns	1
t_{SU_OD}	Data set-up time during open drain mode	3	—	ns	
t_{CAS}	Clock after START (S) Condition • ENTAS0 • ENTAS1 • ENTAS2 • ENTAS3	38.4 n 38.4 n 38.4 n 38.4 n	1 µ 100 µ 2 m 50 m	s s s s	
t_{CBP}	Clock before STOP (P) condition	t_{CAS}(min)/2	—	ns	
$t_{MMOverlap}$	Current master to secondary master overlap time during handoff	$t_{DIG\_OD\_L}$	—	ns	
t_{AVAL}	Bus available condition	1	—	µs	
t_{IDLE}	Bus idle condition	1	—	ms	
t_{MMLock}	Time internal where new master not driving SDA low	t_{AVAL}	—	µs	

1. C_b = total capacitance of the one bus line in pF.

Table 59. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	—	12.5	MHz	
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	
t_{DIG_L}		32	—	—	ns	
t_{HIGH_MIXED}	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	

Table continues on the next page...

Table 59. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes (continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$t_{DIG\_H\_MIXED}$		32	—	45	ns	1
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	
t_{DIG_H}		32	—	—	ns	
tSCO	Clock in to data out for slave					
	Load capacitance = 50 pF	—	—	38	ns	
	Load capacitance = 25 pF	—	—	36	ns	
	Load capacitance = 15 pF	—	—	35	ns	
	Load capacitance = 1 pF	—	—	33	ns	
t_{CR}	SCL clock rise time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	
t_{CF}	SCL clock fall time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	
t_{HD_PP}	SDA signal data hold • Master mode • Slave mode	 t_{CR} + 3 and t_{CF} + 3 0	 — —	 — —	ns	
t_{SU_PP}	SDA signal setup	3	—	—	ns	
t_{CASr}	Clock after repeated START (Sr)	t_{CAS} (min)	—	—	ns	
t_{CBSr}	Clock before repeated START (Sr)	t_{CAS} (min)/2	—	—	ns	
C_b	Capacitive load per bus line	—	—	50	pF	

1. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C devices do not interpret I3C signaling as valid I^2C signaling.

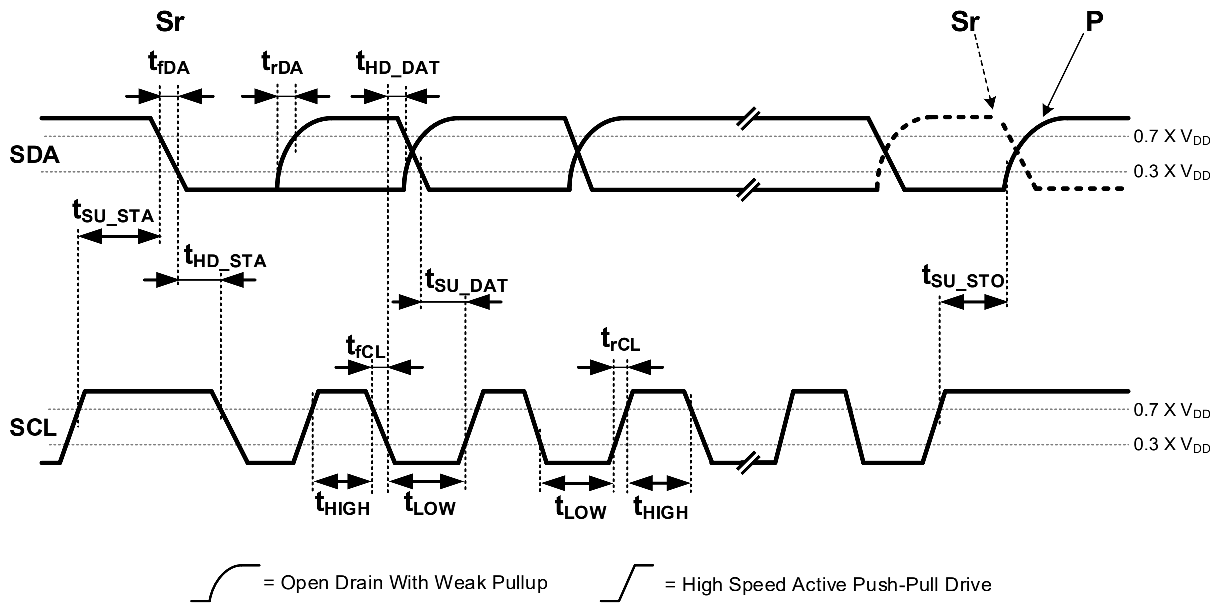


Figure 21. I3C legacy mode timing

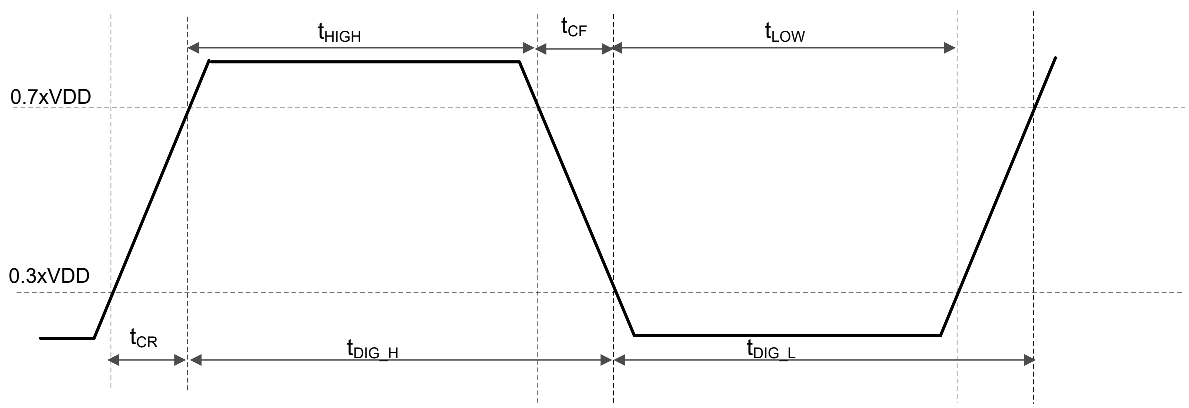


Figure 22. t_{DIG_H} and t_{DIG_L}

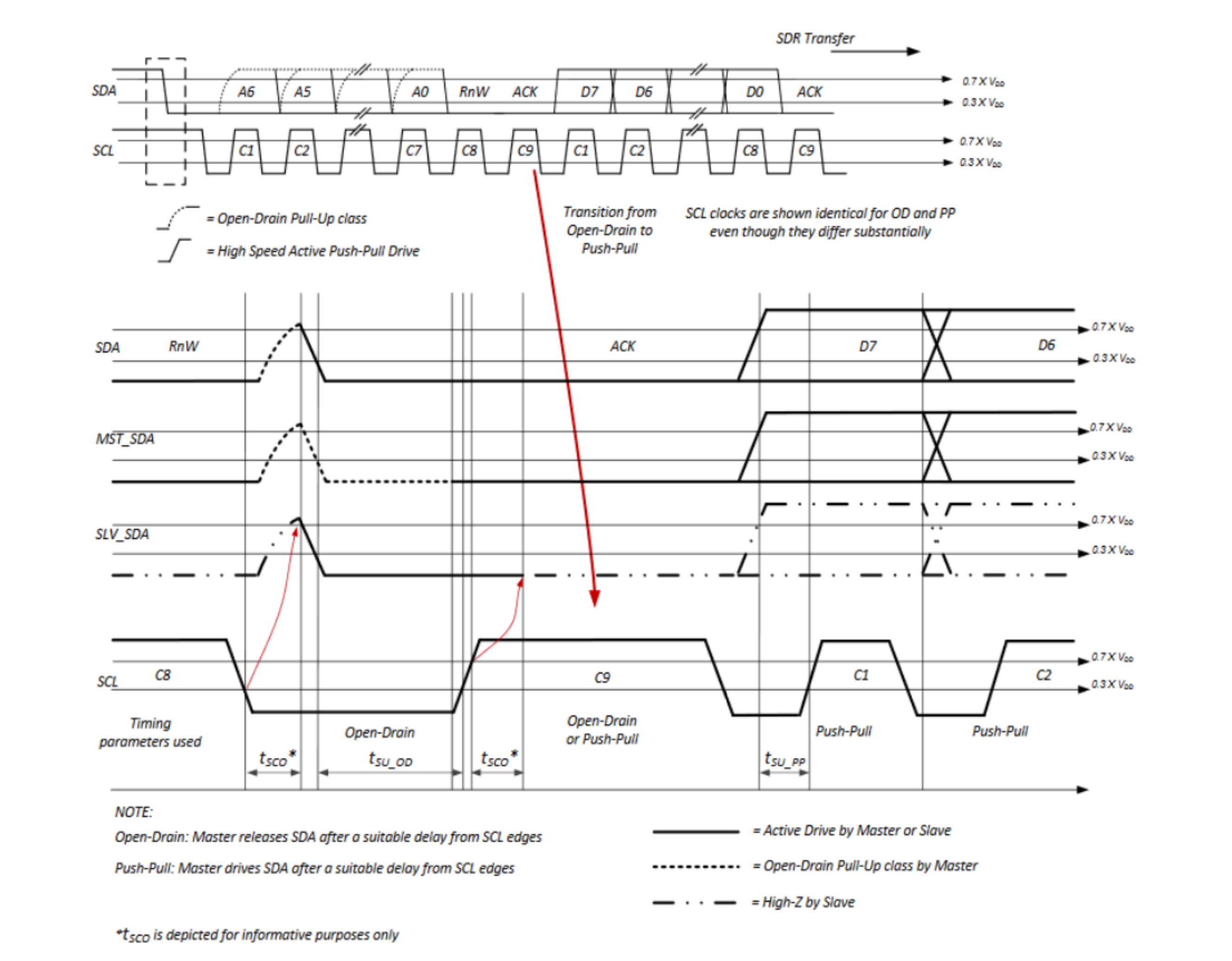


Figure 23. Timing definition for devices on the I3C bus

3.8 Human Machine Interface (HMI) modules

3.8.1 General Purpose Input/Output (GPIO)

See General switching specifications.

3.8.2 Flexible IO controller (FlexIO)

Table 60. FlexIO Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	10	ns	1
t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	10	ns	1

1. Assumes pins muxed on same VDD_IO domain with same load

4 Package dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin QFN	SOT619-17(D)

5 Pinout

5.1 Pinout Table

48QFN	Pin Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	Wakeup
2	PTB4		PTB4	LPSPI1_PCS3	LPUART1_CTS_b	LPI2C1_SDA	I3C0_SDA	TRGMUX0_IN0			FLEXIO0_D30			WUU0_P15
3	PTB5		PTB5	LPSPI1_PCS2	LPUART1_RTS_b	LPI2C1_SCL	I3C0_SCL	TRGMUX0_OUT0			FLEXIO0_D31			
4	VDD_IO_ABC	VDD_IO_ABC												
5	SWITCH_WAKEUP_B	SWITCH_WAKEUP_B												
6	VDD_SWITCH	VDD_SWITCH												
7	VOUT_SWITCH	VOUT_SWITCH												
8	PTA0		PTA0	CMP0_OUT	LPUART0_CTS_b	RF_GPO_11	TPM0_CH4	FLEXIO0_D0	SWD_DIO					WUU0_P0
9	PTA1		PTA1	CMP1_OUT	LPUART0_RTS_b	RF_GPO_10	TPM0_CH5	FLEXIO0_D1	SWD_CLK					

Table continues on the next page...

Table continued from the previous page...

48QFN	Pin Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	Wakeup
10	PTA4	ADC0_A10/CMP0_IN0	PTA4		RF_GPO_9	TPM0_CLKIN	TRACE_SWO	FLEXIO0_D4	BOOT_CONFIG					WUU0_P2/RF_XTAL_OUT_ENABLE
11	PTA16	ADC0_A12	PTA16	LPSPI0_PCS0	EWM0_OUT_b	LPI2C0_SCLS	TPM0_CH4	LPUART0_RX	RF_GPO_8		FLEXIO0_D5			RF_NOT_ALLOWED
12	PTA17	ADC0_A13	PTA17	LPSPI0_SIN	EWM0_IN	LPI2C0_SDAS	TPM0_CH5	LPUART0_TX	RF_GPO_7	RF_GPO_8	FLEXIO0_D6		RF_EXT_XTAL_REQUEST/RF_GPO_7	WUU0_P3/RF_NOT_ALLOWED
13	PTA18	CMP1_IN1	PTA18	LPSPI0_SOUT	LPUART0_CTS_b	LPI2C0_SDA	TPM0_CH3	RF_GPO_0				LPUART0_RX	SPC0_LPREQ	
14	PTA19	CMP1_IN0	PTA19	LPSPI0_SCK	LPUART0_RTS_b	LPI2C0_SCL	TPM0_CH2	RF_GPO_1						WUU0_P4
15	VDD_LDO_CORE	VDD_LDO_CORE												
16	VDD_CORE/VOUT_CORE	VDD_CORE/VOUT_CORE												
17	PTA20	ADC0_A14/CMP0_IN3	PTA20	LPSPI0_PCS2	LPUART0_TX	EWM0_IN	TPM0_CH1	RF_GPO_2		FLEXIO0_D7				
18	PTA21	ADC0_A15/CMP0_IN2	PTA21	LPSPI0_PCS3	LPUART0_RX	EWM0_OUT_b	TPM0_CH0	RF_GPO_3	RF_GPO_7	FLEXIO0_D8	RF_GPO_10			WUU0_P5
19	VSS_DCDC	VSS_DCDC												

Table continues on the next page...

Table continued from the previous page...

48QFN	Pin Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT 5	ALT6	ALT7	ALT8	ALT 9	ALT1 0	ALT11	Wakeu p
20	DCDC_L X	DCDC_ LX												
21	VDD_IO_ D/ VDD_DC DC	VDD_I O_D/ VDD_D CDC												
22	VOUT_S YS/ VDD_SY S	VOUT_ SYS/ VDD_S YS												
23	PTD0	ADC0_ A5	PTD0		RESE T_b									
24	PTD1	ADC0_ B5	PTD1	SPC 0_LP REQ	NMI_b	RF_ GPO _4								
25	PTD2	ADC0_ A6	PTD2	LPT MR0 _ALT 3	TAMP ER0	RF_ GPO _5								
26	PTD3	ADC0_ B6	PTD3	LPT MR1 _ALT 3	TAMP ER1	RF_ GPO _6		TRG MUX0 _IN2						
27	PTD4	XTAL3 2K	PTD4	LPT MR0 _ALT 2	TAMP ER2									
28	PTD5	EXTAL 32K	PTD5	LPT MR1 _ALT 2										
29	VDD_AN A	VDD_A NA												
30	VREFO	VREF O												
49	VREFL[1]	VREFL												
31	XTAL_O UT	XTAL_ OUT												
32	XTAL	XTAL												
33	EXTAL	EXTAL												

Table continues on the next page...

Table continued from the previous page...

48QFN	Pin Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT 5	ALT6	ALT7	ALT8	ALT 9	ALT1 0	ALT11	Wakeu p
34	VDD_RF	VDD_R F												
35	ANT_2P4 GHZ	ANT_2 P4GHZ												
36	VPA_2P4 GHZ	VPA_2 P4GHZ												
37	PTC0		PTC0	LPS PI1_ PCS 2		I3C0 _SD A	TPM 1_C H0		LPI2 C1_S CL		FLE XIO0 _D1 6			WUU0 _P7
38	PTC1		PTC1	LPS PI1_ PCS 3		I3C0 _SC L	TPM 1_C H1		LPI2 C1_S DA		FLE XIO0 _D1 7			WUU0 _P8
39	PTC2		PTC2	LPS PI1_ SOU T	LPUA RT1_ RX	LPI2 C1_ SCL S	TPM 1_C H2		I3C0 _PU R		FLE XIO0 _D1 8			WUU0 _P9
40	PTC3		PTC3	LPS PI1_ SCK	LPUA RT1_ TX	LPI2 C1_ SDA S	TPM 1_C H3				FLE XIO0 _D1 9			
41	VDD_CO RE	VDD_C ORE												
42	PTC4		PTC4	LPS PI1_ SIN		LPI2 C1_ SCL		TPM2 _CH0			FLE XIO0 _D2 0			WUU0 _P10
43	PTC5		PTC5	LPS PI1_ PCS 0		LPI2 C1_ SDA	TPM 1_C H4	TPM2 _CH1			FLE XIO0 _D2 1			
44	PTC6	ADC0_ A8	PTC6	LPS PI1_ PCS 1			TPM 1_C H5				FLE XIO0 _D2 2			WUU0 _P11
45	PTC7	DISAB LED	PTC7	TRG MUX 0_IN 3	TRG MUX0 _OUT 3	SFA 0_CL K	TPM 1_C LKI N	TPM2 _CLKI N	CLK OUT		FLE XIO0 _D2 3			WUU0 _P12/ NMI_b/ RF_NO T_ALL OWED

Table continues on the next page...

Table continued from the previous page...

48QFN	Pin Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT 5	ALT6	ALT7	ALT8	ALT 9	ALT1 0	ALT11	Wakeu p
46	PTB0	ADC0_ B10	PTB0	LPS PI1_ PCS 0			TPM 1_C H0				FLE XIO0 _D2 6			WUU0 _P13
47	PTB1	ADC0_ B11	PTB1	LPS PI1_ SIN			TPM 1_C H1				FLE XIO0 _D2 7			
48	PTB2	ADC0_ B12	PTB2	LPS PI1_ SCK	LPUA RT1_ TX		TPM 1_C H2				FLE XIO0 _D2 8			
1	PTB3	ADC0_ B13	PTB3	LPS PI1_ SOU T	LPUA RT1_ RX		TPM 1_C H3				FLE XIO0 _D2 9			WUU0 _P14
49	VSS	VSS												

1. VREF shorts to VSS.

5.2 Recommended connection for unused analog and digital pins

Table 61 shows the recommended connections for pins if those pins are not used in the customer's application

Table 61. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VOUT_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_CORE	Connect to VDD_LDO_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_SYS	Connect to VDD_IO_D	When the LDO is bypassed, the input and output should be connected together and tied to an external supply that shall not exceed the maximum input voltage for VDD_SYS. The regulator should also be disabled in software.
Power	VDD_DCDC	Ground	When the DCDC is not used, the input should be tied to VSS through a 10 kΩ resistor.
Power	DCDC_LX	Float	

Table continues on the next page...

Table 61. Recommended connection for unused interfaces (continued)

Pin Type	Pin Function	Recommendation	Comments
Power	VDD_IO_D	Must be powered	VDD_IO_D is used to power parts of the system power controller (SPC) and must be powered to use the chip. If LDO_SYS is not being used, then tie VDD_IO_D to VOUT_SYS and supply power from an external source. The regulator should also be disabled in software.
Power	VDD_SWITCH	Must be powered	Powers FRO16 and a portion of RAM.
Power	VOUT_SWITCH	Float	
Power	VDD_IO_ABC	Must be powered	VDD_IO_ABC powers the mux logic for PORTA, PORTB and PORTC. It must be powered during POR. The recommendation is to keep it powered, but it can be connected to the output of the Smart Power Switch and be left floating in shelf storage mode.
Power	VPA_2P4GHz	Float	
Power	VDD_ANA	Float	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_DCDC	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_RF	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n*_*x*	Float	
Analog/non-GPIO	VREFO	Float	Analog output - Float
Analog/non-GPIO	TAMPERx	Float	
Analog/non-GPIO	RTC_WAKEUP_B	Float	
Analog/non-GPIO	RTC_RTCCLKOUT	Float	
Analog/non-GPIO	EXTAL32K	Float	
Analog/non-GPIO	XTAL32K	Float	Analog output - Float
Analog/non-GPIO	EXTAL_32M	Float	
Analog/non-GPIO	XTAL_32M	Float	Analog output - Float
GPIO/Analog	PTx/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	PTD1/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float

Table continues on the next page...

Table 61. Recommended connection for unused interfaces (continued)

Pin Type	Pin Function	Recommendation	Comments
GPIO/Digital	PTx	Float	Float (default is disabled)

5.3 Pinouts diagram

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

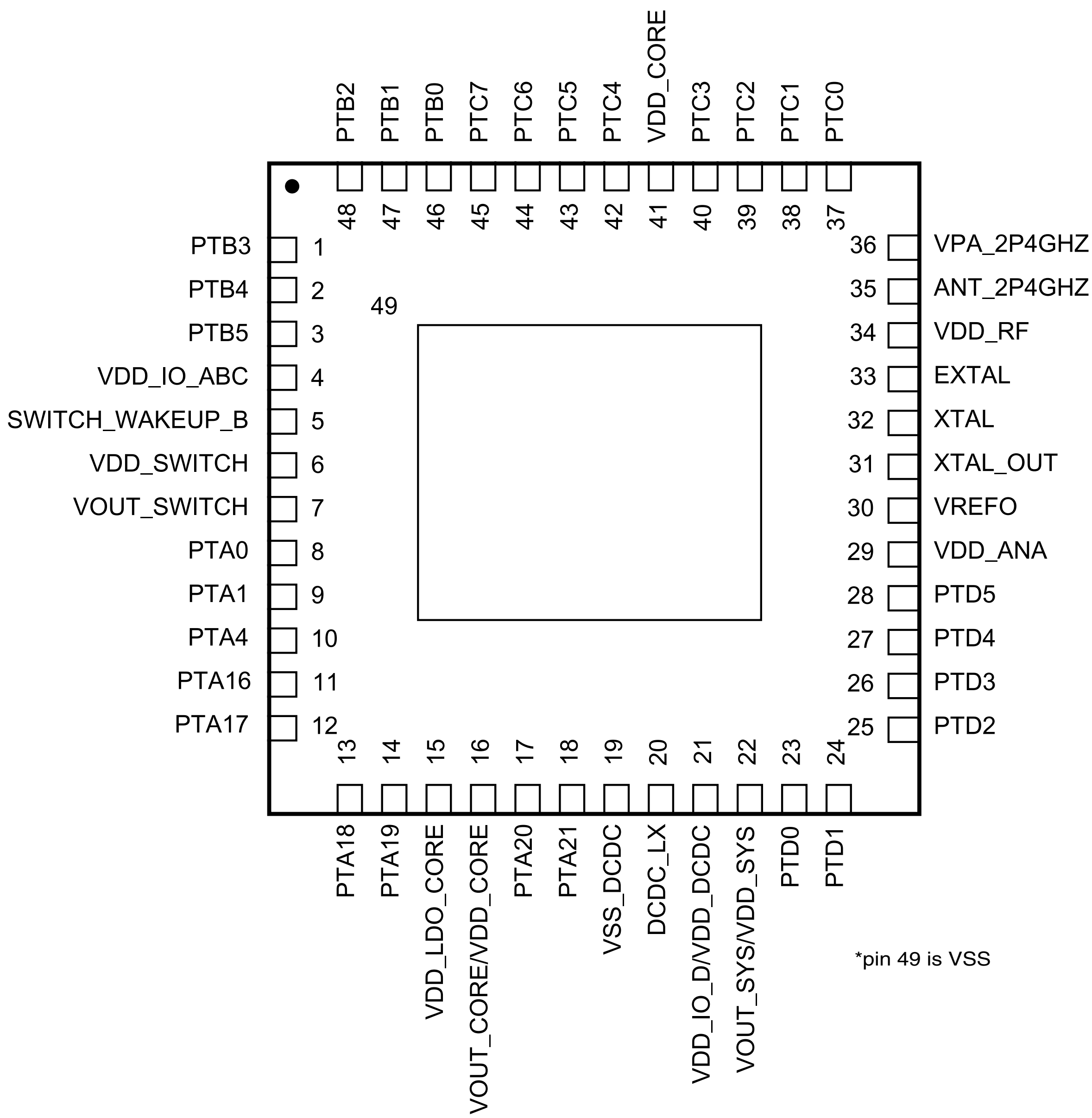


Figure 24. 48-pin QFN package pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: K32W1480

7 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

7.1 Part number format

Part numbers for this device have the following format:

B S R FS SF T PG SR PT

Table 62. Part number fields descriptions

Field	Description	Values
B	Brand	• K32W
S	Security	• 1 = Secure Enclave
R	Radio	• 4 = Bluetooth LE + 802.15.4
FS	Flash Size	• 8 = 1 MB
SF	Sub Feature	• 0 = Baseline
T	Temperature	• V = Industrial, –40 ºC to + 105 ºC (Ta)
PG	Package	• FT = 48 HVQFN “Wettable”, 7 mm x 7 mm, 0.5p
SR	Silicon Revision	• A = Initial Mask Set • B = Production Mask Set
PT	Packaging Type	• R = Tape and Reel • T = Tray

7.2 Example

This is an example part number:

K32W1480VFTBT

7.3 Package marking

Part numbers for this device have the following format:

B S R FS SF T PG SR

Table 63. Package marking

Field	Description	Values
B	Brand	• K32W

Table continues on the next page...

Table 63. Package marking (continued)

Field	Description	Values
S	Security	• 1 = Secure Enclave
R	Radio	• 4 = Bluetooth LE + 8021.15.4
FS	Flash Size	• 8 = 1MB
SF	Sub Feature	• 0 = Baseline
T	Temperature	• V = Industrial, –40 ºC to + 105 ºC
PG	Package	• FT = 48 HVQFN “Wettable”, 7 mm x 7 mm, 0.5p
SR	Silicon Revision	• A = Initial Mask Set • P = Production Mask Set

7.3.1 Package marking information

The K32W package has the following top-side marking:

- First line: aaaaaa
- Second line: aaaaaa
- Third line: mmmmm
- Fourth line: xxxywwxx

Table 64. Package marking

Identifier	Description
a	Reduced part number code, refer to Package marking table
m	Mask set
y	Year
w	Work week
x	NXP internal use

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

Table continues on the next page...

Table continued from the previous page...

Term	Definition
	• *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. NOTE The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions NOTE Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

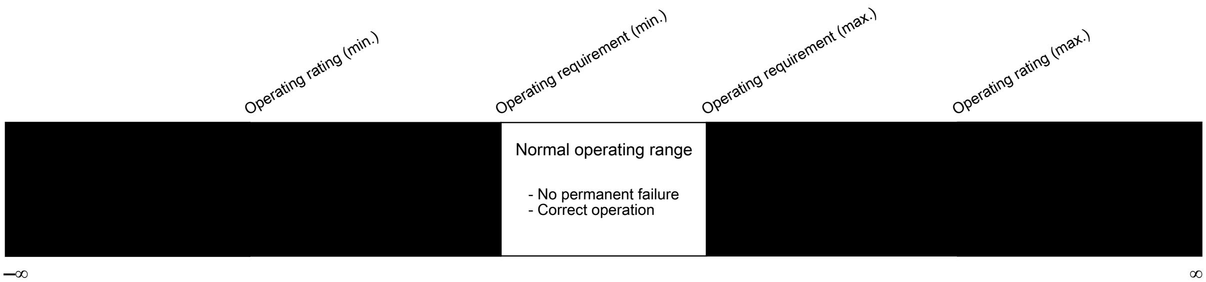
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.3 Typical-value conditions

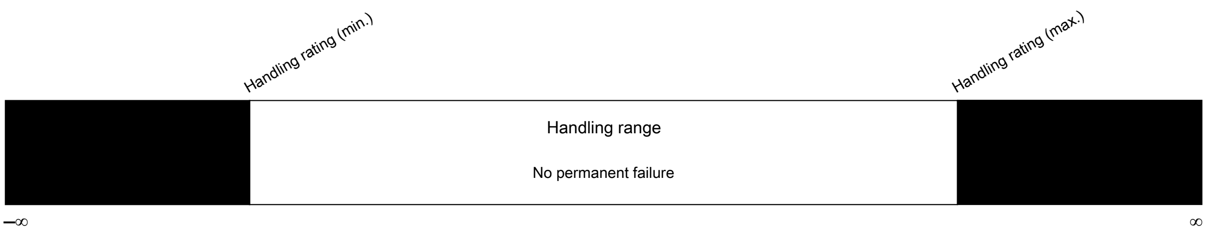
Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

8.4 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Abbreviations and Acronyms

The following table provides the list of abbreviations and acronyms their definitions.

Table 65. Abbreviations and Acronyms and their definition

Abbreviations and Acronyms	Definitions
ADC	Analog-to-Digital Converter
AXBS	Crossbar Switch
CMC	Core Mode Controller

Table continues on the next page...

Table 65. Abbreviations and Acronyms and their definition (continued)

Abbreviations and Acronyms	Definitions
CRC	Cyclic Redundancy Check
CTI	Cross Trigger Interface
DAP	Debug Access Port
DMA	Direct Memory Access
DSP	Digital Signal Processing
DWT	Data Watchpoint and Trace
EWM	External Watchdog Monitor
FRO	Free Running Oscillator
FMC	Flash Memory Controller
FPU	Floating Point Unit
GPIO	General-purpose Input and Output
I3C	Improved Inter-Integrated Circuit
ITM	Instruction Trace Macrocell
LPCMP	Low Power Comparator
LPI2C	Low Power Inter-Integrated Circuit
LPIT	Low Power Periodic Interrupt Timer
LPSPI	Low Power Serial Peripheral Interface
LPTMR	Low-Power Timer
LPUART	Low Power Universal Asynchronous Receiver/ Transmitter
MPU	Memory Protection Unit
MRCC	Module Reset and Clock Control
MSCM	Miscellaneous System Control Module
MU	Messaging Unit
NBU	Narrowband Unit
NPX	FMC with NVM PRINCE Encryption and Decryption
NVIC	Nested Vectored Interrupt Controller
NVM	Non-Volatile Memory
OSC	Oscillator
RFMC	Radio Mode Controller
RTC	Real Time Clock
SEMA42	Semaphore Module
SCG	System Clock Generator

Table continues on the next page...

Table 65. Abbreviations and Acronyms and their definition (continued)

Abbreviations and Acronyms	Definitions
SFA	Signal Frequency Analyzer
SMSCM	Secure Miscellaneous System Control Module
SPC	System Power Controller
SWD	Serial Wire Debug
TPIU	Trace Port Interface Unit
TPM	Timer/PWM Module
TRDC	Trusted Resource Domain Controller
TRNG	True Random Number Generator
TRGMUX	Trigger Multiplexer
TSTMR	Time Stamp Timer
VREF	Voltage Reference
WDOG	Watchdog
WUU	Wake-Up Unit

10 Revision history

The following table provides a revision history for this document.

Table 66. Revision History

Rev. No.	Date	Substantial Changes
0	Aug 2021	Initial release
1	Sept 2021	• Editorial updates • Updated the Front Matter Content • Updated the part number to K32W1480VFTAT to add 'T' for Tray • Updated the EdgeLock Secure Enclave in K32W1480 block diagram • Removed the bullet of 0 to 40 °C in Δf_{fro16K} in Free-running oscillator FRO-16K specifications • Updated the maximum values of Flash timing specifications • Updated the Voltage and current operating requirements table • Updated the typical value of $V_{LVDV\_HYS\_IO\_ABC}$ and $V_{HVD\_HYS\_SYS}$ in HVD, LVD, and POR operating requirements • Updated the typical values of VDD_CORE supply HVD and LVD Operating Ratings table in HVD, LVD, and POR operating requirements • Updated t_{POR} in Power mode transition operating behaviors table • Updated the description and values of VDD_IO_D in LDO_SYS electrical specifications

Table continues on the next page...

Table 66. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated the description of I2C/I3C/I/O pins in General switching specifications • Updated Voltage and current operating behaviors table • Added Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1) chart, Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1), and Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0) in CMP and 8-bit DAC electrical specifications • Updated maximum value of C_L in VREF operating requirements and values of V_{dev} in Voltage reference electrical specifications • Updated VDD_ANA symbol to VDD_IO_ABC and the maximum value of VREFH to VDD_IO_ABC in CMP and 8-bit DAC electrical specifications • Removed the references of NVM and ATx in pinout table Pinout Table • Updated Transmit and PLL Feature Summary and Receiver Feature Summary • Removed the references of SUOX and SOX from 32 kHz oscillator electrical specifications • Updated Power Consumption Operating Behaviors table
2	Dec 2021	• Updated the values under low-power consumption section in Front Matter Content • Updated Front Matter • Editorial updates • Added SIM_SDID value in Device Revision table • Updated the values of I_{ICIO}, and added another footnote to I_{ICIO} in Table 9 • Updated the first footnote in Table 14 • Updated the maximum value of I_{LOAD} at Normal drive mode in Table 15 • Updated I_{LOAD} parameter in Table 16 • Updated Table 20 • Updated the values of Jit_{osc} and $v_{ec\_extal32}$ in Table 31 • Added typical values to all parameters in Table 39 • Added new parameter VPA_2P4GHz in Table 40 • Updated the values amd added footnotes in Table 41 • Updated Table 42 • Updated the values of f_{ADCK} and R_{ADIN} in Table 47 • Updated Table 48 • Updated Table 49 • Updated typical and maximum value of V_{acc} in Table 51 • Added maximum value of f_{SCL} and minimum value of t_{SU_PP} in Table 59 • Added Abbreviations and Acronyms

Table continues on the next page...

Table 66. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated Table 43 • Removed NVM_SDO and RF_UART signals from Pinout Table • Updated Table 30
3	Dec 2022	• Updated Front Matter Content • Added SoC Power Consumption • Updated minimum and maximum value of Electrostatic discharge voltage, charged-device model (antenna pin) in ESD and Latch-Up Ratings to -250 V and +250 V • Updated complete ESD and Latch-Up Ratings • Updated the minimum Target VDD_CORE in Table 11 to 1.05 V • Updated Bluetooth LE 5.2 to Bluetooth LE 5.3 all over the document • Updated the ambient temperature from 120 °C to 105 °C all over the document • Updated the SIM_SDID in Device Revision Number table • Updated ARM to Arm in block diagram • Update the minimum value of VDD_CORE and VDD_LDO_CORE in Voltage and current operating requirements • Updated the values of V_{OUT_DCDC} in Table 14 • Removed $V_{switchWakeup}$ and $t_{switchWakeup}$ from Smart power switch • Removed the maximum value of $SEL_{BLE1M,\ 4+\ MHz}$ in Table 41 • Removed 26 MHz from Reference frequency bullet in Transmit and PLL Feature Summary • Updated the values in Power Consumption Operating Behaviors • Updated the maximum value of IEEE 802.15.4 Error Vector Magnitude in Table 43 from 4 % to 5 % • Updated Table 62 • Updated Package marking • Updated First Line of Package marking information from aaaaaaa to aaaaaa • Updated the minimum value and maximum value of VOUT_CORE for low drive strength in LDO_CORE electrical specifications • Updated the values of tPWDN and tDPWDN and removed t_{POR} and $t_{PORFAST}$ in Power mode transition operating behaviors • Updated Table 23 to show IDD values of 25 °C only • Added the values to Typical power-down mode RAM current adders • Updated Reference oscillator specification • Updated typical value of f_{ref} in 2.4 GHz radio transceiver electrical specification to show 32 MHz only

Table continues on the next page...

Table 66. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Added footnotes to Table 41 and Transmit and PLL Feature Summary • Removed the second footnote in Table 42 • Updated the "K32W1480VFTAT" and "K32W1480VFTAR" to "K32W1480VFTBT" and "K32W1480VFTBR" respectively all over the document • Updated the frequency from 48 MHz to 64 MHz in "Dedicated CM3 core running at up to 48MHz" in front matter

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

Definitions

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Date of release: 12/2022

Document identifier: K32W1480