PCAL9722

Ultra low-voltage translating 22-bit SPI I/O expander with Agile I/O features, interrupt output and reset

Rev. 1.1 — 1 May 2023 Product data sheet

1 General description

The PCAL9722 is a 22-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the SPI interface. The ultra low-voltage interface allows for direct connection to a microcontroller operating down to 1.1 V.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level down to 1.1 V to I/O devices operating at a different voltage level 1.65 V to 5.5 V. The PCAL9722 has built-in level shifting feature that makes these devices extremely flexible in mixed power supply systems where communication between incompatible I/O voltages is required, allowing seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SPI) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL9722: $V_{DD(SPI)}$ and $V_{DD(P)}$. $V_{DD(SPI)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL9722 is provided through $V_{DD(SPI)}$. $V_{DD(SPI)}$ should be connected to the V_{DD} of the external SPI lines. This indicates the V_{DD} level of the SPI to the PCAL9722, while the voltage level on Port P of the PCAL9722 is determined by the $V_{DD(P)}$.

The PCAL9722 works up to 5 MHz of SCLK speed and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include interrupts that can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The system master can reset the PCAL9722 in the event of a time-out or other improper operation by asserting a LOW in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the SPI state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the part.

The PCAL9722 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. As well, the $\overline{\text{INT}}$ output can be specified to activate on input pin edges. There are a large number of interrupt mask functions available to maximize flexibility.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without communication via the SPI bus. Thus, the PCAL9722 can remain a simple slave device. The input latch feature holds or latches the

input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed SPI address and allow up to two devices to share the same SPI bus.

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2 Features and benefits

- SPI bus to parallel port expander
- 5 MHz SPI bus
- Operating power supply voltage range of 1.1 V to 5.5 V on the SPI bus side
- Allows bidirectional voltage-level translation and GPIO expansion between 1.1 V to 5.5 V on SPI and 1.8 V, 2.5 V, 3.3 V, 5.5 V on Port P
- Low standby current consumption: 2.0 µA typical at 3.3 V V_{DD}
- Schmitt trigger action allows slow input transition and better switching noise immunity at the SPI inputs (SCLK, SDIN, $\overline{CS}$)
  - V_{hys} = 0.11 V (typical) at 1.1 V
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
  - V_{hys} = 0.55 V (typical) at 5.5 V
- 5.5 V tolerant I/O ports and SPI bus pins
- Active LOW reset input ($\overline{RESET}$)
- Open-drain active LOW interrupt output ($\overline{INT}$)
- Internal power-on reset
- Noise filter on SPI inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Package offered: HVQFN32

2.1 Agile I/O features

- Output port configuration: bank selectable or pin selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/pull-down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

2.2 Additional Agile I/O Plus features

- Interrupt edge specification on a bit-by-bit basis
- Interrupt individual clear without disturbing other events
- Read all interrupt events without clear
- Switch debounce hardware

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3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCAL9722HN	L9722	HVQFN32	plastic, thermal enhanced very thin quad flat package; 0.125 dimple wettable flank; 32 terminals; 0.5 mm pitch; 5 mm x 5 mm x 0.85 mm body	SOT617-3
PCAL9722HN/Q900 [1]	9722Q	HVQFN32	plastic, thermal enhanced very thin quad flat package; 0.125 dimple wettable flank; 32 terminals; 0.5 mm pitch; 5 mm x 5 mm x 0.85 mm body	SOT617-3

[1] Automotive AEC-Q100 (Grade 1) compliant. Contact NXP support for PPAP.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCAL9722HN	PCAL9722HNMP	HVQFN32	Reel 13” Q2/T3 SMD DP	6000	T_{amb} = -40 °C to +85 °C
PCAL9722HN/Q900 [1]	PCAL9722HN/Q900MP	HVQFN32	Reel 13” Q2/T3 SMD DP	6000	T_{amb} = -40 °C to +125 °C

[1] Automotive AEC-Q100 (Grade 1) compliant. Contact NXP support for PPAP.

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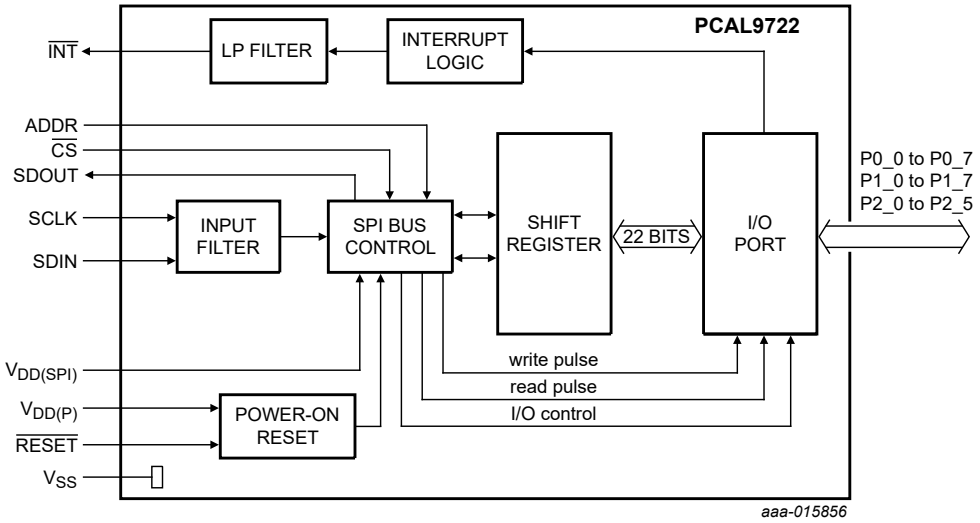
4 Block diagram



All I/Os are set to inputs at reset.

Figure 1. Block diagram of PCAL9722 (positive logic)

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5 Pinning information

5.1 Pinning

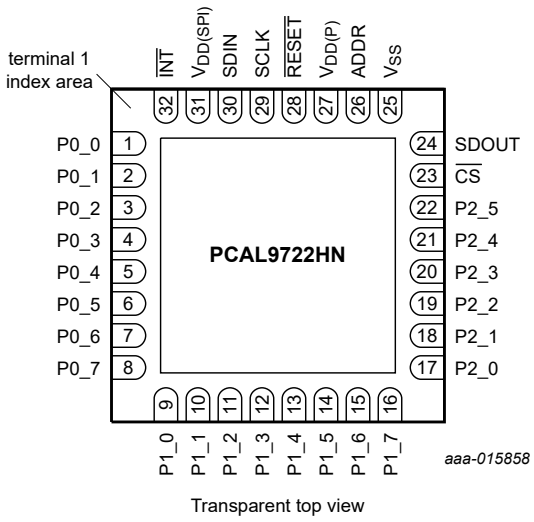

Figure 2. Pin configuration for HVQFN32

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
SCLK	29	I	SPI serial clock input
SDIN	30	I	SPI serial data input
$V_{DD(SPI)}$	31	power supply	Supply voltage of SPI bus. Connect directly to the V_{DD} of the external SPI bus master. Provides voltage-level translation.
$\overline{INT}$	32	O	Interrupt output. Connect to $V_{DD(SPI)}$ or $V_{DD(P)}$ through a pull-up resistor.
P0_0 [1]	1	I/O	Port 0 input/output 0
P0_1 [1]	2	I/O	Port 0 input/output 1
P0_2 [1]	3	I/O	Port 0 input/output 2
P0_3 [1]	4	I/O	Port 0 input/output 3
P0_4 [1]	5	I/O	Port 0 input/output 4
P0_5 [1]	6	I/O	Port 0 input/output 5
P0_6 [1]	7	I/O	Port 0 input/output 6
P0_7 [1]	8	I/O	Port 0 input/output 7
P1_0 [2]	9	I/O	Port 1 input/output 0
P1_1 [2]	10	I/O	Port 1 input/output 1
P1_2 [2]	11	I/O	Port 1 input/output 2
P1_3 [2]	12	I/O	Port 1 input/output 3
P1_4 [2]	13	I/O	Port 1 input/output 4

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Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
P1_5 [2]	14	I/O	Port 1 input/output 5
P1_6 [2]	15	I/O	Port 1 input/output 6
P1_7 [2]	16	I/O	Port 1 input/output 7
P2_0 [3]	17	I/O	Port 2 input/output 0
P2_1 [3]	18	I/O	Port 2 input/output 1
P2_2 [3]	19	I/O	Port 2 input/output 2
P2_3 [3]	20	I/O	Port 2 input/output 3
P2_4 [3]	21	I/O	Port 2 input/output 4
P2_5 [3]	22	I/O	Port 2 input/output 5
$\overline{CS}$	23	I	SPI chip select input
SDOUT	24	O	SPI serial data output
V_{SS}	25	ground	Supply ground
ADDR	26	I	Address input. Connect directly to $V_{DD(SPI)}$ or ground.
$V_{DD(P)}$	27	power supply	Supply voltage of PCAL9722 for Port P
$\overline{RESET}$	28	I	Active LOW reset input. Connect to $V_{DD(SPI)}$ through a pull-up resistor if no active connection is used.

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/Os are configured as inputs.
[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-on, all I/Os are configured as inputs.
[3] Pins P2_0 to P2_5 correspond to bits P2.0 to P2.5. At power-on, all I/Os are configured as inputs.

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6 Functional description

Refer to Figure 1.

6.1 Device address

Following a Chip Select ($\overline{CS}$) asserted condition (from HIGH to LOW), the bus master must send the target slave address followed by a read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation bit. The slave address of the PCAL9722 is shown in Figure 3. Slave address pin ADDR chooses one of two slave addresses. Table 4 shows all two slave addresses by connecting the ADDR pin to V_{SS}, or V_{DD}.

Table 4. PCAL9722 address map

ADDR	Device family high-order address bits						Variable portion of address	Address
	A6	A5	A4	A3	A2	A1	A0	
V_{SS}	0	1	0	0	0	0	0	40h
V_{DD}	0	1	0	0	0	0	1	42h

The last bit of the first byte defines the reading from or writing to the PCAL9722. When set to logic 1 a read is selected, while logic 0 selects a write operation.

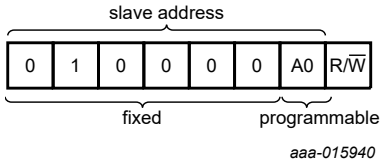

Figure 3. PCAL9722 address

6.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
SPI-bus slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	-	-	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

6.3 Pointer register and command byte

Following the first byte of the slave address, the bus master sends a command byte, which is write only and stored in the pointer register in the PCAL9722. The lowest 7 bits (B[6:0] in Table 6) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 4. At power-up or hardware reset, the pointer register defaults to 00h, with the AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the Auto-Increment bit is set (AI = 1), the seven low-order bits of the pointer register are automatically incremented after a read or write until the chip select ($\overline{CS}$) is de-asserted. This allows the user to program the

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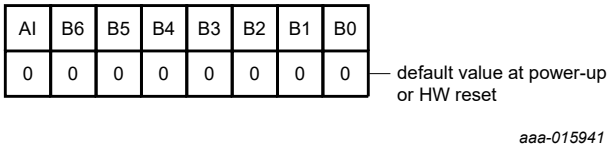
registers sequentially without modifying the pointer register. The contents of these bits will roll over to '000 0000' after the last register (address = 76h) is accessed. Unimplemented register addresses (reserved registers) are skipped. If more than 52 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and previously-written data will be overwritten. The de-assertion of chip select ($\overline{CS}$) condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI = 0), the 2 least significant bits are automatically incremented after a read or write for 3-register group which allows the user to program each of the 3-register group sequentially. If more than 3 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 1 is read first, the next 2nd byte will be input port 2, and next 3nd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are two special 6-register groups: output drive strength (40h~45h) and interrupt edge (60h~65h) registers will allow user to program each of the 6-register group sequentially. Only Output port configuration register location (5Ch) remains in the same location after a successive read or write.



AI = Auto-Increment

Figure 4. Pointer register bits

Table 6. Command byte

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx[1]
0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx[1]
0	0	0	0	0	1	0	02h	Input port 2	read byte	xxxx xxxx[1]
0	0	0	0	0	1	1	03h	reserved[2]	reserved	reserved
0	0	0	0	1	0	0	04h	Output port 0	read/write byte	1111 1111
0	0	0	0	1	0	1	05h	Output port 1	read/write byte	1111 1111
0	0	0	0	1	1	0	06h	Output port 2	read/write byte	1111 1111
0	0	0	0	1	1	1	07h	reserved[2]	reserved	reserved
0	0	0	1	0	0	0	08h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	1	0	0	1	09h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	1	0	1	0	0Ah	Polarity Inversion port 2	read/write byte	0000 0000
0	0	0	1	0	1	1	0Bh	reserved[2]	reserved	reserved
0	0	0	1	1	0	0	0Ch	Configuration port 0	read/write byte	1111 1111
0	0	0	1	1	0	1	0Dh	Configuration port 1	read/write byte	1111 1111
0	0	0	1	1	1	0	0Eh	Configuration port 2	read/write byte	1111 1111
-	-	-	-	-	-	-	0Fh to 3Fh	reserved[2]	reserved	reserved
1	0	0	0	0	0	0	40h	Output drive strength register port 0A	read/write byte	1111 1111
1	0	0	0	0	0	1	41h	Output drive strength register port 0B	read/write byte	1111 1111

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Table 6. Command byte*...continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	0	0	0	0	1	0	42h	Output drive strength register port 1A	read/write byte	1111 1111
1	0	0	0	0	1	1	43h	Output drive strength register port 1B	read/write byte	1111 1111
1	0	0	0	1	0	0	44h	Output drive strength register port 2A	read/write byte	1111 1111
1	0	0	0	1	0	1	45h	Output drive strength register port 2B	read/write byte	1111 1111
1	0	0	0	1	1	0	46h	reserved[2]	reserved	reserved
1	0	0	0	1	1	1	47h	reserved[2]	reserved	reserved
1	0	0	1	0	0	0	48h	Input latch register port 0	read/write byte	0000 0000
1	0	0	1	0	0	1	49h	Input latch register port 1	read/write byte	0000 0000
1	0	0	1	0	1	0	4Ah	Input latch register port 2	read/write byte	0000 0000
1	0	0	1	0	1	1	4Bh	reserved[2]	reserved	reserved
1	0	0	1	1	0	0	4Ch	Pull-up/pull-down enable register port 0	read/write byte	0000 0000
1	0	0	1	1	0	1	4Dh	Pull-up/pull-down enable register port 1	read/write byte	0000 0000
1	0	0	1	1	1	0	4Eh	Pull-up/pull-down enable register port 2	read/write byte	0000 0000
1	0	0	1	1	1	1	4Fh	reserved[2]	reserved	reserved
1	0	1	0	0	0	0	50h	Pull-up/pull-down selection register port 0	read/write byte	1111 1111
1	0	1	0	0	0	1	51h	Pull-up/pull-down selection register port 1	read/write byte	1111 1111
1	0	1	0	0	1	0	52h	Pull-up/pull-down selection register port 2	read/write byte	1111 1111
1	0	1	0	0	1	1	53h	reserved[2]	reserved	reserved
1	0	1	0	1	0	0	54h	Interrupt mask register port 0	read/write byte	1111 1111
1	0	1	0	1	0	1	55h	Interrupt mask register port 1	read/write byte	1111 1111
1	0	1	0	1	1	0	56h	Interrupt mask register port 2	read/write byte	1111 1111
1	0	1	0	1	1	1	57h	reserved[2]	reserved	reserved
1	0	1	1	0	0	0	58h	Interrupt status register port 0	read byte	0000 0000
1	0	1	1	0	0	1	59h	Interrupt status register port 1	read byte	0000 0000
1	0	1	1	0	1	0	5Ah	Interrupt status register port 2	read byte	0000 0000
1	0	1	1	0	1	1	5Bh	reserved[2]	reserved	reserved
1	0	1	1	1	0	0	5Ch[3]	Output port configuration register	read/write byte	0000 0000
1	0	1	1	1	0	1	5Dh	reserved[2]	reserved	reserved
1	0	1	1	1	1	0	5Eh	reserved[2]	reserved	reserved
1	0	1	1	1	1	1	5Fh	reserved[2]	reserved	reserved
1	1	0	0	0	0	0	60h	Interrupt edge register port 0A	read/write byte	0000 0000

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Table 6. Command byte*...continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	1	0	0	0	0	1	61h	Interrupt edge register port 0B	read/write byte	0000 0000
1	1	0	0	0	1	0	62h	Interrupt edge register port 1A	read/write byte	0000 0000
1	1	0	0	0	1	1	63h	Interrupt edge register port 1B	read/write byte	0000 0000
1	1	0	0	1	0	0	64h	Interrupt edge register port 2A	read/write byte	0000 0000
1	1	0	0	1	0	1	65h	Interrupt edge register port 2B	read/write byte	0000 0000
1	1	0	0	1	1	0	66h	reserved[2]	reserved	reserved
1	1	0	0	1	1	1	67h	reserved[2]	reserved	reserved
1	1	0	1	0	0	0	68h	Interrupt clear register port 0	write byte	0000 0000
1	1	0	1	0	0	1	69h	Interrupt clear register port 1	write byte	0000 0000
1	1	0	1	0	1	0	6Ah	Interrupt clear register port 2	write byte	0000 0000
1	1	0	1	0	1	1	6Bh	reserved[2]	reserved	reserved
1	1	0	1	1	0	0	6Ch	Input status port 0	read byte	xxxx xxxx[1]
1	1	0	1	1	0	1	6Dh	Input status port 1	read byte	xxxx xxxx[1]
1	1	0	1	1	1	0	6Eh	Input status port 2	read byte	xxxx xxxx[1]
1	1	0	1	1	1	1	6Fh	reserved[2]	reserved	reserved
1	1	1	0	0	0	0	70h	Individual pin output port 0 configuration register	read/write byte	0000 0000
1	1	1	0	0	0	1	71h	Individual pin output port 1 configuration register	read/write byte	0000 0000
1	1	1	0	0	1	0	72h	Individual pin output port 2 configuration register	read/write byte	0000 0000
1	1	1	0	0	1	1	73h	reserved[2]	reserved	reserved
1	1	1	0	1	0	0	74h	Switch debounce enable 0	read/write byte	0000 0000
1	1	1	0	1	0	1	75h	Switch debounce enable 1	read/write byte	0000 0000
1	1	1	0	1	1	0	76h	Switch debounce count	read/write byte	0000 0000
-	-	-	-	-	-	-	77h to 7Fh	reserved[2]	reserved	reserved

[1] Undefined.
[2] These registers marked "reserved" should not be written, and the master will not be acknowledged when accessed.
[3] Successive read and write accesses to remain at this register address.

6.4 Register descriptions

6.4.1 Input port registers (00h, 01h, 02h)

The Input port registers (registers 00h, 01h, 02h) reflect the incoming logic levels of the pins. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. If a pin is configured as an output (registers 04h, 05h, 06h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 5Ch and registers 70h, 71h, 72h), the input port value is forced to 0. An Input port register group read operation is performed as described in Section 7.5.

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After reading input port registers, all interrupts will be cleared.

Table 7. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 8. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Table 9. Input port 2 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	0 (NA)	0 (NA)	X	X	X	X	X	X

6.4.2 Output port registers (04h, 05h, 06h)

The Output port registers (registers 04h, 05h, 06h) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register group write is described in Section 7.3 and a register group read is described in Section 7.5.

Table 10. Output port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 11. Output port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Table 12. Output port 2 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	O2.7	O2.6	O2.5	O2.4	O2.3	O2.2	O2.1	O2.0
Default	1 (NA)	1 (NA)	1	1	1	1	1	1

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6.4.3 Polarity inversion registers (08h, 09h, 0Ah)

The Polarity inversion registers (registers 08h, 09h, 0Ah) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register group write is described in Section 7.3 and a register group read is described in Section 7.5.

Table 13. Polarity inversion port 0 register (address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 14. Polarity inversion port 1 register (address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Table 15. Polarity inversion port 2 register (address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	N2.7	N2.6	N2.5	N2.4	N2.3	N2.2	N2.1	N2.0
Default	0 (NA)	0 (NA)	0	0	0	0	0	0

6.4.4 Configuration registers (0Ch, 0Dh, 0Eh)

The Configuration registers (registers 0Ch, 0Dh, 0Eh) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register group write is described in Section 7.3 and a register group read is described in Section 7.5.

Table 16. Configuration port 0 register (address 0Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 17. Configuration port 1 register (address 0Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

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Table 18. Configuration port 2 register (address 0Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
Default	1 (NA)	1 (NA)	1	1	1	1	1	1

6.4.5 Output drive strength registers (40h, 41h, 42h, 43h, 44h, 45h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41h CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41h CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See Section 8.1 for more details. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 19. Current control port 0A register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 20. Current control port 0B register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 21. Current control port 1A register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 22. Current control port 1B register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

Table 23. Current control port 2A register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.3		CC2.2		CC2.1		CC2.0	
Default	1	1	1	1	1	1	1	1

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Table 24. Current control port 2B register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.7 (NA)		CC2.6 (NA)		CC2.5		CC2.4	
Default	1	1	1	1	1	1	1	1

6.4.6 Input latch registers (48h, 49h, 4Ah)

The input latch registers (registers 48h, 49h, 4Ah) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0, 1 and 2). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read ‘1’. The next read of the input port register bit 4 register should now read ‘0’.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and I/O pins return to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 25. Input latch port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 26. Input latch port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

Table 27. Input latch port 2 register (address 4Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	L2.7	L2.6	L2.5	L2.4	L2.3	L2.2	L2.1	L2.0

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Table 27. Input latch port 2 register (address 4Ah)*...continued*

Bit	7	6	5	4	3	2	1	0
Default	0 (NA)	0 (NA)	0	0	0	0	0	0

6.4.7 Pull-up/pull-down enable registers (4Ch, 4Dh, 4Eh)

The pull-up and pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.4.11 and Section 6.4.15). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 28. Pull-up/pull-down enable port 0 register (address 4Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 29. Pull-up/pull-down enable port 1 register (address 4Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

Table 30. Pull-up/pull-down enable port 2 register (address 4Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE2.7	PE2.6	PE2.5	PE2.4	PE2.3	PE2.2	PE2.1	PE2.0
Default	0 (NA)	0 (NA)	0	0	0	0	0	0

6.4.8 Pull-up/pull-down selection registers (50h, 51h, 52h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 31. Pull-up/pull-down selection port 0 register (address 50h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

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Table 32. Pull-up/pull-down selection port 1 register (address 51h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

Table 33. Pull-up/pull-down selection port 2 register (address 52h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD2.7	PUD2.6	PUD2.5	PUD2.4	PUD2.3	PUD2.2	PUD2.1	PUD2.0
Default	1 (NA)	1 (NA)	1	1	1	1	1	1

6.4.9 Interrupt mask registers (54h, 55h, 56h)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 34. Interrupt mask port 0 register (address 54h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 35. Interrupt mask port 1 register (address 55h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

Table 36. Interrupt mask port 2 register (address 56h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M2.7	M2.6	M2.5	M2.4	M2.3	M2.2	M2.1	M2.0
Default	1 (NA)	1 (NA)	1	1	1	1	1	1

6.4.10 Interrupt status registers (58h, 59h, 5Ah)

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

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When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register group read operation is described in Section 7.5.

Table 37. Interrupt status port 0 register (address 58h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 38. Interrupt status port 1 register (address 59h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

Table 39. Interrupt status port 2 register (address 5Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0
Default	0 (NA)	0 (NA)	0	0	0	0	0	0

6.4.11 Output port configuration register (5Ch)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 5). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (5Ch) before the Configuration register (0Ch, 0Dh, 0Eh) sets the port pins as outputs.

ODEN0 configures Port 0_x, ODEN1 configures Port 1_x, and ODEN2 configures Port 2_x.

Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (70h, 71h, 72h). See Section 6.4.15 for more information.

A register group read or write operation is not allowed on this register. Successive read or write accesses will remain at this register address.

Table 40. Output port configuration register (address 5Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					ODEN2	ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.4.12 Interrupt edge registers (60h, 61h, 62h and 63h, 64h, 65h)

The interrupt edge registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers (54h, 55h and 56h). If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the $\overline{INT}$ output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h, 01h or 02h) which can be latched with a corresponding '1' set in the Input Latch register (48h, 49h, 4Ah). If the Interrupt edge register entry is set to 11b, any edge, positive- or negative-going, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will

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require a negative-going edge to cause an interrupt event. These edge interrupt events are latched, regardless of the status of the Input Latch register (48h, 49h, 4Ah). These edged interrupts can be cleared in a number of ways: Reading input port registers (00h, 01h, 02h); setting the Interrupt Mask register (54h, 55h, 56h) to 1 (masked); setting the Interrupt Clear register (68h, 69h, 6Ah) to 1 (this is a write-only register); resetting the Interrupt Edge register (60h to 65h) back to 0. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 41. Interrupt edge port 0A register (address 60h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 42. Interrupt edge port 0B register (address 61h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 43. Interrupt edge port 1A register (address 62h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 44. Interrupt edge port 1B register (address 63h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Table 45. Interrupt edge port 2A register (address 64h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.3		IE2.2		IE2.1		IE2.0	
Default	0	0	0	0	0	0	0	0

Table 46. Interrupt edge port 2B register (address 65h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.7 (NA)		IE2.6 (NA)		IE2.5		IE2.4	
Default	0	0	0	0	0	0	0	0

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Table 47. Interrupt edge bits (IEx.x)

Bit 1	Bit 0	Description
0	0	level-triggered interrupt
0	1	positive-going (rising) edge triggered interrupt
1	0	negative-going (falling) edge triggered interrupt
1	1	any edge (positive or negative-going) triggered interrupt

6.4.13 Interrupt clear registers (68h, 69h, 6Ah)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{INT}$ will be cleared. After writing a logic 1 the bit returns to logic 0. A register group write operation is described in Section 7.3.

Table 48. Interrupt clear port 0 register (address 68h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Table 49. Interrupt clear port 1 register (address 69h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

Table 50. Interrupt clear port 2 register (address 6Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC2.7	IC2.6	IC2.5	IC2.4	IC2.3	IC2.2	IC2.1	IC2.0
Default	0 (NA)	0 (NA)	0	0	0	0	0	0

6.4.14 Input status registers (6Ch, 6Dh, 6Eh)

The read-only input status registers function exactly like Input Port 0, 1 and 2 (00h, 01h, 02h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration register (0Ch, 0Dh, 0Eh), and is also configured as open-drain (register 5Ch and 70h, 71h, 72h), the read for that pin will always return 0, otherwise that state of that pin is returned. A register group read operation is described in Section 7.5.

Table 51. Input status port 0 register (address 6Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	X	X	X	X	X	X	X	X

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Table 52. Input status port 1 register (address 6Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II1.7	II1.6	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	X	X	X	X	X	X	X	X

Table 53. Input status port 2 register (address 6Eh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II2.7	II2.6	II2.5	II2.4	II2.3	II2.2	II2.1	II2.0
Default	0 (NA)	0 (NA)	X	X	X	X	X	X

6.4.15 Individual pin output configuration registers (70h, 71h, 72h)

The individual pin output configuration registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration register (5Ch).

If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx will set that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (5Ch), the IOCRx, and finally the Configuration register (0Ch, 0Dh, 0Eh) to set the pins as outputs. A register group write operation is described in Section 7.3. A register group read operation is described in Section 7.5.

Table 54. Individual pin output configuration register 0 (address 70h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Table 55. Individual pin output configuration register 1 (address 71h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

Table 56. Individual pin output configuration register 2 (address 72h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR2.7	IOCR2.6	IOCR2.5	IOCR2.4	IOCR2.3	IOCR2.2	IOCR2.1	IOCR2.0
Default	0 (NA)	0 (NA)	0	0	0	0	0	0

6.4.16 Switch debounce enable registers (74h, 75h)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic

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requires an oscillator time base input and if this function is used, P0_0 is designated as the oscillator input. If P0_0 is not configured as input and if SD0.0 is not set to logic 1, then switch debounce logic is not connected to any pin. See Section 6.9 for additional information about Switch debounce logic functionality.

Table 57. Switch debounce enable Port 0 register (address 74h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 58. Switch debounce enable Port 1 register (address 75h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

6.4.17 Switch debounce count register (76h)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P0_0, determines the debounce time (for example, the debounce time will be 10 µs if this register is set to 0Ah and external oscillator frequency is 1 MHz). See Section 6.9 for further information.

Table 59. Switch debounce count register (address 76h) bit description [1]

Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

[1] The switch debounce logic is disabled if this register is set to 00h.

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above $V_{DD(P)}$ to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

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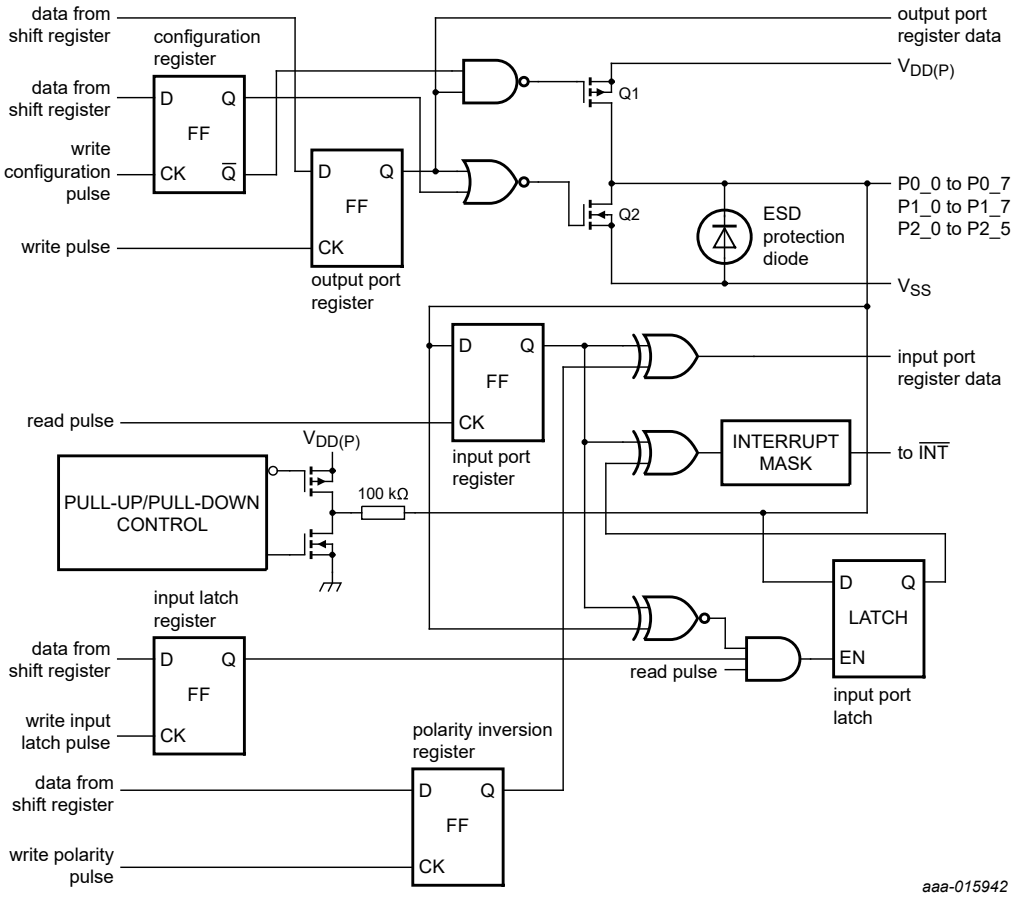

On power-up or reset, all registers return to default values.

Figure 5. Simplified schematic of P0_0 to P2_5

6.6 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCAL9722 in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that time, the reset condition is released and the PCAL9722 registers and SPI bus state machine initializes to their default states. After that, $V_{DD(P)}$ must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. See Section 8.2.

6.7 Reset input (RESET)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin LOW for a minimum of $t_{w(rst)}$. The PCAL9722 registers and SPI bus state machine are changed to their default state once $\overline{RESET}$ is LOW (0). When $\overline{RESET}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to $V_{DD(SPI)}$ if no active connection is used.

6.8 Interrupt output (INT)

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to $V_{DD(P)}$ or $V_{DD(SPI)}$ depending on the application. When any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system master (MCU) that one of input port states has

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changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

In order to enable the interrupt output, the following three conditions must be satisfied:

- The GPIO must be configured as an input port by writing "1" to configuration port registers (0Ch, 0Dh, 0Eh)
- The interrupt mask registers (54h, 55h, 56h) must set to "0" to unmask interrupt sources.
- The interrupt edge registers (60h to 65h) select what action on each input pin will cause an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The input latch registers (48h, 49h, 4Ah) control each input pin either to enable latched input state or non-latched input state. When input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and $\overline{INT}$ pin de-asserted by using one of the following methods and conditions:

- Power on reset (POR), hardware reset from $\overline{RESET}$ pin
- Read input port registers (00h, 01h, 02h)
- Write logic 1 to interrupt clear registers (68h, 69h, 6Ah)
- Write logic 1 to interrupt mask registers (54h, 55h, 56h)
- Write logic 0 to configuration registers (0Ch, 0Dh, 0Eh), set pin as output port.
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger and change latch to non-latch mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in interrupt edge registers

When using the input latch feature, the input pin state is latched. The interrupt is de-asserted only when data is read from the port that generated the interrupt. The interrupt reset occurs when $\overline{CS}$ is de-asserted (from LOW to HIGH). Any change of the inputs after resetting is detected and is transmitted as $\overline{INT}$.

6.9 Switch debounce circuitry

Mechanical switches do not make clean make-or-break connections and the contacts can ‘bounce’ for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PCAL9722 implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P0_1 to P0_7, P1_0 to P1_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration. The circuit block diagram (Figure 7) shows the functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector will reset the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output. Figure 8 shows the typical opening and closing switch debounce operation timing.

To use the debounce circuitry, set the port pins (P0_1 to P0_7, and P1_0 to P1_7) with switches attached in the Switch Debounce Enable 0 and 1 registers (74h, 75h). Connect an external oscillator signal on P0_0, which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (76h). The combination of time base of the external oscillator and the debounce count sets the qualification debounce period or t_{DP} in Figure 8. Note that all debounce counters will use the same time base and count, but they all function independently.

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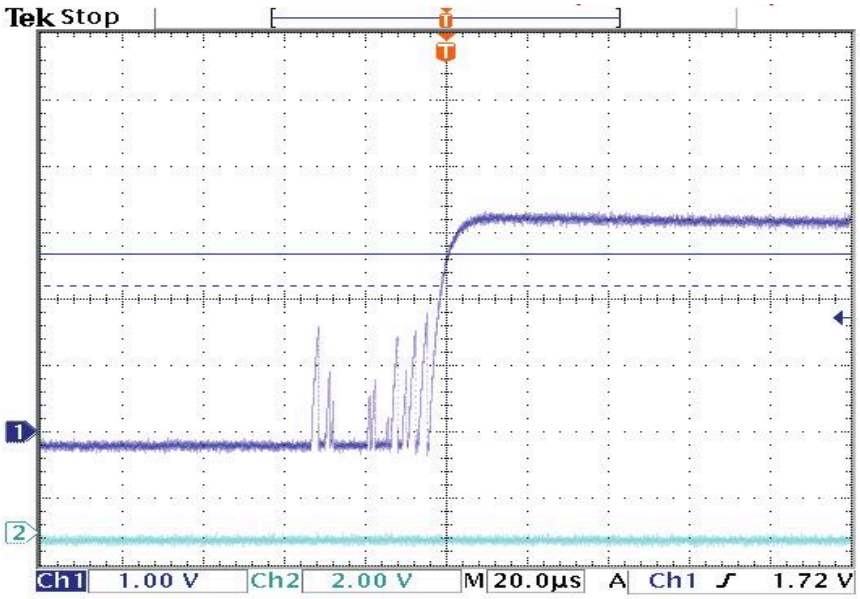
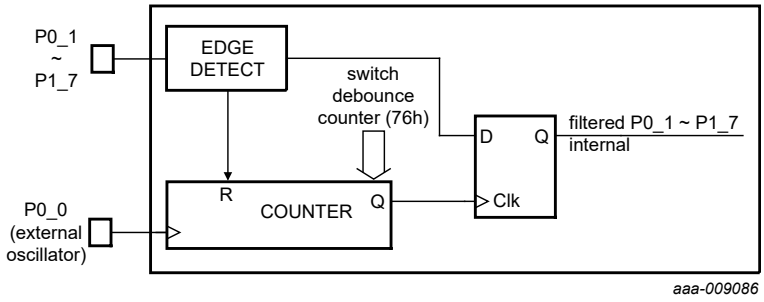


Figure 6. Switch contact bounce



The first time external clock is connected, external clock is required to wait 9 clock cycles for the debounce circuit in normal operation.

Figure 7. Debouncer block diagram

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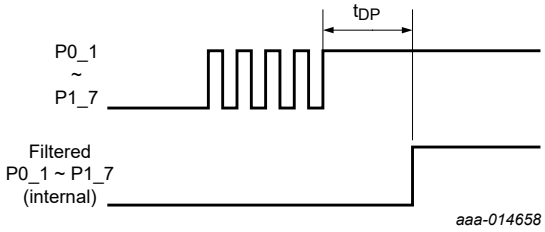

t_{DP} = [PERIOD of EXT CLOCK] * [Debounce counter(76h)] = 1 µs * 10 = 10 µs (if external clock = 1 MHz, debounce count register (76h) = 0Ah)

Figure 8. Switch debounce timing

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7 Characteristics of the 4-wire SPI serial-bus interface

The PCAL9722 communicates through an addressable SPI-compatible 4-wire serial bidirectional interface (read or write). The interface has three inputs and one output: serial clock (SCLK), active LOW chip select (/CS), serial data in (SDIN) and serial data out (SDOUT). /CS must be low to clock data into the device, and SDIN must be stable when sampled on the rising edge of SCLK. The PCAL9722 will ignore all activity on SCLK and SDIN except when /CS is low.

7.1 SPI-compatible 4-wire serial interface signals

$\overline{CS}$: The active LOW Chip Select line is used to activate and access the SPI slaves. As long as $\overline{CS}$ is HIGH, all slaves will ignore the clock and data inputs, and the data output is in high impedance state. Whenever this pin is in a logic LOW state, data can be transferred between the master and all slaves.

SCLK: Serial clock is provided by SPI master and determines the speed of the data transfer. All receiving and sending data are done synchronously (clocks the internal SPI shift register and the output driver) to this clock. It should be in its idle state (low) when $\overline{CS}$ is de-asserted (HIGH).

SDIN: Serial Data In is sampled on the rising edge of SCLK into the internal shift registers when $\overline{CS}$ is asserted (LOW). The device ignores all activity on SDIN when CS is de-asserted.

SDOUT: Serial Data Out is the pin on which the internal shift registers data is shifted out serially. SDOUT is in a high-impedance state until the $\overline{CS}$ pin goes to a logic LOW state. New data will appear at the SDOUT pin following the falling edge of SCLK during read cycle.

This SPI-compatible 4-wire serial interface allows multiple slaves to be connected to the same $\overline{CS}$. Each slave is identified using a unique slave address from ADDR input pin for the address encoding up to two possible slave addresses.

7.2 Data format

- SDIN Data input for write: at least 24 bits or [16 + (N*8)] bits (N is number of data byte to write; N ≥ 1)
- SDOUT Data output for read: data bytes start read back after first two bytes (slave address byte and register address byte).
- Clock frequency: up to 5 MHz

The slave address is assigned by the first 7-bit only two slave addresses available either 40h (ADDR=0) or 42h (ADDR=1) and the 8th bit is to indicate either write (R/W=0) or read (R/W=1) operation, and the register address (00h - 76h) on the serial map is specified by the next byte. The third byte transfers the data to the address specified by the register address that was written by the second byte and if the data subsequently continues even after this, the register address is automatically incremented for the fourth and subsequent bytes. As a result, it is possible to send the data continuously from the specified address. Data of less than one byte is ignored.

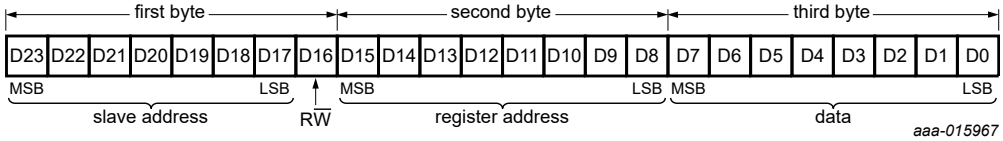

Figure 9. SPI data format

7.3 Write access sequence

In write operation, when 24 SCLK clock signals have been input during the low period of /CS, the SDIN is taken in at the rising edge of SCLK. If the number of SCLK clock signals during the low period of /CS is 23 or less, the

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SDIN is not taken in. If it is 25 or more, the register address is automatically incremented every time 1 byte is taken in.

Register write sequences always begin from the bus idle condition. The bus idle condition refers to the /CS being high and the SCLK being low.

The registers are written using the following write sequence for one byte of data (from a bus idle condition):

1. Drive $\overline{CS}$ low. This enables the internal shift register.
2. Shift 24 bits of data into the device in a MSB first fashion. Data must be stable during the rising edge of SCLK.
3. The first 7-bit is set for slave address and the 8th bit of the first byte data must be a '0' indicating it is a write only transfer.
4. The second 8 bits of data should be the address of the register that is intended to write.
5. After the last bit of data is transferred, drive SCLK low if there is no more data to be transferred.
6. De-assert $\overline{CS}$ (drive it high) to end of write cycle.

If fewer than 24 bits of data are transferred before de-asserting /CS then the data is ignored and the register will not be updated. The write transfer format is shown in the Figure 10 below.

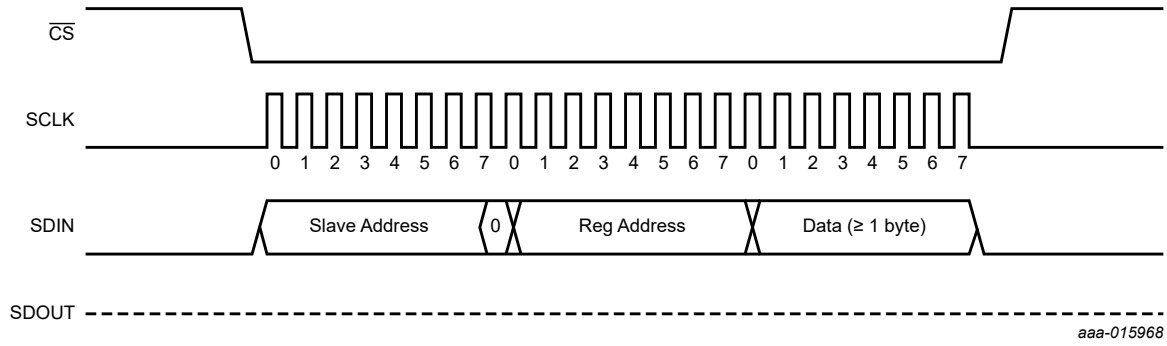

Figure 10. Write access

If more than 24 bits of data are transferred i.e. there are more than 24 clock pulses before de-asserting the CS, the register address is auto incremented. Auto Increment is discussed in a section below.

7.4 Auto increment

When the Auto-Increment bit is set (AI = 1; MSB bit) in register address (the second byte). The register address is incremented sequentially from the register which is indicated by the seven low-order bits in the pointer register and once the last address (76h) in the register map is reached, the address is rolled over to the first address (00h), and previously-written data will be overwritten.

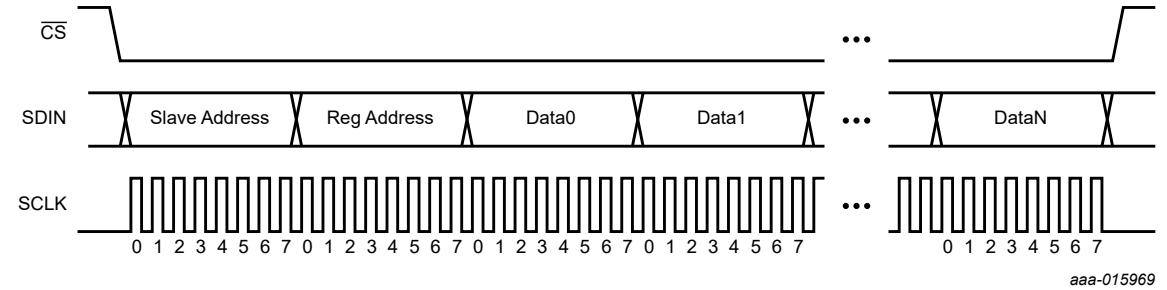

Figure 11. Write with auto increment

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7.5 Read Access Sequence

In read operation, the registers are read using the following read sequence (from a bus idle condition) as shown in Figure 12.

1. Drive $\overline{CS}$ low. This enables the internal shift register.
2. Shift 24 bits of data into the device in a MSB first fashion. Data must be stable during the rising edge of SCLK
3. The first 7-bit is set for slave address and the 8th bit of the first byte data must be a '1' indicating it is a read only transfer.
4. The second 8 bits of data should be the address of the register that is intended to read.
5. The third data byte is NOP (no operation) which is dummy data byte (don't care).
6. The read data is shifted out on SDOUT starting from dummy data byte when SCLK is continuously running from SPI master.
7. After the last bit of data is transferred, drive SCLK low if there is no more data to be transferred.
8. De-assert $\overline{CS}$ (drive it high) to end of read cycle.

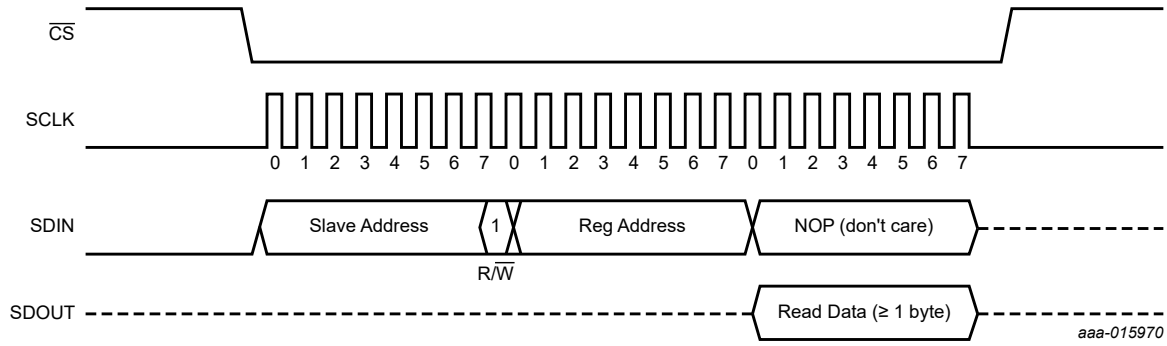

Figure 12. Read access

7.6 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' as shown in Figure 13, two PCAL9722 slave devices can be interfaced to a common SPI bus by connecting SDIN inputs together, connecting SCLK inputs together, connecting $\overline{CS}$ inputs together, and connecting SDOUT outputs together to a micro-controller master device. Each PCAL9722 device has address selection input pin ADDR to set the slave address.

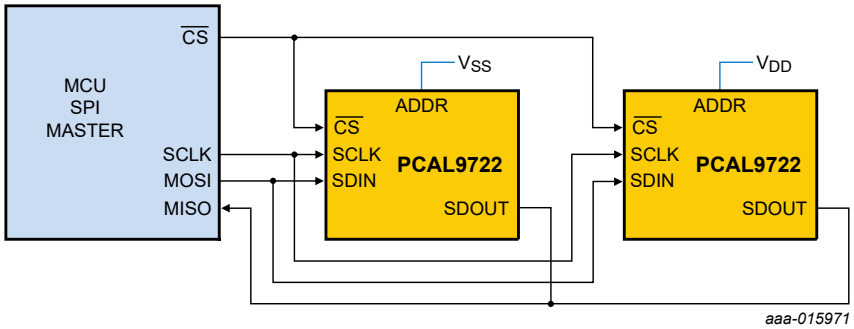

Figure 13. System level configuration

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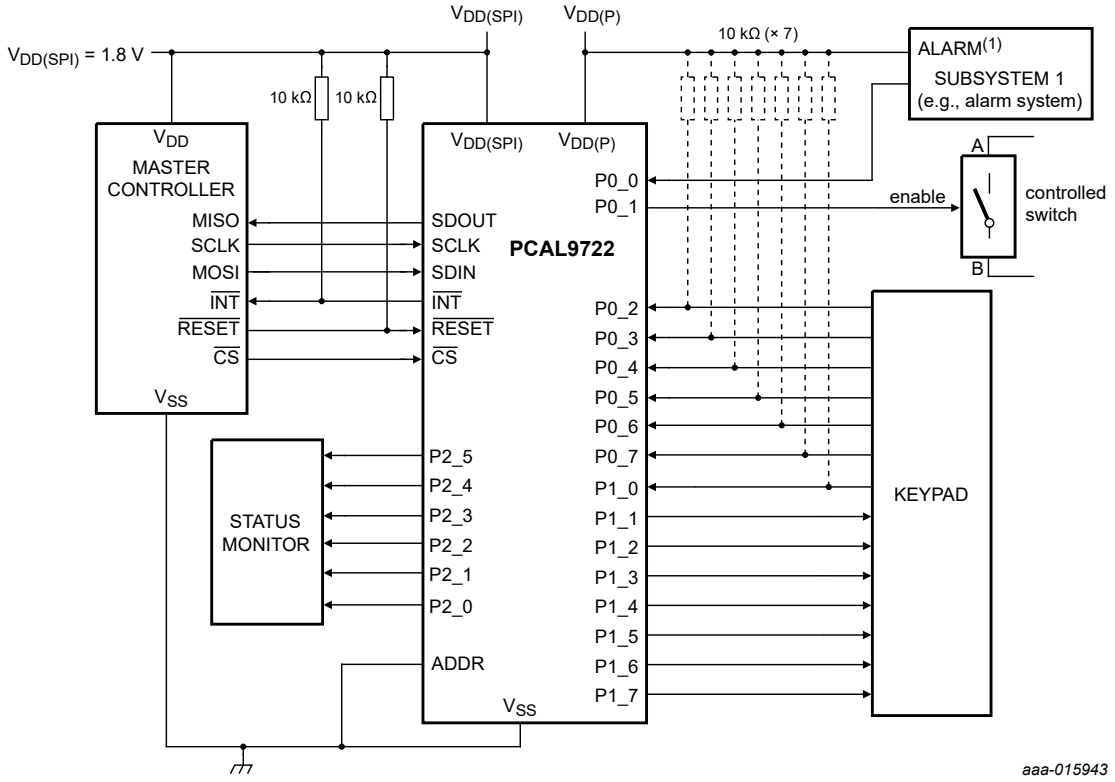
8 Application design-in information



Device address configured as 0100 000x for this example.

P0_0 and P0_2 through P1_0 are configured as inputs.

P0_1 and P1_1 through P1_7, and P2_0 through P2_5 are configured as outputs.

1. External resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed with internal pull-up or pull-down resistor option. If an output in the P port is configured as an output, there is no need for external pull-up resistors.

Figure 14. Typical application

8.1 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or ‘fingers’ that drive the I/O pad.

Figure 15 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50 %.

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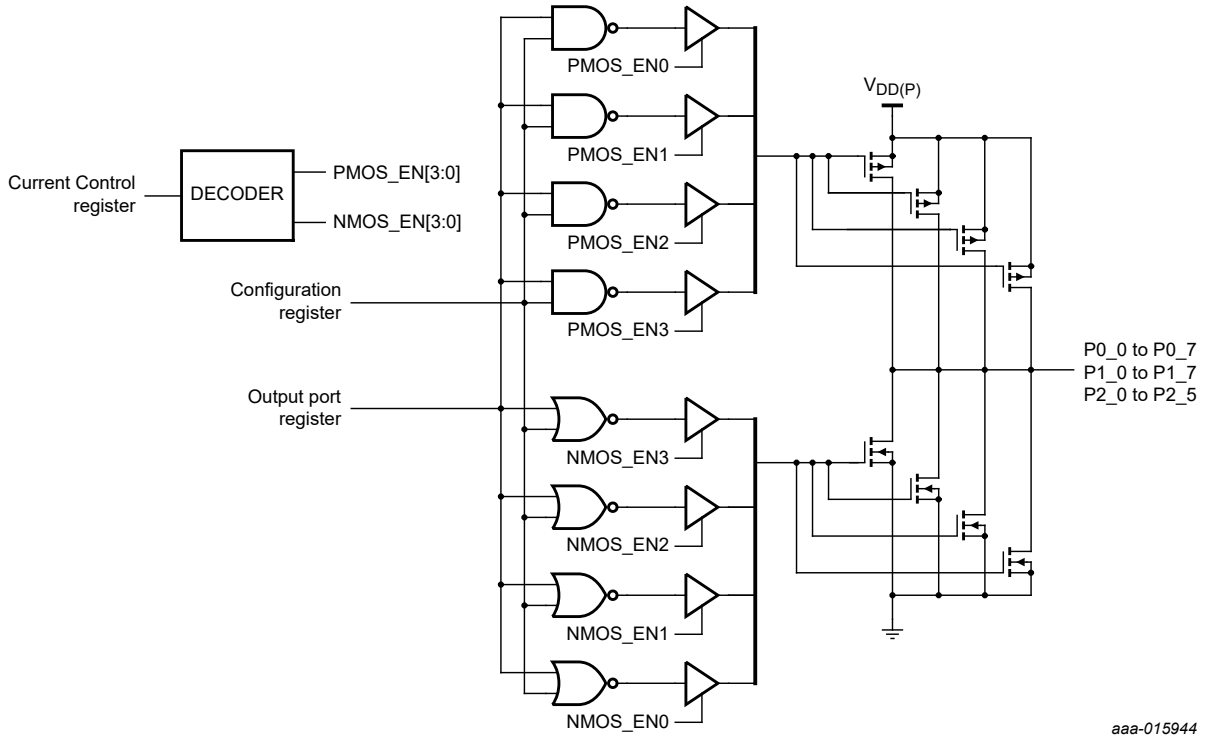

Figure 15. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

8.2 Power-on reset requirements

In the event of a glitch or data corruption, PCAL9722 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 16 and Figure 17.

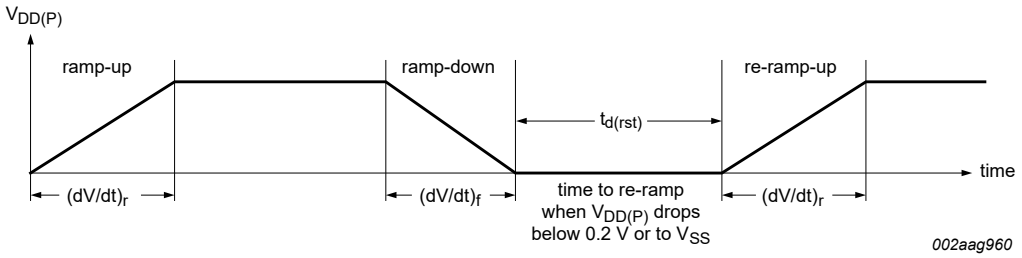

Figure 16. $V_{DD(P)}$ is lowered below 0.2 V or to 0 V and then ramped up to $V_{DD(P)}$

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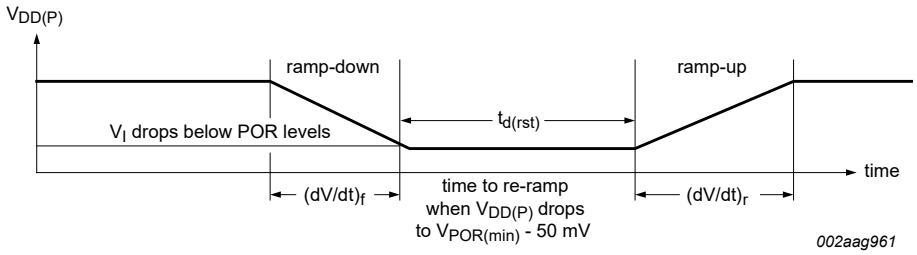

Figure 17. $V_{DD(P)}$ is lowered below the POR threshold, then ramped back up to $V_{DD(P)}$

Table 60 specifies the performance of the power-on reset feature for PCAL9722 for both types of power-on reset.

Table 60. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 16		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 16		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 16; re-ramp time when $V_{DD(P)}$ drops below 0.2 V or to V_{SS}		1	-	-	µs
		Figure 17; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)}$ - 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 18	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 18	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{DD(P)}$		0.7	-	-	V
		rising $V_{DD(P)}$		-	-	1.5	V

[1] Level that $V_{DD(P)}$ can glitch down to with a ramp rate at 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.
[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 18 and Table 60 provide more information on how to measure these specifications.

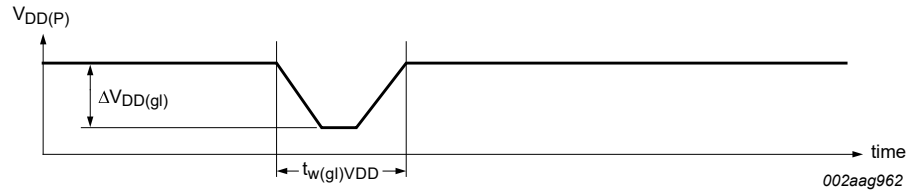

Figure 18. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the SPI bus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 19 and Table 60 provide more details on this specification.

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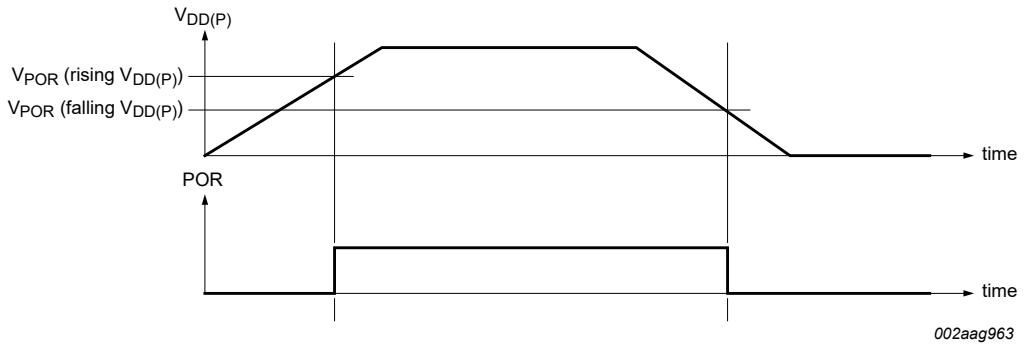

Figure 19. Power-on reset voltage (V_{POR})

8.3 Device current consumption with internal pull-up and pull-down resistors

The PCAL9722 integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in registers 50h, 51h and 52h, while the resistor is connected by the enable registers 4Ch, 4Dh and 4Eh. The configuration of the resistors is shown in Figure 5.

If the resistor is configured as a pull-up, that is, connected to V_{DD}, a current will flow from the $V_{DD(P)}$ pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current will flow from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 23 for a graph of supply current versus the number of pull-up resistors.

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9 Limiting values

Table 61. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(SPI)}$	SPI bus supply voltage			-0.5	+6.5	V
$V_{DD(P)}$	supply voltage port P			-0.5	+6.5	V
$V_{I(P)}$	input voltage on all ports		[1]	-0.5	+6.5	V
$V_{O(P)}$	output voltage on all ports		[1]	-0.5	+6.5	V
$V_{I(I)}$	input voltage on SPI-bus, $\overline{RESET}$, ADDR			-0.5	+6.5	V
$V_{O(I)}$	output voltage on SPI-bus, $\overline{INT}$			-0.5	+6.5	V
I_{IK}	input clamping current	ADDR, $\overline{RESET}$, SCLK, $\overline{CS}$; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$		-	±20	mA
		SDIN, SDOUT; $V_O < 0$ V or $V_O > V_{DD(SPI)}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; P port; V_O = 0 V to $V_{DD(P)}$		-	50	mA
		continuous; SDOUT, $\overline{INT}$; V_O = 0 V to $V_{DD(SPI)}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port; V_O = 0 V to $V_{DD(P)}$		-	25	mA
I_{DD}	supply current	continuous through V_{SS}		-	200	mA
$I_{DD(P)}$	supply current port P	continuous through $V_{DD(P)}$		-	160	mA
$I_{DD(SPI)}$	SPI bus supply current	continuous through $V_{DD(SPI)}$		-	10	mA
T_{stg}	storage temperature			-65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

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10 Recommended operating conditions

Table 62. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(SPI)}$	SPI supply voltage			1.1	5.5	V
$V_{DD(P)}$	supply voltage port P			1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCLK, SDIN, $\overline{CS}$, $\overline{RESET}$, ADDR		0.7 × $V_{DD(SPI)}$	5.5	V
		P2_5 to P0_0		0.7 × $V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	SCLK, SDIN, $\overline{CS}$, $\overline{RESET}$, ADDR		-0.5	0.3 × $V_{DD(SPI)}$	V
		P2_5 to P0_0		-0.5	0.3 × $V_{DD(P)}$	V
I_{OH}	HIGH-level output current	P2_5 to P0_0		-	10	mA
I_{OL}	LOW-level output current	P2_5 to P0_0		-	25	mA
T_{amb}	ambient temperature	operating in free air; PCAL9722HN		-40	+85	°C
		operating in free air; PCAL9722HN/Q900		-40	+150	°C

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11 Thermal characteristics

Table 63. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient on a JEDEC 2S2P board	HVQFN32 package	[1]	34.6	K/W

[1] The package thermal resistance is calculated in accordance with JESD 51-7.

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12 Static characteristics

Table 64. Static characteristics for PCAL9722HN

T_{amb} = -40 °C to +85 °C; $V_{DD(SPI)}$ = 1.1 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	I_I = -18 mA		-1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD(P)}$ or V_{SS}; I_O = 0 mA		-	1.2	1.5	V
V_{OH}	HIGH-level output voltage [2]	P port; I_{OH} = -8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.8	-	-	V
		$V_{DD(P)}$ = 3 V		2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.1	-	-	V
		P port; I_{OH} = -2.5 mA and CCX.X = 00b; I_{OH} = -5 mA and CCX.X = 01b; I_{OH} = -7.5 mA and CCX.X = 10b; I_{OH} = -10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.7	-	-	V
		$V_{DD(P)}$ = 3 V		2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.0	-	-	V
		SDOUT port					
		$V_{DD(SPI)} \leq$ 1.65 V, I_{OH} = -0.4 mA		0.8 × $V_{DD(SPI)}$	-	-	V
		$V_{DD(SPI)}$ ∴> 1.65 V, I_{OH} = -4 mA		$V_{DD(SPI)}$ - 0.3	-	-	V
V_{OL}	LOW-level output voltage [2]	P port; I_{OL} = 8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.25	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.20	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.3	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V
		SDOUT port					
		$V_{DD(SPI)} \leq$ 1.65 V, I_{OL} = 1.2 mA		-	-	0.2 × $V_{DD(SPI)}$	V

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Table 64. Static characteristics for PCAL9722HN*...continued*

T_{amb} = -40 °C to +85 °C; $V_{DD(SPI)}$ = 1.1 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
		$V_{DD(SPI)}$.∴> 1.65 V, I_{OL} = 4 mA		-	-	0.4	V
I_{OL}	LOW-level output current [3]	$\overline{INT}$; V_{OL} = 0.4 V; $V_{DD(P)}$ = 1.65 V to 5.5 V		3	[4]	-	mA
I_I	input current	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; $V_{DD(P)}$ = 1.65 V to 5.5 V; V_I = $V_{DD(SPI)}$ or V_{SS}		-	-	±1	µA
I_{IH}	HIGH-level input current	P port without internal pull-up resistor; V_I = $V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{IL}	LOW-level input current	P port without internal pull-up resistor; V_I = V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{DD}	supply current	$I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on ADDR, SDIN, $\overline{CS}$ and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs					
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 5 MHZ		-	500	750	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 5 MHZ		-	300	500	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 5 MHZ		-	200	350	µA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 0 MHZ		-	3	12	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 0 MHZ		-	2	6.5	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 0 MHZ		-	1.5	4.5	µA
		Active mode; $I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on SDIN, $\overline{CS}$, ADDR, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCLK} = 5 MHZ; continuous register read with 100 pF load on SDOUT					
		$V_{DD(P)}$ = 3.6 V to 5.5 V		-	2500	4200	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V		-	2200	3200	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V		-	1800	2800	µA
		with pull-ups enabled; $I_{DD(SPI)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCLK} = 0 kHz					
		$V_{DD(P)}$ = 1.65 V to 5.5 V		-	1.65	2.4	mA

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Table 64. Static characteristics for PCAL9722HN*...continued*

T_{amb} = -40 °C to +85 °C; $V_{DD(SPI)}$ = 1.1 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
ΔI_{DD}	additional quiescent supply current [5]	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; one input at $V_{DD(SPI)}$ - 0.6 V, other inputs at $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	30	µA
		P port; one input at $V_{DD(P)}$ - 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	80	µA
C_i	input capacitance [6]	V_I = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	6	7	pF
C_{io}	input/output capacitance [6]	$V_{I/O}$ = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7	8	pF
		$V_{I/O}$ = $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7.5	8.5	pF
$R_{pu(int)}$	internal pull-up resistance	input/output		50	100	150	kΩ
$R_{pd(int)}$	internal pull-down resistance	input/output		50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V or 3.6 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)}$ = $V_{DD(SPI)}$ = 3.3 V and T_{amb} = 25 °C.
[2] The total current sourced by all I/Os must be limited to 160 mA.
[3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0_0 to P0_7 and P1_0 to P1_7) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and $V_{DD(SPI)}$ = $V_{DD(P)}$ = 3.3 V. Typical value for $V_{DD(SPI)}$ = $V_{DD(P)}$ < 2.5 V, V_{OL} = 0.6 V.
[5] Internal pull-up/pull-down resistors disabled.
[6] Value not tested in production, but guaranteed by design and characterization.

Table 65. Static characteristics for PCAL9722HN/Q900

T_{amb} = -40 °C to +125 °C; $V_{DD(SPI)}$ = 1.1 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	I_I = -18 mA		-1.2	-	-	V
V_{POR}	power-on reset voltage	V_I = $V_{DD(P)}$ or V_{SS}; I_O = 0 mA		-	1.2	1.5	V
V_{OH}	HIGH-level output voltage [2]	P port; I_{OH} = -8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.8	-	-	V
		$V_{DD(P)}$ = 3 V		2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.1	-	-	V
		P port; I_{OH} = -2.5 mA and CCX.X = 00b; I_{OH} = -5 mA and CCX.X = 01b; I_{OH} = -7.5 mA and CCX.X = 10b; I_{OH} = -10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.7	-	-	V
		$V_{DD(P)}$ = 3 V		2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.0	-	-	V

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Table 65. Static characteristics for PCAL9722HN/Q900*...continued*

T_{amb} = -40 °C to +125 °C; $V_{DD(SPI)}$ = 1.1 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
		SDOUT port					
		$V_{DD(SPI)}$ ≤ 1.65 V, I_{OH} = -0.4 mA		0.8 × $V_{DD(SPI)}$	-	-	V
		$V_{DD(SPI)}$.∴> 1.65 V, I_{OH} = -4 mA		$V_{DD(SPI)}$ - 0.3	-	-	V
V_{OL}	LOW-level output voltage [2]	P port; I_{OL} = 8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.25	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.20	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.3	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V
		SDOUT port					
		$V_{DD(SPI)}$ ≤ 1.65 V, I_{OL} = 1.2 mA		-	-	0.2 × $V_{DD(SPI)}$	V
		$V_{DD(SPI)}$.∴> 1.65 V, I_{OL} = 4 mA		-	-	0.4	V
I_{OL}	LOW-level output current [3]	$\overline{INT}$; V_{OL} = 0.4 V; $V_{DD(P)}$ = 1.65 V to 5.5 V		3	[4]	-	mA
I_I	input current	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; $V_{DD(P)}$ = 1.65 V to 5.5 V; V_I = $V_{DD(SPI)}$ or V_{SS}		-	-	±1	µA
I_{IH}	HIGH-level input current	P port without internal pull-up resistor; V_I = $V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{IL}	LOW-level input current	P port without internal pull-up resistor; V_I = V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{DD}	supply current	$I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on ADDR, SDIN, $\overline{CS}$ and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs					
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 5 MHZ		-	500	750	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 5 MHZ		-	300	500	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 5 MHZ		-	200	350	µA

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Table 65. Static characteristics for PCAL9722HN/Q900*...continued*

T_{amb} = -40 °C to +125 °C; $V_{DD(SPI)}$ = 1.1 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 0 MHZ		-	3	12	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 0 MHZ		-	2	6.5	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 0 MHZ		-	1.5	4.5	µA
		Active mode; $I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on SDIN, $\overline{CS}$, ADDR, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCLK} = 5 MHZ; continuous register read with 100 pF load on SDOUT					
		$V_{DD(P)}$ = 3.6 V to 5.5 V		-	2500	4200	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V		-	2200	3200	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V		-	1800	2800	µA
		with pull-ups enabled; $I_{DD(SPI)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCLK} = 0 kHz					
		$V_{DD(P)}$ = 1.65 V to 5.5 V		-	1.65	2.4	mA
ΔI_{DD}	additional quiescent supply current [5]	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; one input at $V_{DD(SPI)}$ - 0.6 V, other inputs at $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	30	µA
		P port; one input at $V_{DD(P)}$ - 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	80	µA
C_i	input capacitance [6]	V_I = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	6	7	pF
C_{io}	input/output capacitance [6]	$V_{I/O}$ = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7	8	pF
		$V_{I/O}$ = $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7.5	8.5	pF
$R_{pu(int)}$	internal pull-up resistance	input/output		50	100	150	kΩ
$R_{pd(int)}$	internal pull-down resistance	input/output		50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V or 3.6 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)}$ = $V_{DD(SPI)}$ = 3.3 V and T_{amb} = 25 °C.
[2] The total current sourced by all I/Os must be limited to 160 mA.
[3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0_0 to P0_7 and P1_0 to P1_7) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and $V_{DD(SPI)}$ = $V_{DD(P)}$ = 3.3 V. Typical value for $V_{DD(SPI)}$ = $V_{DD(P)}$ < 2.5 V, V_{OL} = 0.6 V.
[5] Internal pull-up/pull-down resistors disabled.
[6] Value not tested in production, but guaranteed by design and characterization.

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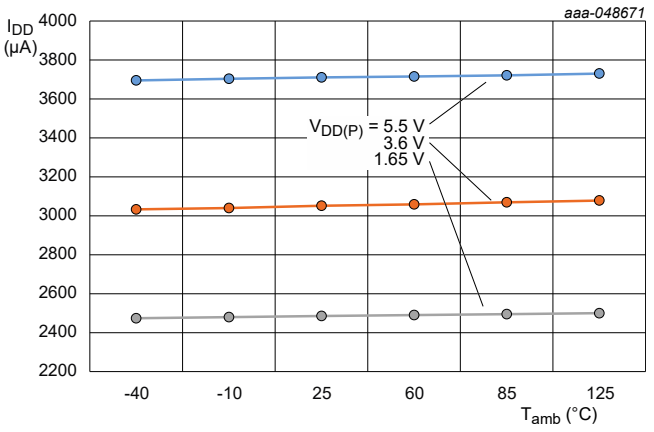
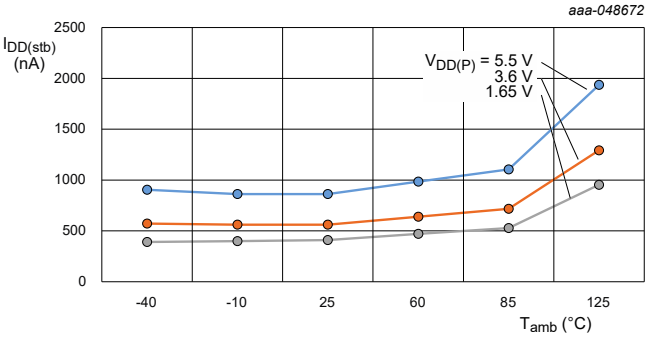
12.1 Typical characteristics



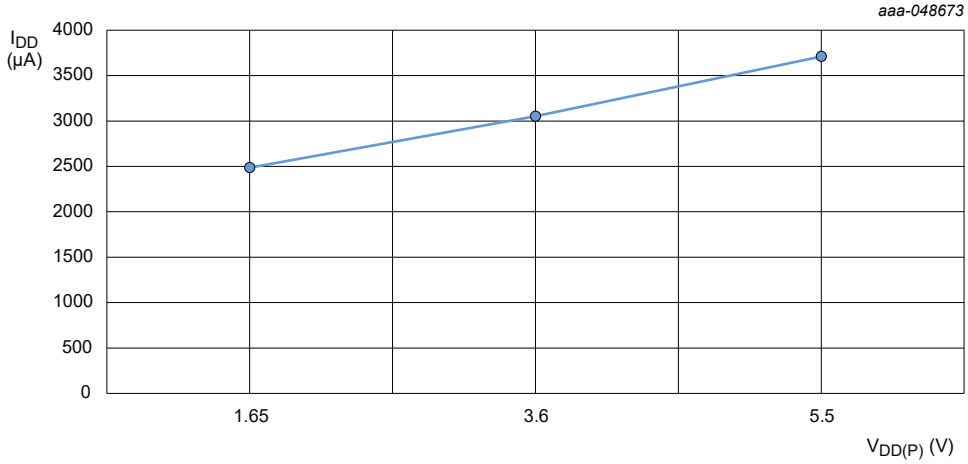
$I_{DD} = I_{DD(SPI)} + I_{DD(P)}$, f_{SCLK} = 5 MHz

Figure 20. Supply current versus ambient temperature



$I_{DD} = I_{DD(SPI)} + I_{DD(P)}$, f_{SCLK} = 0 Hz

Figure 21. Standby supply current versus ambient temperature



T_{amb} = 25 °C; $I_{DD} = I_{DD(SPI)} + I_{DD(P)}$, f_{SCLK} = 5 MHz

Figure 22. Supply current versus supply voltage

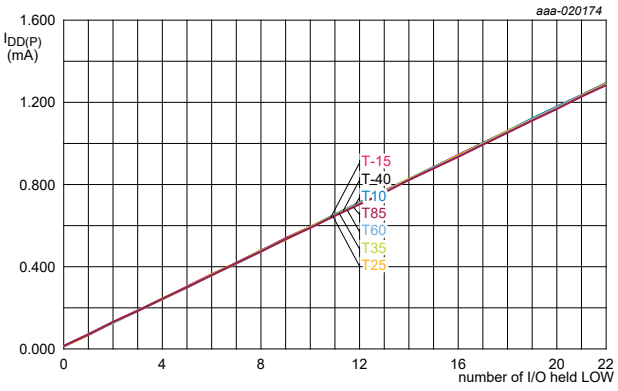


Figure 23. Supply current versus number of I/O held LOW

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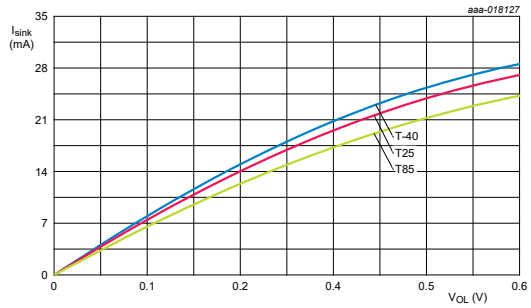
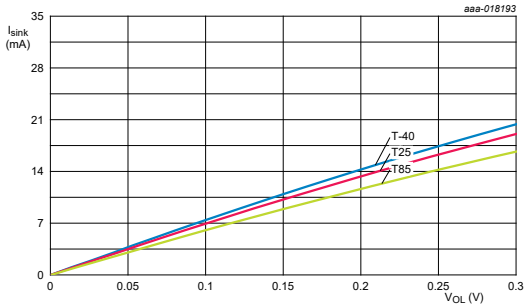
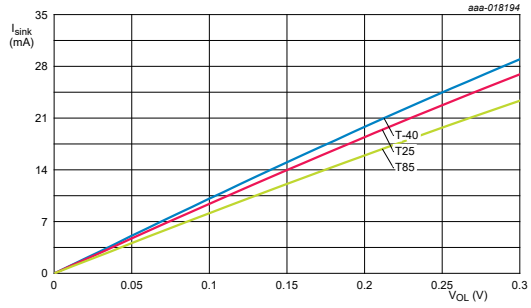


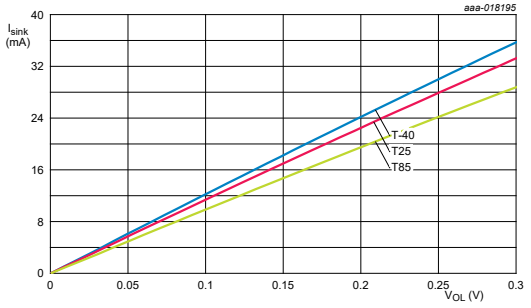
a. $V_{DD(P)}$ = 1.65 V



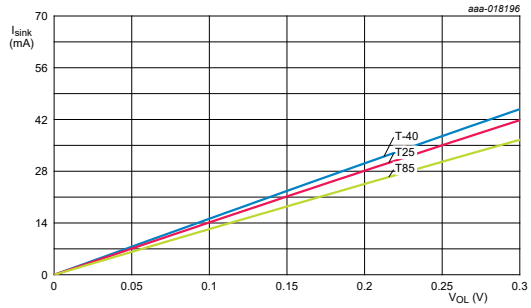
b. $V_{DD(P)}$ = 1.8 V



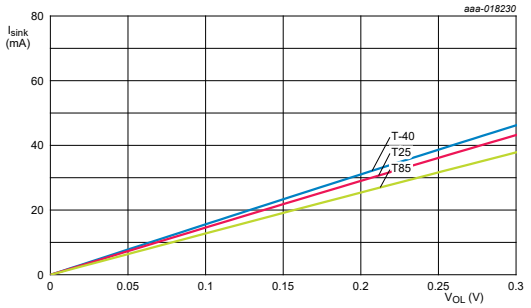
c. $V_{DD(P)}$ = 2.5 V



d. $V_{DD(P)}$ = 3.3 V



e. $V_{DD(P)}$ = 5 V



f. $V_{DD(P)}$ = 5.5 V

Figure 24. I/O sink current vs LOW-level output voltage

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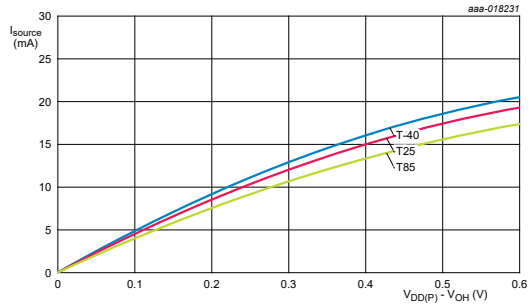
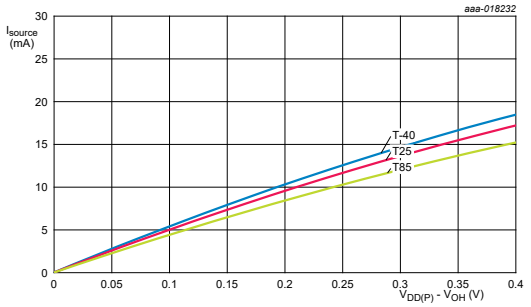
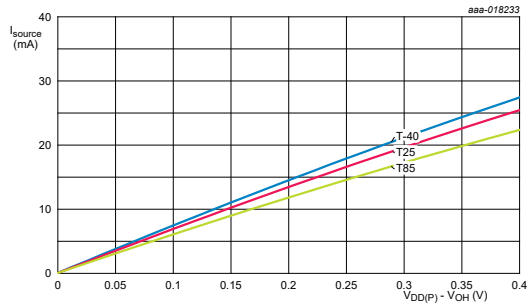


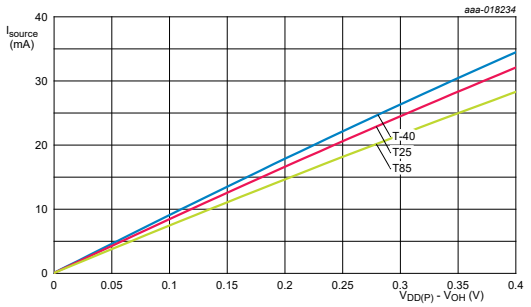
a. $V_{DD(P)}$ = 1.65 V



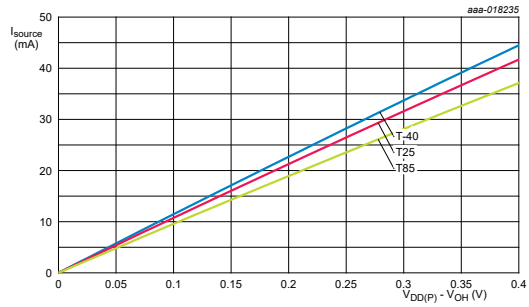
b. $V_{DD(P)}$ = 1.8 V



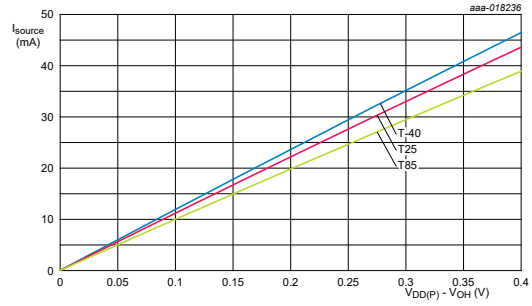
c. $V_{DD(P)}$ = 2.5 V



d. $V_{DD(P)}$ = 3.3 V



e. $V_{DD(P)}$ = 5 V



f. $V_{DD(P)}$ = 5.5 V

Figure 25. I/O source current vs HIGH-level output voltage

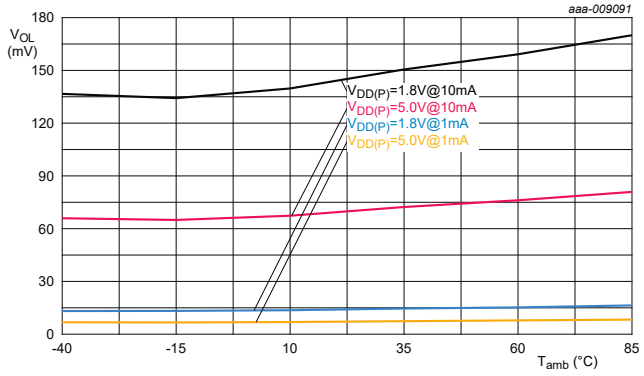


Figure 26. LOW-level output voltage vs temperature

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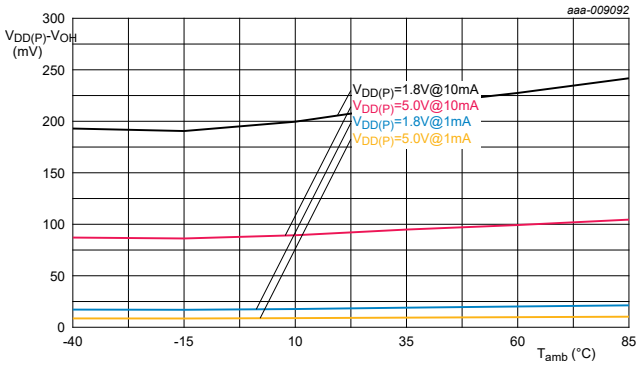

Figure 27. I/O high voltage vs temperature

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13 Dynamic characteristics

Table 66. SPI bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 29.

Symbol	Parameter	Conditions		$V_{DD(SPI)} \leq 1.65$		$V_{DD(SPI)} \leq 5.5$		
				Min	Max	Min	Max	Unit
f_{SCLK}	maximum input clock frequency			-	2	-	5	MHz
t_{LOW}	LOW period of the SCLK clock			250	-	100	-	ns
t_{HIGH}	HIGH period of the SCLK clock			250	-	100	-	ns
t_{DS}	SDIN to SCLK set-up time			20	-	20	-	ns
t_{DH}	SDIN to SCLK hold time			30	-	30	-	ns
t_{CSS}	CSn to SCLK rise set-up time			100	-	100	-	ns
t_{CS_HI}	minimum CSn de-asserted HIGH time			200	-	200	-	ns
t_{CSH}	SCLK fall to CSn de-asserted hold time			20	-	20	-	ns
$t_{DIS(SDOUT)}$	SDOUT disable time	C_L = 100 pF		-	150	-	150	ns
$t_{V(SDOUT)}$	SDOUT valid time	C_L = 100 pF		-	200	-	200	ns

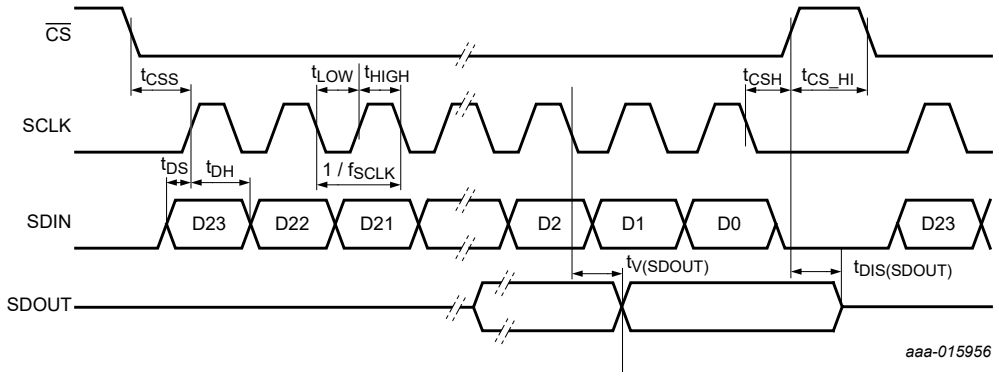

Figure 28. Definition of timing

Table 67. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 31.

Symbol	Parameter	Conditions		SPI bus		Unit
				Min	Max	
$t_{w(rst)}$	reset pulse width			150	-	ns
$t_{rec(rst)}$	reset recovery time			500	-	ns
t_{rst}	reset time		[1]	600	-	ns

[1] Minimum time for SDOUT to become HIGH.

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Table 68. Switching characteristics

Over recommended operating free air temperature range; C_L ≤ 100 pF; unless otherwise specified. See Figure 30.

Symbol	Parameter	Conditions		SPI bus		Unit
				Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$		-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCLK to $\overline{INT}$		-	1	µs
$t_{v(Q)}$	data output valid time	from SCLK to P port		-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCLK		30	-	ns
$t_{h(D)}$	data input hold time	from P port to SCLK		10	-	ns

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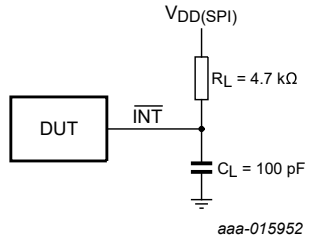
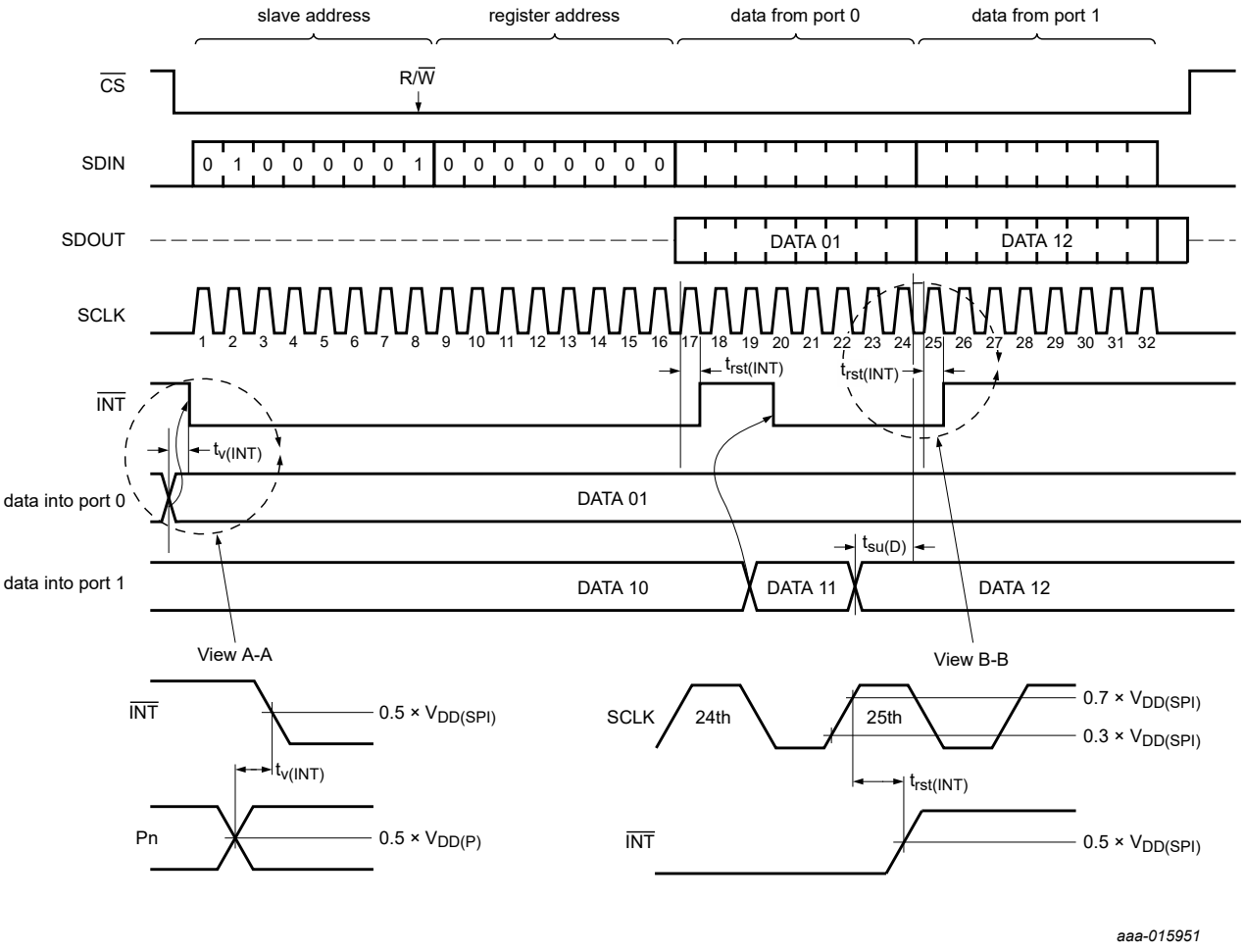
14 Parameter measurement information



a. Interrupt load configuration



C_L includes probe and jig capacitance.
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.
All parameters and waveforms are not applicable to all devices.
b. Voltage waveforms

Figure 29. Interrupt load circuit and voltage waveforms

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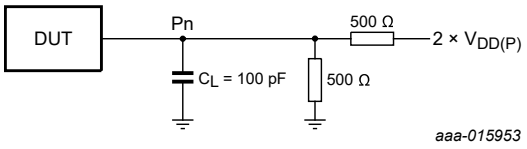
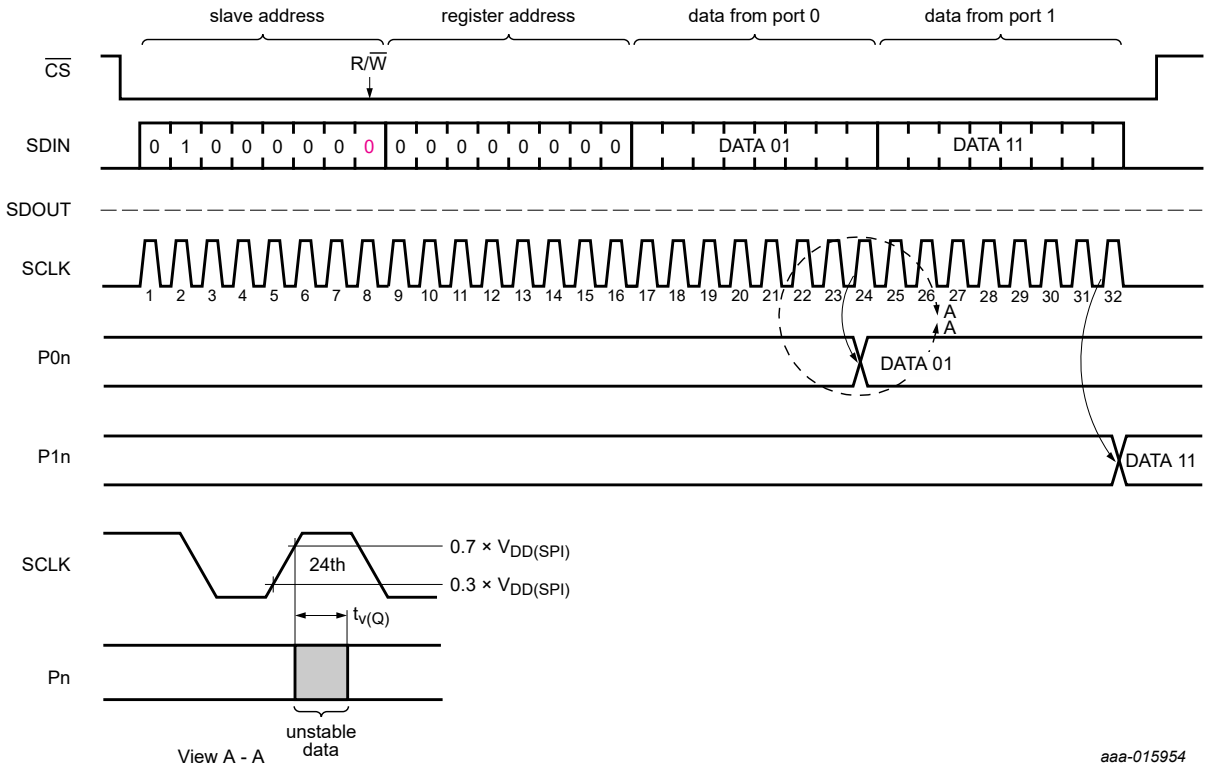
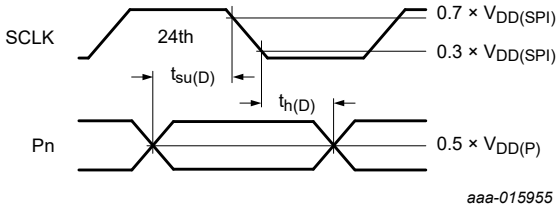


a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



C_L includes probe and jig capacitance.

$t_{v(Q)}$ is measured from 0.7 × $V_{DD(SPI)}$ on SCLK to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

c. Read mode (R/$\overline{W}$ = 1)

Figure 30. P port load circuit and voltage waveforms

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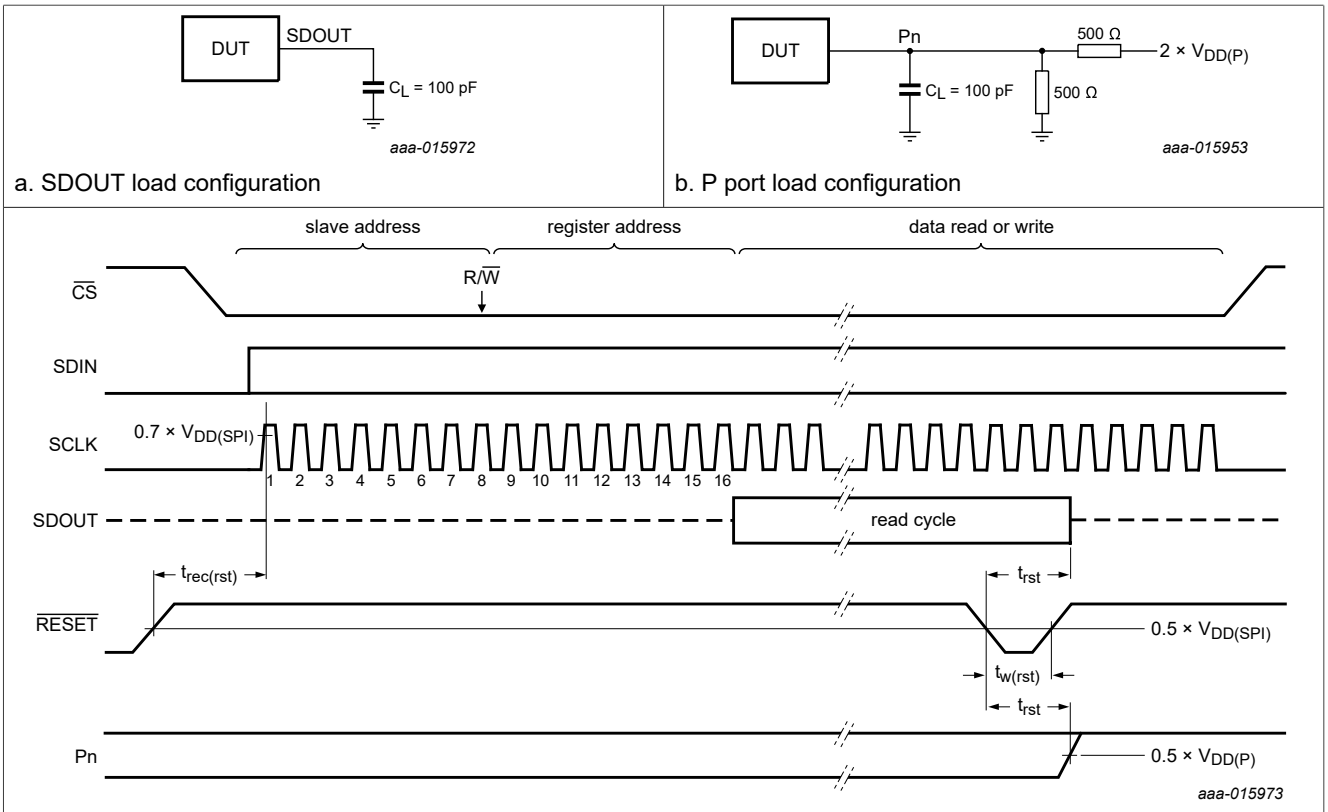

a. SDOUT load configuration

b. P port load configuration

c. $\overline{RESET}$ timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

Figure 31. Reset load circuits and voltage waveforms

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15 Package information

15.1 Package summary

Terminal position code Q: (quad)

Package type descriptive code: HVQFN32

Package type industry code: HVQFN32

Package style descriptive code: HVQFN (thermal enhanced very thin quad flatpack; no leads)

Package body material type: P (plastic)

JEDEC package outline code: MO-220

Mounting method type: S (surface mount)

Issue date: 22-10-2002

Manufacturer package code: 98ASA01350D

Table 69. Package summary

Parameter	Min	Nom	Max	Unit
package length	4.9	5	5.1	mm
package width	4.9	5	5.1	mm
seated height	0.8	0.85	1	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	32	-	

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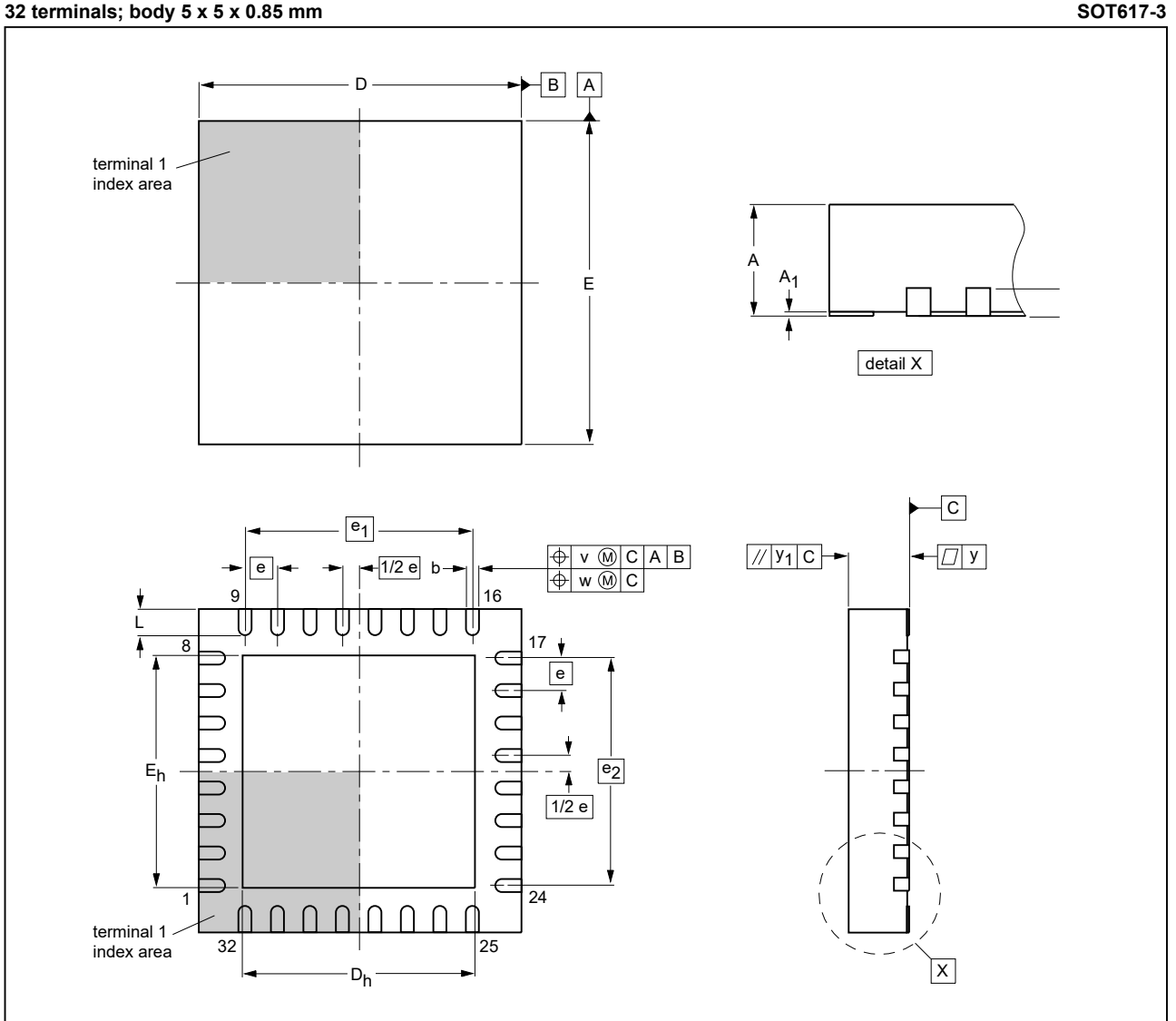
15.2 Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Figure 32. Package outline SOT617-3 (HVQFN32)

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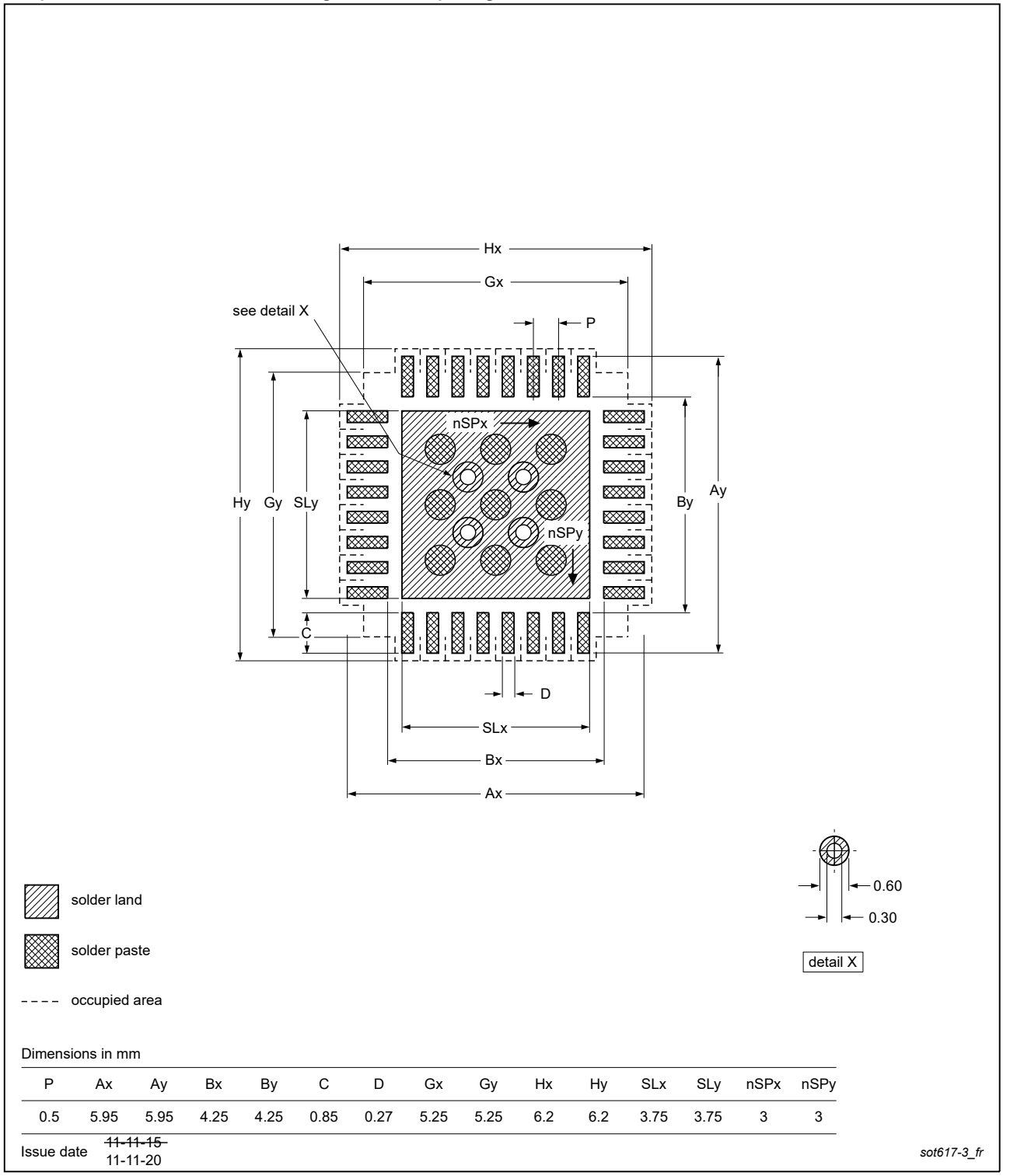
15.3 Soldering

Footprint information for reflow soldering of HVQFN32 package **SOT617-3**



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

sot617-3_fr

Figure 33. Reflow soldering footprint for HVQFN32 (SOT617-3)

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16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 34) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

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- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 70 and Table 71

Table 70. SnPb eutectic process (from J-STD-020D)

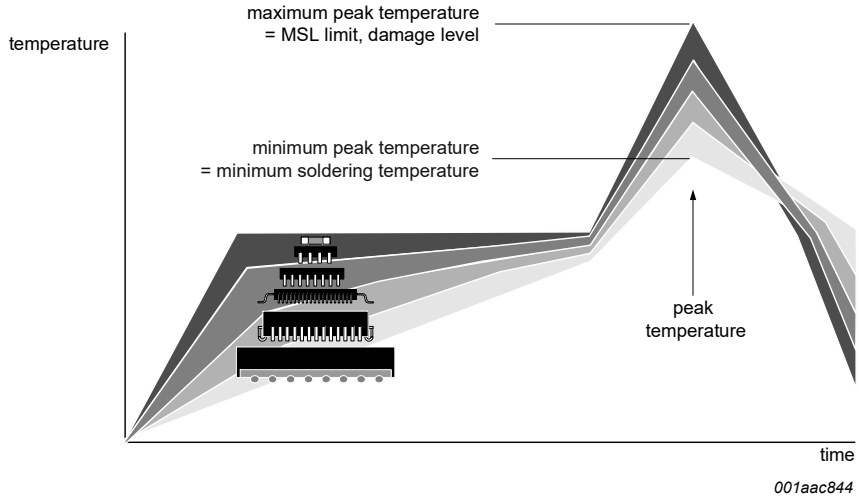
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 71. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.



MSL: Moisture Sensitivity Level

Figure 34. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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17 Abbreviations

Table 72. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MISO	Master In, Slave Out
MOSI	Master Out, Slave In
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SPI	Serial Peripheral Interface

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18 Revision history

Table 73. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCAL9722 v.1.1	20230501	Product data sheet	-	PCAL9722 v.1.0
Modifications:	• Table 2: Updated orderable part number and packing method information			
PCAL9722 v.1.0	20221208	Product data sheet	-	-

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19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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