



# NMH1000

## Magnetic switch

Rev. 2 — 5 April 2023

Product data sheet

## 1 General description

The NMH1000 is a hall effect magnetic field switch. The switch is most sensitive to a vertical field passing through the top-to-bottom surfaces, orthogonal to the plane of the application printed circuit board. The switch operates at low voltage, low current, low output data rate, and is a small physical size.

Processing of input consists of functional blocks such as a configurable state machine, analog-to-voltage conversion of the input, and comparison to generate the bi-state output, arranged in linear succession.

## 2 Features and benefits

- Threshold selection 3-state hardware pin.
- Threshold selection data bit(s) in an I<sup>2</sup>C accessible register.
- Sample rate selection 3-state hardware pin.
- Sample rate selection data bit(s) in an I<sup>2</sup>C accessible register.
- Mode selection hardware pin to select between standalone or I<sup>2</sup>C serial interface.
- Mode selection data bit(s) in an I<sup>2</sup>C accessible register.
- Two types of output indicate the absence of a magnetic field as compared to an internally set threshold:
  - Binary state hardware pin.
  - Binary state data bit(s), configurable as assert-high or assert-low, in an I<sup>2</sup>C accessible register.

## 3 Applications

- **Electronic system wake-up:** Detecting the proximity vs. lack of proximity to an included magnet when the electronics are removed from its delivery packaging, to wake up the electronics.
- **Laptop lid open / closed:** Detecting the proximity vs. lack of proximity to a magnet mounted to laptop lid, to trigger a status change, for example turn on / off the display.
- **Door or window open / closed:** Detecting the proximity vs. lack of proximity to a magnet mounted to a door, lid, or window, to trigger a status change, for example an alarm.



## 4 Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
NMH1000	VSON	Very thin small outline package, no leads, 6 terminals, 0.5 mm pitch, 1.4 mm x 1.4 mm x 0.85 mm body	SOT2078-1

Refer to AN1902<sup>[1]</sup> for additional information regarding use-case design and manufacturing recommendations.

## 5 Block diagram

The device consists of a monolithic die holding a Hall effect transducer, conversion, and comparison chain. Supporting blocks are described in [Section 5.1](#).

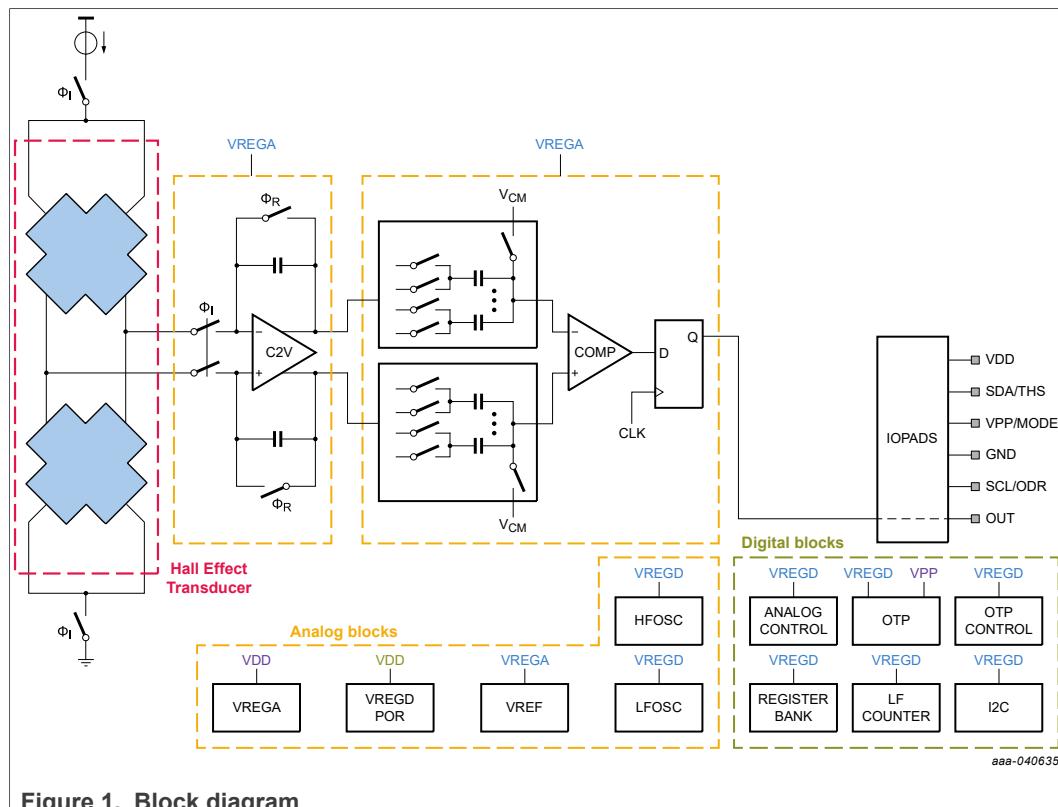


Figure 1. Block diagram

## 5.1 Block descriptions

- **Hall effect:** A transducer which generates a small charge which is proportional to the proximal magnetic flux density.
- **VREGA block:**
  - **C2V:** Converts the Hall effect charge to a voltage, which is stored onto the capacitor across the amplifier.
  - **Comparator:** Compares the voltage generated by the C2V with the pre-defined threshold voltage, then determines the state of the output Q, either Asserted or Cleared.
- **Analog blocks:**
  - **HF and LF Oscillator:** Configurable frequency ( $f_{HFO}$  and  $f_{LFO}$ ) RC-Relaxation oscillators with independent trim bits for trimming.
  - **Regulators and references:** Regulators to step down the external supply for analog and digital circuits. Bandgap reference and current reference for biasing all analog module.
- **Digital blocks:**
  - **Analog control block:** Control signal generation for regulators and references, C2V, oscillators, comparator, for example, based on different operational modes.
  - **OTP:** A 16 x 8 bit array, it requires external  $V_{PPTM}$  for programming.
  - **OTP controller block:** Provides read and write control for OTP. All control signals needed by OTP are generated by this module.
  - **Register bank:** Provides the registers where users can write configurations or read status values.
  - **LF counter:** Counts the specific time depending on the sample rate (ODR) set by the user.
  - **I<sup>2</sup>C and test register block:** Includes the address decode logic and interrupt functions.

## 6 Pinning information

### 6.1 Pinning

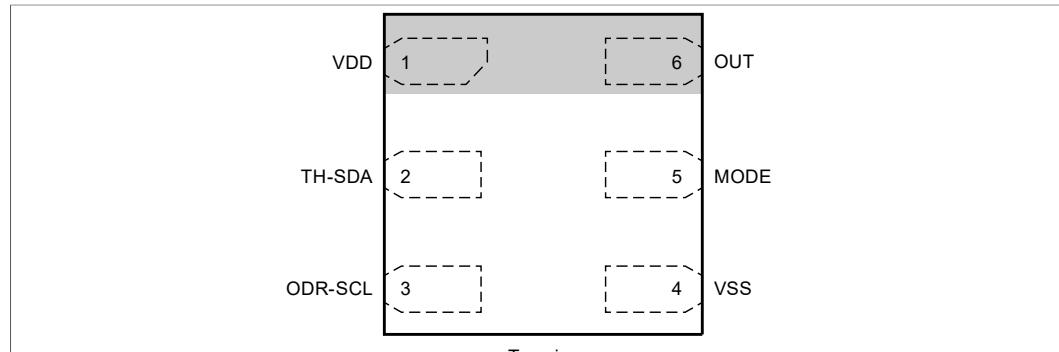


Figure 2. Pin configuration

**Note:** Gray area denotes the end of the device where pin 1 is located.

## 6.2 Pin description

Package and pin assignments support the options of magnetic field threshold and sample rate selections, based on the voltage applied to the MODE pin, upon appropriate voltage applied to the  $V_{DD}$  pin, relative to the  $V_{SS}$  pin.

Table 2. Pin description

Symbol	Pin	Type	Description
$V_{DD}$	1	Supply	Main supply voltage
TH-SDA <sup>[1]</sup>	2	I/O	Standalone mode: Threshold $I^2C$ user mode: $I^2C$ serial data
ODR-SCL <sup>[2]</sup>	3	I	Standalone mode: Sample rate $I^2C$ user mode: $I^2C$ serial clock
$V_{SS}$	4	Ground	Main ground
MODE <sup>[3]</sup>	5	I	Selects between Standalone or $I^2C$ modes.
OUT <sup>[4]</sup>	6	O	Standalone mode: Output indicating absence of field

[1] Three states: low state for medium threshold  $B_O$ -M, open circuit for low threshold  $B_O$ -L, or high state for high threshold  $B_O$ -H, relative to  $V_{SS}$

[2] Three states: low state for medium sample rate  $f_{ODR}$ -M, open circuit for low sample rate  $f_{ODR}$ -L, or high state for high sample rate  $f_{ODR}$ -H, relative to  $V_{SS}$

[3] Two states: low state for standalone, high state for  $I^2C$  User Mode, relative to  $V_{SS}$

[4] Two states: default assert for magnet not present, clear for magnet present, relative to  $V_{SS}$

## 6.3 Orientation

The device adheres to the convention of north magnetic field represented by positive/North polarity, orthogonal to the plane of the package body top surface and the arrows depict increasing strengths.



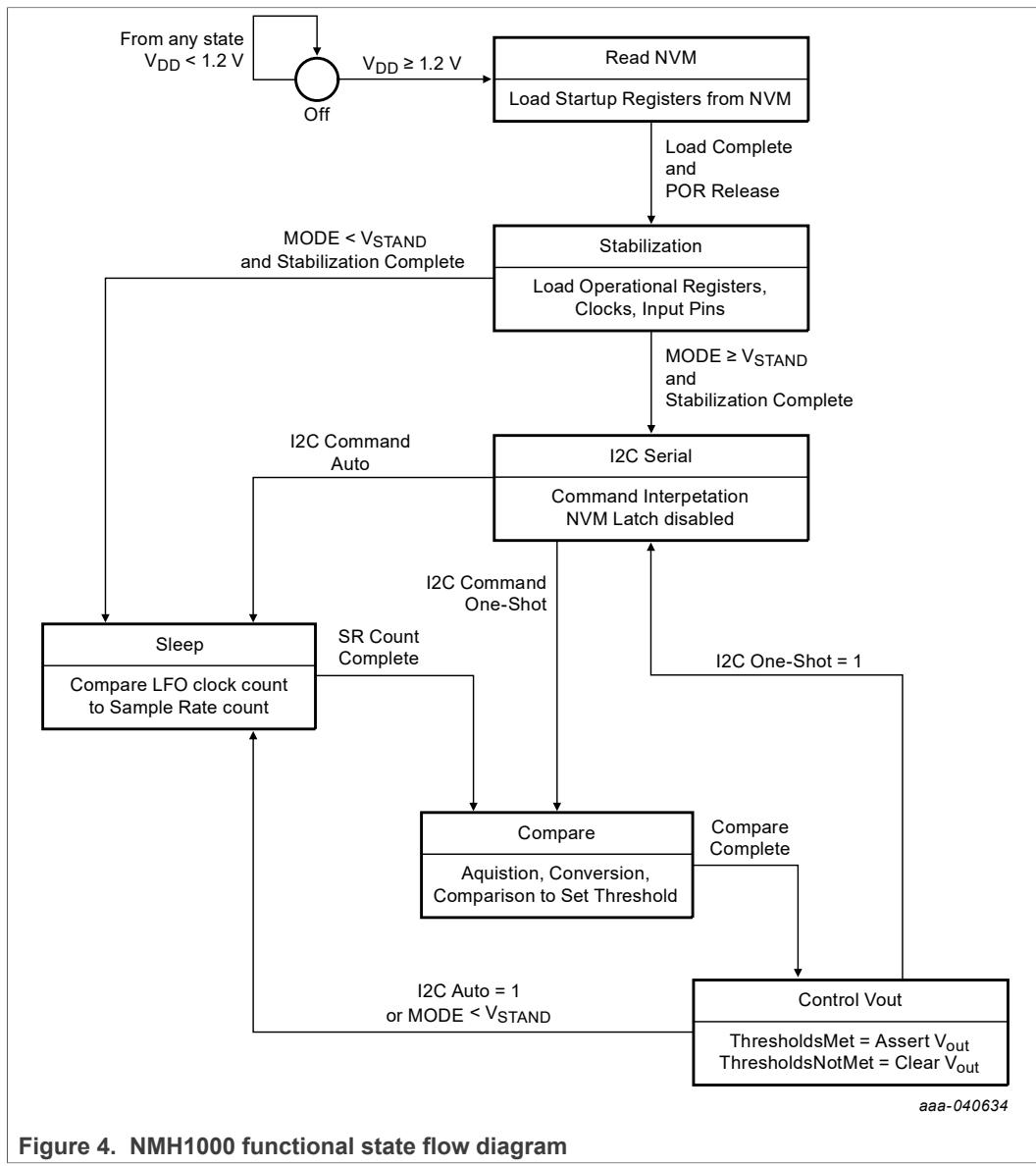
Figure 3. Magnetic field vs. package orientation

## 7 Functional description

### 7.1 Operating modes

#### 7.1.1 Functional states

Figure 4 illustrates the functional states that the device transitions between.



#### 7.1.2 Interface Operational Modes

The NMH1000 operates under one of two modes when appropriately configured as described in the following sections:

- I<sup>2</sup>C user mode.
- Standalone mode.

Entry into each of the two user modes is initiated by the voltage existing at the MODE pin at the time of the V<sub>DD</sub> pin rising above V<sub>DDMIN</sub>, and followed by a read of NVM Start-up register(s), both relative to the V<sub>SS</sub> pin:

- MODE < V<sub>STAND</sub> results in the device entering standalone mode and forcing OPMODE to 0.
- MODE ≥ V<sub>STAND</sub> results in the device entering I<sup>2</sup>C user mode and forcing OPMODE to 1.

Transition from I<sup>2</sup>C user mode to standalone mode is initiated by the host writing I2C\_DIS to 1, which results in OPMODE being forced to 0.

**Note:** The device reloads the NVM into operating registers after t<sub>RLDS</sub> seconds from final power application, needing a duration of t<sub>RLDC</sub>.

## 7.2 Threshold configurations

### 7.2.1 Fixed thresholds

In standalone mode, fixed thresholds with fixed hysteresis are selected by voltage applied to V<sub>TH</sub> pin relative to V<sub>SS</sub> pin.

#### 7.2.1.1 Fixed threshold selection via V<sub>TH</sub> pin voltage

Table 3. Fixed threshold selection

V <sub>TH</sub>	Threshold <sup>[1]</sup>
V <sub>TH</sub> < V <sub>BO-L</sub>	Medium magnetic field
V <sub>BO-L</sub> ≤ V <sub>TH</sub> ≤ V <sub>BO-H</sub>	Low magnetic field
V <sub>TH</sub> > V <sub>BO-H</sub>	High magnetic field

[1] See [Table 27](#).

### 7.2.2 User-defined threshold

In I<sup>2</sup>C mode, user-defined output assert threshold without hysteresis is selected by write to register bits, in units of B<sub>Δ</sub> in G/LSB:

Table 4. User-defined assert thresholds

USER_ASSERT_THRESH[7:3]	Assert Threshold <sup>[1]</sup> - B <sub>OA</sub>
0 0 0 0 0	0 G
0 0 0 0 1	Lowest in-range magnetic field to assert the output
1 1 1 1 1	Highest in-range magnetic field to assert the output

[1] See to [Section 10.6 "I<sup>2</sup>C user mode, output assertion"](#)

In I<sup>2</sup>C mode, user-defined output clear threshold without hysteresis is selected by write to register bits, in units of B<sub>Δ</sub> in G/LSB:

Table 5. User-defined output clear thresholds

USER_CLEAR_THRESH[7:3]	Clear Threshold <sup>[1]</sup> - B <sub>Oc</sub>
0 0 0 0 0	0 G
0 0 0 0 1	Lowest in-range magnetic field to clear the output

**Table 5. User-defined output clear thresholds...continued**

USER_CLEAR_THRESH[7:3]	Clear Threshold <sup>[1]</sup> - $B_{oc}$
1 1 1 1 1	Highest in-range magnetic field to clear the output

[1] See to [Section 10.7 "I<sup>2</sup>C user mode, output clear"](#)

**Note:** If the USER\_ASSERT\_THRESH and USER\_CLEAR\_THRESH are set too close in value to each other, the intended hysteresis may cause the output to change states at unintended magnetic field strengths, or may cause the output to not change states at intended magnetic field strengths.

Be aware of the minimum hysteresis noted in [Table 32](#).

## 7.3 Sample rate configurations

### 7.3.1 Fixed sample rates

In standalone mode, the sample rate is the selected voltage applied to V<sub>ODR</sub> pin relative to V<sub>SS</sub> pin.

#### 7.3.1.1 Sample rate selection via V<sub>ODR</sub> pin voltage

**Table 6. Sample rate selection**

V <sub>ODR</sub>	Sample Rate <sup>[1]</sup>
$V_{ODR} < V_{fODR-L}$	$f_{ODR-M}$
$V_{fODR-L} \leq V_{ODR} \leq V_{fODR-H}$	$f_{ODR-L}$
$V_{ODR} > V_{fODR-H}$	$f_{ODR-H}$

[1] See [Section 10.2 "Clocks and rates"](#).

### 7.3.2 User-defined sample rate

In I<sup>2</sup>C mode, the user-defined sample rate is selected by a write to register bits:

**Table 7. I<sup>2</sup>C mode user-defined sample rate**

USER_ODR[2:0]	Sample Rate
0 0 0	$f_{ODR-L}$
0 0 1	$5 \times f_{ODR-L}$
0 1 0	$f_{ODR-M}$
0 1 1	$5 \times f_{ODR-M}$
1 0 0	$f_{ODR-H}$
1 0 1	$5 \times f_{ODR-H}$
1 1 0	$10 \times f_{ODR-H}$
1 1 1	config. error

## 7.4 Output control function description

### 7.4.1 Output hysteresis

Hysteresis is implemented as the magnetic field difference between the output being cleared versus the output being asserted.

- In Standalone mode, the hysteresis is a fixed difference.
- In I<sup>2</sup>C mode with the selection of one of the three fixed thresholds, the hysteresis is a fixed difference, equal to the Standalone mode hysteresis.
- In I<sup>2</sup>C mode with customer selected thresholds, the hysteresis is the result of the customer choices of output Clear threshold versus output Assert threshold.

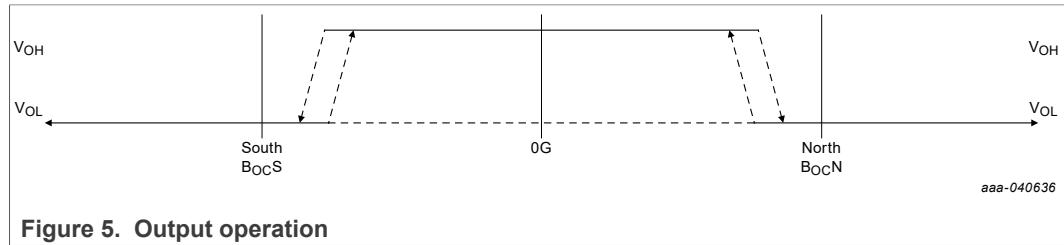


Figure 5. Output operation

### 7.4.2 Control Output State

#### 7.4.2.1 Standalone mode output assert / clear states

In Standalone mode, the OUT pin asserts to high state upon the completion of the comparison stage, and the magnetic field is lower than the selected threshold Low, Medium, or High, minus the hysteresis.

In Standalone mode, the OUT pin is cleared to low state upon completion of the comparison stage, and the magnetic field is higher than the selected threshold Low, Medium, or High.

#### 7.4.2.2 User-defined output assert / clear states

In I<sup>2</sup>C mode, the OUT pin and OUT-B register bit asserted and cleared states are selectable via the V\_POL register bit.

Table 8. User-defined output assert and clear states

V_POL	OUT pin assert / clear state
0	OUT pin Assert = high / OUT pin Clear = low
1	OUT pin Assert = low / OUT pin Clear = high

## 7.5 I<sup>2</sup>C serial data function description

### 7.5.1 I<sup>2</sup>C pin functions

Two signals support the I<sup>2</sup>C-bus:

- Serial Clock Line - SCL.
- Serial Data line - SDA.

SCL is input and used for clocking the data into or out from the SDA data line.

SDA is bidirectional and used for sending and receiving the data.

When the bus is free, both the lines idle high.

The I<sup>2</sup>C interface is compliant to the standard mode (100 kHz).

SDA and SCL both expect external pull-up resistors connected to V<sub>DD</sub>.

- 1 kΩ minimum, board capacitance 20 pF maximum.

### 7.5.2 I<sup>2</sup>C timing diagram

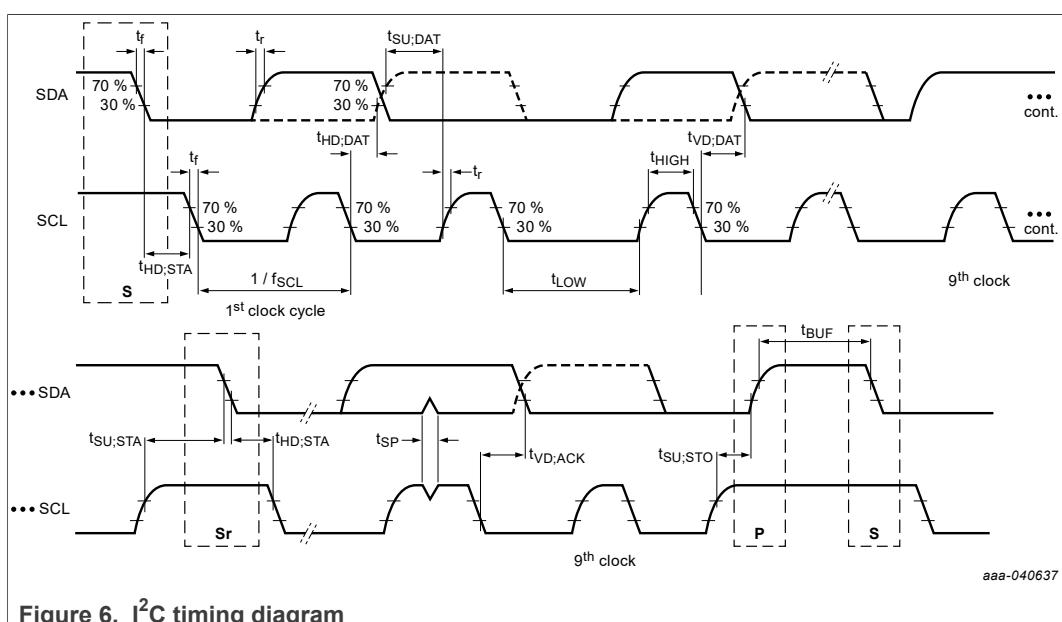


Figure 6. I<sup>2</sup>C timing diagram

### 7.5.3 I<sup>2</sup>C operation

The I<sup>2</sup>C transaction on the bus is initiated through a start condition (START) signal. START signal is defined as a HIGH to LOW transition on the SDA line while the SCL line is held HIGH. After START is transmitted by the host, the bus is considered busy. The next byte of data transmitted after START contains the device address in the first seven bits, and the eighth bit indicates whether the host is receiving data from the device or transmitting data to the device. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the host. The ninth clock pulse, following the device address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low for it to remain stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited because the internal addressing wraps after \$6D to \$00, continuing to \$6D again, then to \$00, and so forth. The wrapping applies to both write transfers and read transfers. Note that usable addresses stop at \$09, therefore a host may expect random values between \$0A to \$6D. If the host is unable to receive another complete byte of data until it has performed some other function, the host can hold the SCL line low, forcing the transmitter into a wait state. Data transfer continues only when the host is ready for another byte and releases the clock line.

A stop condition (STOP) is defined as a low to high transition on the SDA line while the SCL line is high. Data transfer is terminated by a STOP.

A host may also issue a RESTART during a data transfer. The device expects RESTARTs to randomly read from specific registers.

The bus logic of the device resets on receipt of a START, or RESTART condition. The device anticipates the sending of a device address, even if these START conditions are not positioned or follow proper format.

The device accepts the first bit of an address after each START, or RESTART condition.

The device detects when the SDA line is held low, and in such cases, releases the SDA line when the host issue no more than nine cycles of the SCL line.

The device determines the value in the NVM I<sup>2</sup>C address register. If the value is not \$00 and not \$FF, the device uses this address during I<sup>2</sup>C transactions. If the address register is either \$00 or \$FF, the address defaults to \$xx.

#### 7.5.4 I<sup>2</sup>C protocol diagram

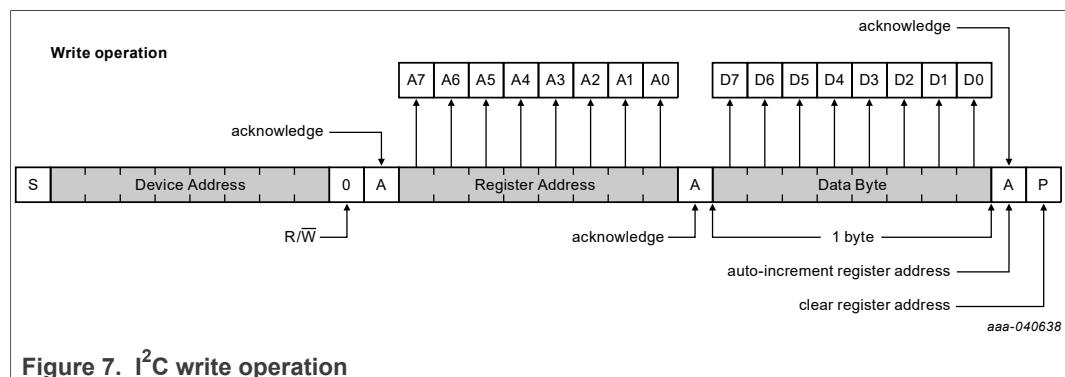


Figure 7. I<sup>2</sup>C write operation

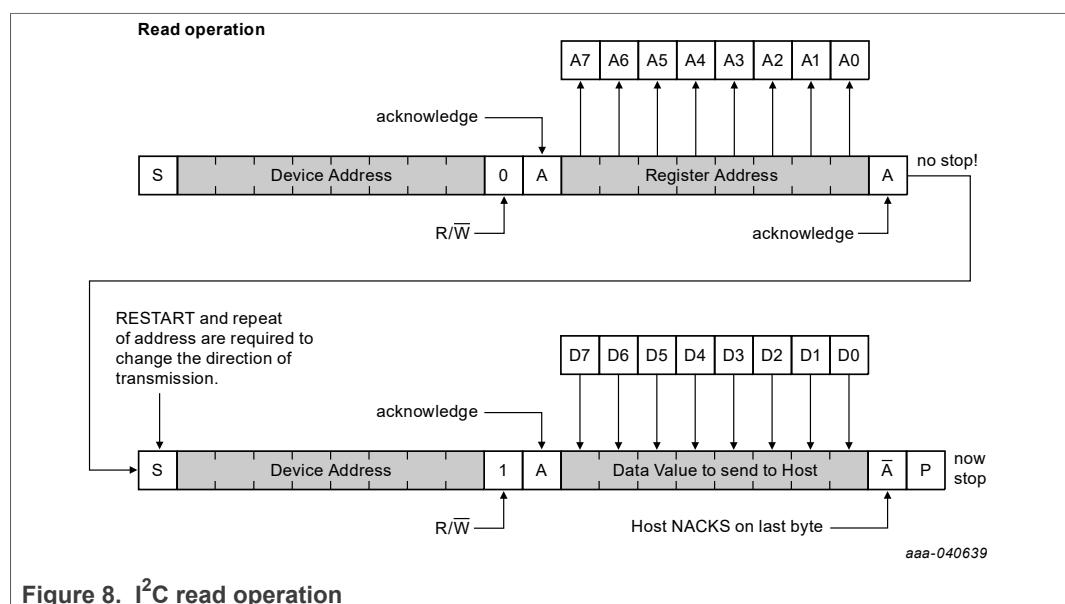


Figure 8. I<sup>2</sup>C read operation

## 7.6 Register map

### 7.6.1 Register overview

Table 9. Register map overview

Address	Name	Description	AO or S <sup>[1]</sup>	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00	<a href="#">STATUS</a>	Status reporting of modes and selections	S	OUTPUT	MDO	MDR	—	OPMODE	—	RST_STAT	OUT_B
\$01	<a href="#">CONTROL_REG1</a>	Control of Operations	S	—	—	V_POL	I2C_DIS	AUTO	ONE_SHOT	—	RST
\$02	—	Reserved	—	—	—	—	—	—	—	—	—
\$03	<a href="#">OUT_M_REG</a>	Report of Magnetic Strength	S	MAG_DATA [7:2]						—	—
\$04	<a href="#">USER_ASSERT_THRESH</a>	User selectable output Assert threshold, N or S	AO	USER_ASSERT_THRESH [7:3]					Reserved		
\$05	<a href="#">USER_CLEAR_THRESH</a>	User selectable output Clear threshold, N or S	AO	USER_CLEAR_THRESH [7:3]					Reserved		
\$06	<a href="#">USER_ODR</a>	User selectable sleep sample output data rates	AO	—	—	—	—	—	USER_ODR[2:0]		
\$07	—	Reserved	—	—	—	—	—	—	—	—	—
\$08	<a href="#">WHO_AM_I</a>	I <sup>2</sup> C Configured Identifier	S	WHO_AM_I [7:0]							
\$09	<a href="#">I2C_ADDR</a>	I <sup>2</sup> C Configured Address - default after reset = \$60	S	—	ADDR [6:0]						

[1] AO - Always On, S - Switched

### 7.6.2 Register details

#### 7.6.2.1 Status reporting of modes and selections (STATUS) (\$00h)

Table 10. STATUS – Status reporting of modes and selections (address \$00h) bit allocation

Bit	7	6	5	4	3	2	1	0
<b>Symbol</b>	OUTPUT	MDO	MDR	—	OPMODE	—	RST_STAT	OUT_B
<b>Reset</b>	0	1	1	—	1	—	1	x
<b>Access</b>	R/W	R/W	R/W	—	R/W	—	R/W	R/W

Table 11. STATUS – Status reporting of modes and selections (address \$00h) bit descriptions

Bit	Symbol	Access	Value	Description
7	OUTPUT	R/W		V <sub>out</sub> control block state. This bit follows the state of the OUT pin in either case of V_POL = 0 or 1.
			0	The state of VOUT is driven to low; Result of Reset.
			1	The state of VOUT is driven to high.
6	MDO	R/W		Magnetic data overwrite indicates the validity of the value in register \$03. After asserting to 1, the MDO bit retains this value after the register \$03 returns to the range of \$00 to \$1F, until a read operation is performed on register \$00. The MDO reasserts if the register \$03 is again > \$1F.
			0	Register \$03 value is within the range \$00 to \$1F.
			1	Register \$03 value is >\$1F indicates out-of-range or fault; Result of reset.

Table 11. STATUS – Status reporting of modes and selections (address \$00h) bit descriptions...continued

Bit	Symbol	Access	Value	Description
5	MDR	R/W		Magnetic data ready indicates the value in register \$03 is available for read operation. After asserting to 1, the MDR bit retains this value after the register \$03 becomes available, until a read operation is performed on register \$00. The MDR reasserts if the register \$03 is again not available.
			0	\$03 data available.
			1	\$03 data not available; Result of reset.
3	OPMODE	R/W		The read-only OPMODE indicates the mode of the internal state-machine.
			0	Indicates $V_{PP} < V_{STAND}$ and the device in standalone mode indicating a state machine fault, since the registers are only accessible in the $I^2C$ mode.
			1	Indicates $V_{PP} \geq V_{STAND}$ and the device in $I^2C$ user mode.
1	RST_STAT	R/W		Reset status indicates the state-machine reset sequence. RST_STAT set to 1 as the device enters POR or soft reset. This bit is cleared to 0 upon reading the register \$00. After asserting to 1, the RST_STAT bit retains this value after the exit of POR or soft rest, until a read operation is performed on register \$00. The RST_STAT reasserts if POR or soft reset is entered.
			0	Reset sequence complete and read operation performed on register \$00.
			1	Reset sequence not complete; Result of reset.
0	OUT_B	R/W		Output buffer indicates a latched state of the OUT pin after a transition from either Asserted to Clear or Clear to Asserted. After asserting to 1, or clearing to 0, the OUT_B bit retains this value until a read operation is performed on register \$00. This bit is intended to allow the user or tester to check for a transition while the actual OUT pin or OUTPUT bit may have changed state again between checks.
			0	OUT cleared on previous cycle.
			1	OUT asserted on previous cycle.

### 7.6.2.2 Control of operations (CONTROL\_Reg1) (\$01h)

Table 12. CONTROL\_Reg1 – Control of operations(address \$01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	V_POL	I2C_DIS	AUTO	ONE_SHOT	—	RST
Reset	—	—	0	0	0	0	—	0
Access	—	—	R/W	R/W	R/W	R/W	—	R/W

Table 13. CONTROL\_Reg1 – Control of operations (address \$01h) bit description

Bit	Symbol	Access	Value	Description
5	V_POL	R/W		V_POL provides control of the user-defined OUT pin and resultant OUT_B register bit assert / clear polarity.
			0	Assert = out pin high, Clear = out pin low; Result of reset.
			1	Assert = out pin low, Clear = out pn high.

Table 13. CONTROL\_Reg1 – Control of operations (address \$01h) bit description...continued

Bit	Symbol	Access	Value	Description
4	I2C_DIS	R/W		I2C_DIS provides control of the operating mode "on-the-fly" after the device exits POR or Soft Reset. I2C_DIS allows the user to force the device into standalone mode from the I <sup>2</sup> C mode. <b>Note:</b> Writing 1 to I2C_DIS is a one-time-only operation. Bringing the device into I <sup>2</sup> C mode from standalone requires a full power cycle and release of POR. <b>Note:</b> MAG_DATA retains its last value, and is updated upon next write to ONE_SHOT.
			0	Write to 0 has no effect; Read of 0 indicates I <sup>2</sup> C mode; Result of reset.
			1	Write to 1 forces the device from I <sup>2</sup> C mode to standalone mode; Read of 1 indicates a state machine fault, since the registers are only accessible in the I <sup>2</sup> C mode.
3	AUTO	R/W		AUTO provides control of the state machine to enter a sequential autonomous mode cycling from sleep to compare to Vout control, then back to sleep, for example. The sequence is halted when the AUTO is written to 0.
			0	Write to 0 halts or prevents autonomous mode; Read of 0 indicates that autonomous mode is not active; Result of reset.
			1	Write to 1 starts the autonomous mode; Read of 1 indicates that autonomous mode is active.
2	ONE_SHOT	R/W		ONE_SHOT provides control of the state machine to trigger a single sequence of compare to Vout control, then halt. The bit clears upon the sequence being completed.
			0	Write to 0 has no effect; Read of 0 indicates One-Shot is not active; Result of reset.
			1	Write to 1 triggers a one-shot sequence; Read of 1 has no effect.
				<b>Note:</b> The BUSY bit indicates that the sequence is underway or not completed. <b>Note:</b> MAG_DATA retains its last value, and is updated upon next write to ONE_SHOT.
0	RST	R/W		RST provides I <sup>2</sup> C access to force an internal device soft reset:
			0	No reset is forced.
			1	Internal device reset is forced.

### 7.6.2.3 Magnetic strength report (OUT\_M\_REG) (\$03h)

Table 14. OUT\_M\_REG – Magnetic strength report (address \$03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MAG_DATA [7:2]							reserved
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Table 15. OUT\_M\_REG – Magnetic strength report (address \$03h) bit description

Bit	Symbol	Access	Value	Description
7 to 2	MAG_DATA	R/W		MAG_DATA[7:2] indicates a relative magnetic field strength in units of $B\Delta$ in G/LSB.
			\$00	0 G; Result of reset.
			\$01	Lowest in-range magnetic field strength.
			\$1F	Highest in-range magnetic field strength.

#### 7.6.2.4 User selectable output, assert threshold, N or S (USER\_ASSERT\_THRESH) (\$04h)

Table 16. USER\_ASSERT\_THRESH – User selectable output, assert threshold, N or S (address \$04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USER_ASSERT_THRESH [7:3]						Reserved	
Reset	0	0	0	0	0	—	—	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 17. USER\_ASSERT\_THRESH – User selectable output, assert threshold, N or S (address \$04h) bit description

Bit	Symbol	Access	Value	Description
7 to 3	USER_ASSERT_THRESH	R/W		In I <sup>2</sup> C mode, USER_ASSERT_THRESH[7:3] provides the capability for the user to override the fixed threshold controlling the output assert condition, in units of $B\Delta$ in G/LSB.
				<i>Note: Hysteresis is controlled by appropriate user settings for both USER_ASSERT_THRESH and USER_CLEAR_THRESH registers.</i>
			\$00	0 G; Result of reset.
			\$01	Lowest in-range magnetic field to assert the output.
			\$1F	Highest in-range magnetic field to assert the output.

#### 7.6.2.5 User selectable output, clear threshold, N or S (USER\_CLEAR\_THRESH) (\$05h)

Table 18. USER\_CLEAR\_THRESH – User selectable output, clear threshold, N or S (address \$05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USER_CLEAR_THRESH [7:3]						Reserved	
Reset	0	0	0	0	0	—	—	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19. USER\_CLEAR\_THRESH – User selectable output, clear threshold, N or S (address \$05h) bit description

Bit	Symbol	Access	Value	Description
7 to 3	USER_CLEAR_THRESH	R/W		In I <sup>2</sup> C mode, USER_CLEAR_THRESH[7:3] provides the capability for the user to override the fixed threshold controlling the output clear condition, in units of BΔ in G/LSB. <i>Note: Hysteresis is controlled by appropriate user settings for both USER_ASSERT_THRESH and USER_CLEAR_THRESH registers.</i>
			\$00	0 G; Result of reset.
			\$01	Lowest in-range magnetic field to clear the output.
			\$1F	Highest in-range magnetic field to clear the output.

#### 7.6.2.6 User selectable sleep sample output data rates (USER\_ODR) (\$06h)

Table 20. USER\_ODR – User selectable sleep sample output data rates (address \$06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	—	—	—	USER_ODR[2:0]		
Reset	—	—	—	—	—	0	0	0
Access	—	—	—	—	—	R/W	R/W	R/W

Table 21. USER\_ODR – User selectable sleep sample output data rates (address \$06h) bit description

Bit	Symbol	Access	Value	Description
2 to 0	USER_ODR	R/W		In I <sup>2</sup> C mode, USER_ODR[2:0] provides the capability for the user to override the fixed sample rate controlling the sleep-compare-Vout cycle time.
			0 0 0	Low sample rate selected.
			0 0 1	5 x Low sample rate selected.
			0 1 0	Medium sample rate selected.
			0 1 1	5 x Medium sample rate selected.
			1 0 0	High sample rate selected.
			1 0 1	5 x High sample rate selected.
			1 1 0	10 x High sample rate selected.
			1 1 1	Configuration error.

#### 7.6.2.7 I<sup>2</sup>C configured identifier (WHO\_AM\_I) (\$08h)

Table 22. WHO\_AM\_I - I<sup>2</sup>C configured identifier (address \$08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WHO_AM_I [7:0]							
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. WHO\_AM\_I - I<sup>2</sup>C configured identifier (address \$08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	WHO_AM_I	R/W		WHO_AM_I[7:0] provides the device identification register. The value is programmed in the NVM at final test. Each variation has its own unique device ID.
			\$00	WHO_AM_I error condition.
			\$01	Generic open market default value.
			\$02 to \$FE	Customer defined unique values.
			\$FF	WHO_AM_I not programmed.

#### 7.6.2.8 I<sup>2</sup>C configured identifier (I2C\_ADDR) (\$09h)

Table 24. I2C\_ADDR - I<sup>2</sup>C configured identifier (address \$09h) bit allocation

Bit	7	6	5	4	3	2	1	0	
Symbol	RD/WR	I2C_ADDR [6:0]							
Reset	—	1	1	0	0	0	0	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Table 25. I2C\_ADDR - I<sup>2</sup>C configured identifier (address \$09h) bit description

Bit	Symbol	Access	Value	Description
7	RD/WR	R/W	—	Bit 7 identifies a Read or Write operation.
6 to 0	I2C_ADDR	R/W		I2C_ADDR[6:0] is register mapped and loaded by default value \$60 from OTP at boot time. After that, users may write any non-zero value to it. This non-zero value is used until the device is reset. If the device is reset, the same default value of \$60 is reloaded and used again.
				\$60 = default loaded at exit of reset.
				\$00 = lowest address value.
				\$7F = highest address value.

## 8 Limiting values

Table 26. Limiting values

Symbol	Description	Condition	Min	Typ	Max	Unit
B <sub>G</sub>	Magnetic field	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	—	—	Not limited	G (Gauss)
V <sub>SUP</sub>	V <sub>DD</sub> to V <sub>SS</sub> range	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	-0.3	—	3.6	V
V <sub>IO</sub>	IO pin voltage, each pin vs V <sub>DD</sub> / V <sub>SS</sub>	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max	V <sub>SS</sub> - 0.3	—	V <sub>SUP</sub> + 0.3	V
I <sub>IO</sub>	IO pin current, each pin vs V <sub>DD</sub> / V <sub>SS</sub>	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	-10	—	10	mA

Table 26. Limiting values...continued

Symbol	Description	Condition	Min	Typ	Max	Unit
$I_{SUBIO}$	Substrate current injection, all IO pins, current from pin to $V_{SS} - 0.3$ V	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	—	100	—	mA
$I_{LATCH}$	Latch-up current, current to/from pin to $V_{DD}/V_{DDA} + 0.3$ V	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	-100	—	100	mA
$ESD_{HBM}$	Electrostatic discharge, Human Body Model (HBM) all pins	$T_A = 25$ °C, $V_{DD} = 1.5$ V	-2000	—	2000	V
$ESD_{CDM}$	Electrostatic discharge, Charged Device Model (CDM) all pins	$T_A = 25$ °C, $V_{DD} = 1.5$ V	-500	—	500	V
$EOS_{EMIR}$	Conducted immunity DPI, until OUT unintentionally changes state or $I^2C$ corruption	$T_A = 25$ °C, $V_{DD} = 1.5$ V	—	30	—	dBm
$T_{STG}$	Unpowered storage temperature range	—	-40	—	150	°C

## 9 Recommended operating conditions

Table 27. Operating conditions

Symbol	Description	Condition	Min	Typ	Max	Unit
<b>Transitions</b>						
$t_{OP}$	Power-on initialization	From $V_{DD} > 1.2$ V to Operation Ready; 25 °C and 1.5 V.	—	4.8	5.1	ms
$t_{BOC-A}$	Cleared state to Asserted state phase delay	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	—	100	—	μs
<b>Voltages</b>						
$V_{DD}$	Operating voltage range where Min = $V_{DD}$ Min, Typ = 1.5 V, Max = $V_{DD}$ Max	$T_A$ Min $\leq T_A \leq T_A$ Max	1.2	1.5	$V_{SUP}$	V
$V_{STAND}$	MODE pin voltage - Standalone mode	$T_A = 25$ °C, $V_{DD} = 1.5$ V	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V
$V_{STAND}$	Mode pin voltage - $I^2C$ mode	$T_A = 25$ °C, $V_{DD} = 1.5$ V	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V
$V_{TH}$	TH-SDA pin - Standalone mode, Low threshold	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	$0.4 \times V_{DD}$	$0.5 \times V_{DD}$	$0.6 \times V_{DD}$	V
$V_{TH}$	TH-SDA pin - Standalone mode, Medium threshold	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	—	—	$0.3 \times V_{DD}$	V
$V_{TH}$	TH-SDA pin - Standalone mode, High threshold	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	$0.7 \times V_{DD}$	—	—	V
$V_{ODR}$	ODR-SCL pin - Standalone mode, Low sample rate	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	$0.4 \times V_{DD}$	$0.5 \times V_{DD}$	$0.6 \times V_{DD}$	V
$V_{ODR}$	ODR-SCL pin - Standalone mode, Medium sample rate	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	—	—	$0.3 \times V_{DD}$	V
$V_{ODR}$	ODR-SCL pin - Standalone mode, High sample rate	$T_A$ Min $\leq T_A \leq T_A$ Max, $V_{DD}$ Min $\leq V_{DD} \leq V_{DD}$ Max	$0.7 \times V_{DD}$	—	—	V

Table 27. Operating conditions...continued

Symbol	Description	Condition	Min	Typ	Max	Unit
<b>Temperatures</b>						
T <sub>A</sub>	Operating temperature range where Min = T <sub>A</sub> Min, Typ = 25 °C, Max = T <sub>A</sub> Max	V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	-40 °C	25	+85	°C

## 10 Characteristics

### 10.1 Supply currents

Table 28. Supply currents

Symbol	Description	Condition	Min	Typ	Max	Unit
I <sub>DDS-LODR</sub>	Supply current, Low ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the Low ODR stand-alone mode.	—	47.5	187	nA
I <sub>DDS-MODR</sub>	Supply current, Medium ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the Medium ODR stand-alone mode	—	72.2	234	nA
I <sub>DDS-HODR</sub>	Supply current, High ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the High ODR stand-alone mode.	—	319.6	760	nA
I <sub>DDS-S</sub>	Supply current, Sleep mode	Typ = 25 °C, V <sub>DD</sub> = 1.5 V Max = T <sub>A</sub> Min to T <sub>A</sub> Max and V <sub>DD</sub> Min to V <sub>DD</sub> Max	—	42	300	nA
I <sub>DDS-M</sub>	Supply current, measurement	Typ = 25 °C, V <sub>DD</sub> = 1.5 V Max = T <sub>A</sub> Min to T <sub>A</sub> Max and V <sub>DD</sub> Min to V <sub>DD</sub> Max	—	580	650	µA
I <sub>DDS-2</sub>	Supply current, I <sup>2</sup> C command/response	Typ = 25 °C, 1.5 V, Max = T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	—	35	45	µA

### 10.2 Clocks and rates

Table 29. Clocks and rates

Symbol	Description	Condition	Min	Typ	Max	Unit
f <sub>LFO</sub>	Low frequency oscillator	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	2.8	3.2	3.5	kHz
f <sub>HFO</sub>	High frequency oscillator	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	1.7	2	2.3	MHz

Table 29. Clocks and rates...continued

Symbol	Description	Condition	Min	Typ	Max	Unit
$f_{SCL}$	$I^2C$ input clock	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	1	MHz
$f_{ODR-H}$	Sample rate - High	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	10	—	Hz
$f_{ODR-M}$	Sample rate - Medium	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	1	—	Hz
$f_{ODR-L}$	Sample rate - Low	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	0.1	—	Hz

### 10.3 $I^2C$ pin thresholds

Table 30.  $I^2C$  pin thresholds

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{IH}$	Digital high-level input voltage	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max at } I_{IH} \text{ max}$	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V
$V_{IL}$	Digital low-level input voltage	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max at } I_{IL} \text{ Max}$	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V
$V_{OH}$	Digital high-level output voltage	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max at } I_{OH} \text{ Max}$	$V_{DD} - 0.3$	—	—	V
$V_{OL}$	Digital low-level output voltage	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max at } I_{OL} \text{ Max}$	—	—	$V_{SS} + 0.3$	V
$I_{pin}$	Digital pin current	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	—	—	$\pm 10$	mA

### 10.4 Serial data timing characteristics

Table 31. Serial data timing characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
$C_B$	Board capacitive load SDA, SCL	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	1	$\mu\text{F}$
$t_{BUF}$	Bus free time, between stop and start	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.7	—	—	$\mu\text{s}$
$t_{HD}$ to $t_{STA}$	Restart hold, after this period the first clock may be generated	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.0	—	—	$\mu\text{s}$
$t_{SU}$ to $t_{STA}$	Restart setup	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.7	—	—	$\mu\text{s}$
$t_{SU}$ to $t_{STO}$	Stop setup	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.0	—	—	$\mu\text{s}$
$t_{HD}$ to $t_{DAT}$	SDA hold	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	300	—	—	ns
$t_{SU}$ to $t_{DAT}$	SDA setup	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	250	—	—	ns
$t_{LOW}$	SCL low	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.7	—	—	$\mu\text{s}$

Table 31. Serial data timing characteristics...continued

Symbol	Description	Condition	Min	Typ	Max	Unit
$t_{HIGH}$	SCL high	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.0	—	—	$\mu\text{s}$
$t_r$	SDA and SCL rise	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	1000	ns
$t_f$	SDA and SCL fall	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	300	ns

## 10.5 Magnetic field characteristics

Table 32. Magnetic field characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
<b>Transfer Function</b>						
$B\Delta$	Sensitivity	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	—	1.75	—	G/LSB
$B_{off}$	Offset	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	—	0	—	G
$B_{hyst}$	Assert - Clear hysteresis	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	20	—	—	G
$BOC_{x-L}$	OUT pin transition, Low threshold	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	—	—	$\pm 100$	G
$BOC_{x-M}$	OUT pin transition, Medium threshold	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	—	—	$\pm 160$	G
$BOC_{x-H}$	OUT pin transition, High threshold	$T_A = 25^\circ\text{C}, V_{DD} = 1.5 \text{ V}$	—	—	$\pm 230$	G

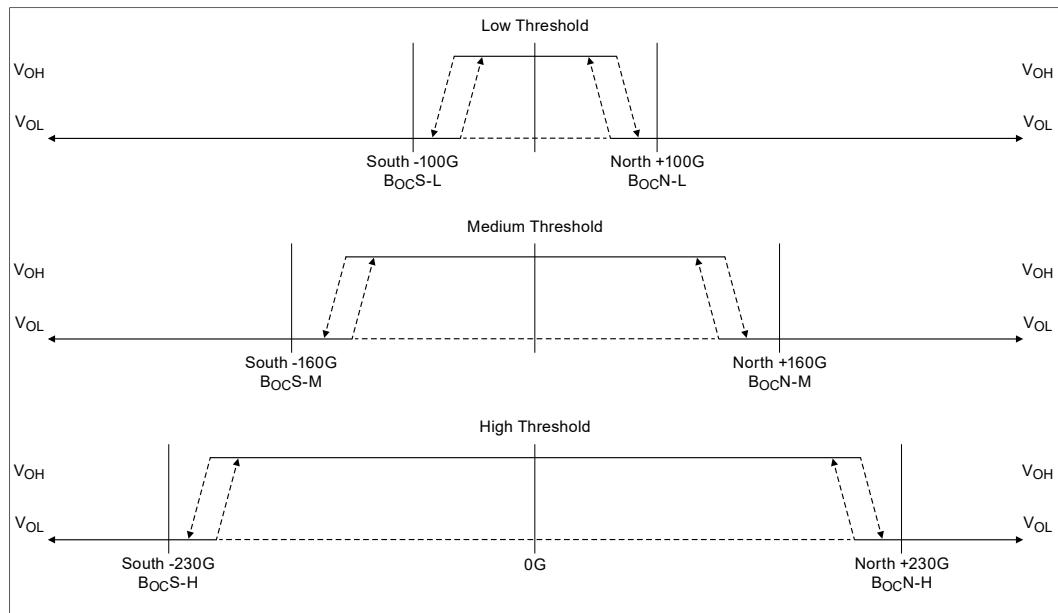


Figure 9. Output operation at each of the three standalone threshold settings

## 10.6 I<sup>2</sup>C user mode, output assertion

Table 33. I<sup>2</sup>C user mode, recommended lowest USER\_ASSERT\_THRESH [7:3] output assertion

Symbol	Description	Condition	Min	Typ	Max	Unit
B <sub>OA</sub> -I2C	Output assertion, magnetic field collapsing	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	—	< 0x10	—	hex

## 10.7 I<sup>2</sup>C user mode, output clear

Table 34. I<sup>2</sup>C user mode, recommended highest USER\_CLEAR\_THRESH [7:3] output clear

Symbol	Description	Condition	Min	Typ	Max	Unit
B <sub>OC</sub> -I2C	Output clear, magnetic field increasing	T <sub>A</sub> Min ≤ T <sub>A</sub> ≤ T <sub>A</sub> Max, V <sub>DD</sub> Min ≤ V <sub>DD</sub> ≤ V <sub>DD</sub> Max	—	> 0xF0	—	hex

## 11 Application information

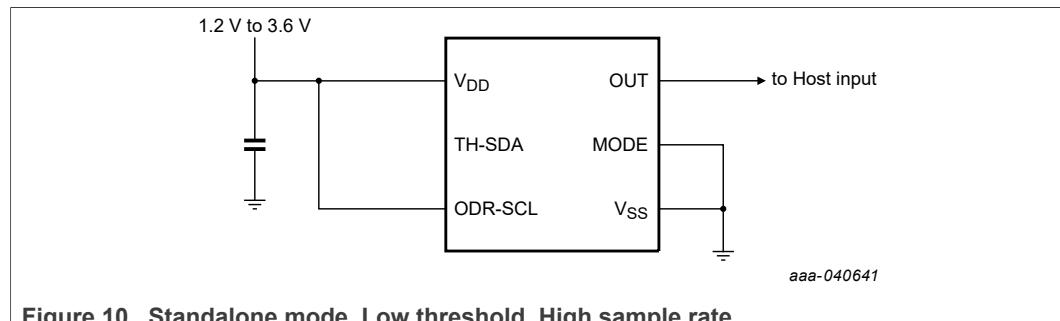


Figure 10. Standalone mode, Low threshold, High sample rate

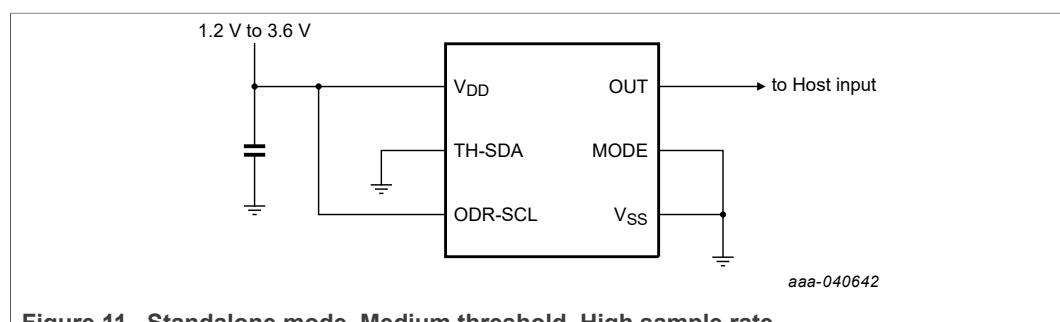


Figure 11. Standalone mode, Medium threshold, High sample rate

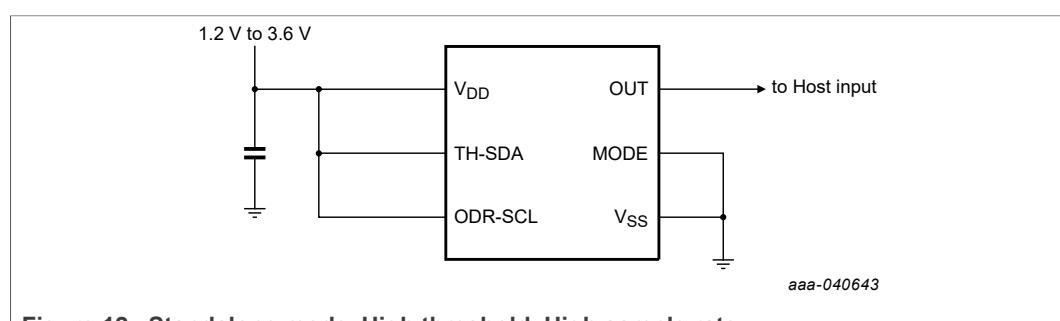


Figure 12. Standalone mode, High threshold, High sample rate

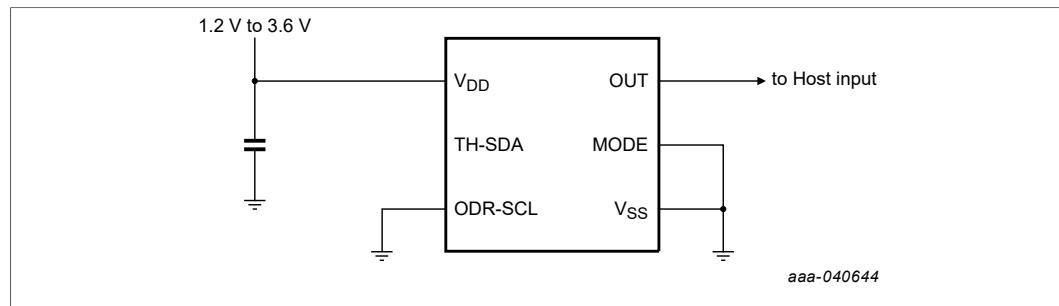


Figure 13. Standalone mode, Low threshold, Medium sample rate

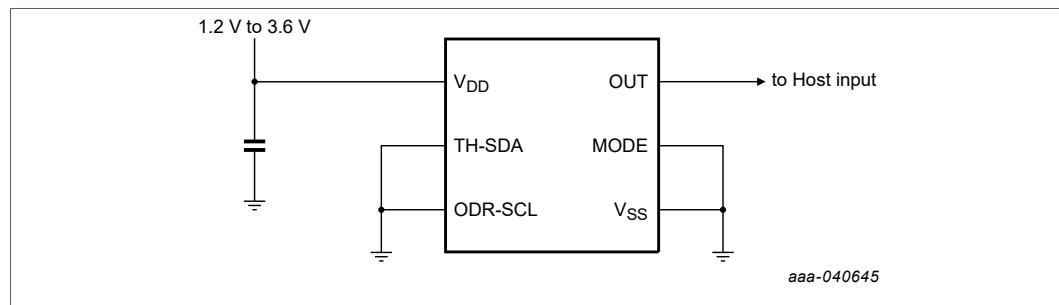


Figure 14. Standalone mode, Medium threshold, Medium sample rate

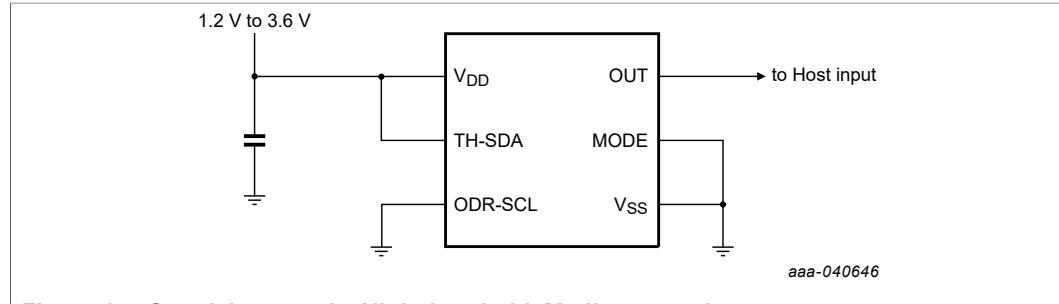


Figure 15. Standalone mode, High threshold, Medium sample rate

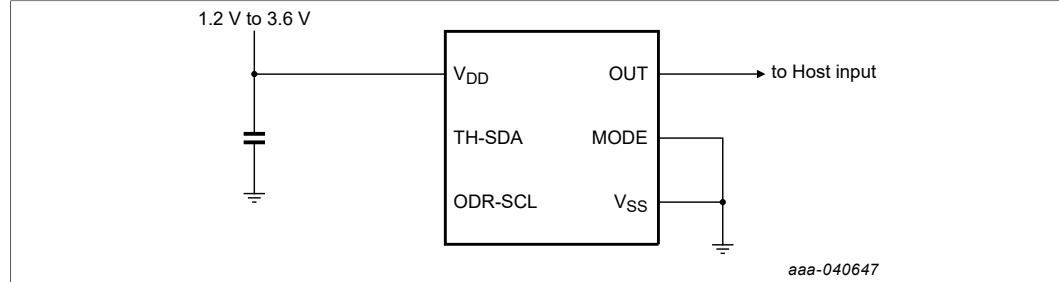


Figure 16. Standalone mode, Low threshold, Low sample rate

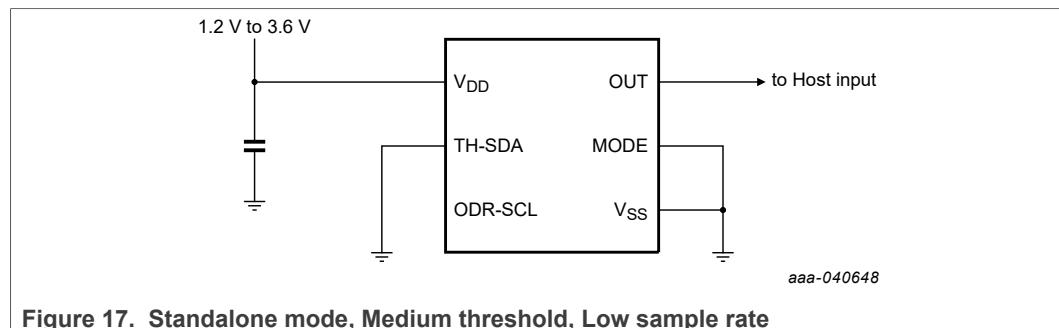


Figure 17. Standalone mode, Medium threshold, Low sample rate

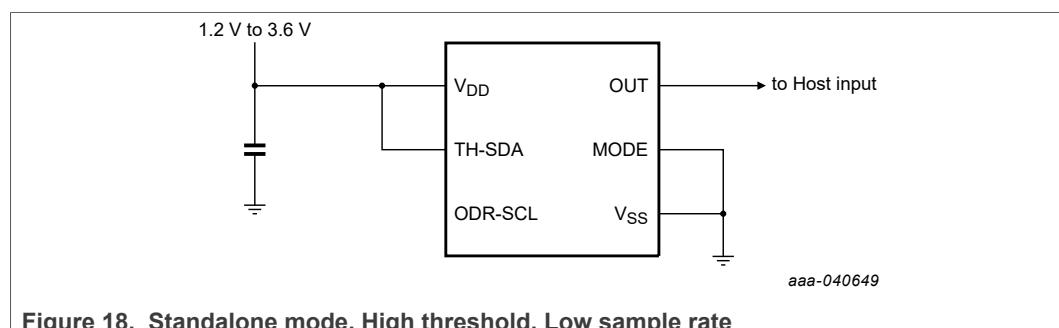
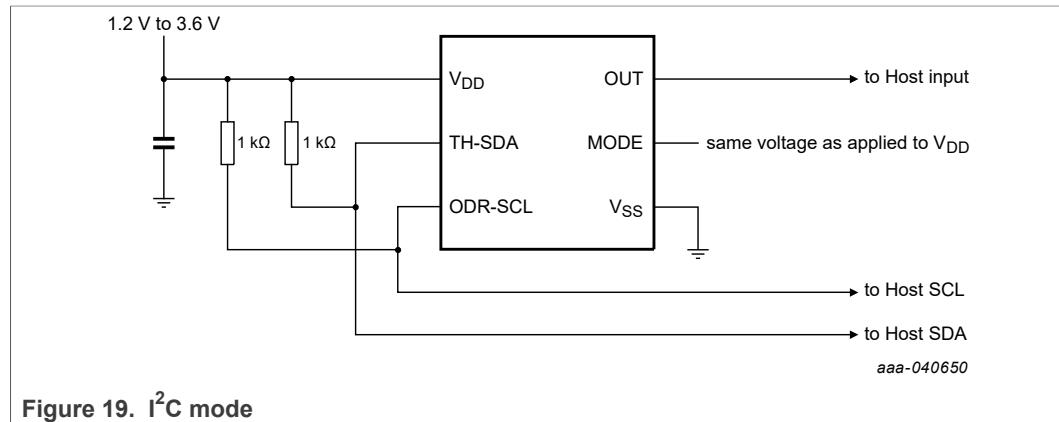


Figure 18. Standalone mode, High threshold, Low sample rate

Figure 19. I<sup>2</sup>C mode

## 12 Package outline

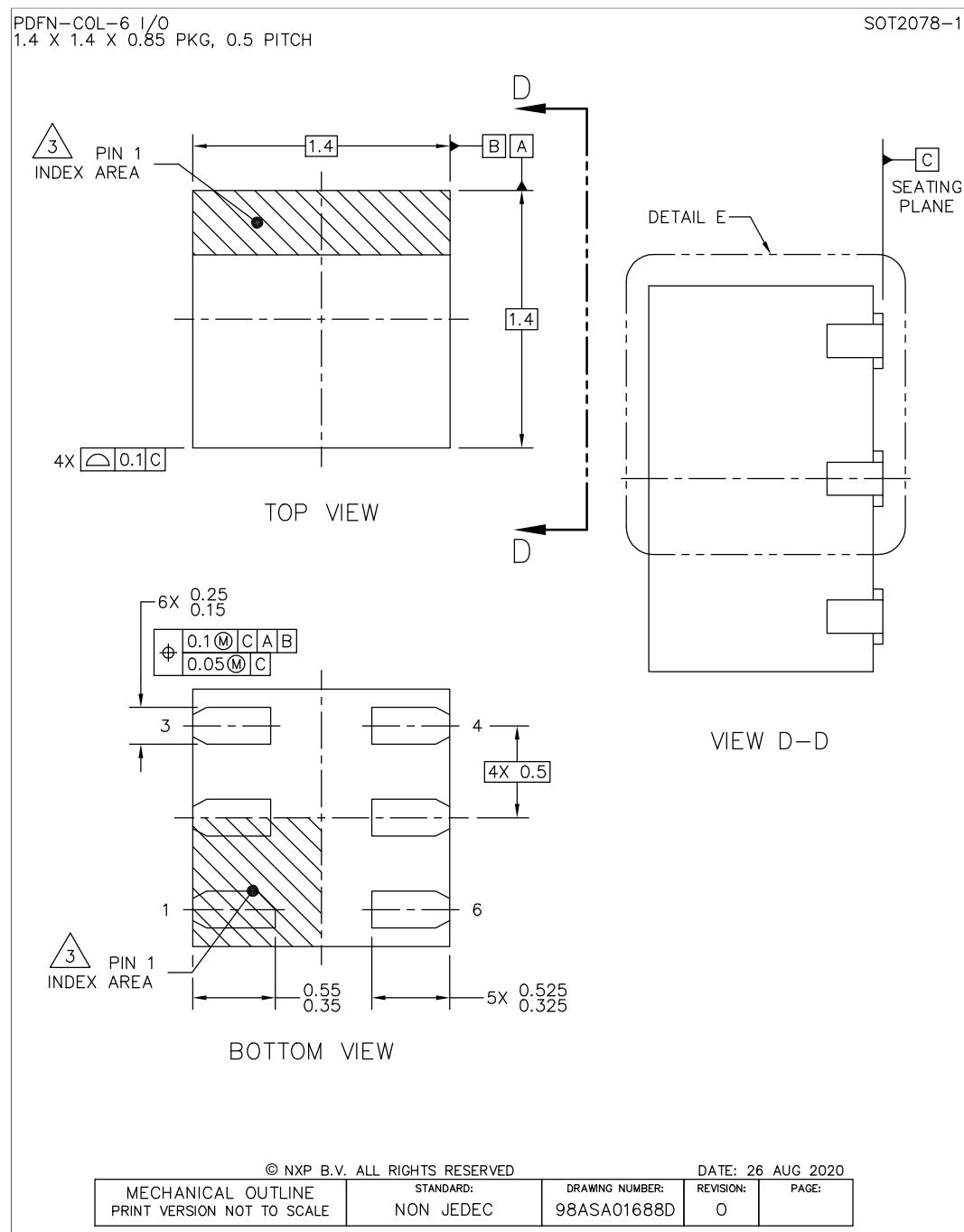


Figure 20. Package outline VSON6 (SOT2078-1)

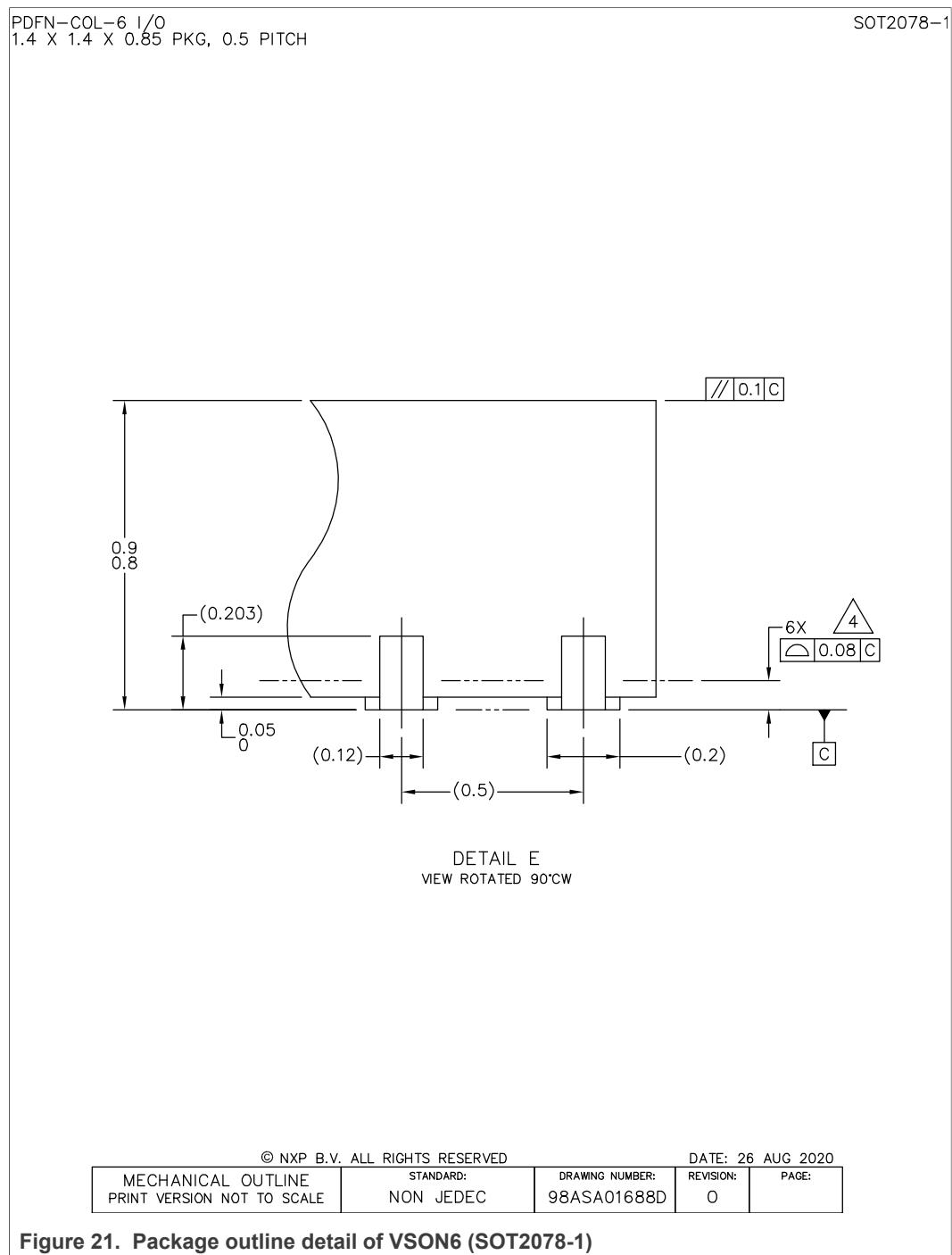


Figure 21. Package outline detail of VSON6 (SOT2078-1)

PDFN-COL-6 I/O  
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

SOT2078-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS.
5. MIN. METAL GAP SHOULD BE 0.15 MM.

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DATE: 26 AUG 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01688D	REVISION: O	PAGE:
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Figure 22. Package outline note VSON6 (SOT2078-1)

## 13 Soldering information

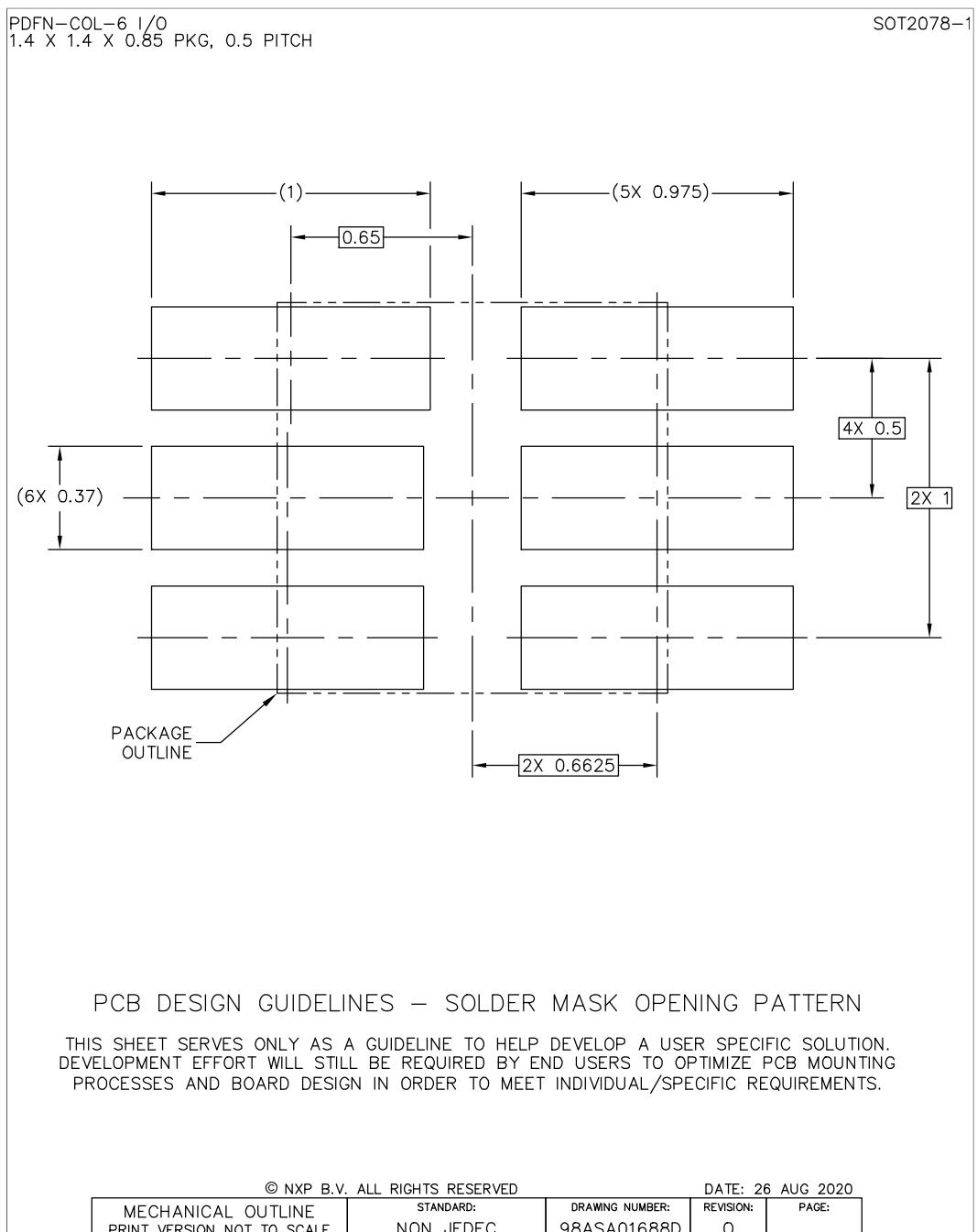
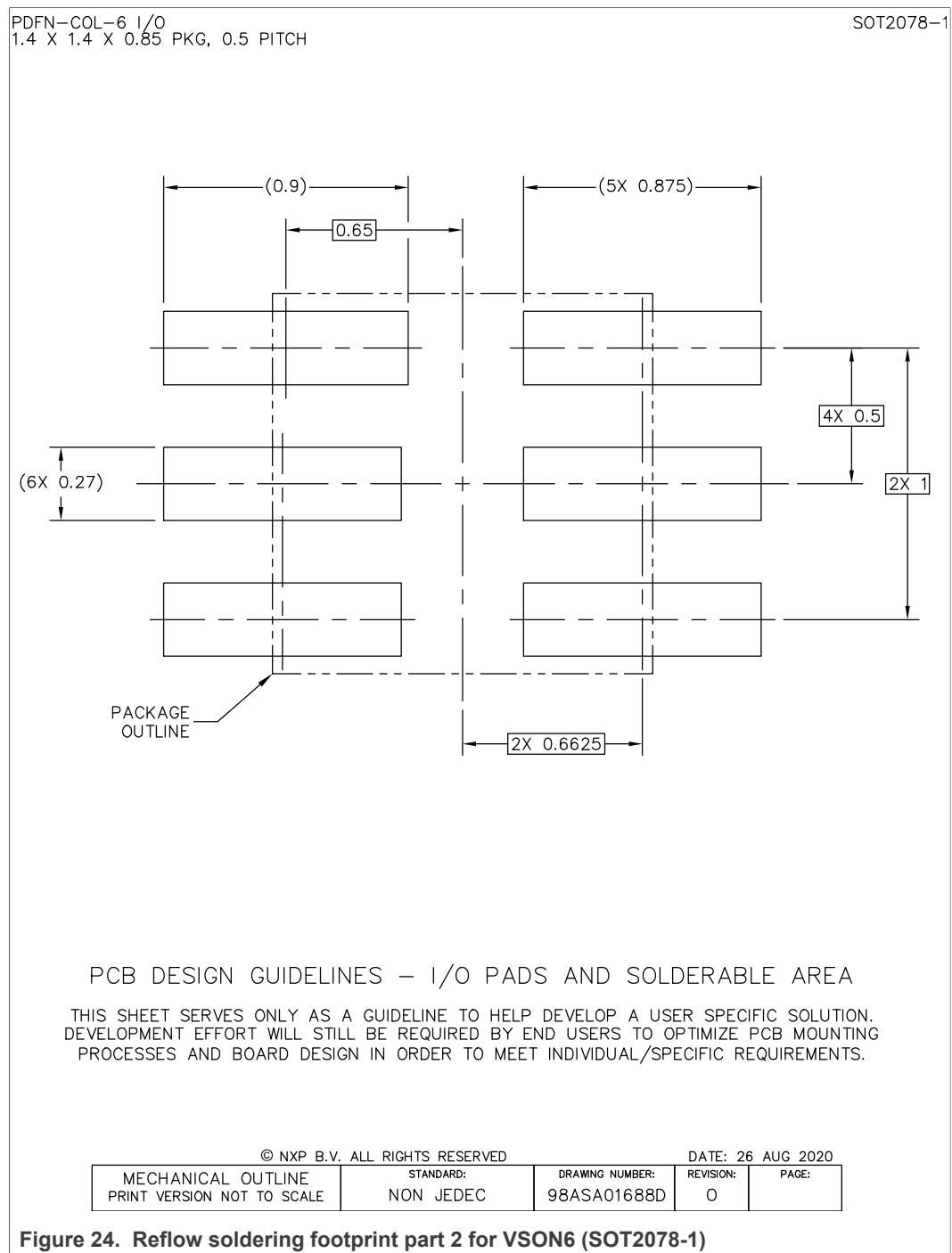
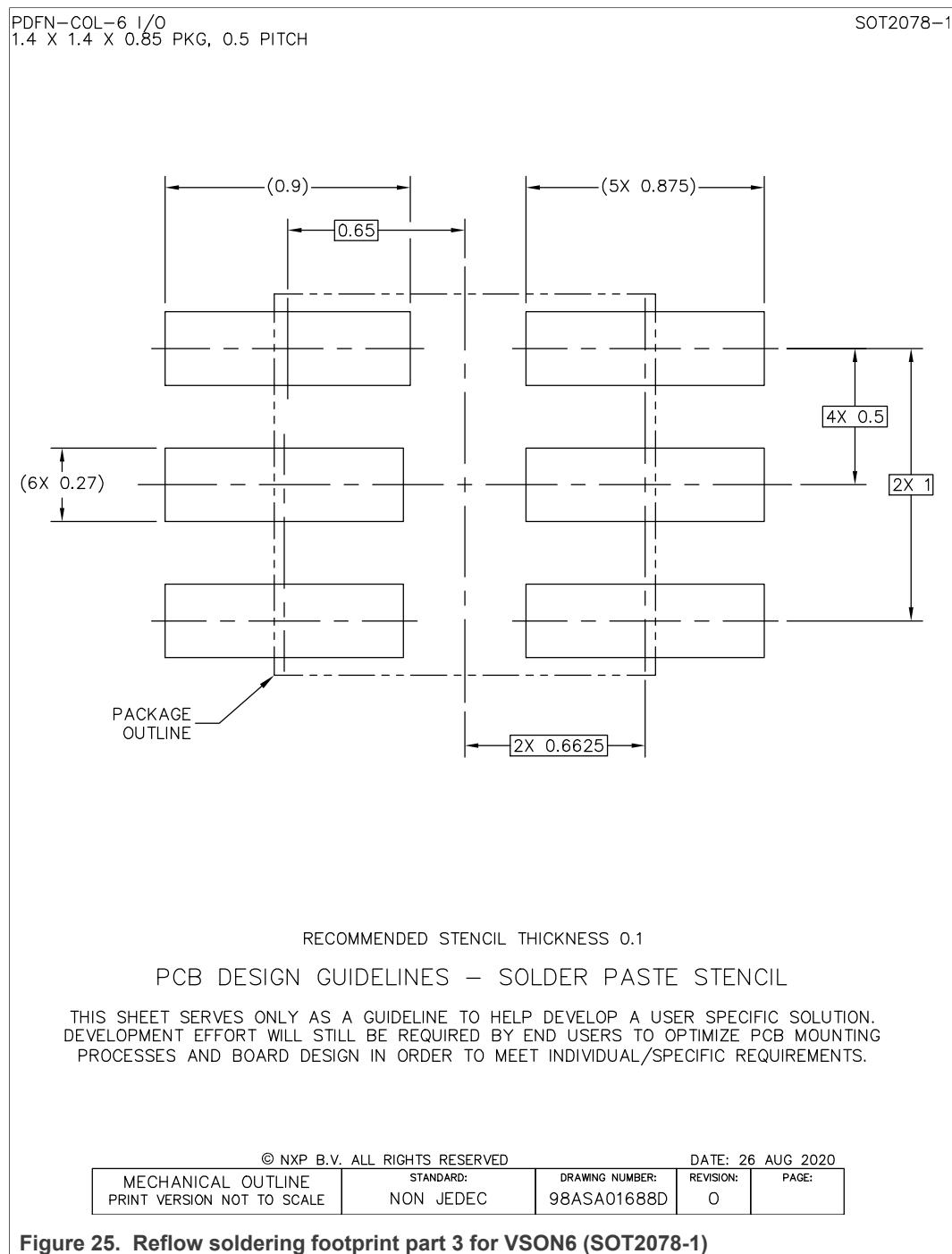


Figure 23. Reflow soldering footprint part 1 for VSON6 (SOT2078-1)





## 14 References

[1] AN1902 — Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages  
<https://www.nxp.com/docs/en/application-note/AN1902.pdf>

## 15 Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NMH1000 v.2	20230405	Product data sheet	—	NMH1000 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 8, Table 26</a>, <math>I_{SUBIO}</math>: revised the Typ value from "600" to "100" and revised the Unit from "<math>\mu A</math>" to "mA".</li> <li>• <a href="#">Section 9, Table 27</a>, revised as follows: <ul style="list-style-type: none"> <li>– <math>t_{OP}</math>: revised the Typ value from "2" to "4.8" and Max value from "—" to "5.1"..</li> <li>– <math>T_A</math>: revised the Min value from 0 °C to -40 °C and revised the Max value from +70 to +85.</li> </ul> </li> <li>• <a href="#">Section 10.1, Table 28</a>, revised as follows: <ul style="list-style-type: none"> <li>– <math>I_{DDS-LODR}</math>: revised the Max value from "139" to "187".</li> <li>– <math>I_{DDS-MODR}</math>: revised the Max value from "193" to "234".</li> <li>– <math>I_{DDS-HODR}</math>: revised the Max value form "700" to "760".</li> <li>– <math>I_{DDS-S}</math>, <math>I_{DDS-M}</math>, and <math>I_{DDS-2}</math>: inserted three rows at the end of the table.</li> </ul> </li> <li>• <a href="#">Section 10.2, Table 29</a>, <math>f_{SCL}</math>: revised the Max value from "100" to "1" and revised the Unit from "kHz" to "MHz".</li> <li>• <a href="#">Section 10.3, Table 30</a>, revised as follows: <ul style="list-style-type: none"> <li>– <math>I_{PIN}</math>: inserted new row.</li> <li>– <math>I_{IH}</math>, <math>I_{IL}</math>, <math>I_{OH}</math>, and <math>I_{OL}</math>: removed the rows from the table.</li> </ul> </li> <li>• <a href="#">Section 10.4, Table 31</a>, revised as follows: <ul style="list-style-type: none"> <li>– <math>C_B</math>: revised Max value from "100" to "1".</li> <li>– <math>C_B</math>: revised the Unit from "pF" to "<math>\mu F</math>".</li> <li>– <math>t_{SU}</math> to <math>t_{STA}</math>: revised the Unit from "<math>\mu</math>" to "<math>\mu s</math>".</li> <li>– <math>t_{SU}</math> to <math>t_{DAT}</math>: revised the Unit from "<math>\mu s</math>" to "ns".</li> </ul> </li> </ul>			
NMH1000 v.1	20230303	Product data sheet	—	—
Modifications:	<ul style="list-style-type: none"> <li>• Initial release.</li> </ul>			

## 16 Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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## Tables

Tab. 1.	Ordering information .....	2
Tab. 2.	Pin description .....	4
Tab. 3.	Fixed threshold selection .....	6
Tab. 4.	User-defined assert thresholds .....	6
Tab. 5.	User-defined output clear thresholds .....	6
Tab. 6.	Sample rate selection .....	7
Tab. 7.	I2C mode user-defined sample rate .....	7
Tab. 8.	User-defined output assert and clear states .....	8
Tab. 9.	Register map overview .....	11
Tab. 10.	STATUS – Status reporting of modes and selections (address \$00h) bit allocation .....	11
Tab. 11.	STATUS – Status reporting of modes and selections (address \$00h) bit descriptions .....	11
Tab. 12.	CONTROL_Reg1 – Control of operations(address \$01h) bit allocation .....	12
Tab. 13.	CONTROL_Reg1 – Control of operations (address \$01h) bit description .....	12
Tab. 14.	OUT_M_REG – Magnetic strength report (address \$03h) bit allocation .....	13
Tab. 15.	OUT_M_REG – Magnetic strength report (address \$03h) bit description .....	14
Tab. 16.	USER_ASSERT_THRESH – User selectable output, assert threshold, N or S (address \$04h) bit allocation .....	14
Tab. 17.	USER_ASSERT_THRESH – User selectable output, assert threshold, N or S (address \$04h) bit description .....	14
Tab. 18.	USER_CLEAR_THRESH – User selectable output, clear threshold, N or S (address \$05h) bit allocation .....	14
Tab. 19.	USER_CLEAR_THRESH – User selectable output, clear threshold, N or S (address \$05h) bit description .....	15
Tab. 20.	USER_ODR – User selectable sleep sample output data rates (address \$06h) bit allocation .....	15
Tab. 21.	USER_ODR – User selectable sleep sample output data rates (address \$06h) bit description .....	15
Tab. 22.	WHO_AM_I - I2C configured identifier (address \$08h) bit allocation .....	15
Tab. 23.	WHO_AM_I - I2C configured identifier (address \$08h) bit description .....	16
Tab. 24.	I2C_ADDR - I2C configured identifier (address \$09h) bit allocation .....	16
Tab. 25.	I2C_ADDR - I2C configured identifier (address \$09h) bit description .....	16
Tab. 26.	Limiting values .....	16
Tab. 27.	Operating conditions .....	17
Tab. 28.	Supply currents .....	18
Tab. 29.	Clocks and rates .....	18
Tab. 30.	I2C pin thresholds .....	19
Tab. 31.	Serial data timing characteristics .....	19
Tab. 32.	Magnetic field characteristics .....	20
Tab. 33.	I2C user mode, recommended lowest USER_ASSERT_THRESH [7:3] output assertion .....	21
Tab. 34.	I2C user mode, recommended highest USER_CLEAR_THRESH [7:3] output clear ....	21
Tab. 35.	Revision history .....	30

## Figures

Fig. 1.	Block diagram .....	2
Fig. 2.	Pin configuration .....	3
Fig. 3.	Magnetic field vs. package orientation .....	4
Fig. 4.	NMH1000 functional state flow diagram .....	5
Fig. 5.	Output operation .....	8
Fig. 6.	I2C timing diagram .....	9
Fig. 7.	I2C write operation .....	10
Fig. 8.	I2C read operation .....	10
Fig. 9.	Output operation at each of the three standalone threshold settings .....	20
Fig. 10.	Standalone mode, Low threshold, High sample rate .....	21
Fig. 11.	Standalone mode, Medium threshold, High sample rate .....	21
Fig. 12.	Standalone mode, High threshold, High sample rate .....	21
Fig. 13.	Standalone mode, Low threshold, Medium sample rate .....	22
Fig. 14.	Standalone mode, Medium threshold, Medium sample rate .....	22
Fig. 15.	Standalone mode, High threshold, Medium sample rate .....	22
Fig. 16.	Standalone mode, Low threshold, Low sample rate .....	22
Fig. 17.	Standalone mode, Medium threshold, Low sample rate .....	23
Fig. 18.	Standalone mode, High threshold, Low sample rate .....	23
Fig. 19.	I2C mode .....	23
Fig. 20.	Package outline VSON6 (SOT2078-1) .....	24
Fig. 21.	Package outline detail of VSON6 (SOT2078-1) .....	25
Fig. 22.	Package outline note VSON6 (SOT2078-1) ....	26
Fig. 23.	Reflow soldering footprint part 1 for VSON6 (SOT2078-1) .....	27
Fig. 24.	Reflow soldering footprint part 2 for VSON6 (SOT2078-1) .....	28
Fig. 25.	Reflow soldering footprint part 3 for VSON6 (SOT2078-1) .....	29

## Contents

1	General description .....	1	7.6.2.8	I2C configured identifier (I2C_ADDR) (\$09h) .....	16
2	Features and benefits .....	1	8	Limiting values .....	16
3	Applications .....	1	9	Recommended operating conditions .....	17
4	Ordering information .....	2	10	Characteristics .....	18
5	Block diagram .....	2	10.1	Supply currents .....	18
5.1	Block descriptions .....	3	10.2	Clocks and rates .....	18
6	Pinning information .....	3	10.3	I2C pin thresholds .....	19
6.1	Pinning .....	3	10.4	Serial data timing characteristics .....	19
6.2	Pin description .....	4	10.5	Magnetic field characteristics .....	20
6.3	Orientation .....	4	10.6	I2C user mode, output assertion .....	21
7	Functional description .....	5	10.7	I2C user mode, output clear .....	21
7.1	Operating modes .....	5	11	Application information .....	21
7.1.1	Functional states .....	5	12	Package outline .....	24
7.1.2	Interface Operational Modes .....	5	13	Soldering information .....	27
7.2	Threshold configurations .....	6	14	References .....	29
7.2.1	Fixed thresholds .....	6	15	Revision history .....	30
7.2.1.1	Fixed threshold selection via VTH pin voltage .....	6	16	Legal information .....	31
7.2.2	User-defined threshold .....	6			
7.3	Sample rate configurations .....	7			
7.3.1	Fixed sample rates .....	7			
7.3.1.1	Sample rate selection via VODR pin voltage .....	7			
7.3.2	User-defined sample rate .....	7			
7.4	Output control function description .....	8			
7.4.1	Output hysteresis .....	8			
7.4.2	Control Output State .....	8			
7.4.2.1	Standalone mode output assert / clear states .....	8			
7.4.2.2	User-defined output assert / clear states .....	8			
7.5	I2C serial data function description .....	8			
7.5.1	I2C pin functions .....	8			
7.5.2	I2C timing diagram .....	9			
7.5.3	I2C operation .....	9			
7.5.4	I2C protocol diagram .....	10			
7.6	Register map .....	11			
7.6.1	Register overview .....	11			
7.6.2	Register details .....	11			
7.6.2.1	Status reporting of modes and selections (STATUS) (\$00h) .....	11			
7.6.2.2	Control of operations (CONTROL_Reg1) (\$01h) .....	12			
7.6.2.3	Magnetic strength report (OUT_M_REG) (\$03h) .....	13			
7.6.2.4	User selectable output, assert threshold, N or S (USER_ASSERT_THRESH) (\$04h) .....	14			
7.6.2.5	User selectable output, clear threshold, N or S (USER_CLEAR_THRESH) (\$05h) .....	14			
7.6.2.6	User selectable sleep sample output data rates (USER_ODR) (\$06h) .....	15			
7.6.2.7	I2C configured identifier (WHO_AM_I) (\$08h) .....	15			

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