

Jitter Optimized, Factory Programmable TCXO

ASGTX5

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ESD Sensitive



5.0 x 3.2 x 1.5 mm

RoHS/RoHS II Compliant

MSL Level = 1

Features

- Ultra-Low Jitter: 332 fs Typ RMS @ 156.25MHz
- Available with any frequency from 15MHz to 2,100MHz
- Factory programmable
- Lowest in-class power consumption (75mA Typ LVDS)
- ± 3.0 ppm stability over -40 to +85°C
- 3.3V, 2.5V, 1.8V Vdd supply voltage
- LVPECL, LVDS, HCSL, & CML differential output options
- Industry standard 5.0 x 3.2mm footprint
- Meets Stratum-IV requirement of $< \pm 25$ ppm All Inclusive Frequency Stability over product life

Common Key Electrical Specifications

Applications

- Networking & communications
- 10G/40G/100G optical Ethernet
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range	LVPECL	15		2,100	MHz	Option "P"
	LVDS	15		2,100		Option "D"
	HCSL	15		700		Option "H"
	CML	15		2,100		Option "M"
Supply Voltage (Vdd) ^[Note 1]		2.97	3.30	3.63	V	Option "A"
		2.25	2.50	2.75		Option "B"
		1.71	1.80	1.89		Option "C"
Supply Current (Idd)	LVPECL		100	120	mA	Max @ 2,100MHz; 3.3V
	LVDS		75	90		Max @ 2,100MHz; 3.3V
	HCSL		80	100		Max @ 700MHz; 3.3V
	CML		70	85		Max @ 2,100MHz; 3.3V
Operating Temperature Range		-20		+70	°C	Option "D"
		-40		+85		Option "F"
Storage Temperature		-55		+15	°C	
Frequency Accuracy (Initial Set-Tolerance) ^[Note 2] at time of shipment (Pre-Reflow) @ +25°C ± 3 °C		-1.00		+1.0	ppm	Relative to carrier
Shift through Reflow Soldering		-1.00		+1.0 0	ppm	Relative to initial tolerance
Frequency Stability over Operating Temperature Range, relative to post reflow stabilized frequency		-2.5	$< \pm 1.00$	+2.5	ppm	Over -20°C to +70°C
		-3.0	$< \pm 2.00$	+3.0		Over -40°C to +85°C

Note 1: Supply Voltage (Vdd) = 1.80V option not available with LVPECL output

Note 2: Some non-standard carrier frequencies between 15MHz and 2.1GHz may not be able to meet the Initial Frequency Accuracy (Initial Set-Tolerance) at time of shipment (Pre-Reflow). Please contact Abracon for details.



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Parameters			Min.	Typ.	Max.	Unit	Notes
Aging over first year @ +25°C±3°C			-1.00		+1.00	ppm	
Aging over 20 Year Product Life [Note 3]			-7.00		+7.00	ppm	
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life [Note 3 & 4]			-11.50		+11.5	ppm	Over -20°C to +70°C
			-12.50		+12.5		Over -40°C to +85°C
Rise (Tr) / Fall (Tf) Time (20% to 80% V _{peak} to peak)					400	ps	
Duty Cycle			45		55	%	
Powerup Time				< 5.0	10	ms	
Output Enable & Disable Control			0.7*(V _{dd})			V	Output Enable; or No Connect
					0.3*(V _{dd})		Output Disable; High Impedance
Output Enable Time					2.50	ms	70% of VDD (min.) to enable output
Output Disable Time					10	µs	30% of VDD (max) to disable output
Output Disable Current Consumption	LVPECL			99		mA	Max @ 2100MHz; 3.3V
	LVDS			74			Max @ 2100MHz; 3.3V
	HCSL			79			Max @ 700MHz; 3.3V
	CML			69			Max @ 2100MHz; 3.3V
Output High Voltage (V _{OH}) Output Low Voltage (V _{OL})	LVPECL	V _{OH}	V _{dd} -1.03		V _{dd} -0.6	V	50Ω to V _{dd} -2.0V or Thevenin equivalent
		V _{OL}	V _{dd} -1.85		V _{dd} -1.6		
	LVDS	V _{OH}		1.4	1.6		100Ω between OUT-P and OUT-N
		V _{OL}	0.9	1.1			
	HCSL	V _{OH}	0.66		1.15		50Ω to GND
		V _{OL}	0.0		0.15		
	CML	V _{OH}	V _{dd} -0.085		V _{dd}		50Ω to V _{dd}
		V _{OL}	V _{dd} -0.6		V _{dd} -0.32		

Note 3: Relative to post reflow measured frequency @ +25°C±3°C

Note 4: Includes initial frequency accuracy, shift through Reflow, stability over operating temperature, load pulling, frequency pushing and aging over (20) years



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RMS Phase Jitter (12 kHz -20 MHz BW) | Vdd= +3.3V

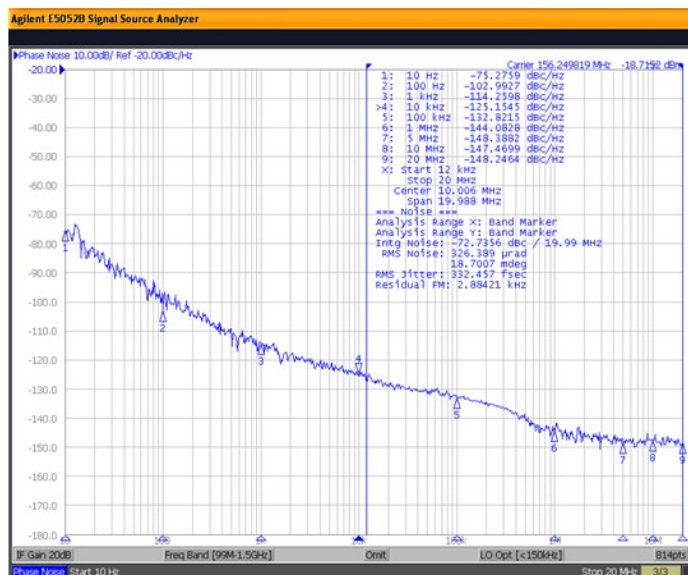
Carrier F0 (MHz)	Min.	Typ.	Max.	Unit	Notes
15.00 to 50.00		< 500		fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
51.00 to 1,200		< 350		fsec	
1,201 to 2,100		< 225		fsec	

Phase Noise Test Setup

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = NOT Omitted (Normalized in dBc/Hz)
- Specified Spur Omission Function = NOT Enabled
- IF Gain = 20dB
- Attenuation = 5dB
- Average = 3

Representative Phase Noise Plots

F0=156.2500MHz, Vdd=3.3V, LVPECL
rms Phase Jitter = 332 fsec



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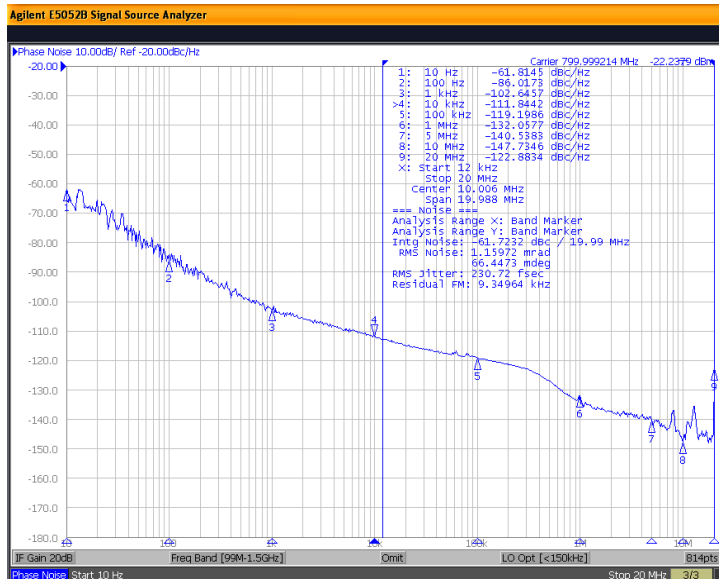


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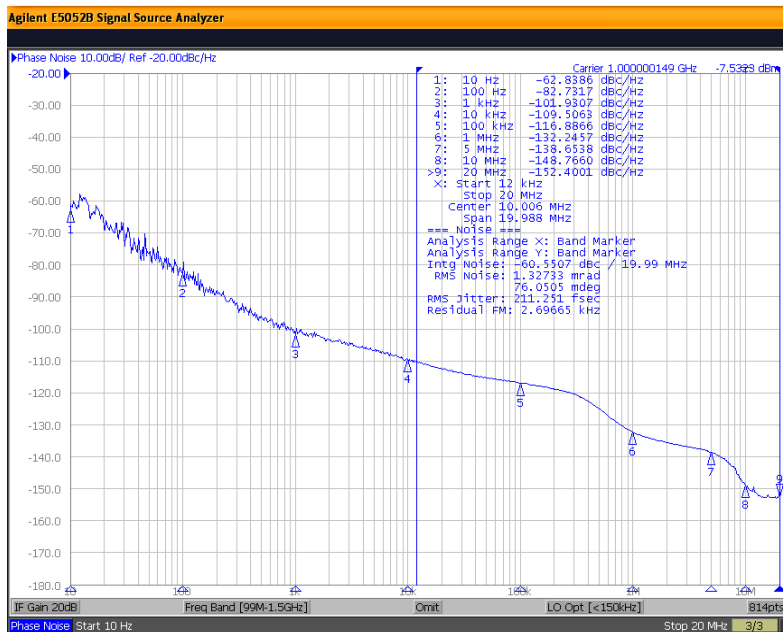


5.0 x 3.2 x 1.5 mm
RoHS/RoHS II Compliant
MSL Level = 1

F0=800.0000MHz, Vdd=3.3V, LVPECL
rms Phase Jitter = 231 fsec



F0=1.0000GHz, Vdd=3.3V, LVPECL
rms Phase Jitter = 211 fsec



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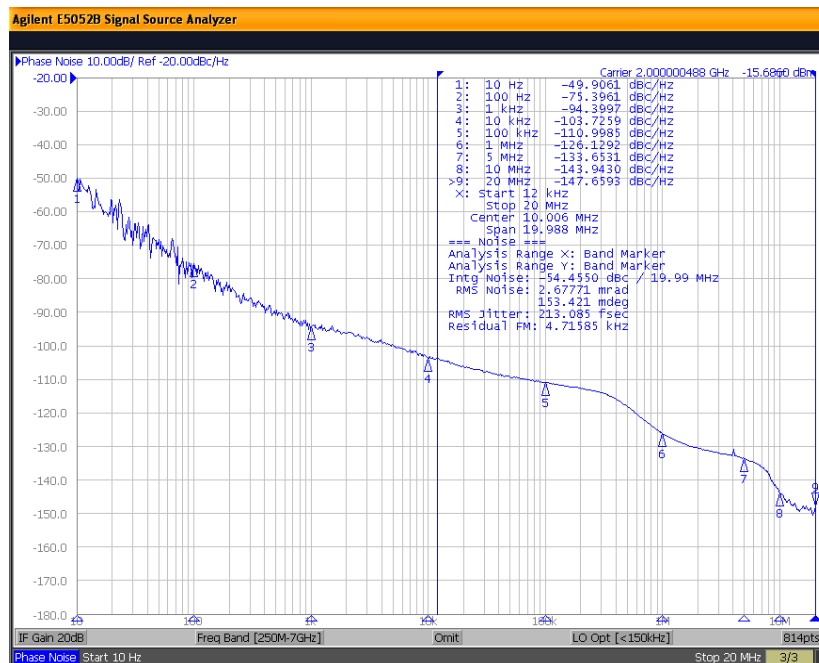
5.0 x 3.2 x 1.5 mm

RoHS/RoHS II Compliant

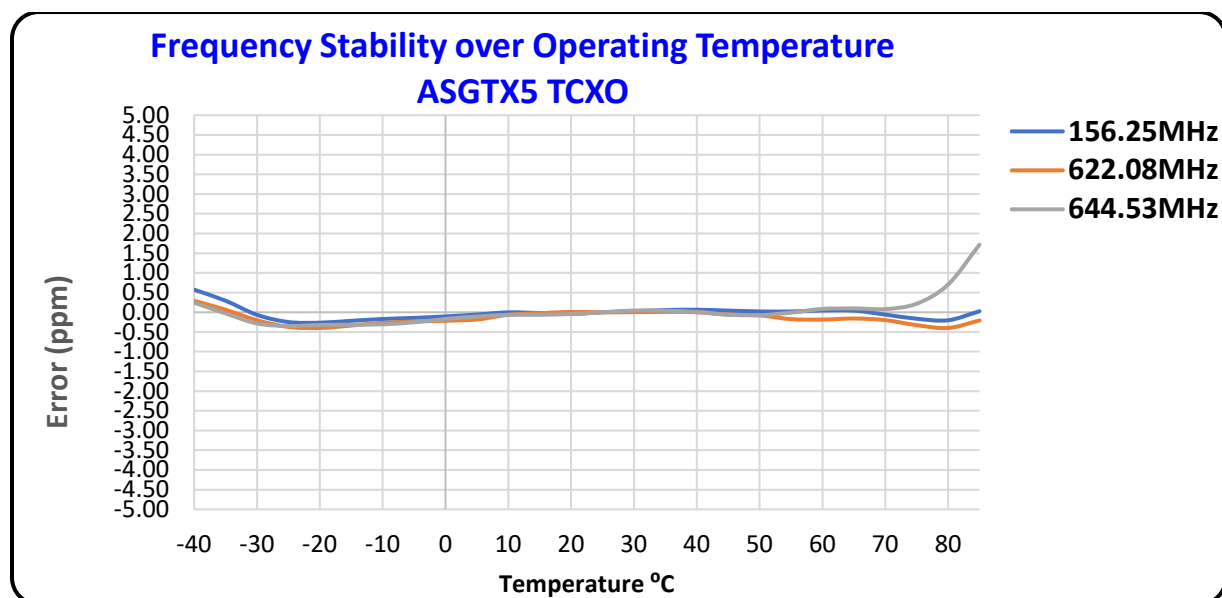
MSL Level = 1

F0=2.0000GHz, Vdd=3.3V, LVPECL

rms Phase Jitter = 213 fsec



Typical Frequency vs. Temperature Characteristics



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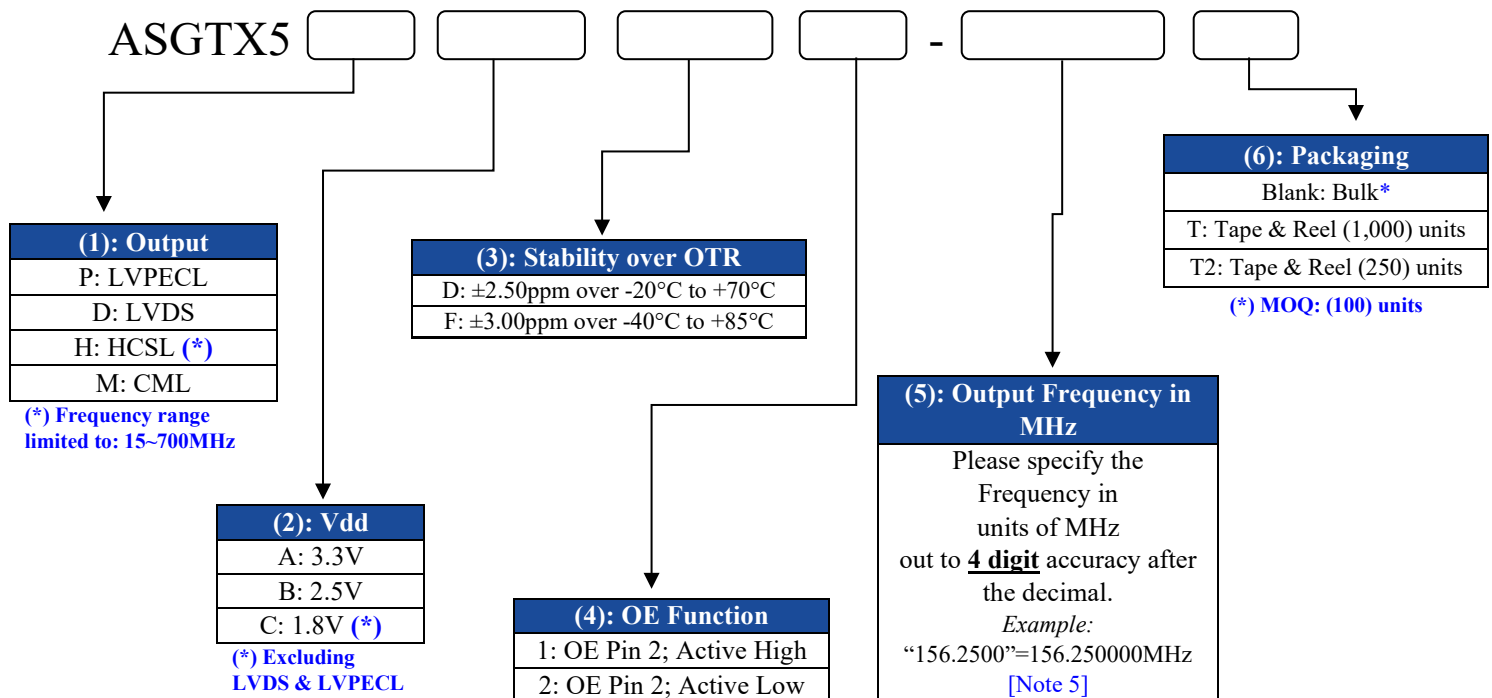


5.0 x 3.2 x 1.5 mm

RoHS/RoHS II Compliant

MSL Level = 1

Options and Part Identification [\[Note 5\]](#)



Part Number Example:

ASGTX5PAD1-156.2500T2

Note 5: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.

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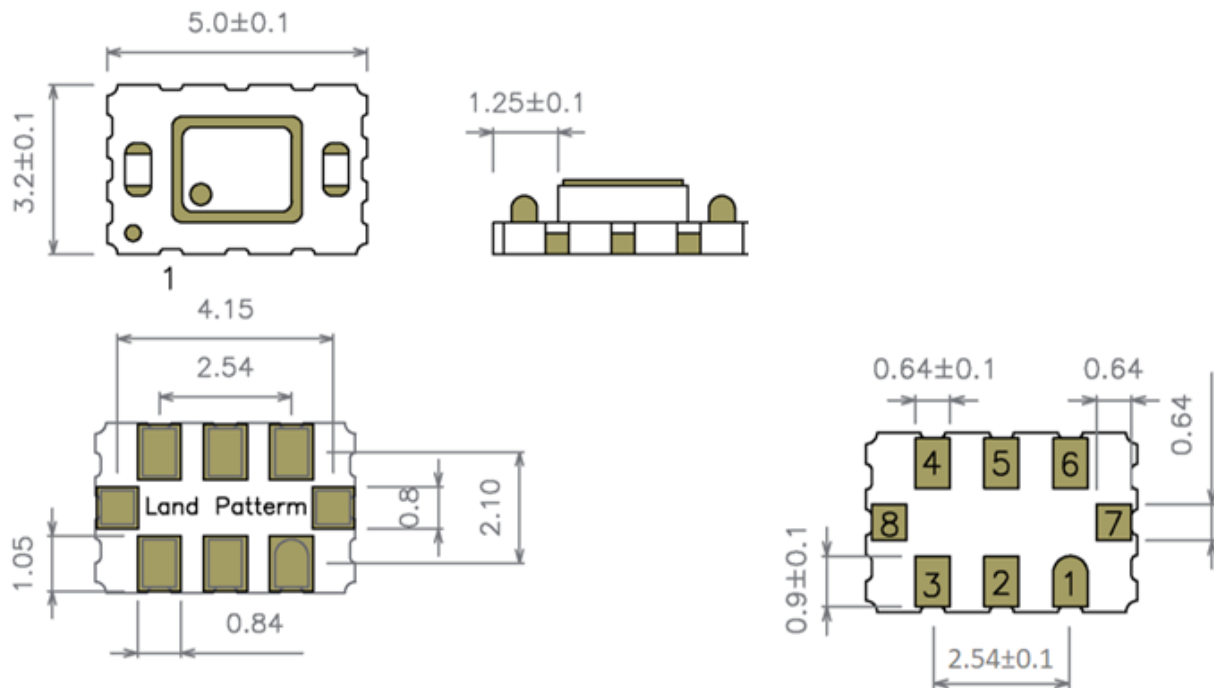


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MSL Level = 1

Mechanical Dimensions & Pin Configuration



Pin#	Function
1	No Connect (NC) {TCXO Configuration}
2	Output Enable / Disable (OE)
3	Ground
4	RF Output (Q)
5	RF Output Complimentary (Q')
6	Supply Voltage (Vdd)
7	Do Not Connect (leave floating)
8	Do Not Connect (leave floating)

Option	OE pin functionality (Pin#2)
1	Output Enable Active HIGH
2	Output Enable Active LOW

Dimensions: [mm]

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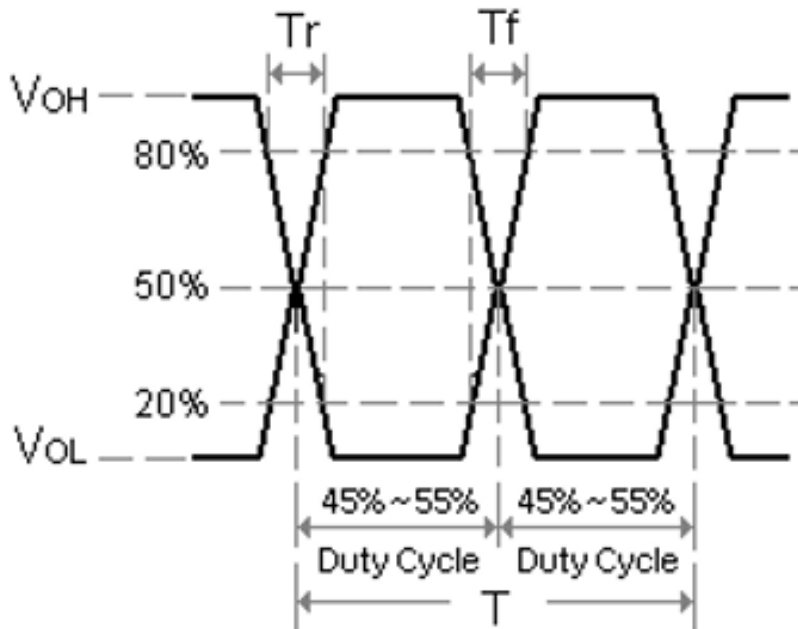


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Differential Output Waveform



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Reflow Profile [JEDEC J-STD-020]

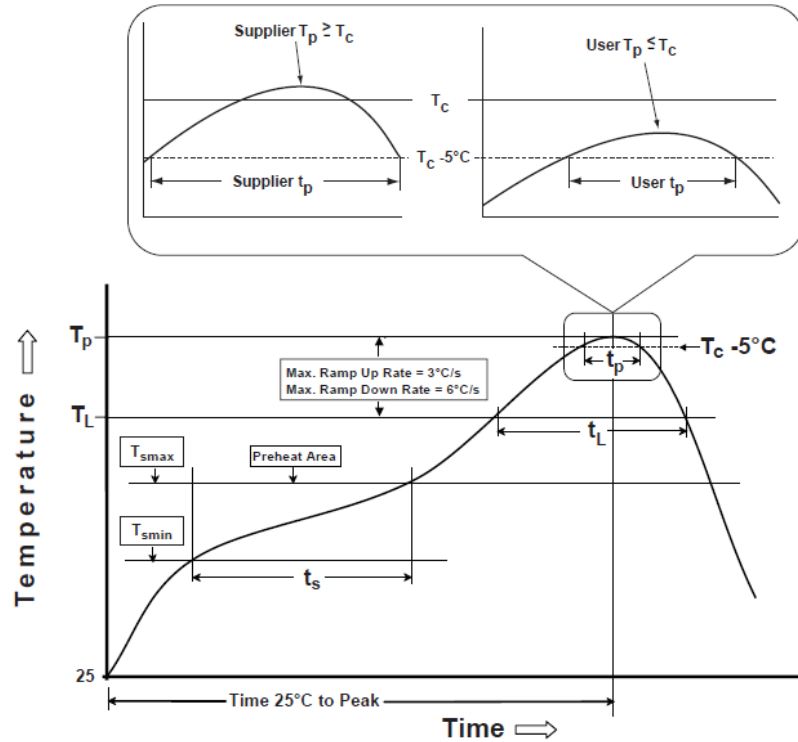


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_p)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_p)*	see Table 1	see Table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

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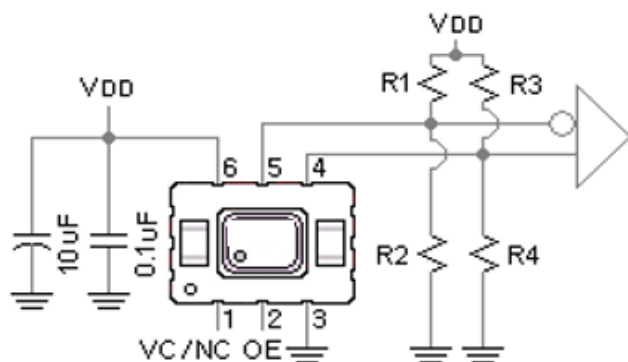


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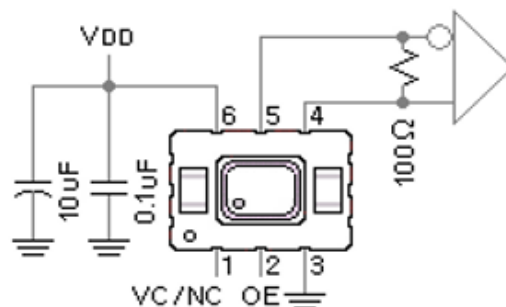
Recommended Test Circuit

LVPECL

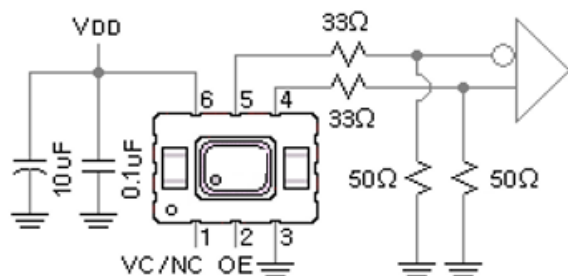


Vdd=3.3V: R1=R3=127Ω; R2=R4=82.5 Ω
Vdd=2.5V: R1=R3=250Ω; R2=R4=62.5 Ω

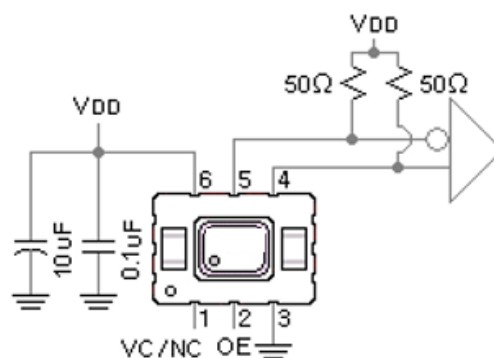
LVDS



HCSL



CML



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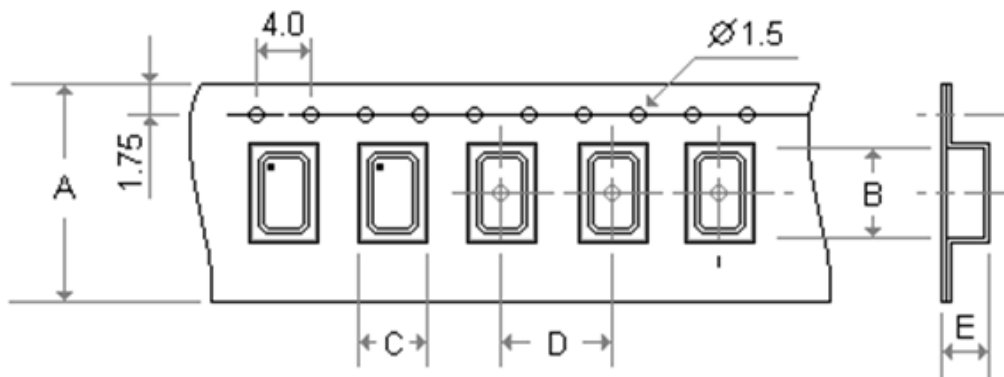
Packaging

Blank = Bulk*[*MOQ = (100) units]

T = Tape & Reel (1,000) units / reel

T2 = Tape & Reel (250) units / reel

Feeding (PULL) Direction →

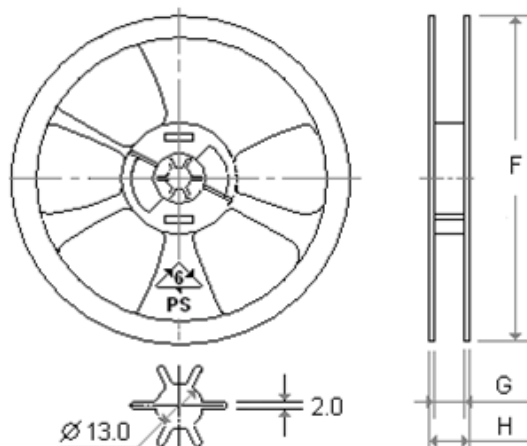


Tape Dimensions (mm)

A	12.0
B	5.3
C	3.6
D	8.0
E	1.4

Reel Dimensions

F	180
G	13.0
H	16.0



Dimensions: [mm]

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