



NR1620 series

150 mA 0.4 V Output & Ultra-Low Supply Current Voltage Regulator

FEATURES

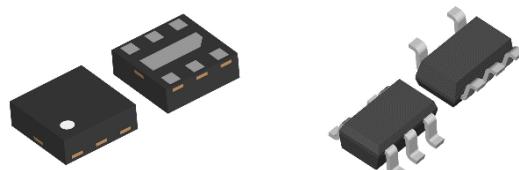
- Quiescent Current: Typ. 0.4 μ A
- Output Voltage Accuracy: ± 9.9 mV ($T_a = 25^\circ\text{C}$)
- Input Voltage Range (Maximum rating):
 V_{BIAS} : 2.4 V to 5.5 V (6.5 V)
 V_{IN} : 0.6 V to V_{BIAS} (6.5 V)
- Output Voltage Range: 0.4 V to 1.2 V (0.1 V step)
- Ripple Rejection:
Typ. 90 dB ($f = 1$ kHz, Ripple in V_{IN})
Typ. 60 dB ($f = 100$ kHz, Ripple in V_{IN})
- Dropout Voltage : Typ. 150 mV
($I_{OUT}=150$ mA, $V_{SET}=1.0$ V, $V_{BIAS}=V_{SET}+1.4$ V)
- Short-Circuit Current Limit: Typ. 110 mA
- Ceramic Capacitors Supported: C_{IN} , C_{BIAS} , C_{OUT}
 C_{OUT} : 2.2 μ F to 100 μ F
- Operation Mode: automatic mode switching
(fast mode, low power mode)
- Output Current: 150 mA
- Discharge Function selectable

Application

- Wearable devices such as smartwatches, smartbands, and health monitoring
- Lithium-ion battery equipment, coin cell battery equipment
- Low-power CPUs, memory, sensor devices, energy harvesting

GENERAL DESCRIPTION

The NR1620 series are a voltage regulator manufactured using a CMOS process with the output current of 150 mA. This device supports the V_{IN} input voltage as low as 0.6 V and the output voltage as low as 0.4 V. This device can be used as a power supply for the core of a microcontroller, various interfaces, etc. In addition, the ultra-low quiescent current of 0.4 μ A makes it suitable to use in systems that require low consumption and long time operation, such as battery-driven systems. NMOS power transistors are driven by a bias power input pin (V_{BIAS}) independent of the power input pin (V_{IN}) to achieve highly efficient regulation.

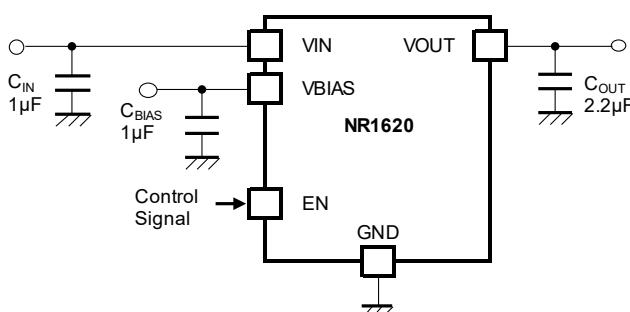


DFN1212-6-GK

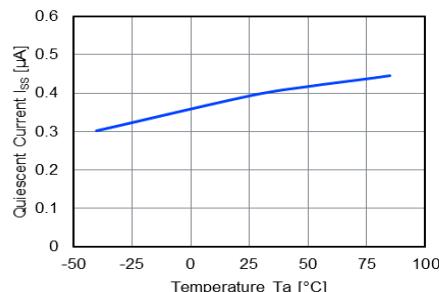
SOT-23-5-DC

1.2 x 1.2 x 0.4 (mm) 2.9 x 2.8 x 1.1 (mm)

TYPICAL APPLICATION CIRCUIT



QUIESCENT CURRENT



$V_{SET} = 0.4$ V, $V_{BIAS} = 5.5$ V, $V_{IN} = V_{SET} + 0.5$ V,
 $I_{OUT} = 0$ mA, $C_{IN} = 1$ μ F, $C_{BIAS} = 1$ μ F, $C_{OUT} = 2.2$ μ F

■ PRODUCT NAME INFORMATION

NR1620 aa bbb c dd e

Description of configuration

composition	Itemn	Description
aa	Package code	GK:DFN1212-6-GK DC:SOT-23-5-DC
bb	Output Voltage	Set Output Voltage (V_{SET}) The ranges from 0.4 V (040) to 1.2 V (120) in 0.1 V steps are lineaped.
c	Version	Indicating whether the discharge function is available. A:available B: not available
dd	Packing	Insert Direction. Refer to the packing specifications.
e	Grade	Indicating the quality grade. S: Consumer

Version

c	auto-discharge function
A	✓
B	-

Grade

e	Applications	Operating Temperature Range	Test Temperature
S	Consumer	-40°C to 85°C	25°C

■ ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	Plating Composition	WEIGHT (mg)	Quantity per Reel (pcs)
NR1620GK bbb c E4S	DFN1212-6-GK	✓	✓	NiPdAu	2	5000
NR1620DC bbb c E1S	SOT-23-5-DC	✓	✓	Sn	14	3000

[Click](#) here for details.

Note: Please contact us if you require a voltage other than the existing fixed-output product.

■ PIN DESCRIPTIONS(NR1620GK)



DFN1212-6-GK Pin Configuration

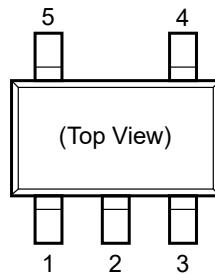
Pin No.	Pin Name	I/O	Description
1	VIN	Power	Power Supply Input Pin Connect the capacitor between the VIN pin and GND.
2	GND	-	Ground Pin
3	EN	I	Enable Pin (Active-High) Input "Low" to this pin shuts down the IC. Input "High" to this pin enables the IC.
4	VBIAS	Power	Bias Supply Input Pin Connect a capacitor between VBIAS pin and GND.
5	NC	-	No Connection Electrically OPEN, but to maintain mounting strength, it is recommended to mount the pins on a board.
6	VOUT	O	Output Pin Connect the output capacitor(C_{out}) between VOUT pin and GND.

*1 The potential of the tab on the backside of the package is the substrate potential.

It is recommended to connect it to the GND.

Please refer to "[TYPICAL APPLICATION CIRCUIT](#)" or "[THEORY OF OPERATION](#)" for details.

■ PIN DESCRIPTIONS (NR1620DC)



SOT-23-5-DC Pin Configuration

Pin No.	Pin Name	I/O	Description
1	VIN	Power	Power Supply Input Pin Connect the input capacitor between the VIN pin and GND.
2	GND	-	Ground Pin
3	VOUT	O	Output Pin Connect the output capacitor (C_{OUT}) between VOUT pin and GND.
4	VBIAS	Power	Bias supply input pin Connect a capacitor between VBIAS pin and GND.
5	EN	I	Enable Pin (Active-high) Input "Low" to this pin shuts down the IC. Input "High" to this pin enables the IC.

Please refer to "[TYPICAL APPLICATION CIRCUIT](#)" or "[THEORY OF OPERATION](#)" for details.

■ ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
Bias Supply Voltage	V_{BIAS}	-0.3 to 6.5	V
Input Voltage	V_{IN}	-0.3 to $V_{BIAS} + 0.3$	V
EN pin input Voltage	V_{EN}	-0.3 to 6.5	V
Output Voltage	V_{OUT}	-0.3 to $V_{IN} + 0.3$	V
Junction Temperature Range ¹	T_j	-40 to 125	°C
Storage Temperature Range	T_{stg}	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

¹ Calculate the power consumption of the IC from the operating conditions and calculate the junction temperature with the thermal resistance. Please refer to "THERMAL CHARACTERISTICS" below for thermal resistance under our measured substrate conditions.

■ THERMAL CHARACTERISTICS

Package	Parameter	Measurement Result	Unit
DFN1212-6-GK	Thermal Resistance (θ_{ja})	117	°C /W
	Thermal Characterization Parameter (ψ_{jt})	50	
SOT-23-5-DC	Thermal Resistance (θ_{ja})	150	°C /W
	Thermal Characterization Parameter (ψ_{jt})	51	

θ_{ja} : Junction-to-Ambient Thermal Resistance

ψ_{jt} : Junction-to-Top Thermal Characterization Parameter

For more information, click [here](#).

■ ELECTROSTATIC DISCHARGE RATINGS

	Conditions	Protection Voltage
HBM	$C = 100 \text{ pF}$, $R = 1.5 \text{ k}\Omega$	$\pm 2000 \text{ V}$
CDM		$\pm 1000 \text{ V}$

ELECTROSTATIC DISCHARGE RATINGS

The electrostatic discharge test is done based on JESD47.

In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Bias Supply Voltage	V_{BIAS}	2.4 to 5.5 ($V_{SET} < 1.0$) $V_{SET} + 1.4$ to 5.5 ($V_{SET} \geq 1.0$)	V
Input Voltage	V_{IN}	0.6 to V_{BIAS}	V
EN Pin Input Voltage	V_{EN}	0 to 5.5	V
Output Current	I_{OUT}	0 to 150	mA
Operating Temperature Range	T_a	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS

$V_{BIAS} = 3.3V$, $V_{IN} = V_{SET} + 0.5V$, $V_{EN} = V_{BIAS}$, $I_{OUT} = 10mA$, $C_{IN} = 1.0\mu F$, $C_{BIAS} = 1.0\mu F$, $C_{OUT} = 2.2\mu F$ unless otherwise specified.
For items without temperature conditions, TYP values are at $T_a = 25^\circ C$ and MIN/MAX values are applied to all the temperature range of $-40^\circ C \leq T_a \leq 85^\circ C$.

NR1620GKbbb/ NR1620DCbbb

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Output Voltage Accuracy	V_{OUT}	$T_a = 25^\circ C$	$0.4V \leq V_{SET} \leq 0.9V$	-9.9	-	+9.9	mV
			$0.9V < V_{SET} \leq 1.2V$	-1.1	-	+1.1	%
		$-40^\circ C \leq T_a \leq 85^\circ C$	$0.4V \leq V_{SET} \leq 0.9V$	-18	-	+18	mV
			$0.9V < V_{SET} \leq 1.2V$	-2	-	+2	%
Fast Mode switch-over Current	I_{OUTH}			-	6	-	mA
Low Power Mode switch-over current	I_{OUTL}			-	0.7	-	mA
Output Voltage Difference between Modes ^{*1}	ΔV_{OUT}	$I_{OUT} = 1\mu A$ (low power mode) to $10mA$ (fast mode)		-26	-	26	mV
Load Regulation ^{*2}	$\Delta V_{OUT}/\Delta I_{OUT}$	$I_{OUT} = 10mA$ to $150mA$	$NR1620GKxxxx$	-4	5	15	mV
			$NR1620DCxxxx$	-4	10	20	
Dropout Voltage ^{*3,4}	V_{DO}	$I_{OUT} = 100mA$, $150mA$		Refer to the PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS			
Quiescent Current ^{*5}	I_Q	$I_{OUT} = 0mA$		-	0.4	0.9	μA
Shutdown Current ^{*5}	I_{SD}	$V_{BIAS} = V_{IN} = 5.5V$, $V_{EN} = 0V$, $T_a = 25^\circ C$		-	4	110	nA
Line Regulation (V_{BIAS})	$\Delta V_{OUT}/\Delta V_{BIAS}$	$V_{BIAS} = V_{SET} + 1.4V$ (Min. $2.4V$) to $5.5V$		-0.2	0.05	0.4	%/V
Line Regulation (V_{IN})	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{IN} = V_{SET} + 0.3V$ to $3.3V$		-0.35	0.05	0.35	%/V
Short Current Limit	I_{SC}	$V_{BIAS} = 5.5V$, $V_{OUT} = 0V$		60	110	160	mA
EN pin High Input Voltage (enable device)	V_{ENH}	$V_{BIAS} = 5.5V$		1.0	-	5.5	V
EN pin Low Input Voltage (disable device)	V_{ENL}	$V_{BIAS} = V_{SET} + 1.4V$ (Min. $2.4V$),		0	-	0.4	V
Discharge FET On-resistance	$R_{ON,DIS}$	$V_{EN} = 0V$, $V_{OUT} = 0.1V$	$NR1620xxxxA$	-	50	-	Ω
VIN Ripple Rejection	RR	$f = 1kHz$		-	90	-	dB
		$f = 100kHz$		-	60	-	dB

All test parameters listed in Electrical Characteristics without VIN Power Supply Ripple Rejection are tested under the condition of $T_j \approx T_a = 25^\circ C$.

^{*1} Output Voltage Difference between Modes is the value calculated with $V_{OUT}(@I_{OUT} = 1\mu A) - V_{OUT}(@I_{OUT} = 10mA)$.

^{*2} Load Regulation is the value calculated with $V_{OUT}(@I_{OUT} = 10mA) - V_{OUT}(@I_{OUT} = 150mA)$.

^{*3} If the output voltage (V_{OUT}) + dropout voltage < $0.6V$, please use the input voltage V_{IN} under the recommended operating conditions ($0.6V$ or higher).

^{*4} Dropout Voltage is specified as the minimum voltage difference between VIN Input Voltage (V_{IN}), required to obtain 95% of set output voltage (V_{SET}) at specified load current, and Output Voltage (V_{OUT}).

^{*5} It is specified as the sum of VIN pin current and VBIAS pin current.

■ PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS

● Output Voltage ($I_{OUT} = 10 \text{ mA}$)

PRODUCT NAME	TYP	$T_a = 25^\circ\text{C}$		$-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$		[Unit: V]
		MIN	MAX	MAX	MAX	
NR1620xx040	0.4	0.390	0.410	0.382	0.418	
NR1620xx050	0.5	0.490	0.510	0.482	0.518	
NR1620xx060	0.6	0.590	0.610	0.582	0.618	
NR1620xx070	0.7	0.690	0.710	0.682	0.718	
NR1620xx075	0.75	0.740	0.760	0.732	0.768	
NR1620xx080	0.8	0.790	0.810	0.782	0.818	
NR1620xx090	0.9	0.890	0.910	0.882	0.918	
NR1620xx100	1.0	0.989	1.011	0.980	1.020	
NR1620xx110	1.1	1.087	1.113	1.078	1.122	
NR1620xx120	1.2	1.186	1.214	1.176	1.224	

All of the above electrical characteristic items are tested under the condition of $T_j \approx T_a = 25^\circ\text{C}$.

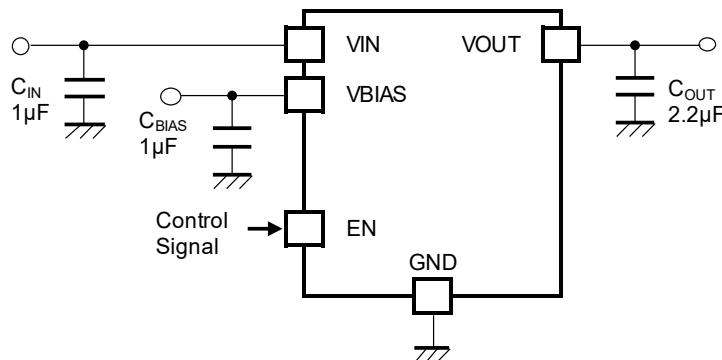
● Dropout Voltage

For this item, the Typ value is for $T_a = 25^\circ\text{C}$ and the MAX value is for temperature conditions of $-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$.

PRODUCT NAME	$I_{OUT}=100 \text{ mA}$		$I_{OUT}=150 \text{ mA}$		[Unit: mV]
	TYP	MAX	TYP	MAX	
NR1620xx040	87	100	131	150	
NR1620xx050	88	102	133	152	
NR1620xx060	90	103	135	155	
NR1620xx070	91	105	137	158	
NR1620xx075	93	107	139	161	
NR1620xx080					
NR1620xx090	95	110	142	164	
NR1620xx100	97	112	145	168	
NR1620xx110	99	114	148	172	
NR1620xx120	101	117	151	176	

All of the above electrical characteristic items are tested under the condition of $T_j \approx T_a = 25^\circ\text{C}$.

■ TYPICAL APPLICATION CIRCUIT



NR1620 TYPICAL APPLICATION CIRCUIT

● EXTERNAL COMPONENTS INFORMATION

Input Capacitor (C_{IN}, C_{BIAS})

Connect an input capacitor (C_{BIAS}) of 1 μF or more between the VBIAS pin and the GND pin at the shortest distance. Also, connect an input capacitor (C_{IN}) of 1 μF or more between the VIN pin and the GND pin at the shortest distance.

It is recommended to use a ceramic capacitor of 6.3 V or more such as X5R or X7R having small temperature dependence to ESR, ESL, and capacitance.

Output Capacitor(C_{OUT})

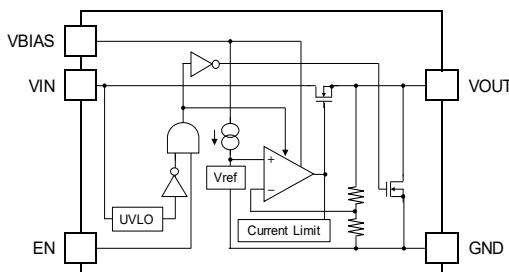
Phase compensation is provided to secure stable operation even when the load current is varied.

Connect a capacitor(C_{OUT}) of 2.2 μF or more but less than 100μF between the VOUT pin and the GND pin closely.

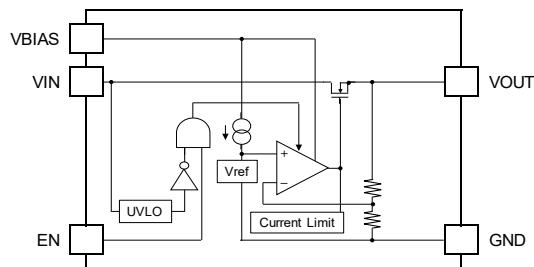
We recommend to use ceramic capacitors with very low ESR and ESL and good temperature characteristics such as X5R or X7R type. Besides, set for the output capacitor to ensure the following effective capacitance in consideration of the dependence of temperature, DC bias, and package size.

Set Output Voltage (V _{SET})	Effective Capacitance
0.4 V ≤ V _{SET} ≤ 1.2 V	1.5 μF min. 100 μF max.

■ BLOCK DIAGRAMS



NR1620xxxxxA Block Diagram



NR1620xxxxxB Block Diagram

■ THEORY OF OPERATION

● Enable Function

Forcing above designated "High" voltage to EN pin, the NR1620 becomes active. Forcing below designated "Low" voltage to EN pin shuts down the NR1620.

Products with a discharge function (NR1620xxxxA) turn on the discharge FET in the shutdown state to discharge the output capacitor (C_{out}). Products without a discharge function (NR1620xxxxB) discharge the charge of the output capacitor (C_{out}) in the load circuit in the shutdown state.

When the EN pin is OPEN, the NR1620 is in an undefined state because it is not pulled up or down internally. If control by the EN pin is not possible or is not required, connect the EN pin to the VBIAS pin, etc., so that "High" is input at start-up.

In case of the EN pin is connected to the VBIAS pin, the built-in FET for discharge is not expected to work properly.

Even if voltage is applied to the EN pin before the VBIAS and VIN pins, it will not result in IC failure.

● Discharge Function (NR1620xxxxA)

This function turns on the FET connected between the VOUT pin and GND pin to discharge the charge stored in the output capacitor (C_{out}) and quickly reduce the output voltage to near 0 V. This function is enabled when the EN pin is "Low".

The FET on-resistance is Typ. 50Ω ($V_{BIAS} = 3.3\text{ V}$, $V_{IN} = V_{SET} + 0.5\text{ V}$, $V_{OUT} = 0.1\text{ V}$).

This function is effective when the Bias supply voltage (V_{BIAS}) is within the recommended operating conditions.

Please note that when the EN input voltage and the VBIAS Input voltage (V_{BIAS}) are used in common, the C_{out} charge cannot be discharged sufficiently when the VBIAS Input voltage (V_{BIAS}) drops.

● Under Voltage Lockout Circuit(UVLO)

The UVLO function is an auxiliary function that stops the operation of the IC, when the input voltage (V_{IN}) is low (typ:under 0.35 V) and the IC cannot operate normally. In versions with a discharge function, the output pin is pulled down by the discharge FET when this function works. To restart the operation, the input voltage (V_{IN}) must be higher than 0.5V.

This function is effective when the bias input voltage (VBIAS) is within the recommended operating condition.

● Current limit function at startup

This function limits the inrush current at startup (I_{RUSH}), which is the sum of the charge current (I_{CHG}) to the output capacitor (C_{out}) and the load current (I_{LOAD}), by the startup current limit ($I_{LIMRISE}$, Typ. 75 mA). The inrush current at startup (I_{RUSH}) is defined by the following formula.

$$I_{RUSH} = I_{CHG} + I_{LOAD}$$

I_{CHG} : Charge current to output capacitors.

I_{LOAD} : Load current

With an output capacitor (C_{out} , more than $75\text{ }\mu\text{F}/V_{SET}$) and load current (I_{LOAD}) such that this inrush current value at startup (I_{RUSH}) reaches the startup current limit ($I_{LIMRISE}$, Typ. 75 mA), the output voltage rises at a slope determined by the output current limit at startup ($I_{LIMRISE}$). The rise time (t_{0N}) due to the inrush current limiting function can be determined by the following formula.

$$t_{0N} = t_{01} + C_{out} \times V_{SET} / I_{LIMRISE}$$

t_{01} : Delay Time at Start-up Typ. $880\text{ }\mu\text{s}$

C_{out} : Effective capacitance value of output capacitor

V_{SET} : Set Output Voltage $I_{LIMRISE}$: Current Limit at Start-up Typ. 75 mA

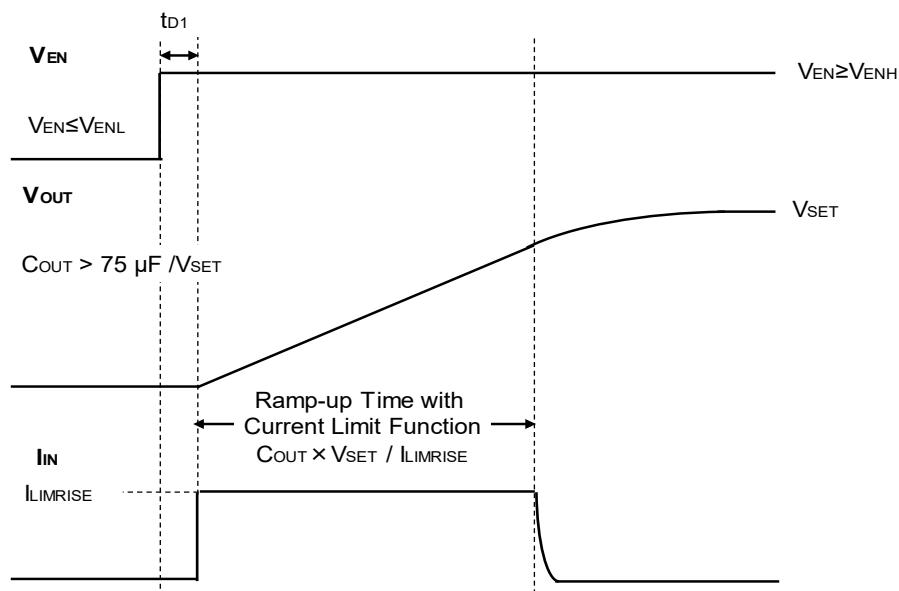
The start-up current limit ($I_{LIMRISE}$) is in effect until 4.2 ms (typ.) after EN start-up.

After that, the output current limit (I_{LM} , Typ. 240 mA) and the short-circuit current (I_{SC} , Typ. 110 mA) protect against overcurrent.

To enable the inrush current limit function, apply the recommended operating conditions ($V_{SET} + 1.4V$, Min. 2.4V or more) as the bias input voltage (V_{BIAS}) and then input "High" to the EN pin to activate it.

If "High" is input to the EN pin while the bias input voltage (V_{BIAS}) does not match the recommended operating conditions, the NR1620 may start up without the inrush current limit function enabled.

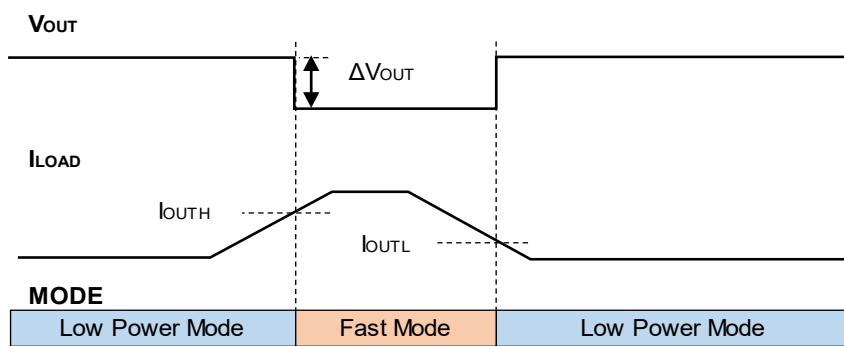
If the load current (I_{LOAD}) exceeds the start-up current limit ($I_{LIMRISE}$) during start-up, the output voltage (V_{OUT}) will not reach the set output voltage (V_{SET}). The UVLO function is active during output voltage start-up. This protection function may work when the IC starts up with load current or when a large output capacitor (C_{OUT}) is connected. In such cases, adjust the output capacitor (C_{OUT}) or startup timing to reduce the inrush current.



● Automatic Mode Switching Function

The automatic mode switching feature can improve battery life, especially in battery-powered applications with long-cycle intermittent operation. NR1620 has two modes: fast mode and low power mode. Fast mode is a mode with high current consumption for fast transient response. Low power mode achieves lower current consumption, although in this mode transient response becomes slower compared to the Fast mode.

When the load current (I_{LOAD}) exceeds the fast mode switching current (I_{OUTH}), it switches to fast mode, and when it falls below the low power mode switching current (I_{OUTL}), it switches to low power mode. Switching currents (I_{OUTH} , I_{OUTL}) have hysteresis and they will never be equal. Output voltage may have difference between fast mode and low power mode. For details, refer to "Output Voltage Difference between Modes" in the Electrical Characteristics.



■ THERMAL CHARACTERISTICS (DFN1212-6-GK)

Thermal characteristics depend on mounting conditions. The thermal characteristics below are the results of measurements under conditions determined by our company with reference to JEDEC STD. (JESD51).

Measurement Result

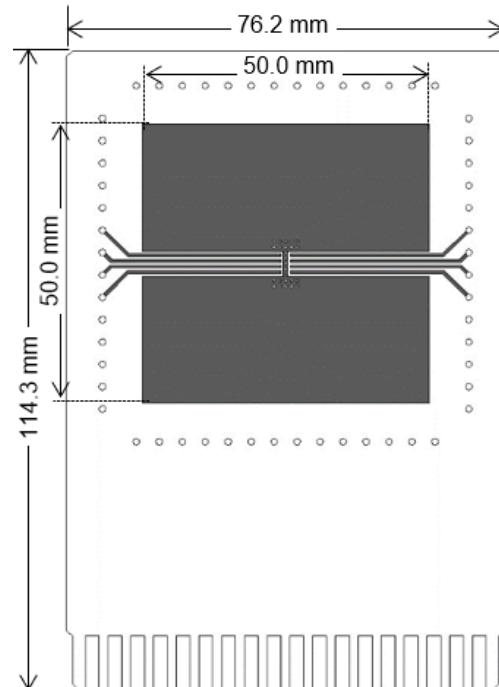
Item	Measurement Result
Thermal Resistance (θ_{ja})	117°C/W
Thermal Characterization Parameter (ψ_{jt})	50°C/W

θ_{ja} : Junction-to-Ambient Thermal Resistance

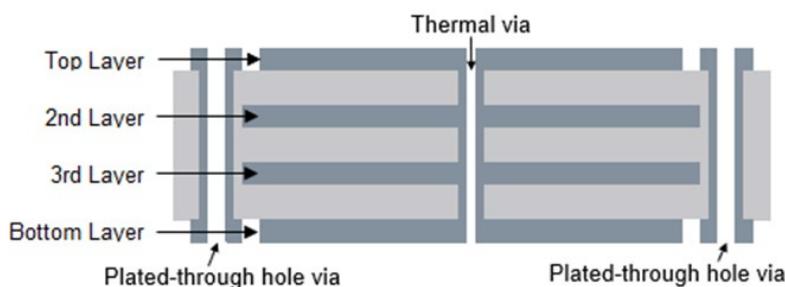
ψ_{jt} : Junction-to-Top Thermal Characterization Parameter

Measurement Conditions

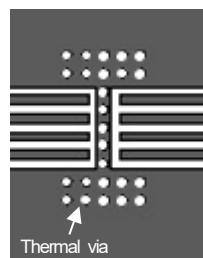
Item	Specification
Measurement Condition	Mounting on Board (Still Air)
Board material	FR-4
Board size	76.2 mm × 114.3 mm × t 0.8 mm
Copper foil layer	1 50 mm × 50 mm (coverage rate 95%), t 0.075 mm
	2 50 mm × 50 mm (coverage rate 100%), t 0.035 mm
	3 50 mm × 50 mm (coverage rate 100%), t 0.035 mm
	4 50 mm × 50 mm (coverage rate 100%), t 0.075 mm
Thermal vias	φ 0.2 mm × 25 pcs



Measurement Board Pattern



Cross section view of layers and vias



Enlarged view of IC mounting area

● CALCULATION METHOD OF JUNCTION TEMPERATURE

The junction temperature (T_j) can be calculated from the following formula.

$$T_j = T_a + \theta_{ja} \times P$$

$$T_j = T_c(\text{top}) + \psi_{jt} \times P$$

Where:

T_a : Ambient temperature

$T_c(\text{top})$: Package mark side center temperature

$P = (V_{IN} - V_{OUT}) \times I_{out}$: Power consumption under user's conditions

■ THERMAL CHARACTERISTICS (SOT-23-5-DC)

Thermal characteristics depend on mounting conditions. The thermal characteristics below are the results of measurements under conditions determined by our company with reference to JEDEC STD. (JESD51).

Measurement Result

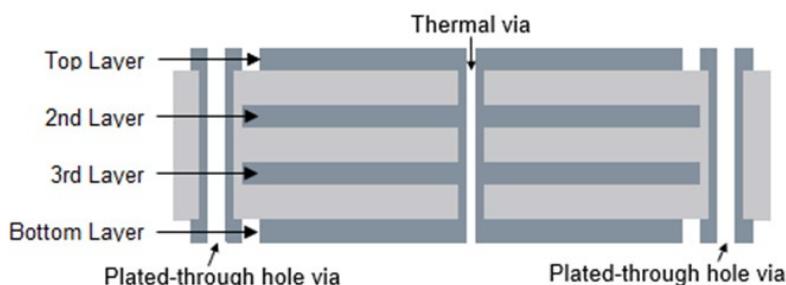
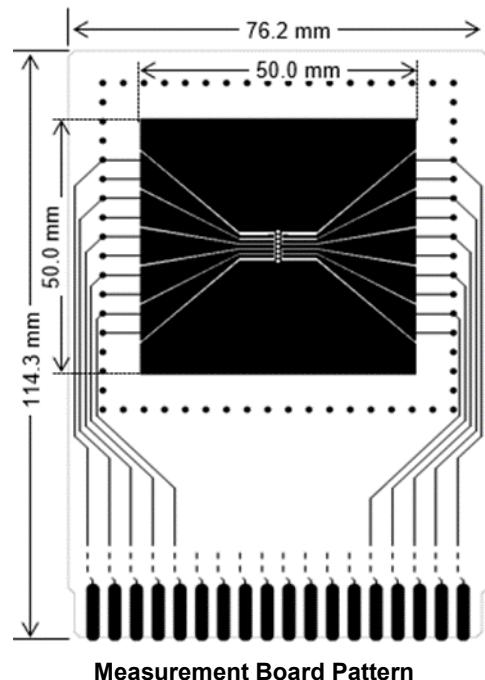
Item	Measurement Result
Thermal Resistance (θ_{ja})	150°C/W
Thermal Characterization Parameter (ψ_{jt})	51°C/W

θ_{ja} : Junction-to-Ambient Thermal Resistance

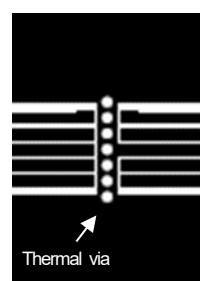
ψ_{jt} : Junction-to-Top Thermal Characterization Parameter

Measurement Conditions

Item	Specification
Measurement Condition	Mounting on Board (Still Air)
Board material	FR-4
Board size	76.2 mm × 114.3 mm × t 0.8 mm
Copper foil layer	1 50 mm × 50 mm (coverage rate 95%), t 0.040 mm
	2 50 mm × 50 mm (coverage rate 100%), t 0.035 mm
	3 50 mm × 50 mm (coverage rate 100%), t 0.035 mm
	4 50 mm × 50 mm (coverage rate 95%), t 0.040 mm
Thermal vias	φ 0.3 mm × 7 pcs



Cross section view of layers and vias



Enlarged view of IC mounting area

● CALCULATION METHOD OF JUNCTION TEMPERATURE

The junction temperature (T_j) can be calculated from the following formula.

$$T_j = T_a + \theta_{ja} \times P$$

$$T_j = T_c(\text{top}) + \psi_{jt} \times P$$

Where:

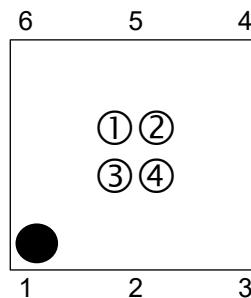
T_a : Ambient temperature

$T_c(\text{top})$: Package mark side center temperature

$P = (V_{IN} - V_{OUT}) \times I_{OUT}$: Power consumption under user's conditions

■ MARKING SPECIFICATION (DFN1212-6-GK)

①② : Product Code (Abbreviation)
③④ : Lot Number ... Alphanumeric Serial Number



DFN1212-6-GK Marking

NOTICE

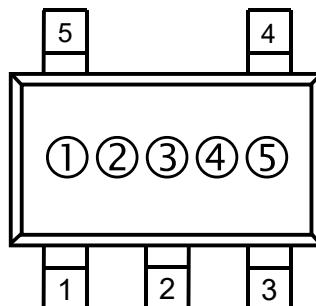
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

Marking List

Product Code	①②	Product Code	①②
NR1620GK040A	10	NR1620GK040B	20
NR1620GK050A	11	NR1620GK050B	21
NR1620GK060A	12	NR1620GK060B	22
NR1620GK070A	13	NR1620GK070B	23
NR1620GK075A	14	NR1620GK075B	24
NR1620GK080A	15	NR1620GK080B	25
NR1620GK090A	16	NR1620GK090B	26
NR1620GK100A	17	NR1620GK100B	27
NR1620GK110A	18	NR1620GK110B	28
NR1620GK120A	19	NR1620GK120B	29

■ MARKING SPECIFICATION (SOT-23-5-DC)

①②③ : Product Code (Abbreviation)
④⑤ : Lot Number ... Alphanumeric Serial Number



SOT-23-5-DC Marking

NOTICE

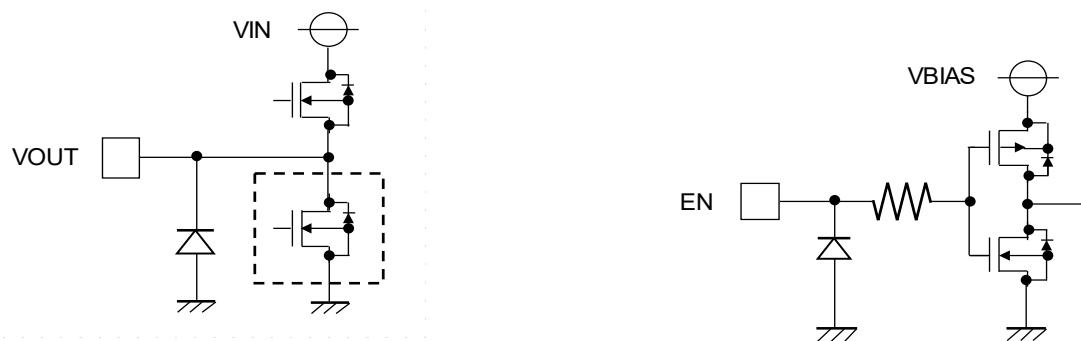
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

Marking List

Product Code	①②③	Product Code	①②③
NR1620DC040A	5A0	NR1620DC040B	5B0
NR1620DC050A	5A1	NR1620DC050B	5B1
NR1620DC060A	5A2	NR1620DC060B	5B2
NR1620DC070A	5A3	NR1620DC070B	5B3
NR1620DC075A	5A4	NR1620DC075B	5B4
NR1620DC080A	5A5	NR1620DC080B	5B5
NR1620DC090A	5A6	NR1620DC090B	5B6
NR1620DC100A	5A7	NR1620DC100B	5B7
NR1620DC110A	5A8	NR1620DC110B	5B8
NR1620DC120A	5A9	NR1620DC120B	5B9

■ Application Note

● Internal Equivalent Circuit Diagram of Pin

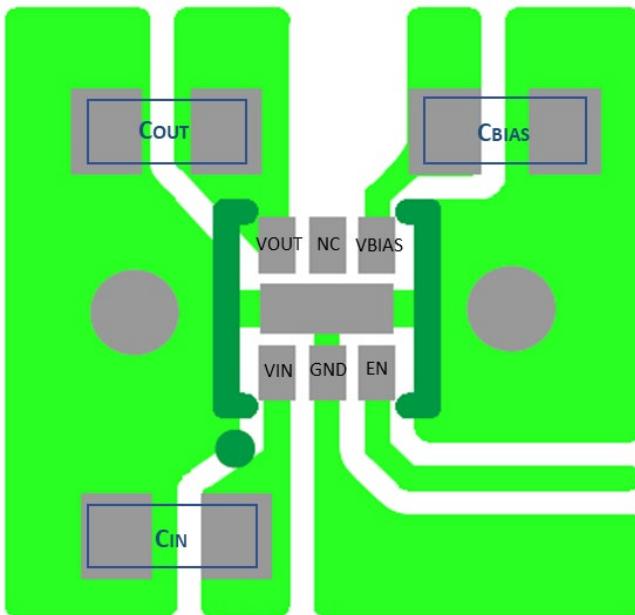


*Dotted frame corresponds to (NR1620xxxxA)

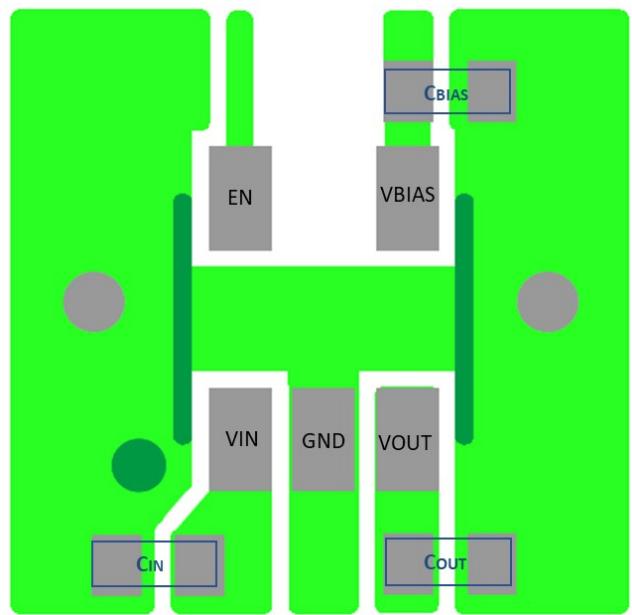
VOUT Pin

EN Pin

● Evaluation Board / PCB Layout Pattern Example



NR1620GK



NR1620DC

● TECHNICAL NOTES

Constraints of the voltage value and the sequence of V_{BIAS} and V_{IN}

The voltage regulating operation is guaranteed under the condition that V_{IN} Input voltage (V_{IN}) is equal or below to V_{BIAS} Input voltage (V_{BIAS}). Therefore, during voltage regulating operation, please set the applying voltage for each pin so that $V_{IN} \leq V_{BIAS}$.

During startup, if V_{BIAS} is applied after applying V_{IN} and V_{EN} , ensure that $V_{IN} \leq V_{BIAS}$ within 300 μ s after applying V_{BIAS} .

There are no constraints on the shutdown sequence.

EN pin input voltage setting

Please set the applying voltage for EN pin below to V_{ENL} or up to V_{ENH} . However, please note that V_{BIAS} current consumption will slightly increase in the range of $V_{ENH} \leq V_{EN} \leq V_{BIAS} - 1$ V. (Typ: 60 nA)

■ TYPICAL CHARACTERISTICS

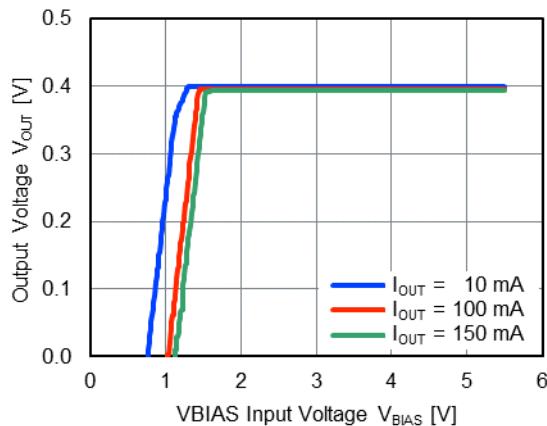
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

$T_a = 25^\circ C$, $C_{IN} = 1 \mu F$, $C_{BIAS} = 1 \mu F$, $C_{OUT} = 2.2 \mu F$ unless otherwise noted.

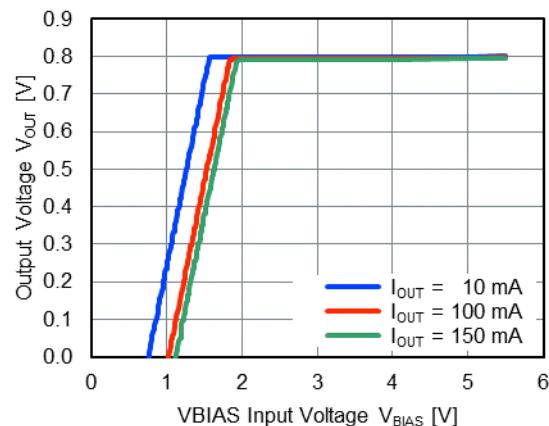
1) Output Voltage vs VBIAS Input Voltage

V_{BIAS} = 5.5 V to 0 V, $V_{IN} = V_{SET} + 0.5$ V

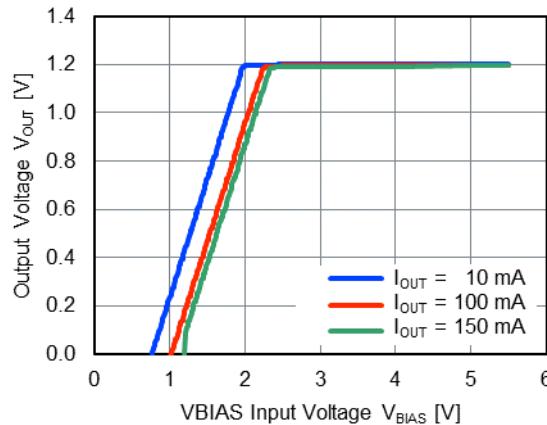
NR1620xx040x



NR1620xx080x



NR1620xx120x

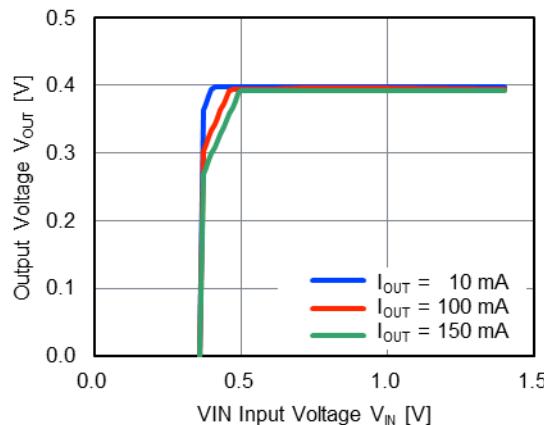


2) Output Voltage vs VIN Input Voltage

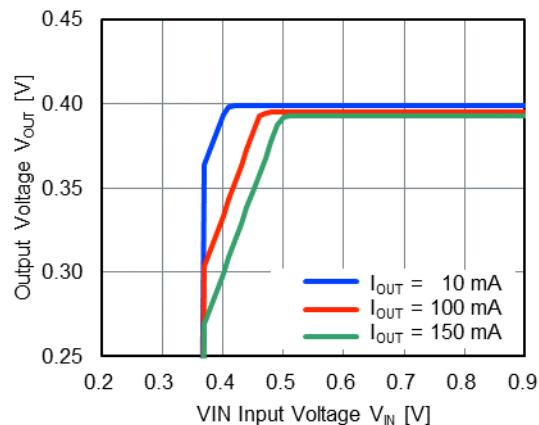
 $V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = V_{SET} + 1 \text{ V}$ to 0 V

NR1620xx040x

Overall View

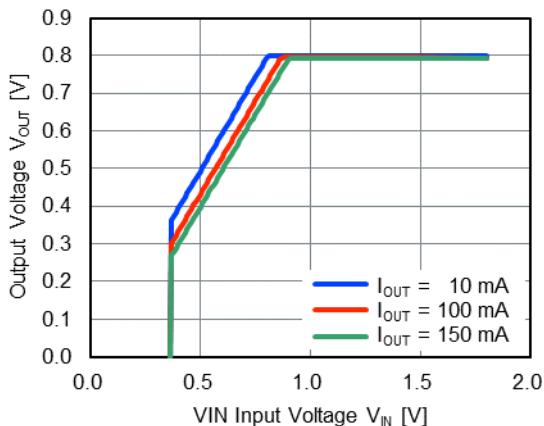


Enlarged View

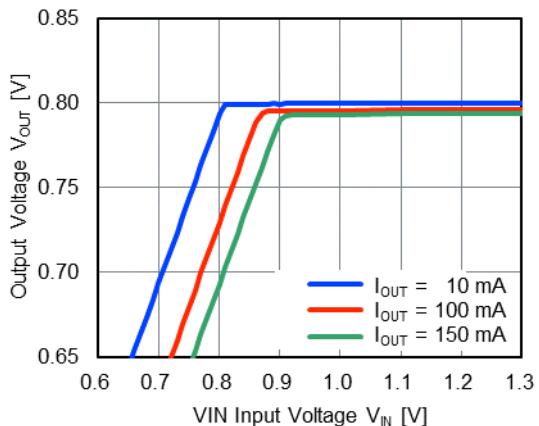


NR1620xx080x

Overall View

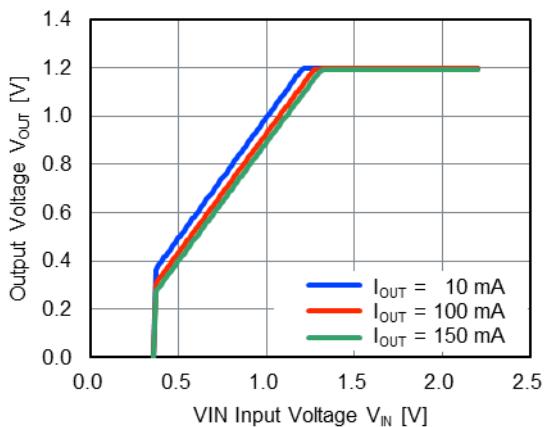


Enlarged View

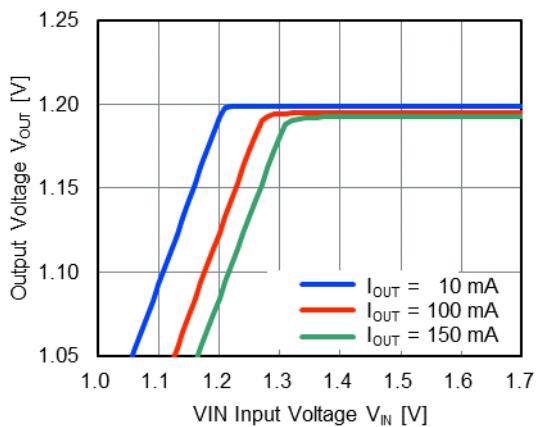


NR1620xx120x

Overall View



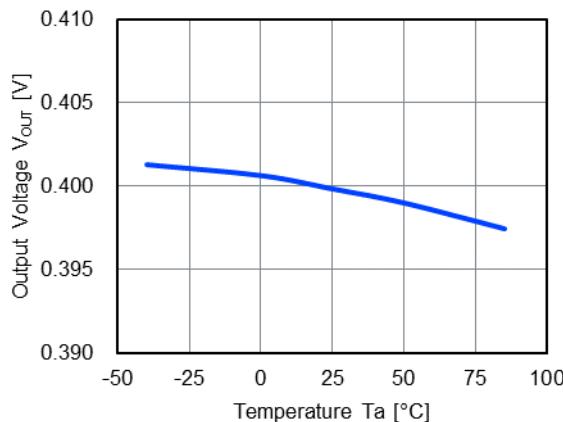
Enlarged View



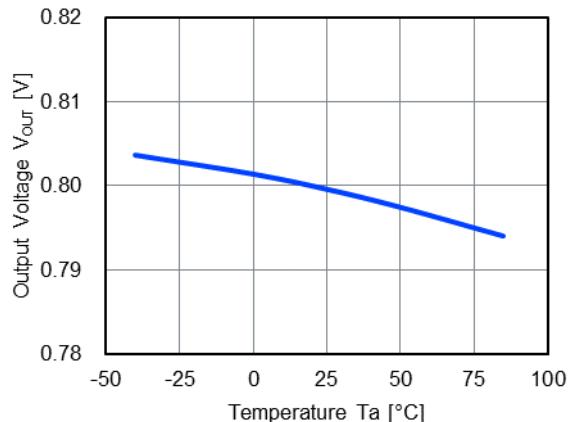
3) Output Voltage vs Temperature

 $V_{IN} = V_{SET} + 0.5 \text{ V}$, $V_{BIAS} = 3.3 \text{ V}$, $I_{OUT} = 10 \text{ mA}$

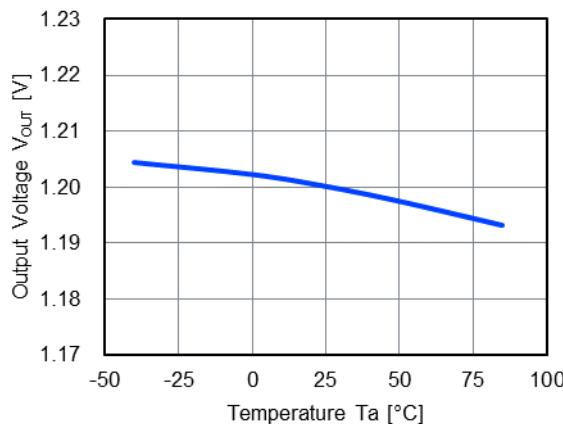
NR1620xx040x



NR1620xx080x



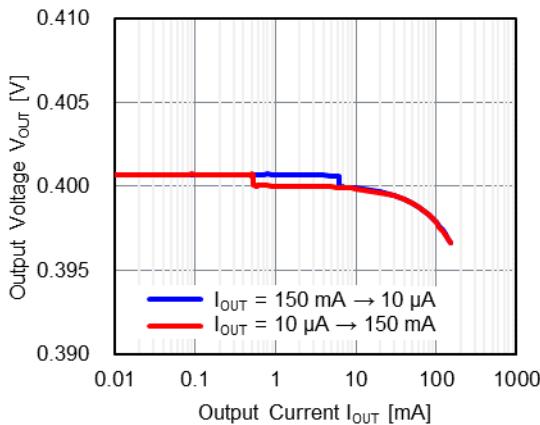
NR1620xx120x



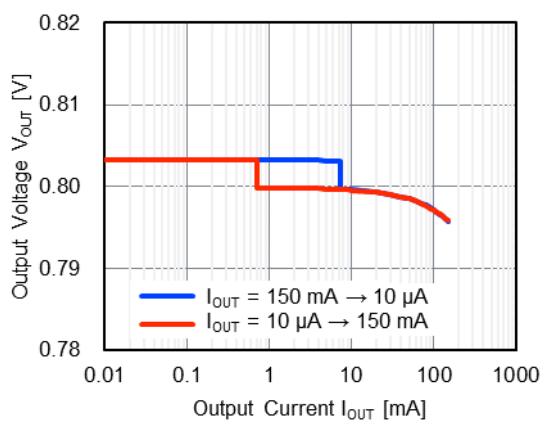
4) Output Voltage vs Output Current (Load Regulation)

 $V_{IN} = V_{SET} + 0.5 \text{ V}$, $V_{BIAS} = 3.3 \text{ V}$

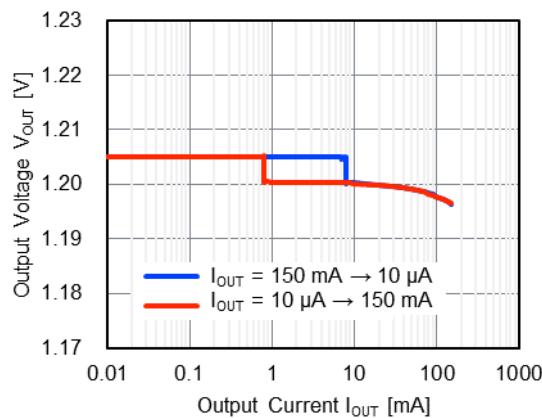
NR1620xx040x



NR1620xx080x



NR1620xx120x

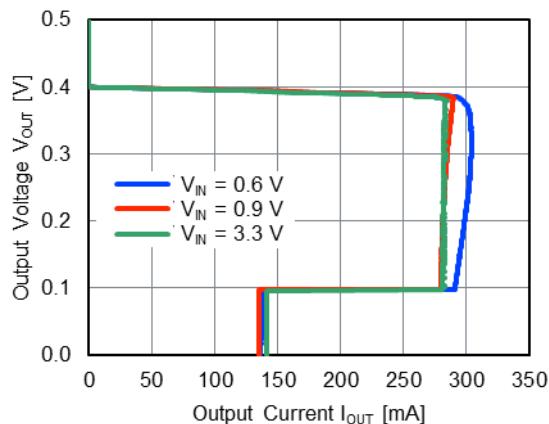
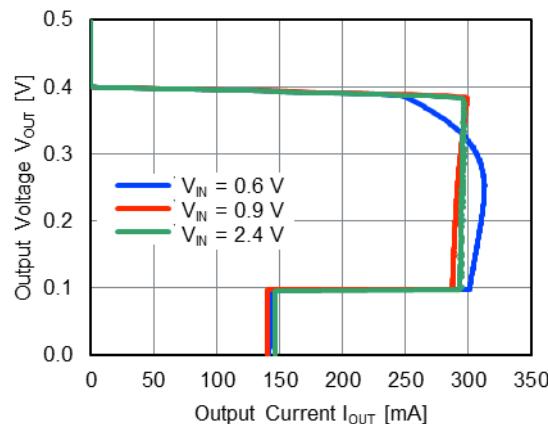


5) Output Voltage vs Output Current (Current Limit)

NR1620xx040x

$V_{BIAS} = 2.4 \text{ V}$

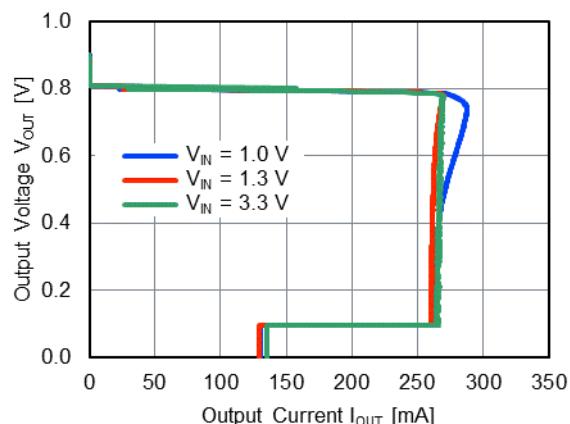
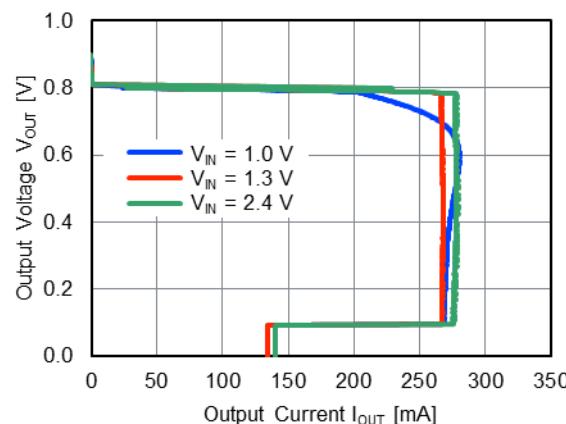
$V_{BIAS} = 3.3 \text{ V}$



NR1620xx080x

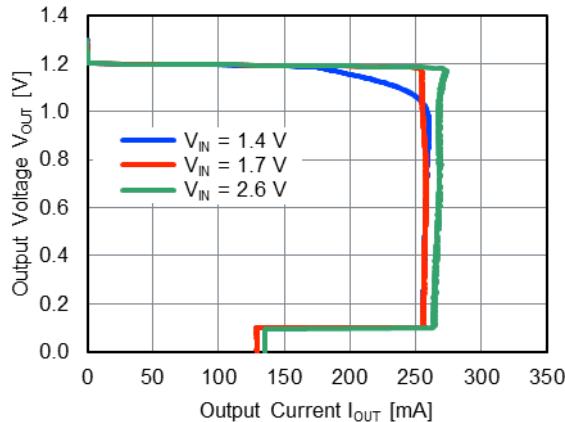
$V_{BIAS} = 2.4 \text{ V}$

$V_{BIAS} = 3.3 \text{ V}$

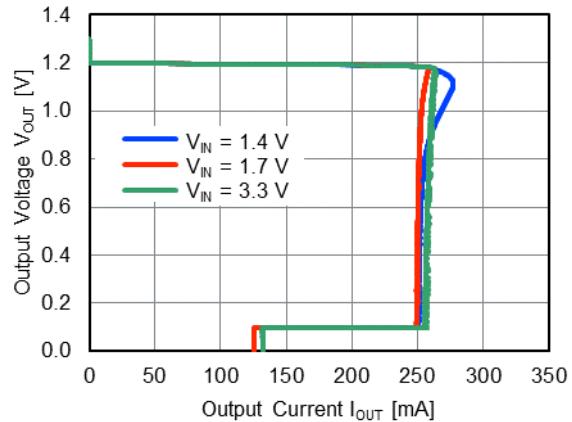


NR1620xx120x

$V_{BIAS} = 2.6 \text{ V}$



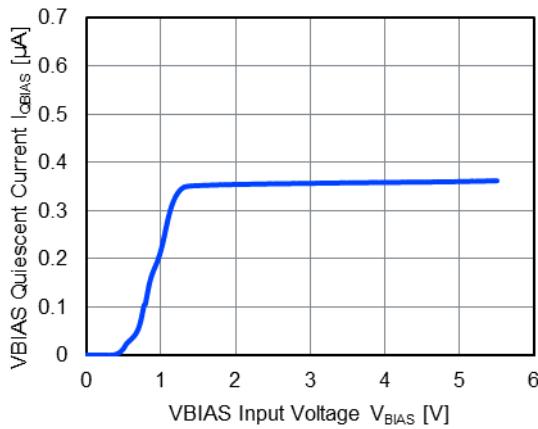
$V_{BIAS} = 3.3 \text{ V}$



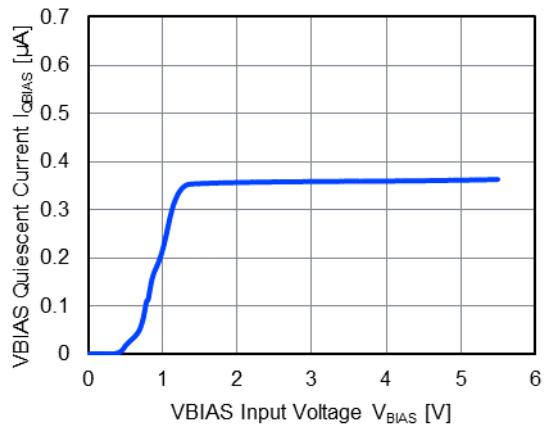
6) VBIAS Quiescent Current vs VBIAS Input Voltage

V_{BIAS} = 5.5 V to 0 V, $V_{IN} = V_{SET} + 0.5 \text{ V}$, C_{BIAS} = none

NR1620xx040x

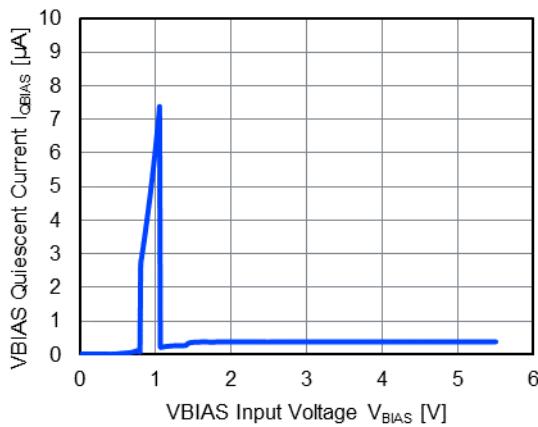


NR1620xx080x

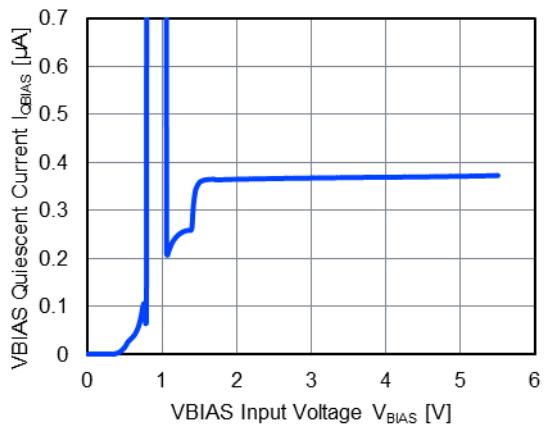


NR1620xx120x

Overall View



Enlarged View

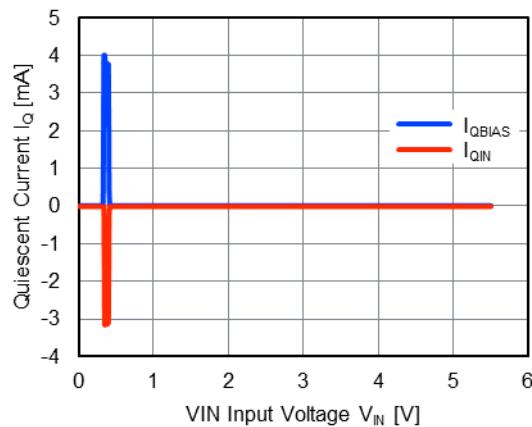


7) VBIAS/VIN Quiescent Current vs VIN Input Voltage

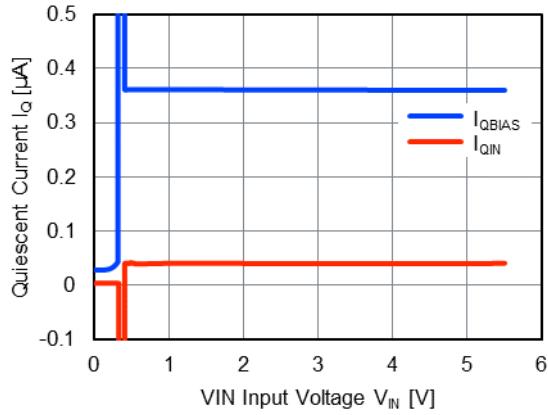
 $V_{BIAS} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$ to 0 V , $C_{BIAS} = \text{none}$

NR1620xx040x

Overall View

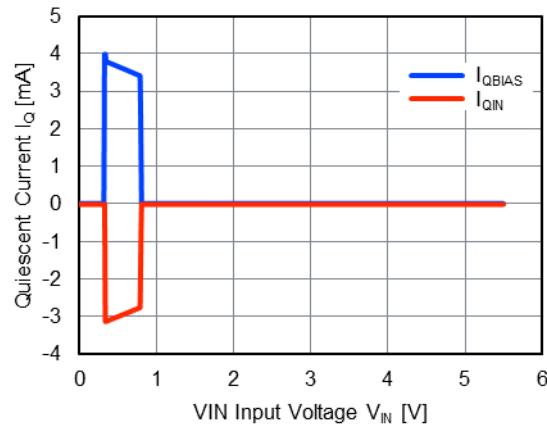


Enlarged View

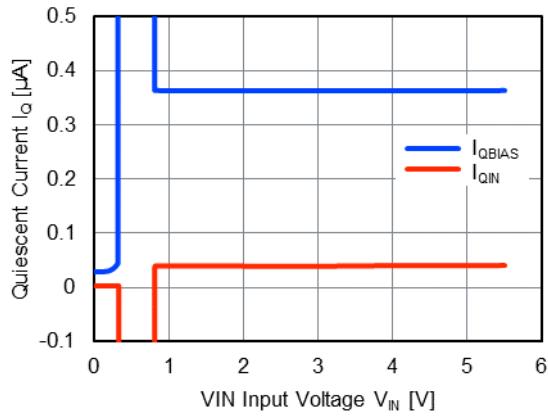


NR1620xx080x

Overall View

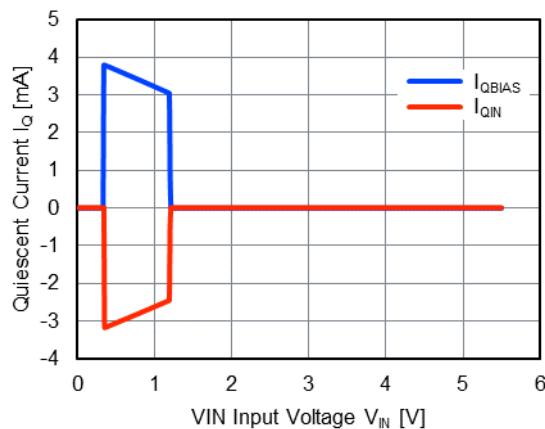


Enlarged View

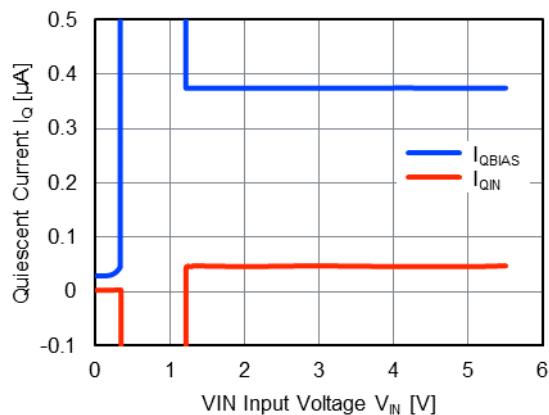


NR1620xx120x

Overall View



Enlarged View

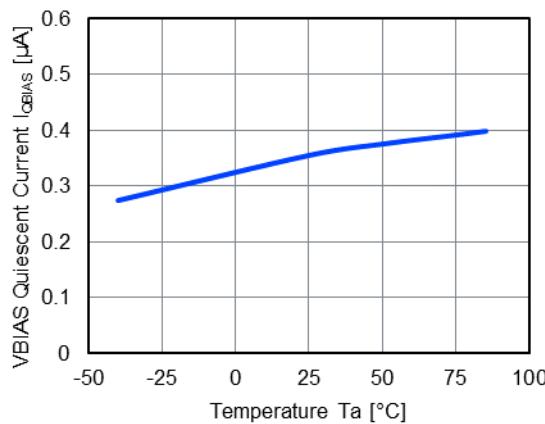


*Please note that if the input voltage V_{IN} drops below the output setting voltage V_{SET} , current will flow from the V_{BIAS} pin to the V_{IN} pin via the inside of the IC. (However, it will not flow under conditions where V_{BIAS} also decreases at the same time as V_{IN})

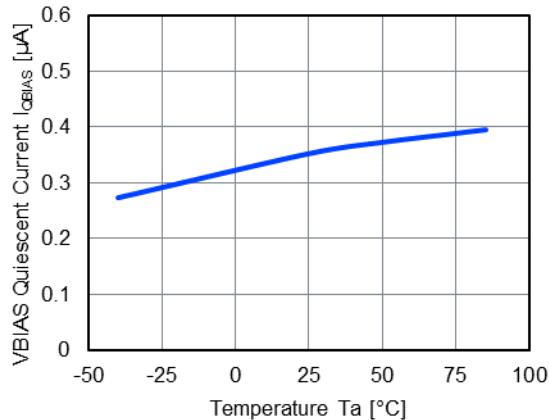
8) VBIAS Quiescent Current vs Temperature

$$V_{BIAS} = 5.5 \text{ V}, V_{IN} = V_{SET} + 0.5 \text{ V}$$

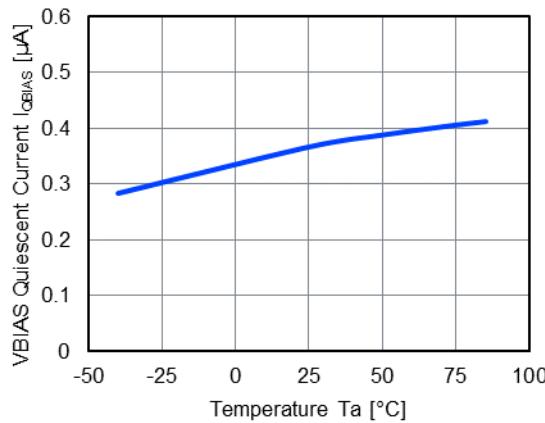
NR1620xx040x



NR1620xx080x



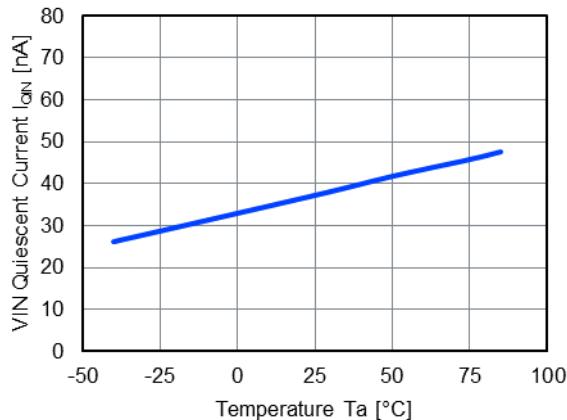
NR1620xx120x



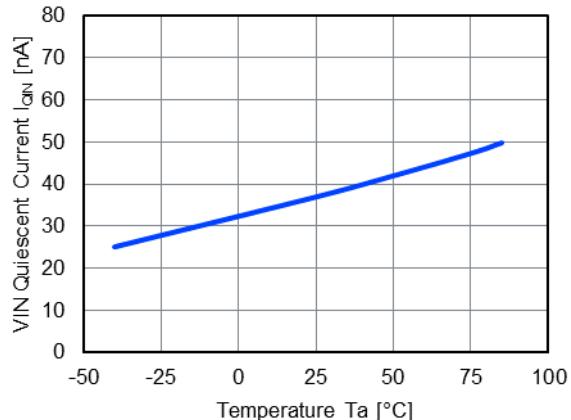
9) VIN Quiescent Current vs Temperature

 $V_{BIAS} = 5.5 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$

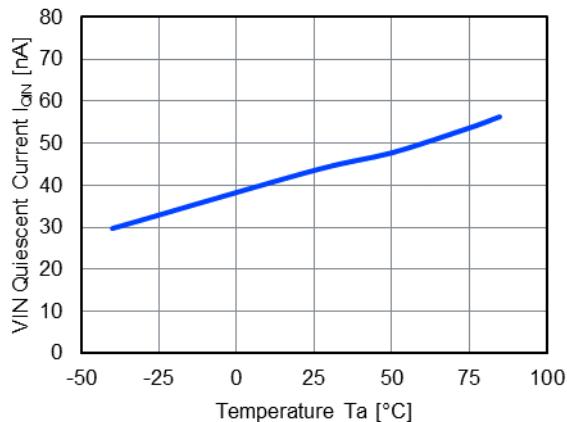
NR1620xx040x



NR1620xx080x



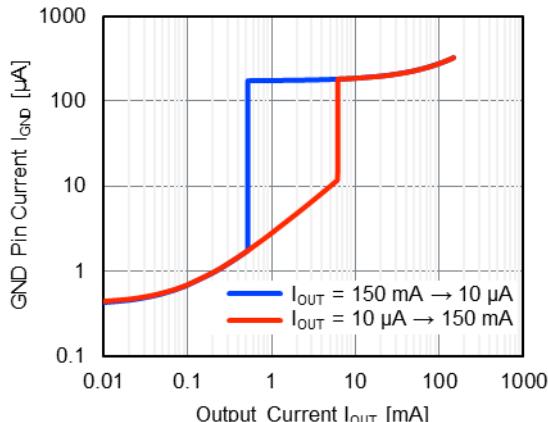
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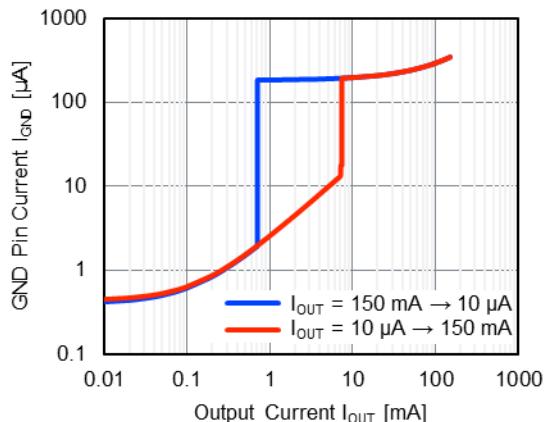
10) GND Pin Current vs Output Current

 $V_{BIAS} = 5.5 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$

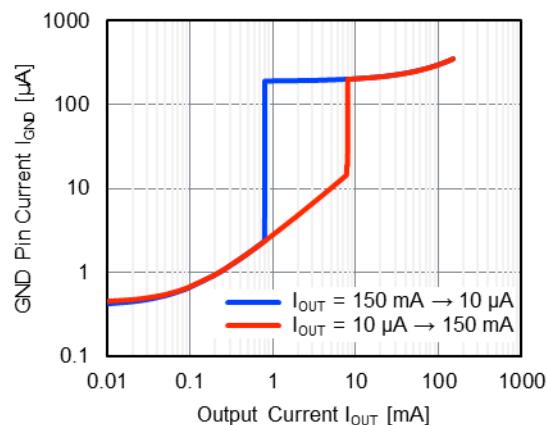
NR1620xx040x



NR1620xx080x



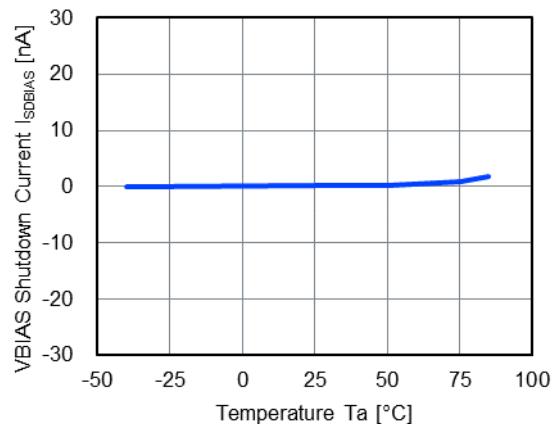
NR1620xx120x



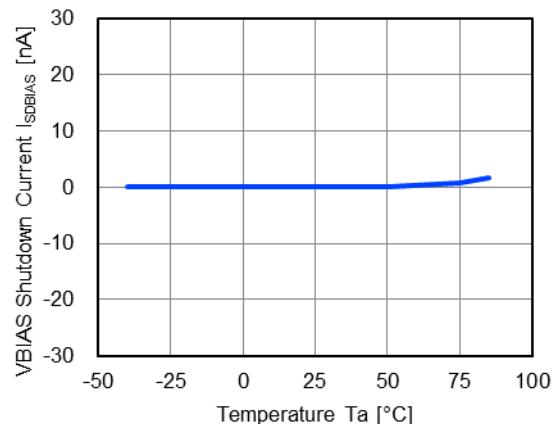
11) VBIAS Shutdown Current vs Temperature

 $V_{BIAS} = 5.5 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$

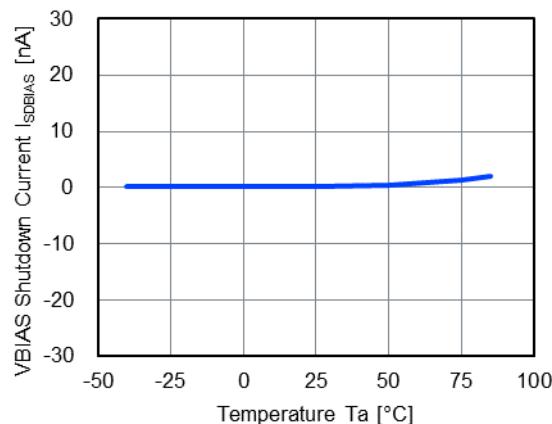
NR1620xx040x



NR1620xx080x



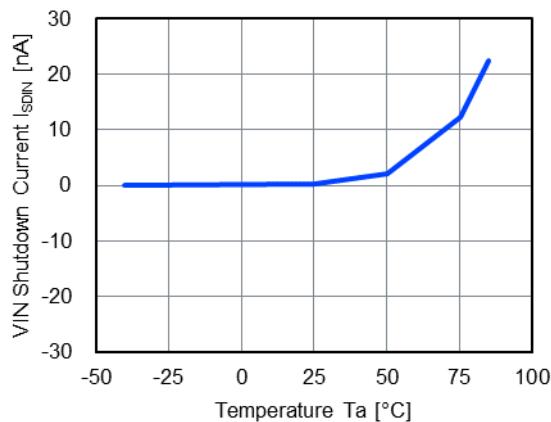
NR1620xx120x



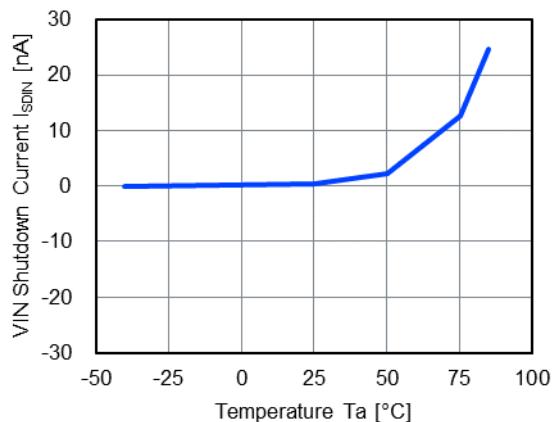
12) VIN Shutdown Current vs Temperature

$V_{BIAS} = 5.5 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$

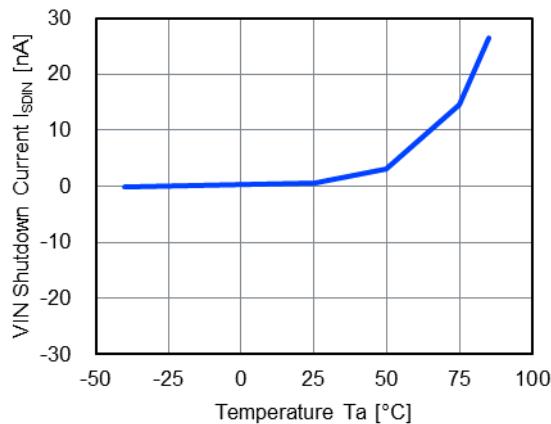
NR1620xx040x



NR1620xx080x

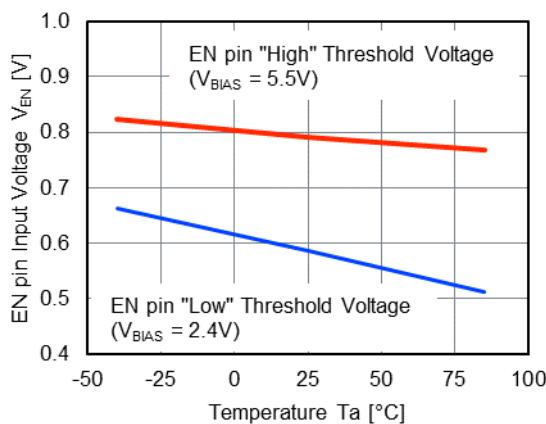


NR1620xx120x



13) EN Pin Input "High / Low" Voltages vs Temperature

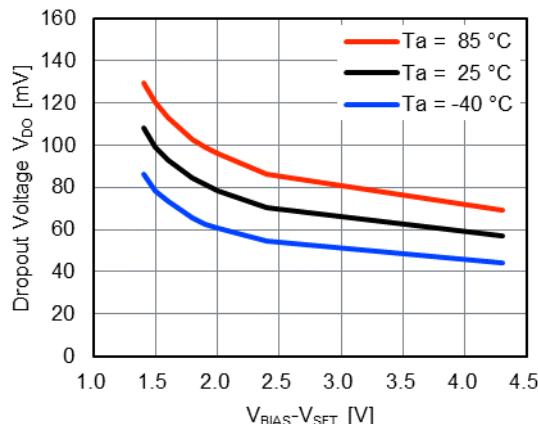
NR1620xxxxx



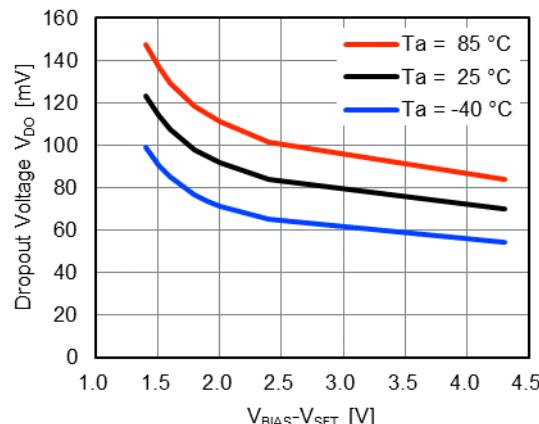
14) Dropout Voltage vs Gate Drive Voltage

V_{IN} = Sweep, I_{OUT} = 100 mA

NR1620GK120x

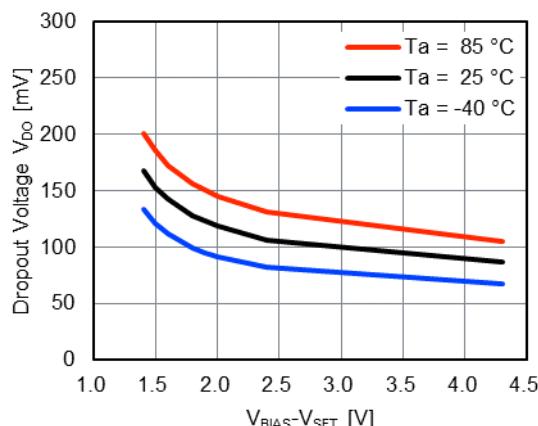


NR1620DC120x

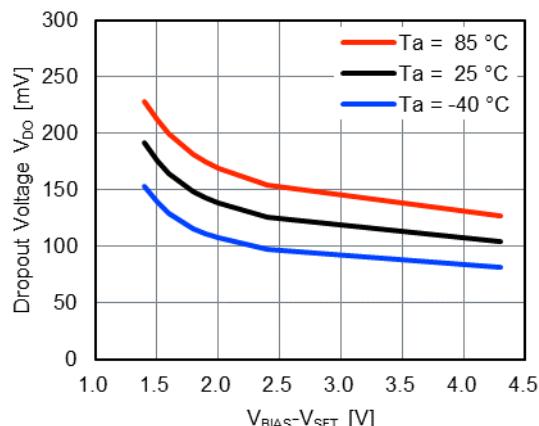


I_{OUT} = 150 mA

NR1620GK120x



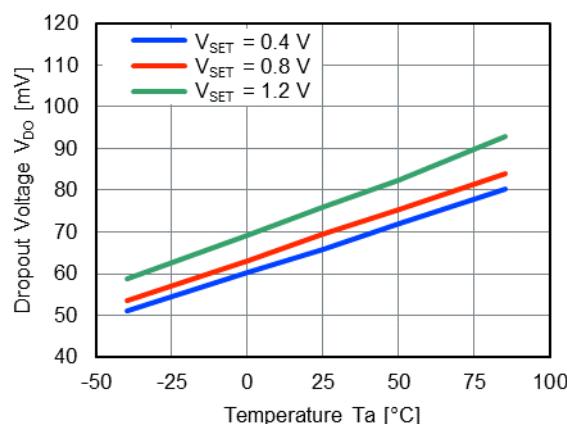
NR1620DC120x



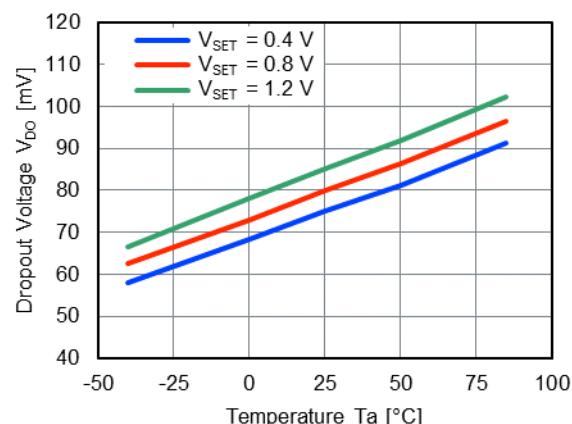
15) Dropout Voltage vs Temperature

V_{BIAS} = 3.3 V, V_{IN} = Sweep, I_{OUT} = 100 mA

NR1620GK120x

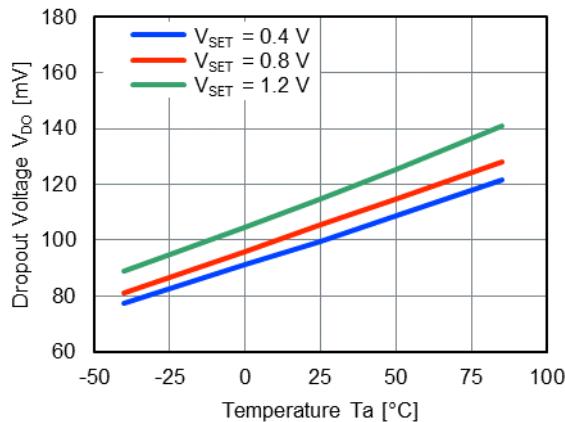


NR1620DC120x

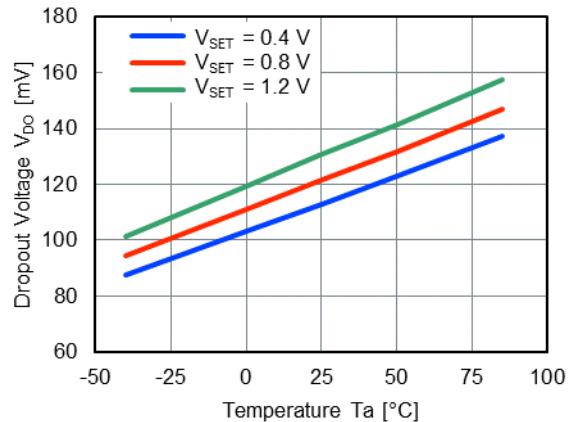


$I_{OUT} = 150 \text{ mA}$

NR1620GK120x



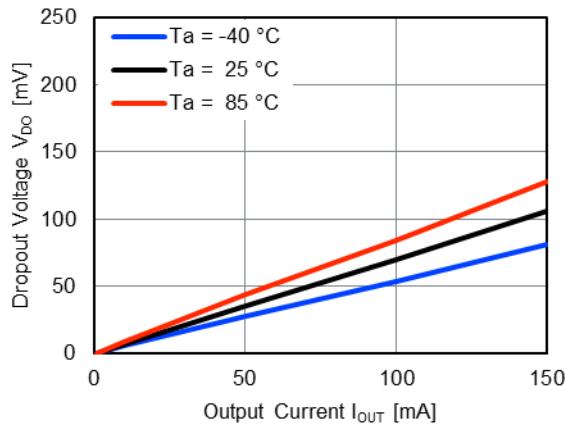
NR1620DC120x



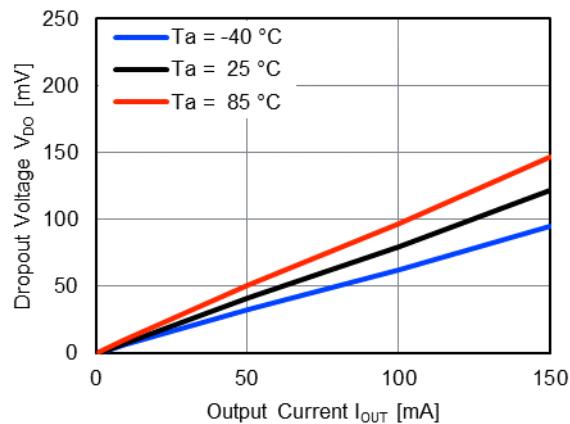
16) Dropout Voltage vs Output Current

$V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = \text{Sweep}$

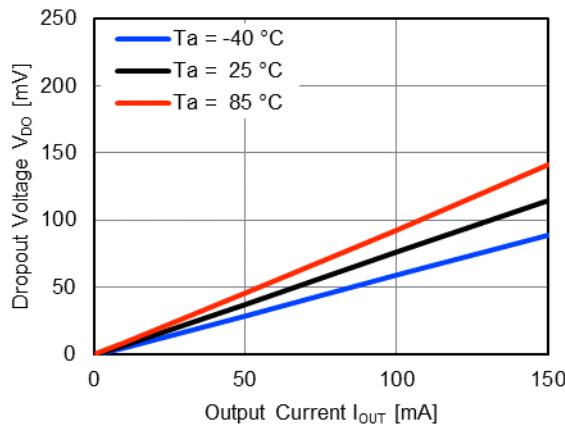
NR1620GK080x



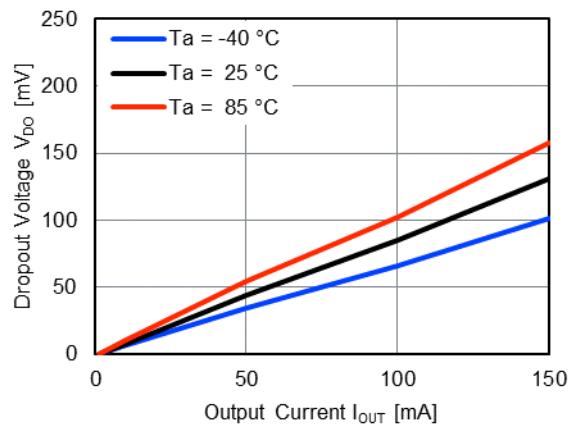
NR1620DC080x



NR1620GK120x



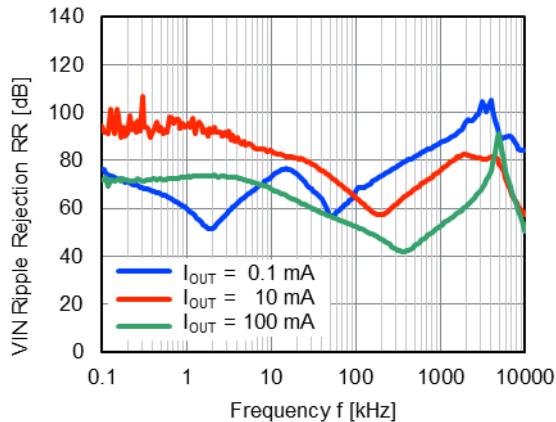
NR1620DC120x



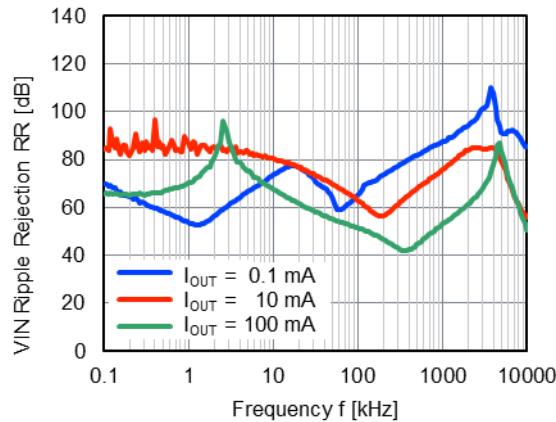
17) VIN Ripple Rejection vs Frequency

$V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$ ($V_{Ripple} = 0.2V_{PP}$), $C_{IN} = \text{none}$

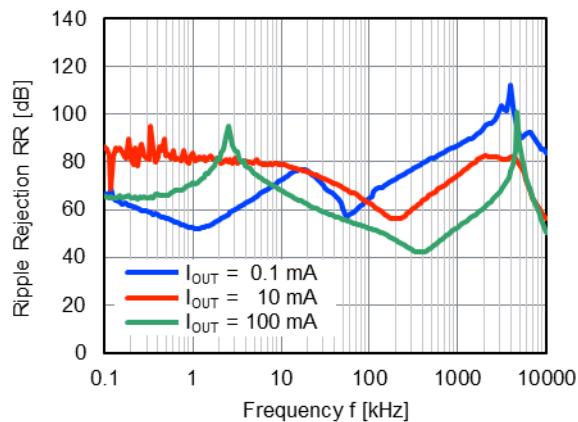
NR1620xx040x



NR1620xx080x



NR1620xx120x

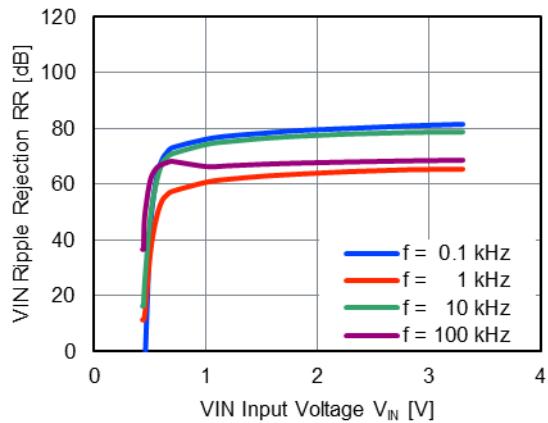


18) VIN Ripple Rejection vs VIN Input Voltage

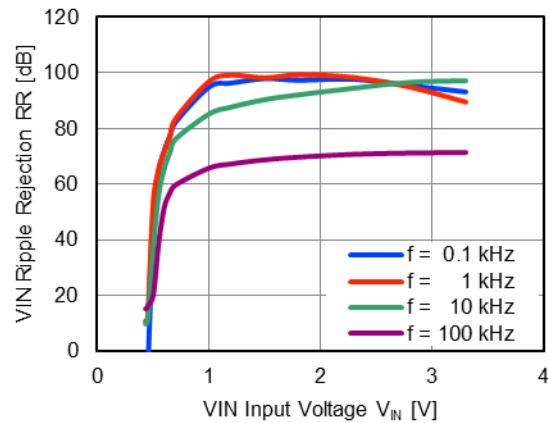
$V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = 3.3 \text{ V}$ to 0 V ($V_{Ripple} = 0.2V_{PP}$), $C_{IN} = \text{none}$

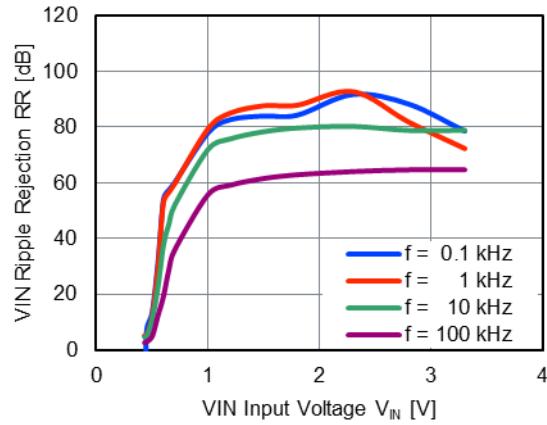
NR1620xx040x

$I_{OUT} = 0.1 \text{ mA}$

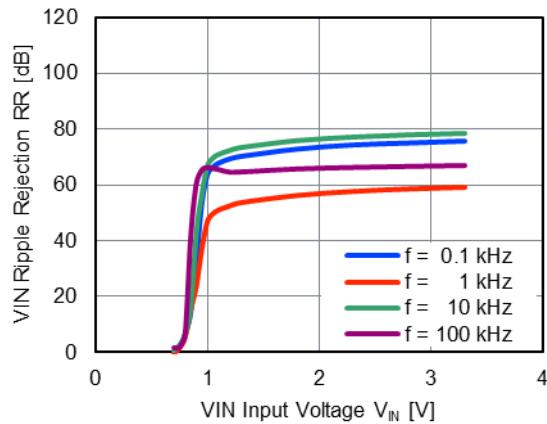
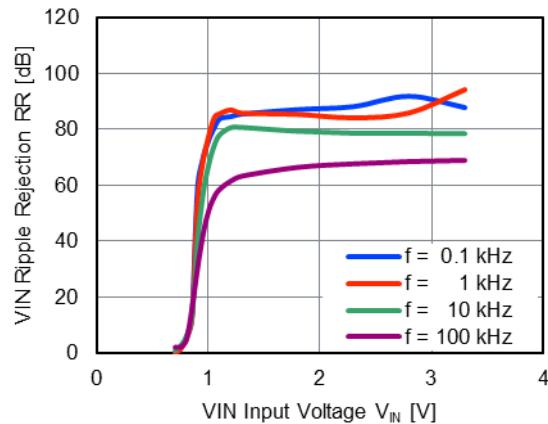
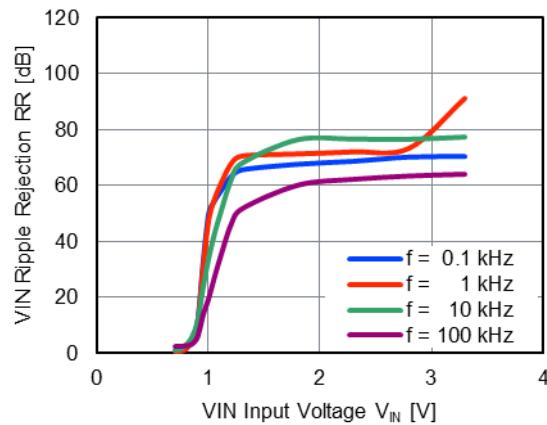


$I_{OUT} = 10 \text{ mA}$



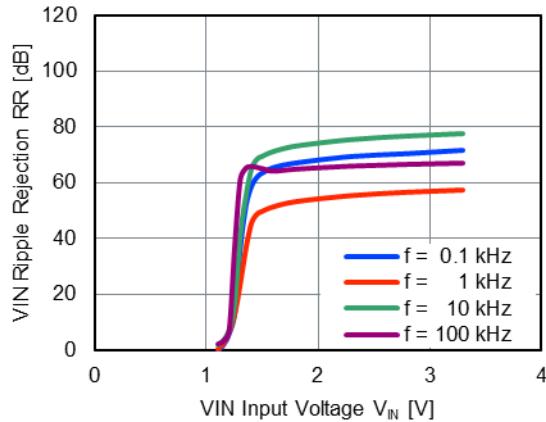
$I_{OUT} = 100 \text{ mA}$ 

NR1620xx080x

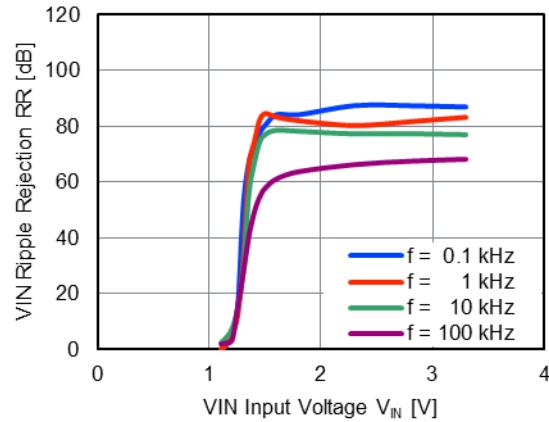
 $I_{OUT} = 0.1 \text{ mA}$  $I_{OUT} = 10 \text{ mA}$  $I_{OUT} = 100 \text{ mA}$ 

NR1620xx120x

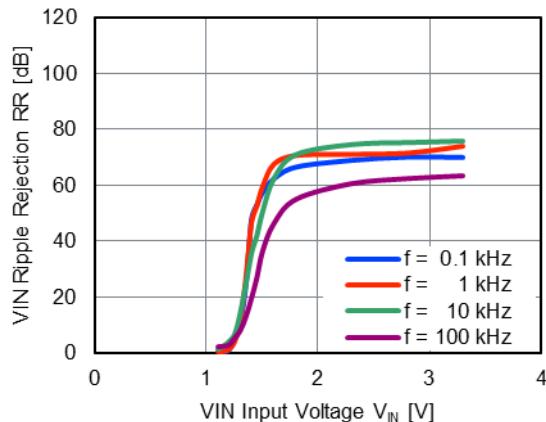
$I_{OUT} = 0.1 \text{ mA}$



$I_{OUT} = 10 \text{ mA}$



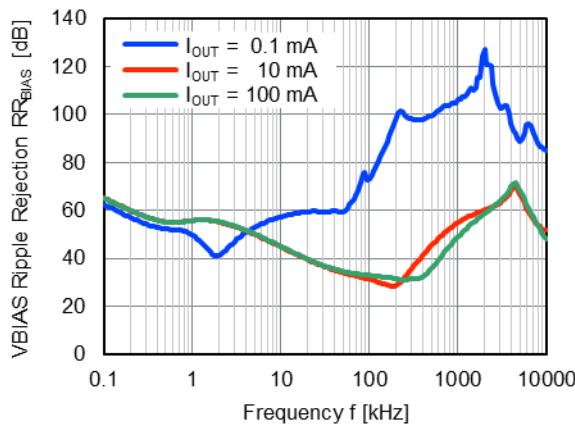
$I_{OUT} = 100 \text{ mA}$



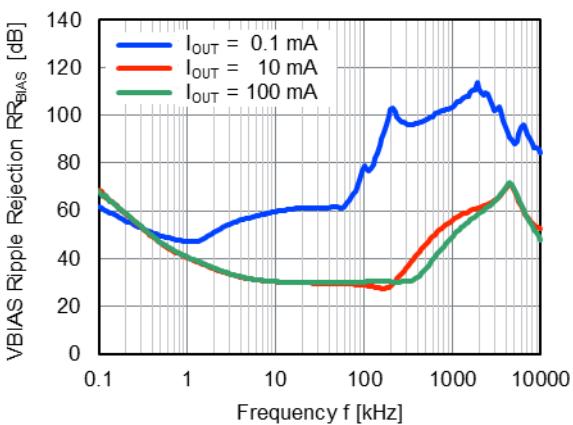
19) VBIAS Ripple Rejection vs Frequency

$V_{BIAS} = 3.3 \text{ V}$ ($V_{Ripple} = 0.2 \text{ V}_{PP}$), $V_{IN} = V_{SET} + 0.5 \text{ V}$, $C_{BIAS} = \text{none}$

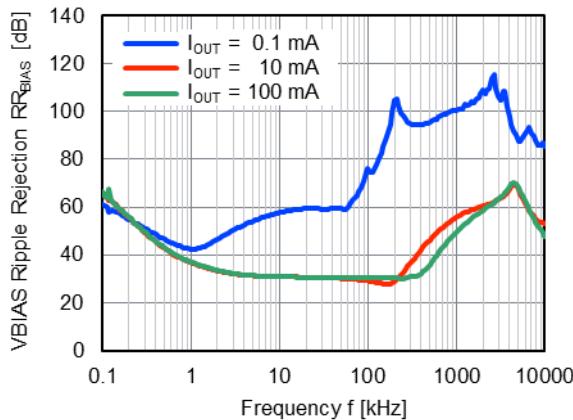
NR1620xx040x



NR1620xx080x



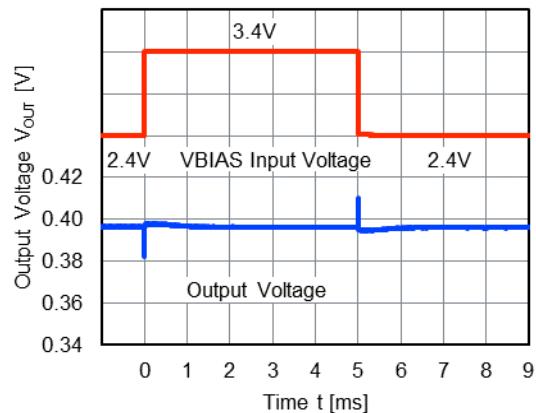
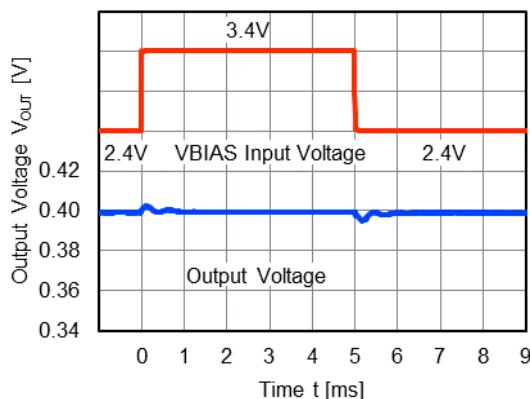
NR1620xx120x



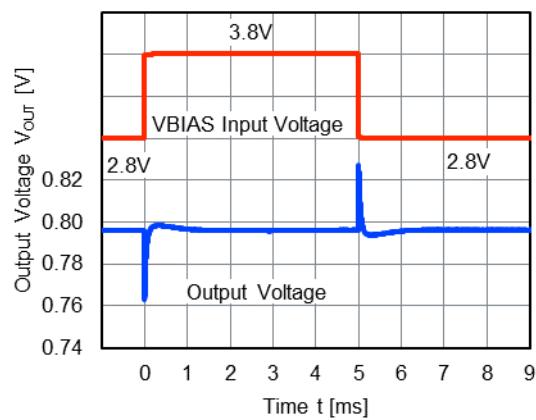
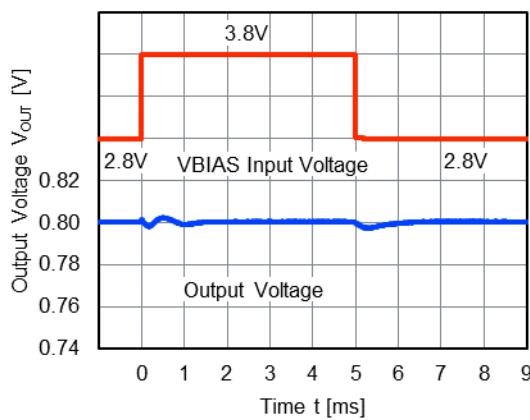
20) VBIAS Line Transient Response

 $V_{BIAS} = V_{SET} + 2\text{ V} \leftrightarrow V_{SET} + 3\text{ V}$ ($t_R = t_F = 5\text{ }\mu\text{s}$), $V_{IN} = V_{SET} + 0.5\text{ V}$, $C_{BIAS} = \text{none}$

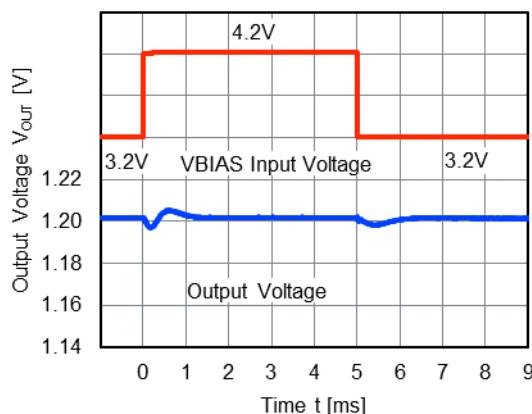
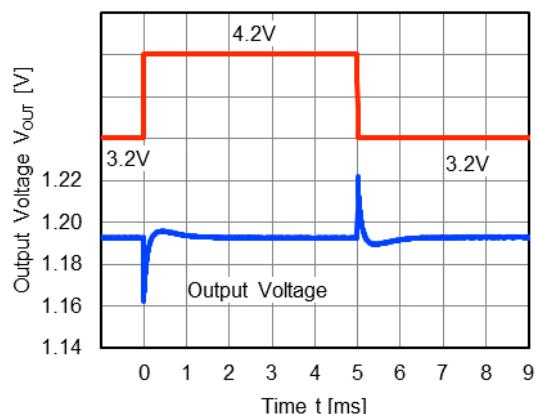
NR1620xx040x

 $I_{OUT} = 100\text{ }\mu\text{A}$ $I_{OUT} = 10\text{ mA}$ 

NR1620xx080x

 $I_{OUT} = 100\text{ }\mu\text{A}$ $I_{OUT} = 10\text{ mA}$ 

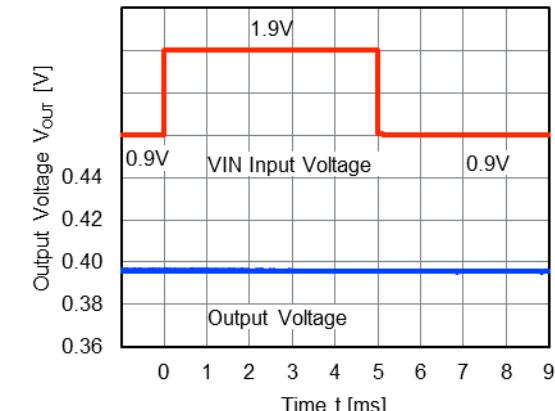
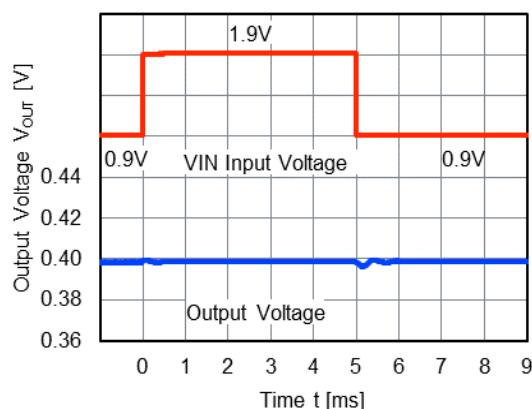
NR1620xx120x

 $I_{OUT} = 100 \mu A$  $I_{OUT} = 10 \text{ mA}$ 

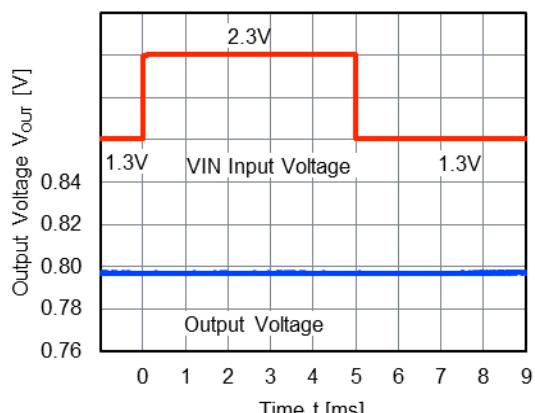
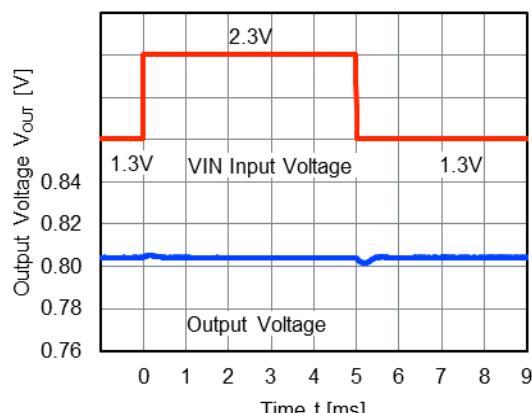
21) VIN Line Transient Response

 $V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V} \leftrightarrow V_{SET} + 1.5 \text{ V}$ ($t_R = t_F = 5 \mu \text{s}$), $C_{IN} = \text{none}$

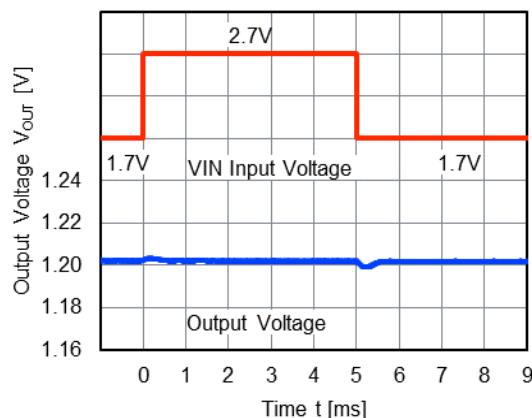
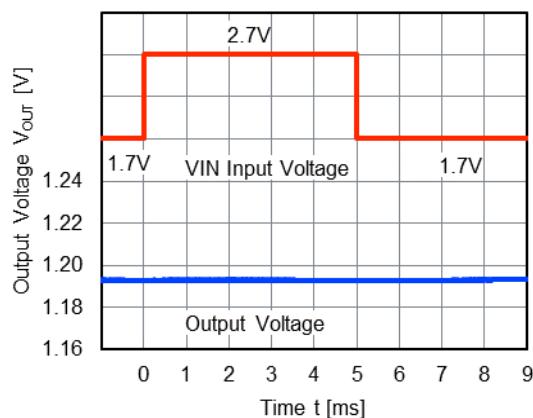
NR1620xx040x

 $I_{OUT} = 100 \mu A$ $I_{OUT} = 10 \text{ mA}$ 

NR1620xx080x

 $I_{OUT} = 100 \mu A$ $I_{OUT} = 10 \text{ mA}$ 

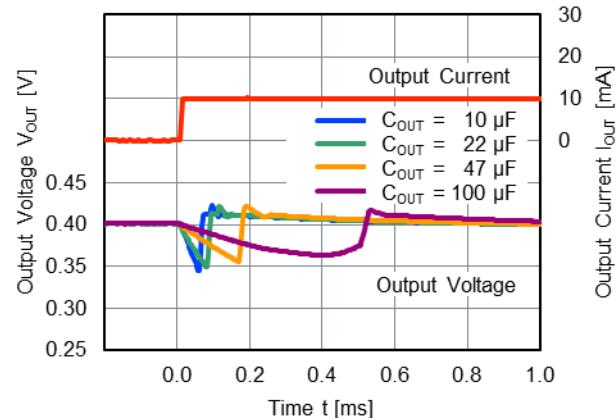
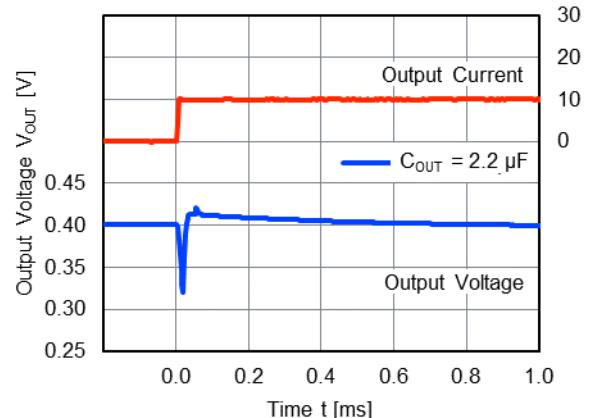
NR1620xx120x

 $I_{OUT} = 100 \mu A$  $I_{OUT} = 10 mA$ 

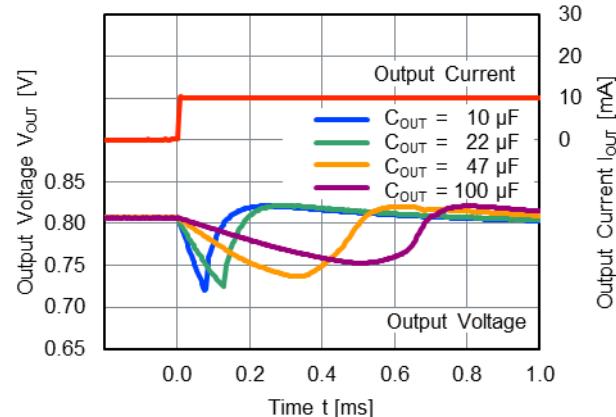
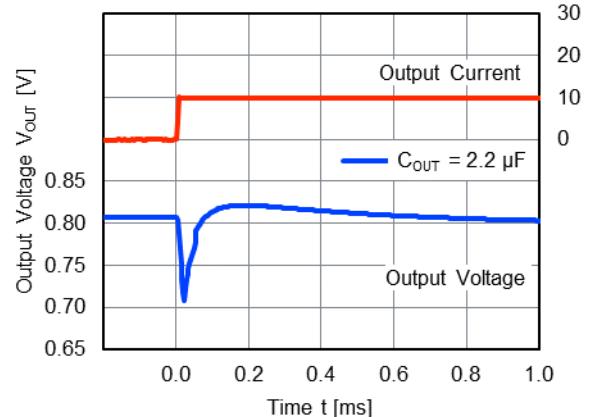
22) Load Transient Response

 $V_{BIAS} = 3.3 V$, $V_{IN} = V_{SET} + 0.5 V$ $I_{OUT} = 1 \mu A \rightarrow 10mA (t_R = 0.5 \mu s)$

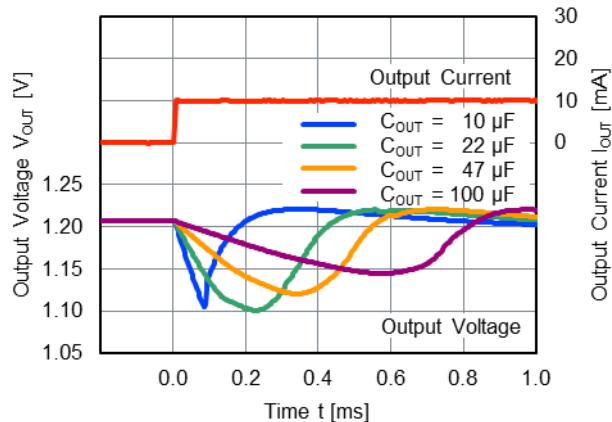
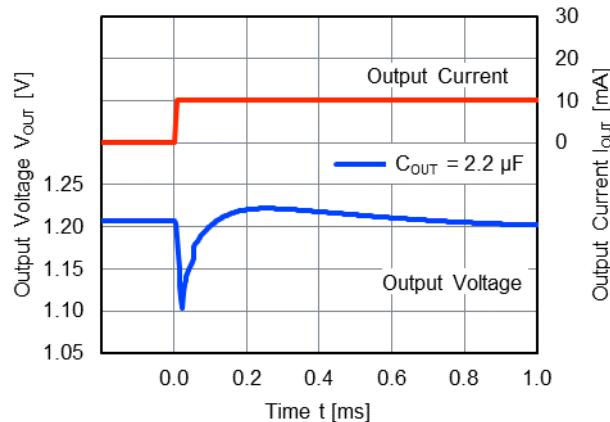
NR1620xx040x



NR1620xx080x



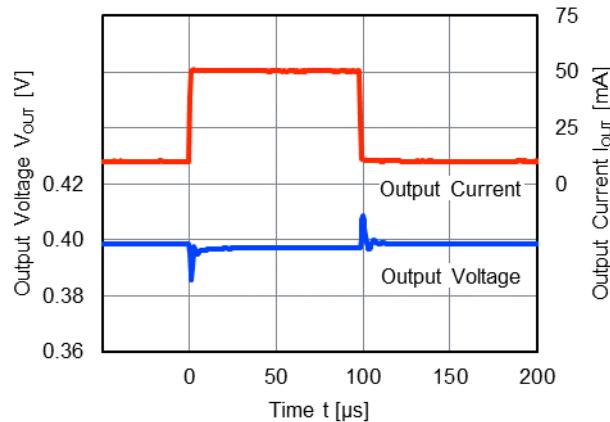
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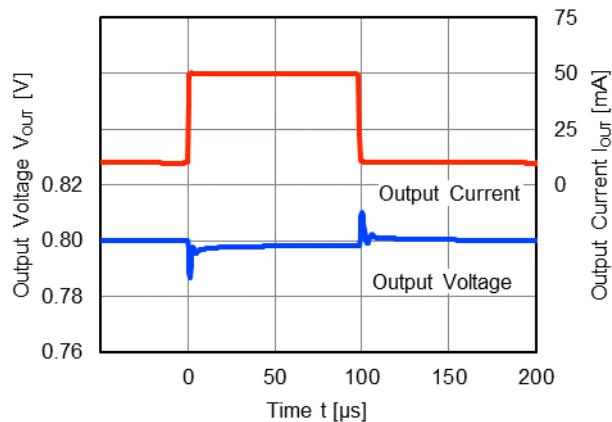
$V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$

$I_{OUT} = 10 \text{ mA} \leftrightarrow 50 \text{ mA}$ ($t_R = t_F = 0.5 \mu \text{s}$)

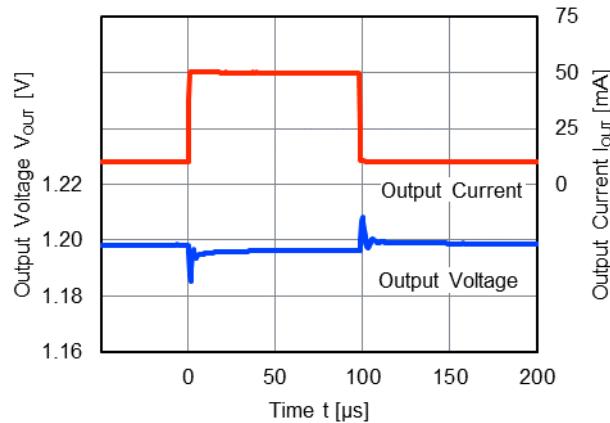
NR1620xx040x



NR1620xx080x



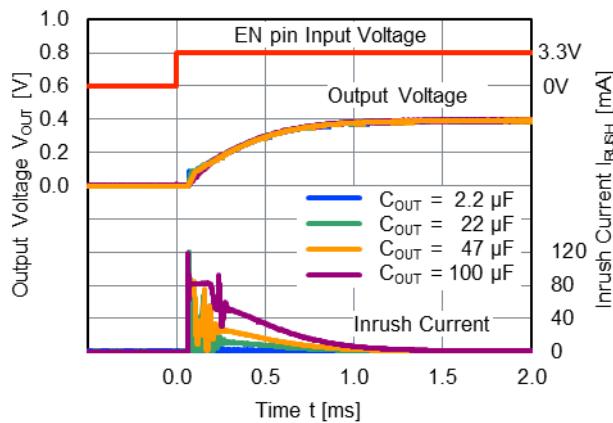
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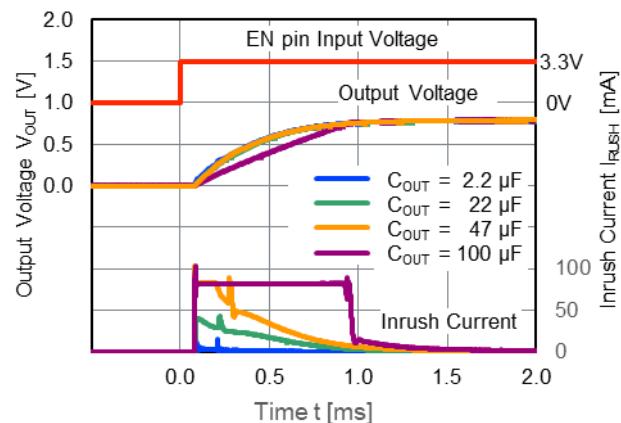
23) Inrush Current

 $V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$, $V_{EN} = 0 \text{ V to } 3.3 \text{ V}$

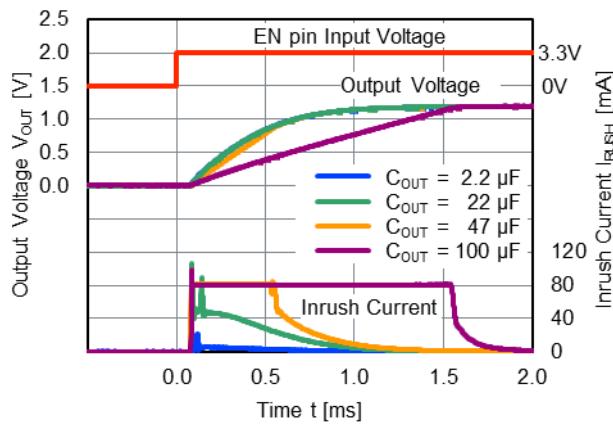
NR1620xx040x



NR1620xx080x



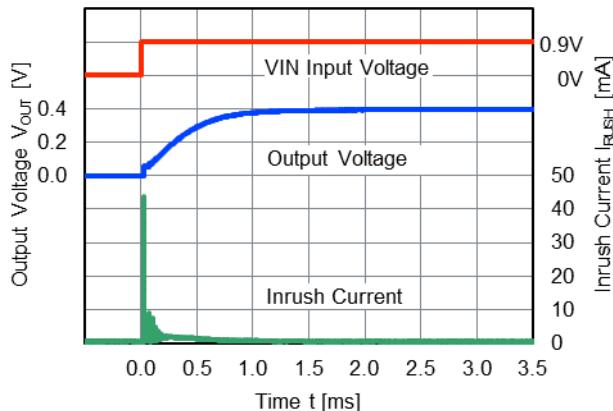
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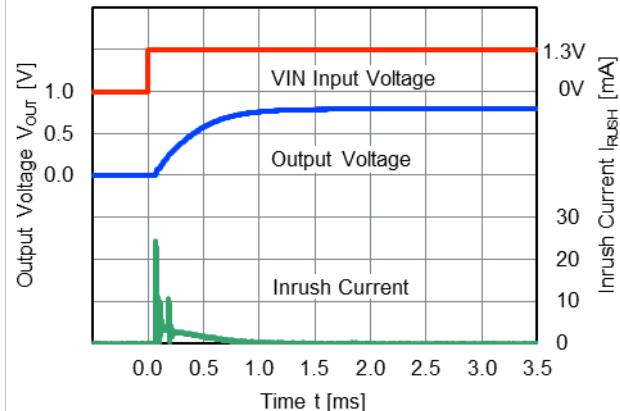
24) Turn on Speed with VIN Pin

 $V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = 0 \text{ V to } V_{SET} + 0.5 \text{ V}$

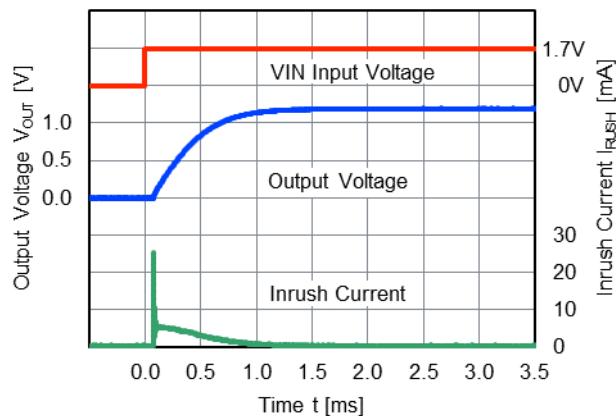
NR1620xx040x



NR1620xx080x



NR1620xx120x

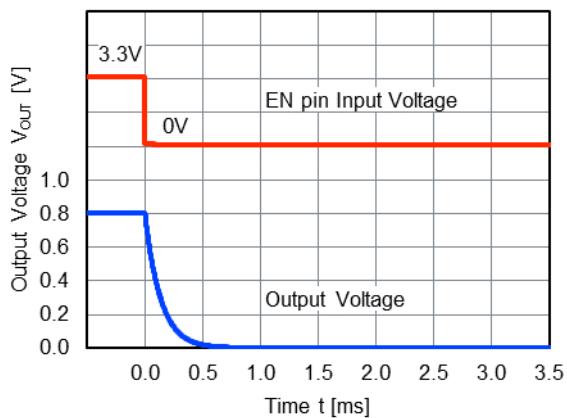
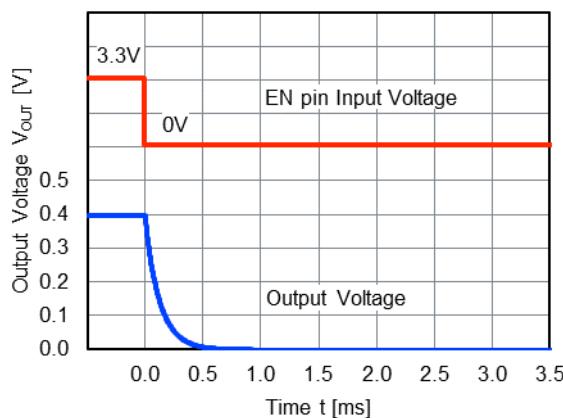


25) Turn off Speed with EN Pin

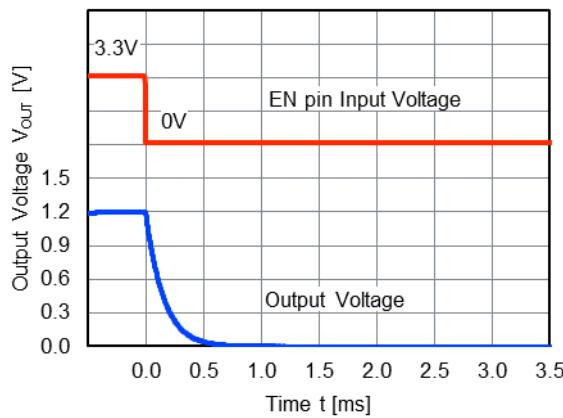
 $V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = V_{SET} + 0.5 \text{ V}$, $V_{EN} = 3.3 \text{ V to } 0 \text{ V}$

NR1620xx040A

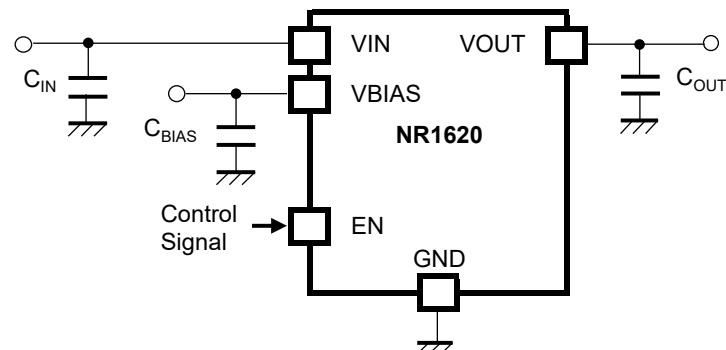
NR1620xx080A



NR1620xx120A



■ TEST CIRCUIT



NR1620 Test Circuit

【Components List for Our Evaluation】

Symbol	Capacitance	Parts Number
C _{IN}	1 μ F	GRM155C70J105KE11D
C _{BIAS}	1 μ F	GRM155C70J105KE11D
C _{OUT}	2.2 μ F	GRM155R61C225KE11D

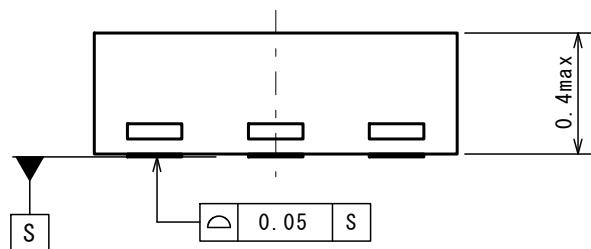
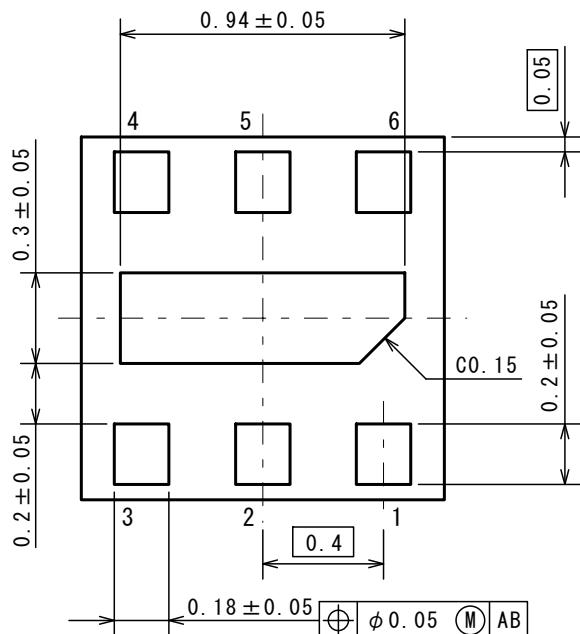
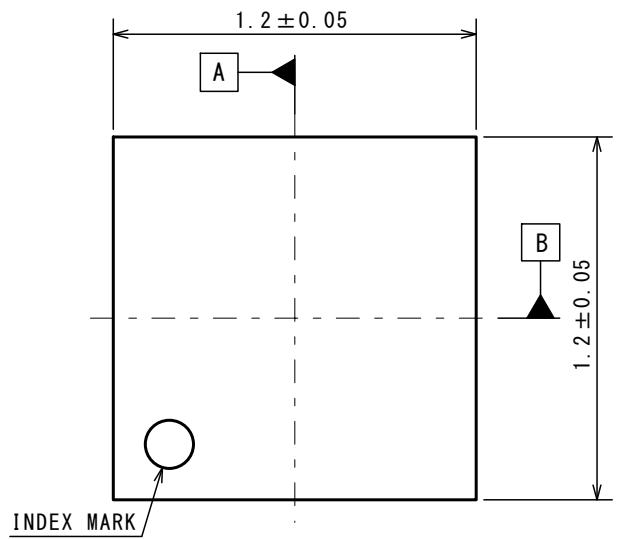
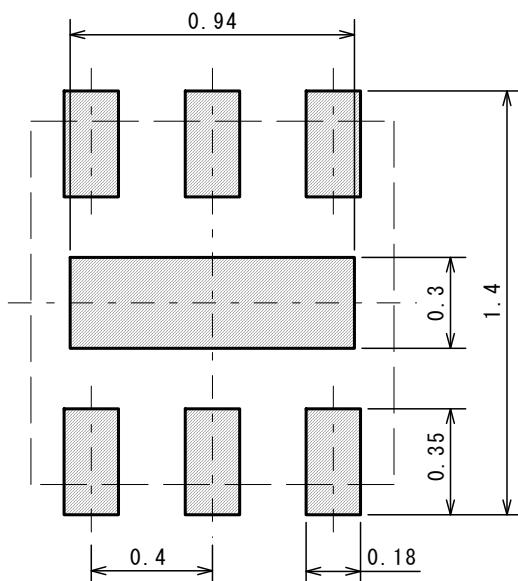
Nissinbo Micro Devices Inc.

DFN1212-6-GK

PI-DFN1212-6-GK-E-A

■ PACKAGE DIMENSIONS

UNIT: mm

**■ EXAMPLE OF SOLDER PADS DIMENSIONS**

Nissinbo Micro Devices Inc.

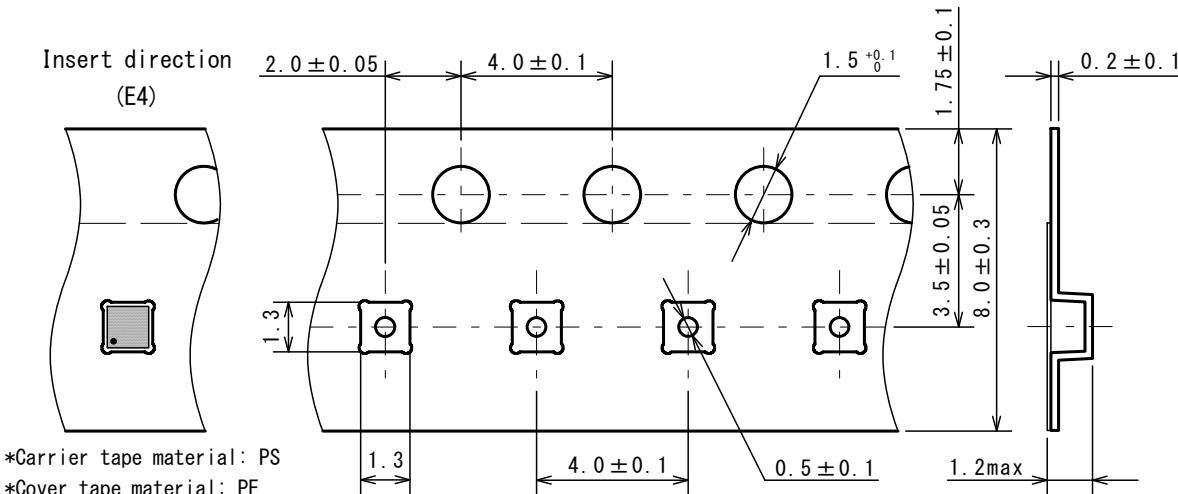
DFN1212-6-GK

PI-DFN1212-6-GK-E-A

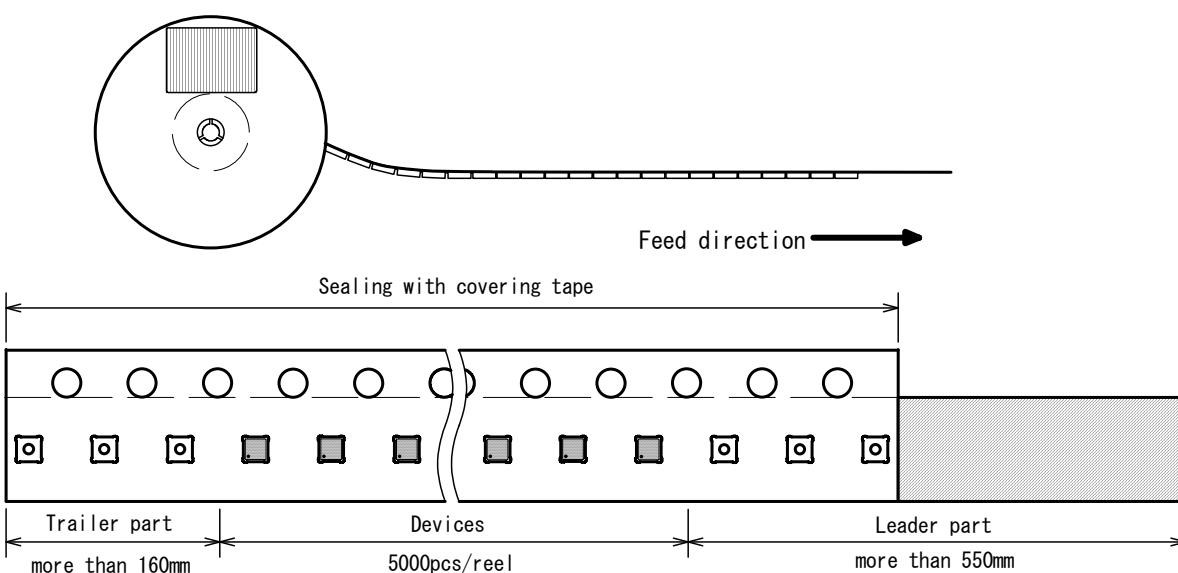
■ PACKING SPEC

(1) Taping dimensions / Insert direction

UNIT: mm



(2) Taping state

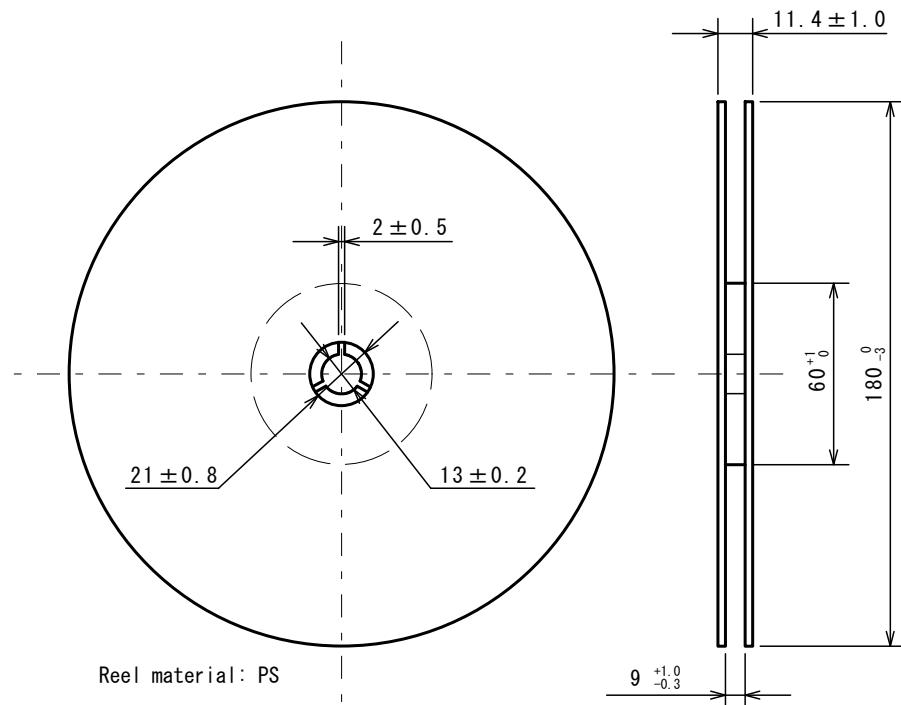


Nissinbo Micro Devices Inc.

DFN1212-6-GK

PI-DFN1212-6-GK-E-A

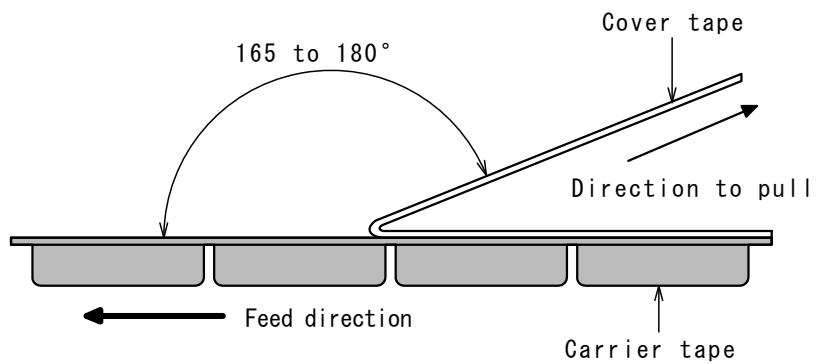
(3) Reel dimensions



(4) Peeling strength

Peeling strength of cover tape

- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.0N

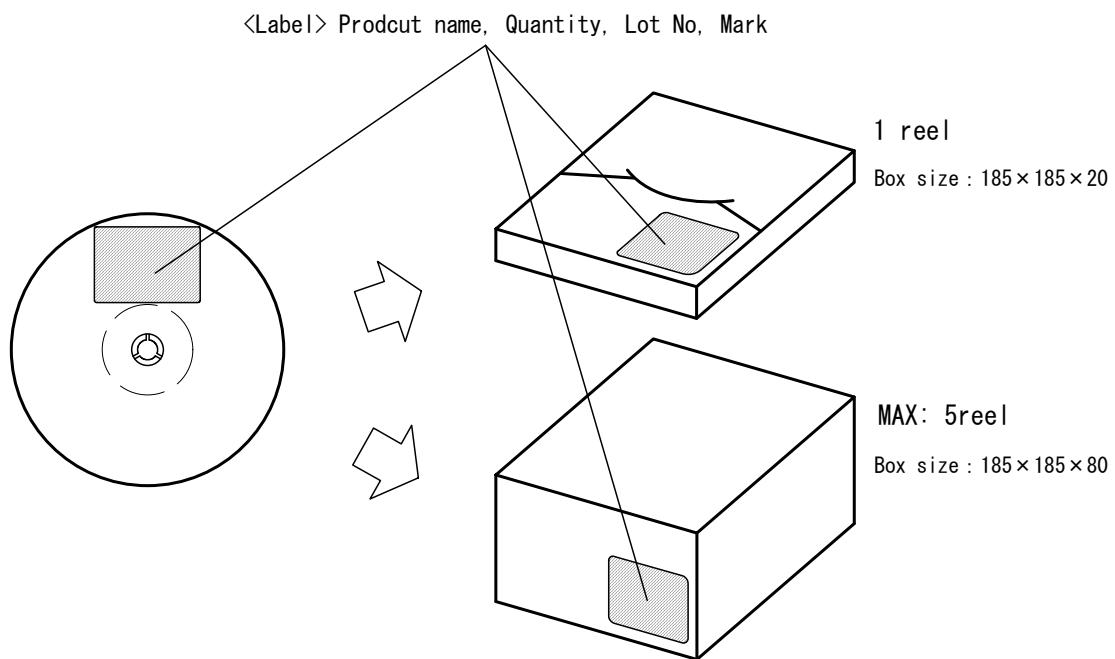


Nissinbo Micro Devices Inc.

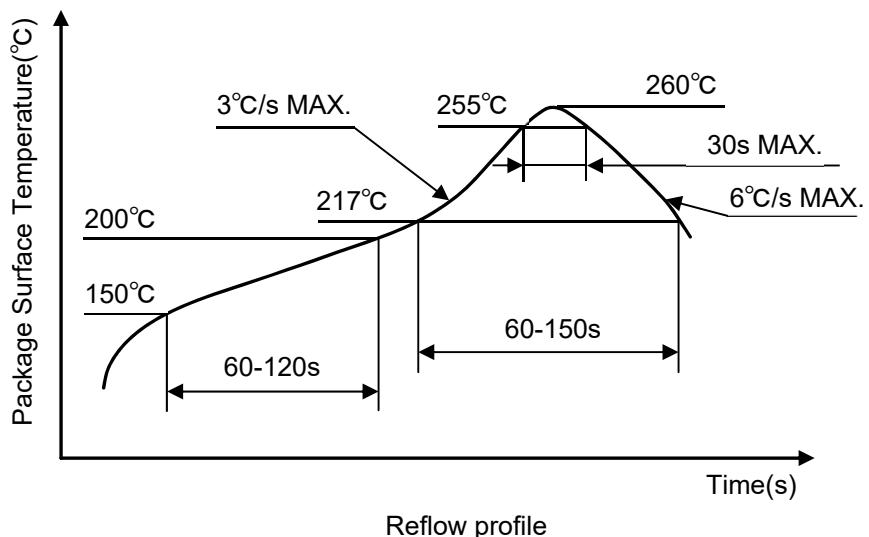
DFN1212-6-GK

PI-DFN1212-6-GK-E-A

(5) Packing state



■ HEAT-RESISTANCE PROFILES



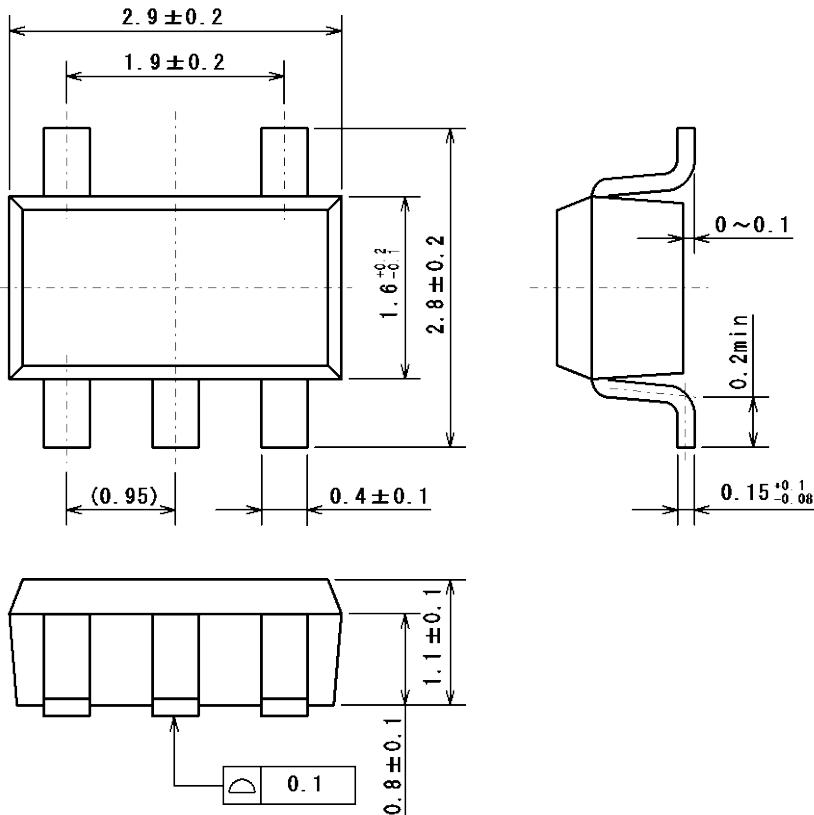
Nissinbo Micro Devices Inc.

SOT-23-5-DC

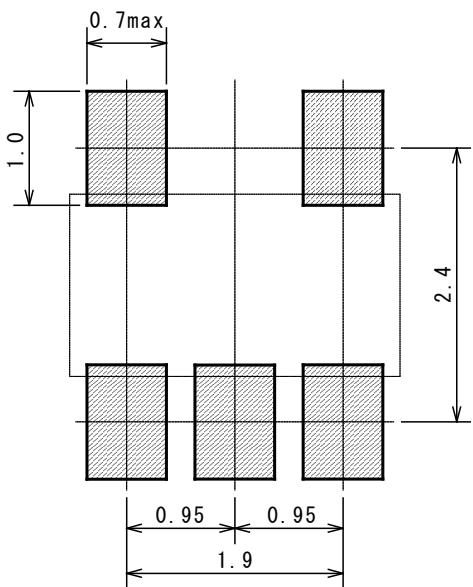
PI-SOT-23-5-DC-E-F

■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Nissinbo Micro Devices Inc.

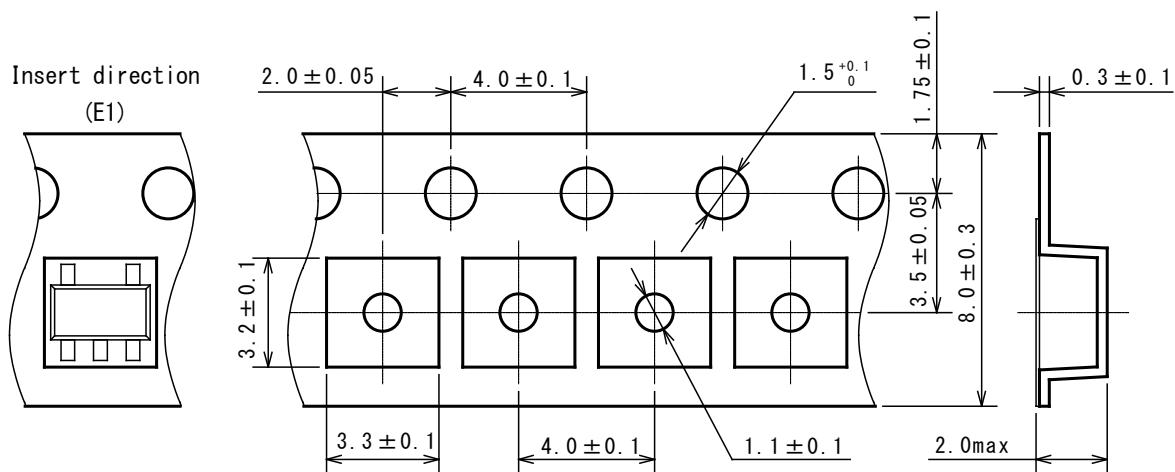
SOT-23-5-DC

PI-SOT-23-5-DC-E-F

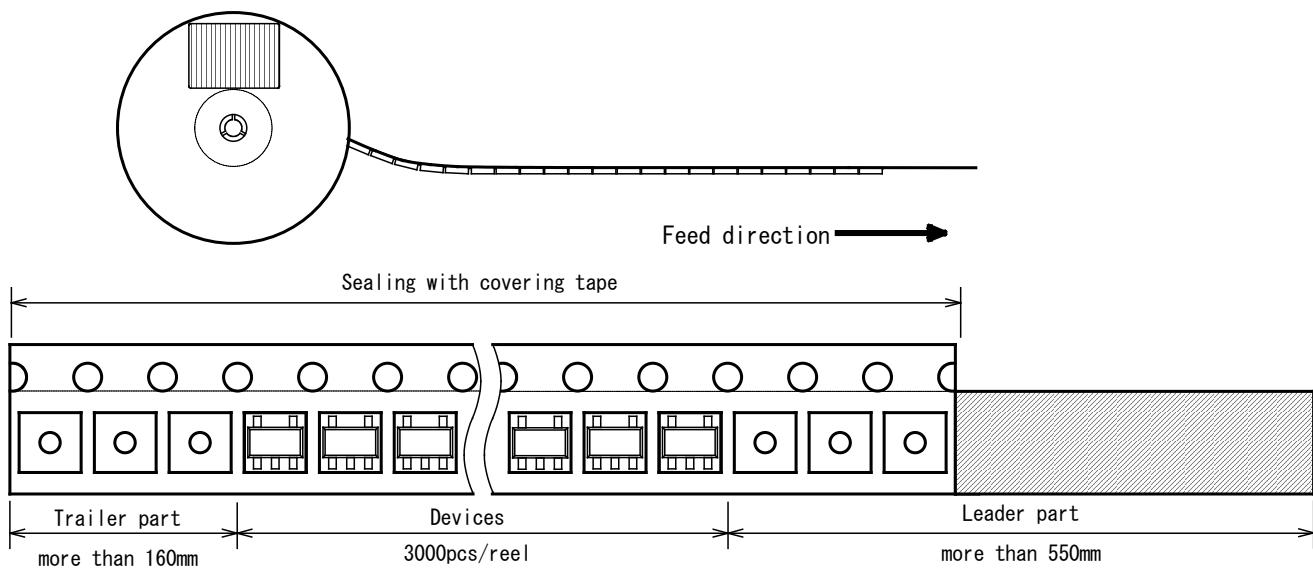
■ PACKING SPEC

(1) Taping dimensions / Insert direction

UNIT: mm



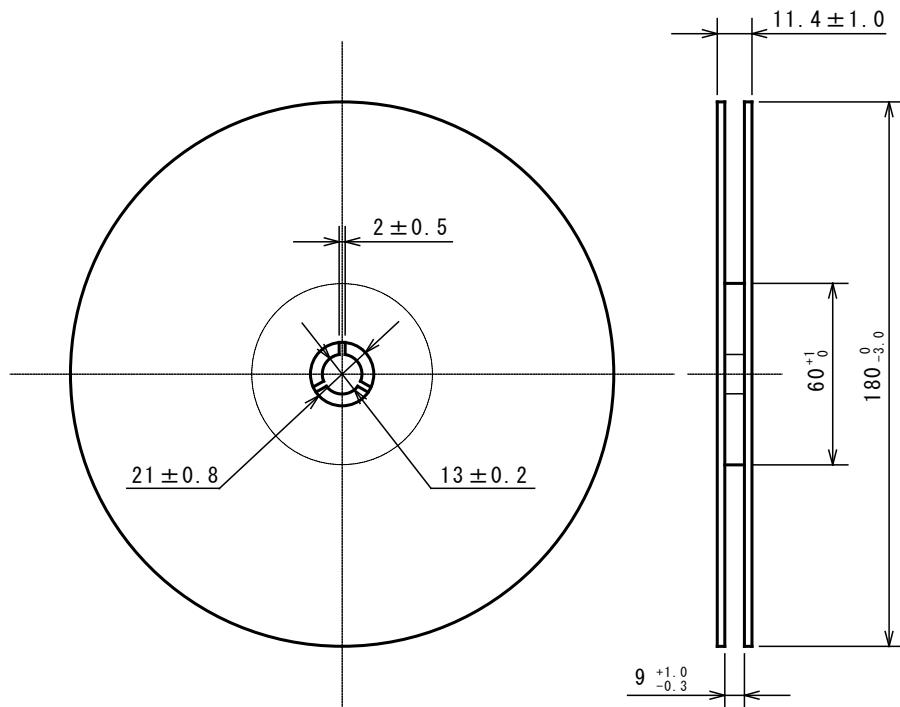
(2) Taping state



Nissinbo Micro Devices Inc.**SOT-23-5-DC**

PI-SOT-23-5-DC-E-F

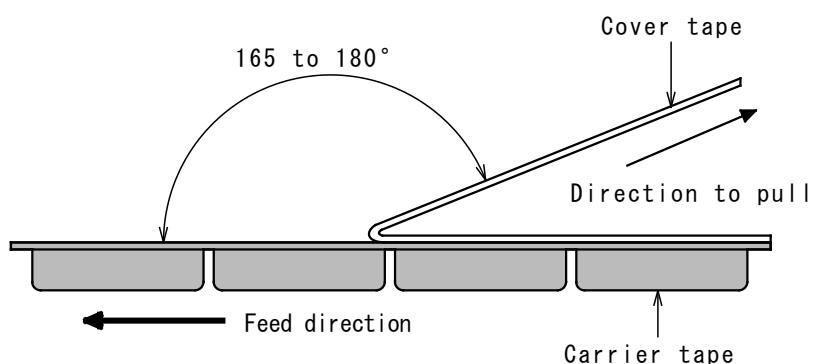
(3) Reel dimensions



(4) Peeling strength

Peeling strength of cover tape

- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.0N



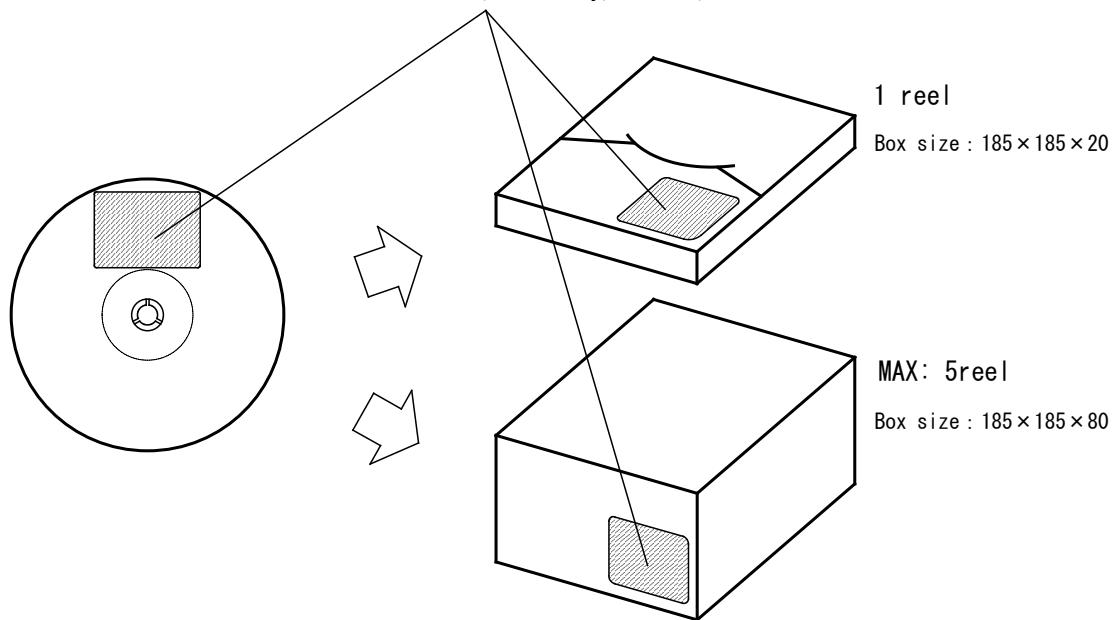
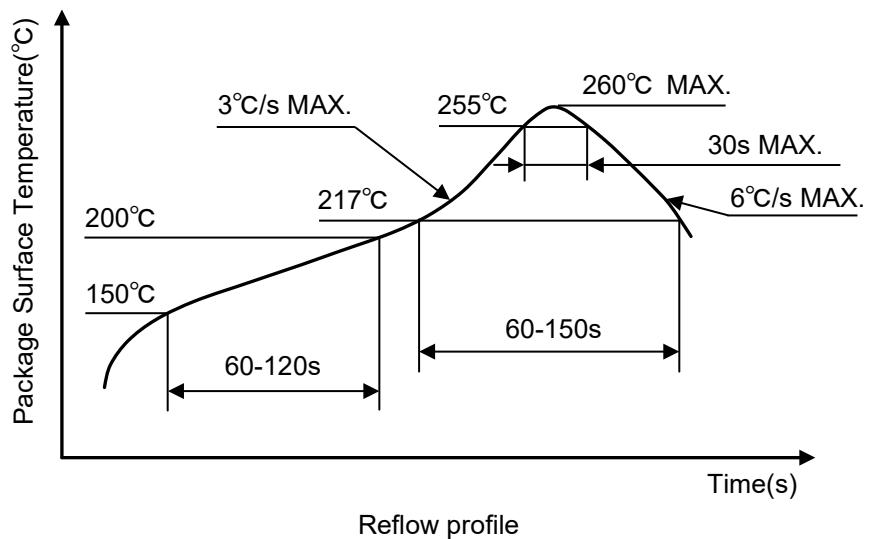
Nissinbo Micro Devices Inc.

SOT-23-5-DC

PI-SOT-23-5-DC-E-F

(5) Packing state

<Label> Product name, Quantity, Lot No, Mark

**■ HEAT-RESISTANCE PROFILES**

Revision History

Date	Revision	Changes
March 08, 2024	Ver. 1.0	Initial release

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
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 - Aerospace Equipment
 - Equipment Used in the Deep Sea
 - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
 - Life Maintenance Medical Equipment
 - Fire Alarms / Intruder Detectors
 - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
 - Various Safety Devices
 - Traffic control system
 - Combustion equipment

In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.

6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty

8-1. Quality Warranty Period

In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.

8-2. Quality Warranty Remedies

When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.

Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.

8-3. Remedies after Quality Warranty Period

With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.

9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.



Nisshinbo Micro Devices Inc.

Official website

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