



# MPQ8633A-H

## 16V, 12A, Configurable-Frequency, Synchronous Step-Down Converter with Adjustable Current Limit and Voltage Tracking

### DESCRIPTION

The MPQ8633A-H is a fully integrated, high-frequency, synchronous step-down converter. It offers a very compact solution that can achieve up to 12A of output current ( $I_{OUT}$ ) across a wide input voltage ( $V_{IN}$ ) range, with excellent load and line regulation. The MPQ8633A-H operates at high efficiency across a wide  $I_{OUT}$  load range.

Internally compensated constant-on-time (COT) control provides fast transient response and eases loop stabilization.

The selectable switching frequency ( $f_{SW}$ ) can be set to 600kHz, 800kHz, or 1000kHz by configuring the MODE pin. This maintains a constant  $f_{SW}$ , regardless of  $V_{IN}$  and the output voltage ( $V_{OUT}$ ).

During start-up, the internal soft-start timer ( $t_{SS}$ ) (1ms) ramps up  $V_{OUT}$  in a controlled manner.  $t_{SS}$  can be increased by adding a capacitor on the TRK/REF pin. An open-drain power good (PG) signal indicates whether  $V_{OUT}$  is within its nominal voltage range. If the input fails to supply power to the MPQ8633A-H, then the PG voltage ( $V_{PG}$ ) is clamped at about 0.7V via an external pull-up voltage.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8633A-H requires a minimal number of readily available, standard external components, and is available in a QFN-21 (3mmx4mm) package.

### FEATURES

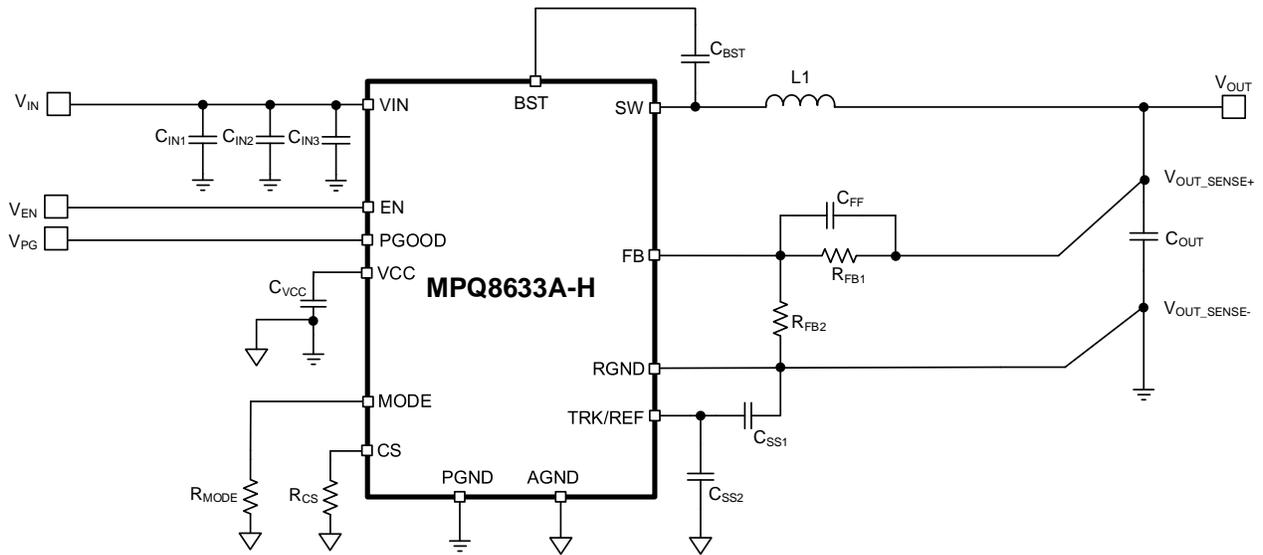
- Wide Input Voltage ( $V_{IN}$ ) Range:
  - 2.7V to 16V with External 3.3V Bias
  - 4V to 16V with Internal Bias or External 3.3V Bias
- Differential Output Voltage ( $V_{OUT}$ ) Remote Sense
- Configurable Accurate Current Limit ( $I_{LIMIT}$ )
- 12A Output Current ( $I_{OUT}$ )
- Integrated Low  $R_{DS(ON)}$  Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive Constant-On-Time (COT) Control for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- Reference Voltage ( $V_{REF}$ ) Accuracy:
  - 0.5%  $V_{REF}$  Accuracy from 0°C to 70°C
  - 1%  $V_{REF}$  Accuracy from -40°C to +125°C
- Selectable Pulse-Skip Mode (PSM) or Forced Continuous Conduction Mode (FCCM)
- Excellent Load Regulation
- $V_{OUT}$  Tracking
- $V_{OUT}$  Discharge
- PGOOD Clamped Low during Power Failure
- Configurable Soft-Start Time ( $t_{SS}$ ) from 1ms
- Pre-Biased Start-Up
- 600kHz, 800kHz, or 1000kHz Selectable Switching Frequency ( $f_{SW}$ )
- Non-Latch OCP, UVP, OVP, UVLO Protection, and Thermal Shutdown
- Adjustable  $V_{OUT}$  from 0.6V to 90% of  $V_{IN}$  (5.5V Max)
- Available in a QFN-21 (3mmx4mm) Package

### APPLICATIONS

- Telecommunication Systems
- Networking Systems
- Servers
- Base Stations

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

## TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ8633A-HGLE	QFN-21 (3mmx4mm)	<i>See Below</i>	1

For Tape & Reel, add suffix -Z (e.g. MPQ8633A-HGLE-Z).

## TOP MARKING

**MPYW**

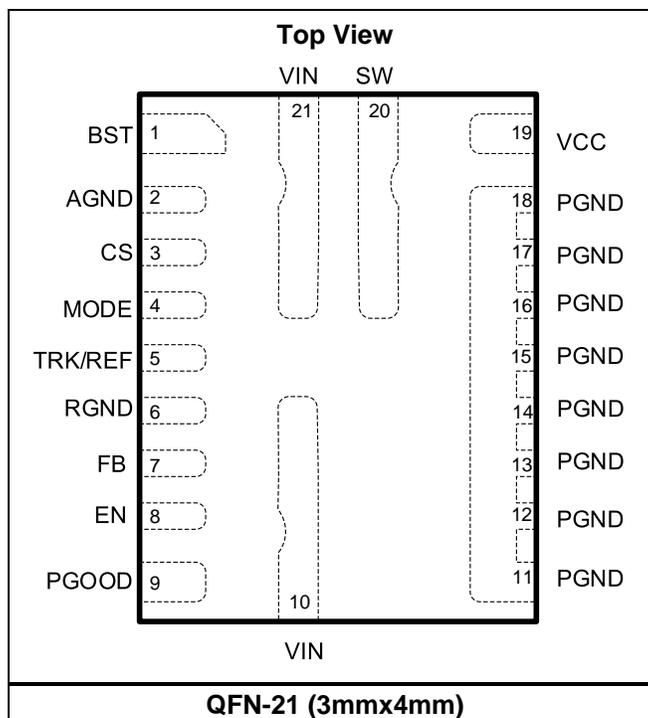
**8633**

**ALLL**

**EH**

MP: MPS prefix  
 Y: Year code  
 W: Week code  
 8633A: First five digits of the part number  
 LLL: Lot number  
 E: Package prefix  
 H: Non-latch OVP

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	BST	<b>Bootstrap.</b> Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
2	AGND	<b>Analog ground.</b> Select the AGND pin to be the control circuit reference point.
3	CS	<b>Current limit.</b> Connect a resistor between the CS pin and AGND to set the current limit ( $I_{LIMIT}$ ) trip point.
4	MODE	<b>Mode selection.</b> Configure the MODE pin to select either forced continuous conduction mode (FCCM) or pulse-skip mode (PSM). MODE also selects the switching frequency ( $f_{SW}$ ). See table 1 on page 14 for additional details.
5	TRK/REF	<b>External voltage-tracking input.</b> The output voltage ( $V_{OUT}$ ) tracks the TRK/REF input signal. Use a ceramic decoupling capacitor to decouple the TRK/REF pin. Place this capacitor as close to TRK/REF as possible. Capacitors with X7R or X5R grade dielectrics are recommended due to their stable temperature characteristics. The TRK/REF capacitor ( $C_{TRK/REF}$ ) determines the soft-start time ( $t_{SS}$ ). See Equation 2 on page 14 for additional details.
6	RGND	<b>Differential remote-sense negative input.</b> Connect the RGND pin directly to the negative side of the voltage-sensing point. Short RGND to PGND if remote sense is not used.
7	FB	<b>Feedback and differential remote-sense positive input.</b> An external resistor divider connected between the output and RGND (tapped to the FB pin) sets $V_{OUT}$ . Place this resistor divider as close to FB as possible. Do not use vias on the FB traces.
8	EN	<b>Enable.</b> The EN pin is an input signal that turns the converter on and off. Pull EN high to turn the converter on; pull EN low to turn it off. Connect the EN and VIN pins via a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
9	PGOOD	<b>Power good output.</b> The PGOOD pin is an open-drain output. A pull-up resistor connected to a DC voltage is required to indicate whether $V_{OUT}$ is within the regulation voltage range. If the output is in regulation, PGOOD is pulled high. There is a delay (about 1ms) between when the FB voltage ( $V_{FB}$ ) exceeds 92.5% and the PGOOD voltage ( $V_{PG}$ ) is pulled high.
10, 21	VIN	<b>Input voltage.</b> The VIN pin supplies power to the internal MOSFET and converter. Use decoupling input capacitors to decouple the input rail. Use wide PCB traces to make the VIN connection.
11, 12, 13, 14, 15, 16, 17, 18	PGND	<b>System ground.</b> The PGND pin is the reference ground of the regulated $V_{OUT}$ , and requires careful consideration when designing the PCB layout. Use wide PCB traces to make the PGND connection.
19	VCC	<b>Internal 3V LDO output.</b> The driver and the control circuitry are powered by the VCC pin. Use a $\geq 1\mu F$ ceramic decoupling capacitor to decouple VCC. Place this capacitor as close to VCC as possible. Capacitors with X7R or X5R grade dielectrics recommended due to their stable temperature characteristics.
20	SW	<b>Switch output.</b> Connect the SW pin to the inductor and the bootstrap capacitor ( $C_{BST}$ ). SW is pulled up to the VIN voltage ( $V_{IN}$ ) by the HS-FET during the pulse-width modulation (PWM) duty cycle on time ( $t_{ON}$ ). SW is pulled low by the inductor current ( $I_L$ ) during the PWM off time ( $t_{OFF}$ ). Use wide PCB traces to make the SW connection.

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Input voltage ( $V_{IN}$ )	18V
$V_{SW}$ (DC)	-0.3V to $V_{IN} + 0.3V$
$V_{SW}$ (25ns) <sup>(2)</sup>	-3V to +25V
$V_{SW}$ (25ns)	-5V to +25V
$V_{BST}$	$V_{SW} + 4V$
$V_{CC}$ , $V_{EN}$	4.5V
All other pins	-0.3V to +4.3V
Junction temperature	170°C
Lead temperature	260°C
Storage temperature	-65°C to +170°C

**Recommended Operating Conditions** <sup>(3)</sup>

Input voltage ( $V_{IN}$ )	4V to 16V
$V_{IN}$ (DC) - $V_{SW}$ (DC) <sup>(4)</sup>	-0.3V to $V_{IN} + 0.3V$
$V_{SW}$ (DC) <sup>(4)</sup>	-0.3V to $V_{IN} + 0.3V$
Output voltage ( $V_{OUT}$ )	0.6V to 5.5V
External VCC Bias ( $V_{CC\_EXT}$ )	3.12V to 3.6V
Max output current ( $I_{OUT\_MAX}$ )	12A
Max output current limit ( $I_{LIMIT\_MAX}$ )	16A
Max peak inductor current ( $I_{L\_PEAK\_MAX}$ )	18A
EN voltage ( $V_{EN}$ )	3.6V
Operating junction temp ( $T_J$ )	-40°C to +125°C

**Thermal Resistance** <sup>(5) (6)</sup>  $\theta_{JB}$   $\theta_{JC\_TOP}$ 

QFN-21 (4mmx3mm)	9.....21.....°C/W
------------------	-------------------

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) Measured using a differential oscilloscope probe.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) If  $V_{IN}$  is 16V, then the voltage rating can be between -3V and +23V for  $\leq 25ns$ , with a maximum repetition rate of 1000kHz.
- 5)  $\theta_{JB}$  is the thermal resistance from the junction to the board around the PGND pin's soldering point.
- 6)  $\theta_{JC\_TOP}$  is the thermal resistance from the junction to the top of the package.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Currents</b>						
Shutdown current	$I_{SD}$	$V_{EN} = 0V$		10	20	$\mu A$
Quiescent current	$I_Q$	$V_{EN} = 2V$ , $V_{FB} = 0.62V$		650	850	$\mu A$
<b>MOSFETs</b>						
High-side MOSFET (HS-FET) switch leakage	$I_{SW\_LKG\_HS}$	$V_{EN} = 0V$ , $V_{SW} = 0V$		0	10	$\mu A$
Low-side MOSFET (LS-FET) switch leakage	$I_{SW\_LKG\_LS}$	$V_{EN} = 0V$ , $V_{SW} = 12V$		0	30	
HS-FET on resistance	$R_{DS(ON)\_HS}$	$V_{EN} = 2V$ , $T_J = 25^{\circ}C$		13.3		m $\Omega$
LS-FET on resistance	$R_{DS(ON)\_LS}$	$V_{EN} = 2V$ , $T_J = 25^{\circ}C$		3.8		m $\Omega$
<b>Current Limit (<math>I_{LIMIT}</math>)</b>						
Current limit threshold	$V_{LIMIT}$		1.15	1.2	1.25	V
$I_{CS}$ to $I_{OUT}$ ratio	$I_{CS} / I_{OUT}$	$I_{OUT} \geq 2A$	18	20	22	$\mu A/A$
LS-FET negative current limit	$I_{LIMIT\_NEG}$			-9		A
Negative current limit timer <sup>(7)</sup>	$t_{NCL}$			200		ns
<b>Switching Frequency (<math>f_{sw}</math>)</b>						
Switching frequency <sup>(8)</sup>	$f_{sw}$	$R_{MODE}$ is pulled to AGND, $I_{OUT} = 0A$ , $V_{OUT} = 1V$	480	600	720	kHz
		$R_{MODE} = 30.1k\Omega$ , $I_{OUT} = 0A$ , $V_{OUT} = 1V$	680	800	920	kHz
		$R_{MODE} = 60.4k\Omega$ , $I_{OUT} = 0A$ , $V_{OUT} = 1V$	850	1000	1150	kHz
Minimum on time <sup>(7)</sup>	$t_{ON\_MIN}$	$V_{FB} = 500mV$			50	ns
Minimum off time <sup>(7)</sup>	$t_{OFF\_MIN}$	$V_{FB} = 500mV$			180	ns
<b>Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)</b>						
OVP threshold	$V_{OVP}$		113	116	119	% of $V_{REF}$
UVP threshold	$V_{UVP}$		77	80	83	% of $V_{REF}$
<b>Feedback (FB) and Soft Start (SS)</b>						
Reference voltage	$V_{REF}$	$T_J = -40^{\circ}C$ to $+125^{\circ}C$	594	600	606	mV
		$T_J = 0^{\circ}C$ to $+70^{\circ}C$	597	600	603	mV
TRK/REF source current	$I_{SOURCE\_TRK/REF}$	$V_{TRK/REF} = 0V$		42		$\mu A$
TRK/REF sink current	$I_{SINK\_TRK/REF}$	$V_{TRK/REF} = 1V$		12		$\mu A$
Soft-start time	$t_{SS}$	$C_{TRK/REF} = 1nF$ , $T_J = 25^{\circ}C$	0.75	1	1.25	ms
<b>Error Amplifier (EA)</b>						
EA offset	$V_{OFFSET}$		-3	0	+3	mV
FB current	$I_{FB}$	$V_{FB} = V_{REF}$		50	100	nA

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Enable (EN) and Under-Voltage Lockout (UVLO) Protection</b>						
EN rising threshold	$V_{EN\_RISING}$		1.17	1.22	1.27	V
EN hysteresis	$V_{EN\_HYS}$			200		mV
EN current	$I_{EN}$	$V_{EN} = 2V$		0		$\mu A$
Soft-shutdown discharge MOSFET on resistance	$R_{DS(ON)\_DISCHARGE}$			80	150	$\Omega$
<b><math>V_{IN}</math> UVLO</b>						
$V_{IN}$ UVLO rising threshold	$V_{IN\_UVLO\_RISING}$	$V_{CC} = 3.3V$	2.1	2.4	2.7	V
$V_{IN}$ UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	$V_{CC} = 3.3V$	1.55	1.85	2.15	V
<b>VCC Regulator</b>						
VCC UVLO rising threshold	$V_{CC\_UVLO\_RISING}$		2.65	2.8	2.95	V
VCC UVLO falling threshold	$V_{CC\_UVLO\_FALLING}$		2.35	2.5	2.65	V
VCC voltage	$V_{CC}$		2.88	3.00	3.12	V
VCC load regulation		$I_{CC} = 25mA$		0.5		% of $V_{CC}$
<b>Power Good (PG)</b>						
PG rising high threshold	$V_{PG\_RISING\_HIGH}$	$V_{FB}$ is pulled high	89.5	92.5	95.5	% of $V_{REF}$
PG rising low threshold	$V_{PG\_RISING\_LOW}$	$V_{FB}$ is pulled high	113	116	119	% of $V_{REF}$
PG falling high threshold	$V_{PG\_FALLING\_HIGH}$	$V_{FB}$ is pulled low	98	101	104	% of $V_{REF}$
PG falling low threshold	$V_{PG\_FALLING\_LOW}$	$V_{FB}$ is pulled low	77	80	83	% of $V_{REF}$
PG low to high delay	$t_{PG}$	$T_J = 25^{\circ}C$	0.6	0.9	1.2	ms
PG sink current capability	$V_{PG\_SINK}$	$I_{PG} = 10mA$			0.4	V
PG leakage current	$I_{PG\_LKG}$	$V_{PG} = 3.3V$			3	$\mu A$
PG output voltage low level	$V_{OUT\_LOW\_100}$	$V_{IN} = 0V$ , $V_{PG}$ is pulled up to 3.3V via a 100k $\Omega$ resistor, $T_J = 25^{\circ}C$		650	800	mV
	$V_{OUT\_LOW\_10}$	$V_{IN} = 0V$ , $V_{PG}$ is pulled up to 3.3V via a 10k $\Omega$ resistor, $T_J = 25^{\circ}C$		750	900	mV
<b>Thermal Shutdown</b>						
Thermal shutdown <sup>(7)</sup>	$T_{SD}$			160		$^{\circ}C$
Thermal shutdown hysteresis <sup>(7)</sup>				30		$^{\circ}C$

**Notes:**

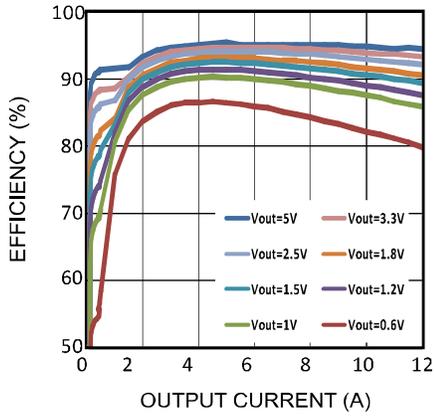
- 7) Guaranteed by design.  
 8) Guaranteed by design to remain in the specified range across different temperature ranges.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_A = 25^\circ C$ ,  $V_{OUT} = 1.2V$ ,  $f_{sw} = 800kHz$ , unless otherwise noted.

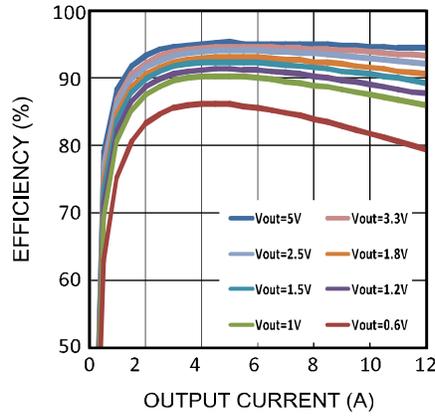
### Efficiency

PSM,  $L = 1.1\mu H$ ,  $f_{sw} = 800kHz$



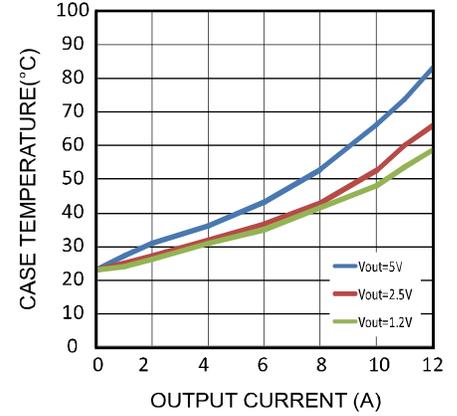
### Efficiency

FCCM,  $L = 1.1\mu H$ ,  $f_{sw} = 800kHz$



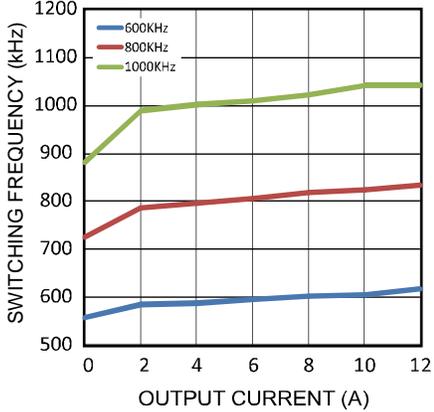
### Case Temperature Rise

$f_{sw} = 800kHz$

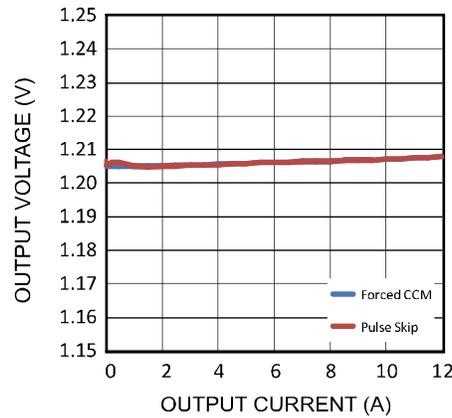


### Switching Frequency vs. Output Current

FCCM



### Load Regulation

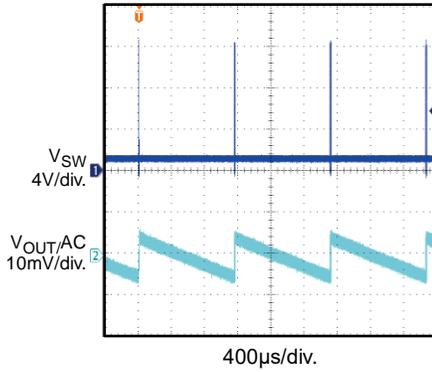


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.

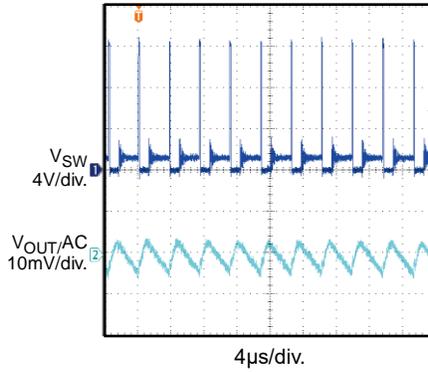
### Steady State

$I_{OUT} = 0A$ , PSM



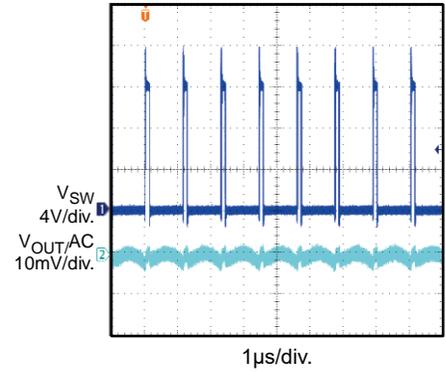
### Steady State

$I_{OUT} = 0.5A$ , PSM



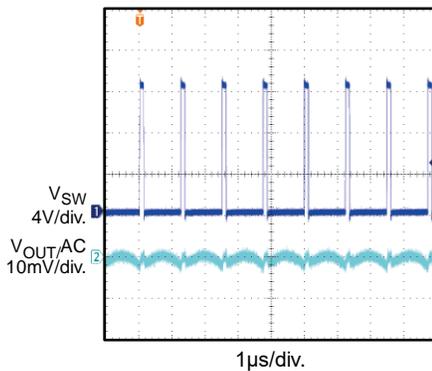
### Steady State

$I_{OUT} = 12A$ , PSM



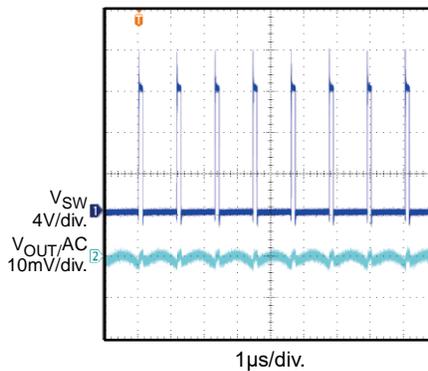
### Steady State

$I_{OUT} = 0A$ , FCCM



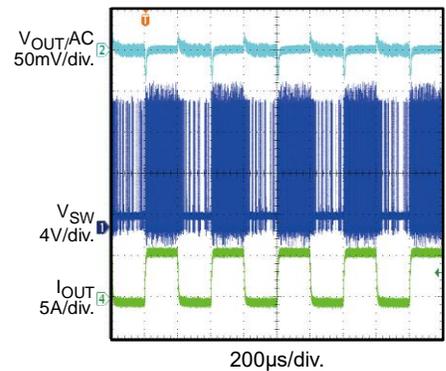
### Steady State

$I_{OUT} = 12A$ , FCCM



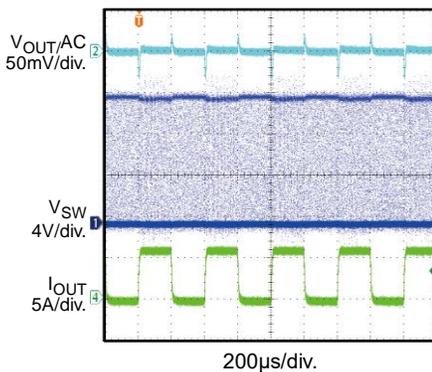
### Load Transient

$I_{OUT} = 0A$  to 6A, PSM



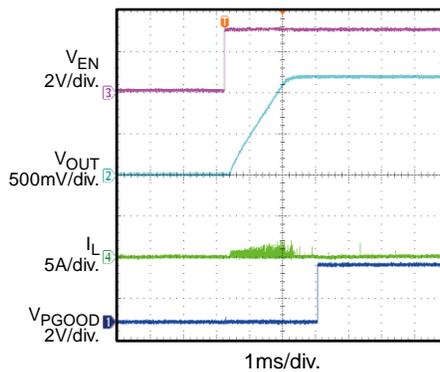
### Load Transient

$I_{OUT} = 0A$  to 6A, FCCM



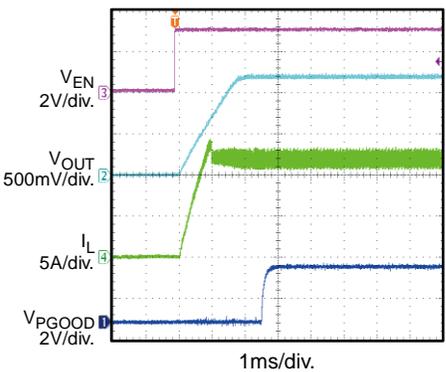
### Start-Up through EN

$I_{OUT} = 0A$ , PSM



### Start-Up through EN

$I_{OUT} = 12A$ , PSM

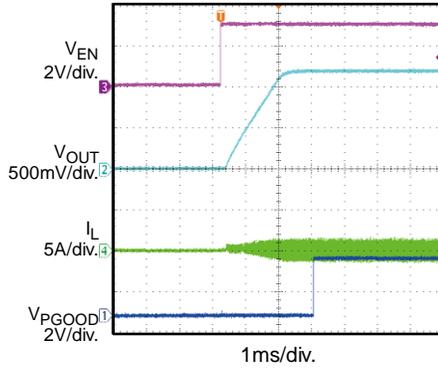


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Performance waveforms are tested on the evaluation board.

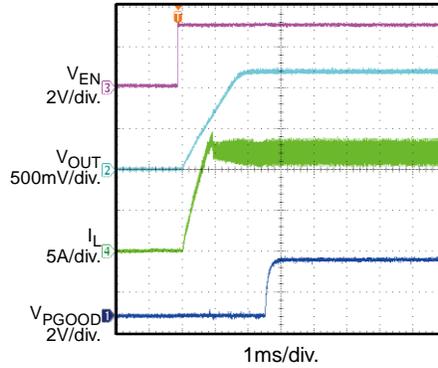
### Start-Up through EN

$I_{OUT} = 0A$ , FCCM



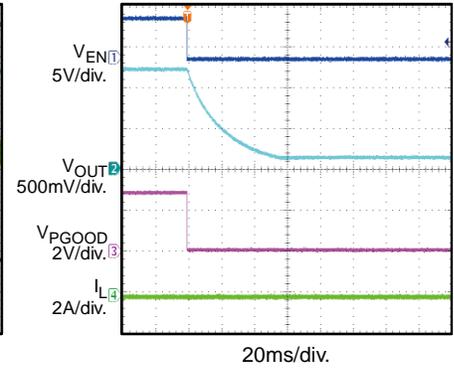
### Start-Up through EN

$I_{OUT} = 12A$ , FCCM



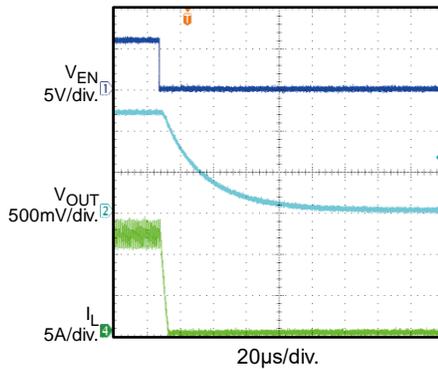
### Shutdown through EN

$I_{OUT} = 0A$ , PSM



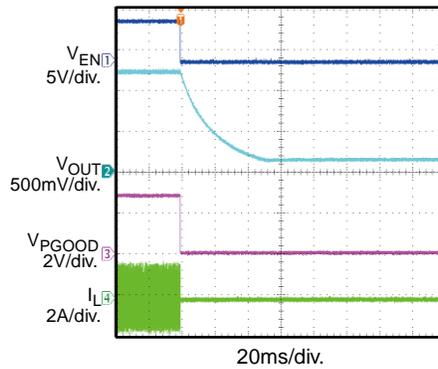
### Shutdown through EN

$I_{OUT} = 12A$ , PSM



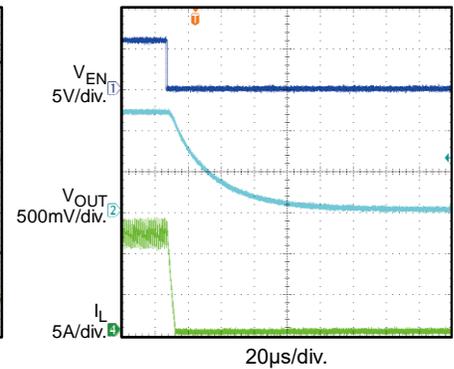
### Shutdown through EN

$I_{OUT} = 0A$ , FCCM



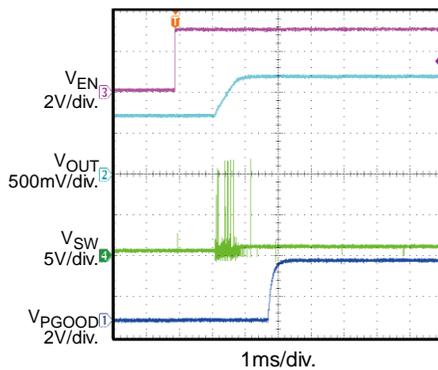
### Shutdown through EN

$I_{OUT} = 12A$ , FCCM



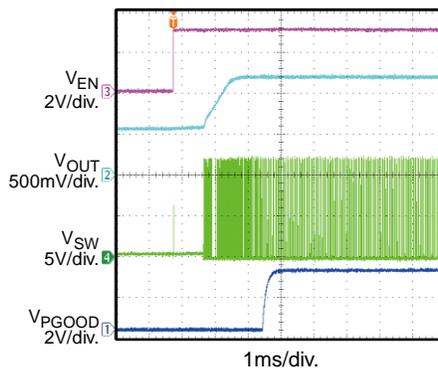
### Pre-Bias Start-Up

PSM

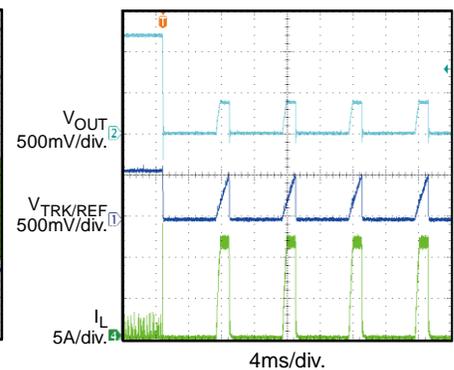


### Pre-Bias Start-Up

FCCM



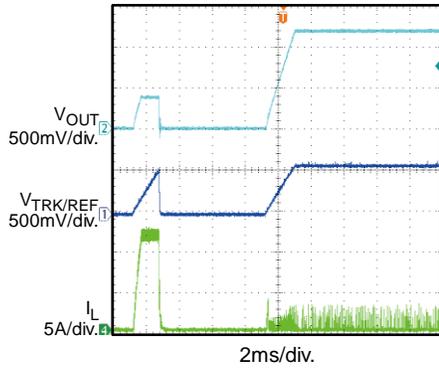
### OCP Entry



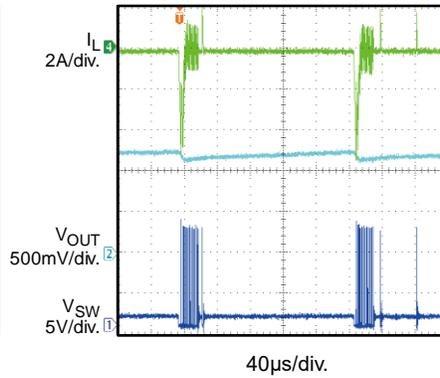
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.

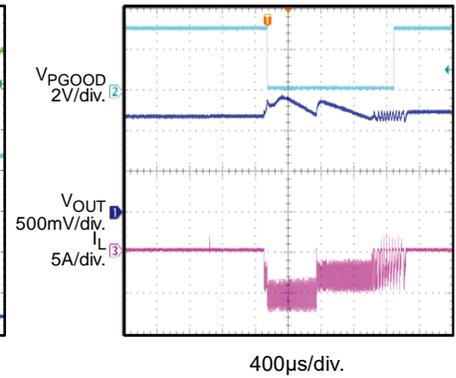
### OCP Recovery



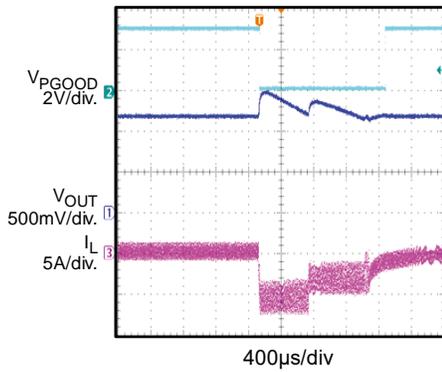
### Output Sink Mode PSM



### Over-Voltage Protection PSM



### Over-Voltage Protection FCCM



## FUNCTIONAL BLOCK DIAGRAM

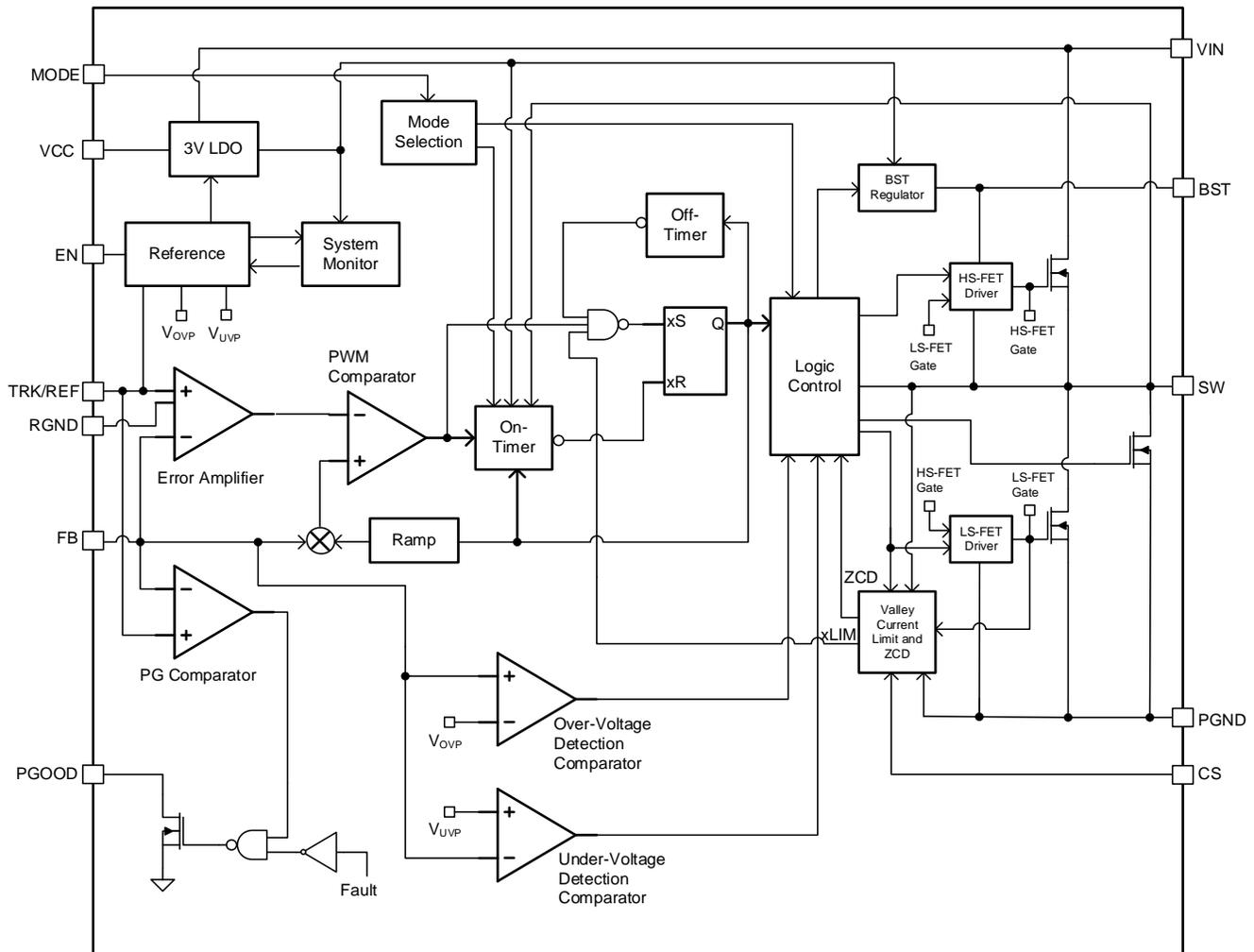


Figure 1: Functional Block Diagram

## OPERATION

### Constant-On-Time (COT) Control

Constant-on-time (COT) control provides fast load transient response and eases loop stabilization. Figure 2 shows COT control.

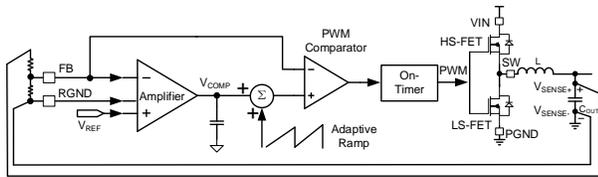


Figure 2: COT Control

The operational amplifier corrects any error voltage between the FB voltage ( $V_{FB}$ ) and the reference voltage ( $V_{REF}$ ). With the amplifier, the MPQ8633A-H can provide excellent load regulation across the entire load range, regardless of the operation mode.

The dedicated RGND pin provides differential output voltage ( $V_{OUT}$ ) remote sensing. The remote-sensing traces should be kept in a low-impedance state for the best performance.

The MPQ8633A-H includes internal ramp compensation to support the low ESR MLCC output capacitor ( $C_{OUT}$ ) solution. Adaptive internal ramp compensation provides stability across the entire input voltage ( $V_{IN}$ ) range and  $V_{OUT}$  range with proper design of the output L/C filter.

### Pulse-Width Modulation (PWM)

The amplifier corrects any error voltage between  $V_{FB}$  and  $V_{REF}$ , and generates a fairly smooth DC comparator (COMP) voltage ( $V_{COMP}$ ). The internal ramp is superimposed onto COMP. The superimposed  $V_{COMP}$  is compared to  $V_{FB}$ . If  $V_{FB}$  drops below  $V_{COMP}$ , then the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time ( $t_{ON}$ ). This fixed  $t_{ON}$  is determined by  $V_{IN}$ ,  $V_{OUT}$ , and the selected switching frequency ( $f_{SW}$ ). Once  $t_{ON}$  finishes, the HS-FET turns off. The HS-FET turns on again once  $V_{FB}$  drops below  $V_{COMP}$ . By repeating this operation, the MPQ8633A-H regulates  $V_{OUT}$ . The integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off to minimize conduction loss. If both the HS-FET and the LS-FET turn on simultaneously, then a dead short occurs

between the  $V_{IN}$  and PGND pins. This is known as shoot-through. To avoid shoot-through, a dead time (DT) is inserted between the HS-FET off time ( $t_{OFF}$ ) and the LS-FET  $t_{ON}$ , and vice versa.

Figure 3 shows PWM mode under heavy-load conditions.

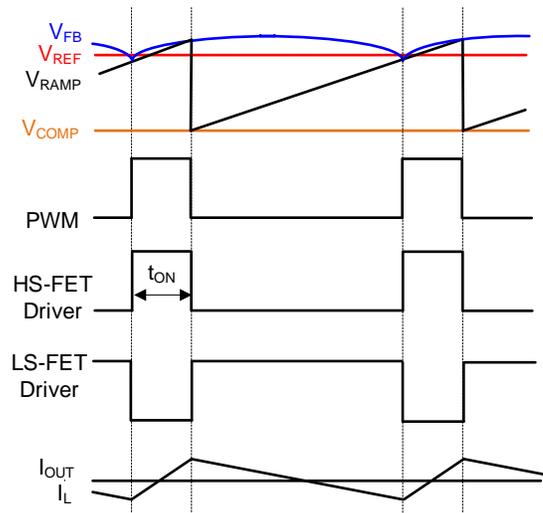


Figure 3: PWM Mode at Heavy-Loads

### Forced Continuous Conduction Mode (FCCM)

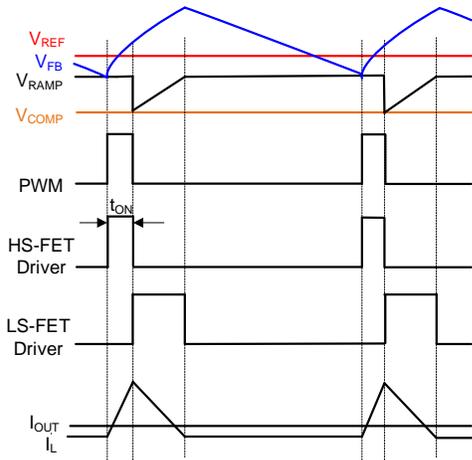
If the output current ( $I_{OUT}$ ) is high, and the inductor current ( $I_L$ ) exceeds 0A, then the part operates in forced continuous conduction mode (FCCM) (see Figure 3). The MPQ8633A-H can also be configured to operate in FCCM while  $I_{OUT}$  is low (see the Mode Selection section on page 14).

In FCCM,  $f_{SW}$  is fairly constant (PWM mode), and the  $V_{OUT}$  ripple ( $\Delta V_{OUT}$ ) remains fairly constant across the entire load range.

### Pulse-Skip Mode (PSM)

Under light-load conditions, the MPQ8633A-H can be configured to operate in pulse-skip mode (PSM) to optimize efficiency (see the Mode Selection section on page 14).  $I_L$  decreases as the load decreases. Once  $I_L$  reaches 0A, the part transitions from FCCM to PSM.

Figure 4 on page 14 shows PSM under light-load conditions.


**Figure 4: PSM at Light Loads**

If  $V_{FB}$  drops below  $V_{COMP}$ , then the HS-FET turns on for a fixed interval. Once the HS-FET turns off, the LS-FET turns on until  $I_L$  reaches 0A. In PSM,  $V_{FB}$  should not reach  $V_{COMP}$  as  $I_L$  reaches 0A. The LS-FET driver enters a high-impedance (Hi-Z) state as  $I_L$  reaches 0A. A current modulator takes control of the LS-FET and limits  $I_L$  below -1mA, and the output capacitors discharge to PGND slowly via the LS-FET. In PSM, the HS-FET does not turn on as frequently as it does in FCCM. As a result, the efficiency in PSM is higher than that in FCCM.

As  $I_{OUT}$  increases, the current modulator regulation time decreases. The HS-FET turns on more frequently, and  $f_{SW}$  increases accordingly.  $I_{OUT}$  reaches its critical level once the current modulator time is 0s. The critical level of  $I_{OUT}$  can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The part enters PWM mode once  $I_{OUT}$  exceeds its critical level. Then  $f_{SW}$  remains fairly constant across the entire  $I_{OUT}$  range.

The MPQ8633A-H can be configured to operate in FCCM while under light-load conditions (see Table 1).

### Mode Selection

The MPQ8633A-H provides both FCCM and PSM for light-load operation. It also has three selectable  $f_{SW}$  options. The MODE resistor ( $R_{MODE}$ ) selects  $f_{SW}$  and the operation

mode under light-load conditions (see Table 1).

**Table 1: Mode Selection at Light-Loads**

$R_{MODE}$	Mode	$f_{sw}$ (kHz)
Pulled to VCC	PSM	600
243k $\Omega$ ( $\pm 20\%$ ) or pulled to AGND	PSM	800
121k $\Omega$ ( $\pm 20\%$ ) or pulled to AGND	PSM	1000
Pulled to AGND	FCCM	600
30.1k $\Omega$ ( $\pm 20\%$ ) or pulled to AGND	FCCM	800
60.4k $\Omega$ ( $\pm 20\%$ ) or pulled to AGND	FCCM	1000

### Soft Start (SS)

The minimum soft-start time ( $t_{SS}$ ) is limited at 1ms.  $t_{SS}$  can be increased by adding a soft-start capacitor ( $C_{SS}$ ) between the TRK/REF and RGND pins.

$C_{SS}$  can be calculated with Equation (2):

$$C_{SS}(\text{nF}) = \frac{t_{SS}(\text{ms}) \times 36\mu\text{A}}{0.6(\text{V})} \quad (2)$$

### Output Voltage Tracking and Reference

TRK/REF is an analog input pin that can track another power supply or accept an external reference. If an external voltage signal is connected to TRK/REF, then TRK/REF acts as a reference for  $V_{OUT}$ .  $V_{FB}$  follows this external voltage signal, and the soft-start settings are ignored. The TRK/REF input signal can be between 0.3V and 1.4V. During start-up, the TRK/REF voltage ( $V_{TRK/REF}$ ) should exceed 600mV to ensure proper operation. After start-up,  $V_{TRK/REF}$  can be between 0.3V and 1.4V.

### Pre-Biased Start-Up

The MPQ8633A-H is designed for a monotonic start-up into a pre-biased load. If the output is pre-biased to a certain voltage during start-up, then the IC turns both the HS-FET and LS-FET off until  $V_{TRK/REF}$  exceeds the sensed voltage on the FB pin. If the BST voltage ( $V_{BST}$ ) drops below the 2.3V before  $V_{TRK/REF}$  exceeds the sensed voltage on the FB pin, then the LS-FET turns on to charge  $V_{BST}$  via VCC. The LS-FET turns on for very short pulses, so that the drop in the pre-biased level is negligible.

### Output Voltage Discharge

If the MPQ8633A-H shuts down through EN, then  $V_{OUT}$  discharge mode is enabled. Both the HS-FET and the LS-FET latch off, and a discharge MOSFET connected between the SW and PGND pins turns on to discharge  $V_{OUT}$ . The typical on resistance of this MOSFET is 80Ω. Once  $V_{FB}$  drops below 10% of  $V_{REF}$ , the discharge MOSFET turns off.

### Current Sense and Over-Current Protection (OCP)

The MPQ8633A-H features an on-die current sense and a configurable positive current limit ( $I_{LIMIT}$ ) threshold.

$I_{LIMIT}$  is active once the MPQ8633A-H starts up. During the LS-FET  $t_{ON}$ ,  $I_L$  is sensed by a current mirror, which generates a current output at the CS pin. The current-sense gain ( $G_{CS}$ ) ratio is the value of this current output over the actual current.

The current-sense resistor ( $R_{CS}$ ) connected between the CS and AGND pins makes the current-sense voltage ( $V_{CS}$ ) proportional to  $I_L$  cycle-by-cycle. The HS-FET turns on once  $V_{CS}$  drops below the internal over-current protection (OCP) threshold ( $V_{OCP}$ ) during the LS-FET  $t_{ON}$  to limit the inductor valley current cycle-by-cycle.

$R_{CS}$  can be calculated with Equation (3):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times \left( I_{LIMIT} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}} \right)} \quad (3)$$

Where  $V_{OCP}$  is 1.2V,  $G_{CS}$  is 20μA/A, and  $I_{LIMIT}$  is the desired current limit in amps (A).

Once the device starts up, hiccup mode is active after a delay time (3ms). If the device detects an over-current (OC) fault for 31 consecutive cycles, or if the  $V_{FB}$  drops below the under-voltage protection (UVP) threshold ( $V_{UVP}$ ), the part enters hiccup mode. In hiccup mode, the HS-FET latches off and the LS-FET latches off during zero-current detection (ZCD).  $V_{TRK/REF}$  is also discharged. After about 11ms, the MPQ8633A-H attempts to initiate an SS. If the OC fault is still present after 3ms, then the device repeats this operation until the OC fault is removed, and  $V_{OUT}$  ramps up smoothly to its regulation level.

### Negative Inductor Current Limit

If the LS-FET detects a negative current (-9A), then the LS-FET turns off for 200ns to limit the negative current.

### Output Sink Mode (OSM)

The MPQ8633A-H employs output sink mode (OSM) to regulate  $V_{OUT}$  to its targeted value. If  $V_{FB}$  exceeds 104% of  $V_{REF}$  (and is below  $V_{OVP}$ ), then the part operates in OSM. In OSM, the LS-FET remains on until the LS-FET current ( $I_{LS}$ ) reaches the negative  $I_{LIMIT}$  ( $I_{LIMIT\_NEG}$ ) (-5.5A). Once  $I_{LS}$  reaches -5.5A, the LS-FET turns off for 200ns and the HS-FET turns on. The LS-FET turns on again after 100ns. The MPQ8633A-H continues to operate in OSM until  $V_{FB}$  drops below 102% of  $V_{REF}$ . Once  $V_{FB}$  drops below 102% of  $V_{REF}$ , the MPQ8633A-H exits OSM after 15 consecutive cycles of FCCM.

### Over-Voltage Protection (OVP)

The MPQ8633A-H monitors  $V_{OUT}$  by connecting FB to the tap of the FB resistor divider. The resistor divider detects whether an over-voltage (OV) fault has occurred. This also provides hiccup mode for OVP.

If  $V_{FB}$  exceeds 116% of  $V_{REF}$ , then OVP is triggered. PGOOD is pulled down until it reaches the low-side  $I_{LIMIT\_NEG}$ . Once it reaches  $I_{LIMIT\_NEG}$ , the LS-FET turns off for 200ns, and the HS-FET turns on for the LS-FET  $t_{OFF}$ . After 200ns, the LS-FET is turned on again. The MPQ8633A-H continues this operation to try to discharge the excessive voltage on the output. The part exits OVP discharge mode once  $V_{FB}$  drops below 105% of  $V_{REF}$ .

### Thermal Shutdown

The IC monitors the junction temperature ( $T_J$ ) internally. If  $T_J$  exceeds the thermal shutdown threshold (typically 160°C), then the converter shuts down, and the TRK/REF capacitors are discharged. Once  $T_J$  drops below 130°C, the IC initiates an SS to resume normal operation. There is about 30°C hysteresis. Thermal shutdown is a non-latch protection.

### Output Voltage Setting and Remote Output Voltage Sensing

Choose a value for R1. Then R2 can be calculated with Equation (4) on page 16:

$$R2(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1(k\Omega) \quad (4)$$

Connect a feed-forward capacitor ( $C_{FF}$ ) in parallel with  $R1$  to improve load transient response.  $R1$  and  $C_{FF}$  add an extra zero to the system, which improves loop response.  $R1$  and  $C_{FF}$  are selected so that the zero formed by  $R1$  and  $C_{FF}$  is between 20kHz and 60kHz. The zero ( $f_{ZERO}$ ) can be calculated with Equation (5):

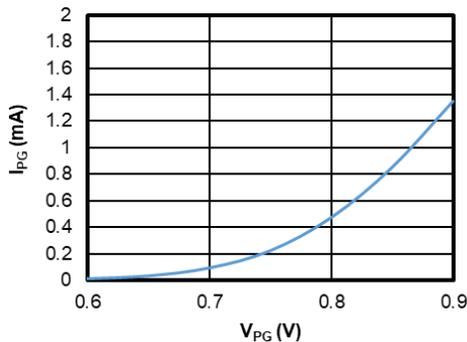
$$f_{ZERO} = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (5)$$

### Power Good (PG)

The PGOOD pin is a power good (PG) output. PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source (<3.6V) via a pull-up resistor (e.g. 10kΩ). Once  $V_{IN}$  is applied, the MOSFET turns on, and PGOOD is pulled to AGND before TRK/REF is ready. Once  $V_{FB}$  exceeds 92.5% of  $V_{REF}$ , PGOOD is pulled high after a delay time (0.8ms).

If  $V_{FB}$  drops below 80% of  $V_{REF}$  or exceeds 116% percent of  $V_{REF}$ , then PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If  $V_{IN}$  fails to power the MPQ8633A-H, then PGOOD is clamped low regardless of whether it is tied to an external DC source via a pull-up resistor. Figure 5 shows the relationship between the PGOOD voltage ( $V_{PG}$ ) and the PGOOD pull-up current ( $I_{PG}$ ).



**Figure 5: Clamped  $V_{PG}$  vs.  $I_{PG}$**

### Enable (EN) Configuration

The EN pin is an input signal that turns the MPQ8633A-H on and off. Pull EN high to turn the converter on; pull EN low to turn it off. Do not float EN. EN can be driven by an analog or digital control logic signal to enable and disable the device.

The MPQ8633A-H provides accurate EN thresholds. A resistor divider between the  $V_{IN}$  and AGND pins can be used to configure the start-up  $V_{IN}$  ( $V_{IN\_SU}$ ).

This is highly recommended for applications without a dedicated EN control logic signal to avoid  $V_{EN}$  from bouncing between the EN UVLO rising and falling thresholds during start-up and shutdown.  $V_{IN\_SU}$  can be calculated with Equation (6):

$$V_{IN\_SU}(V) = V_{EN\_RISING} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (6)$$

Where  $V_{EN\_RISING}$  is 1.22V.

Choose  $R_{UP}$  and  $R_{DOWN}$  so that  $V_{EN}$  does not exceed 3.6V once  $V_{IN}$  reaches its maximum value.

EN can also be connected to  $V_{IN}$  via a pull-up resistor ( $R_{UP}$ ). Choose  $R_{UP}$  so that the maximum EN current ( $I_{EN\_MAX}$ ) is 50μA.  $R_{UP}$  can be calculated with Equation (7):

$$R_{UP}(k\Omega) = \frac{V_{IN\_MAX}(V)}{0.05(mA)} \quad (7)$$

## APPLICATION INFORMATION

### Selecting the Input Capacitor ( $C_{IN}$ )

The step-down converter has a discontinuous input current ( $I_{IN}$ ), and requires a capacitor to supply AC current to the step-down converter while maintaining the DC  $V_{IN}$ . Use ceramic capacitors for the best performance. Place the input capacitors as close to the  $V_{IN}$  pin as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R dielectrics are recommended due to their stable temperature characteristics and low ESR.

The input capacitors should have a ripple current rating that exceeds the converter's maximum input ripple current ( $I_{CIN\_MAX}$ ). The input ripple current ( $I_{CIN}$ ) can be estimated with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (8)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor ( $C_{IN}$ ) with an RMS current rating that exceeds half the maximum load current ( $I_{LOAD\_MAX}$ ).  $C_{IN}$  determines the converter's  $V_{IN}$  ripple ( $\Delta V_{IN}$ ). If there is a  $\Delta V_{IN}$  requirement in the system, then select  $C_{IN}$  to meet the system's specification.

$\Delta V_{IN}$  can be calculated with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (11)$$

### Selecting the Output Capacitor ( $C_{OUT}$ )

The output capacitor ( $C_{OUT}$ ) maintains the DC  $V_{OUT}$ . Use POSCAP or ceramic capacitors for

the best performance. The  $V_{OUT}$  ripple ( $\Delta V_{OUT}$ ) can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (12)$$

When using ceramic capacitors, the capacitance dominates the impedance at  $f_{SW}$ . The capacitance also dominates  $\Delta V_{OUT}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (13)$$

When using POSCAP capacitors, the ESR dominates the impedance at  $f_{SW}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (14)$$

### Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching  $V_{IN}$ . A larger-value inductor results in less ripple current and a lower  $\Delta V_{OUT}$ ; however, a larger-value inductor has a larger physical size, a higher series resistance, and a lower saturation current. Choose an inductor so that the peak-to-peak inductor ripple current ( $\Delta I_L$ ) is between 30% and 40% of the maximum output DC load current. The peak inductor current ( $I_{L\_PEAK}$ ) should be below the maximum output DC load current. The inductance ( $L$ ) can be calculated with Equation (15):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (15)$$

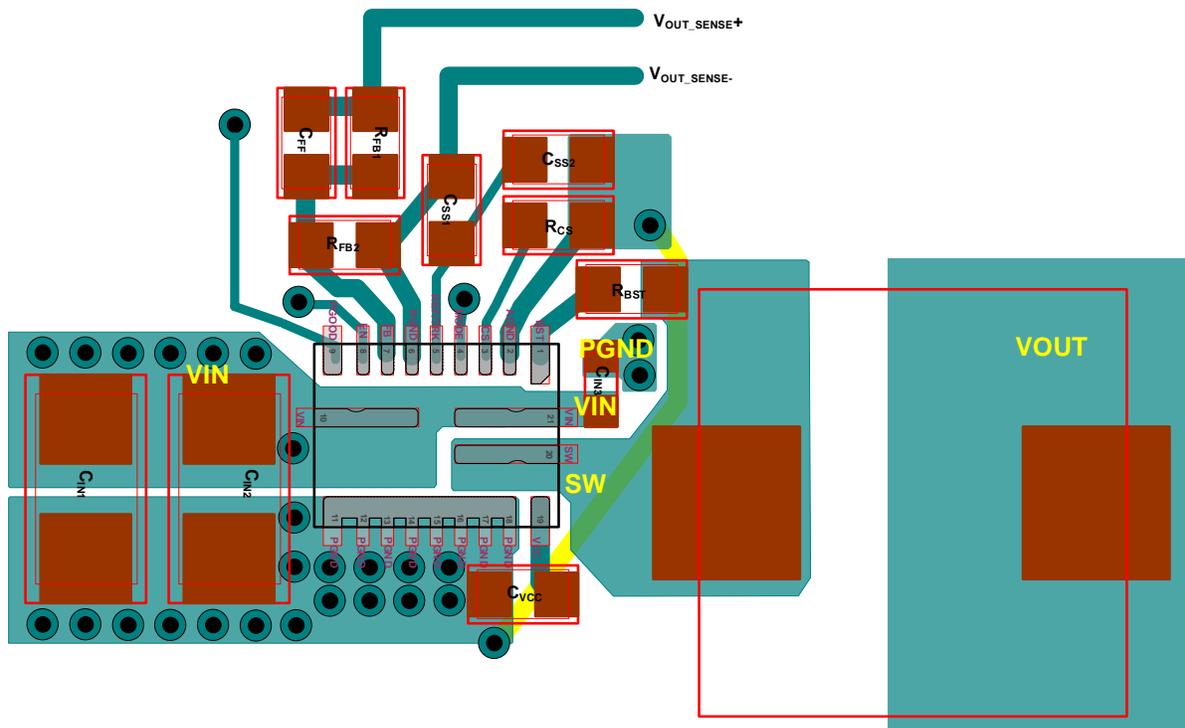
Choose an inductor that will not saturate under the maximum  $I_{L\_PEAK}$ .  $I_{L\_PEAK}$  can be calculated with Equation (16):

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (16)$$

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 6 and follow the guidelines below:

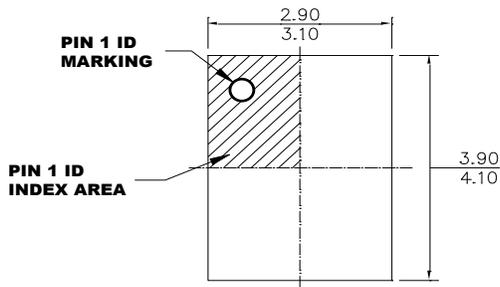
1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Place the major MLCC capacitors on the same layer as the IC.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Connect a  $\geq 1\mu\text{F}$  capacitor (0402) to VIN on the right side of the IC. VIN is extended to the right to connect this capacitor.
5. Place two or more 20mil/10mil vias on the inner solid ground plane. Place these via on the ground side of the capacitor.
6. Place multiple vias as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
7. Place the VCC decoupling capacitor close to the IC.
8. Connect the AGND and PGND pins at the point of the VCC capacitor's ground connection.
9. Place a  $0.1\mu\text{F}$  to  $1\mu\text{F}$  BST capacitor as close to the BST and SW pins as possible.
10. Route the BST path using  $\geq 20\text{mil}$  trace width.
11. Place the TRK/REF capacitor close to the TRK/REF and RGND pins.
12. If a via must be placed on the PGOOD pad, place it at least 10mm away from the positive side of the first input decoupling capacitor. Place this via close to the IC.



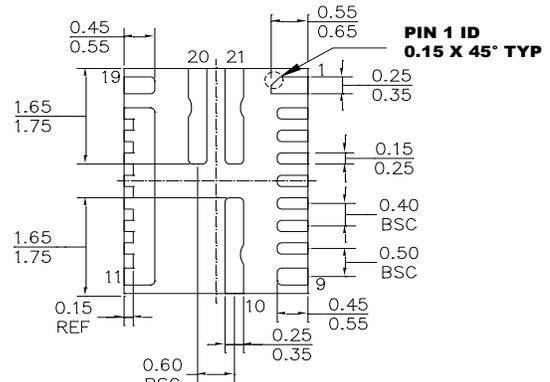
**Figure 6: Recommended PCB Layout**

# PACKAGE INFORMATION

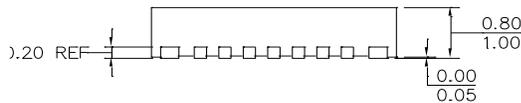
## QFN-21 (3mmx4mm)



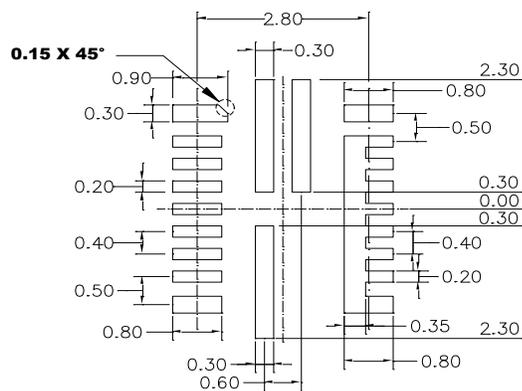
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

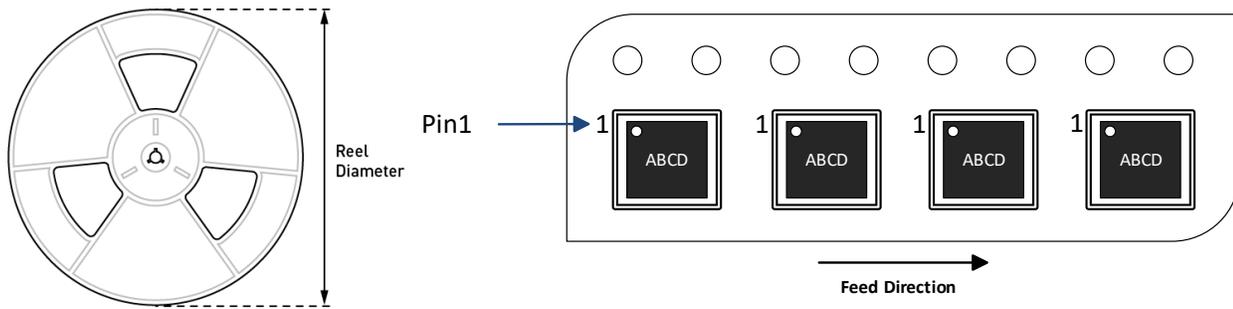


**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

### CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ8633A-HGLE-Z	QFN-21 (4mmx3mm)	5000	N/A	13in	12mm	8mm



## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/19/2022	Initial Release	-

**Notice:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Monolithic Power Systems \(MPS\):](#)

[MPQ8633A-HGLE-P](#) [MPQ8633A-HGLE-Z](#)