MPM3650C

1.2MHz, Synchronous, 2.75 to 17V, 6A, Ultra-Thin Power Module

DESCRIPTION

The MPM3650C is a fully integrated, high-frequency, synchronous, rectified, step-down power module with an internal inductor. It offers a highly compact solution to achieve 6A of continuous output current over a wide input range, with excellent load and line regulation. The MPM3650C offers synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides ultra-fast transient response and easy loop design, as well as very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MPM3650C requires a minimal number of readily available, standard external components. It is available in a space-saving QFN-24 (4mmx6mm) package.

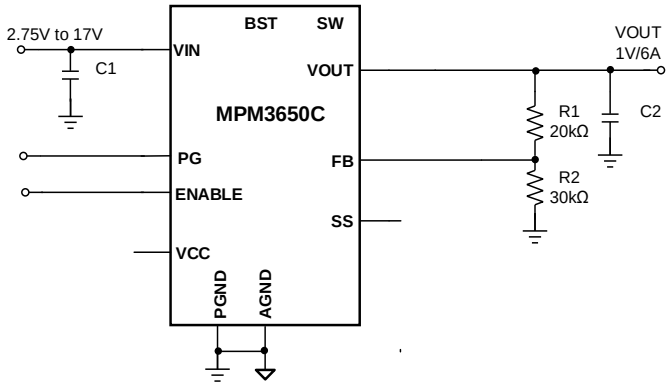
FEATURES

- Wide 2.75V to 17V Operating Input Range
- Output Currents:
  - 0.6V to 1.8V, 6A Output
  - 1.8V to 3.3V, 5A Output
- Internal Power MOSFETs
- Output Adjustable from 0.6V
- High-Efficiency Synchronous Mode Operation
- Forced CCM for Low V_{OUT} Ripple
- Supports Pre-Biased Start-Up
- Fixed 1200kHz Switching Frequency
- Externally Programmable Soft-Start Time
- EN and Power Good for Power Sequencing
- Over-Current Protection and Hiccup Mode
- Thermal Shutdown
- Available in a QFN-24 (4mmx6mmx1.6mm) package

APPLICATIONS

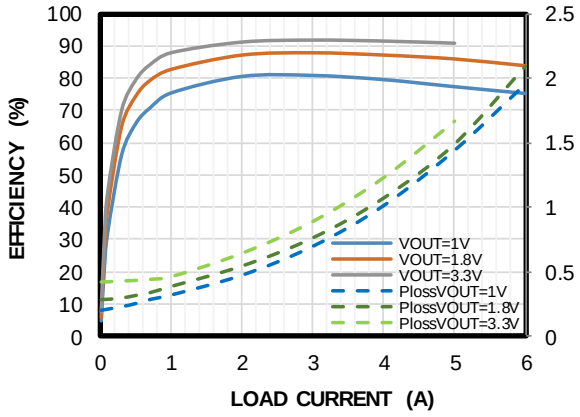
- FPGA Power Systems
- Optical Modules
- Telecom
- Networking
- Industrial Equipment

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{IN} = 12V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3650CGQW	QFN-24 (4mmx6mmx1.6mm)	*See Below*	3

* For Tape & Reel, add suffix –Z (e.g. MPM3650CGQW–Z).

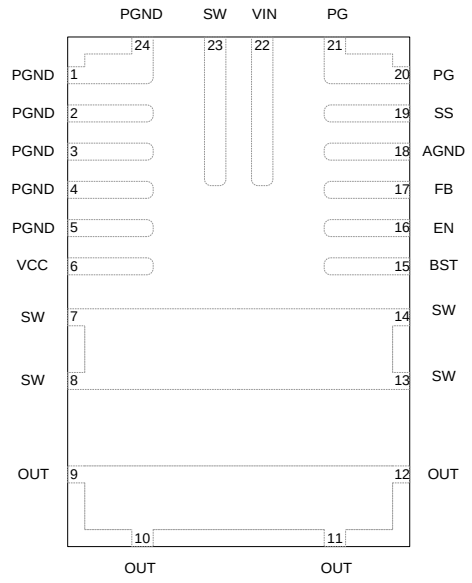
TOP MARKING

MPSYWW
M3650C
LLLLLL
M

MPS: MPS prefix
Y: Year code
WW: Week code
M3650C: Part number
LLLLLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



QFN-24 (4mmx6mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 4, 5, 24	PGND	**System ground.** This pin is the reference ground of the regulated output voltage. Because of this, extra care must be taken when designing the PCB layout. It is recommended to connect this pin to GND with copper pours and vias.
6	VCC	**Internal bias supply output.**
7, 8, 13, 14, 23	SW	**Switch output**. Float the SW pins.
9, 10, 11, 12	OUT	**Output pin.** Connect to this pin to the output capacitor (C_{OUT}).
15	BST	**Bootstrap**. Float the BST pin.
16	EN	**Enable.** Pull EN high to enable the part. When floating, EN is pulled down to GND by internal 1.2MΩ resistor so it is disabled.
17	FB	**Feedback**. Sets the output voltage when connected to the tap of an external resistor divider that is connected between output and GND.
18	AGND	**Signal ground.** AGND is not internally connected to System Ground, make sure AGND connected to system Ground in PCB layout.
19	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid start up inrush current. This pin includes an internal 22nF SS capacitor.
20, 21	PG	**Power good output**. The output of this pin is an open drain output. It will change state if under-voltage protection (UVP), over-current protection (OCP), over-temperature protection (OTP) or an over-voltage (OV) happens.
22	VIN	**Supply voltage**. The part operates from a 2.75V to 17V input rail. Use a 0402 size, 0.1µF input capacitor to decouple the input rail. Use wide PCB trace to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +20V
V_{SW} ..... -0.3V (-5V<10ns) to + V_{IN} + 0.7V (23V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
All other pins .....-0.3V to + 4V
Continuous power dissipation ..... (T_A = 25℃) (2) 3.816W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +125°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM).....2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.75V to 17V
Output voltage (V_{OUT})..... 0.6V to 3.3V
Operating junction temp..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVM3650C-QW-00A (4)……32.75...10.217 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation on EVM3650C-QW-00A board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVM3650C-QW-00A, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C [5], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.75		17	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2	5	µA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	µA
MOSFET						
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 7V			5	µA
Current Limit						
Valley current limit	I_{LIMIT_VY}		6	7		A
Short hiccup duty cycle [6]	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		0.9	1.2	1.6	MHz
Minimum on time [6]	t_{ON_MIN}			50		ns
Minimum off time [6]	t_{OFF_MIN}			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	µA
Enable and UVLO						
EN rising threshold	V_{EN_RISING}		1.19	1.23	1.27	V
EN falling threshold	$V_{EN\_FALLING}$		0.96	1	1.04	V
EN pin pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout (UVLO) rising threshold	VCC_{Vth}		2.4	2.5	2.6	V
VCC UVLO threshold	VCC_{HYS}			200		mV
VCC regulator	V_{CC}	V_{IN} = 5V		3.5		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good under-voltage (UV) rising threshold	$PGUV_{VTH\_HI}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{VTH\_LO}$		0.75	0.80	0.85	V_{FB}
Power good over-voltage (OV) rising threshold	$PGOV_{VTH\_HI}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{VTH\_LO}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{TD}	Both edge		50		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	T_{SD-HYS}			20		°C

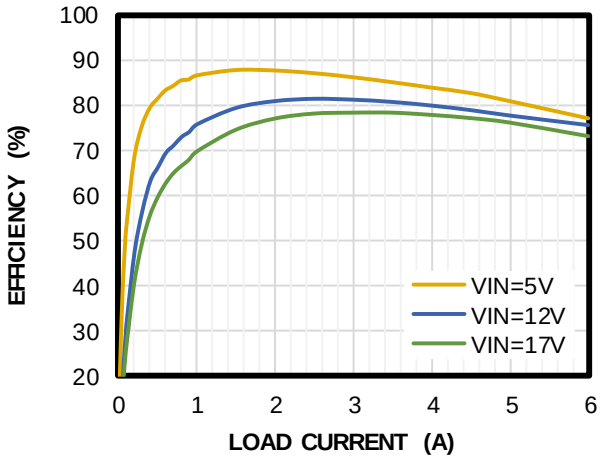
Notes:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization testing.

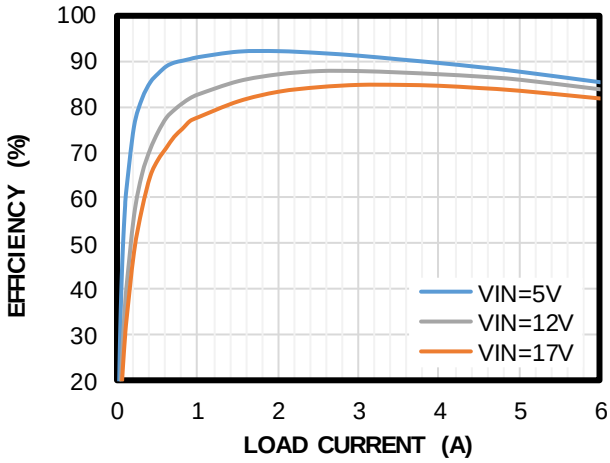
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

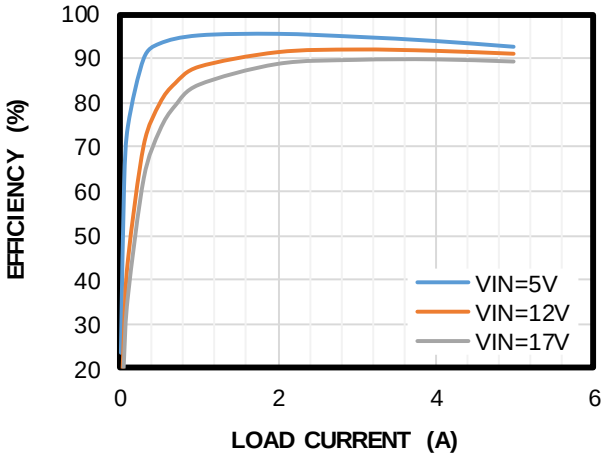
Efficiency vs. Load Current
V_{OUT} = 1V



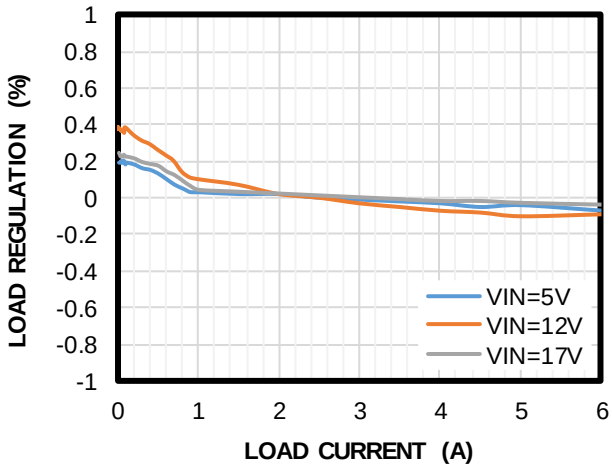
Efficiency vs. Load Current
V_{OUT} = 1.8V



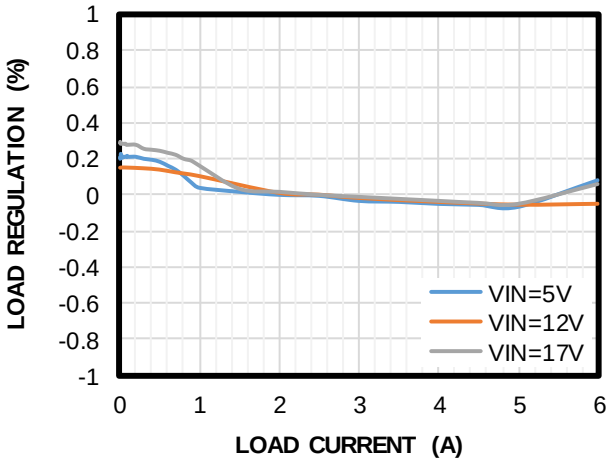
Efficiency vs. Load Current
V_{OUT} = 3.3V



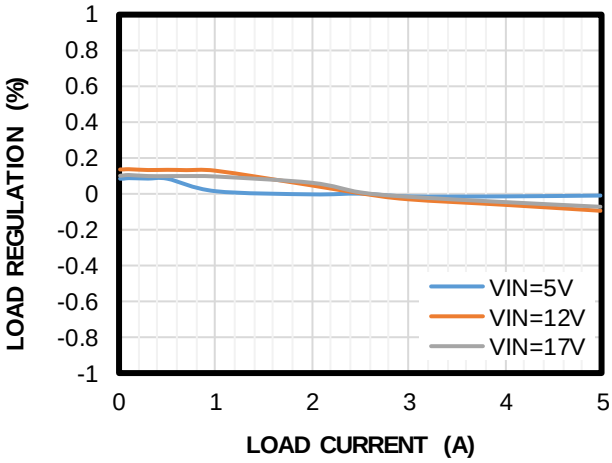
Load Regulation
V_{OUT} = 1V



Load Regulation
V_{OUT} = 1.8V



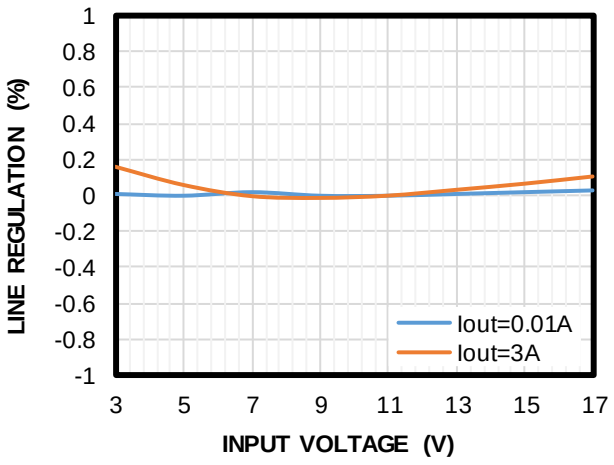
Load Regulation
V_{OUT} = 3.3V



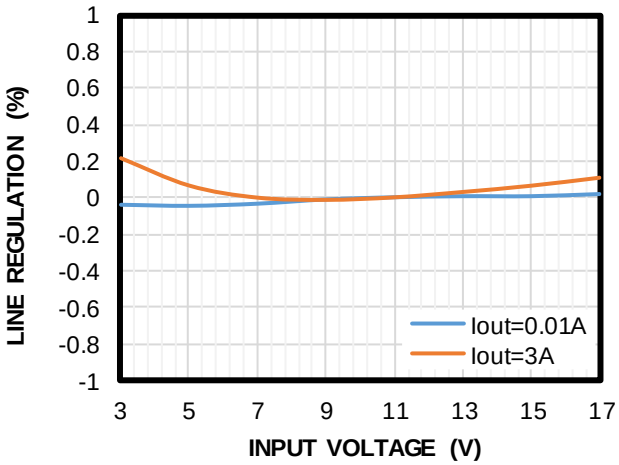
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

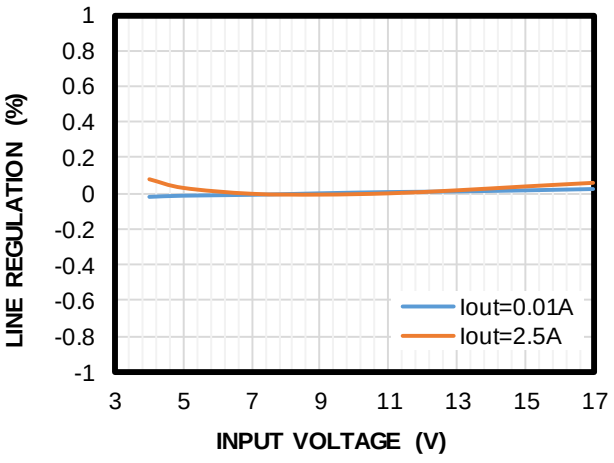
Line Regulation
V_{OUT} = 1V



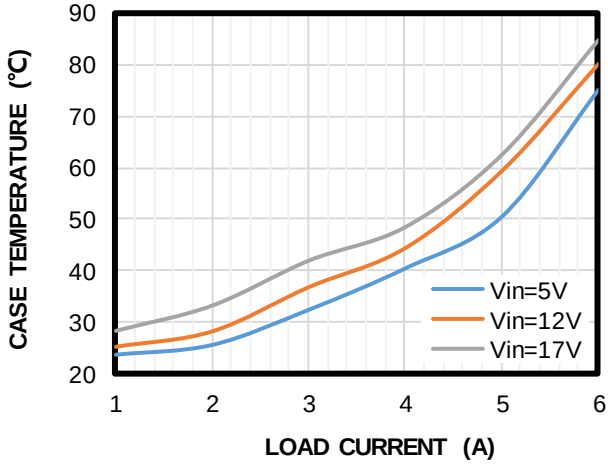
Line Regulation
V_{OUT} = 1.8V



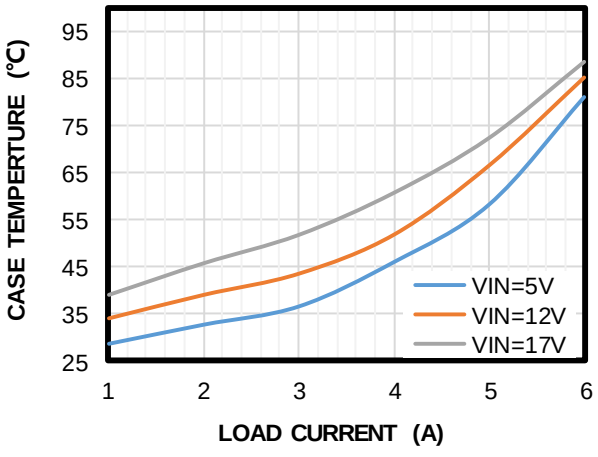
Line Regulation
V_{OUT} = 3.3V



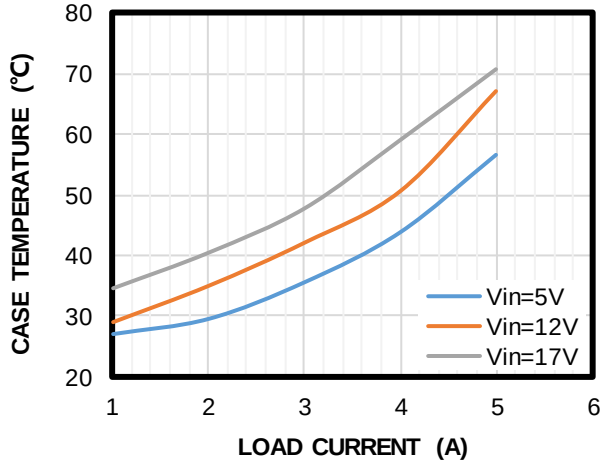
Case Temperature vs. Load Current
V_{OUT} = 1V, T_A = 15°C



Case Temperature vs. Load Current
V_{OUT} = 1.8V, T_A = 15°C



Case Temperature vs. Load Current
V_{OUT} = 3.3V, T_A = 15°C

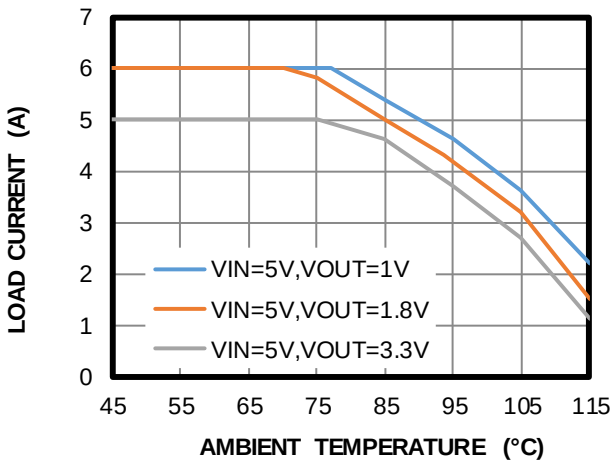


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

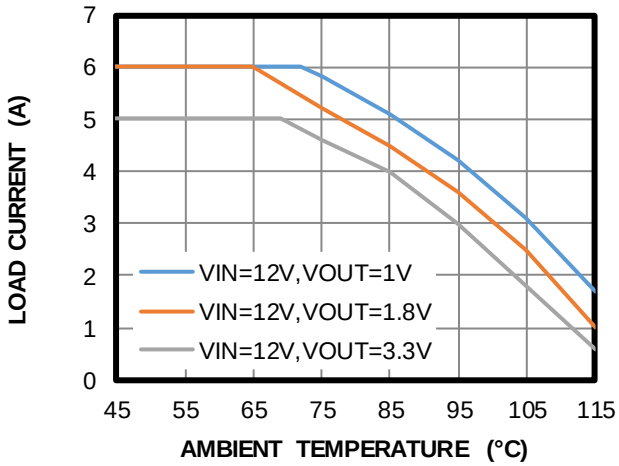
Thermal Derating

V_{IN} = 5V, no airflow



Thermal Derating

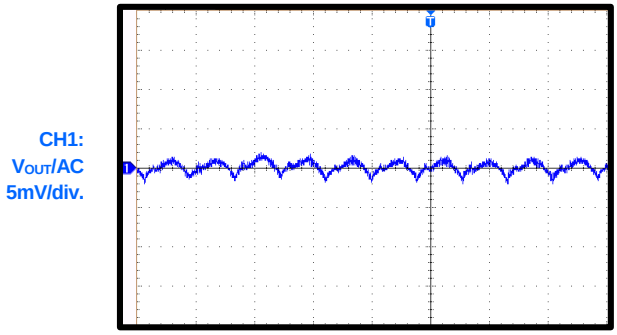
V_{IN} = 12V, no airflow



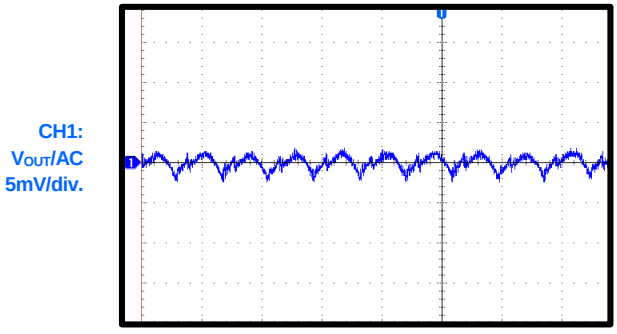
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

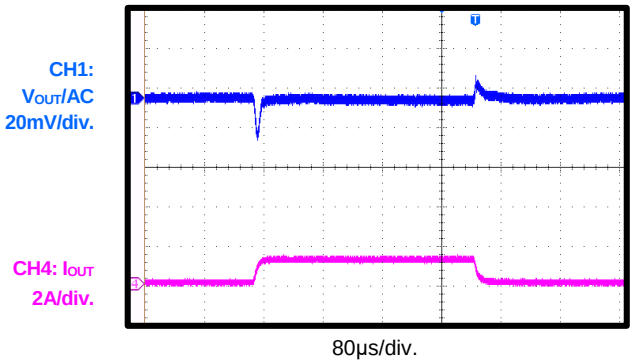
V_{OUT} Ripple
I_{OUT} = 0A



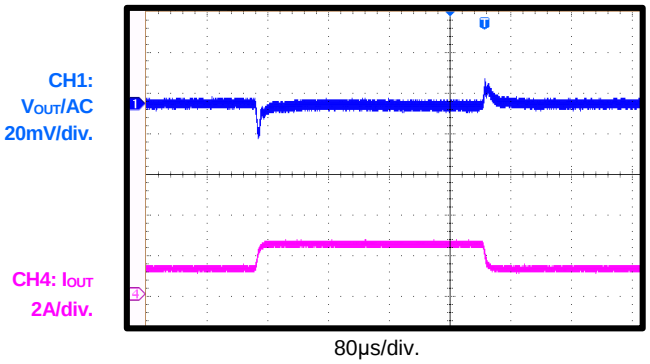
V_{OUT} Ripple
I_{OUT} = 6A



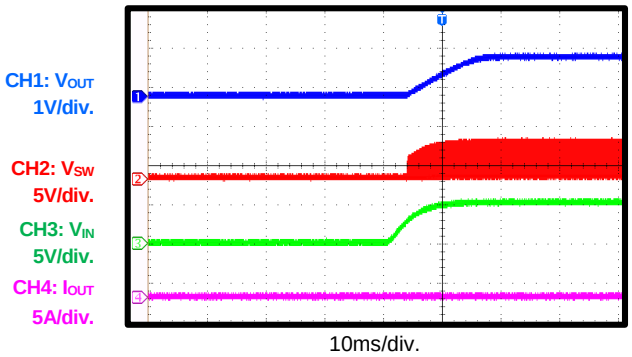
Load Transient
I_{OUT} = 0A to 3A



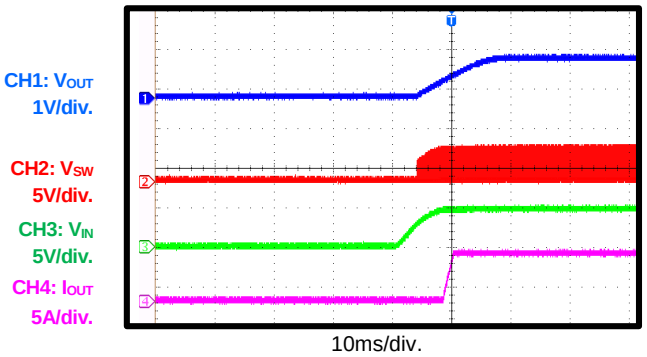
Load Transient
I_{OUT} = 3A to 6A



Start-Up through VIN
I_{OUT} = 0A



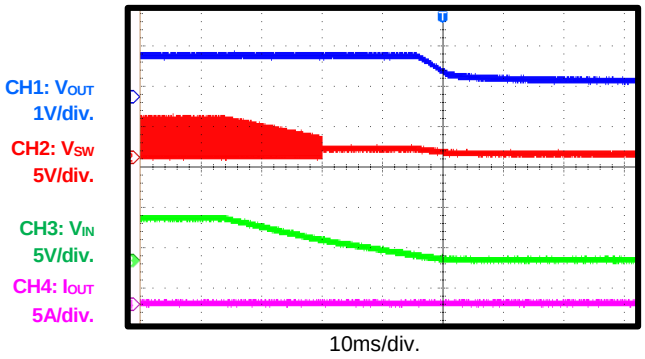
Start-Up through VIN
I_{OUT} = 6A



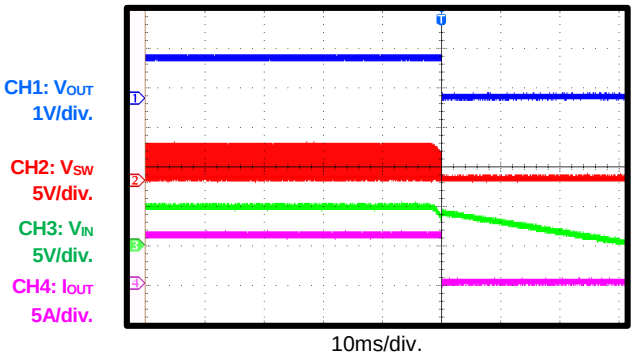
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

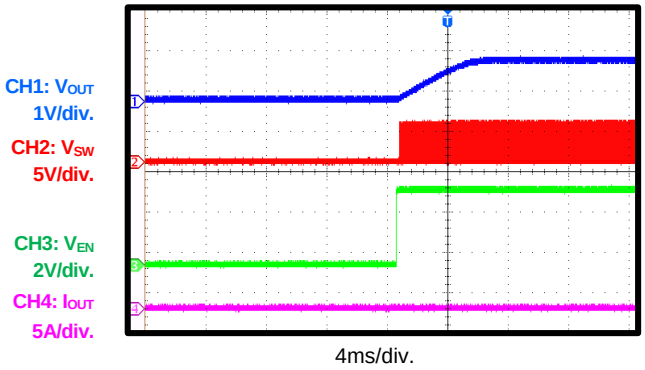
Shutdown through VIN
I_{OUT} = 0A



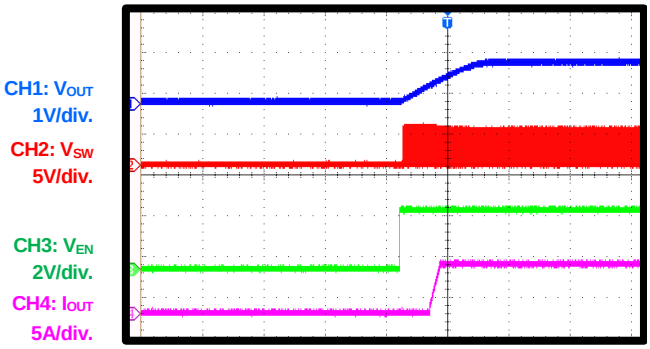
Shutdown through VIN
I_{OUT} = 6A



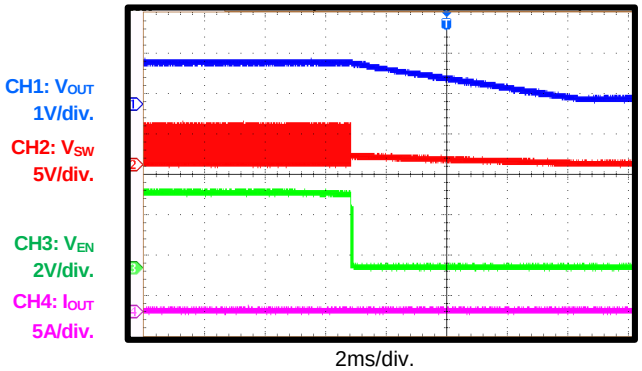
Start-Up through EN
I_{OUT} = 0A



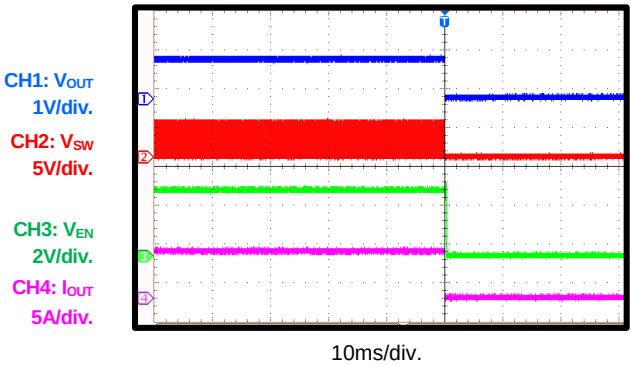
Start-Up through EN
I_{OUT} = 6A



Shutdown through EN
I_{OUT} = 0A



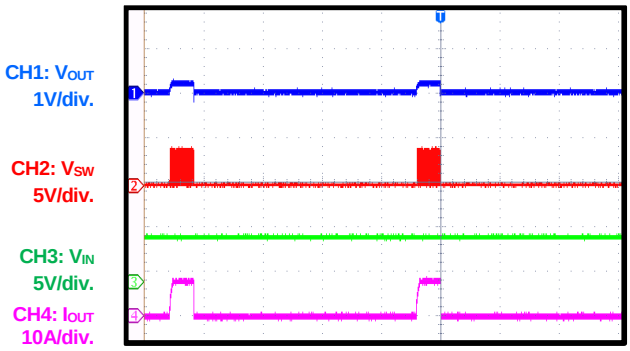
Shutdown through EN
I_{OUT} = 6A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

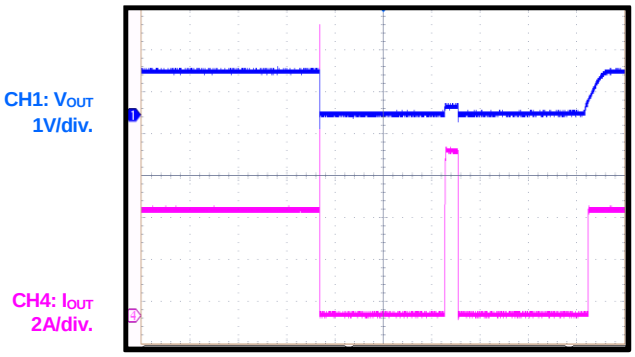
V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

Steady State



20ms/div.

SCP Entry and Recovery



200ms/div.

FUNCTIONAL BLOCK DIAGRAM

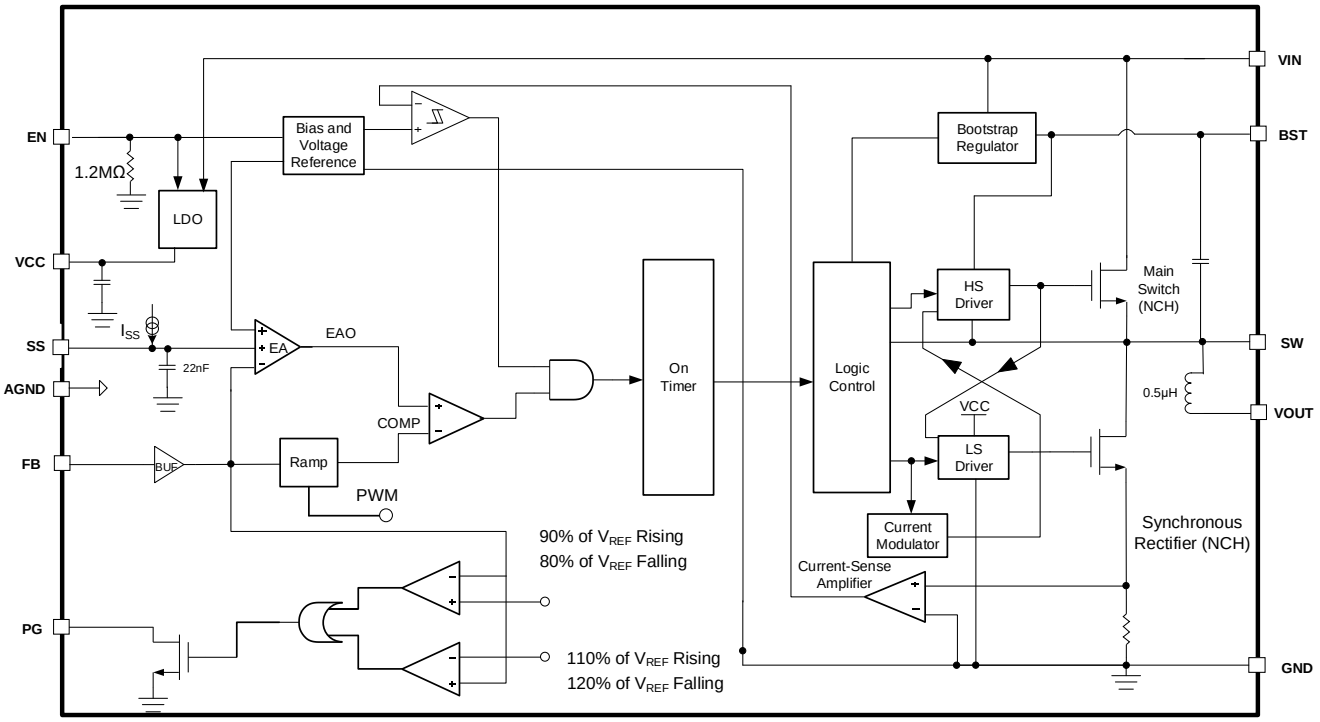


Figure 1: Functional Block Diagram

OPERATION

The MPM3650C is a fully integrated, synchronous, rectified, step-down power module. Constant-on-time (COT) control provides fast transient response and easy loop stabilization. Figure 2 shows the MPM3650C's simplified ramp compensation block.

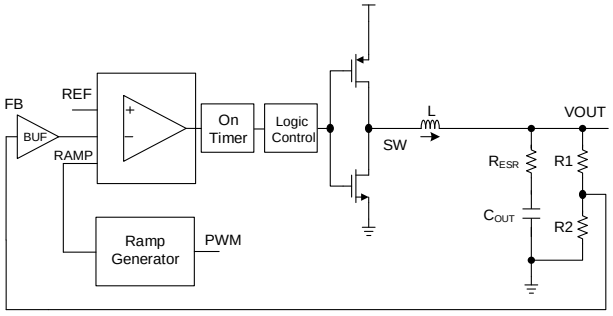


Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage (V_{OUT}) and the input voltage (V_{IN}), in order to make the switching frequency fairly constant across the entire input voltage range.

After the on period elapses, the HS-FET turns off. Once V_{FB} drops below V_{REF}, it turns on again. By repeating this operation, the device regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off, to minimize conduction loss. If both the HS-FET and LS-FET are on at the same time, a dead short occurs between input and GND. This is called shoot-through. In order to avoid shoot-through, a dead time (DT) is internally generated between the HS-FET off period and LS-FET on period, and vice versa.

Internal compensation is applied during COT control to ensure stable operation even when ceramic capacitors are being used as the output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

Forced Continuous Conduction Mode (FCCM)

The MPM3650C works in forced continuous conduction mode (FCCM). Figure 3 shows FCCM operation.

When V_{FB} is below V_{EAO}, the HS-FET turns on for a fixed interval, which is determined by the one-shot on-timer. When the HS-SFET turns off, the LS-FET turns on and remains on until the next period.

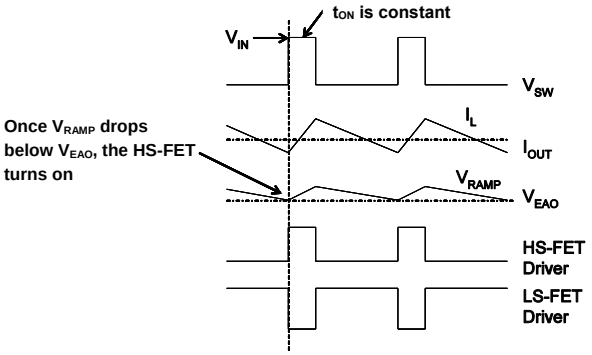


Figure 3: FCCM Operation

During FCCM operation, the switching frequency (f_{SW}) is fairly constant. This constant f_{SW} during FCCM is called pulse-width modulation (PWM) mode.

VCC Regulator

The 3.5V internal regulator power most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 3.5V, the output of the regulator is in full regulation; when V_{IN} falls below 3.5V, the output of the regulator decreases following V_{IN}. The device includes an internal, 1μF decoupling ceramic capacitor.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.23V to turn the regulator on; drive it below 1V to turn it off.

When left floating, EN is pulled down to GND by an internal 1.2MΩ resistor.

EN can be connected directly to V_{IN}. It supports an input voltage range up to 17V.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the MPM3650C from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator VCC. The VCC UVLO rising threshold is about 2.5V, and its falling threshold is about 2.3V.

Once V_{IN} exceeds the UVLO rising threshold voltage, the MPM3650C starts up. Once V_{IN} falls below the UVLO falling threshold voltage, the device shuts down. This is a non-latch protection.

Soft Start

The MPM3650C employs a soft start (SS) mechanism to ensure smooth output ramping during start-up. When the EN pin goes high, an internal, 6μA current source charges the SS capacitor. When the device is on, EN is on, and $V_{SS} < V_{REF}$, then the SS voltage (V_{SS}) takes over V_{REF} to the PWM comparator. V_{OUT} smoothly ramps up with V_{SS}. Once V_{SS} exceeds V_{REF}, it continues to ramp up until $V_{SS} = V_{REF}$, at which point V_{REF} takes over. At this point, soft start finishes and the MPM3650C enters steady state operation.

The SS capacitor value can be calculated with Equation (1):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

The MPM3650C has an internal, 22nF soft start capacitor. If the output capacitance is a large value, it is not recommended to set the soft-start time (t_{SS}) too short, or else the device could too easily reach the current limit during SS. See the EVB datasheet for further details.

Power Good (PG) Indicator

The PG pin is the open drain of a MOSFET that connects to VCC or another voltage source through a resistor (e.g. 100kΩ). If V_{IN} is applied so that the PG pin is pulled to GND before SS completes, then the MOSFET turns on. After the FB voltage (V_{FB}) reaches 90% of V_{REF}, there is a 50μs delay and the PG pin is pulled high. When V_{FB} drops to 80% of V_{REF}, the PG pin is pulled low.

If UVLO or over-temperature protection (OTP) occurs, the PG pin is pulled low immediately. If an over-current (OC) condition occurs and V_{FB} drops below 80% of V_{REF}, PG is pulled low after a 0.05ms delay. If an over-voltage (OV) condition occurs and V_{FB} exceeds 120% of V_{REF}, PG is pulled low after a 0.05ms delay. If V_{FB} returns to back below 110% of V_{REF}, there is a 0.05ms delay and then PG is pulled high.

If the input supply fails to power the MPM3650C, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. Figure 4 shows the relationship between the PG voltage and the pull-up current.

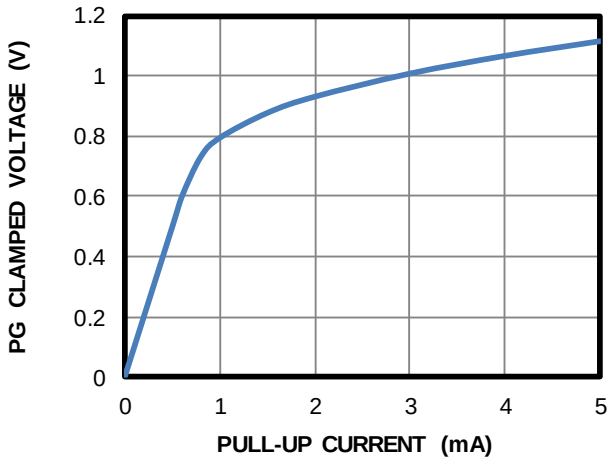


Figure 4: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM3650C offers valley limit control. The LS-FET monitors the current flow through itself. The HS-FET waits until the valley current limit does not trigger before turning on again. Meanwhile, V_{OUT} drops until V_{FB} is below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MPM3650C enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device tries to recover from an OC fault using hiccup mode. OCP includes short-circuit protection (SCP). The MPM3650C disables the output power stage, discharges the soft-start capacitor, then automatically tries to soft start again. If the OC condition still remains after soft start ends, the device repeats this operation cycle until the OC condition disappears and the output rises to the regulation level again. OCP is a non-latch protection.

Pre-Biased Start-Up

The MPM3650C is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up and the BST voltage is refreshed and charged, then the soft-start capacitor's voltage is also charged.

If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor's voltage exceeds the sensed output voltage at the FB pin, the part begins normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the MPM3650C shuts down. When the temperature falls back below its lower threshold (typically 130°C), the chip is enabled again.

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. The shutdown procedure first blocks the signaling path to avoid any fault triggering, then the internal supply rail is pulled down.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage. First, choose a value for R2. Too small of an R2 value leads to considerable quiescent current loss, while too large an R2 value makes FB noise sensitive. It is recommended to choose an R2 value within 2kΩ and 100kΩ. Typically, set the current going through R2 to be less than 250μA for balance system stability and minimize load loss. Calculate R1 with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

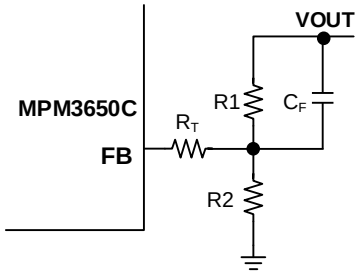


Figure 5: Feedback Network

Table 1 shows recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)	CF (pF)	RT (Ω)
1.0	20	30	39	0
1.2	20	20	39	0
1.5	20	13	39	0
1.8	20	10	39	0
2.5	20	6.34	39	0

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and therefore requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the converter's input voltage ripple. If there is an input voltage ripple requirement for the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculate with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor must be able to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

In addition to accounting for the output ripple, a larger-value output capacitor provides better load transient response. However, if the output capacitor value is too great, the output voltage is unable to reach the design value during the soft-start time, and the device will fail to regulate. The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (10):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{SS} is the soft-start time.

PCB Layout Guidelines [7]

Efficient PCB layout is crucial for stable device operation. A 4-layer layout is recommended to achieve better thermal performance. For the best results, refer to Figure 6 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Connect a large ground plane directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure the high-current paths at PGND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor, as close to the VIN and PGND pins as possible to minimize high-frequency noise.
5. Keep the paths between the input capacitor and IN as short and wide as possible.
6. Place a VCC decoupling capacitor close to the MPM3650C, and connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Connect VIN, VOUT, and PGND to a large copper area to improve thermal performance and long-term reliability.
8. Separate the input PGND area from the other PGND areas on the top layer, and connect them together at the internal layers and bottom layer with multiple vias.
9. Ensure that there is a complete GND plane at either the internal layer or the bottom layer.
10. Ensure that any signal trace is placed far away from SW.
11. Use multiple vias to connect the power planes to internal layers.

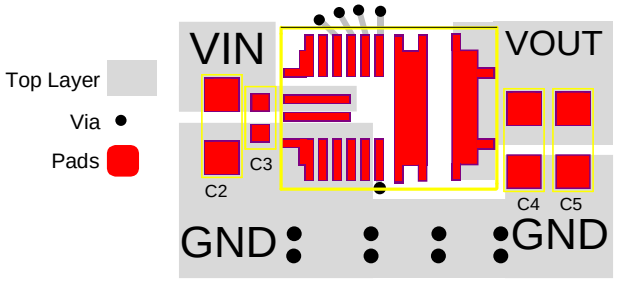


Figure 6: Recommended PCB Layout

Note:

7) The recommended layout is based on Figure 7 (see the Typical Application Circuits section on page 18).

TYPICAL APPLICATION CIRCUITS

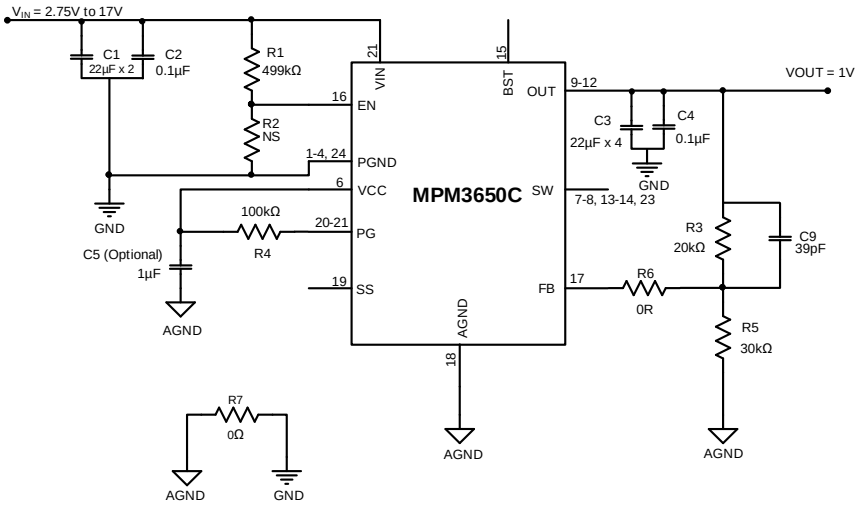


Figure 7: Typical Application Circuit with a 1V Output

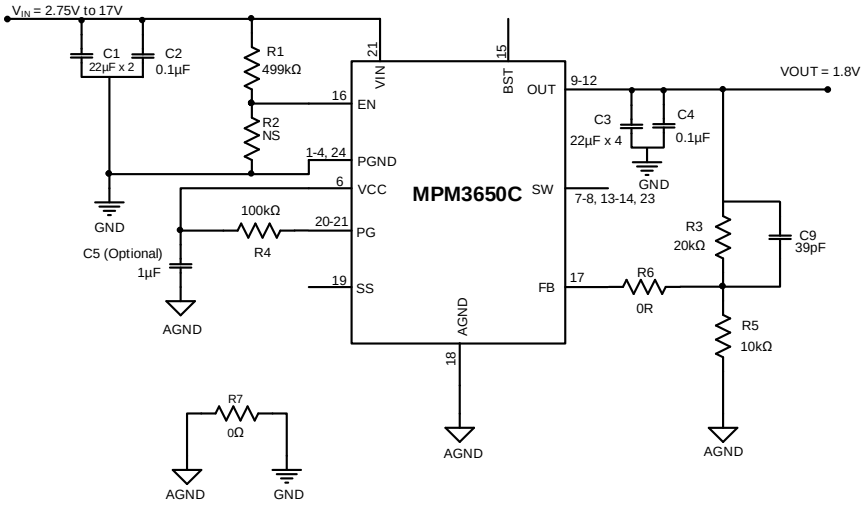


Figure 8: Typical Application Circuit with a 1.8V Output

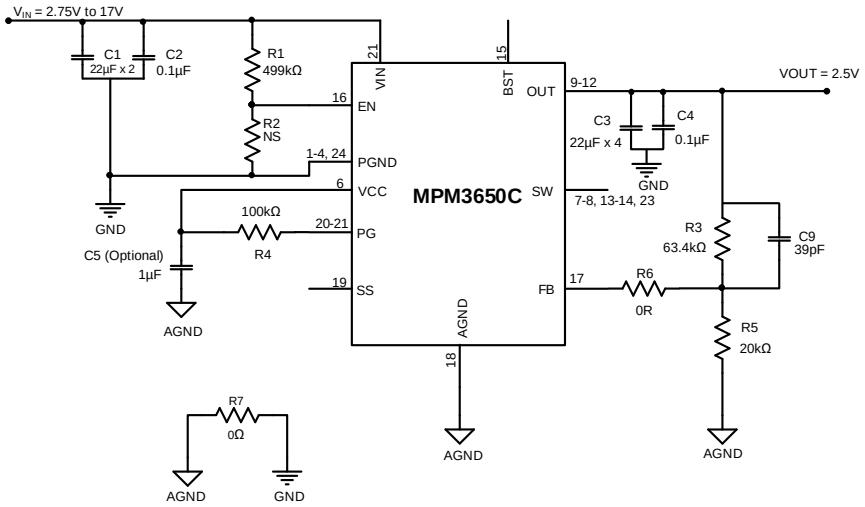
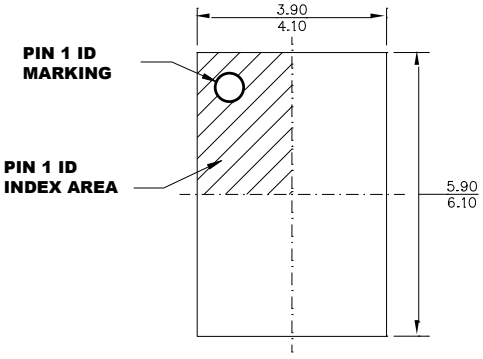


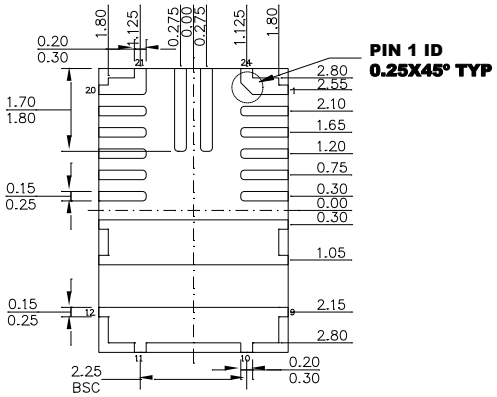
Figure 9: Typical Application Circuit with a 2.5V Output

PACKAGE INFORMATION

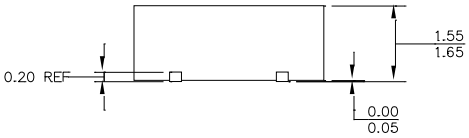
QFN-24 (4mmx6mmx1.6mm)



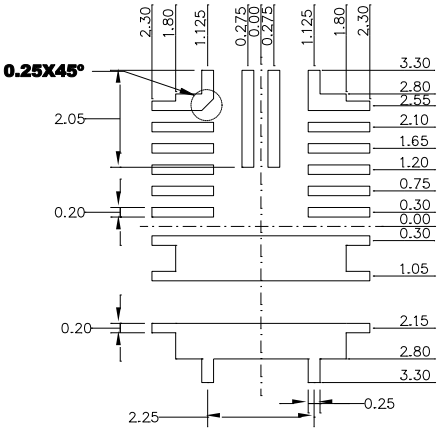
TOP VIEW



BOTTOM VIEW



SIDE VIEW

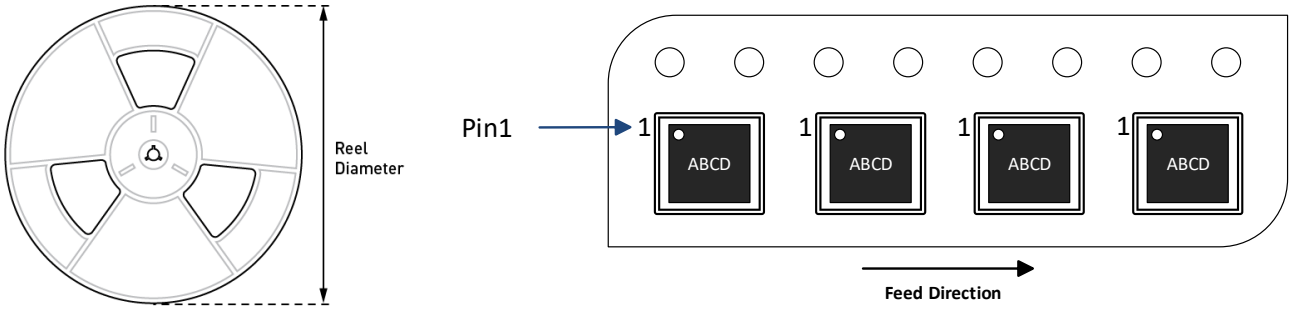


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3650CGQW–Z	QFN-24 (4mmx6mmx1.6mm)	2500	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/22/2020	Initial Release	-

Mouser Electronics

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Monolithic Power Systems (MPS):

MPM3650CGQW-P MPM3650CGQW-Z