MPM3612

3V to 22V Input, 1A, Ultra-Low 5µA I_Q Power Module in an LGA Package

DESCRIPTION

The MPM3612 is a synchronous, rectified, step-down, switch-mode power module with built-in internal power MOSFETs and high light-load efficiency. The MPM3612 has an ultra-low 5µA quiescent current (I_Q). The MPM3612 offers a very compact solution that can achieve up to 1A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input supply range.

The MPM3612 switching edge is optimized for EMI reduction. Constant-on-time (COT) control enables seamless mode transition and fast load transient response.

Protection features include over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

The MPM3612 requires a minimal number of readily available, standard external components, and is available in a space-saving LGA (3mmx3mmx2mm) package.

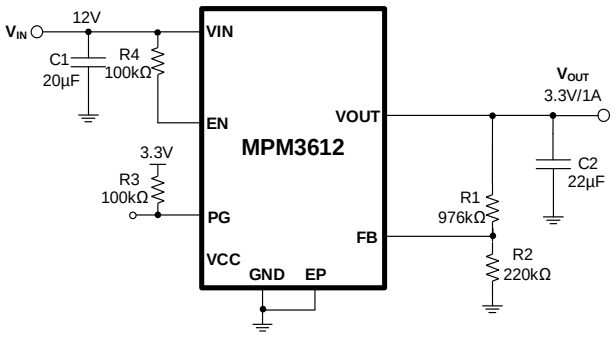
FEATURES

- Wide 3V to 22V Operating Input Voltage (V_{IN}) Range
- 5µA Low Quiescent Current (I_Q)
- 1A Load Current
- High Efficiency from 100µA to 1A Load at 4V to 22V V_{IN}
- Power-Save Mode (PSM)
- 1.25MHz Fixed Switching Frequency (f_{SW}) during Continuous Conduction Mode (CCM)
- t_{ON} Extension to Support Large Duty Cycles
- Power Good (PG) Indication
- EN Shutdown Output Discharge
- Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Hiccup Mode
- Adjustable Output Voltage (V_{OUT})
- Available in an LGA (3mmx3mmx2mm) Package

APPLICATIONS

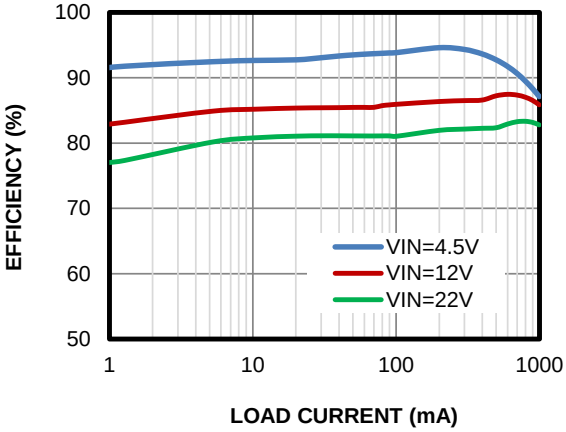
- Internet of Things (IoT)
- Home Automation and Home Security
- Single- or Multi-Cell Li-Ion Battery Systems
- Multi-Cell Dry Battery Systems
- Server Power

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 3.3V



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3612GLQ	LGA (3mmx3mmx2mm)	*See Below*	3

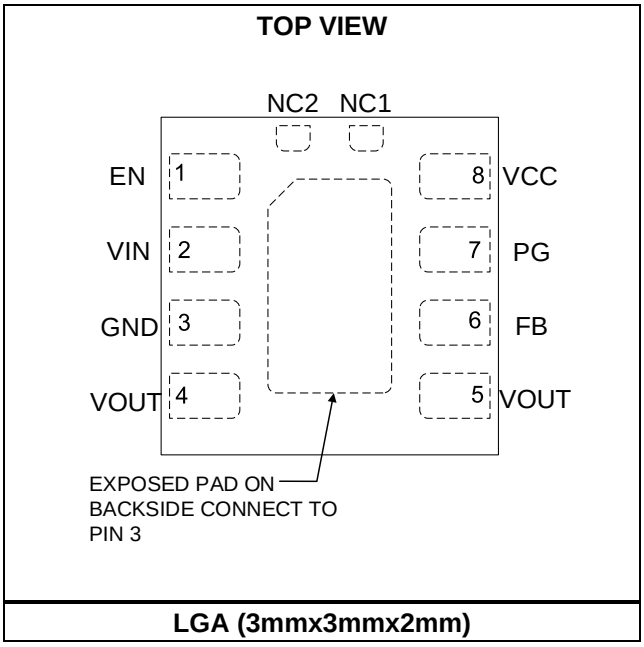
* For Tape & Reel, add suffix -Z (e.g. MPM3612GLQ-Z).

TOP MARKING

BNRY
LLLL

BNR: Product code of MPM3612GLQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



LGA (3mmx3mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable control pin.** Pull this pin to logic high to enable MPM3612; pull it to logic low to disable the part. Do not float this pin.
2	VIN	**Supply voltage.** The MPM3612 operates from a 3V to 22V input rail. A capacitor is required to decouple the input rail. Use wide PCB traces and multiple vias for the VIN power trace during PCB layout.
3	GND	**System ground.** This pin is the reference ground for the regulated output voltage (V_{OUT}), and requires special consideration during PCB layout.
4, 5	VOUT	**Module voltage output node.**
6	FB	**Feedback.** This pin sets V_{OUT} when connected to the tap of an external resistor divider that is connected between VOUT and GND.
7	PG	**Power good output.** This pin is an open drain that indicates whether the power is good (no under-voltage [UV] or over-voltage [OV] fault).
8	VCC	**Internal 3.3V LDO output.** The driver and control circuits are powered by the voltage from this pin.
NC1	NC1	**Not connected.**
NC2	NC2	**Not connected.**
Exposed pad	-	**Exposed pad.** Connect to GND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{EN}, V_{OUT} .....-0.3V to +24V
V_{SW}.....-0.3V (-5V < 10ns) to +24V (28V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{PG} 6.5V
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A = 25°C) (2)
..... 1.78W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 22V
Output voltage (V_{OUT})..... 0.6V to V_{IN} x D_{MAX}
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4, 5, 6, 7)

LGA (3mmx3mmx2mm)
θ_{JA}.....70.3°C/W
θ_{JC_TOP}.....34.9°C/W
θ_{JB}.....54.9°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
5) The thermal parameter is based on test on the EVM3612-LQ-00A evaluation board under no airflow cooling conditions in a standard enclosure. The EVM3612-LQ-00A is a 6.4cmx6.4cm, 2-layer PCB, with a 2oz. top and bottom layer copper thickness.
6) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on $T_J = \theta_{JC\_TOP} \times P_{LOSS} + T_{CASE\_TOP}$, where P_{LOSS} is the module's entire power loss in a real application, and T_{CASE_TOP} is the case top temperature.
7) The junction-to-board thermal characterization parameter, θ_{JB}, estimates T_J in the real system, based on $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the module's entire power loss in a real application, and T_{BOARD} is board temperature.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN_SD}				2	μA
Quiescent current	I_Q	V_{FB} = 0.7V		5	9	μA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			260	450	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			120	200	mΩ
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{IN} = 22V, V_{SW} = 0V and 22V, T_J = 25°C			1	μA
Low-side (LS) valley current limit	I_{VALLEY}		1.15	1.4	1.65	A
LS sink current limit [9]	I_{LS_SINK}	OVP or output discharge		-600		mA
Internal inductance	L			2.2		μH
Internal inductor DCR	L_{DCR}	T_J = 25°C		200		mΩ
Switching frequency	f_{SW}	V_{OUT} = 3.3V, in CCM	-10%	1250	+10%	kHz
Minimum off time [9]	t_{OFF_MIN}			140		ns
Minimum on time [9]	t_{ON_MIN}			40		ns
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV	96	98		%
Feedback voltage	V_{FBR}	Room temp	594	600	606	mV
	V_{FBF}	Over-temperature	-1.5%	600	+1.5%	mV
Feedback current	I_{FB}	V_{FB} = 620mV		10	50	nA
Output over-voltage protection (OVP) rising threshold	V_{OVP_R}		115%	120%	125%	V_{REF}
Output over-voltage (OV) deglitch time [9]	t_{OVP}			8		μs
Output OVP recovery	V_{OVP_F}		105%	110%	115%	V_{REF}
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UV\_VTH}$		2.63	2.8	2.97	V
V_{IN} UVLO threshold hysteresis	$V_{IN\_UV\_HYS}$			170		mV
Soft-start time	t_{SS}	10% to 90% of V_{OUT}	1	1.3	1.6	ms
VCC voltage	V_{CC}	I_{CC} = 2.5mA	3.1	3.3	3.5	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0A to 5mA	0.1	0.5	0.9	%
Thermal shutdown [9]	T_{STD}			150		°C
Thermal hysteresis [9]	T_{HYS}			20		°C
EN rising threshold	V_{EN_R}		1.05	1.2	1.35	V
EN hysteresis	V_{EN_F}			150		mV
EN input current	I_{EN}	V_{EN} = 2V			0.1	μA
Power good (PG) under-voltage (UV) rising threshold	$V_{PG\_UV\_R}$		87%	92%	97%	V_{REF}
PG UV falling threshold	$V_{PG\_UV\_F}$		82%	87%	92%	V_{REF}
PG OV rising threshold	$V_{PG\_OV\_R}$		108%	113%	118%	V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG OV falling threshold	$V_{PG\_OV\_F}$		103%	108%	113%	V_{REF}
PG rising delay	$t_{PG\_R\_DLY}$			120		µs
PG falling delay	$t_{PG\_F\_DLY}$			50		µs
PG sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V

Notes:

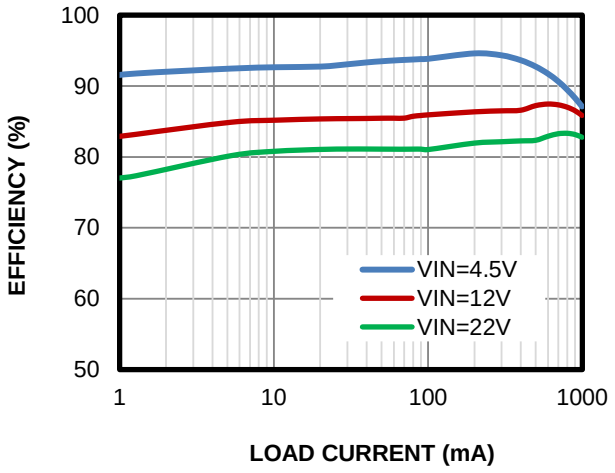
8) Guaranteed by over-temperature correlation. Not tested in production.
9) Guaranteed by sample characterization. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

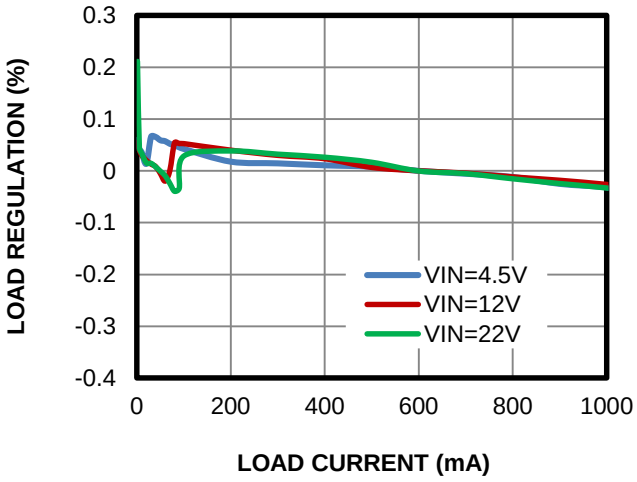
Efficiency vs. Load Current

V_{OUT} = 3.3V



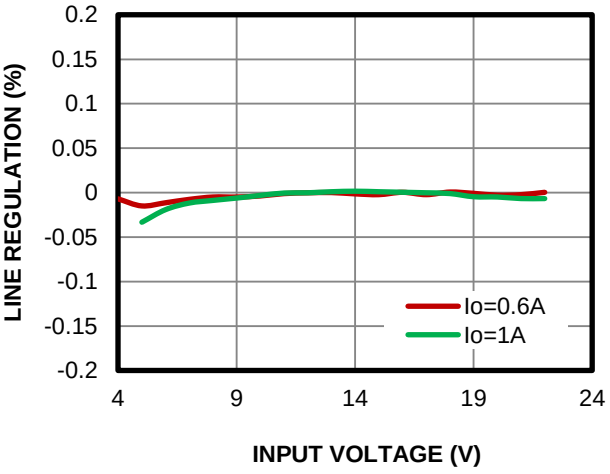
Load Regulation vs. Load Current

V_{OUT} = 3.3V

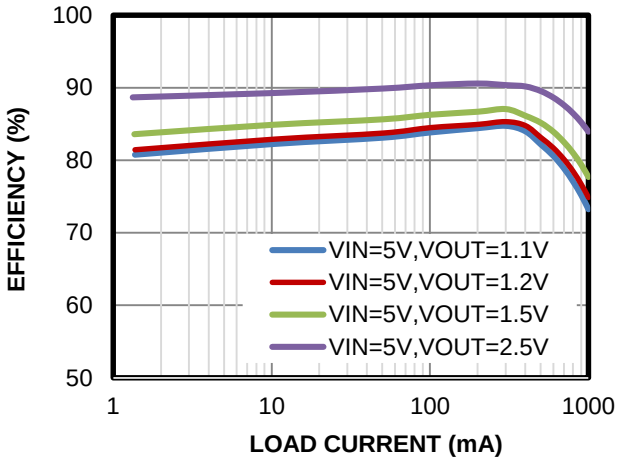


Line Regulation vs. Input Voltage

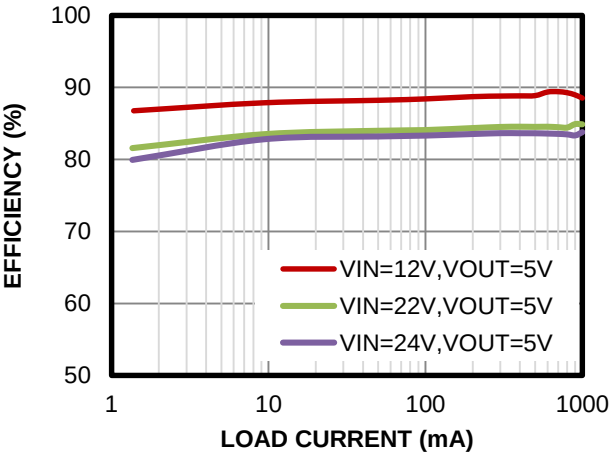
V_{OUT} = 3.3V



Efficiency vs. Load Current



Efficiency vs. Load Current

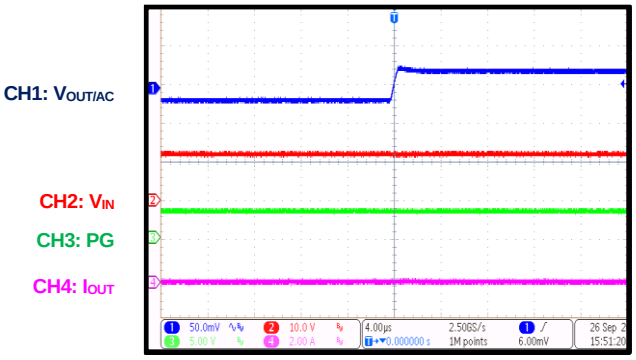


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

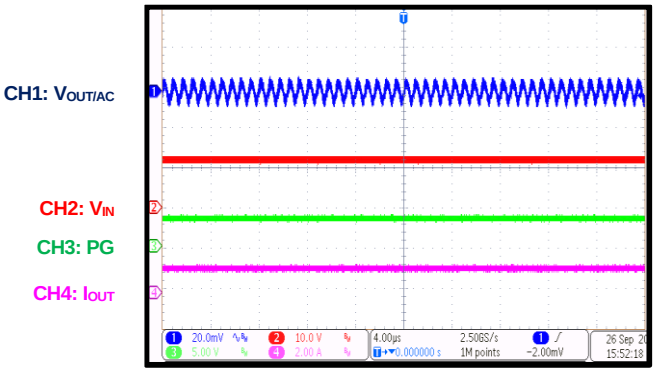
Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



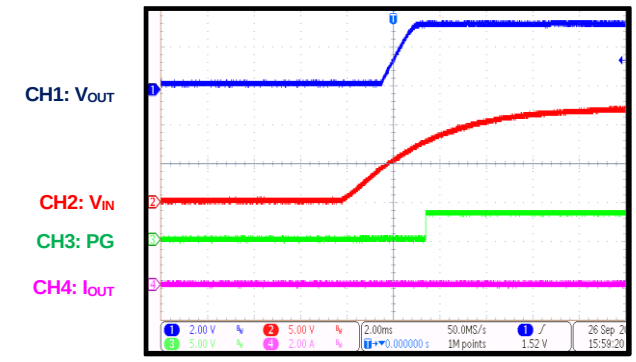
Steady State

V_{IN} = 12V,V_{OUT} = 3.3V, I_{OUT} = 1A



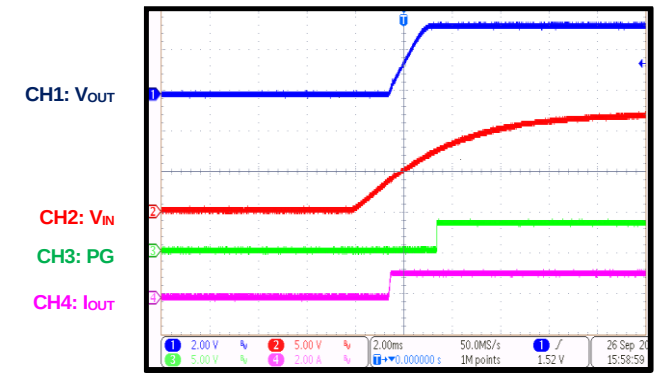
Start-Up through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



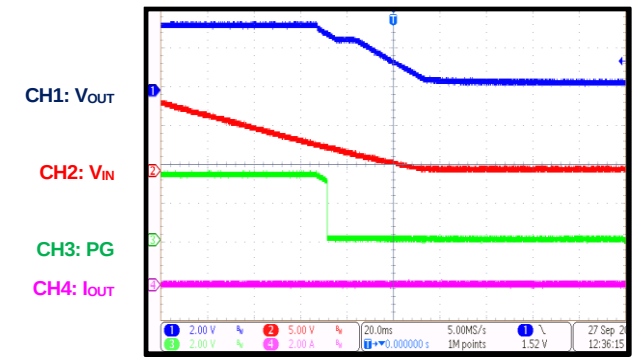
Start-Up through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



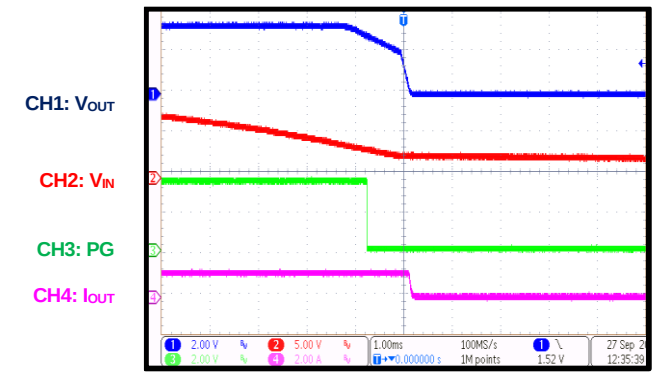
Shutdown through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



Shutdown through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A

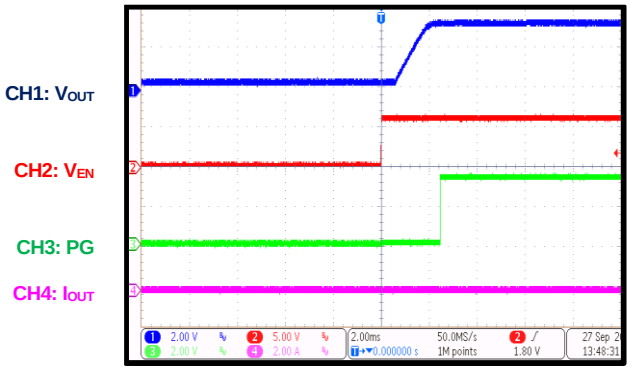


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

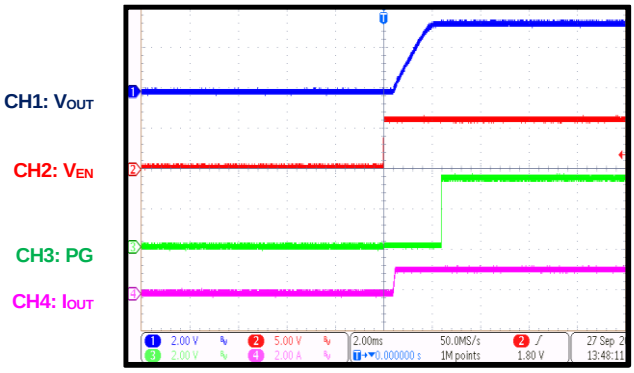
Start-Up through EN

V_{IN} = 12V,V_{OUT} = 3.3V, I_{OUT} = 0A



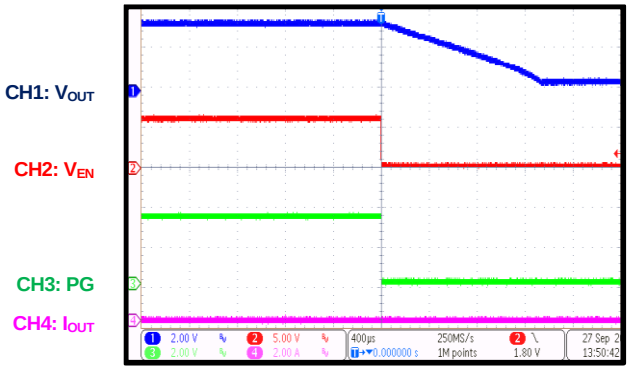
Start-Up through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



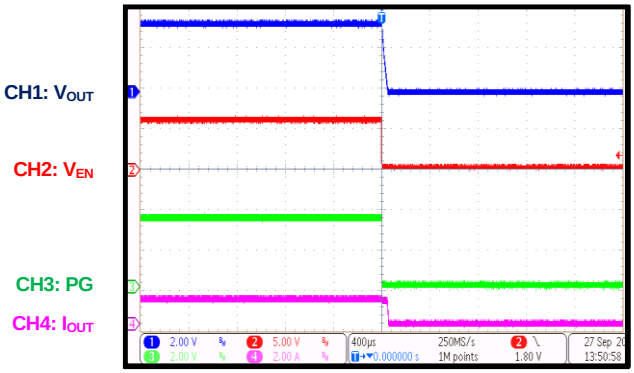
Shutdown through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



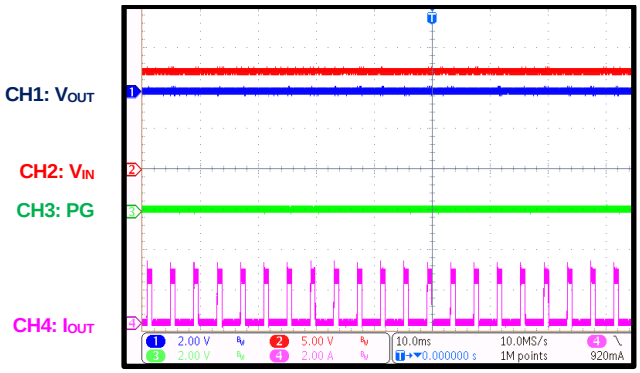
Shutdown through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



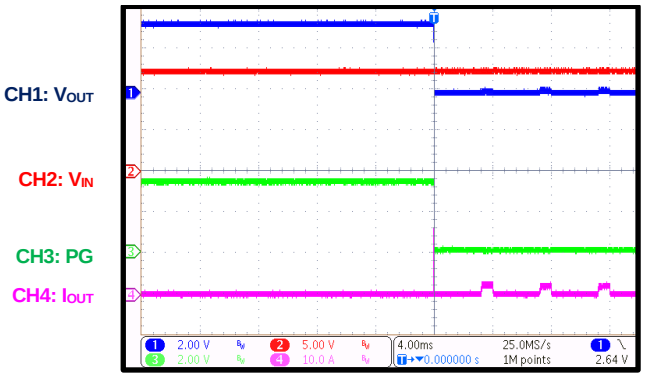
SCP Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



SCP Entry

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

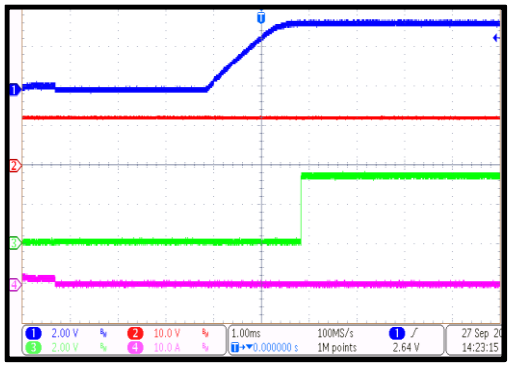


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

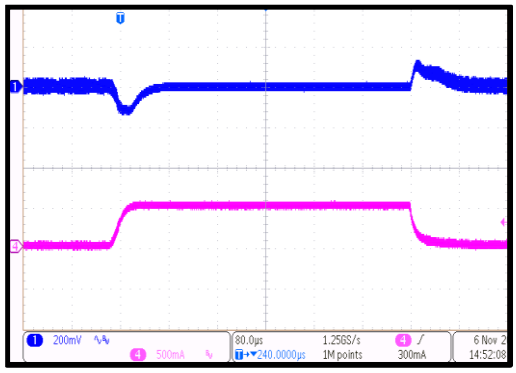
SCP Recovery

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



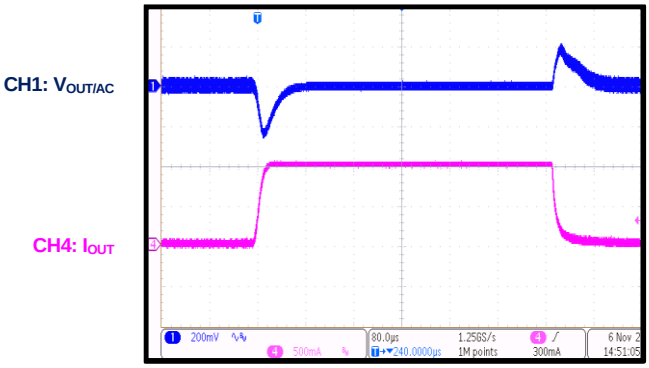
Load Transient

0.8A/µs, 0A to 0.5A, V_{IN} = 12V, V_{OUT} = 3.3V



Load Transient

0.8A/µs, 0A to 1A, V_{IN} = 12V, V_{OUT} = 3.3V

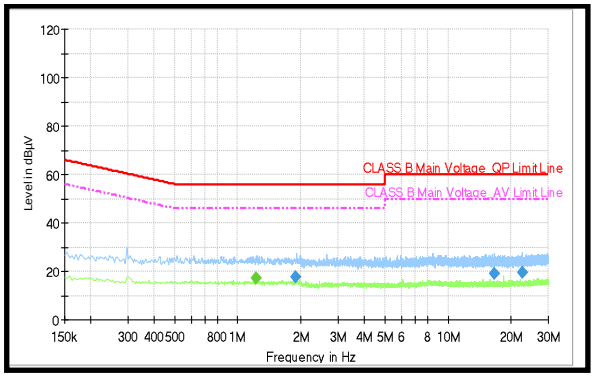


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

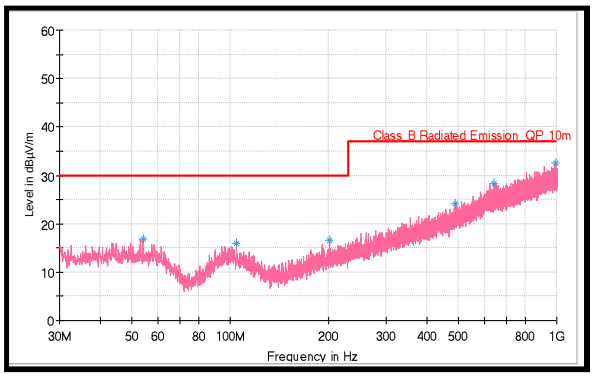
EN55022 Class B Conducted Emissions

V_{OUT} = 3.3V, input Pi filter: 8.8µF, 2.2µF, 8.8µF, 2.2µH

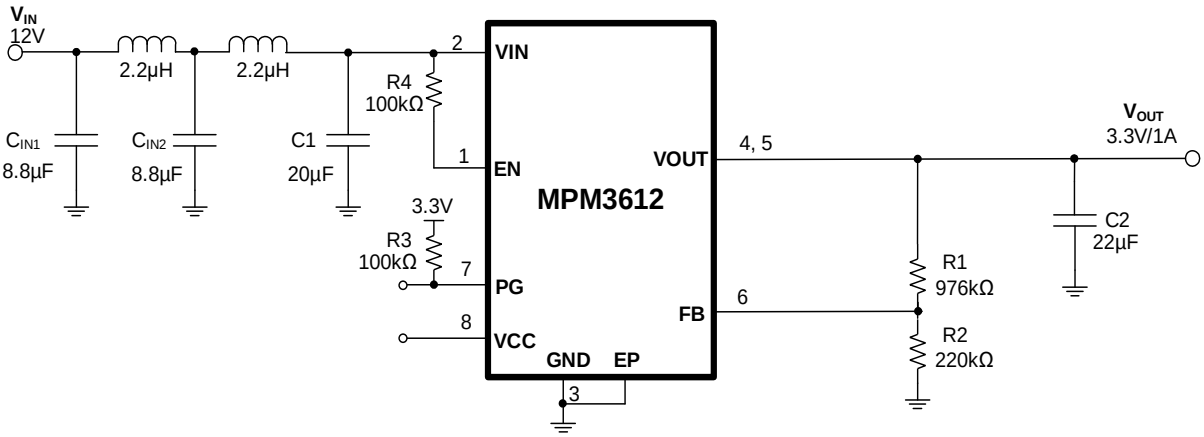


EN55022 Class B Radiated Emissions

V_{OUT} = 3.3V, input Pi filter: 8.8µF, 2.2µF, 8.8µF, 2.2µH



EMI TEST CIRCUIT



FUNCTIONAL BLOCK DIAGRAM

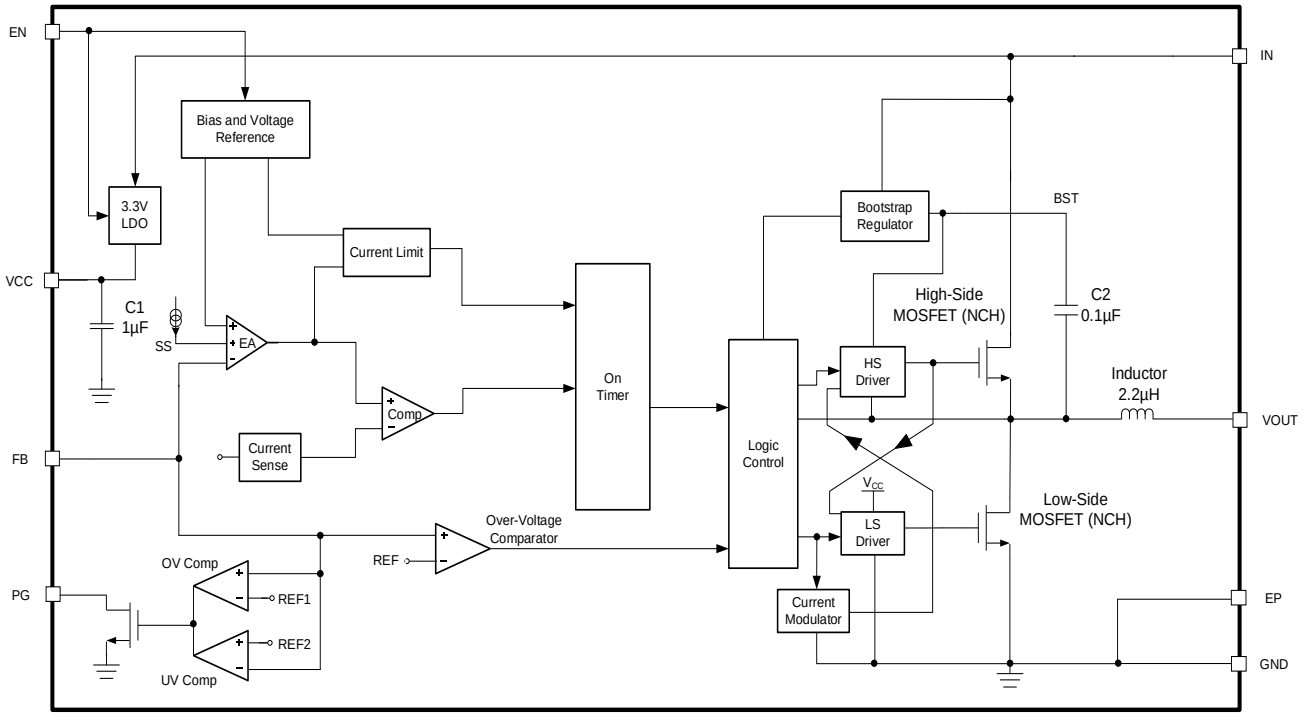


Figure 1: Functional Block Diagram

OPERATION

The MPM3612 is a low quiescent current (I_Q), fully integrated, synchronous, rectified, step-down power module. It offers a very compact solution to achieve up to 1A of output current (I_{OUT}) across a wide input supply range with excellent efficiency.

Pulse-Width Modulation (PWM) Operation

The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 2 shows the MPM3612's simplified ramp compensation block. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the ISENSE ramp (V_{ISENSE}) falls below the error amplifier (EA) output voltage (V_{EAO}), which indicates an insufficient output voltage (V_{OUT}).

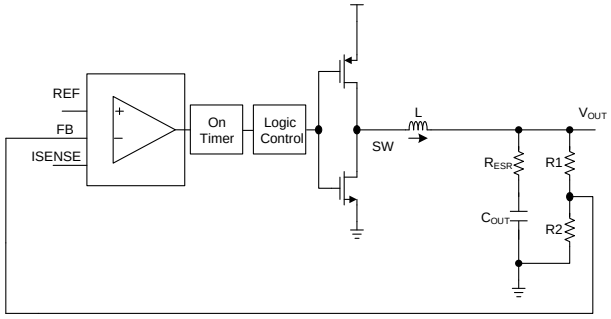


Figure 2: Simplified Control Block

After the on time elapses, the HS-FET shuts down. By cycling the HS-FET on and off, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss.

If the HS-FET and LS-FET are turned on at the same time, a dead short occurs between the input and GND, which dramatically reduces efficiency. This is called shoot-through. The MPM3612 avoids shoot-through by internally generating a dead time (DT) between the HS-FET turning off and LS-FET turning on, and vice versa. The MPM3612 enters either heavy-load operation or light-load operation depending on the amplitude of I_{OUT}.

Light-Load Operation

When the MPM3612 is operating under light-load conditions, it automatically reduces the switching frequency (f_{SW}) to maintain high efficiency and the inductor current (I_L) drops near 0A. When I_L reaches 0A, the LS-FET driver enters tri-state (Hi-Z). At this point, the current modulator controls the LS-FET and limits I_L to about 0A (see Figure 3). Then the output capacitors discharge slowly to GND through the LS-FET and feedback resistors (R1 and R2). This greatly improves device efficiency when I_{OUT} is low.

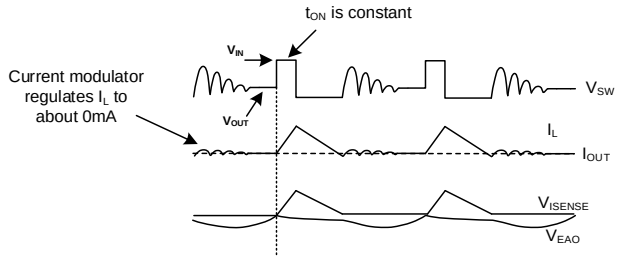


Figure 3: Light-Load Operation

Light-load operation is also called pulse-skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the time period that the current modulator regulates becomes shorter, the HS-FET turns on more frequently, and f_{SW} increases in turn. I_{OUT} reaches its critical level when the current modulator time is zero, and can be calculated using Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device reverts to pulse-width modulation (PWM) mode once I_{OUT} exceeds its critical level. After that, f_{SW} remains constant across the entire I_{OUT} range.

VCC Regulator

A 3.3V internal VCC regulator powers most of the internal circuitries. This regulator takes the input voltage (V_{IN}) and operates across the full V_{IN} range. When V_{IN} is above 3.3V, the output of the regulator is in full regulation. When V_{IN} is below 3.3V, V_{OUT} decreases and follows V_{IN}.

Soft Start (SS)

The MPM3612 employs soft start (SS) to ensure smooth output during start-up. When the part is enabled and the BST voltage (V_{BST}) reaches its rising threshold, an internal current source starts to charge up the internal SS capacitor (C_{SS}).

The SS voltage (V_{SS}) takes over the reference voltage (V_{REF}) to the PWM comparator. V_{OUT} ramps up smoothly with V_{SS}. Once V_{SS} exceeds the V_{REF}, it continues to ramp up while the PWM comparator compares V_{REF} and the FB voltage (V_{FB}). At this point, SS finishes and the device enters steady state operation.

The internal soft-start time (t_{SS}) is fixed to 1.3ms (V_{OUT} from 10% to 90%).

Pre-Biased Start-Up

The MPM3612 is designed for monotonic start-up into pre-biased loads. If V_{OUT} is pre-biased to a certain voltage during start-up, V_{BST} is refreshed and charged and V_{SS} is charged. If V_{BST} exceeds its rising threshold voltage and V_{SS} exceeds the sensed V_{FB}, the part begins normal operation.

Power Good (PG)

The MPM3612 features a power good (PG) output to indicate whether V_{OUT} is ready. The PG pin is an open-drain output. Connect PG to VCC or another voltage source via a pull-up resistor (e.g. 100kΩ). When V_{IN} is applied, the PG pin is pulled down to GND before V_{SS} reaches 1V. Once V_{SS} reaches 1V and V_{FB} exceeds 92% of V_{REF}, there is a 120μs delay and PG is pulled high. During normal operation, PG is pulled low if V_{FB} drops below 87% of V_{REF} (after 50μs delay).

If under-voltage lockout (UVLO) or over-temperature protection (OTP) occurs, or EN goes low, the PG pin is pulled low immediately. If over-current protection (OCP) occurs and V_{FB} drops below 87% of V_{REF}, there is a 50μs delay and PG is pulled low.

PG also indicates whether an output over-voltage (OV) condition has occurred. If V_{OUT} exceeds 113% of the V_{REF} rising threshold, PG pulls low. If V_{OUT} falls below 108% of the V_{REF} falling threshold, PG pulls high again. The PG deglitch timer is 120μs and 50μs for the rising and falling thresholds, respectively. Note that this threshold is below the OVP discharge threshold.

Low-Dropout (LDO) Operation

To improve dropout, the MPM3612 is designed to extend the HS-FET on time if the minimum off time (t_{OFF_MIN}) is triggered. In this scenario, the HS-FET on time is extended and f_{SW} drops. The typical minimum f_{SW} (f_{SW_MIN}) is 240kHz. If f_{SW} drops to 240kHz, the duty cycle reaches its maximum (D_{MAX}) for the duration of the on time. If V_{IN} continues to drop, the MPM3612 operates at 240kHz and V_{OUT} drops. The typical max duty cycle (D_{MAX}) can be calculated with Equation (2):

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW\_MIN} \quad (2)$$

Where t_{OFF_MIN} = 140ns, and f_{SW_MIN} = 240kHz.

Output Over-Voltage Protection (OVP)

The MPM3612 monitors V_{OUT}. If V_{OUT} exceeds 120% of its regulated voltage for more than 8μs, the device enters OVP discharge mode. In OVP discharge mode, the LS-FET turns on and remains on until the low-side (LS) current reaches the negative current limit. This discharges V_{OUT} and tries to keep it within its normal range. If a V_{OUT} OV condition still exists, the LS-FET turns on again after a fixed delay to repeat the discharge behavior.

Once V_{FB} falls below 110% of V_{REF}, the MPM3612 exits OVP discharge mode.

If V_{IN} exceeds 24V during OVP discharge mode, input OVP occurs and the MPM3612 shuts down until V_{IN} drops below 22V. Then the MPM3612 restarts and resumes normal operation. Input OVP is only active during output OV conditions.

Output Discharge

The MPM3612 offers a discharge function that provides an active discharge path for the external C_{OUT}. This function is active when the part is disabled via EN (EN is pulled low). When EN is low, the HS-FET turns off and the LS-FET turns to discharge V_{OUT}. When the LS current reaches its negative current limit, the LS-FET turns off, then turns on again after a fixed delay. This behavior repeats until FB goes low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM3612 includes valley current limit control. When the LS-FET is on, I_L is monitored. If the sensed I_L exceeds the valley current limit threshold, the device enters OCP and the HS-FET is not allowed to turn on until I_L falls below the valley current limit. Meanwhile, V_{OUT} drops until it is below the under-voltage (UV) threshold, typically 60% below V_{REF}.

If under-voltage protection (UVP) and OCP are both triggered, the MPM3612 enters hiccup mode to periodically restart the part. The hiccup duty cycle is very small to reduce power dissipation during a short-circuit condition. During OCP, the device tries to recover from over-current (OC) fault with hiccup mode by disabling the output power stage, discharging C_{SS} and automatically try to soft start again. If the OC condition still exists when SS finishes, the device repeats this operation. OCP is a non-latch protection.

Enable (EN)

EN is a digital control pin that turns the MPM3612 on and off. Pull EN high to turn on the power module; pull it low to turn off the power module. The EN pin cannot be left floating.

The EN pin can survive a 22V V_{IN}, meaning it can be directly connected to VIN for automatic start-up.

Under-Voltage Lockout (UVLO) Protection

The MPM3612 features UVLO protection. If V_{IN} falls below the UVLO falling threshold, the MPM3612 shuts down. Once V_{IN} exceeds the UVLO rising threshold, the device starts up again and resumes normal operation.

Thermal Shutdown

The MPM3612 employs thermal shutdown by internally monitoring the device's junction temperature (T_J). If T_J exceeds the upper threshold (150°C), the power module shuts down. This is a non-latch protection, with about a 20°C hysteresis. Once T_J drops to about 130°C, the device initiates a soft start and resumes normal operation.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set V_{OUT}. First, choose a value for R2. R2 should be chosen reasonably, as too small of a value leads to considerable quiescent current (I_Q) loss, while too large of a value makes the FB pin noise-sensitive. It is recommended to choose R2 to be 100kΩ to 500kΩ. It is typically recommended to set the current through R2 to be between 1μA and 5μA to achieve a good balance between system stability and load loss. R1 can be calculated with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

Figure 4 shows the feedback circuit.

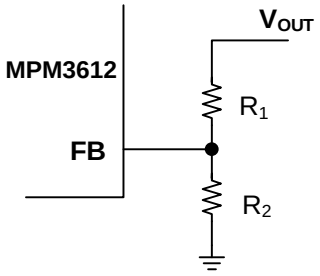


Figure 4: Feedback Network

Table 1 lists recommended resistances for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	147	220
1.2	220	220
1.8	440	220
2.5	697	220
3.3	976	220
5	1613	220

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitor must also have a ripple current rating greater than the maximum input ripple current (I_{CIN}) of the converter. I_{CIN} can be estimated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the input voltage ripple (ΔV_{IN}) of the converter. If there is a ΔV_{IN} requirement in the system, choose an input capacitor that meets the relevant specifications.

ΔV_{IN} can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. Ceramic or POSCAP capacitors are recommended. The V_{OUT} ripple (ΔV_{OUT}) can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (8)$$

In the case of ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The V_{OUT} ripple caused by ESR is very small. In the case of POSCAP capacitors, the ESR dominates the impedance at f_{SW}.

In addition to considering ΔV_{OUT}, the maximum C_{OUT} limitation should be also considered. Choosing a larger C_{OUT} can provide better load transient response. However, if C_{OUT} is too high, V_{OUT} cannot reach the design value during t_{SS}, and the device will fail to regulate. The maximum C_{OUT} (C_{OUT_MAX}) can be estimated with Equation (10):

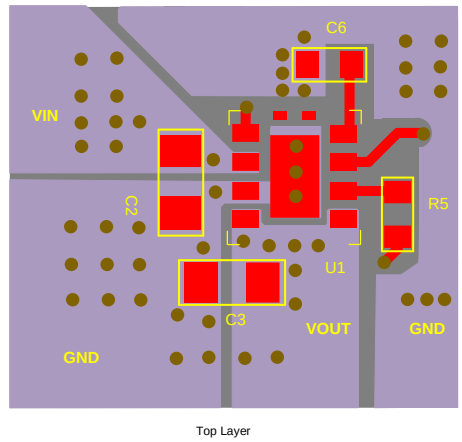
$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during soft start, and t_{SS} is the soft-start time.

PCB Layout Guidelines

Optimized PCB layout is critical for reliable operation. For the best results, refer to Figure 5 and follow the below guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Maximize the VIN and GND copper plane to minimize parasitic impedance.
3. Ensure that the high-current paths (GND, VIN, and VOUT) have short and wide traces.
4. Place as many vias as possible close to the GND pin to minimize parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor as close as possible to the VCC and GND pins.
6. Place the external feedback resistors as close as possible to the FB pin.



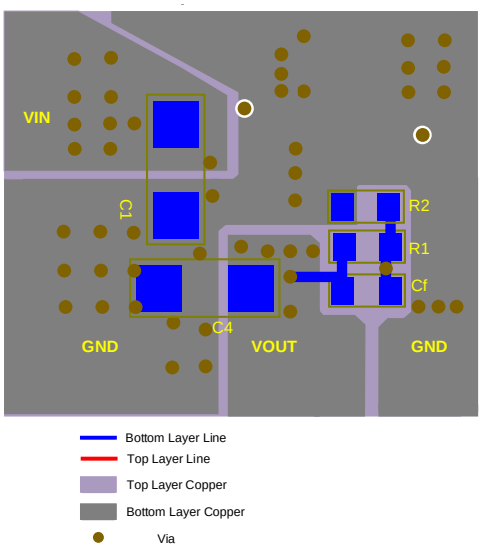


Figure 5: Recommended PCB Layout

Note:

10) This layout covers the full range of specs. A much smaller layout size can be achieved for specific cases — such as those with a higher f_{SW}, lower V_{IN} or I_{OUT} — by selecting physically smaller inductors and capacitors.

TYPICAL APPLICATION CIRCUIT

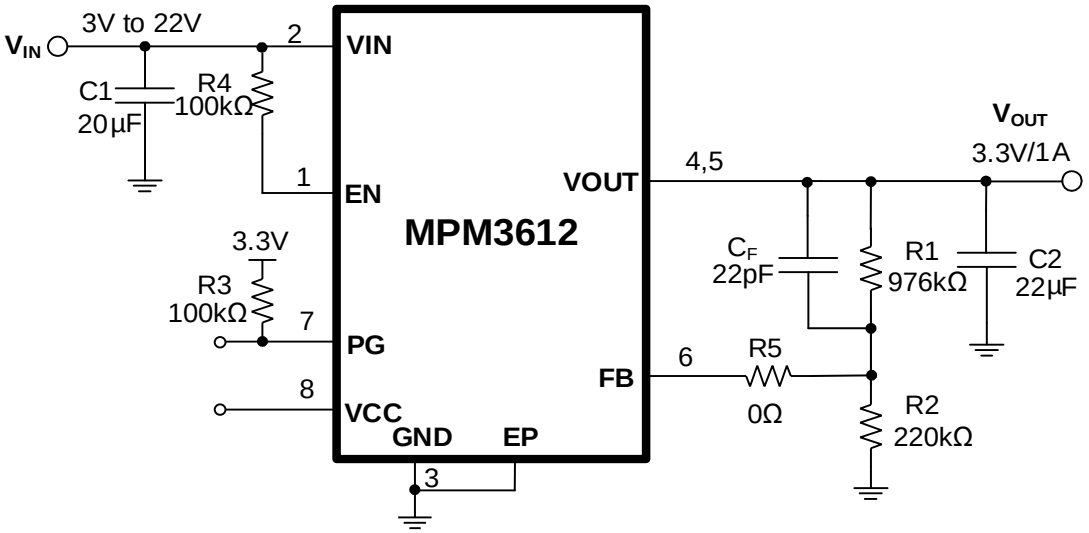
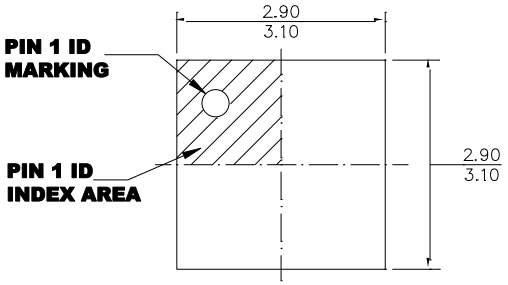


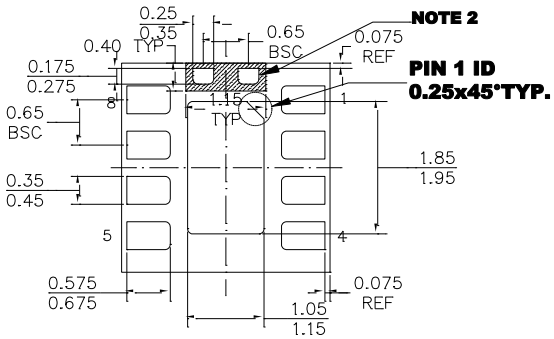
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

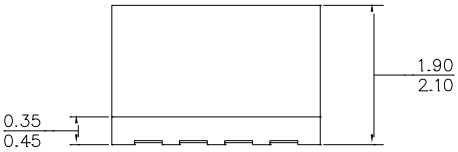
LGA (3mmx3mmx2mm)



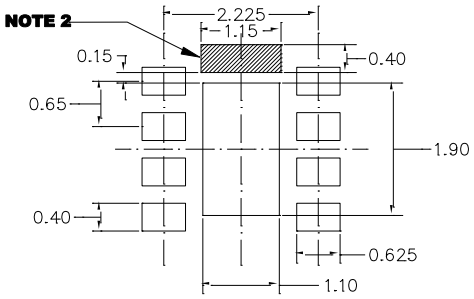
TOP VIEW



BOTTOM VIEW



SIDE VIEW

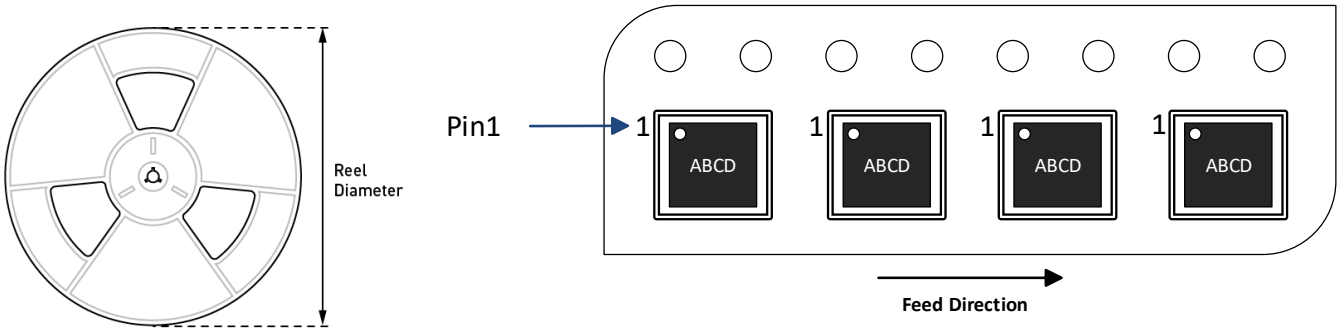


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2)SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-303.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3612GLQ-Z	LGA (3mmx3mmx2mm)	2500	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/15/2023	Initial Release	-

Mouser Electronics

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MPM3612GLQ-Z MPM3612GLQ-P