MP6543H

22V, 2A, Three-Phase Power Stage

DESCRIPTION

The MP6543H family of products (MP6543H, MP6543H-A, and MP6543H-B) are three-phase brushless DC motor drivers. They integrate three half-bridges, consisting of six N-channel power MOSFETs, as well as pre-drivers, gate drive power supplies, and current-sense amplifiers.

The MP6543H has enable (EN) and PWM inputs for each half-bridge. The MP6543H-A has separate high-side (HS) and low-side (LS) inputs, while the MP6543H-B has Hall-effect sensor inputs. Otherwise, these three devices are similar. References to the MP6543H in this document apply to the MP6543H-A and MP6543H-B, unless otherwise noted.

The MP6543H delivers up to 2A of continuous current (depending on thermal and PCB conditions) with an adjustable over-current protection (OCP) threshold. It uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs, and a trickle charge circuit to maintain a sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MP6543H is available in a QFN-24 (3mmx4mm) package with an exposed thermal pad.

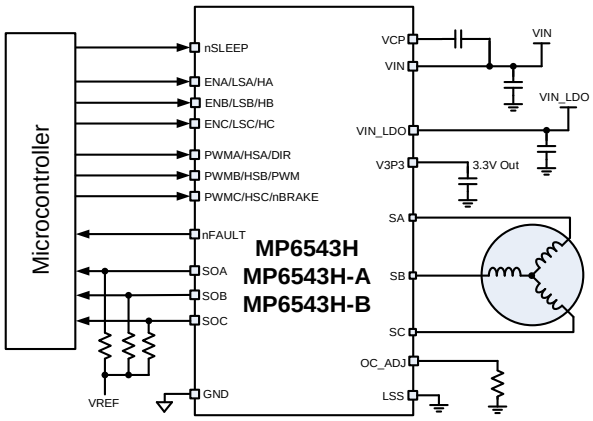
FEATURES

- 3V to 22V Operating Supply Voltage
- Three Integrated Half-Bridge Drivers
- 2A Continuous Output Current
- MOSFET On Resistance: 110mΩ per FET
- MP6543H: EN and PWM Inputs
- MP6543H-A: LS and HS Inputs
- MP6543H-B: Hall-Effect Sensor Inputs
- Built-In 3.3V, 100mA LDO Regulator
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- Under-Voltage Lockout (UVLO) and Thermal Shutdown Protection
- Over-Current Protection (OCP) with Adjustable Threshold
- Integrated, Bidirectional Current-Sense Amplifiers
- Available in a QFN-24 (3mmx4mm) Package

APPLICATIONS

- 3-Phase Brushless DC Motor Drivers

TYPICAL APPLICATION

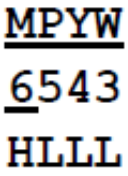


ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6543HGL*	QFN-24 (3mmx4mm)	*See Below*	*1*
MP6543HGL-A**			
MP6543HGL-B***			

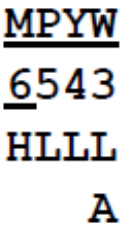
* For Tape & Reel, add suffix –Z (e.g. MP6543HGL–Z).
**For Tape & Reel, add suffix –Z (e.g. MP6543HGL-A–Z).
***For Tape & Reel, add suffix –Z (e.g. MP6543HGL-B–Z).

TOP MARKING



MP: MPS prefix
Y: Year code
W: Week code
6543H: First four digits of the part number
LLL: Lot number

TOP MARKING



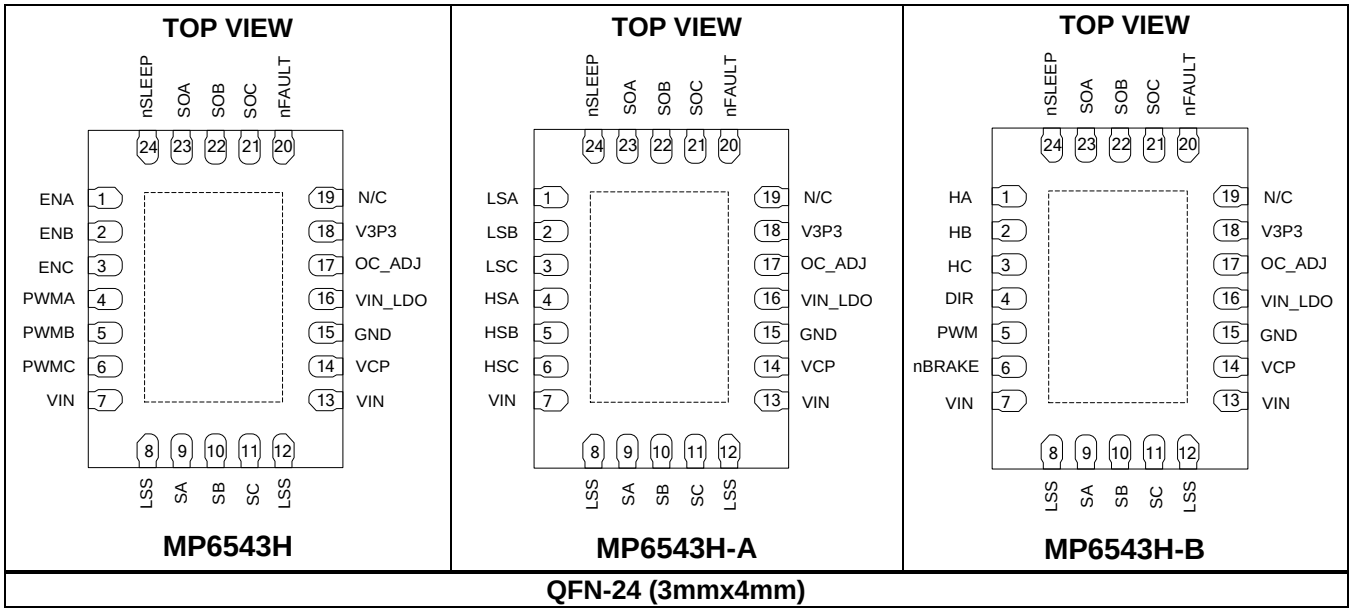
MP: MPS prefix
Y: Year code
W: Week code
xxxx: First four digits of the part number
LLL: Lot number
A: Package suffix

TOP MARKING

MPYW
6543
HLLL
B

MP: MPS prefix
Y: Year code
W: Week code
xxxx: First four digits of the part number
LLL: Lot number
B: Package suffix

PACKAGE REFERENCE



QFN-24 (3mmx4mm)

PIN FUNCTIONS

Pin #	Pin Name (MP6543H)	Pin Name (MP6543H-A)	Pin Name (MP6543H-B)	Description
1	ENA	-	-	**Enable input for phase A.**
	-	LSA	-	**Enable LS-FET for phase A.**
	-	-	HA	**Hall-effect sensor input for phase A.**
2	ENB	-	-	**Enable input for phase B.**
	-	LSB	-	**Enable LS-FET for phase B.**
	-	-	HB	**Hall-effect sensor input for phase B.**
3	ENC	-	-	**Enable input for phase C.**
	-	LSC	-	**Enable LS-FET for phase C.**
	-	-	HC	**Hall-effect sensor input for phase C.**
4	PWMA	-	-	**PWM input for phase A.**
	-	HSA	-	**Enable HS-FET for phase A.**
	-	-	DIR	**Logic input to determine the direction of the motor torque output.**
5	PWMB	-	-	**PWM input for phase B.**
	-	HSB	-	**Enable HS-FET for phase B.**
	-	-	PWM	**External PWM control for speed/torque.**
6	PWMC	-	-	**PWM input for phase C.**
	-	HSC	-	**Enable HS-FET for phase C.**
	-	-	nBRAKE	**Active low logic input for a braking function.**

PIN FUNCTIONS *(continued)*

Pin #	Pin Name	Description
7	VIN	**Input power.**
8, 12	LSS	**Low-side source connection for phases A, B, and C.** The LSS pin must be connected directly to GND.
9	SA	**Phase A output.**
10	SB	**Phase B output.**
11	SC	**Phase C output.**
13	VIN	**Input power.**
14	VCP	**Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor from VCP to VIN.
15	GND	**Ground.**
16	VIN_LDO	**LDO input.**
17	OC_ADJ	**Over-current threshold configuration pin.**
18	V3P3	**3.3V regulator output.** Low-side gate driver supply voltage. Bypass V3P3 to GND with a 4.7µF capacitor.
19	N/C	**No connection.**
20	nFAULT	**Fault indication.** Open-drain output. nFAULT pulls to logic low if a fault occurs.
21	SOC	**Current-sense output for phase C.**
22	SOB	**Current-sense output for phase B.**
23	SOA	**Current-sense output for phase A.**
24	nSLEEP	**Sleep mode input.** nSLEEP pulls to logic low to enter low-power sleep mode. nSLEEP is pulled down internally.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}, V_{IN_LDO}).....-0.3V to +25V
V_{Sx}.....-0.3V to V_{IN} + 0.3V
V_{CP} .....-0.3V to V_{IN} + 5V
AGND to PGND .....-0.3V to +0.3V
Voltage on all other pins .....-0.3 to +5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (3mmx4mm)…….... 2.6W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM)..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 22V
Output current (I_{OUT}) (4).....2A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-24 (3mmx4mm).....48 .....10…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Continuous current depends on PCB layout and ambient temperature.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 18V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		3		22	V
LDO input voltage	V_{IN_LDO}		3		22	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		2.5	3.2	mA
	I_{SLEEP}	nSLEEP = 0		45	60	µA
Control Logic						
Input logic low threshold	V_{IL}				0.4	V
Input logic high threshold	V_{IH}		1.5			V
Logic input current	$I_{IN(H)}$	V = 3.3V	-20		+20	µA
	$I_{IN(L)}$	V = 0V	-20		+20	µA
Power-up delay	t_{PUD}	V_{IN} rising or nSLEEP rising		1.5		ms
Internal pull-down resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT pull-down resistor (R_{ON})	$R_{ON(NFAULT)}$			15		Ω
V3P3 Regulator						
LDO output		I_{OUT} = 0mA to 100mA	3.2	3.3	3.4	V
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	2.5	2.7	2.9	V
UVLO hysteresis	ΔV_{UVLO}			150		mV
OCP threshold	I_{OCP}	ROCP = 0	4.7	6.2	8	A
		ROCP = float	5.5	7.2	9	A
OCP deglitch time	t_{OCD}			1		µs
OCP retry time	t_{OCR}			4		ms
Thermal shutdown (6)	T_{TSD}	T_J rising		160		°C
Thermal shutdown hysteresis (6)	ΔT_{TSD}			25		°C
Current Sense						
Current-sense ratio			1/3600	1/4000	1/4400	A/A
Current-sense output current		LS-FET current = 1A	225	250	275	µA
		LS-FET current = -1A	-275	-250	-225	µA
		LS-FET current = 100mA	22.5	25	27.5	µA
		LS-FET current = -100mA	-27.5	-25	-22.5	µA
Positive and negative matching (ratio of positive to negative)		LS-FET current = ±1A, ±100mA	95%	1	105%	
Phase matching (phase-to-phase ratio)		LS FET current = ±1A, ±100mA	95%	1	105%	
Current-sense output voltage swing		LS FET current = ±0.25A	0		3.6	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output						
HS-FET on resistance	$R_{ON(HS)}$	I_{OUT} = 1A	90	110	135	mΩ
LS-FET on resistance	$R_{ON(LS)}$	I_{OUT} = 1A	85	105	125	
Output rising time (6)		R_{LOAD} = 50Ω		25		ns
Output falling time (6)		R_{LOAD} = 50Ω		25		ns
Dead time (6)		R_{LOAD} = 50Ω		40		ns
PWMx to Sx delay time rising (6)				70		ns
PWMx to Sx delay time falling (6)				70		ns
Charge Pump						
Charge pump output voltage	V_{CP}			V_{IN} + 3.3		V

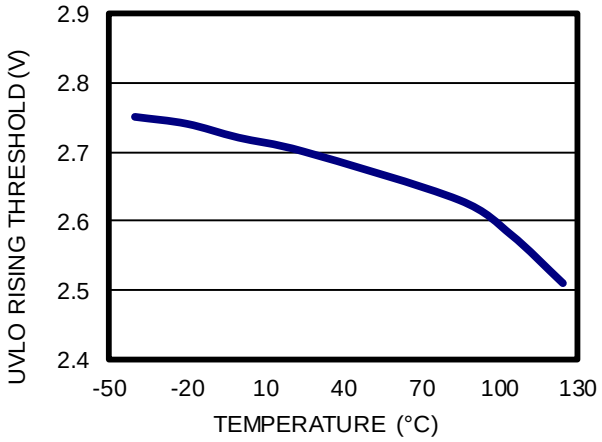
Note:

6) Not tested in production.

TYPICAL CHARACTERISTICS

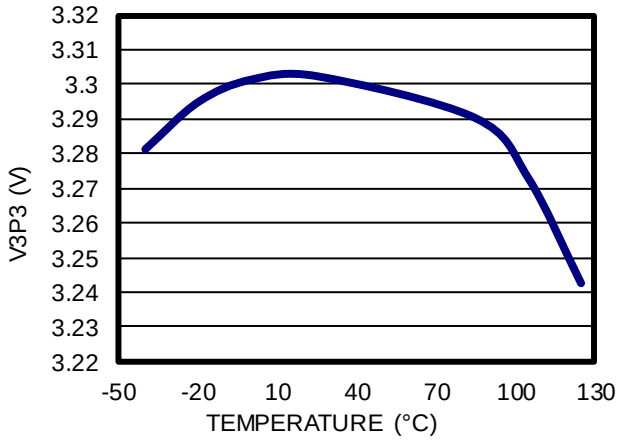
V_{IN} = 18V, unless otherwise noted.

UVLO Rising Threshold vs. Temperature



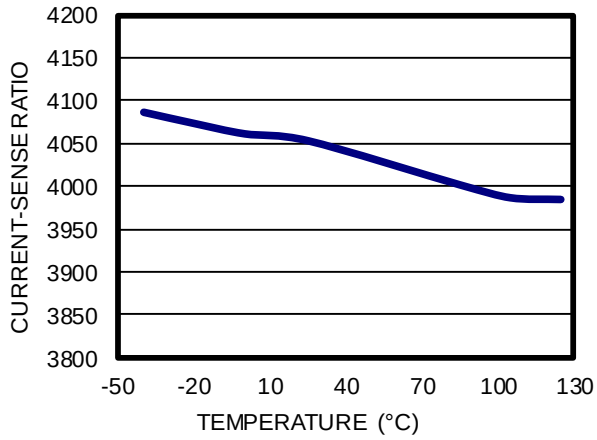
V3P3 vs. Temperature

VIN_LDO = 10V, LDO_LOAD = 100mA



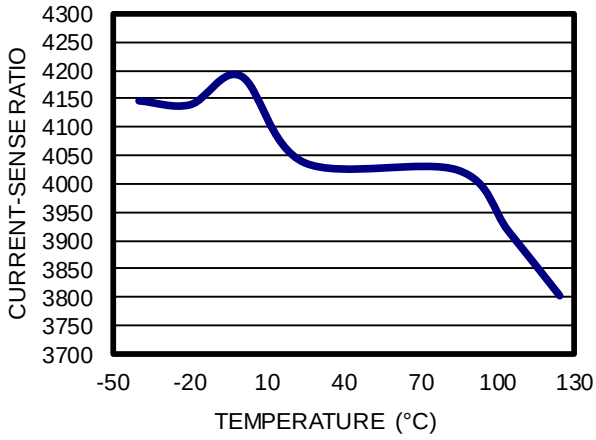
A Phase Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



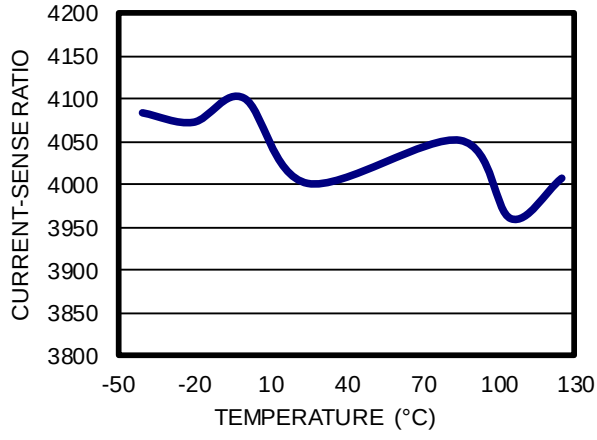
B Phase Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



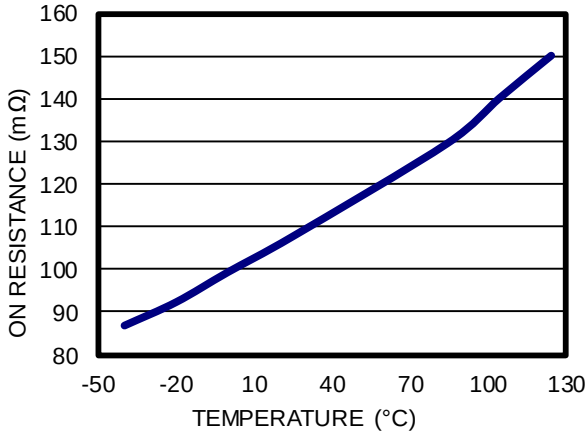
C Phase Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



HS-FET On Resistance vs. Temperature

I_{OUT} = 1A

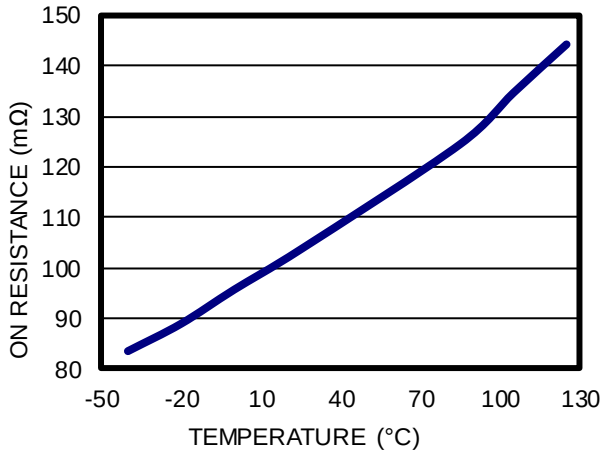


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, unless otherwise noted.

LS-FET On Resistance vs. Temperature

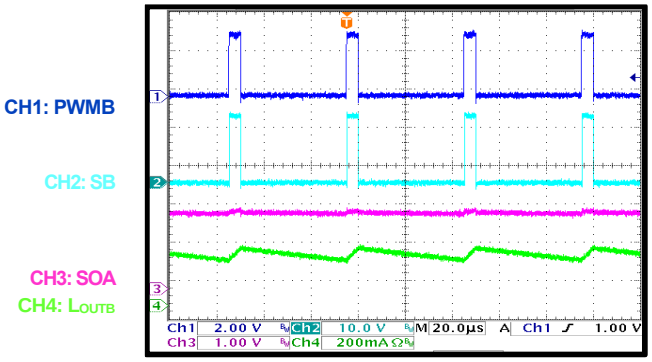
I_{OUT} = 1A



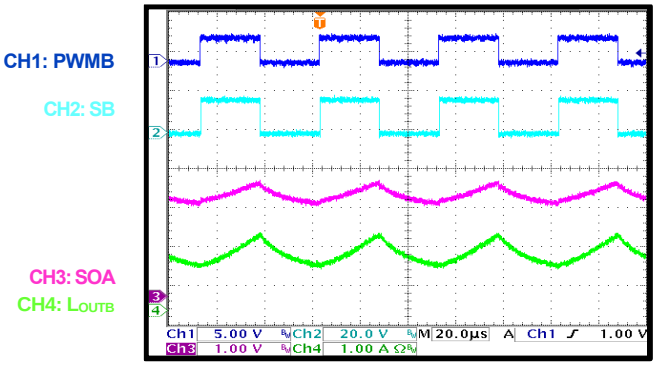
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{IN_LDO} = 18V, B phase switching with 20kHz frequency, A phase LS-FET on, C phase disabled, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 5Ω + 1mH, unless otherwise noted.

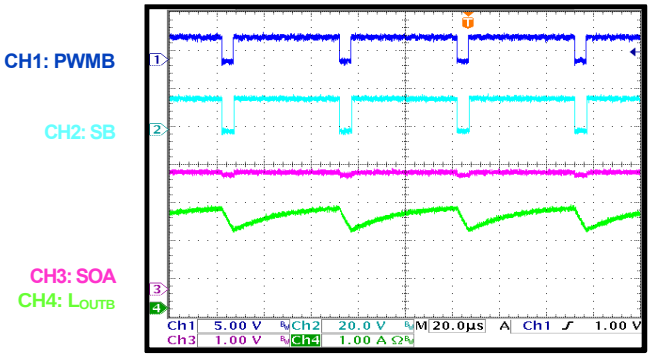
Steady State
Duty = 10%



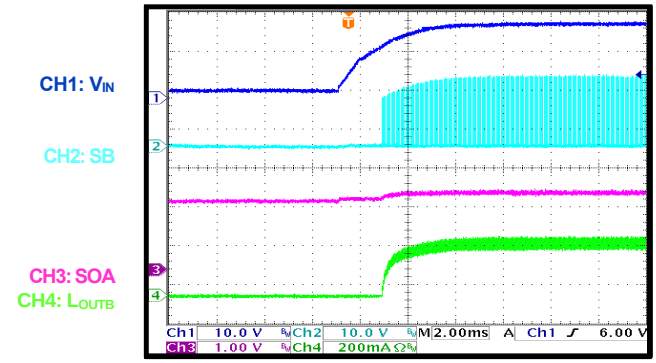
Steady State
Duty = 50%



Steady State
Duty = 90%



Power Ramping Up
Duty = 10%



Power Ramping Up
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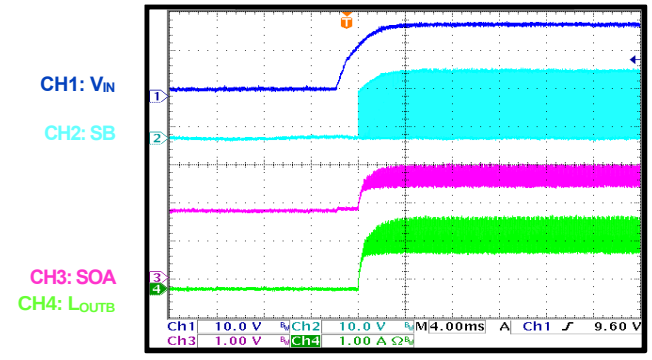

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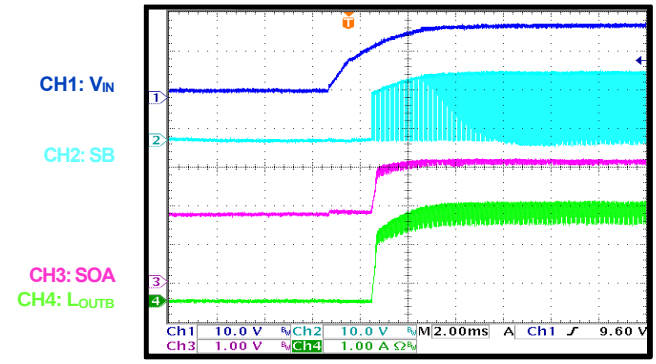
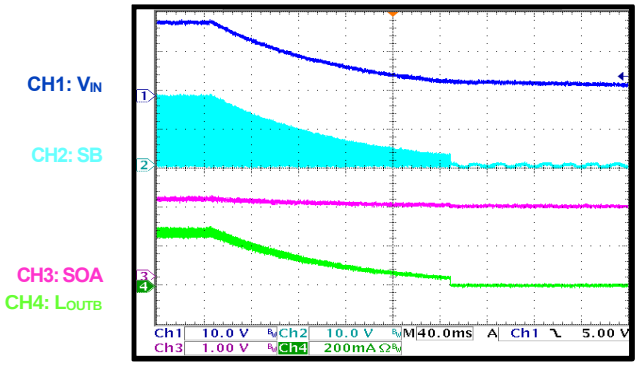
Duty = 90%



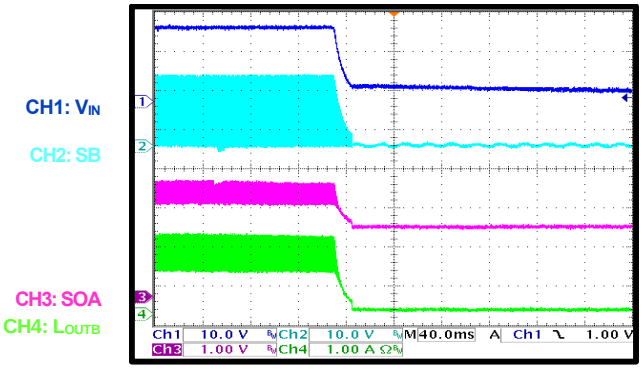
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{IN_LDO} = 18V, B phase switching with 20kHz frequency, A phase LS-FET on, C phase disabled, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 5Ω + 1mH, unless otherwise noted.

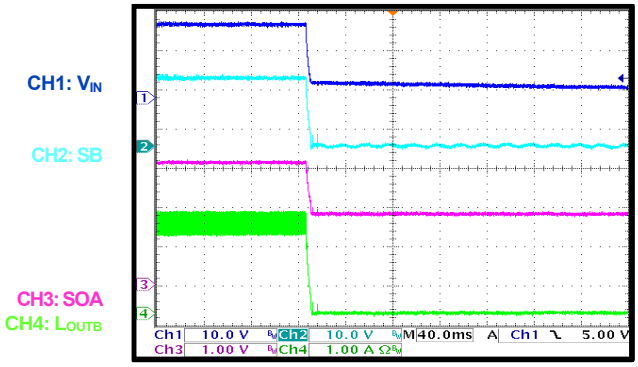
Power Ramping Down
Duty = 10%



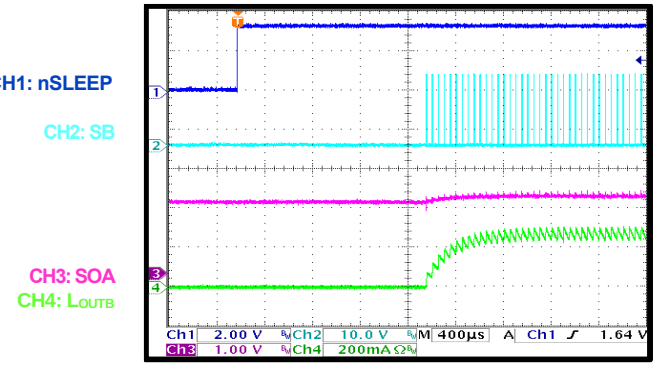
Power Ramping Down
Duty = 50%



Power Ramping Down
Duty = 90%



Sleep Recovery
Duty = 10%



Sleep Recovery
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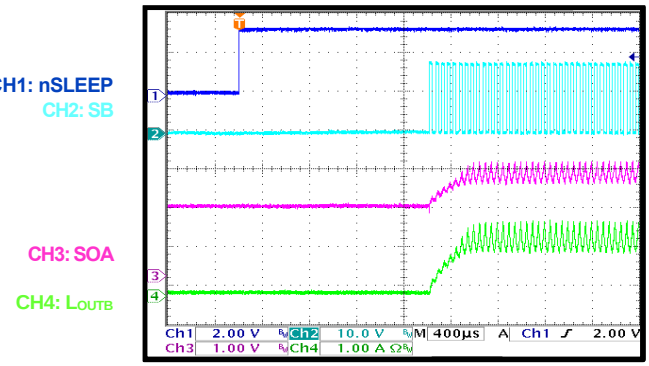

Sleep Recovery
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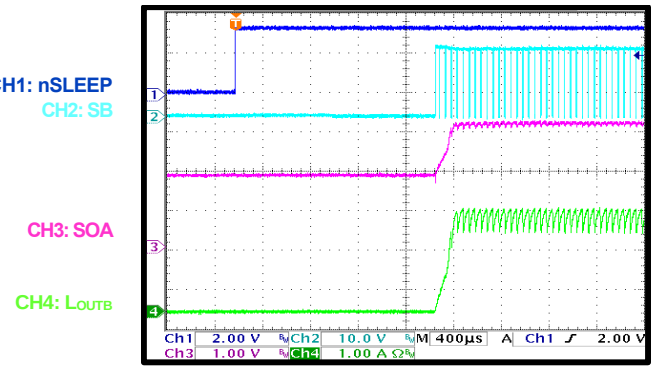

TYPICAL PERFORMANCE CHARACTERISTICS

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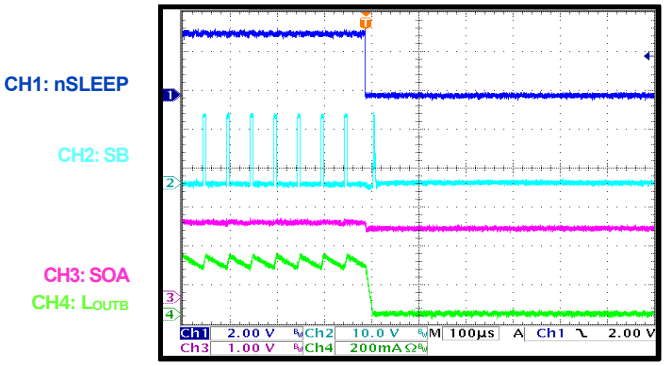
Sleep Entry
Duty = 10%



Sleep Entry
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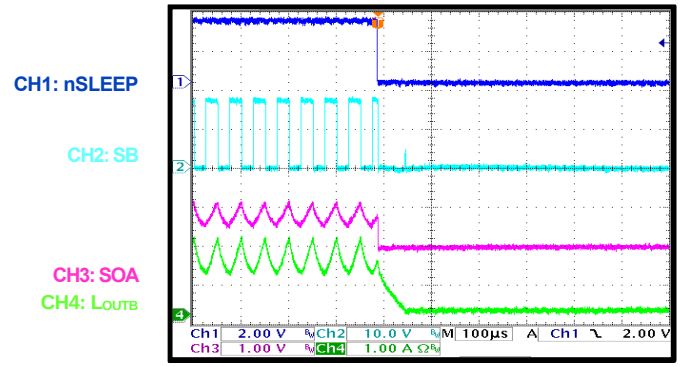

Sleep Entry
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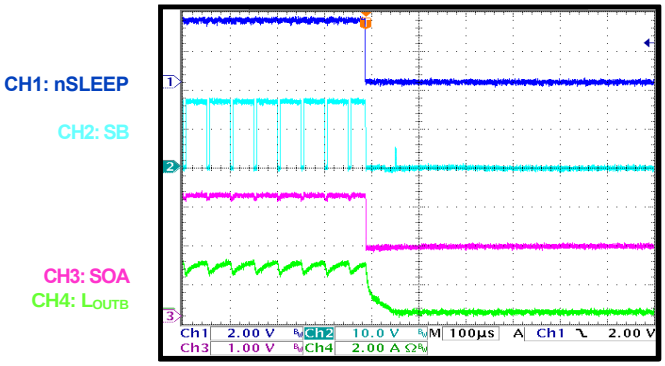


FUNCTIONAL BLOCK DIAGRAM

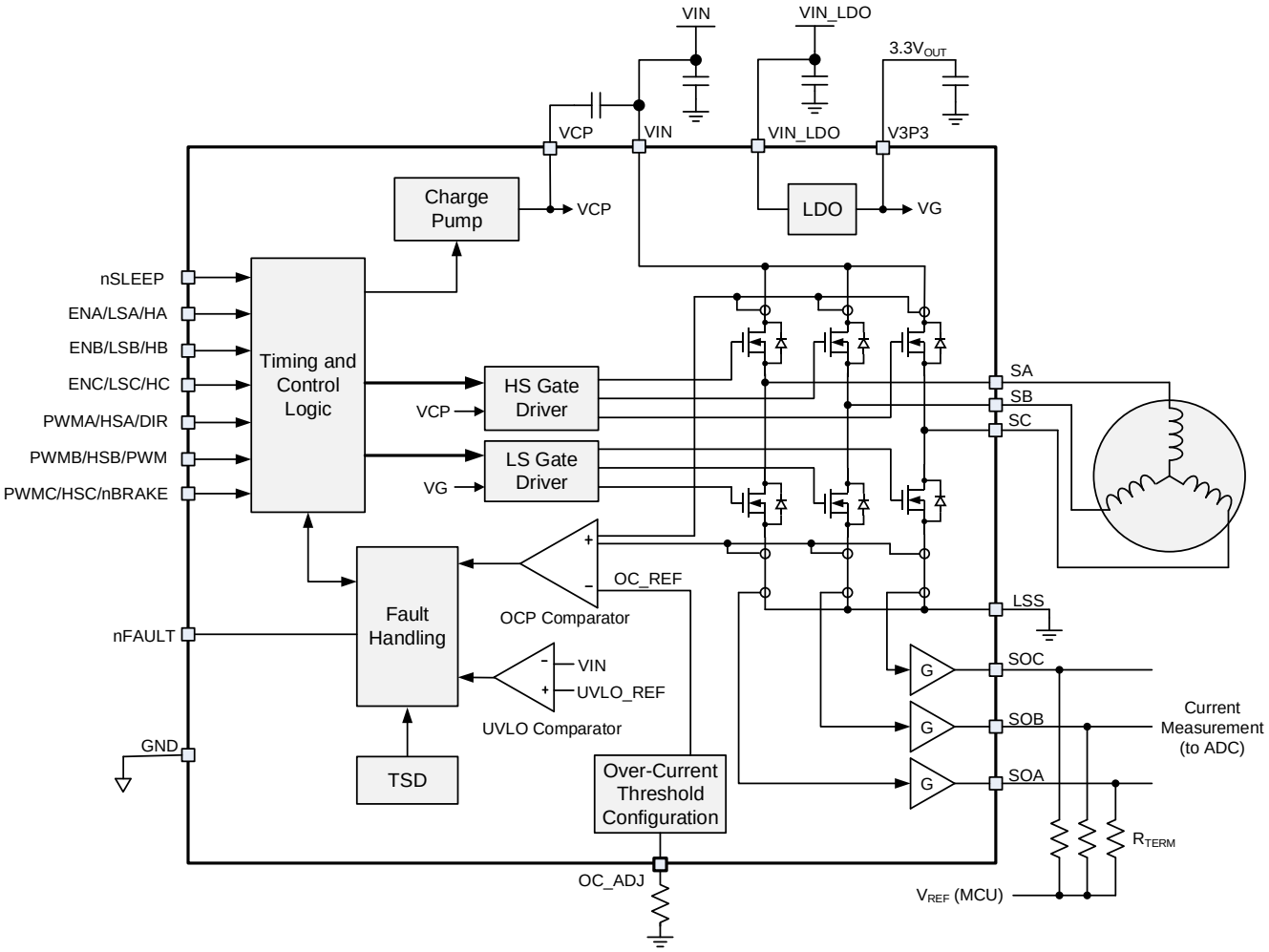


Figure 1: Functional Block Diagram

OPERATION

The MP6543H is a three-channel half-bridge driver intended to drive a brushless DC motor.

Input Logic

The MP6543H (not the MP6543H-A or MP6543H-B) has three logic input pins: ENA, ENB, and ENC. These pins enable the three outputs: SA, SB, and SC. When ENx is low, the corresponding output is disabled (output is high impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output. Table 1 shows the input logic truth table for the MP6543H.

Table 1: Input Logic Truth Table for the MP6543H

ENx	PWMx	Sx
High	High	VIN
High	Low	GND
Low	-	High impedance

The MP6543H-A has separate inputs to independently enable the HS-FETs and LS-FETs of each phase. Table 2 shows the input logic truth table for the MP6543H-A.

Table 2: Input Logic Truth Table for the MP6543H-A

HSx	LSx	Sx
Low	Low	High impedance
Low	High	GND
High	Low	VIN
High	High	High impedance

The MP6543H-B has three Hall-element inputs. The commutation logic for these inputs is determined by three Hall-element inputs spaced at 120°. The PWM, DIR, and nBRAKE inputs control motor speed, direction, and brake engagement, respectively. Table 3 shows the input logic truth table for the MP6543H-B.

Table 3: Input Logic Truth Table for the MP6543H-B

PWM	nBRAKE	Operation Mode
0	1	PWM chop mode: the load current decays
0	0	Brake mode: all low-side gates are on
1	1	Selected drivers are on
1	0	Brake mode: all low-side gates are on

Table 4 shows the commutation table for the MP6543H-B.

Table 4: Commutation Table for the MP6543H-B (nBRAKE = 1)

Logic Inputs				Motor Terminals		
HA	HB	HC	DIR	SA	SB	SC
1	0	1	1	PWM	Hi-Z	Low
1	0	0	1	Hi-Z	PWM	Low
1	1	0	1	Low	PWM	Hi-Z
0	1	0	1	Low	Hi-Z	PWM
0	1	1	1	Hi-Z	Low	PWM
0	0	1	1	PWM	Low	Hi-Z
1	0	1	0	Low	Hi-Z	PWM
0	0	1	0	Low	PWM	Hi-Z
0	1	1	0	Hi-Z	PWM	Low
0	1	0	0	PWM	Hi-Z	Low
1	1	0	0	PWM	Low	Hi-Z
1	0	0	0	Hi-Z	Low	PWM
0	0	0	-	Hi-Z	Hi-Z	Hi-Z
1	1	1	-	Hi-Z	Hi-Z	Hi-Z

Note that the logic inputs have internal pull-down resistors with a large resistance.

nSLEEP Operation

Driving the nSLEEP pin low puts the device into a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. It takes about 1.5ms for the device to respond to inputs after waking up from sleep mode. The nSLEEP input has a pull-down resistor with a large resistance.

Current-Sense Amplifiers

The current flowing in each of the three outputs is sensed by internal current-sense circuits. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. Note that only current flowing in the low-side MOSFET (LS-FET) is sensed, in both the forward and reverse directions.

To convert this current into a voltage (e.g. to an input for an analog to digital converter (ADC)), a termination resistor (R_{REF}) is used as a reference voltage. When there is no current flowing, the resulting output is equal to the reference voltage.

When current is flowing, the voltage is above or below the reference voltage, calculated with Equation (1):

$$V_{SOUT} = V_{REF} + (R_{REF} \times I_{LOAD}) / 4000 \quad (1)$$

To terminate the outputs when using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and ground. The resulting ADC code is half-scale at 0A. Figure 2 shows a simplified drawing of the current measurement circuit.

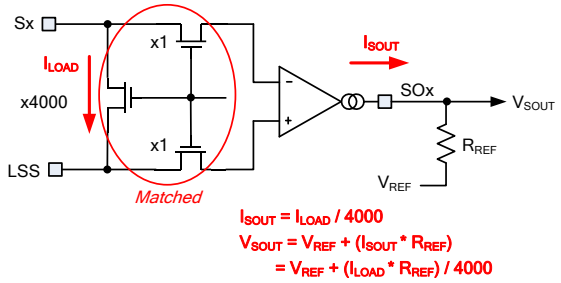


Figure 2: Current Measurement Circuit Diagram

Automatic Synchronous Rectification

If the output MOSFETs are both turned off when driving current through an inductive load, the recirculation current must continue to flow. This current is normally passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6543H implements automatic synchronous rectification.

When both the high-side MOSFET (HS-FET) and LS-FET are turned off, and the voltage on an Sx output pin is driven below ground, the LS-FET turns on until the current almost reaches 0A, or the HS-FET turns on. If the voltage on the Sx pin rises above V_{IN}, the HS-FET turns on until the current almost reaches 0A, or the LS-FET turns on.

nFAULT Output

The MP6543H provides an nFAULT output pin, which is driven active low if a fault occurs, such as over-current protection (OCP) or over-temperature protection (OTP). This pin is an open-drain output, and must be pulled up by an external pull-up resistor.

Input Under-Voltage Lockout (UVLO) Protection

If the voltage on VIN falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Normal operation resumes when V_{IN} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds its safe limits, all output FETs are disabled, and nFAULT is driven low. Normal operation resumes when the die temperature falls to a safe level.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each FET by disabling its gate driver. If the over-current limit threshold is reached, and this value remains for longer than the over-current deglitch time, all six output FETs are disabled (outputs become high impedance), and nFAULT is driven low. Then the current is recirculated through the body diodes. The outputs are disabled for about 4ms, and then they are re-enabled automatically.

Over-current conditions on both the high-side and low-side devices (e.g. a short to ground, supply, or a short across the motor winding) all result in an over-current shutdown. Figure 3 shows a simplified diagram of the OCP circuit for one output.

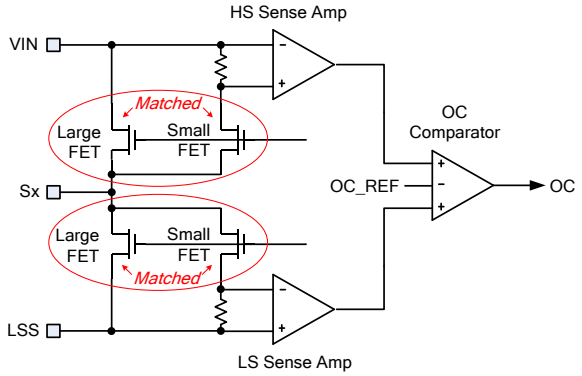


Figure 3: OCP Circuit

The over-current threshold can be configured by connecting a resistor to the OC_ADJ pin. Table 5 shows how to configure the over-current threshold.

Table 5: Over-Current Threshold Configurations

OC_ADJ Resistor Value	Minimum OC Threshold
0Ω	4.7A
Floating	5.5A

3.3V LDO Output

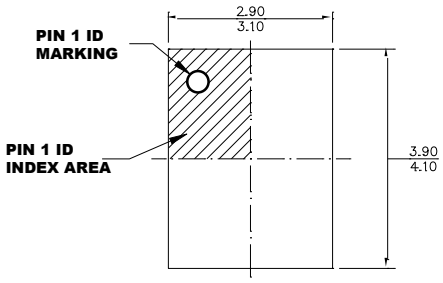
An internal LDO regulator generates a 3.3V voltage with a 100mA capacity, which can be used to power a small low-power microcontroller. Place a 4.7µF to 10µF bypass capacitor between the V3P3 pin and ground.

Charge Pump

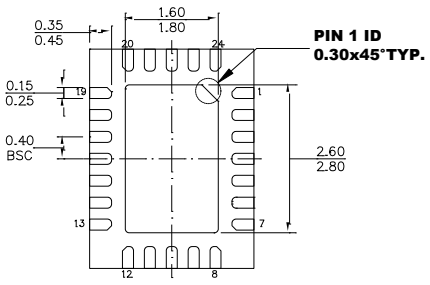
A charge pump generates the gate drive for the high-side FETs. The charge pump requires one external, 1µF ceramic capacitor rated for at least 10V. Place this capacitor between the VIN and VCP pins.

PACKAGE INFORMATION

QFN-24 (3mmx4mm)

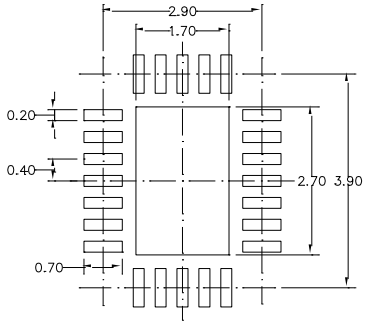


TOP VIEW



BOTTOM VIEW

SIDE VIEW

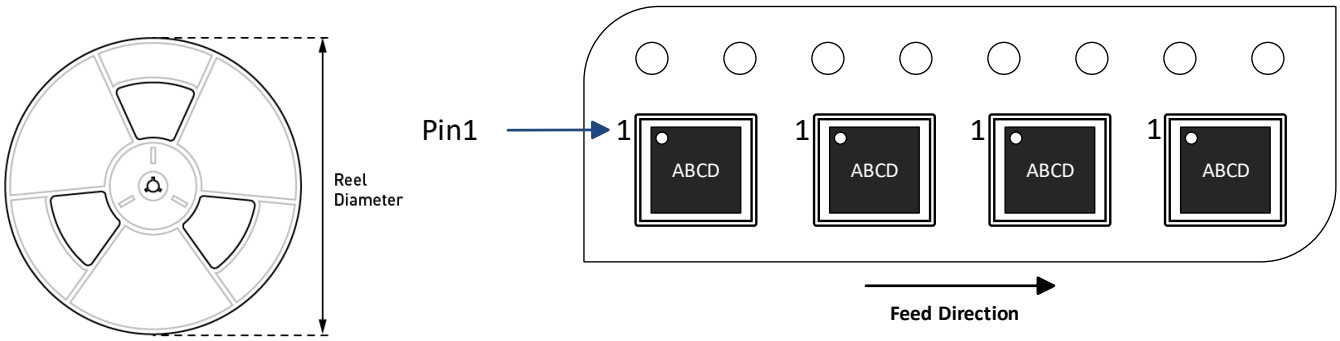


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch	Trailer Leader/ Reel
MP6543HGL	QFN-24 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm	125&125

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	12/8/2020	Initial Release	-

Mouser Electronics

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Monolithic Power Systems (MPS):

MP6543HGL-A-P MP6543HGL-A-Z MP6543HGL-B-P MP6543HGL-B-Z MP6543HGL-P MP6543HGL-Z