MP6543

12V, 2A, Three-Phase Power Stage

DESCRIPTION

The MP6543 family of products are all three-phase brushless DC motor drivers. They integrate three half-bridges, consisting of six N-channel power MOSFETs, along with pre-drivers, gate drive power supplies, and current-sense amplifiers.

The MP6543 has ENABLE and PWM inputs for each ½-H-bridge. The MP6543A has separate high-side and low-side inputs, while the MP6543B has Hall-element inputs. Otherwise, they are similar. References to the MP6543 in this document apply to the other parts, unless otherwise noted.

The MP6543 is able to deliver up 2A continuously (depending on thermal and PCB conditions), with the adjustable over-current protection threshold. It uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs, and a trickle-charge circuit to maintain sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MP6543, MP6543A, and MP6543B are available in a 24-pin, 3mmx4mm QFN package with an exposed thermal pad.

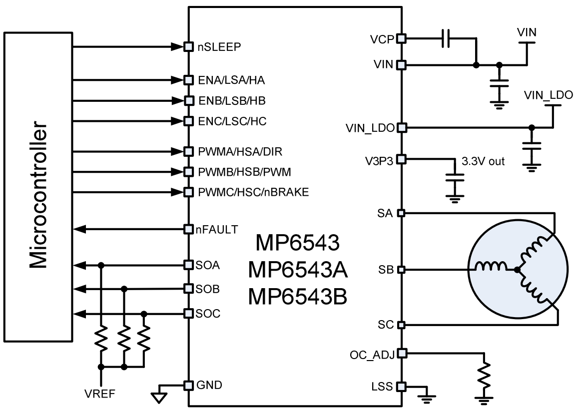
FEATURES

- 3V to 12V Operating Supply Voltage
- Three Integrated Half-Bridge Drivers
- 2A Continuous Output Current
- MOSFET On Resistance: 110mΩ per FET
- MP6543: ENBL & PWM Inputs
  MP6543A: LS & HS Inputs
  MP6543B: Hall-Signal Inputs
- Built-In 3.3V, 100mA LDO Regulator
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- Under-Voltage Lockout (UVLO) and Thermal Shutdown Protection
- Over-Current Protection (OCP) with Adjustable Threshold
- Integrated Bidirectional Current-Sense Amplifiers
- Available in a QFN-24 (3mmx4mm) Package

APPLICATIONS

- Three-Phase BLDC Motor Drivers

TYPICAL APPLICATION



MP6543/6543A/6543B Typical Application Circuit (QFN-24 3mmx4mm)

ORDERING INFORMATION

Part Number	Package	Top Marking
MP6543GL*	QFN-24 (3mmx4mm)	*See Below*
MP6543AGL**		
MP6543BGL***		

* For Tape & Reel, add suffix –Z (e.g. MP6543GL–Z).
**For Tape & Reel, add suffix –Z (e.g. MP6543AGL–Z).
***For Tape & Reel, add suffix –Z (e.g. MP6543BGL–Z).

TOP MARKING (MP6543GL)

MPYW
6543
LLL

MP: MPS prefix
Y: Year code
W: Week code
6543: First four digits of the part number
LLL: Lot number

TOP MARKING (MP6543AGL)

MPYW
6543
ALLL

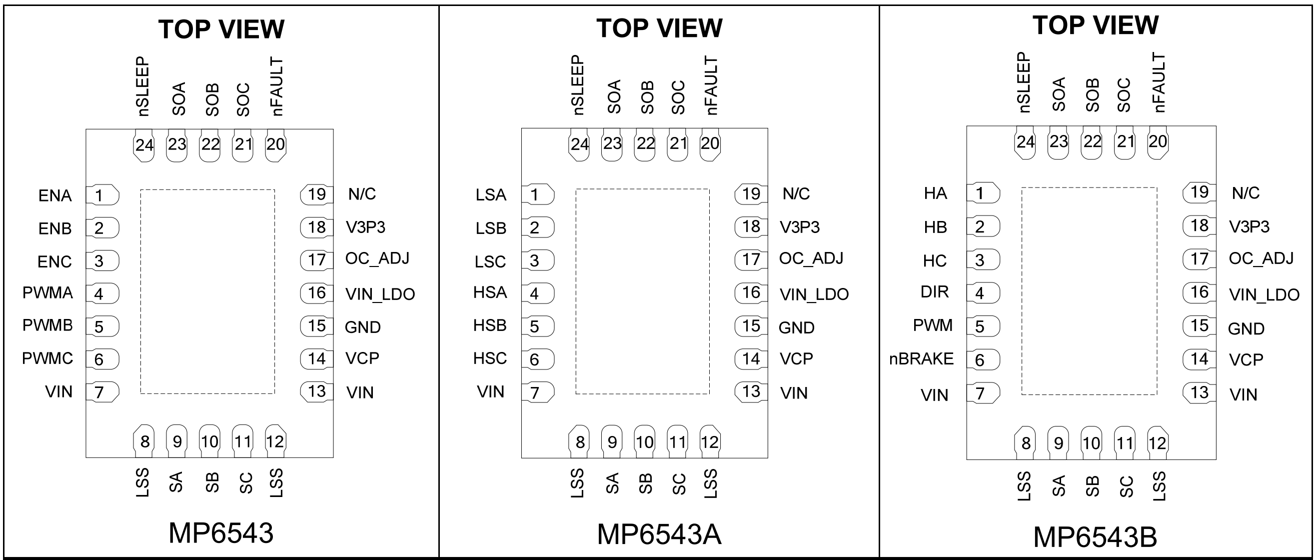
MP: MPS prefix
Y: Year code
W: Week code
6543A: First five digits of the part number
LLL: Lot number

TOP MARKING (MP6543BGL)

MPYW
6543
BLLL

MP: MPS prefix
Y: Year code
W: Week code
6543B: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-24 (3mmx4mm)

PIN FUNCTIONS

Pin #	MP6543 Name	MP6543A Name	MP6543B Name	Description
1	ENA	-	-	**Enable input for phase A.**
	-	LSA	-	**Enable LS-FET for phase A.**
	-	-	HA	**Hall-sensor input, phase A.**
2	ENB	-	-	**Enable input for phase B.**
	-	LSB	-	**Enable LS-FET for phase B.**
	-	-	HB	**Hall-sensor input, phase B.**
3	ENC	-	-	**Enable input for phase C.**
	-	LSC	-	**Enable LS-FET for phase C.**
	-	-	HC	**Hall-sensor input, phase C.**
4	PWMA	-	-	**PWM input for phase A.**
	-	HSA	-	**Enable HS-FET for phase A.**
	-	-	DIR	**Logic input to determine the direction of motor torque output.**
5	PWMB	-	-	**PWM input for phase B.**
	-	HSB	-	**Enable HS-FET for phase B.**
	-	-	PWM	**External PWM control for speed/torque.**
6	PWMC	-	-	**PWM input for phase C.**
	-	HSC	-	**Enable HS-FET for phase C.**
	-	-	nBRAKE	**Active-low logic input for a braking function.**

PIN FUNCTIONS *(continued)*

Pin #	MP6543 Name	MP6543A Name	MP6543B Name	Description
7	VIN			**Input power.**
8	LSS			**Low-side source connection for phases A, B, and C.** Must be connected directly to GND.
9	SA			**Phase A output.**
10	SB			**Phase B output.**
11	SC			**Phase C output.**
12	LSS			**Low-side source connection for phases A, B, and C.** Must be connected directly to GND.
13	VIN			**Input power.**
14	VCP			**Charge pump output.** Connect a 1µF ceramic capacitor to VIN.
15	GND			**Ground.**
16	VIN_LDO			**LDO input.**
17	OC_ADJ			**Over-current threshold programming pin.**
18	V3P3			**3.3V regulator output.** Low-side gate driver supply voltage. Bypass to GND with a 0.47µF ceramic capacitor.
19	N/C			**No connection.**
20	nFAULT			**Fault indication.** Open-drain output type, logic low when in fault condition.
21	SOC			**Current-sense output for phase C.**
22	SOB			**Current-sense output for phase B.**
23	SOA			**Current-sense output for phase A.**
24	nSLEEP			**Sleep mode input.** Logic low to enter low-power sleep mode. Internal pull-down.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}, V_{IN_LDO}) .... -0.3V to +18V
V_{SX} .... -0.3V to V_{IN} +0.3V
V_{CP} .... -0.3V to V_{IN} +5V
AGND to PGND .... -0.3V to +0.3V
Voltage at all other pins .... -0.3 to +5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (3mmx4mm) 2.6W
Junction temperature .... 150°C
Lead temperature...................................... 260°C
Storage temperature ....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 3V to 12V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-24 (3mmx4mm)	48	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may cause excessive die temperature, and the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Continuous current depends on PCB layout and ambient temperature.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 10V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}, V_{IN_LDO}		3		12	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		2.5	3.2	mA
	I_{SLEEP}	nSLEEP = 0		45	60	μA
Control Logic						
Input logic low threshold	V_{IL}				0.4	V
Input logic high threshold	V_{IH}		1.5			V
Logic input current	$I_{IN(H)}$	V = 3.3V	-20		20	μA
	$I_{IN(L)}$	V = 0V	-20		20	μA
Power-up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		1.5		ms
Internal pull-down resistance	R_{PD}	All logic Inputs		500		kΩ
nFAULT pull-down R_{ON}	$R_{ON(NFAULT)}$			15		Ω
V3P3 REGULATOR						
LDO output		IOUT = 0 to 100 mA	3.3	3.45	3.6	V
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	2.5	2.7	2.9	V
UVLO hysteresis	ΔV_{UVLO}			150		mV
OCP threshold	I_{OCP}	ROCP = 0	4.7	6.2	8	A
		ROCP = float	5.5	7.2	9	A
OCP deglitch time	t_{OCD}			1		μs
Thermal shutdown (6)	T_{TSD}	T_J rising		160		°C
Thermal shutdown hysteresis (6)	ΔT_{TSD}			25		°C
Current Sense						
Current-sense ratio			1/3600	1/4000	1/4400	A/A
Current-sense output current		LS-FET current = 1A	225	250	275	μA
		LS-FET current = -1A	-275	-250	-225	μA
Current-sense output current		LS-FET current = 100mA	22.5	25	27.5	μA
		LS-FET current = -100mA	-27.5	-25	-22.5	μA
Positive and negative matching (ratio of positive to negative)		LS-FET current = ±1A, ±100mA	95%	1	105%	
Phase matching (ratio of phase to phase)		LS-FET current = ±1A, ±100mA	95%	1	105%	
Current-sense output voltage swing		LS-FET current = ±0.25A	0		3.6	V
Output						
HS-FET on resistance	$R_{ON(HS)}$	IOUT = 1A	90	110	135	mΩ
LS-FET on resistance	$R_{ON(LS)}$	IOUT = 1A	85	105	125	mΩ
Output rise time (6)		R_{LOAD} = 50Ω		25		ns
Output fall time (6)		R_{LOAD} = 50Ω		25		ns
Dead time (6)		R_{LOAD} = 50Ω		40		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 10V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

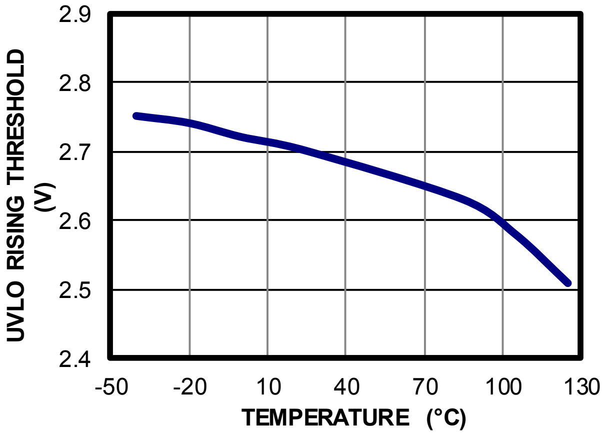
Parameter	Symbol	Condition	Min	Typ	Max	Units
PWMx to Sx delay time rising (6)				70		ns
PWMx to Sx delay time falling (6)				70		ns
Charge Pump						
Charge pump output voltage	V_{CP}			V_{IN} + 3.3		V

Note:

6) Guaranteed by design.

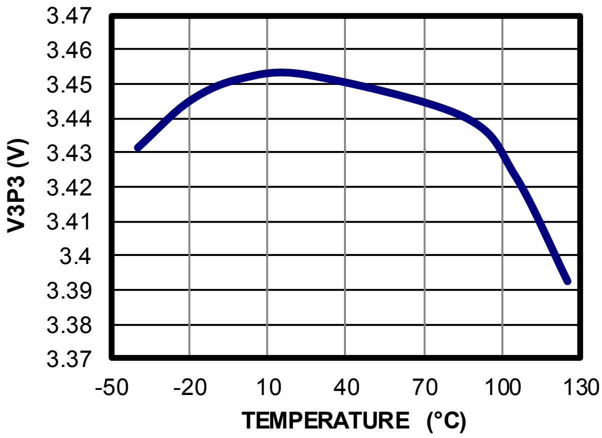
TYPICAL CHARACTERISTICS

UVLO Rising Threshold vs. Temperature



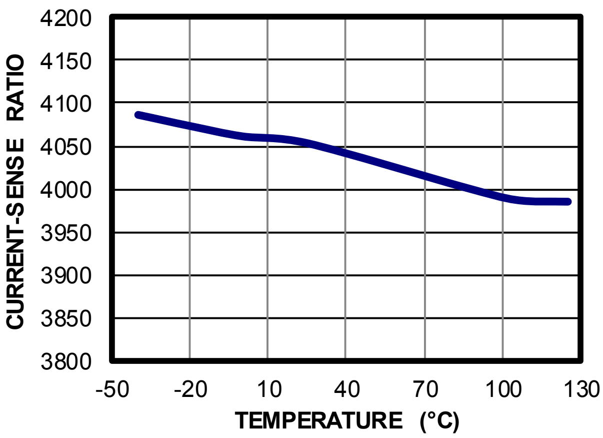
V3P3 vs. Temperature

V_{IN_LDO} = 10V, LDO_LOAD = 100mA



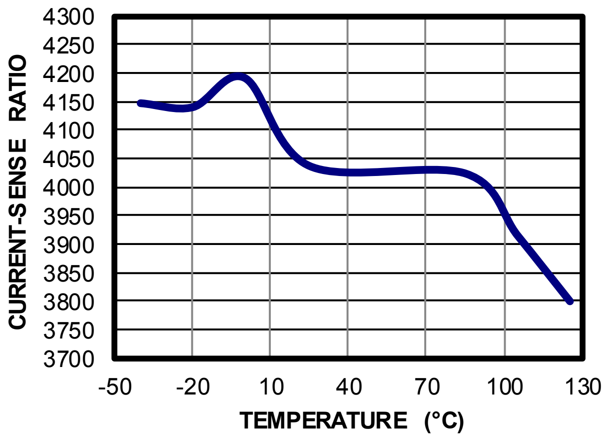
A-Phase Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



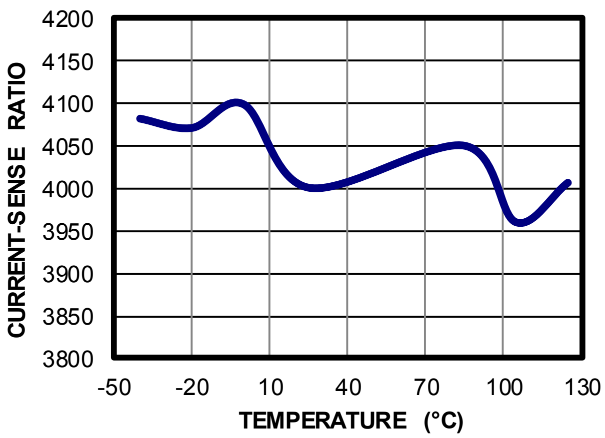
B-Phase Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



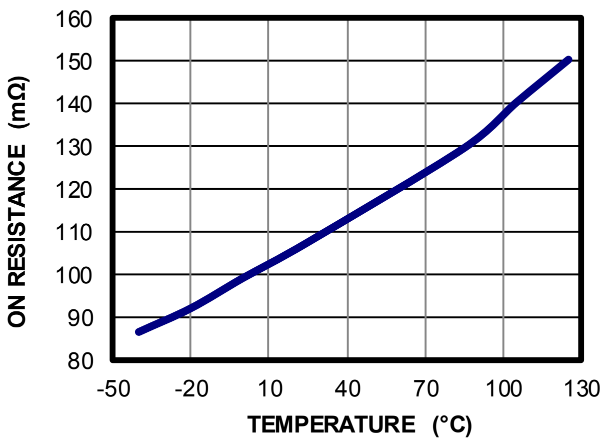
C-Phase Current-Sense Ratio vs. Temperature

I_{OUT} = 1A



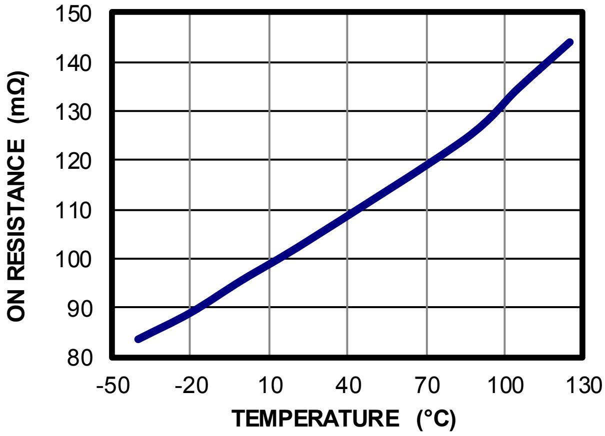
HS On Resistance vs. Temperature

I_{OUT} = 1A



TYPICAL CHARACTERISTICS *(continued)*

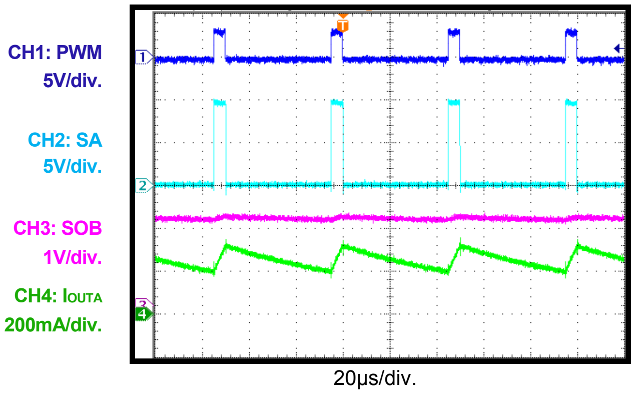
LS On Resistance vs. Temperature
I_{OUT} = 1A



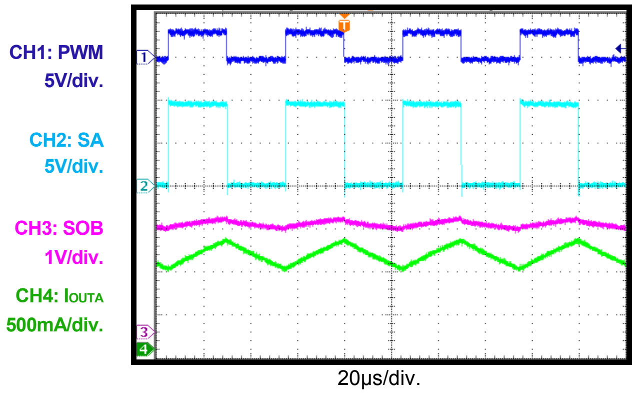
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{IN_LDO} = 10V, A-phase switching with 20kHz frequency, B-phase LS on, C-phase disable, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 2Ω + 0.2mH/phase with star connection, unless otherwise noted.

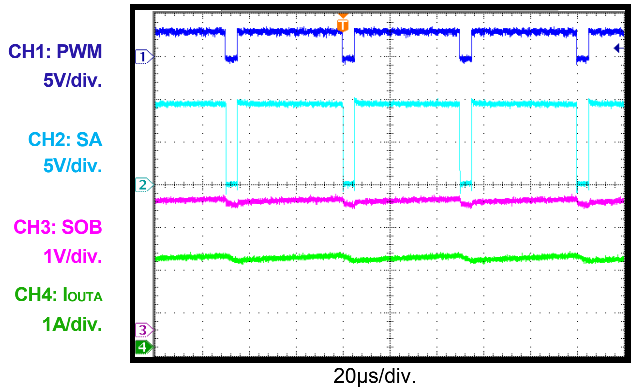
Steady State
Duty = 10%



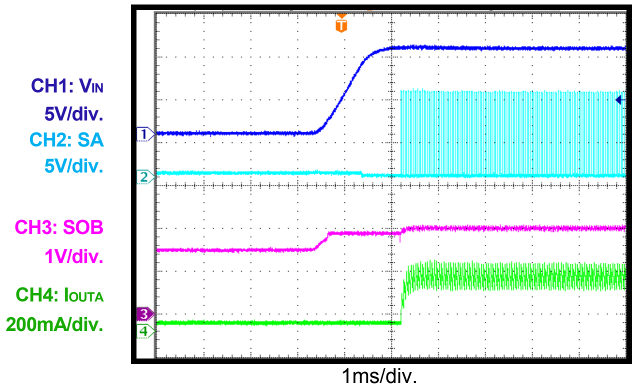
Steady State
Duty = 50%



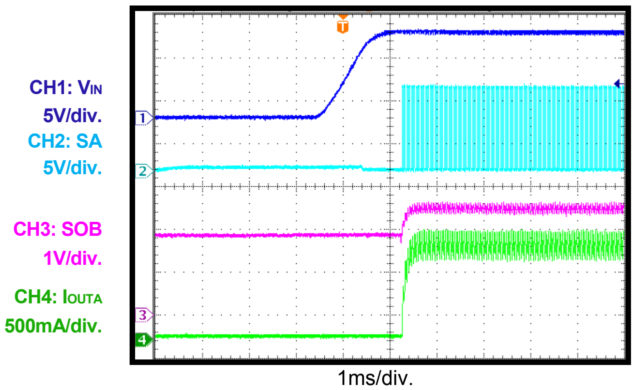
Steady State
Duty = 90%



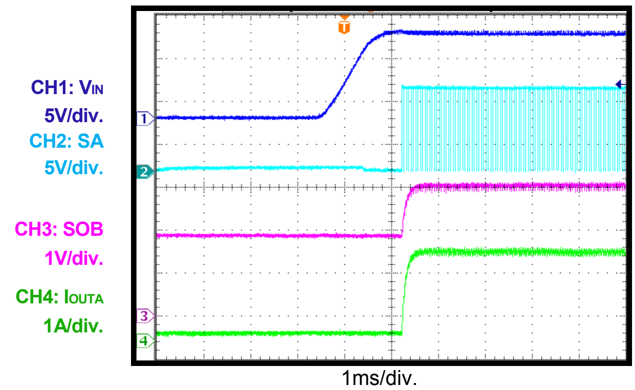
Power Ramp-Up
Duty = 10%



Power Ramp-Up
Duty = 50%



Power Ramp-Up
Duty = 90%

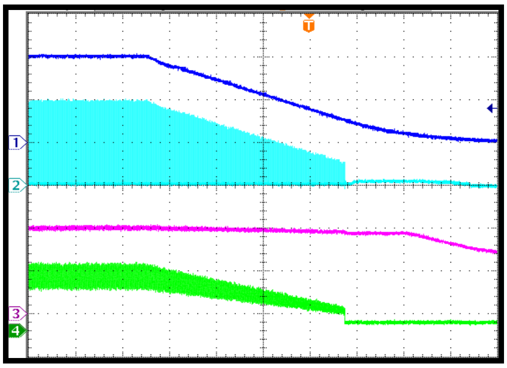


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{IN_LDO} = 10V, A-phase switching with 20kHz frequency, B-phase LS on, C-phase disable, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 2Ω + 0.2mH/phase with star connection, unless otherwise noted.

Power Ramp-Down
Duty = 10%

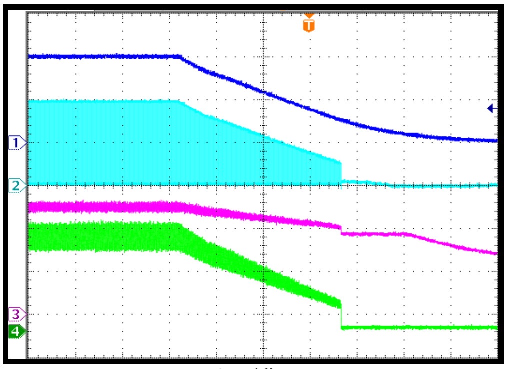
CH1: V_{IN} 5V/div.
CH2: SA 5V/div.
CH3: SOB 1V/div.
CH4: I_{OUTA} 200mA/div.



4ms/div.

Power Ramp-Down
Duty = 50%

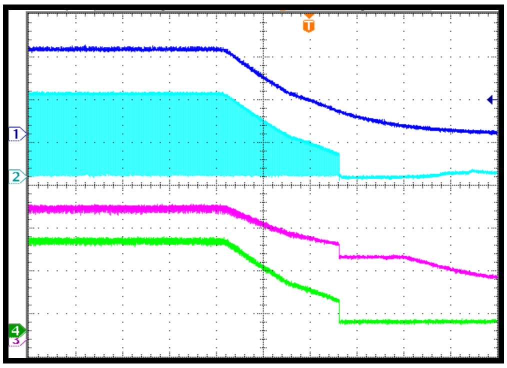
CH1: V_{IN} 5V/div.
CH2: SA 5V/div.
CH3: SOB 1V/div.
CH4: I_{OUTA} 500mA/div.



4ms/div.

Power Ramp-Down
Duty = 90%

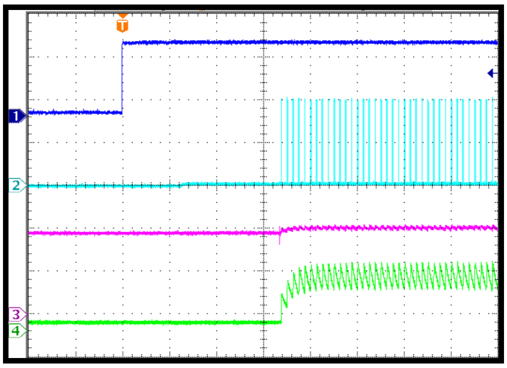
CH1: V_{IN} 5V/div.
CH2: SA 5V/div.
CH3: SOB 1V/div.
CH4: I_{OUTA} 1A/div.



4ms/div.

Sleep Recovery
Duty = 10%

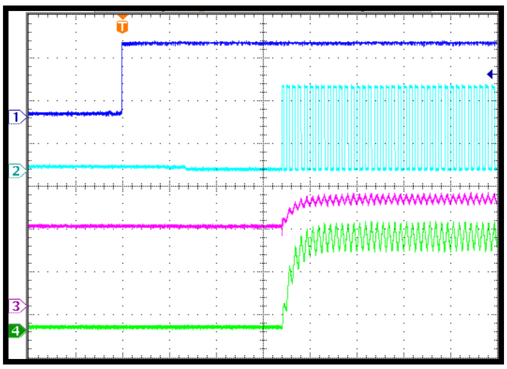
CH1: nSLEEP 2V/div.
CH2: SA 5V/div.
CH3: SOB 1V/div.
CH4: I_{OUTA} 200mA/div.



400µs/div.

Sleep Recovery
Duty = 50%

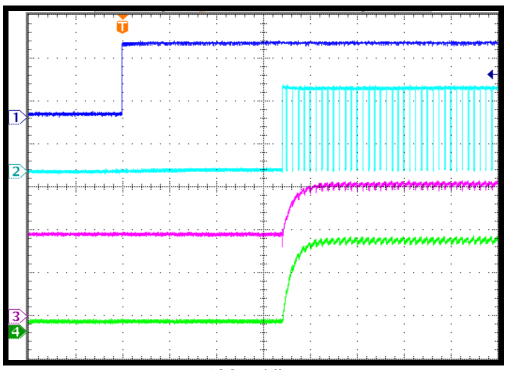
CH1: nSLEEP 2V/div.
CH2: SA 5V/div.
CH3: SOB 1V/div.
CH4: I_{OUTA} 500mA/div.



400µs/div.

Sleep Recovery
Duty = 90%

CH1: nSLEEP 2V/div.
CH2: SA 5V/div.
CH3: SOB 1V/div.
CH4: I_{OUTA} 1A/div.

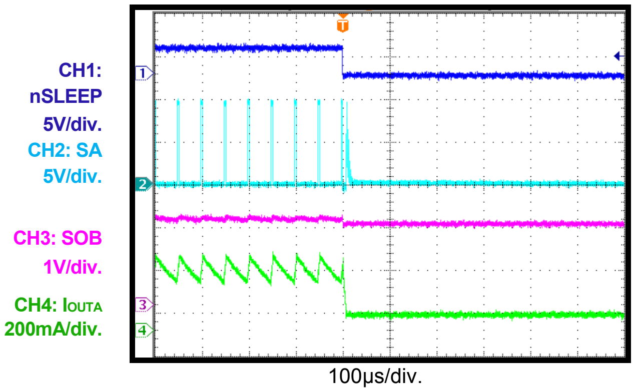


400µs/div.

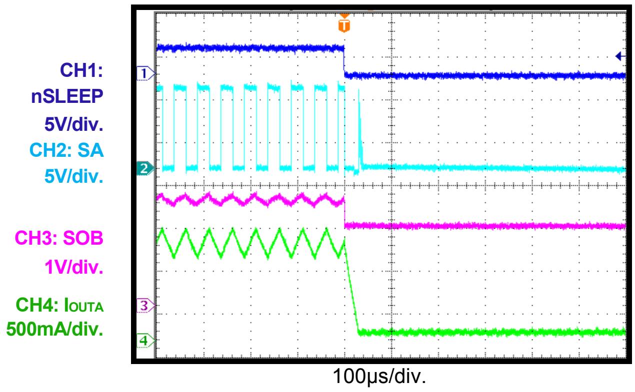
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{IN_LDO} = 10V, A-phase switching with 20kHz frequency, B-phase LS on, C-phase disable, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 2Ω + 0.2mH/phase with star connection, unless otherwise noted.

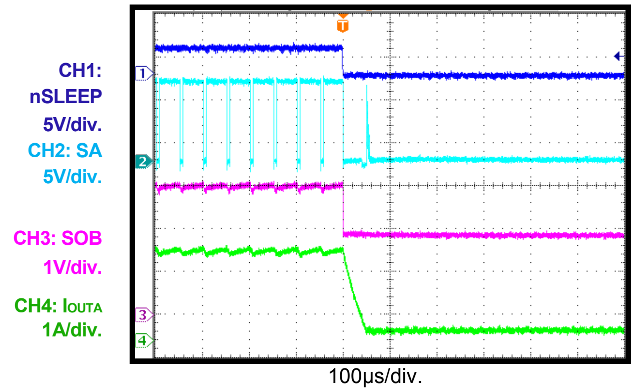
Sleep Entry
Duty = 10%



Sleep Entry
Duty = 50%



Sleep Entry
Duty = 90%



FUNCTIONAL BLOCK DIAGRAM (MP6543/MP6543A/MP6543B)

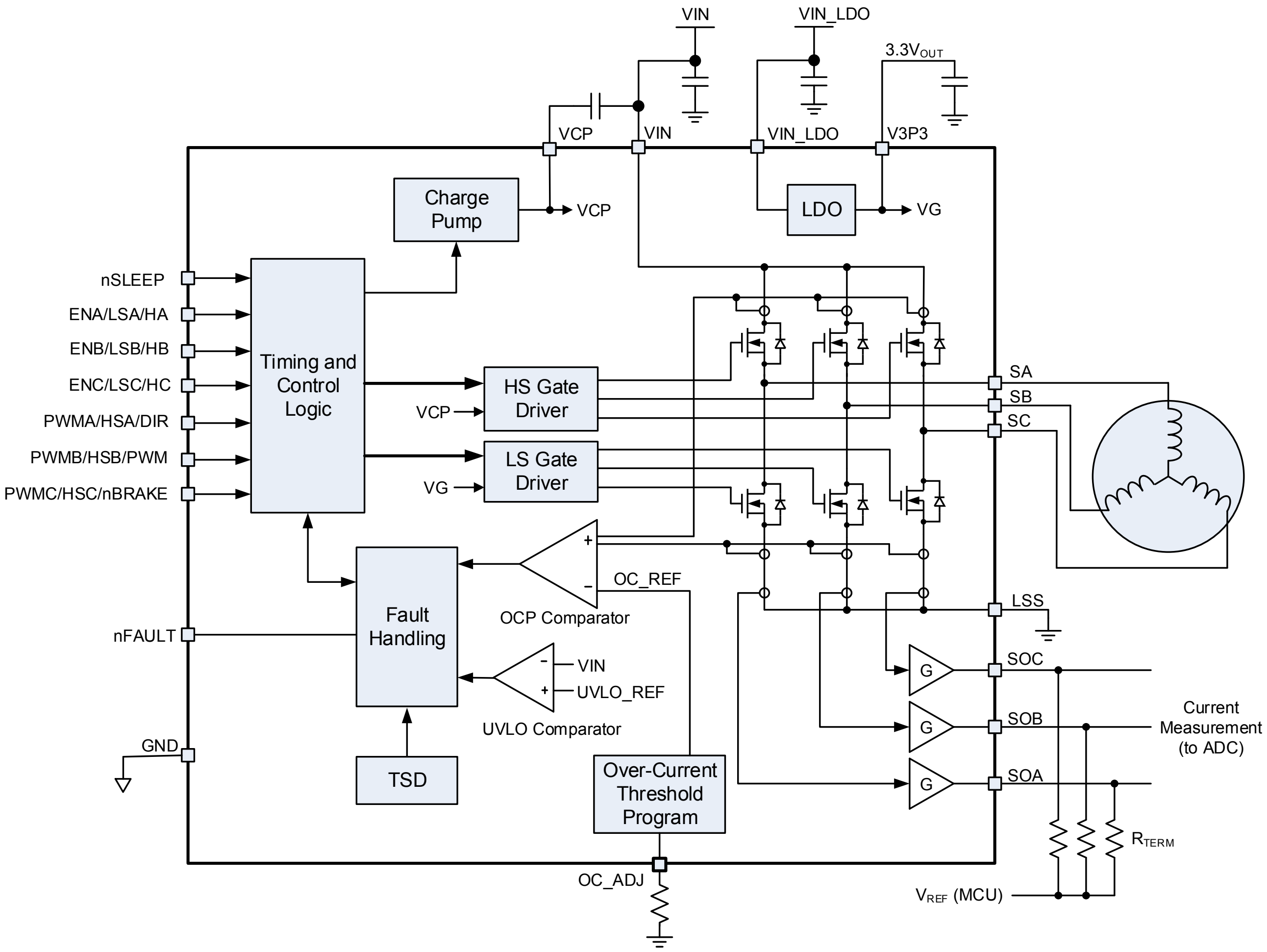


Figure 1: Functional Block Diagram

OPERATION

The MP6543 is a three-channel half-bridge driver intended to drive a brushless DC motor.

Input Logic

The MP6543 has logic input pins ENA, ENB, and ENC, which enable the outputs SA, SB, and SC. When ENx is low, the corresponding output is disabled (output is high-impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output. Table 1.1 shows the logic truth table.

Table 1.1: Input Logic Truth Table of the MP6543

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	High impedance

The MP6543A has separate inputs to enable the HS-FETs and LS-FETs of each phase independently. Table 1.2 shows the logic truth table.

Table 1.2: Input Logic Truth Table of the MP6543A

HSx	LSx	Sx
L	L	High impedance
L	H	GND
H	L	VIN
H	H	High impedance

The MP6543B has three Hall-element inputs, whose commutation logic is determined by three Hall-element inputs spaced at 120°. The PWM, DIR, and nBRAKE inputs control motor speed, direction, and brake engagement, respectively.

Table 1.3: Input Logic Truth Table of the MP6543B

PWM	nBRAKE	Operation Mode
0	1	PWM chop mode – the load current decays
0	0	Brake mode – all low-side gates on
1	1	Selected drivers on
1	0	Brake mode – all low-side gates on

Table 2: Commutation Table of the MP6543B (nBRAKE = 1)

Logic Inputs				Motor Terminals		
HA	HB	HC	DIR	SA	SB	SC
1	0	1	1	PWM	Z	L
1	0	0	1	Z	PWM	L
1	1	0	1	L	PWM	Z
0	1	0	1	L	Z	PWM
0	1	1	1	Z	L	PWM
0	0	1	1	PWM	L	Z
1	0	1	0	L	Z	PWM
0	0	1	0	L	PWM	Z
0	1	1	0	Z	PWM	L
0	1	0	0	PWM	Z	L
1	1	0	0	PWM	L	Z
1	0	0	0	Z	L	PWM
0	0	0	X	Z	Z	Z
1	1	1	X	Z	Z	Z

Note that the logic inputs have internal weak pull-down resistors.

nSLEEP Operation

Driving nSLEEP low puts the device into a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, approximately 1.5ms must pass before the device responds to inputs. The nSLEEP input has a weak pull-down resistor.

Current-Sense Amplifiers

The current flowing in each of the three outputs is sensed by internal current-sensing circuits. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. Note that only current flowing in the LS-FET is sensed, and that it is sensed in both the forward and reverse directions.

To convert this current into a voltage (e.g. to input to an A/D converter), a termination resistor (R_{REF}) is used as a reference voltage. When there is no current flowing, the resultant output will be equal to the reference voltage. When current is flowing, the voltage is above or below the reference voltage, determined with Equation (1):

$$V_{SOUT} = V_{REF} + (R_{REF} * I_{LOAD}) / 4000 \quad (1)$$

To terminate the outputs when using an A/D converter with inputs that are ratiometric to its supply voltage, use two equal-value resistors to the ADC supply and ground. The resulting ADC code will be half-scale at zero current. Figure 2 shows a simplified drawing of the current measurement circuit.

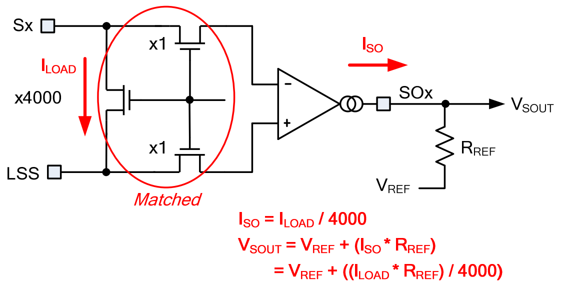


Figure 2: Current Measurement Circuit Diagram

Automatic Synchronous Rectification

When driving current through an inductive load, if the output MOSFETs are both turned off, the recirculation current must continue to flow. This current is normally passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6543 implements automatic synchronous rectification.

When both the HS-FET and LS-FET are turned off and the voltage on an Sx output pin is driven below ground, the LS-FET turns on until the current flowing through it reaches zero, or the HS-FET turns on. Similarly, if the voltage on the Sx pin rises above V_{IN}, the HS-FET turns on until the current reaches zero, or the LS-FET turns on.

nFAULT Output

The MP6543 provides an nFAULT output pin, which is driven active low in a fault condition, such as over-current protection (OCP) or over-temperature protection (OTP). This pin is an open-drain output, and must be pulled up by an external pull-up resistor.

Input UVLO Protection

If the voltage on VIN falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic is reset. Normal operation resumes when V_{IN} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, all output FETs are disabled and nFAULT is driven low. Normal operation resumes when the die temperature has fallen to a safe level.

Over-Current Protection

The OCP circuit limits the current through each FET by disabling its gate driver. If the over-current limit threshold is reached, and lasts for longer than the over-current deglitch time, all six output FETs are disabled (outputs become high-impedance) and nFAULT is driven low. The current is then recirculated through the body diodes. The over-current shutdown is latched until either nSLEEP is reset or VIN is power-cycled.

Over-current conditions on both high-side and low-side devices (e.g. a short to ground, supply, or across the motor winding) all result in an over-current shutdown. Figure 3 shows a simplified diagram of the OCP circuit for one output.

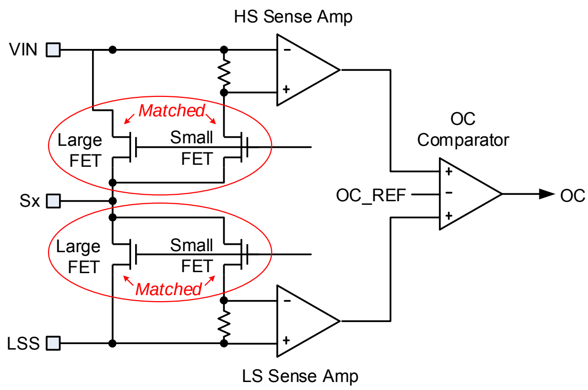


Figure 3: OCP Circuit

OC_ADJ values are outside the specified value range for over-current threshold.

Table 3: Over-Current Threshold

OC_ADJ Resistor Value	Typ OC Threshold
0	6.2A
Float	7.2A

3.3V LDO Output

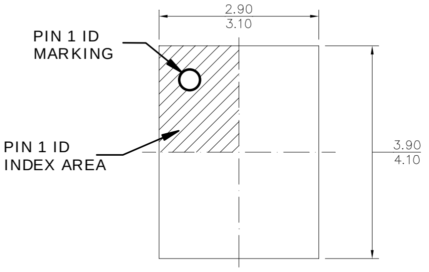
An internal LDO regulator generates a 3.3V voltage with 100mA capacity, which can be used to power a small low-power microcontroller. A bypass capacitor between 4.7μF and 10μF is required from the V3P3 pin to ground.

Charge Pump

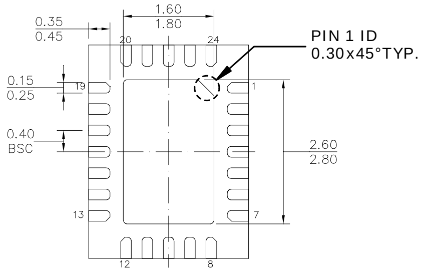
A charge pump is used to generate the gate drive for the high-side FETs. The charge pump requires one external, 1µF ceramic capacitor rated for at least 10V between VIN and VCP.

PACKAGE INFORMATION

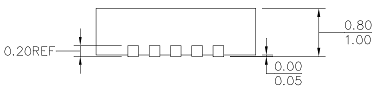
QFN-24 (3mmx4mm)



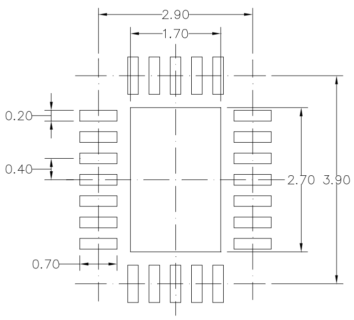
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.