MP4316

45V, 6A, Low I_Q, Synchronous Step-Down Converter with Frequency Spread Spectrum

DESCRIPTION

The MP4316 is a frequency-configurable, synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It can achieve up to 6A of highly efficient, continuous output current (I_{OUT}) with current control mode for fast loop response.

The wide 3.3V to 45V input voltage (V_{IN}) range accommodates a variety of step-down applications in an automotive input environment. The device's 1.7μA shutdown current (I_{SD}) makes it ideal for battery-powered applications.

The MP4316 provides high power conversion efficiency across the entire load range. Advanced asynchronous modulation (AAM) mode achieves high efficiency under light-load conditions by scaling down the switching frequency (f_{SW}) to reduce the switching and gate driver losses.

An open-drain power good (PG) signal indicates whether the output is between 95% and 105% of its nominal voltage. High duty cycle and low-dropout (LDO) mode enable the device to withstand automotive cold-crank conditions.

Full protection features include frequency foldback to prevent inductor current (I_L) runaway during start-up, over-current protection (OCP) with hiccup mode, and thermal shutdown for reliable, fault-tolerant operation.

The MP4316 is available in a QFN-20 (4mmx4mm) package.

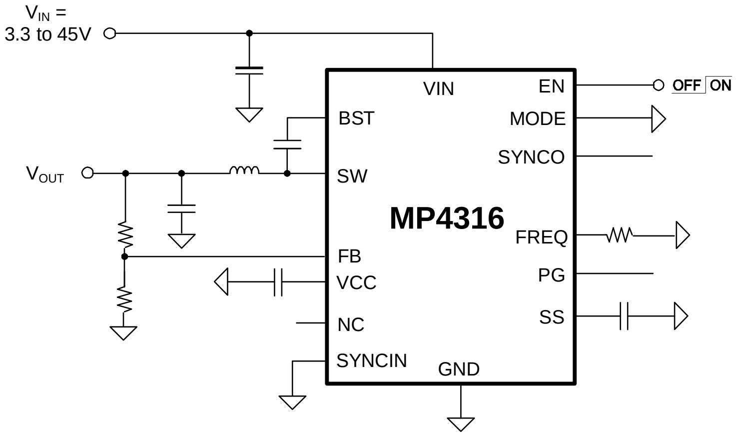
FEATURES

- Wide 3.3V to 45V Operating Input (V_{IN}) Voltage Range
- Up to 6A of Continuous Output Current (I_{OUT})
- Low 1.7μA Shutdown Current (I_{SD})
- 18μA Sleep Mode Quiescent Current (I_Q)
- Internal 48mΩ and 20mΩ Power MOSFETs
- 350kHz to 1000kHz Configurable Switching Frequency (f_{SW}) for Car Battery Applications
- External SYNC Clock
- Out-of-Phase Synchronized Clock Output
- Frequency Spread Spectrum (FSS) for Low Electromagnetic Interference (EMI)
- Symmetric V_{IN} for Low EMI
- Power Good (PG) Output
- External Soft Start (SS)
- 100ns Minimum On Time (t_{ON_MIN})
- Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM)
- Low-Dropout (LDO) Mode
- Over-Current Protection (OCP) with Hiccup Mode
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package

APPLICATIONS

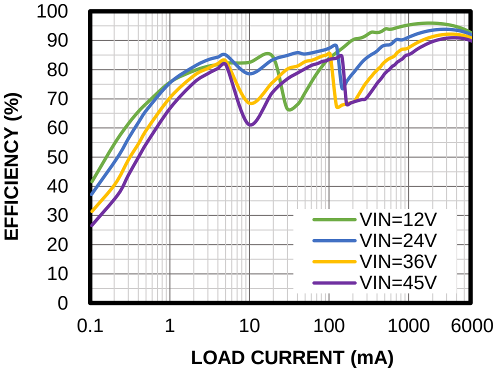
- Radios
- Battery-Powered Systems
- General-Purpose Consumer Applications
- Industrial Power Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 470kHz, L = 4.7μH, DCR = 15mΩ, AAM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MP4316GRE***	QFN-20 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP4316GRE-Z).

** Moisture Sensitivity Level Rating

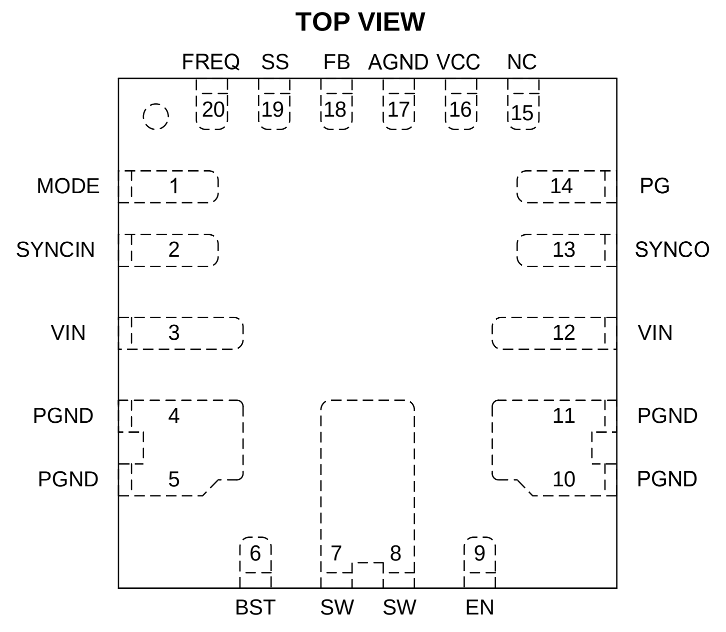
*** Wettable Flank

TOP MARKING

MPSYWW
MP4316
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4316: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**Mode selection.** Pull the MODE pin high to make the converter operate in forced continuous conduction mode (FCCM). Pull MODE low to make the converter operate in advanced asynchronous modulation (AAM) mode. Do not float MODE.
2	SYNCIN	**Synchronous input.** Apply a 350kHz and 1000kHz clock signal to the SYNCIN pin to synchronize the internal oscillator frequency to the external clock. SYNCIN has an internal high impedance (Hi-Z). If using SYNCIN, ensure that the external SYNC clock has an adequate pull-up and pull-down resistance. If the external clock's pull-down resistance is not sufficient, or if SYNCIN enters a Hi-Z state, place a ≤51kΩ resistor between the SYNCIN pin and AGND. Do not float SYNCIN.
3, 12	VIN	**Input supply.** The VIN pin powers the internal circuitry and the high-side MOSFET (HS-FET) connected to the SW pin. To minimize switching spikes at the input, connect a decoupling capacitor between the VIN pin and PGND. Place this capacitor close to VIN.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** The BST pin is the positive power supply for the HS-FET. Connect a bypass capacitor between the BST and SW pins. For more information, see the Selecting the External Bootstrap (BST) Diode and Resistor section on page 32.
7, 8	SW	**Switch output.** The SW pin is the output of the internal power MOSFETs.
9	EN	**Enable.** Pull the EN pin above 1V to turn the converter on; pull EN below 0.85V to turn it off.
13	SYNCO	**Synchronous output.** The SYNCO pin outputs a clock that is 180° out-of-phase with the internal oscillator. SYNCO can also output a signal opposite of the clock applied at the SYNCIN pin. Float SYNCO if not used.
14	PG	**Power good indicator.** The PG pin is an open-drain output. Connect PG to a power source via a pull-up resistor. If the output voltage (V_{OUT}) is between 95% and 105% of the nominal voltage, PG is pulled high. If V_{OUT} exceeds 106.5% or drops below 93% of the nominal voltage, PG is pulled low.
15	NC	**Not connected.** Float the NC pin if not used.
16	VCC	**Bias supply.** The VCC pin supplies 4.9V to the internal control circuit and gate drivers. Connect a decoupling capacitor from VCC to AGND. Place this capacitor close to VCC. For information, see the Selecting the VCC Capacitor (C_{VCC}) section on page 32.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** To set V_{OUT}, connect the FB pin to the center of the external resistor divider connected between the output and AGND. The feedback (FB) voltage (V_{FB}) is about 0.815V. Place the resistor divider as close to FB as possible. Keep vias away from the FB traces.
19	SS	**Soft-start input.** Place a capacitor between the SS pin and AGND to set the soft-start time (t_{SS}). During start-up, SS provides 13µA to the soft-start capacitor (C_{SS}). As the SS voltage (V_{SS}) increases, V_{FB} increases to limit the input inrush current during start-up.
20	FREQ	**Switching frequency setting.** Connect a resistor from the FREQ pin to AGND to set the switching frequency (f_{SW}). For more information, see the f_{SW} vs. R_{FREQ} curves on page 15.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN	-0.3V to +50V
SW	-0.3V to V_{IN_MAX} + 0.3V
BST	V_{SW} + 5.5V
All other pins	-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (5)	
QFN-20 (4mmx4mm)	5.4W
Operating junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

ESD Ratings

Human body model (HBM)	±2kV
Charged device model (CDM)	±750V

Recommended Operating Conditions

Input voltage (V_{IN})	3.3V to 45V
Output voltage (V_{OUT})	0.815V to 0.95 x V_{IN}
Operating junction temp (T_J)	-40°C to +125°C (3)

Thermal Resistance

	θ_{JA}	θ_{JC}	
QFN-20 (4mmx4mm)			
JESD51-7 (4)	44	9	°C/W
EVQ4316-R-00A (5)	23	2.5	°C/W

Notes:

1) Exceeding these ratings may damage the device.

2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

3) An operating junction temperature above 125°C may be supported. Contact MPS for details.

4) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

5) Measured on an MPS standard evaluation board (9cmx9cm), thick 2oz copper, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\ UVLO\_RISING}$		2.8	3	3.2	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.5	2.7	2.9	V
V_{IN} UVLO hysteresis	$V_{IN\ UVLO\_HYS}$			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC voltage regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
Quiescent current during sleep mode	I_{SLEEP}	V_{FB} = 0.85V, sleep mode, no load		18	26	μA
Quiescent current (7)	I_Q	MODE is low, advanced asynchronous modulation (AAM) mode, no load, switching, R_{FB_PU} = 1MΩ, R_{FB_PD} = 324kΩ		20		μA
		MODE is high, forced continuous conduction mode (FCCM), switching, no load, f_{SW} = 2MHz		40		mA
		MODE is high, FCCM, no load, switching, f_{SW} = 470kHz		9.5		mA
Shutdown current	I_{SD}	V_{EN} = 0V		1.7	3.5	μA
Feedback (FB) voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	0.807	0.815	0.823	V
		V_{IN} = 3.3V to 45V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (7)	t_{ON_MIN}			100		ns
Minimum off time (7)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		Deg
High-side MOSFET (HS-FET) peak current limit	I_{LIMIT_PEAK}	30% duty cycle	10	13	16	A
Low-side MOSFET (LS-FET) valley current limit	I_{LIMIT_VALLEY}		8	10	12	A
Zero-current detection (ZCD) current	I_{ZCD}	AAM mode	-0.15	0.1	+0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	7	A
Switch leakage current	I_{SW_LKG}			0.01	1	μA
HS-FET on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		48	80	mΩ
LS-FET on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	8	13	19	μA
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG rising threshold	V_{PG_RISING}	V_{FB} rising, V_{FB} / V_{REF}	92	95	98	% of V_{REF}
		V_{FB} falling, V_{FB} / V_{REF}	102	105	108	
PG falling threshold	$V_{PG\_FALLING}$	V_{FB} falling, V_{FB} / V_{REF}	90.5	93.5	96.5	
		V_{FB} rising, V_{FB} / V_{REF}	103.5	106.5	109.5	
PG output low voltage	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_DELAY\_RISING}$			35		µs
PG falling delay	$t_{PG\_DELAY\_FALLING}$			35		µs
Thermal shutdown (7)	T_{SD}			170		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C

Notes:

6) Guaranteed by over-temperature correlation. Not tested in production.
7) Derived from bench characterization. Not tested in production.

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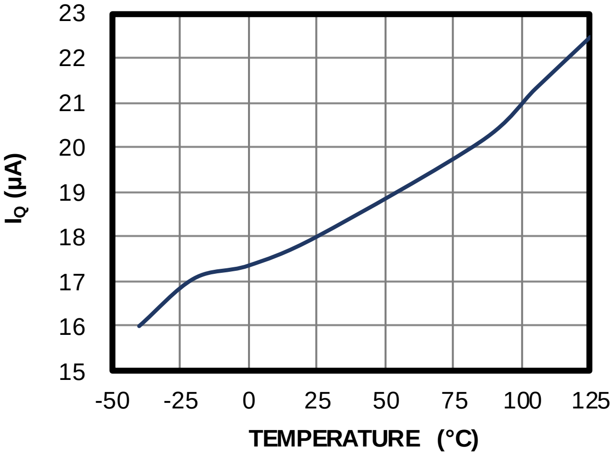
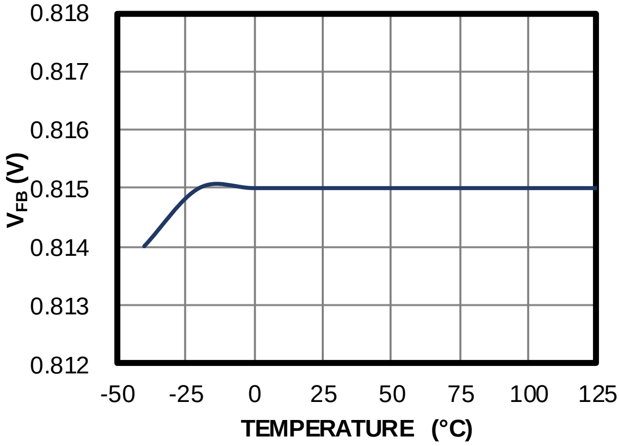
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

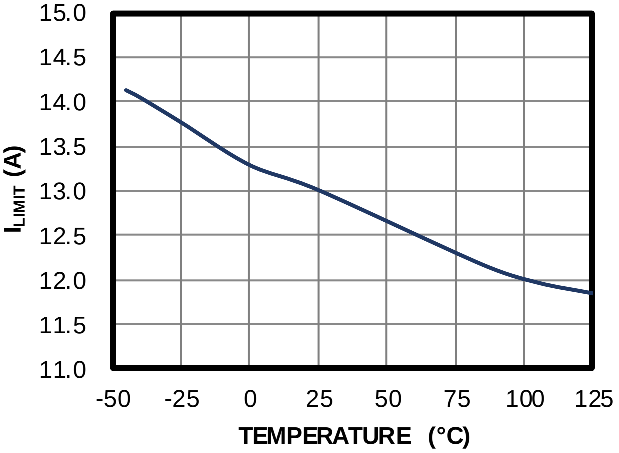
Quiescent Current vs. Temperature



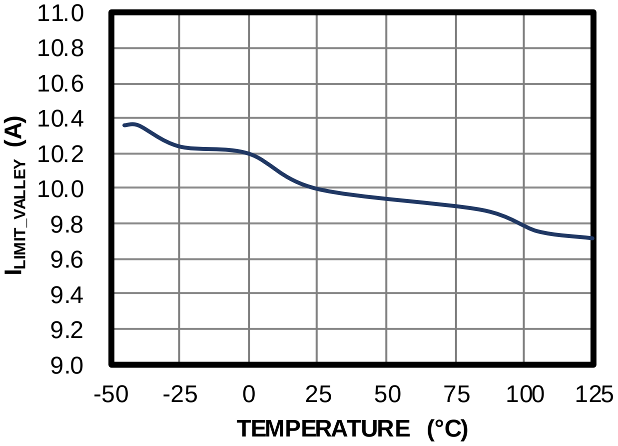
Feedback Voltage vs. Temperature



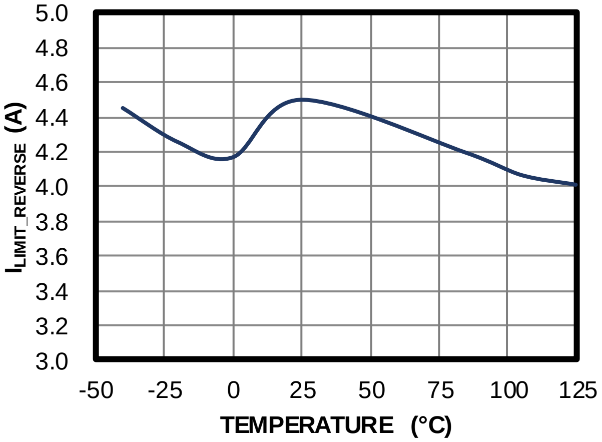
Current Limit vs. Temperature



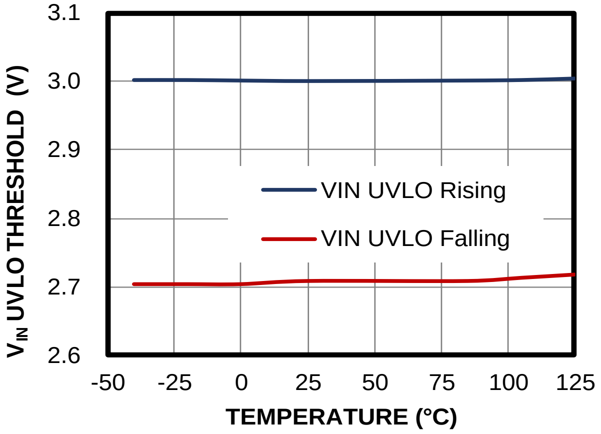
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature

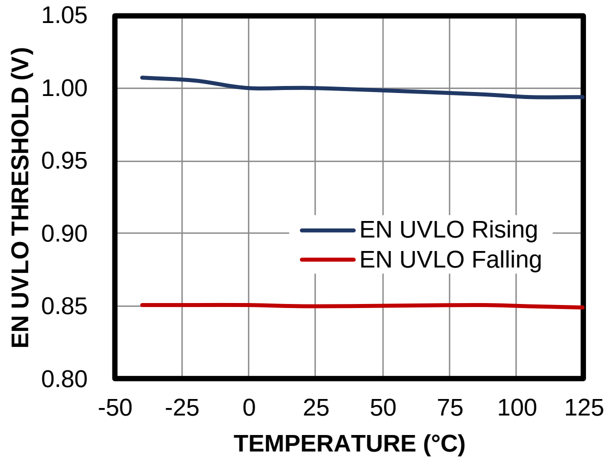


V_{IN} UVLO Threshold vs. Temperature

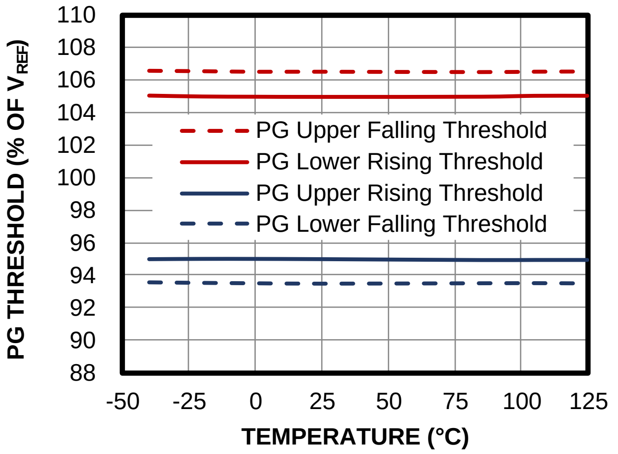


TYPICAL CHARACTERISTICS *(continued)*

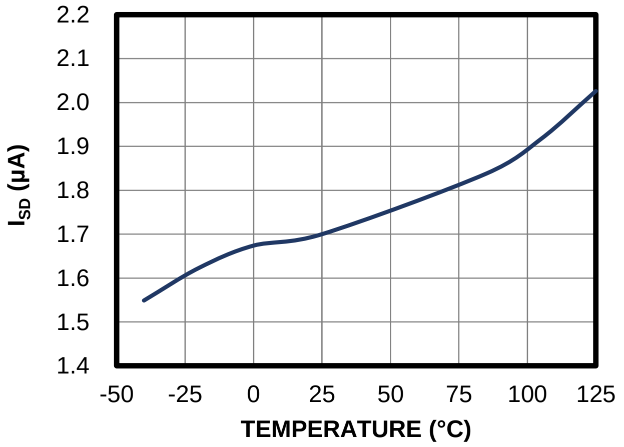
V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.



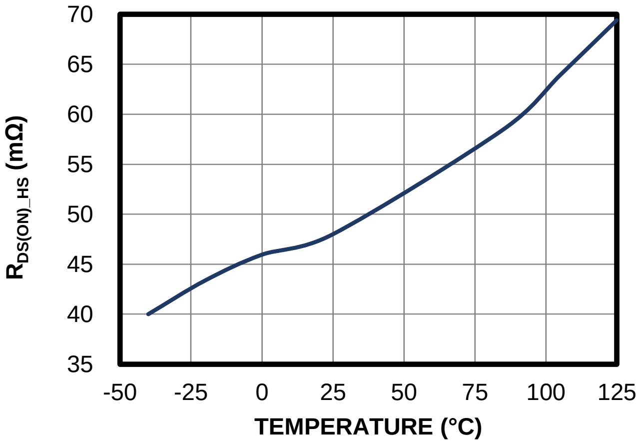
EN UVLO Threshold vs. Temperature



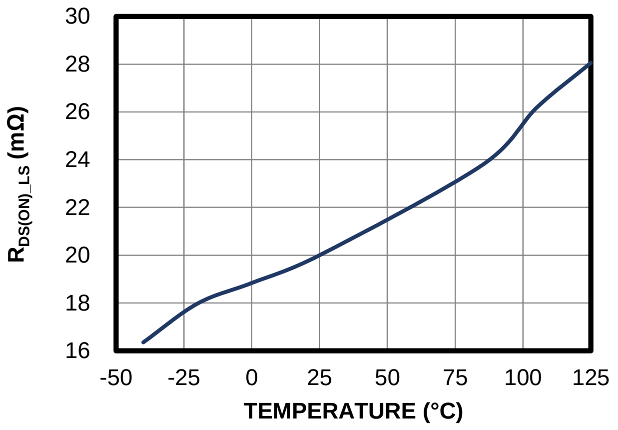
PG Threshold vs. Temperature



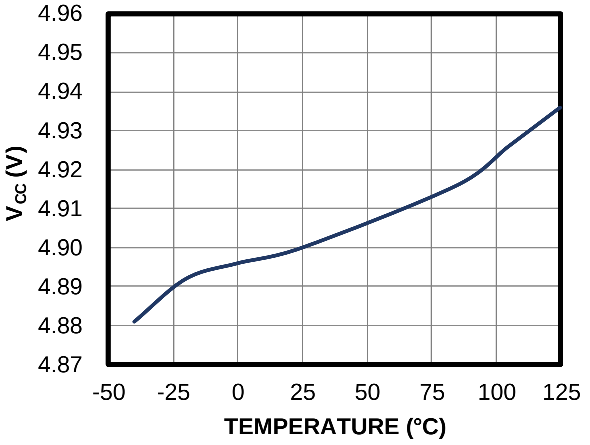
Shutdown Current vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature

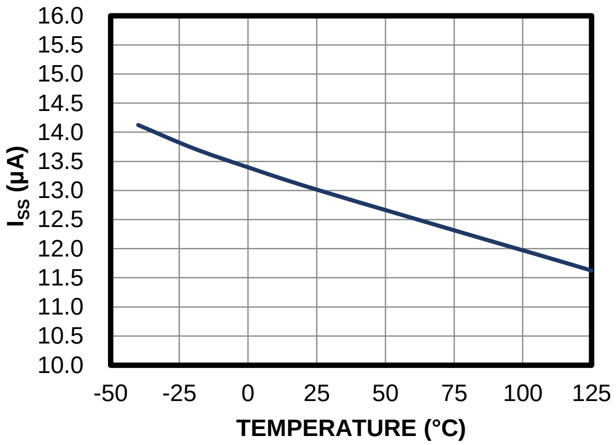


V_{CC} vs. Temperature

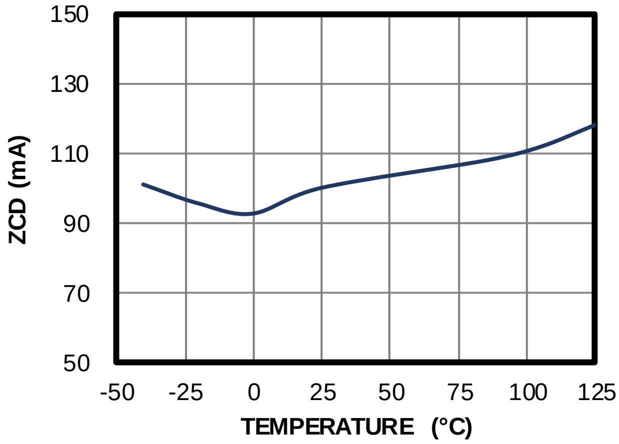
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

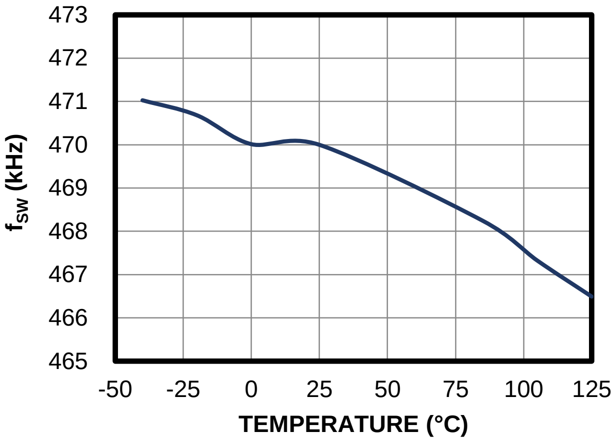


Zero-Current Detection vs. Temperature



Switching Frequency vs. Temperature

R_{FREQ} = 62kΩ

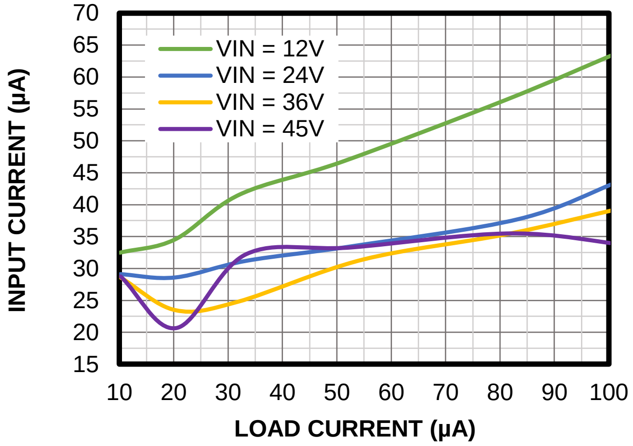


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH $^{(8)}$, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

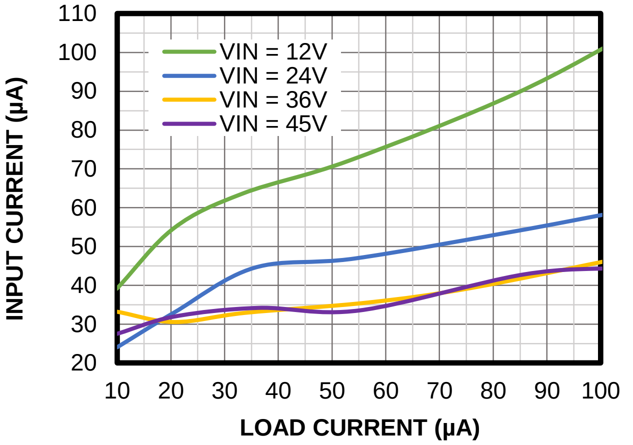
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V



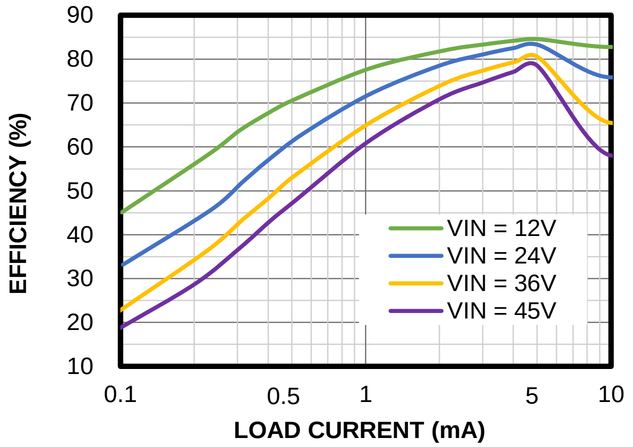
Input Current vs. Load Current

AAM mode, V_{OUT} = 5V



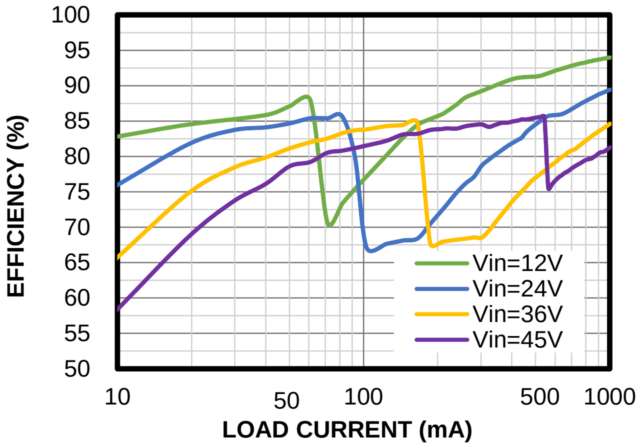
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



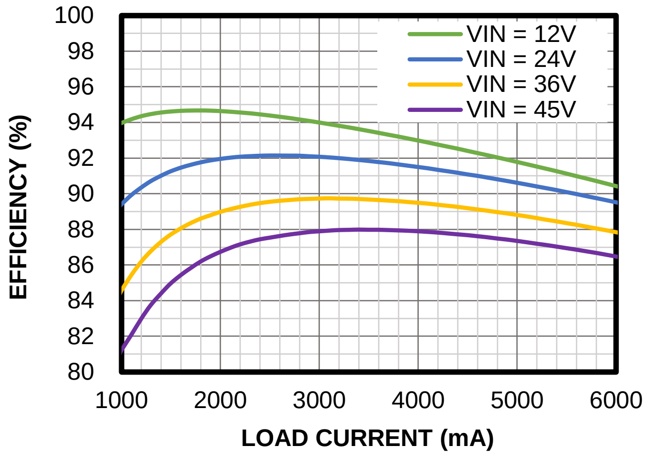
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



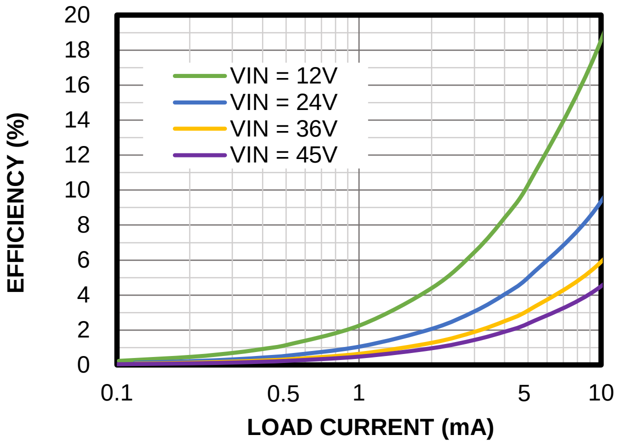
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V

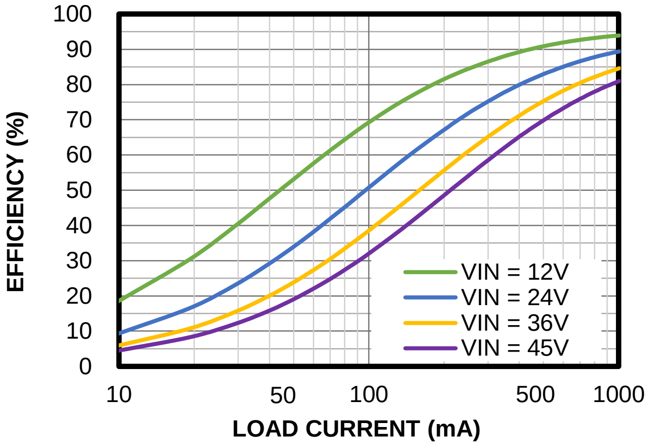


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (8), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

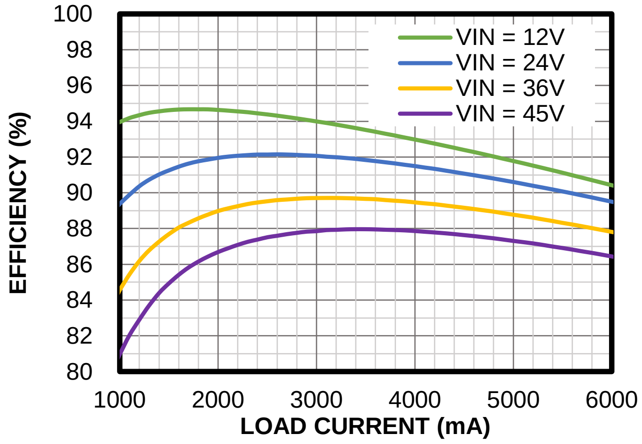
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V



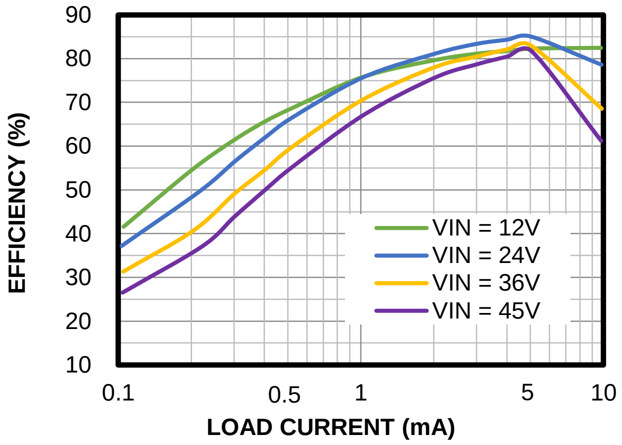
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V



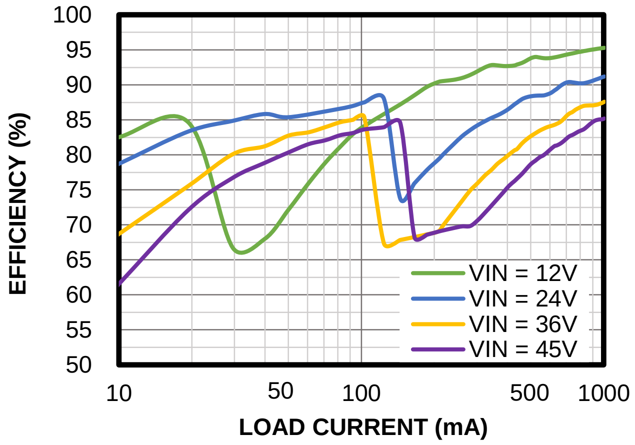
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V



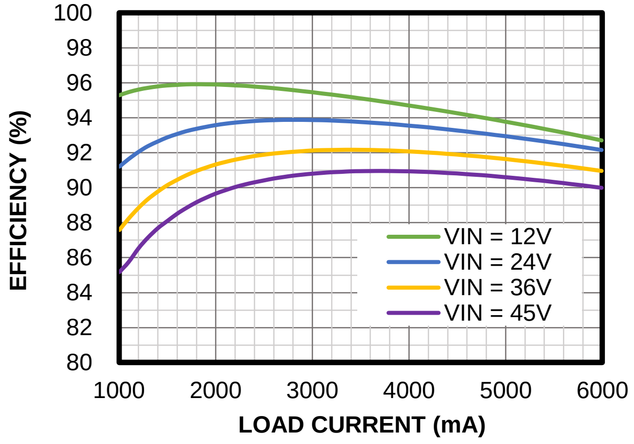
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V



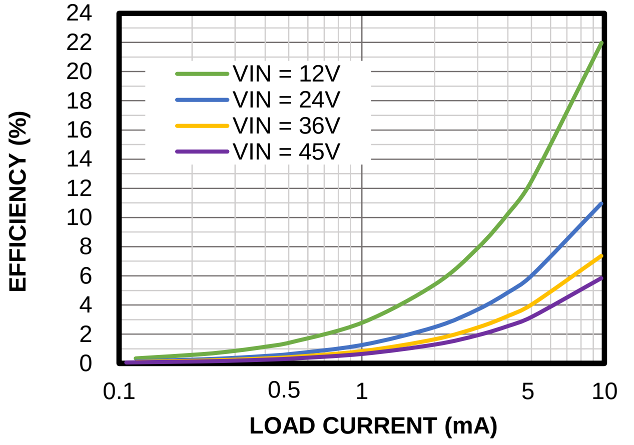
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V



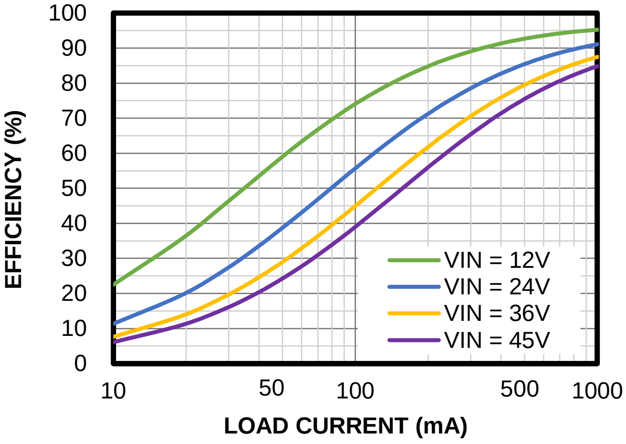
Efficiency vs. Load Current

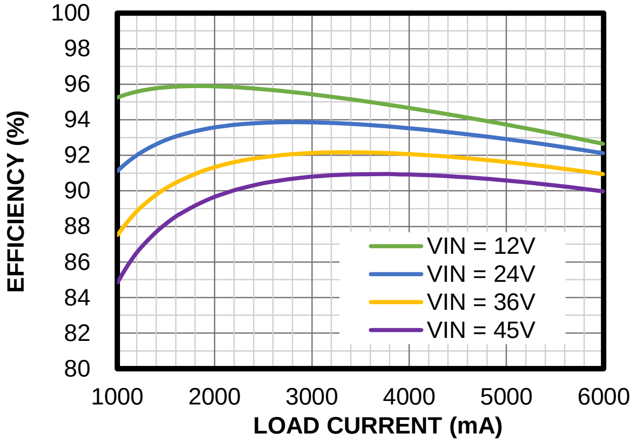
FCCM, V_{OUT} = 5V

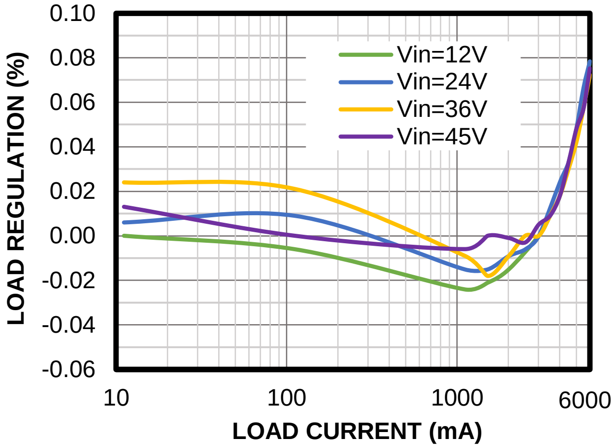


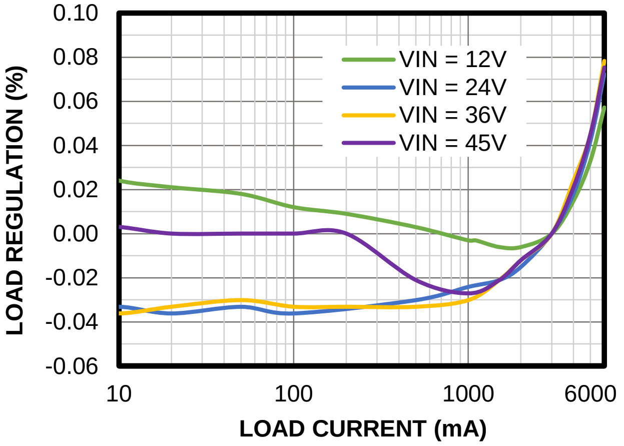
TYPICAL PERFORMANCE CHARACTERISTICS

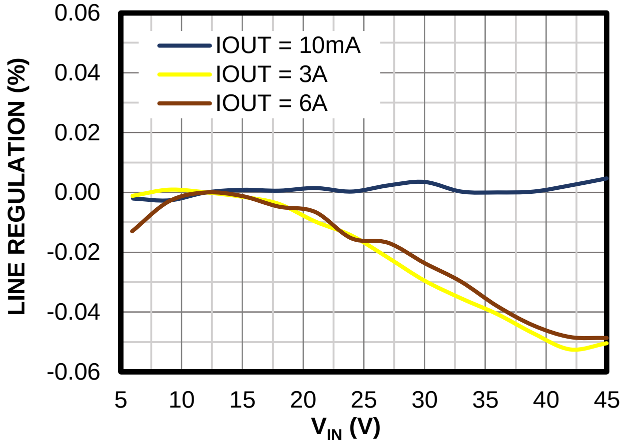
V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH [(8)], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

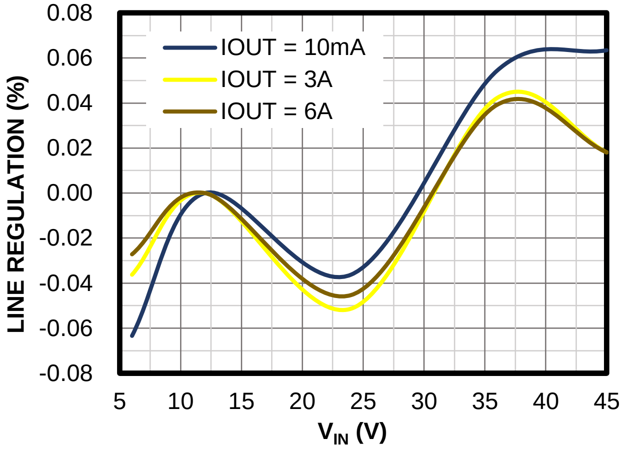

Efficiency vs. Load Current
FCCM, V_{OUT} = 5V


Efficiency vs. Load Current
FCCM, V_{OUT} = 5V


Load Regulation
AAM mode, V_{OUT} = 3.3V


Load Regulation
FCCM, V_{OUT} = 3.3V

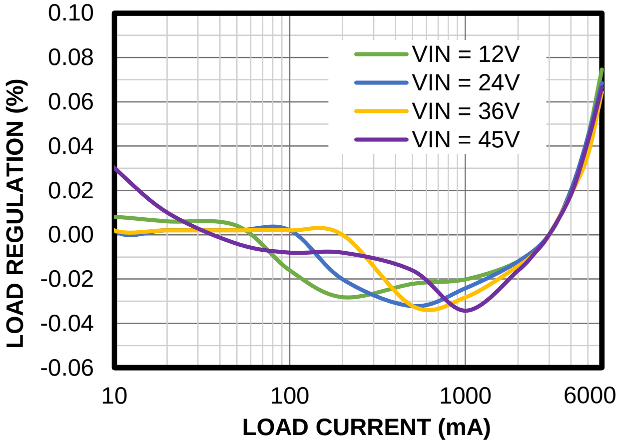

Line Regulation
AAM mode, V_{OUT} = 3.3V


Line Regulation
FCCM, V_{OUT} = 3.3V

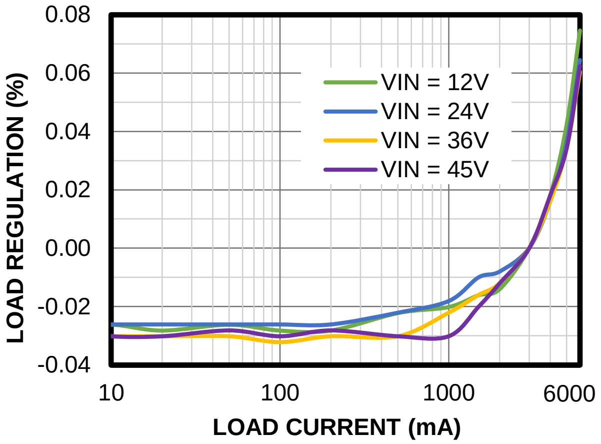
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH $^{(8)}$, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

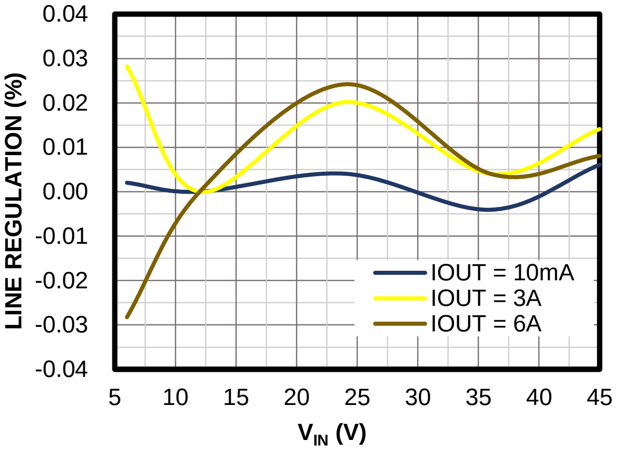
Load Regulation
AAM mode, V_{OUT} = 5V



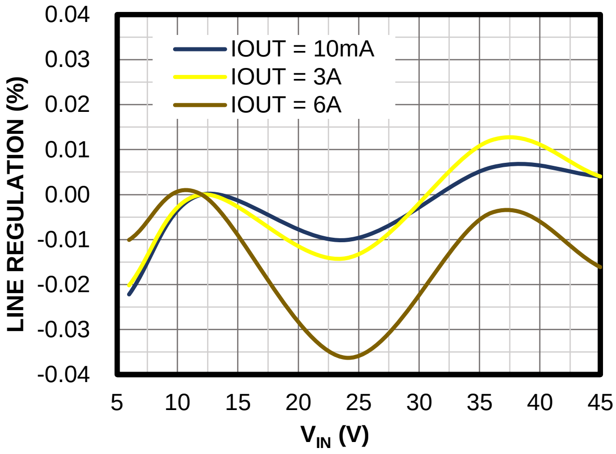
Load Regulation
FCCM, V_{OUT} = 5V



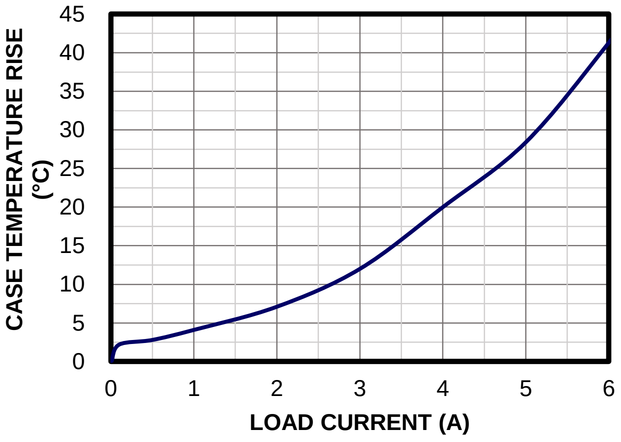
Line Regulation
AAM mode, V_{OUT} = 5V



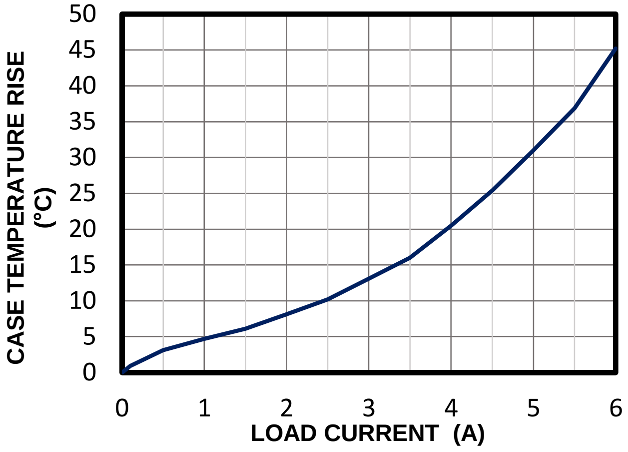
Line Regulation
FCCM, V_{OUT} = 5V



Case Temperature Rise
V_{OUT} = 3.3V



Case Temperature Rise
V_{OUT} = 5V

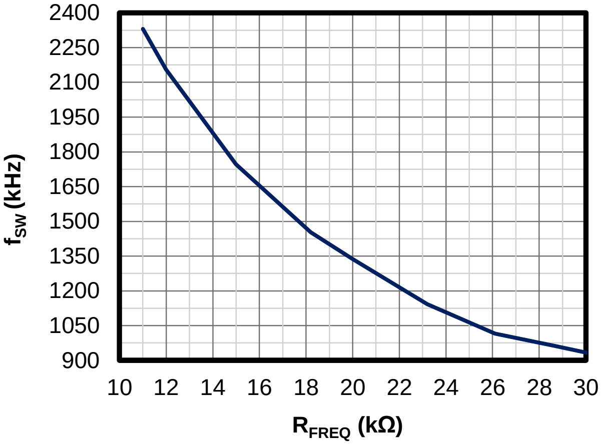


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [(8)], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

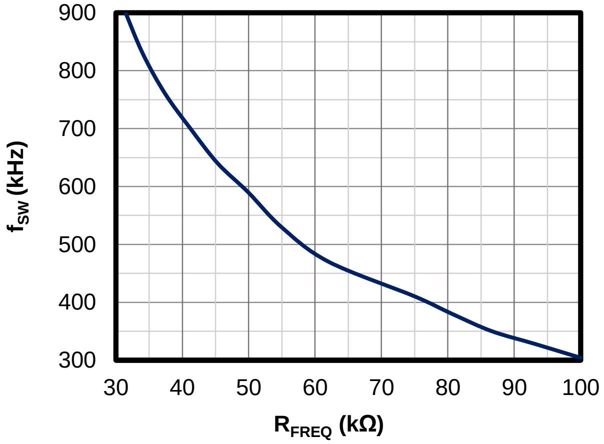
f_{SW} vs. R_{FREQ}

R_{FREQ} = 10kΩ to 30kΩ

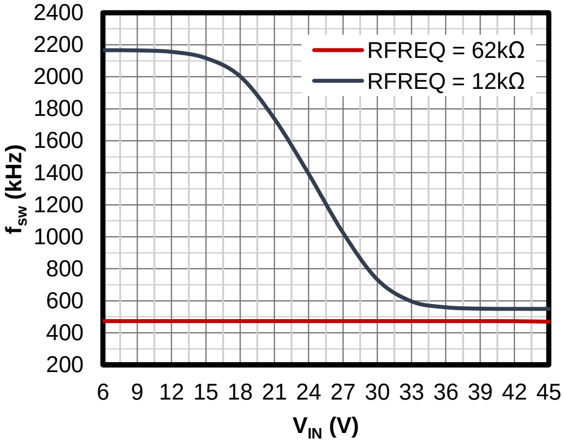


f_{SW} vs. R_{FREQ}

R_{FREQ} = 30kΩ to 100kΩ

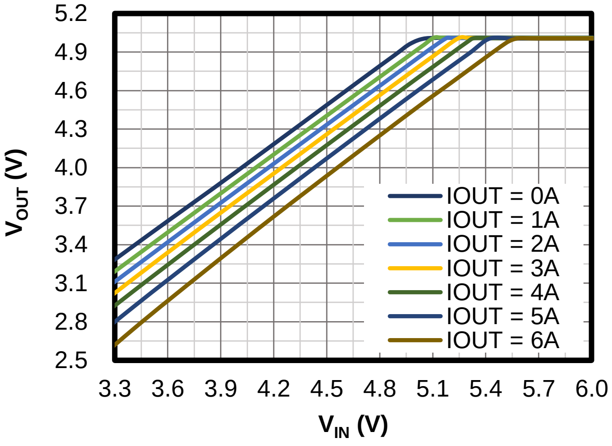


f_{SW} vs. V_{IN}



Low-Dropout Mode

V_{OUT} = 5V

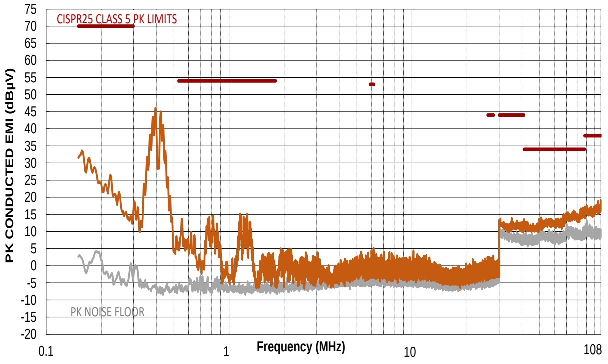


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (8), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (9)

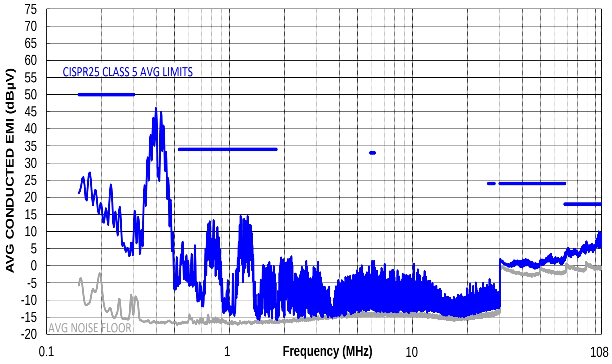
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



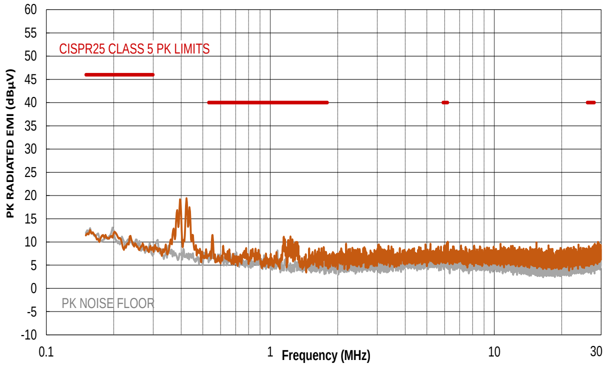
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



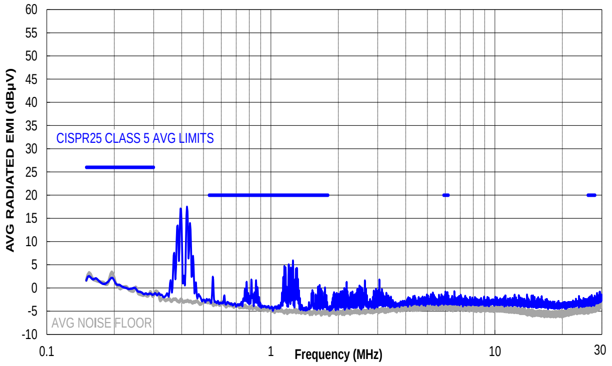
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



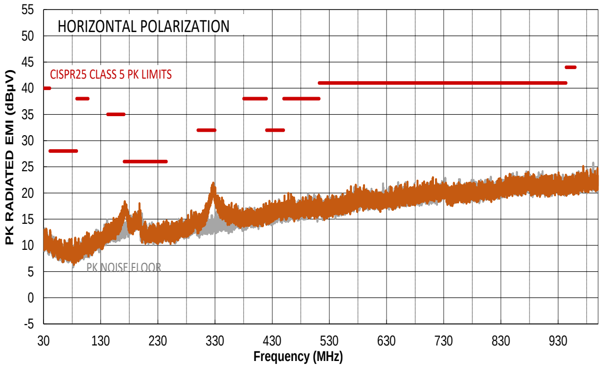
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



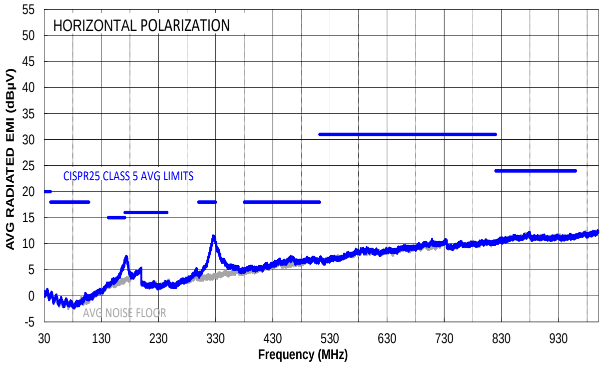
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

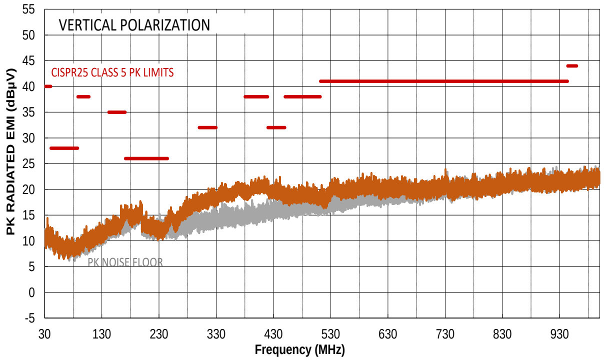


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (8), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (9)

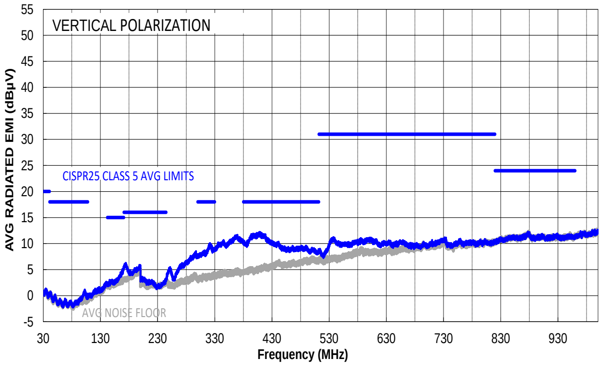
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

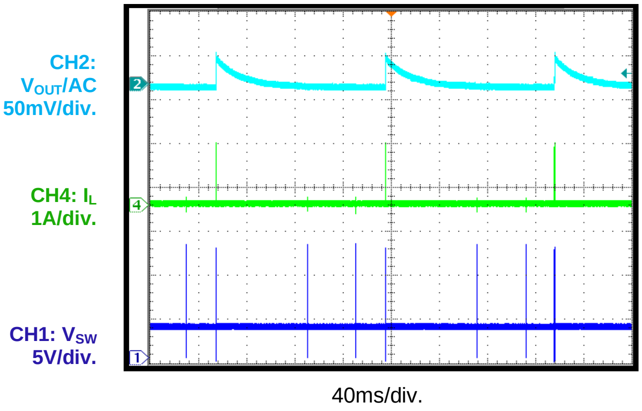
8) Inductor part number: XAL6060-472MEC (DCR = 15mΩ).
9) The EMC test results are based on Figure 11 on page 35.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

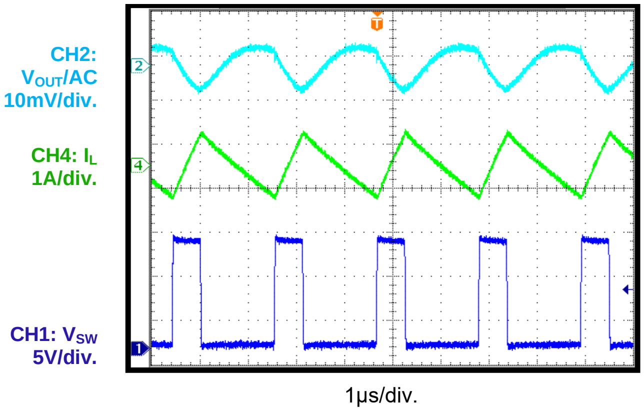
Steady State

I_{OUT} = 0A, AAM mode



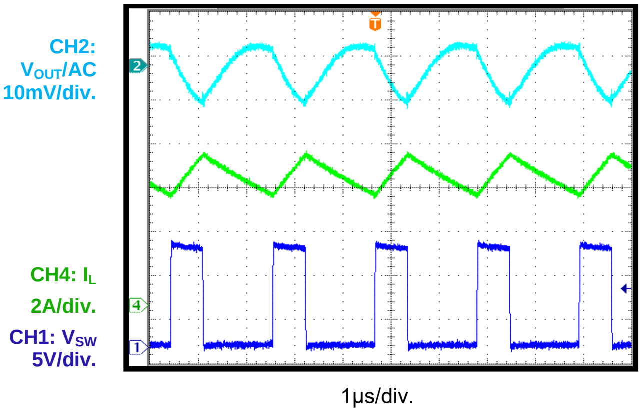
Steady State

I_{OUT} = 0A, FCCM



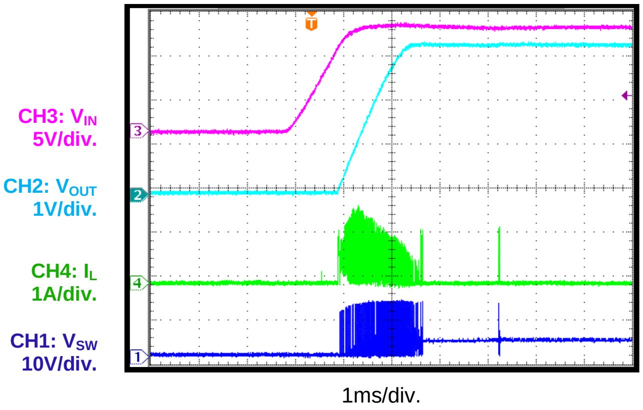
Steady State

I_{OUT} = 6A



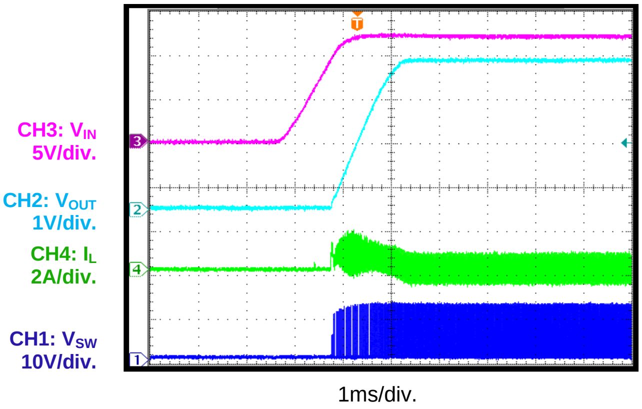
Start-Up through VIN

I_{OUT} = 0A, AAM mode



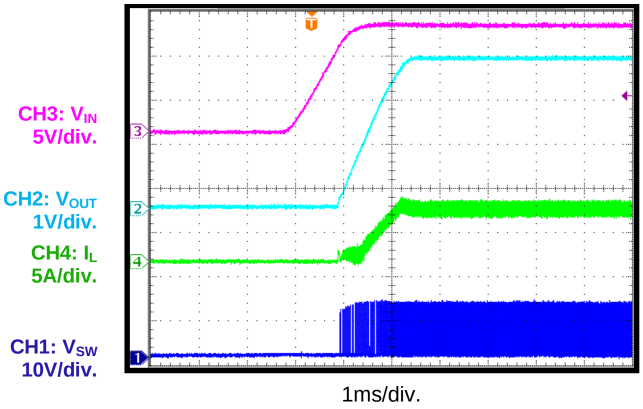
Start-Up through VIN

I_{OUT} = 0A, FCCM



Start-Up through VIN

I_{OUT} = 6A

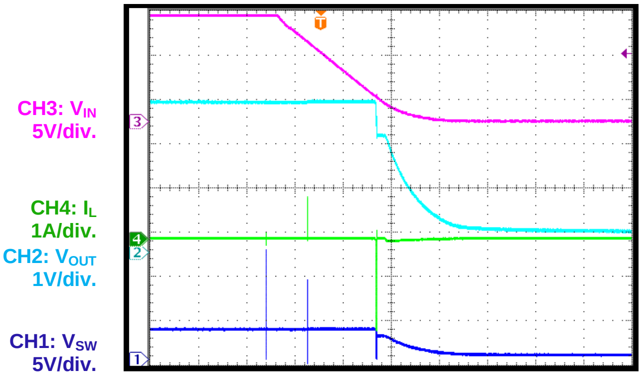


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

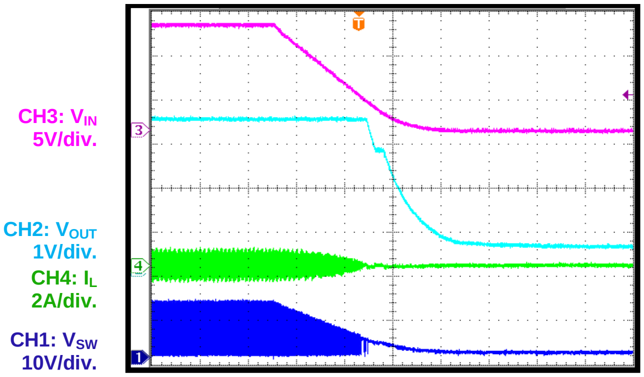
I_{OUT} = 0A, AAM mode



10ms/div.

Shutdown through VIN

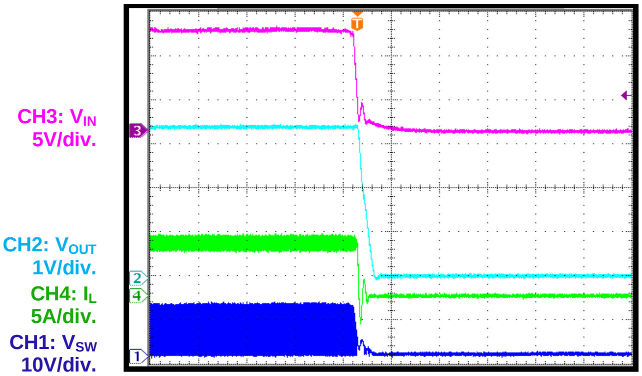
I_{OUT} = 0A, FCCM



10ms/div.

Shutdown through VIN

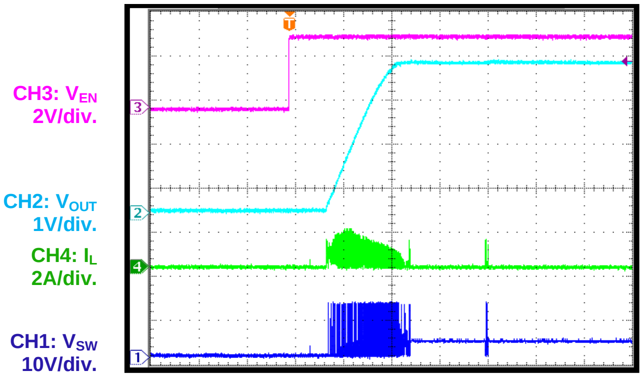
I_{OUT} = 6A



400µs/div.

Start-Up through EN

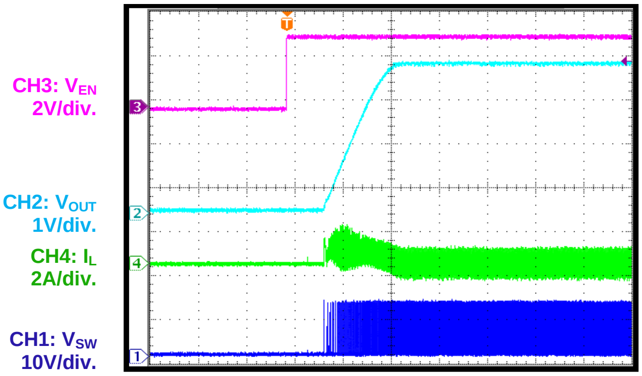
I_{OUT} = 0A, AAM mode



1ms/div.

Start-Up through EN

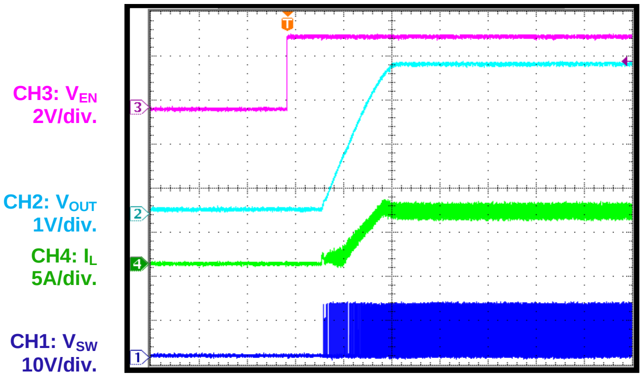
I_{OUT} = 0A, FCCM



1ms/div.

Start-Up through EN

I_{OUT} = 6A



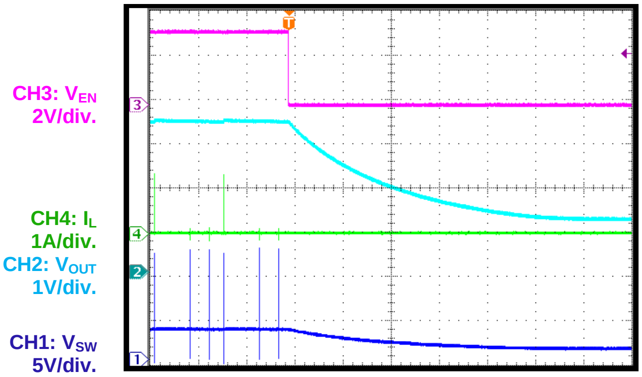
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

Shutdown through EN

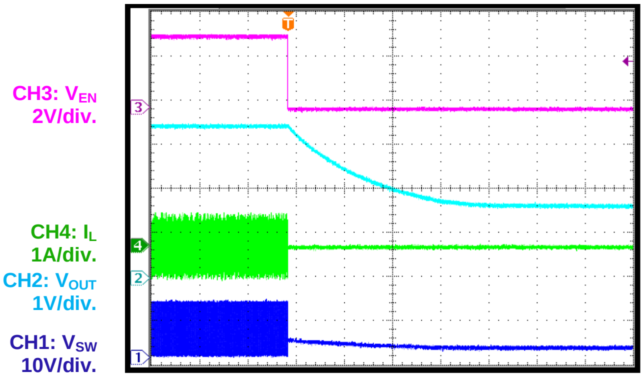
I_{OUT} = 0A, AAM mode



100ms/div.

Shutdown through EN

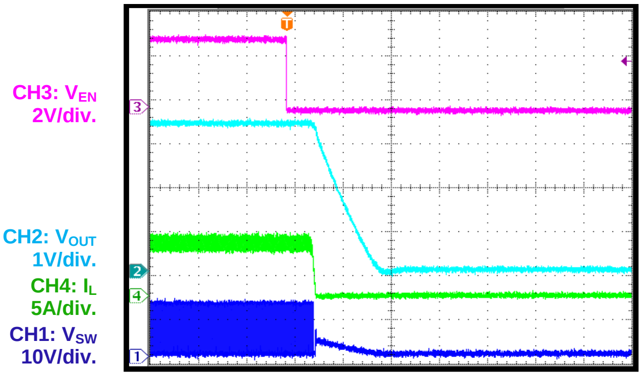
I_{OUT} = 0A, FCCM



100ms/div.

Shutdown through EN

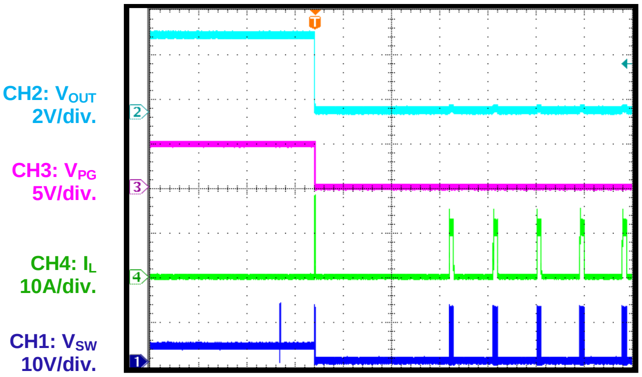
I_{OUT} = 6A



100µs/div.

SCP Entry

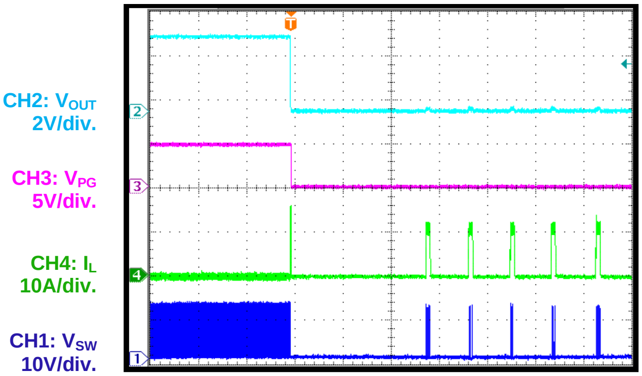
I_{OUT} = 0A, AAM mode



20ms/div.

SCP Entry

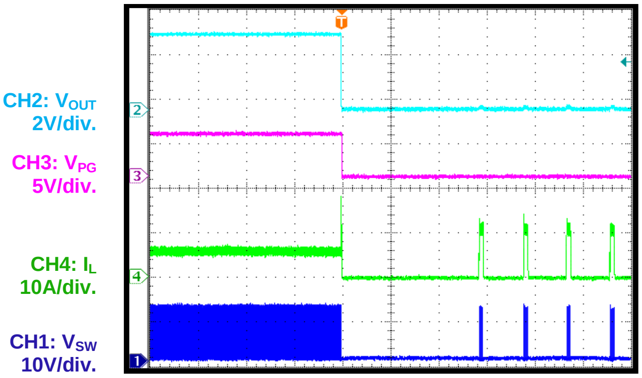
I_{OUT} = 0A, FCCM



20ms/div.

SCP Entry

I_{OUT} = 6A



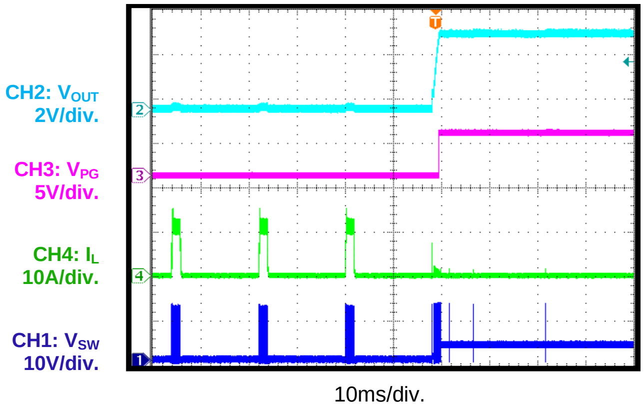
20ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

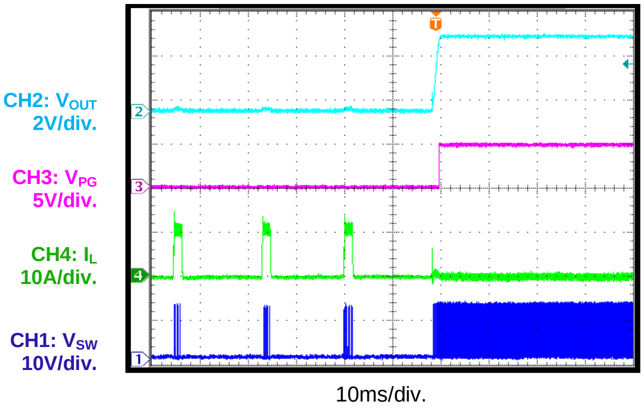
SCP Recovery

I_{OUT} = 0A, AAM mode



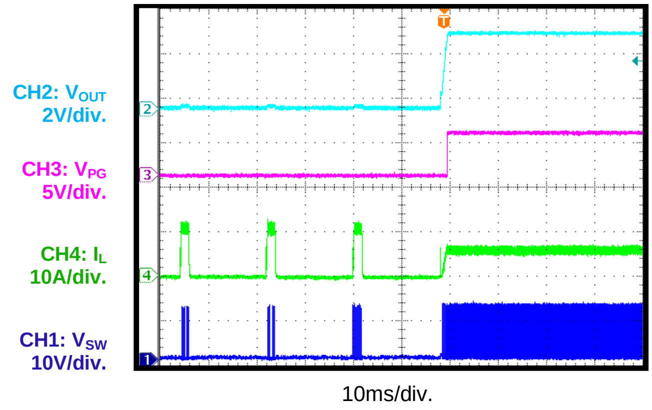
SCP Recovery

I_{OUT} = 0A, FCCM

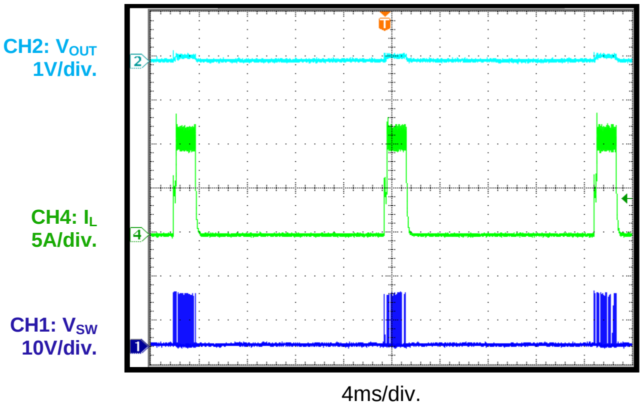


SCP Recovery

I_{OUT} = 6A

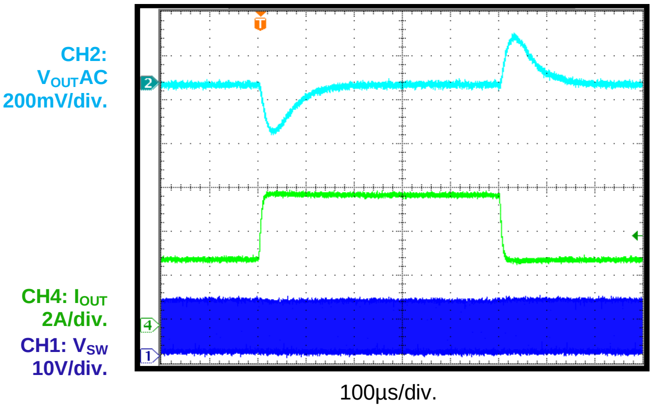


SCP Steady State



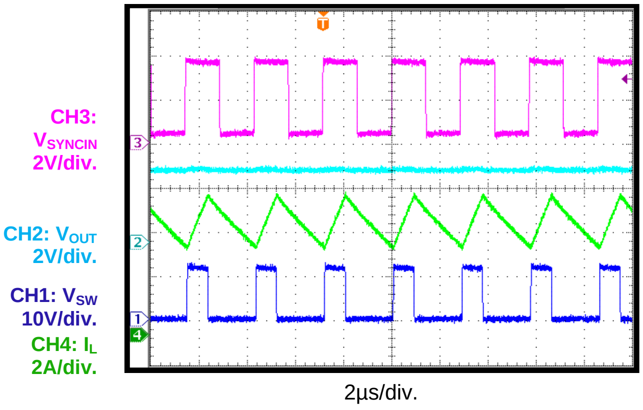
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



SYNCIN Operation

I_{OUT} = 6A, f_{SYNC} = 350kHz

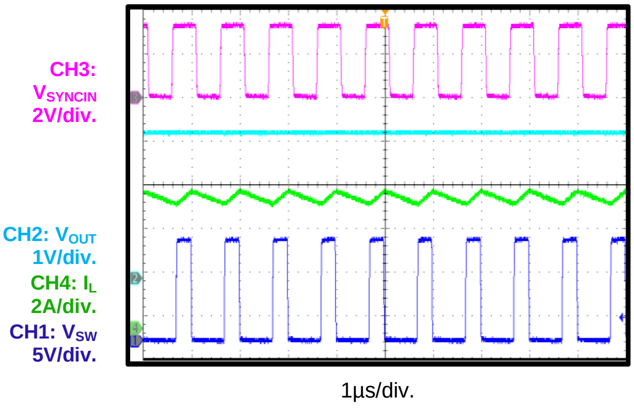


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

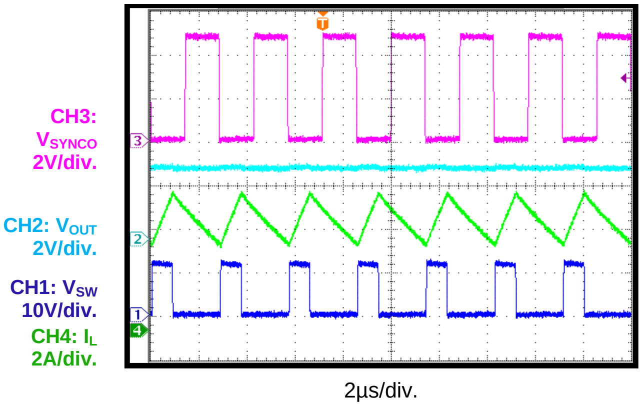
SYNCIN Operation

I_{OUT} = 6A, f_{SYNC} = 1000kHz



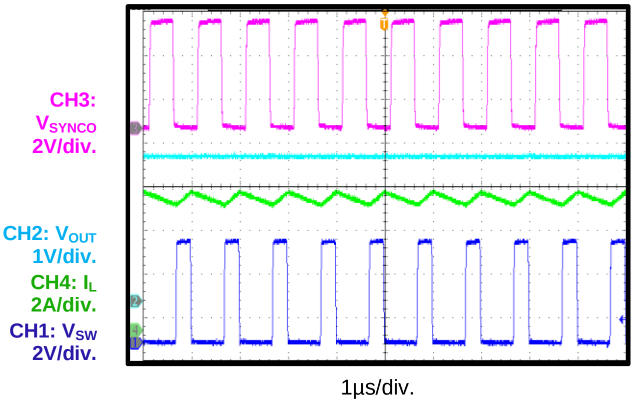
SYNCO Operation

I_{OUT} = 6A, f_{SYNC} = 350kHz



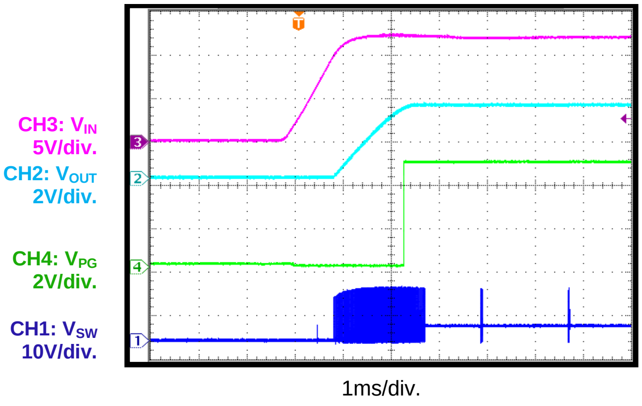
SYNCO Operation

I_{OUT} = 6A, f_{SYNC} = 1000kHz



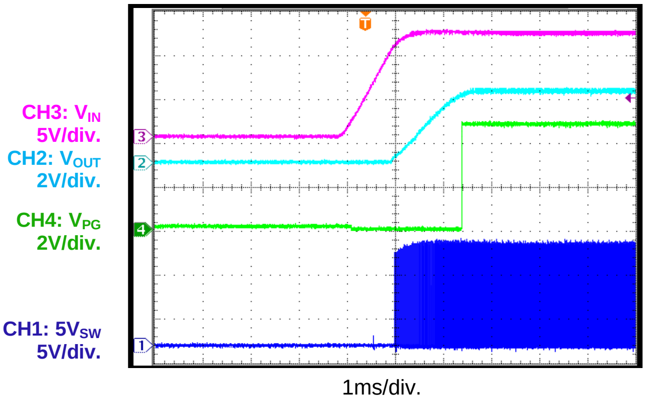
PG Start-Up through VIN

I_{OUT} = 0A



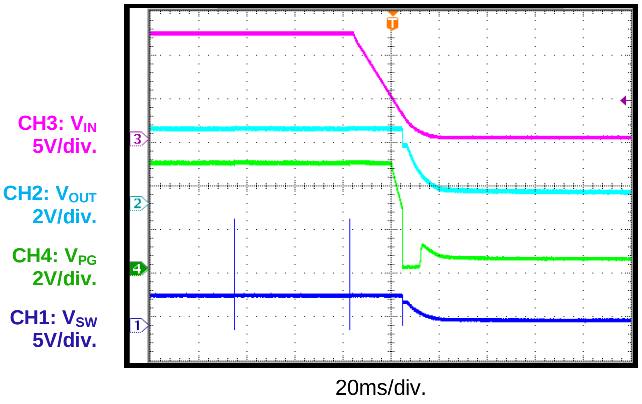
PG Start-Up through VIN

I_{OUT} = 6A



PG Shutdown through VIN

I_{OUT} = 0A

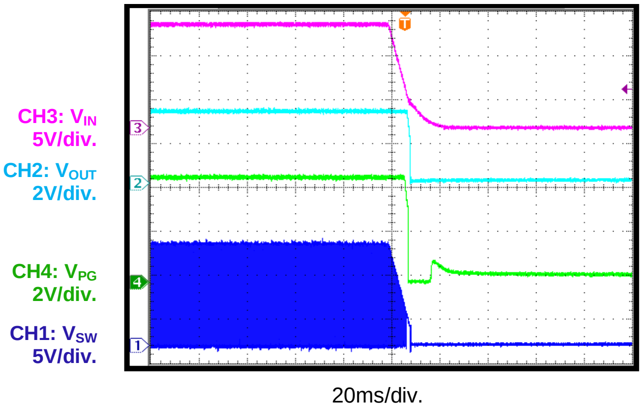


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

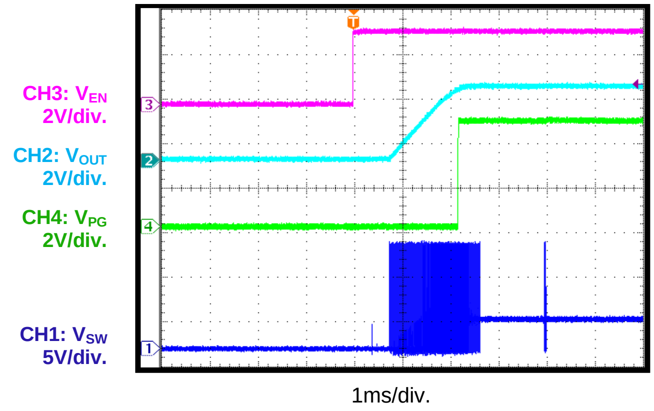
PG Shutdown through VIN

I_{OUT} = 6A



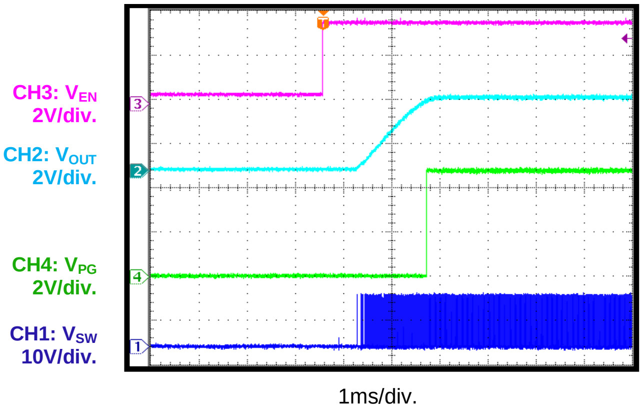
PG Start-Up through EN

I_{OUT} = 0A



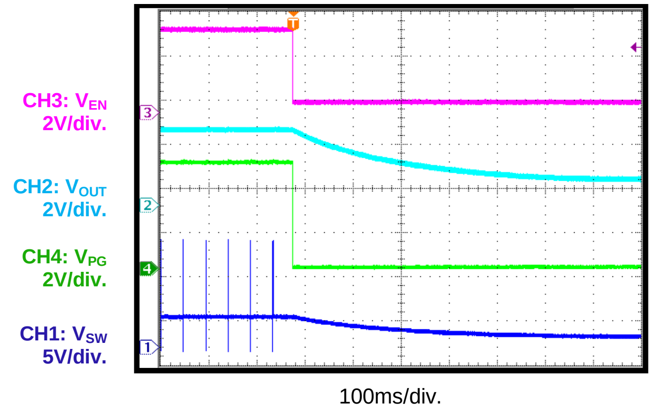
PG Start-Up through EN

I_{OUT} = 6A



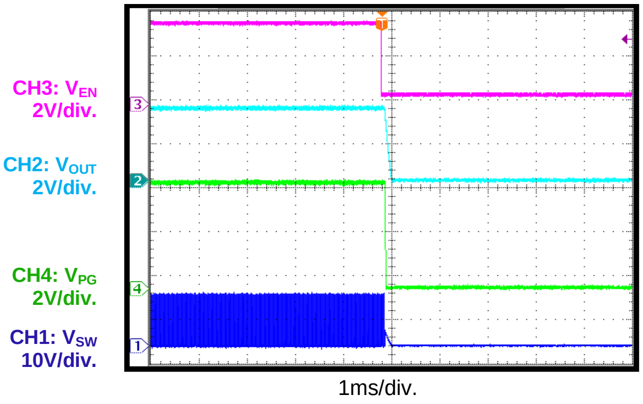
PG Shutdown through EN

I_{OUT} = 0A



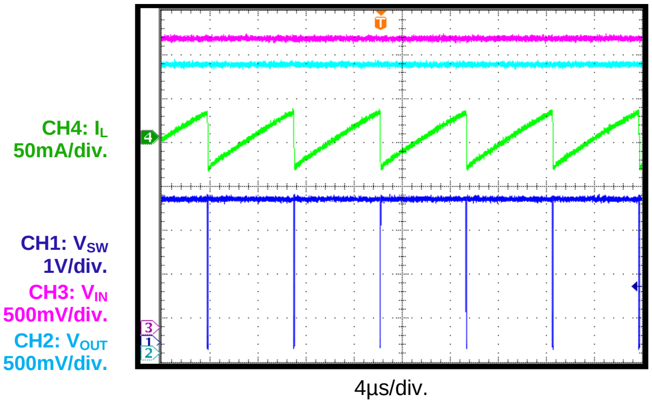
PG Shutdown through EN

I_{OUT} = 6A



LDO Operation

V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 0A

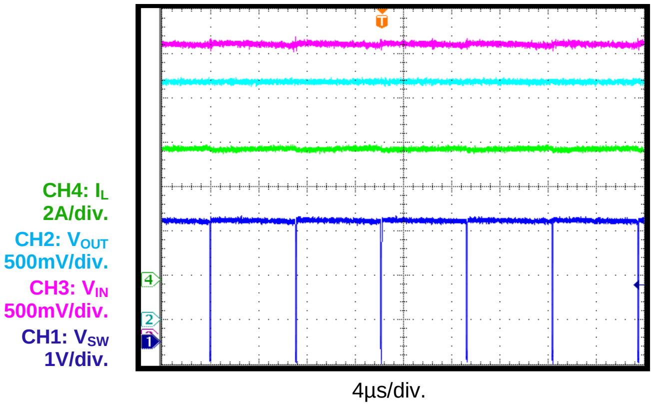


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

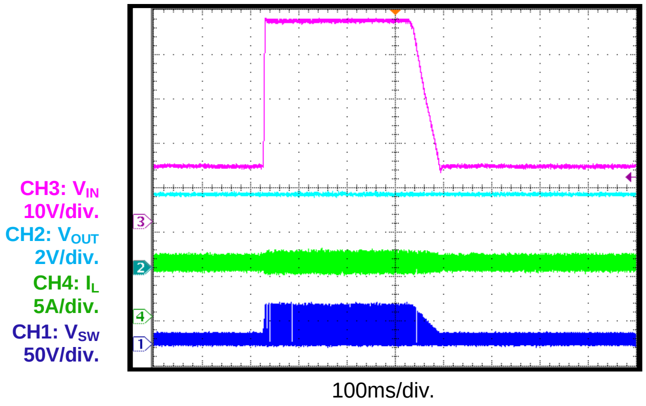
LDO Operation

V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 6A



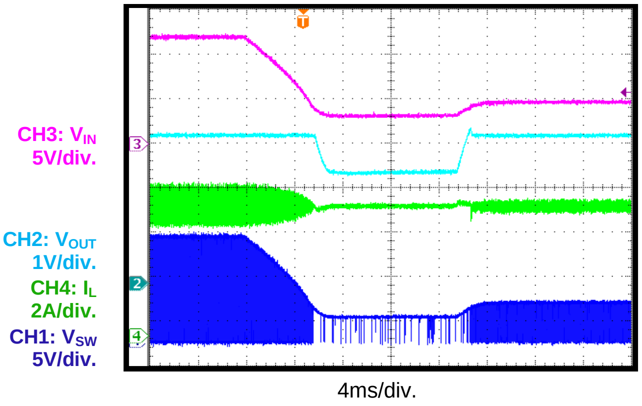
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A



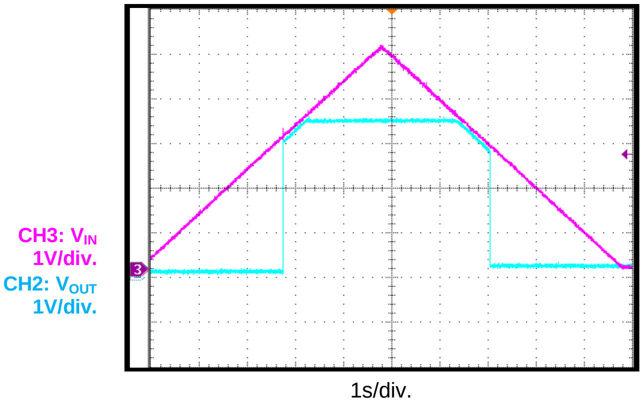
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



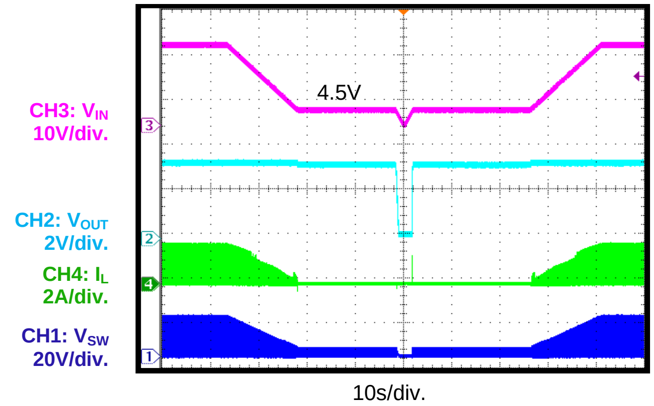
V_{IN} Ramps Up and Down

I_{OUT} = 0.1A



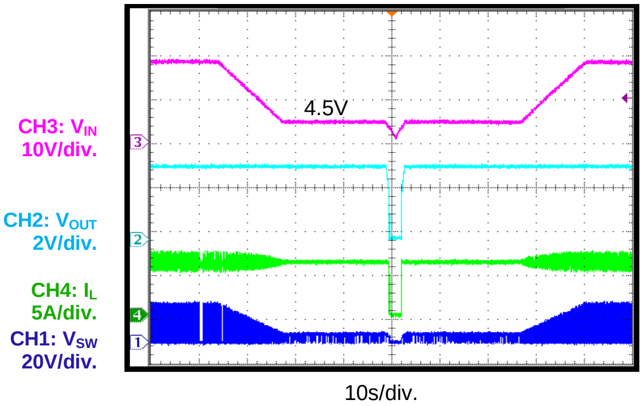
V_{IN} Ramps Down and Up

I_{OUT} = 1mA



V_{IN} Ramps Down and Up

I_{OUT} = 6A



FUNCTIONAL BLOCK DIAGRAM

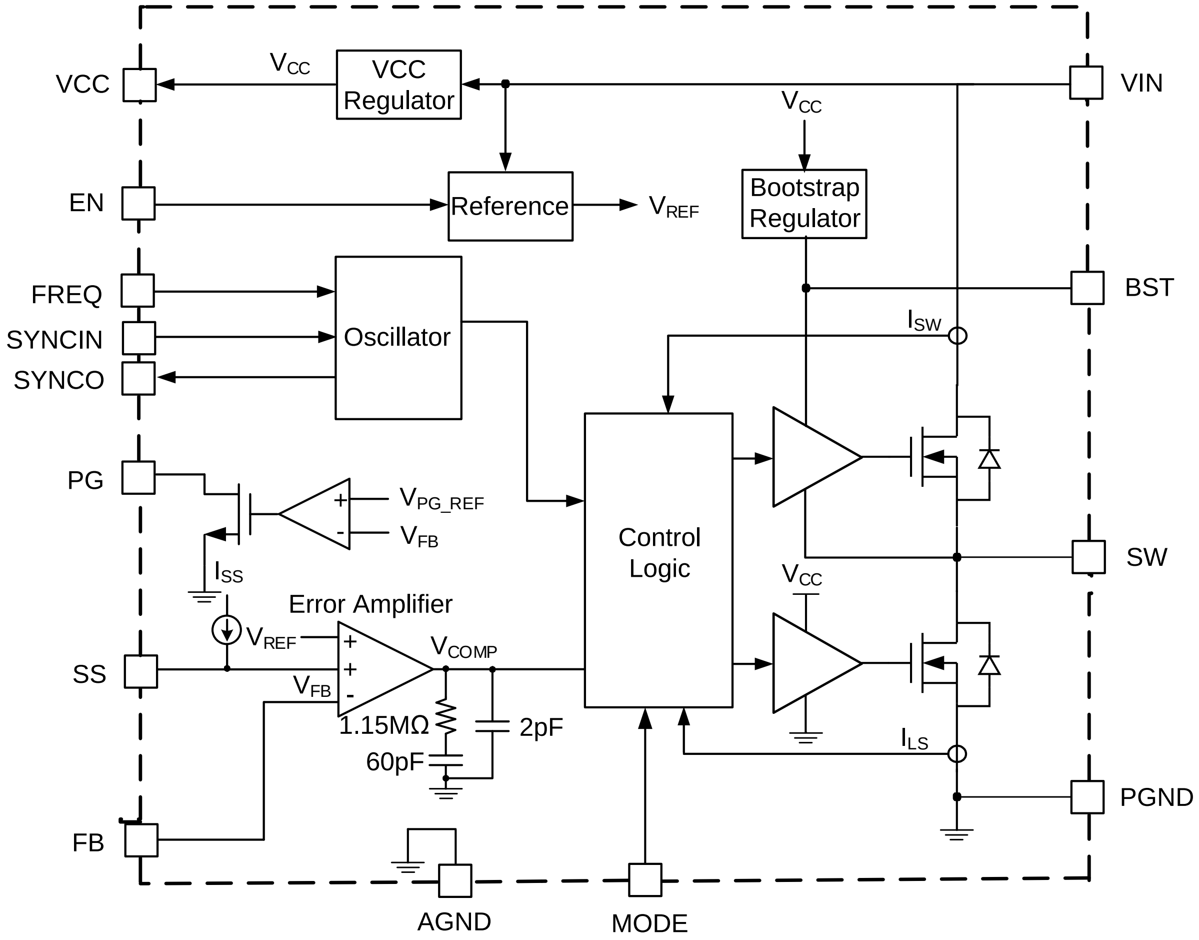


Figure 1: Functional Block Diagram

TIMING SEQUENCE

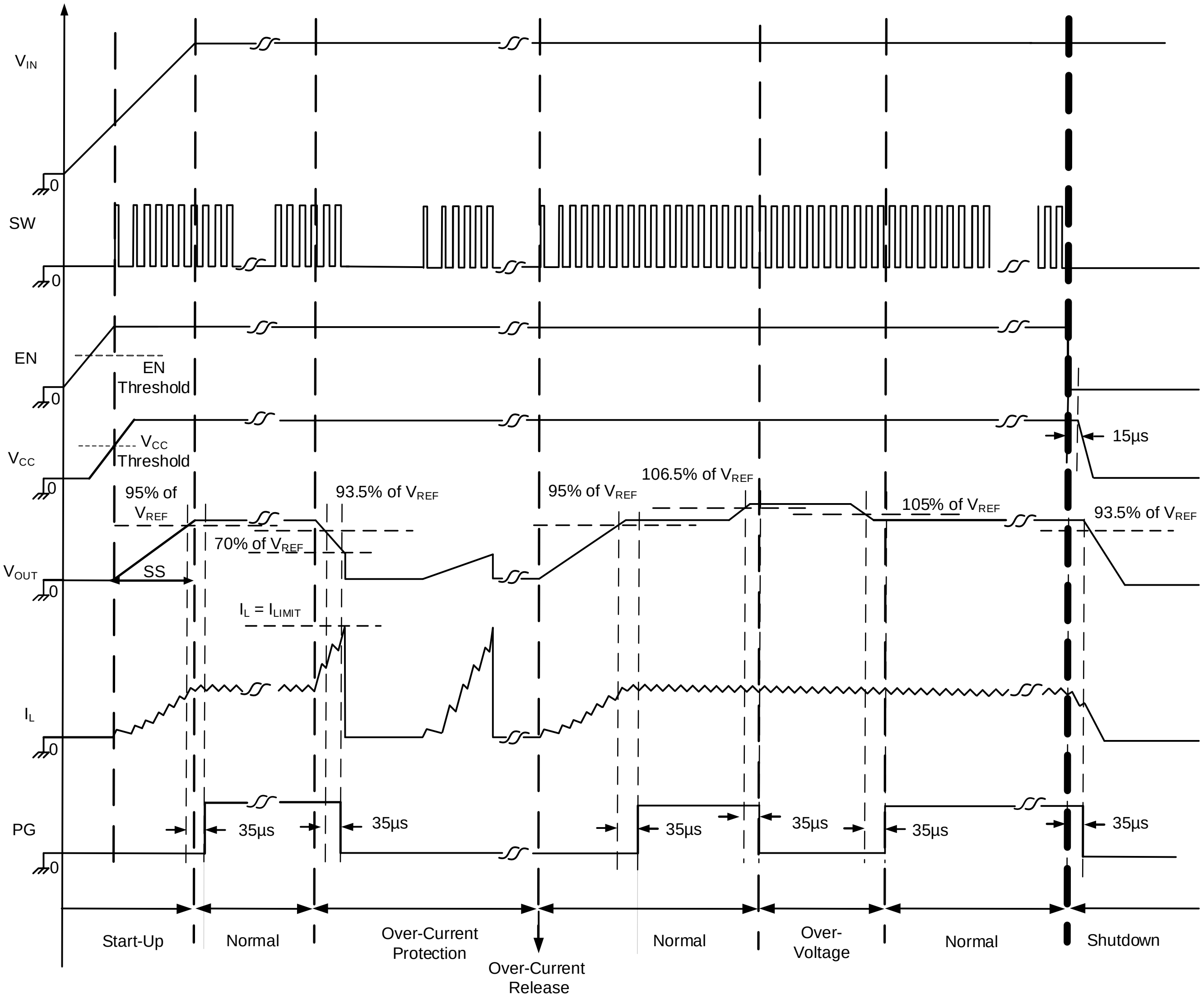


Figure 2: Timing Sequence

OPERATION

The MP4316 is a synchronous, step-down switching converter with integrated internal power MOSFETs. It can achieve up to 6A of highly efficient, continuous output current (I_{OUT}) with current control mode for fast loop response.

The device features a wide 3.3V to 45V input voltage (V_{IN}) range, configurable switching frequency (f_{SW}), external soft start (SS), and a precise current limit. Its low 1.7µA shutdown current (I_{SD}) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP4316 operates with a fixed frequency in peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the internal comparator voltage (V_{COMP}). The HS-FET remains on for a minimum of 100ns.

If the HS-FET is off, the low-side MOSFET (LS-FET) turns on and remains on until the next PWM cycle starts. The LS-FET remains on for a minimum of 80ns before the next cycle starts.

If the HS-FET current does not reach V_{COMP} within one PWM cycle, the HS-FET remains on to avoid shutting down the device. The HS-FET turns off after about 10µs, even if it has not reached V_{COMP}.

Light-Load Operation

The MP4316 has a mode selection pin (MODE) that selects the IC's operation mode at light loads. Under light-load conditions, the MP4316 can operate in either forced continuous conduction mode (FCCM) or advanced asynchronous modulation (AAM) mode.

If MODE is pulled above 1.8V, then the MP4316 operates in FCCM. In FCCM, the device operates with a fixed frequency from no load to full loads. Advantages of FCCM include the controllable fixed frequency and lower V_{OUT} ripple under light-load conditions.

If MODE is pulled below 0.4V, then the MP4316 operates in AAM mode. AAM mode optimizes efficiency under light-load and no-load conditions.

If AAM mode is enabled, then the MP4316 enters asynchronous operation as the inductor current (I_L) approaches 0A (see Figure 3). If the load decreases further or if there is no load, V_{COMP} drops to its set value, and the device enters AAM mode.

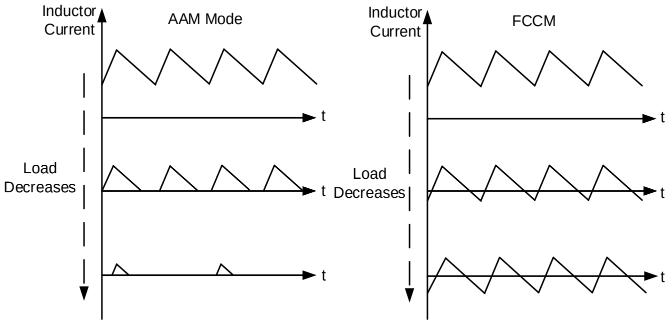


Figure 3: AAM and FCCM

In AAM mode, the internal clock resets once V_{COMP} reaches its set value. The crossover time is used as a benchmark for the next clock. If the load increases and V_{COMP} exceeds its set value, then the device operates in discontinuous conduction mode (DCM) or FCCM, which have a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage (V_{FB}) to the internal reference voltage (V_{REF}) (typically 0.815V), and outputs a current that is proportional to the difference between the voltages. This I_{OUT} charges the compensation network to set V_{COMP}, which controls the power MOSFET's current.

During normal operation, the minimum V_{COMP} is 0.9V, and the maximum is 2V. If the IC shuts down, V_{COMP} is pulled down to AGND internally.

Internal Regulator (VCC)

The 4.9V internal regulator (VCC) powers most of the internal circuitry. The regulator uses the VIN pin as its input and operates across the entire V_{IN} range. If V_{IN} exceeds 4.9V, then VCC is in full regulation. If V_{IN} drops below 4.9V, then VCC's output degrades.

Bootstrap (BST) Charging

The internal bootstrap (BST) regulator charges and regulates the BST capacitor (C_{BST}) to about 5V. If the difference between the BST and SW pin voltages (V_{BST} - V_{SW}) drops below 5V, then a P-channel MOSFET pass transistor connected between the VCC and BST pins turns on to charge C_{BST}. The external circuit should provide enough voltage headroom to facilitate the charging. If the HS-FET turns on, V_{BST} exceeds the VCC voltage (V_{CC}), and C_{BST} cannot be charged.

During high duty cycles, there is less time to charge C_{BST}. This means that C_{BST} may not be charged sufficiently. If the external circuit has an insufficient voltage or not enough time to charge C_{BST}, an additional external circuit is required to ensure that V_{BST} remains in its normal operation range.

Low-Dropout (LDO) Mode and Refreshing the Bootstrap Capacitor (C_{BST})

To improve dropout, the MP4316 is designed to operate at almost 100% duty cycle when V_{BST} - V_{SW} exceeds 2.5V. If V_{BST} - V_{SW} drops below 2.5V, then under-voltage lockout (UVLO) turns off the HS-FET. This allows the LS-FET to conduct and refresh the charge on C_{BST}. In DCM or pulse-skip mode (PSM), the LS-FET turns on to refresh V_{BST}.

Since the supply current sourced from C_{BST} is low, the HS-FET can remain on for more than the required switching cycles to refresh C_{BST}. As a result, the converter has a high effective duty cycle.

The converter's effective duty cycle during dropout is determined by the voltage drops across the HS-FET, the LS-FET, the inductor resistance, the low-side diode, and the PCB resistance.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the converter on and off.

Enabling the IC via an External High or Low Logic Signal

Pull EN below 0.85V to turn the converter off; pull EN above 1V to turn it on.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} exceeds the UVLO rising threshold, then the IC can be enabled and disabled via the EN pin. With an internal current source, a configurable V_{IN} UVLO threshold and hysteresis can be generated. The EN voltage (V_{EN}) can be set via resistor dividers (R_{EN1} + R_{EN2}) (see Figure 4).

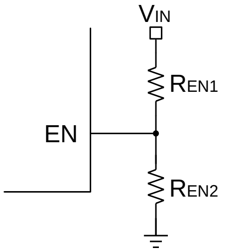


Figure 4: Enable Divider Circuit

Configurable Switching Frequency (f_{SW}) and Frequency Foldback

The MP4316's f_{SW} can be configured via an external resistor (R_{FREQ}) connected from the FREQ pin to AGND, or by a logic-level SYNC signal.

See the f_{SW} vs. R_{FREQ} curves on page 15 to select R_{FREQ} and set f_{SW}. If f_{SW} is set high, it may fold back at high input voltages to avoid triggering a minimum on time (t_{ON_MIN}) that would force the output out of regulation.

Set the f_{SW} between 350kHz and 1000kHz for car battery applications. Table 1 lists the recommended R_{FREQ} values for common switching frequencies. High frequencies can be used in applications that do not require a critical f_{SW} limit or that have a low, stable V_{IN}.

Table 1: R_{FREQ} vs. f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

Frequency Spread Spectrum (FSS)

The MP4316 employs a 12kHz modulation frequency and a fixed 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%) window (see Figure 5). The steps are fixed and independent of the set f_{SW}. This optimizes the frequency spread spectrum (FSS) performance.

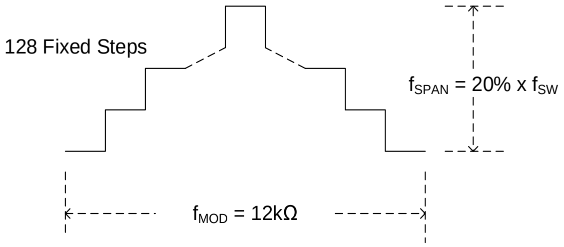


Figure 5: Frequency Spread Spectrum

Side bands are created by modulating f_{SW} via the triangle modulation waveform. This reduces the fundamental f_{SW} emission power and harmonics, which reduces noise caused by peak electromagnetic interference (EMI).

Soft Start (SS)

The MP4316 employs SS to prevent V_{OUT} from overshooting during start-up.

Once a SS is initiated, an internal current source charges the external soft-start capacitor (C_{SS}). If the soft-start voltage (V_{SS}) drops below V_{REF}, then V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

The soft-start capacitance (C_{SS}) can be calculated with Equation (1):

$$C_{SS}(nF)=\frac{t_{SS}(ms)\times I_{SS}(\mu A)}{V_{REF}(V)}=13.5\times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} - 150mV during start-up, then the output has a pre-biased voltage. With a pre-biased voltage, the HS-FET and LS-FET do not turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds the thermal shutdown threshold (about 170°C), then the device shuts down. Once the temperature drops below about 150°C, the device initiates a SS and resumes normal operation.

Current Comparator and Current Limit

The MOSFET currents are sensed via a current-sense MOSFET. This current is fed to the high-speed current comparator for current mode control. The current comparator uses this sensed current as one of its inputs.

If the HS-FET turns on, the comparator is blanked until the end of the turn-on period to mitigate noise. The comparator compares the MOSFET current to the set V_{COMP} value. If the sensed current exceeds V_{COMP}, the comparator outputs low to turn off the HS-FET. The internal MOSFET maximum current is limited internally cycle by cycle.

Output Over-Voltage Protection (OVP) with Hiccup Mode

If an output short to ground occurs, V_{OUT} may drop below 70% of its nominal output voltage. If this occurs, the MP4316 shuts down to discharge C_{SS}. Once C_{SS} is discharged, the device initiates a SS to resume normal operation. This process is repeated until the fault condition is removed.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the MP4316 starts up. The reference block starts up first to generate a stable V_{REF} and currents. Then the internal regulator starts up to provide a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer turns the HS-FET and LS-FET off for about 50µs to blank any start-up glitches. Once the soft-start block is enabled, the device outputs low to ensure that the remaining circuitry is ready before slowly ramping up.

Three events can shut down the IC: V_{EN} going low, V_{IN} going low, and thermal shutdown. Once shutdown is initiated, the signaling path is blocked to avoid triggering any faults. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The power good (PG) pin is an open-drain output. If using the PG pin, connect it to a power source via a pull-up resistor. If V_{OUT} is between 95% and 105% of the nominal voltage, PG is pulled high. If V_{OUT} exceeds 106.5% or drops below 93.5% of the nominal voltage, PG is pulled low.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of the SYNCIN clock. It is recommended that the SYNCIN frequency (f_{SYNCIN}) be between 350kHz and 1000kHz. SYNCIN's off time (t_{OFF}) should be shorter than the internal oscillator period; otherwise, the internal clock may turn on the HS-FET before the rising edge of SYNCIN.

There is no SYNCIN pulse width limit; however, there is always parasitic capacitance on the pad. If the pulse width is too short, then a clear rising and falling edge may not be achieved due to the parasitic capacitance. It is recommended to set the pulse width above 100ns.

If using SYNCIN in AAM mode, pull SYNCIN below 0.4V or float SYNCIN before start-up. Then add the external SYNCIN clock. Connect a 10kΩ to 51kΩ resistor between SYNCIN and AGND to avoid floating SYNCIN.

The SYNCO pin provides a default 180° phase-shifted clock for the internal oscillator. If there is no external SYNCIN clock, SYNCO can provide a 180° phase-shifted clock that is compared to the internal clock.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to the FB pin sets V_{OUT} (see Figure 6).

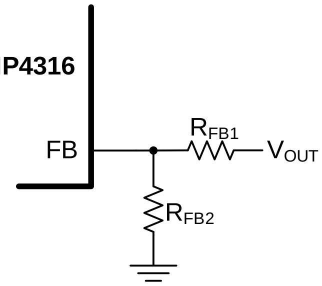


Figure 6: Feedback Network

The feedback resistor (R_{FB2}) can be calculated with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \tag{2}$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Recommended Resistor Values for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7µF to 10µF capacitor is sufficient. It is strongly recommended to use another low-value capacitor (0.1µF) with a small package size (0603) to absorb high-frequency noise. Place the smaller capacitor as close to the VIN pin and PGND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \tag{3}$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \tag{4}$$

For simplification, choose a C_{IN} with an RMS current rating greater than half of the maximum load current (I_{LOAD_MAX}).

C_{IN} can be electrolytic, tantalum, or ceramic. If using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (0.1µF) as close to the device as possible.

The input capacitance determines the input voltage ripple of the converter. If using ceramic capacitors, ensure that C_{IN} meets the system design's input voltage ripple (ΔV_{IN}) requirement. C_{IN} should have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \tag{5}$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Ceramic capacitors with low ESR are recommended for their small size and low output voltage ripple. The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \tag{6}$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \tag{7}$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}.

For simplification, ΔV_{OUT} can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of C_{OUT} also affect the stability of the regulation system. The MP4316 can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

For most applications, a 1µH to 10µH inductor with a DC current rating of at least 25% greater than I_{LOAD_MAX} is recommended. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor offers less ripple current and a lower ΔV_{OUT}; however, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the inductor ripple current (ΔI_L) to be approximately 30% of I_{LOAD_MAX}. The inductance can be estimated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Choose ΔI_L to be about 30% of I_{LOAD_MAX}. The maximum inductor peak current (I_{LP}) can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

Setting V_{IN} Under-Voltage Lockout (UVLO)

The MP4316 has an internal, fixed UVLO threshold. The rising threshold is 3V, and the falling threshold is about 2.7V. For applications that require a higher UVLO, place an external resistor divider between the VIN and EN pins to raise the UVLO threshold (see Figure 7).

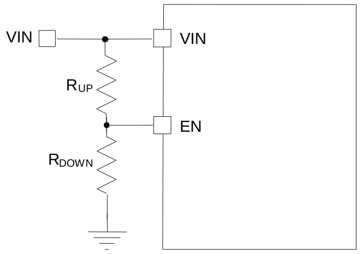


Figure 7: Setting the UVLO Threshold via the EN Resistor Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated with Equation (11):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (11)$$

Where V_{EN_RISING} is 1V.

The UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$) can be calculated with Equation (12):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (12)$$

Where $V_{EN\_FALLING}$ is 0.85V.

Selecting the External Bootstrap (BST) Diode and Resistor

An external BST diode can enhance the BST regulator's efficiency during high duty cycles. A 2.5V to 5V power supply can be used to power the external BST diode. It is recommended to use V_{CC} or V_{OUT} as the power supply (see Figure 8).

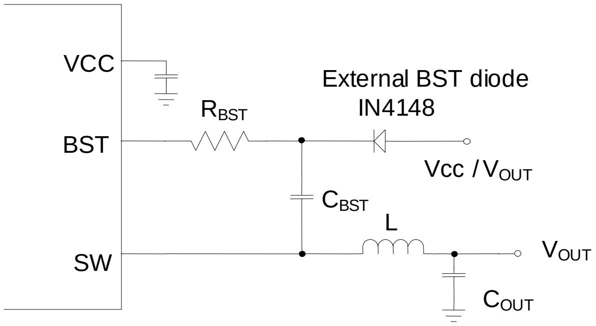


Figure 8: Optional External BST Diode for Enhanced Efficiency

It is recommended to use an IN4148 external BST diode. 1µF. A resistor (R_{BST}) in series with C_{BST} can reduce V_{SW} rising slew rate and voltage spikes. This improves EMI performance and reduces voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction, but can compromise efficiency. To make a tradeoff between EMI and efficiency, it is recommended to keep R_{BST} below 20Ω. The recommended C_{BST} value is 0.1µF to 1µF.

Selecting the VCC Capacitor (C_{VCC})

The VCC capacitor (C_{VCC}) should have a capacitance of 10 times the boost capacitor's capacitance. C_{VCC} should not exceed 68µF.

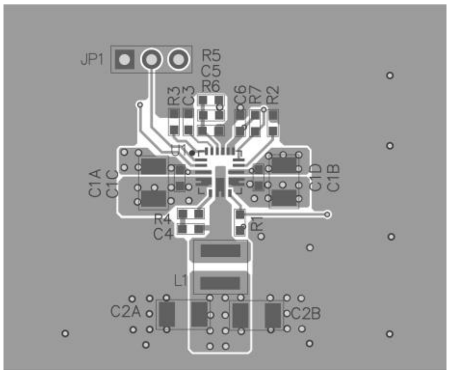
PCB Layout Guidelines [10]

Efficient PCB layout is critical for stable operation. It is recommended to use a 4-layer layout to improve thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

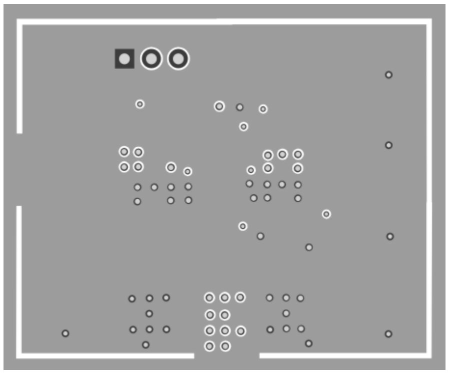
1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large copper plane directly to PGND.
3. If the bottom PCB layer is the ground plane, place multiple vias near PGND.
4. Use short, direct, and wide traces for the high-current paths connected to VIN and PGND.
5. Place C_{IN} as close to the VIN and PGND pins as possible to minimize high-frequency noise. It is recommended that C_{IN} be a ceramic bypass capacitor in a small 0603 package.
6. Keep the connection between C_{IN} and VIN as short and wide as possible.
7. Place C_{VCC} as close to VCC and AGND as possible.
8. Route the SW and BST traces away from sensitive analog areas, such as FB.
9. Keep the FB trace as short as wide as possible by placing the FB resistors close to the IC.
10. Use multiple vias to connect the power planes and the internal layers.

Note:

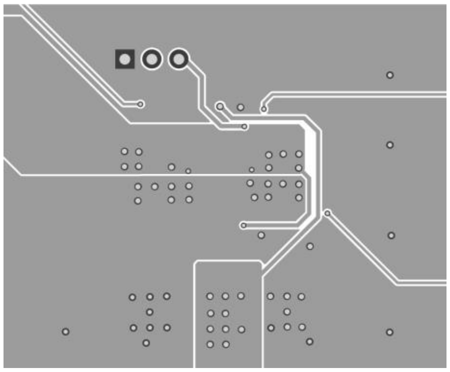
[10] The recommended PCB layout is based on Figure 10 on page 34.



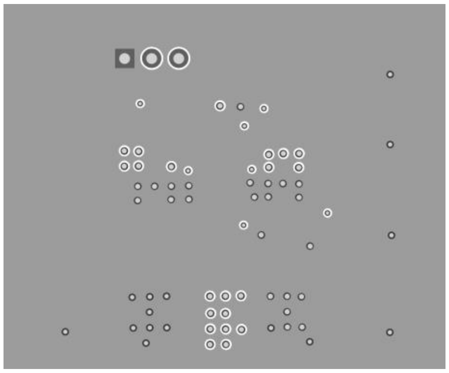
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

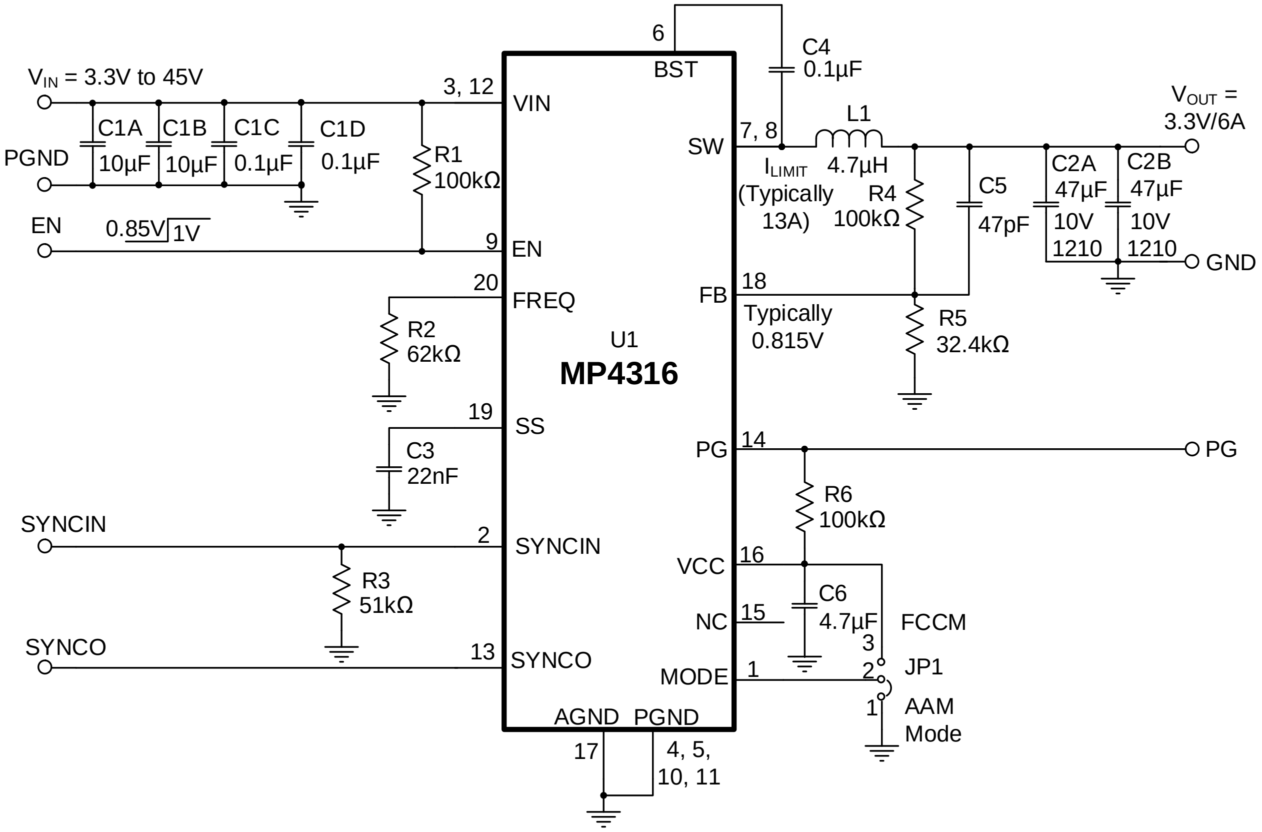


Figure 10: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 470kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

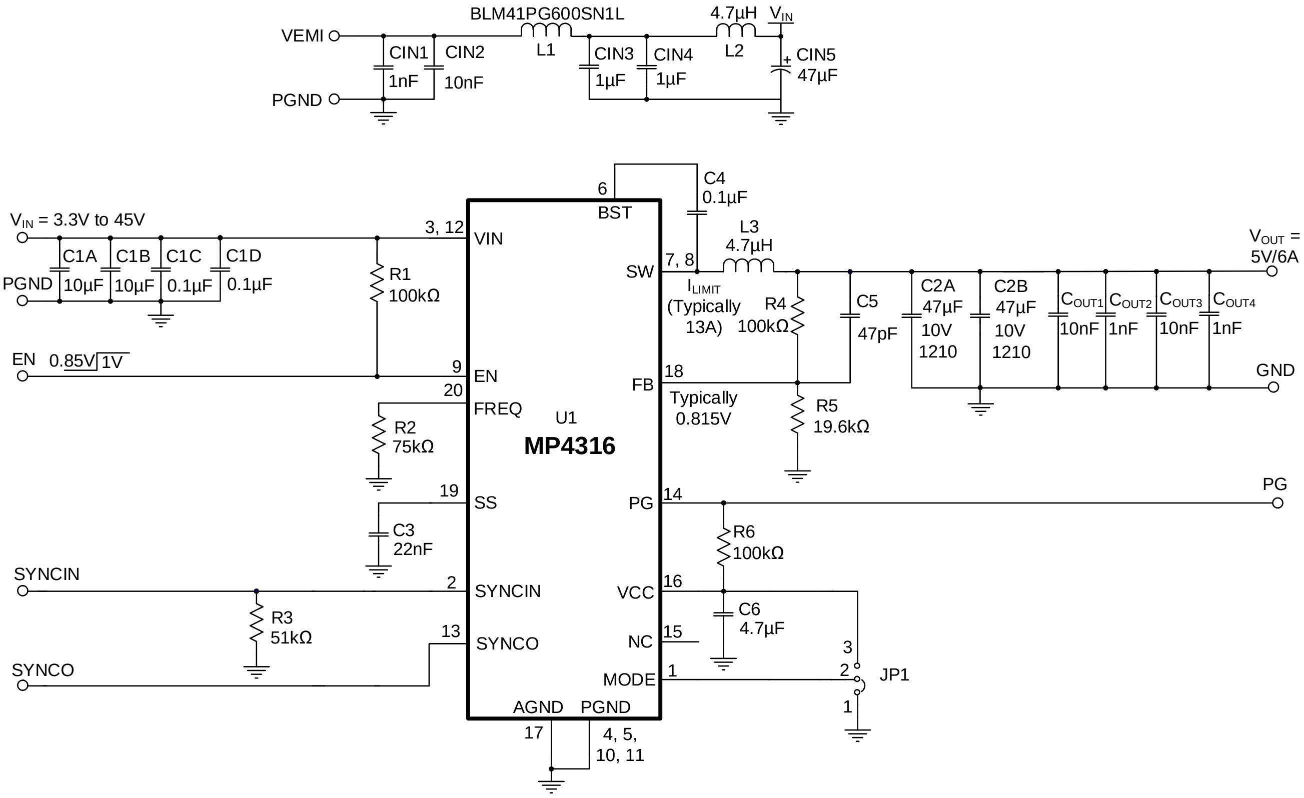
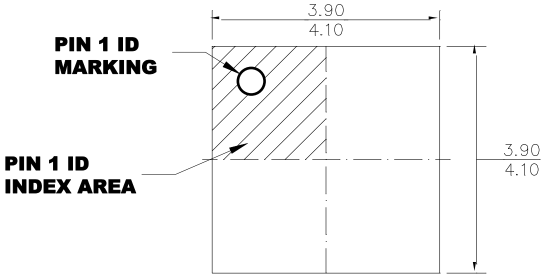


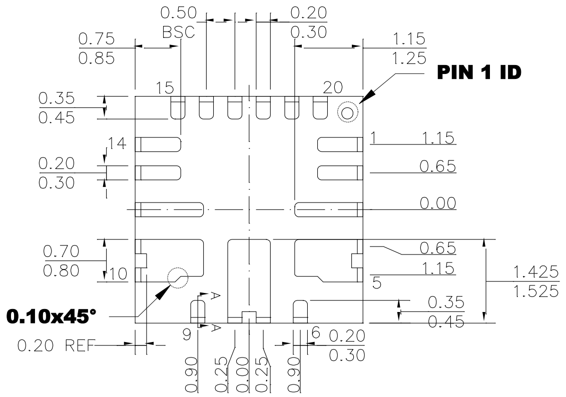
Figure 11: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz, with EMI Filters)

PACKAGE INFORMATION

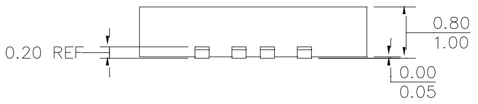
QFN-20 (4mmx4mm)
Wettable Flank



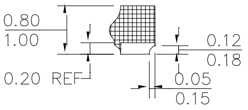
TOP VIEW



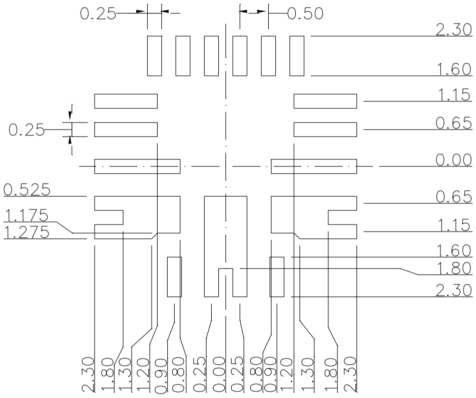
BOTTOM VIEW



SIDE VIEW



SECTION A-A

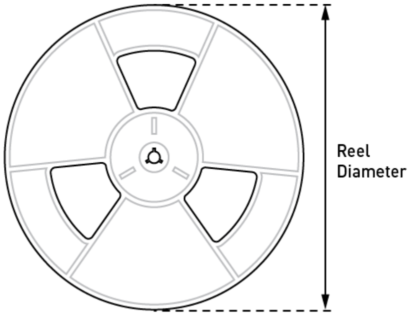


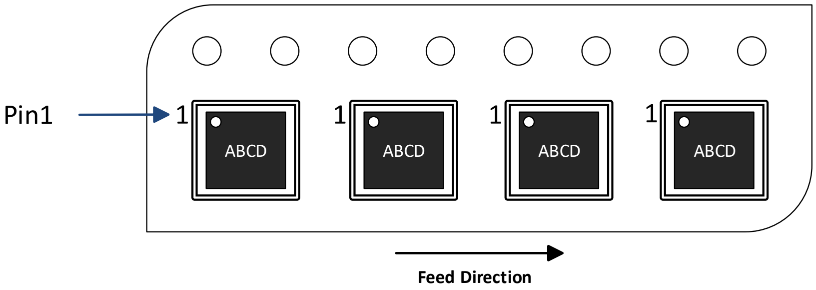
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (13)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4316GRE-Z	QFN-20 (4mmx4mm)	5000	N/A	13in	12mm	8mm

Note:

11) N/A means “not applicable.” Contact MPS for 500 pieces of tape and reel prototype quantities. The order code for a 500-piece partial reel is “-P”. The tape and reel dimensions are the same as the full reel.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/22/2021	Initial Release	-