MCP16701 (EV23P28A) Evaluation Board User's Guide

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MCP16701 (EV23P28A) EVALUATION BOARD USER'S GUIDE

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXXXXA", where "XXXXXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the MCP16701 (EV23P28A) Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- The Microchip Website
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the MCP16701 (EV23P28A) Evaluation Board as a development tool. The manual layout is as follows:

- **Chapter 1. "Product Overview"** – Important information about the MCP16701 (EV23P28A) Evaluation Board.
- **Chapter 2. "Installation and Operation"** – Includes instructions on how to get started with the MCP16701 (EV23P28A) Evaluation Board and a description of each function.
- **Chapter 3. "GUI Installation and Operation"** – Includes instructions on how to install the Graphical User Interface.
- **Chapter 4. "GUI Description"** – Describes the items in the Graphical User Interface.
- **Appendix A. "Schematic and Layouts"** – Shows the schematic and layout diagrams for the MCP16701 (EV23P28A) Evaluation Board.
- **Appendix B. "Bill of Materials (BOM)"** – Lists the parts used to build the MCP16701 (EV23P28A) Evaluation Board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

RECOMMENDED READING

This user's guide describes how to use the MCP16701 (EV23P28A) Evaluation Board. Another useful document is listed below. The following Microchip document is available and recommended as a supplemental reference resource.

- **MCP16701 Data Sheet – *"High-performance, High-accuracy PMIC for High-end MPU and FPGA Power Solutions"* (DS20006993)**

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support.

DOCUMENT REVISION HISTORY

Revision A (March 2025)

- Initial Release of this Document.

NOTES:

Chapter 1. Product Overview

1.1 INTRODUCTION

This chapter provides an overview of the MCP16701 (EV23P28A) Evaluation Board and covers the following topics:

- MCP16701 Short Overview
- MCP16701 (EV23P28A) Evaluation Board Overview
- Contents of the MCP16701 (EV23P28A) Evaluation Board Kit

1.2 MCP16701 SHORT OVERVIEW

The MCP16701 is a Power Management Integrated Circuit (PMIC) dedicated to FPGA and high-end MPU applications. The MCP16701 supports commercial and industrial applications.

The MCP16701 integrates eight parallelable DC-DC buck regulators, four auxiliary LDOs and one low-input/low-output voltage LDO Controller using an external MOSFET. It also features an interrupt flag that signals faults and a 3.4 MHz I^2C interface, and provides support for a large number of FPGAs.

The buck channels support loads up to 1.5A. All low-voltage bucks are 100% duty cycle capable. They can be operated either independently or paralleled in groups of four to support higher currents.

Four 300 mA LDOs are provided so that sensitive analog loads can be supported. The LDOs can also be cascaded (in groups of two) to the output of a DC-DC channel, thus improving overall conversion efficiency.

The MCP16701 power management settings allow for the implementation of low-power mode commanded by a GPIO pin (MODE input of MCP16701). Any channel can also be selectively and permanently set in Auto PFM or FPWM.

Active discharge resistors are provided on each output. All Buck channels and LDOs support soft start-up.

The MCP16701 is available in a 64-pin, 8 mm x 8 mm VQFN package with an operating junction temperature range from -40°C to +105°C.

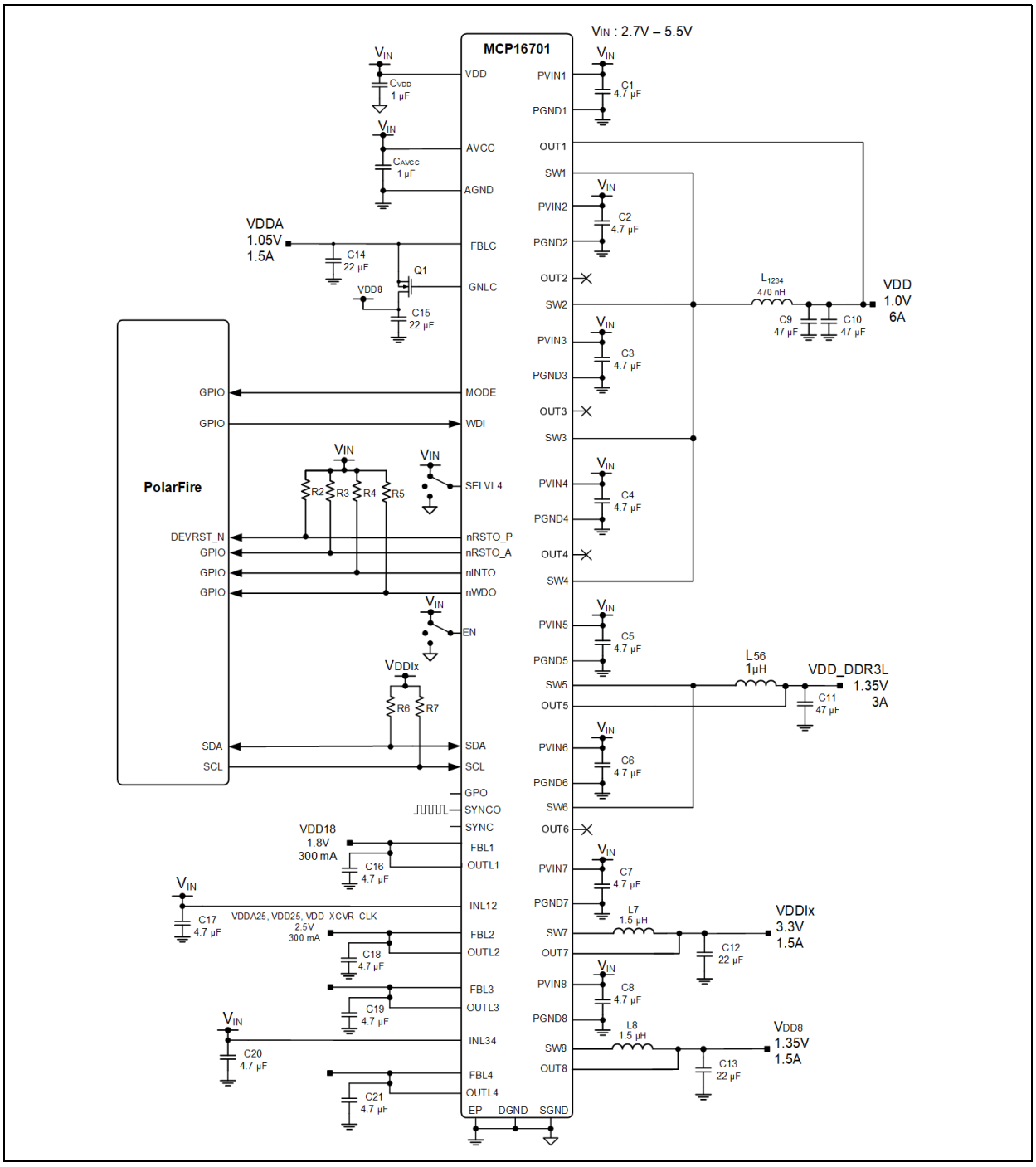


FIGURE 1-1: *Typical MCP16701 with PolarFire Application.*

1.3 MCP16701 (EV23P28A) EVALUATION BOARD OVERVIEW

The MCP16701 (EV23P28A) Evaluation Board is designed to simplify the evaluation and testing of the MCP16701 capabilities. The V_{IN} supply has a 2.7V - 5.5V range and V_{OUT} has a 0.6V - 3.8V range for Bucks and LDOs, and 0.6V - 1.6V for the LDO Controller.

The chosen configuration of the Evaluation Board for the Buck Converters is as follows: Bucks 1-4 in parallel, Bucks 5-6 in parallel, Buck 7 and Buck 8 independent. The LDO Controller is powered by VOUT8.

An on-board MCP2221, which is an USB 2.0 to I^2C/UART Protocol Converter with GPIO, is placed on the board to simplify the configuration of the MCP16701.

The PMIC's mode change can be done with either the 3-pin jumper on the MODE pin or by using the I^2C Monitor GUI to change registry settings.

The on-board load transient generator circuit can be used with an external signal generator to evaluate the load step response of Bucks 1-4 and LDO Controller.

1.4 CONTENTS OF THE MCP16701 (EV23P28A) EVALUATION BOARD KIT

The MCP16701 (EV23P28A) Evaluation Board kit includes:

- MCP16701 (EV23P28A) Evaluation Board (EV23P28A)
- Important Information Sheet

NOTES:

Chapter 2. Installation and Operation

2.1 INTRODUCTION

The MCP16701 (EV23P28A) Evaluation Board was developed to test the MCP16701's capabilities, monitoring features and control settings through the USB interface (via the I^2C Monitor GUI).

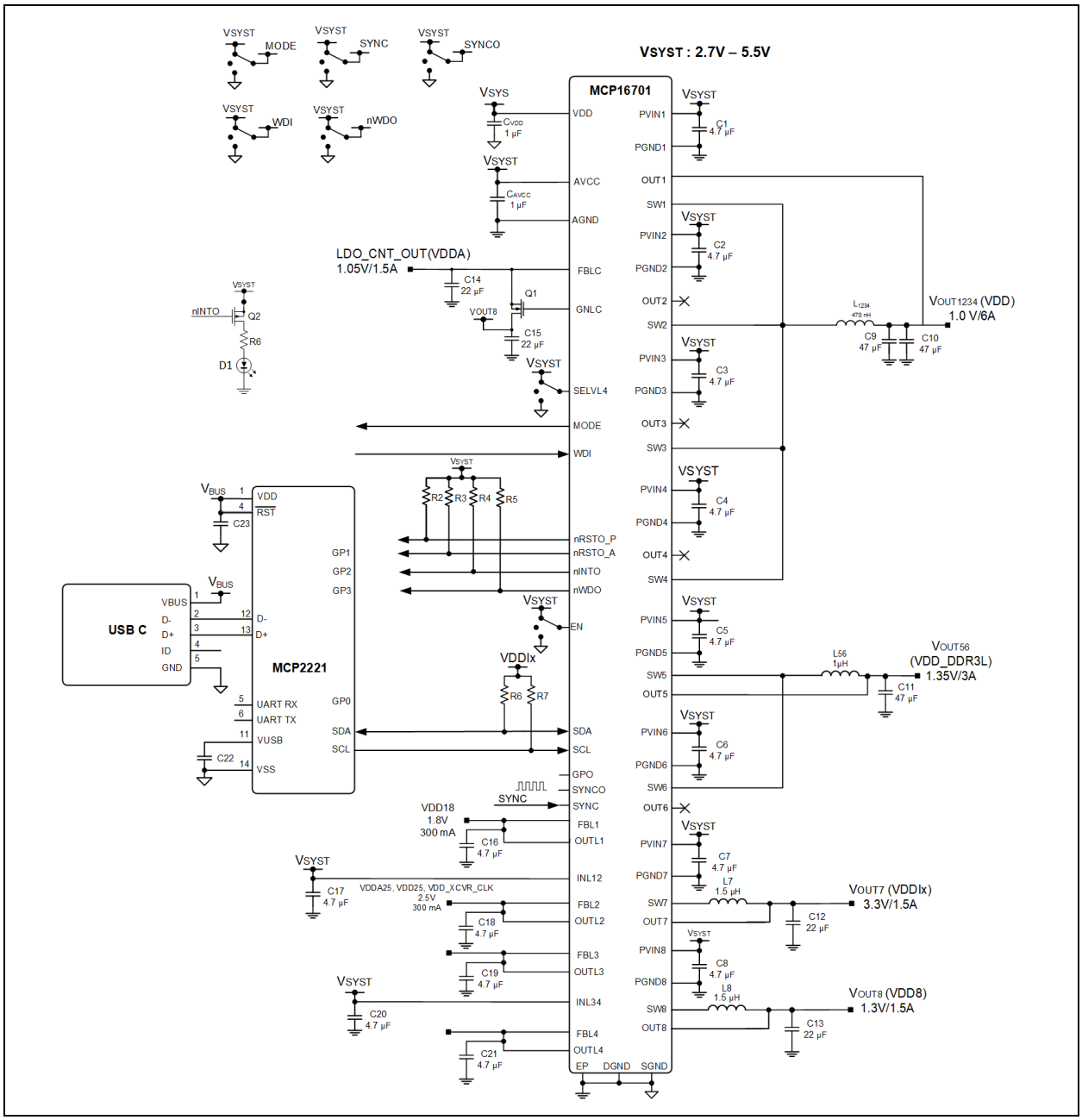


FIGURE 2-1: *MCP16701 (EV23P28A) Evaluation Board with MCP2221 I^2C Bridge.*

2.2 FEATURES

The MCP16701 (EV23P28A) Evaluation Board has the following features:

- Input Voltage: 2.7V to 5.5V
- Eight 1.5A Buck DC-DC Channels
- Four 300 mA High-Accuracy LDOs
- One High-Accuracy, High-PSRR LDO Controller Using External N-channel MOSFET(Q1)
- Output Voltage of 1V for Paralleled Bucks1-4 and Current Capability up to 6A
- Output Voltage of 1.35V for Paralleled Bucks5-6 and Current Capability up to 3A
- Output Voltage of 3.3V for Buck7 and Current Capability of 1.5A
- Output Voltage of 1.35V for Buck8 and Current Capability of 1.5A
- 100% Duty Cycle Capability of Buck Channels
- LDO Controller Output Voltage: 1.05V
- Reference Ground (REFGND) is Routed to Bucks1-4 for an Improved Accuracy of the Output Voltage
- Low-Noise Forced-PWM and Light-Load High-Efficiency Mode Available (Pin-Selectable or Bit Control)
- External Synchronization of Switching Frequency; this Feature can be Active or Disabled in Registry
- Selectable Phase (0°, 90°, 180° or 270°) for Buck Channels
- Global RESET (nRSTO_A) with Programmable Deassertion Delay
- User-defined RESET (nRSTO_P) with Programmable Deassertion Delay
- 400 kHz MCP2221 I^2C Interface; the PMIC has a Maximum of 3.4 MHz Frequency
- On Die Programmable NVM
- NVM Write Password Protection (e.g., Voltage Setting)
- Dedicated VDD Supply Pin for NVM and Interface Allows Programming without Powering up the Application
- Reconfigurable During Runtime
- Hiccup-Mode Current Limit for Buck Channels (can be Disabled)
- Programmable Thermal Early Warning and Thermal Shutdown Protection
- LED Visual Indicator for the nINTO pin (interrupt flag) with Selectable Interrupt Masking for Each Channel
- On-Board Load Transient Generator for VOUT1234 and LDOC_OUT
- Test Points and Headers for all Available Outputs and Input
- Test Points for Switch Nodes
- Headers for Ease of Access to all Digital Signals
- USB-C Connector for Easy Connection with Host PC
- General Purpose Output (GPO)
- Watchdog Timer (WDT)
- 64-pin VQFN Package, 8 mm x 8 mm
- -40°C to +105°C Junction Temperature Range

2.3 GETTING STARTED

The MCP16701 (EV23P28A) Evaluation Board is fully assembled and tested to evaluate and demonstrate the MCP16701.

This board requires a power supply at VSYST with at least 7A current capability if multiple channels are tested under load. Furthermore, the MCP16701 (EV23P28A) Evaluation Board can be powered directly from the USB connector by connecting jumper J5. Note that in this configuration, the amount of power that can be supplied at the outputs is limited by the USB connection and R11. This is only meant to test the sequencing and change register settings using the GUI.

2.3.1 Power Input and Output Connections

To power up the MCP16701, follow the steps below:

1. Connect a power supply to the VSYST and PGND terminals. An ammeter may be placed between the input supply and the VSYST terminal of the evaluation board to monitor the input power. Ensure that the supply voltage is monitored at the VSYST terminal. The ammeter and/or power lead resistance can reduce the voltage supplied to the input.

   Note: Keep the power supply disabled; do not apply power before Step 5.

2. Connect the loads to the VOUTx for Buck converters or OUTLx for LDOs or LDO_CNT_OUT for LDO Controller and PGND terminals. The load can be either passive (resistive) or active (electronic load). An ammeter can be placed between the load and each output terminal to monitor the power rails' current consumption. Ensure that the output voltage is monitored at the output terminals. Alternatively, for high-speed load transient testing of Buck1-4 or LDO Controller, the on-board load transient generator can be used.
3. Make sure the jumpers are connected as in Figure 2-2 (MODE = EN = VDD = HIGH).
4. At this step, the GUI is required to start up the regulators. By default, the evaluation board is preconfigured with the correct registry settings with some of the regulators enabled and others disabled.

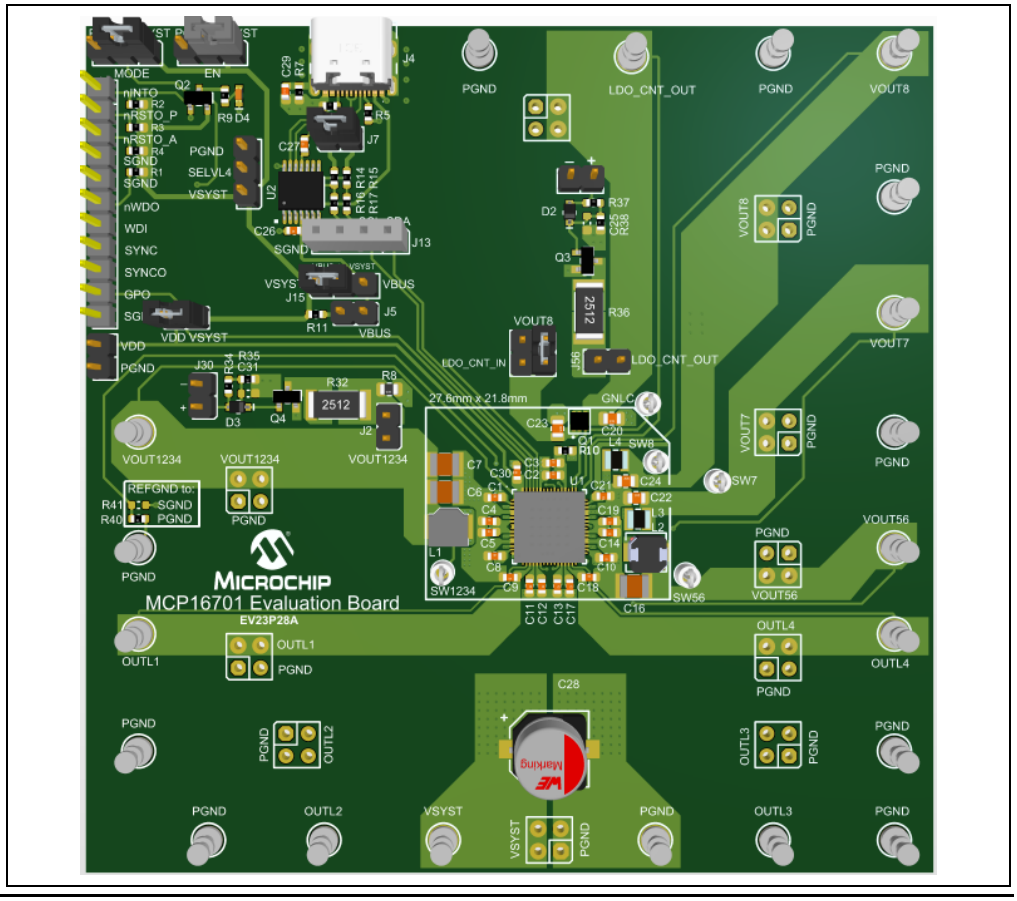


FIGURE 2-2: *MCP16701 (EV23P28A) Evaluation Board Connections.*

5. Set the power supply to 5V and turn it on. Alternatively, if no power supply is available, a jumper can be connected to J5, so that the board is powered from the USB connection.
6. Verify that the output voltages are regulated to the desired V_{OUT} setting of each channel.

2.4 ON-BOARD LOAD TRANSIENT GENERATOR

The MCP16701 (EV23P28A) Evaluation Board provides circuitry to enable load transient testing with fast current rise time and fast, yet controlled, fall time. This is done by fast turn-on, controlled turn-off MOSFET switches (Q3 and Q4). The MOSFETs must be driven by an external signal generator, connected at J30 for Bucks1234 or at J58 for the LDO controller, using a square wave (the suggested low level is 0V, the high level is 5V-6V). Drive levels can be adjusted to modify the switching speed of Q3/Q4, but it is recommended to always ensure complete turn-on and turn-off of the MOSFET after settling, while not exceeding its V_{GS} ratings. By default, the resistor R32 is 0.33Ω, with a power dissipation rating of 1W for Bucks1234. The R36 resistor for the LDO Controller is 2W, with a power dissipation rating of 1W. It is very important not to exceed the power dissipation limit of the resistors. When using the 2512 resistor (1W rating), the constraint is:

EQUATION 2-1:

$$D \times \frac{V_{OUT}^{2}}{R2} < 1W$$

Where:

D = The on-time duty cycle of Q1

V_{OUT} = The selected output voltage

Note: Considerations before performing a load step at Bucks1234 output: $V_{OUT1234}$ is set to 1V. In the standard configuration with R32 at 0.33Ω with a power dissipation rating 1W, the maximum duty cycle from the signal generator is calculated based on the equation below.

EQUATION 2-2:

$$D_{1234\_MAX} < \frac{R}{V_{OUT\_1234}^{2}} \times PowerRating = \frac{0.33\Omega}{1V^{2}} \times 1W = 33.3\%$$

Considerations before performing a load step at the LDO Controller: LDO_CNT_OUT is set to 1.05V. In the standard configuration with R36 at 2Ω with a power dissipation rating of 1W, the maximum duty cycle will be reached. However, if the LDO Controller's output voltage is increased, up to the maximum value of 1.6V, the duty cycle from the signal generator is calculated based on Equation 2-3.

EQUATION 2-3:

$$D_{LDOCNT\_MAX} < \frac{R}{V_{LDOCNT\_OUT}^{2}} \times PowerRating = \frac{2\Omega}{1.6V^{2}} \times 1W = 78.1\%$$

The open drain transient generators are especially useful when testing at very low output voltages, because not many active loads can perform well under those conditions, while current rise times achievable with external load boards are limited by stray inductance.

2.5 LAYOUT CONSIDERATIONS

The MCP16701 PMIC requires at least 25 vias from the ICs Exposed Pad to the ground (GND) plane to dissipate the generated heat. The GND plane can be increased or decreased based on the ambient temperature, air flow or other devices that generate heat. The rule of thumb is that the GND plane must be as big as possible.

The MCP16701 also features Power Ground (PGND) pins that must be connected to the power components (power input and output capacitors) and to a low-impedance return path, such as a dedicated plane or copper pour. It is also recommended to connect the input and output capacitors GND connections, as well as the PGND pins on the same layer (thus, avoiding vias inductance) and the same continuous copper plane for optimal performance.

Connecting the PGND pins and GND planes at the Exposed Pad is recommended (see **Appendix A. "Schematic and Layouts"** for a PCB layout example). For low Electromagnetic Interference (EMI) emissions, routing the switching node of the Buck regulators on an internal plane is recommended, surrounded/enclosed by input supply voltage distribution or GND planes.

The REFGND is a reference to all the regulators and gives better performance to the rail that it is tied close to, but the others have a slight disadvantage. For FPGAs, the core rail is the most important; so it is recommended that the REFGND go directly to the core supply GND. For the MCP16701 Evaluation Board, $V_{OUT1234}$ is suited for the core rail.

NOTES:

Chapter 3. GUI Installation and Operation

3.1 GETTING STARTED

To install, use and evaluate the product, several software and hardware tools are required.

3.1.1 Required Software

- I²C Monitor Graphical User Interface 9.0 or higher
- Microsoft®.NET Framework 4.5 or higher
- Adobe® Reader®
- Windows® 10 or later

3.1.2 Required Hardware

- MCP16701 (EV23P28A) Evaluation Board
- USB-to-USB-C Cable

3.2 GRAPHICAL USER INTERFACE INSTALLATION

The following steps describe how to install the I²C Monitor Graphical User Interface:

1. If Microsoft.NET Framework is already installed, go to Step 3. If not, download Microsoft.NET Framework from www.microsoft.com and follow the installation instructions.
2. If Adobe Reader is already installed, go to Step 3. If not, download Adobe Reader from http://get.adobe.com/reader/ and follow the installation instructions.
3. Download the I²C Monitor Graphical User Interface archive from the product web page under "Documentation".
4. Unzip the I²C Monitor Graphical User Interface archive, which contains the `setup.exe` file.

> **Note:** If an older version or a corrupted version of the current I²C Monitor Graphical User Interface is already installed on the computer, see **Section 3.3 "I2C Monitor Graphical User Interface Uninstall"** before proceeding with the installation.

5. Double-click the `setup.exe` file to open the Install Shield Wizard window and wait for the extraction to complete. If required, the installation can be stopped by pressing the **Cancel** button.

6. In the Welcome to the InstallShield Wizard for I2CMonitor window, click the **Next** button to start the installation.

FIGURE 3-1: *Starting the I²C Monitor Graphical User Interface Installation.*

7. The installation path can be changed, although it is recommended to keep the default path. Click **Next** to continue.

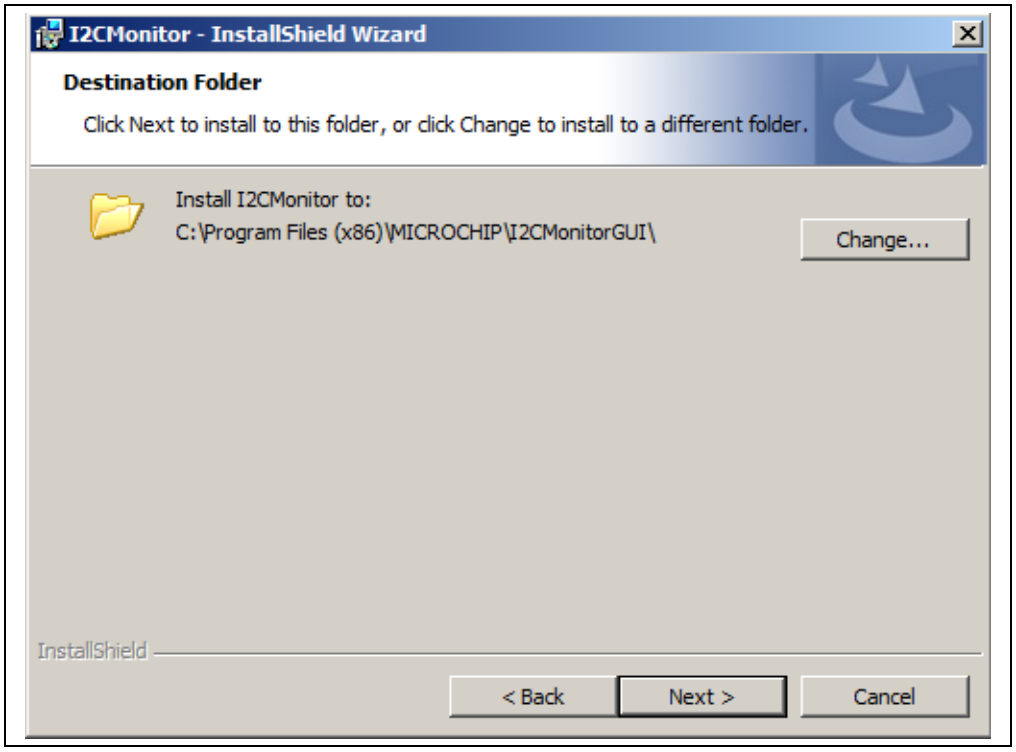


FIGURE 3-2: *Selecting the Destination Folder.*

8. In the Ready to Install the Program window, click the **Install** button and wait for the application to proceed with the installation.

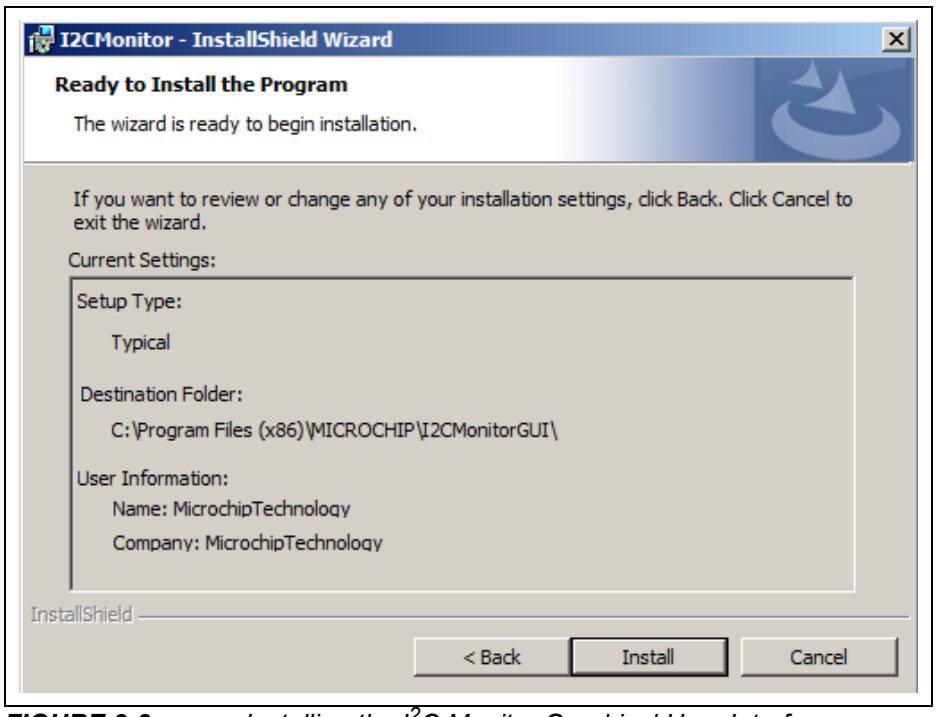


FIGURE 3-3: *Installing the I²C Monitor Graphical User Interface.*

9. Once the installation is complete, click **Finish** to end the installation. To start the GUI, either click the desktop icon or browse to *Windows Start>All Programs>Microchip>I2C Monitor*.

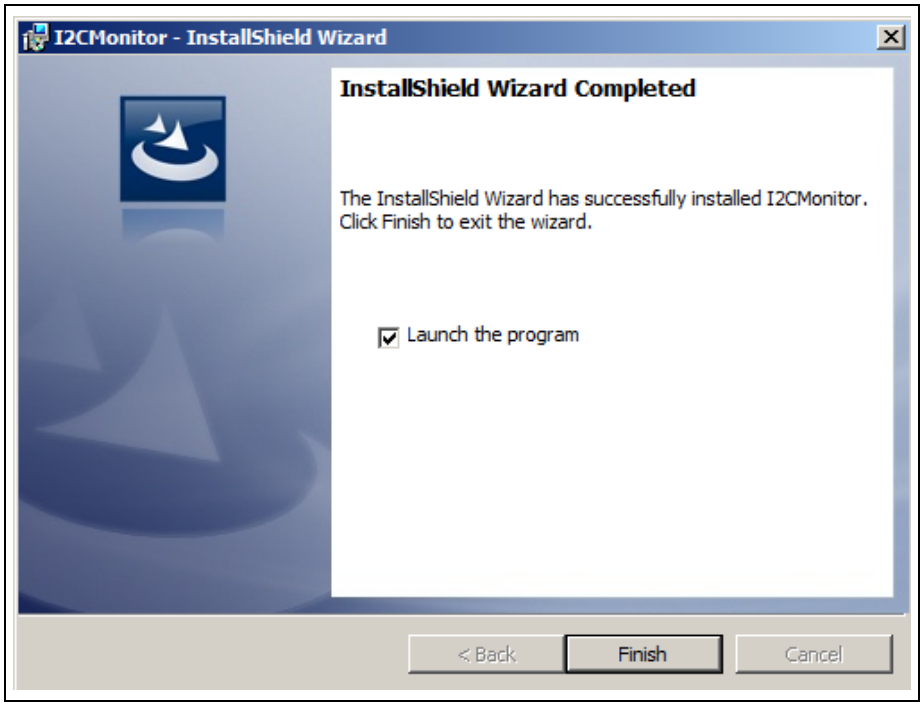


FIGURE 3-4: *InstallShield Wizard Completed Window.*

3.3 I²C MONITOR GRAPHICAL USER INTERFACE UNINSTALL

To install a new version of the I²C Monitor Graphical User Interface, any previous or corrupted version must be removed from the computer.

To uninstall, go to *Windows Start>Control Panel>Uninstall a program>I2C Monitor*.

The I²C Monitor will automatically close once the process is complete.

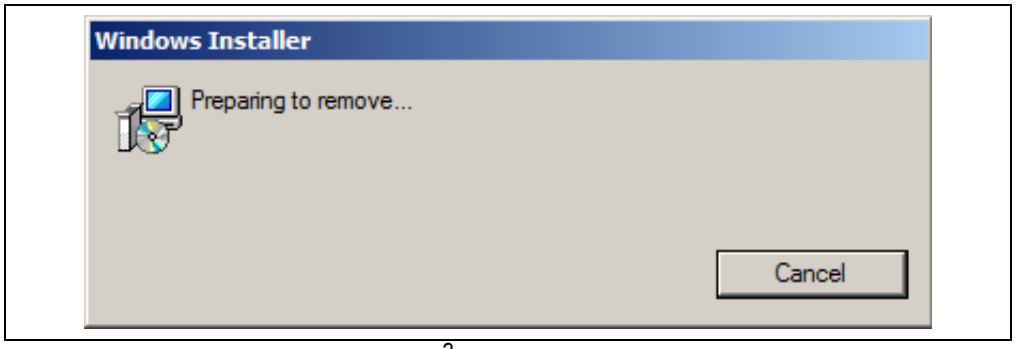


FIGURE 3-5: *Uninstalling the I²C Monitor Graphical User Interface.*

Chapter 4. GUI Description

4.1 INTRODUCTION

This chapter describes how to use the I²C Monitor Graphical User Interface with the MCP16701 (EV23P28A) Evaluation Board.

NOTICE

This chapter provides information on how to use the GUI with the MCP16701. For other devices using the I²C Monitor Graphical User Interface, see their specific Data Sheets and User's Guides.

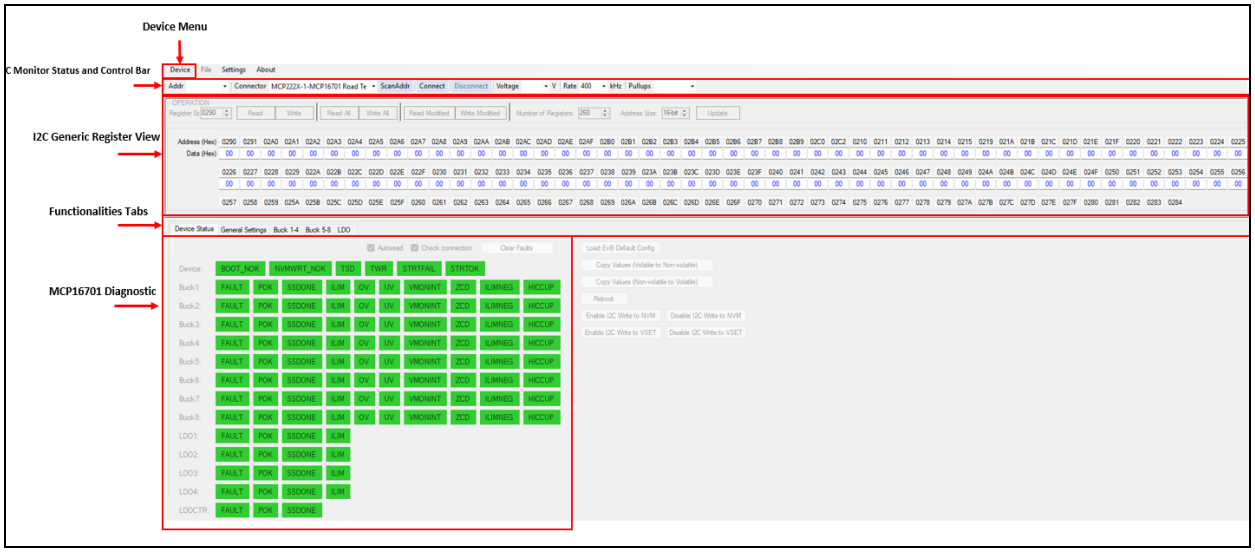


FIGURE 4-1: *I²C Monitor Graphical User Interface Main Window - MCP16701 View.*

All the changes to register values are made in the Volatile Register Map. For these changes to be present after a re-power of the PMIC, follow these steps:

1. Enable I2C Write to VSET and Enable I2C Write to NVM by pressing the corresponding buttons.
2. Copy the Values (Volatile to Non-Volatile) by pressing the corresponding button.
3. Write all registers values by pressing the corresponding button.

4.2 GRAPHICAL USER INTERFACE

4.2.1 Device Menu

The Device drop-down menu allows the user to select the device to be evaluated.

4.2.2 I²C Monitor Status and Control

The *Status and Control* bar contains the items described in Table 4-1.

FIGURE 4-2: *I²C Monitor Status and Control Bar.*

TABLE 4-1: MONITOR STATUS AND CONTROL BAR

Item	Description
Addr	This drop-down menu shows the address of the available devices.
Connector	This drop-down menu shows the type of connector used to connect the board.
ScanAddr	This button is used to scan for a valid address.
Connect/Disconnect	These buttons are used to connect/disconnect the current selected device.
Voltage	This drop-down menu is used to select the voltage level of the communication when using the PICkit™ Serial Analyzer.
Rate	This drop-down menu is used to select the corresponding communication rate for the device.
Pull-ups	This drop-down menu is used to activate the internal pull-ups from the PICkit Serial Analyzer.

In the *Status and Control* bar, the user can select the hardware tool for communicating with the device and the setting it allows.

To connect to a device, the user must first follow the first three steps described in **Section 2.3 "Getting Started"**. After connecting the USB-USB-C cable, the user must scan for a valid address. When a valid address is detected, clicking the **Connect** button initializes the connection with the device, and the registers are available for read and write operations.

4.2.3 I²C Generic Register View

The I²C Generic Register View area contains the items described in Table 4-2. This section of the I²C Monitor GUI is common for any device evaluated.

FIGURE 4-3: *Generic Register View Area.*

TABLE 4-2: I²C GENERIC REGISTER VIEW ITEMS

Panel	Item	Description
Operation	Register	This section shows the registers available for read/write operations.
	Read/Write	These buttons are used for single register read/write operations.
	ReadAll/WriteAll	These buttons are used for reading/writing all the available registers.
	Number of Registers	In this section, the user can set the number of available registers for read/write operations.
	Address Size	In this section, the user can set the registers Address size.
	Update	This button sets the number of available registers for read/write operations in the Register Area.
Register Area		This section shows the current status of the registers address and the content.

The MCP16701 specific registers are described in the MCP16701 Data Sheet.

4.2.4 MCP16701 I²C Diagnostic

The MCP16701 I²C Diagnostic part of the GUI resumes the information contained in the STATUS register.

FIGURE 4-4: *I²C Diagnostic Area.*

This region marks the status and faults of each corresponding bits in the registers. For the SSDONE, STRTOK and POK status flags, green signals a '1' condition and red signals a '0' condition. For the TSD, TWR, BOOT_NOK, NVMWRT_NOK, VMONINT, FAULT, HICCUP, ZCD, OV, UV, STRTFAIL, ILIM, Fault flags, green signals a '0' condition and red signals a '1' condition an active Fault.

If the "Autoread" box is checked, all the information is refreshed automatically. All Fault flags are reset on read, so the GUI memorizes the apparition of a Fault. To clear them from the GUI, the **Clear Faults** button must be clicked.

4.2.5 MCP16701 Special Commands

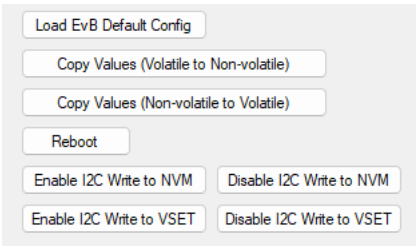


FIGURE 4-5: *Special Commands.*

MCP16701 has a list of special commands:

- Load EvB Default Config will load the typical application registry settings for the evaluation board. After loading the config, click the **Write All** button to make the changes effective.
- REBOOT is equivalent to a device turn-off. It reloads all values from the EEPROM content to volatile registers, followed by a new start-up sequence.
- Enable I2C Write to NVM is required to change the settings of the registers located in the non-volatile memory. Disable I2C Write to NVM revokes write access in the non-volatile memory.
- To change the output voltages, Enable I2C Write to VSET is required; otherwise, any changes to VSET settings will not be taken into account. Disable I2C Write to VSET revokes write access to VSET settings to avoid accidental changes in the VOUT settings.

4.2.6 MCP16701 I2C General Settings

This area of the GUI allows the user to modify the General related features of the PMIC.

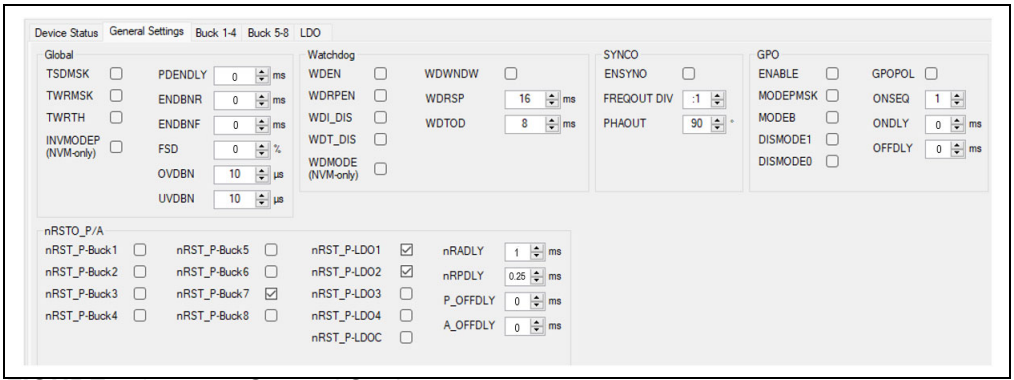


FIGURE 4-6: *General Settings.*

nRSTO_P is an individual POK monitor; it has to be enabled for each channel that needs to be monitored at start-up/shutdown. For the MCP16701 Evaluation Board, the monitored channels are BUCK7, LDO1 and LDO2 because these have VOUT set for I/O rails. When all the I/O rails have successfully powered on (POK threshold is reached), the monitored rails are fully working.

nRSTO_A is the global Reset; it will deassert after all regulators have started correctly.

4.2.6.1 MCP16701 GLOBAL

The MCP16701 Global area in General Settings contains the items in Table 4-3.

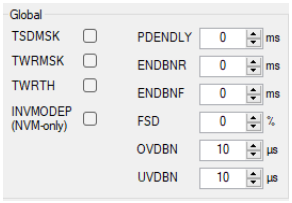


FIGURE 4-7: *Global Settings.*

TABLE 4-3: GLOBAL

Panel	Item	Description
Global	TSDMSK	If the TSDMSK box is ticked, nINTO assertion at Thermal Shutdown is masked.
	TWRMSK	If the TWRMSK box is ticked, nINTO assertion during Thermal Early Warning is masked.
	TWRTH	If the TWRTH box is ticked, Thermal Early Warning Threshold is set to 1.
	INVMODEP (NVM-only)	If the INVMODEP box is ticked, MODE polarity is inverted.
	PDENDLY	This spin box allows Power-Down Enable Delay for Enable L-to-H transition to be ignored until the delay has expired.
	ENDBNR	This spin box allows for debounce time for L-to-H transition of Enable.
	ENDBINF	This spin box allows for debounce time for H-to-L transition of Enable.
	FSD	This spin box allows for Switching Frequency Displacement.
	OVDBN	This spin box allows for Overvoltage comparator debouncing delay.
	UVDBN	This spin box allows for Undervoltage comparator debouncing delay.

4.2.6.2 MCP16701 WATCHDOG

The MCP16701 Watchdog area in General Settings contains the items in Table 4-4.

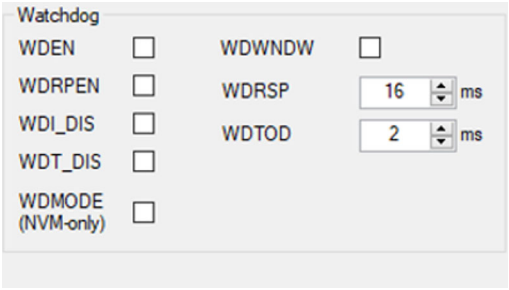


FIGURE 4-8: *Watchdog Settings.*

TABLE 4-4: WATCHDOG

Panel	Item	Description
Watchdog	WDEN	If the WDEN box is ticked, the Watchdog is enabled.
	WDRPEN	If the WDRPEN box is ticked, the Watchdog is enabled on nRSTO_P deassertion.
	WDI_DIS	If the WDI_DIS box is ticked, the Watchdog counter will not be incremented during H-to-L transitions.
	WDT_DIS	If the WDT_DIS box is ticked, the Watchdog counter will not be incremented during Watchdog Timer timeout.
	WDMODE (NVM-only)	If the WDMODE box is ticked, the Watchdog is in MODE 1.
	WDWNDW	If the WDWNDW box is ticked, the Watchdog is windowed.
	WDRSP	This spin box allows the change of Watchdog pulse width.
	WDTOD	This spin box allows for different time-out delays for the Watchdog.

4.2.6.3 MCP16701 SYNCO

The MCP16701 SYNCO area in General Settings contains the items in Table 4-5.

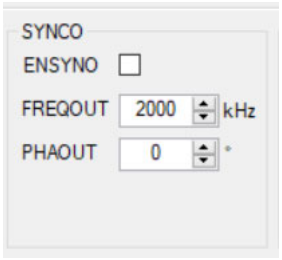


FIGURE 4-9: *SYNCO Settings.*

TABLE 4-5: SYNCO

Panel	Item	Description
SYNCO	ENSYNO	If the ENSYNO box is ticked, Syncronization Output is enabled.
	FREQOUT	This spin box allows for different division ratio for external syncronization.
	PHAOUT	This spin box allows for the syncronization signal to have a different phase.

4.2.6.4 MCP16701 GPO

The MCP16701 GPO area in General Settings contains the items in Table 4-6.

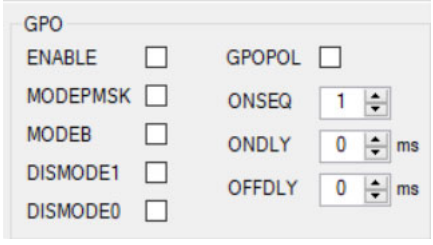


FIGURE 4-10: *GPO Settings.*

TABLE 4-6: GPO

Panel	Item	Description
GPO	ENABLE	If the ENABLE box is ticked, GPO is enabled during start-up.
	MODEPMSK	If the MODEPMSK box is ticked, MODE pin is masked.
	MODEB	If the MODEB box is ticked, MODE pin value is irrelevant.
	DISMODE1	If the DISMODE1 box is ticked, the channel will be disabled when MODE is 1 even if ENABLE is 1.
	DISMODE0	If the DISMODE0 box is ticked, the channel will be disabled when MODE is 0, even if ENABLE is 1.
	GPOPOL	If the GPOPOL box is ticked, the polarity of GPO is inverted.
	ONSEQ	This spin box assigns GPO to a certain ON sequence step.
	ONDLY	This spin box programs the delay between the end of the previous sequence and assertion of GPO.
	OFFDLY	This spin box programs the delay between the deassertion of ENABLE and the deassertion of GPO.

4.2.6.5 MCP16701 NRSTO_P/A

The MCP16701 nRSTO_P/A area in General Settings contains the items in Table 4-7.

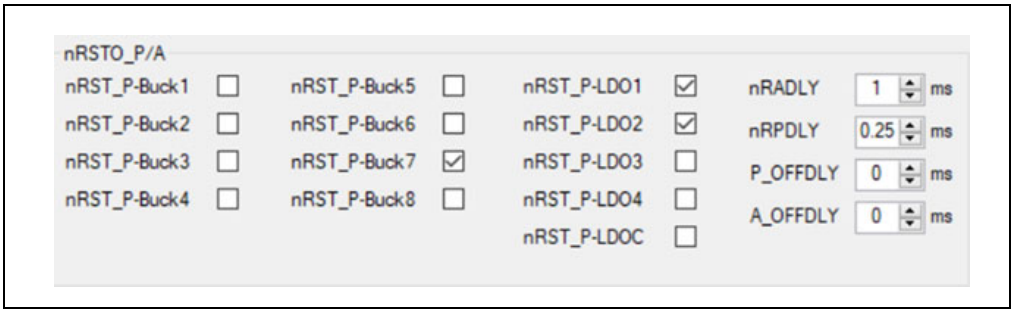


FIGURE 4-11: *nRSTO_P/A Settings.*

TABLE 4-7: NRTSTO_P/A

Panel	Item	Description
nRSTO_P/A	nRST_P BUCKs 1-to-8	If the nRST_P for BUCKS 1-to-8 box is ticked, the channel will be taken into consideration for nRSTO_P deassertion.
	nRST_P LDOs 1-to-4 and LDOC	If the nRST_P for LDOs 1-to-4 and LDOC box is ticked, the channel will be taken into consideration for nRSTO_P deassertion.
	nRADLY	This spin box sets the delay of deassertion of nRSTO_A.
	nRPDLY	This spin box sets the delay of deassertion of nRSTO_P.
	P_OFFDLY	This spin box sets the delay between the deassertion of ENABLE input and the assertion of nRSTO_P.
	A_OFFDLY	This spin box sets the delay between the deassertion of ENABLE input and the assertion of nRSTO_A.

4.2.7 MCP16701 I²C Buck Channel Settings

This area of the GUI allows the user to modify the Buck-related features individually for each of the eight Buck channels. There are two tabs for the Buck Channels, the first one is for Bucks 1 to 4 and the second one for Bucks 5 to 8.

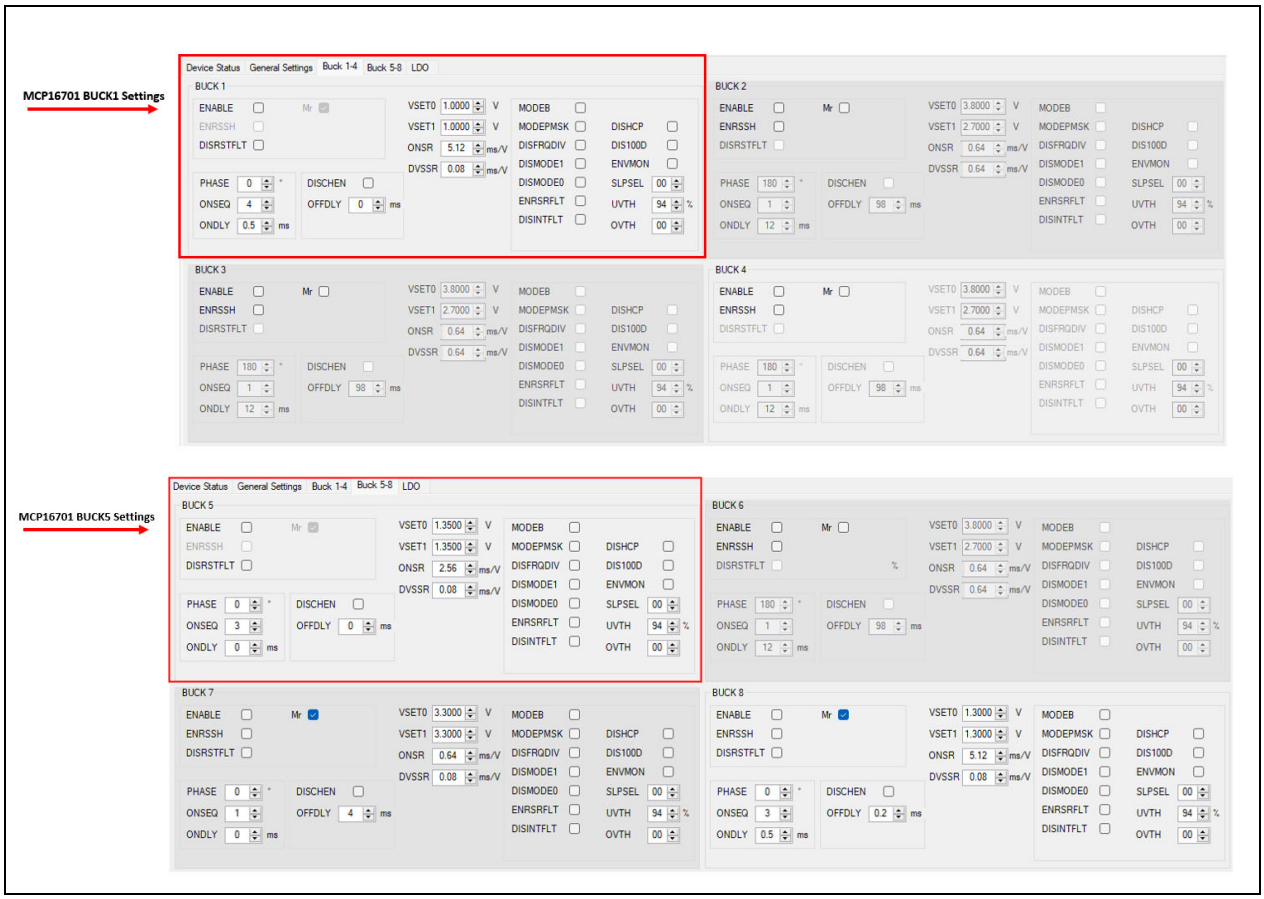


FIGURE 4-12: *I²C Buck Channel Settings.*

4.2.7.1 MCP16701 BUCKS 1-TO-8 GENERAL

The MCP16701 General area in BUCKS 1-to-8 contains the items in Table 4-8.

FIGURE 4-13: *General Buck Channel Settings.*

TABLE 4-8: GENERAL

Panel	Items	Description
General	ENABLE	If the ENABLE box is ticked, the channel will activate at start-up.
	DISRSTFLT	If the DISRSTFLT box is ticked, nRSTO_A/P will not deassert upon channel Fault during runtime.
	ENRSSH	If the ENRSSH box is ticked, a replica channel is disabled with the ENABLE bit.
	Mr	If the Mr box is ticked, the channel will be set to Main. BUCKs 1 and 5 are always Main, cannot be replica.
	VSET0	This spin box changes the output voltage of the channel when MODE is '0'.
	VSET1	This spin box changes the output voltage of the channel when MODE is '1'.

4.2.7.2 MCP16701 BUCKS 1-TO-8 START-UP, SHUTDOWN AND DYNAMIC VOLTAGE SCALING

The MCP16701 Start-Up, Shutdown and Dynamic Voltage Scaling area in BUCKS 1-to-8 contains the items in Table 4-9.

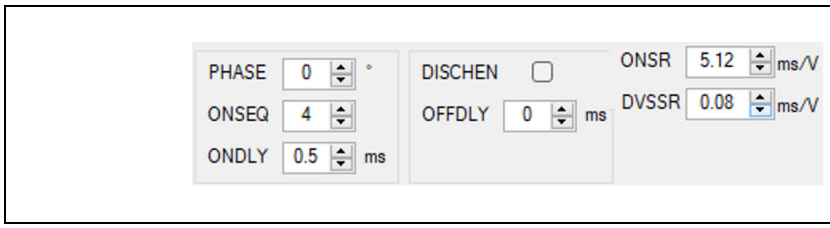


FIGURE 4-14: *Start-up, Shutdown and Dynamic Voltage Scaling Settings for Buck Channels.*

TABLE 4-9: START-UP, SHUTDOWN AND DYNAMIC VOLTAGE SCALING

Panel	Item	Description
Start-Up, Shutdown and DVSR	PHASE	This spin box sets the phase displacement of the Buck converter switch turn-on edge.
	ONSEQ	This spin box assigns the Buck to a certain ON sequence.
	ONDLY	This spin box sets the delay between the end of the previous sequence and the beginning of the converter turn-on.
	DISCHEN	If the DISCHEN box is ticked, the discharge resistor is enabled at turn-off.
	OFFDLY	This spin box sets the delay between the deassertion of ENABLE and the converter turn-off.
	DVSSR	This spin box set the slew-rate for DVS transitions.

4.2.7.3 MCP16701 BUCKS 1-TO-8 FEATURES

The MCP16701 Features area in BUCKS 1-to-8 contains the items in Table 4-10.

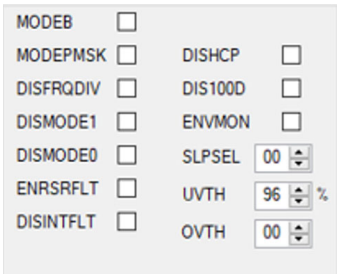


FIGURE 4-15: *Features Settings of Buck Channels.*

TABLE 4-10: FEATURES

Panel	Item	Description
Features	MODEB	If the MODEB box is ticked when MODEMSK = 1, the MODE pin is irrelevant and only MODEB value is taken into account.
	MODEPMSK	If the MODEMSK box is ticked, the MODE pin is not taken into consideration for a MODE change.
	DISFRQDIV	If the DISFRQDIV box is ticked, the frequency division algorithm in light-load efficiency is disabled.
	DISMODE1	If the DISMODE1 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 1.
	DISMODE0	If the DISMODE0 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 0.
	ENRSRFLT	If the ENRSRFLT box is ticked, when a channel has a Fault, an automatic restart will be invoked after 100 ms.
	DISINTFLT	If the DISINTFLT box is ticked, nINTO will not deassert upon channel Fault during runtime.
	DISHCP	If the DISHCP box is ticked, hiccup mode overcurrent protection is disabled for the channel.
	DIS100D	If the DIS100D box is ticked, duty cycle of the channel will be limited to 75%.
	ENVMON	If the ENVMON box is ticked, nINTO will deassert when an OV/UV condition is detected.
	SLPSEL	This spin box changes the slope compensation.
	UVTH	This spin box changes the threshold of undervoltage monitoring.
	OVTH	This spin box changes the threshold of overvoltage monitoring.

4.2.8 MCP16701 I²C LDO Channel Settings

This area of the GUI allows the user to modify the LDO related features individually for each of the four LDO channels and LDO Controller.

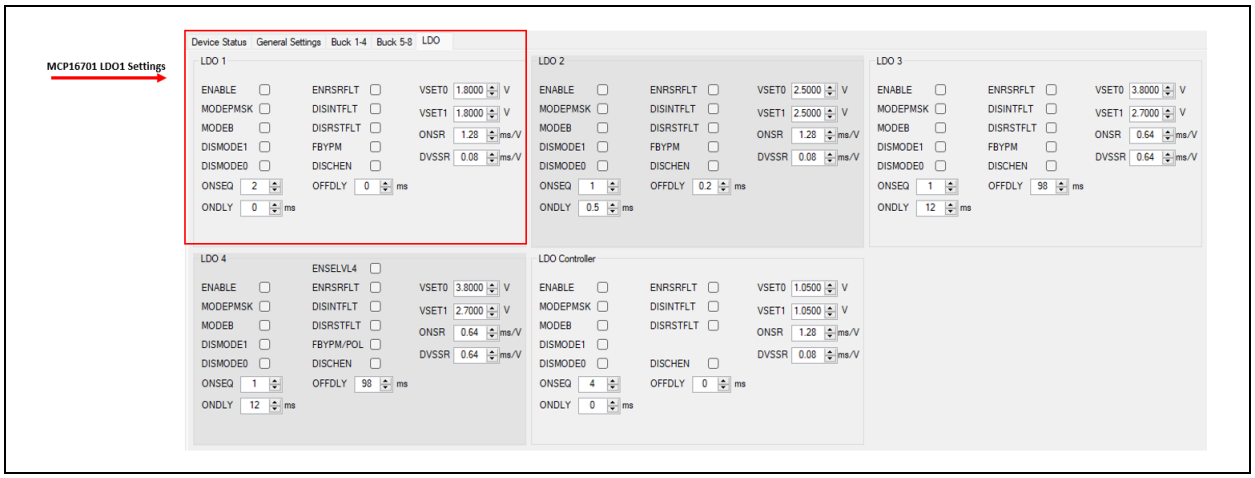


FIGURE 4-16: *I²C LDO Channel Settings.*

4.2.8.1 MCP16701 LDOS 1-TO-4 AND LDO CONTROLLER GENERAL

The MCP16701 General area in LDO contains the items in Table 4-11.

FIGURE 4-17: *General Settings for the LDOs.*

TABLE 4-11: GENERAL

Panel	Item	Description
General	ENABLE	If the ENABLE box is ticked, the channel will activate at Start-Up.
	MODEPMSK	If MODEMSK box is ticked, MODE pin is not taken into consideration for a MODE change.
	ENRSRFLT	If ENRSRFLT box is ticked, when a channel has a Fault, an automatic restart will be invoked after 100 ms.
	DISINTFLT	If DISINTFLT box is ticked, nINTO will not deassert upon channel Fault during runtime.
	VSET0	This spin box changes the output voltage of the channel when MODE is 0.
	VSET1	This spin box changes the output voltage of the channel when MODE is 1.
	ENSELVL4	(LDO4 only) If ENSELVL4 box is ticked, it enables SELVL4 to control LDO4 voltage between 1.8V and 3.3V.

4.2.8.2 MCP16701 LDOS 1-TO-4 AND LDO CONTROLLER START-UP, SHUTDOWN AND DYNAMIC VOLTAGE SCALING

The MCP16701 LDOs 1-to-4 and LDO Controller Start-Up, Shutdown and Dynamic Voltage Scaling area contains the items in Table 4-12.

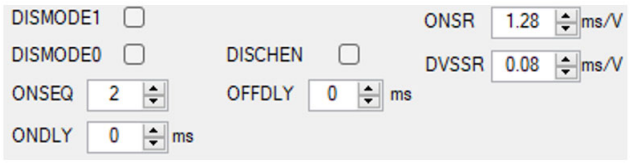


FIGURE 4-18: *Start-Up, Shutdown and Dynamic Voltage Scaling for LDOs.*

TABLE 4-12: START-UP, SHUTDOWN AND DYNAMIC VOLTAGE SCALING

Panel	Item	Description
Start-Up, Shutdown and DVSR	ONSEQ	This spin box assigns the LDO to a certain ON sequence.
	ONDLY	This spin box sets the delay between the end of the previous sequence and the beginning of the LDO turn-on.
	DISCHEN	If the DISCHEN box is ticked, the discharge resistor is enabled at turn-off.
	OFFDLY	This spin box sets the delay between the deassertion of ENABLE and the LDO turn-off.
	ONSR	This spin box sets the slew-rate for Soft-Start ramp.
	DVSSR	This spin box set the slew-rate for DVS transitions.

4.2.8.3 MCP16701 LDOS 1-TO-4 AND LDO CONTROLLER FEATURES

The MCP16701 LDOs 1-to-4 and LDO Controller Features area contains the items in Table 4-13.

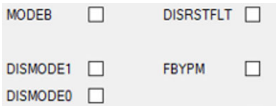


FIGURE 4-19: *Features Settings for LDOs.*

TABLE 4-13: FEATURES

Panel	Item	Description
Features	MODEB	If the MODEB box is ticked when MODEMSK = 1, the MODE pin is irrelevant and only the MODEB value is taken into account.
	DISRSTFLT	If the DISRSTFLT box is ticked, nRSTO_A/P will not deassert upon channel Fault during runtime.
	DISMODE1	If the DISMODE1 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 1.
	DISMODE0	If the DISMODE0 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 0.
	FBYPM/POL	(FBYPM exclusive LDOs 1-to-4) Forces LDOs in Load-Switch Mode.
		(POL LDO4 only) If this box is ticked and ENSELVL4 = 1, it selects the polarity of SELVL4 logic.

4.2.9 Status Bar

The status bar provides information on the status of the device connected to the PC.

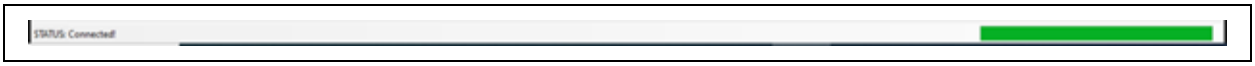


FIGURE 4-20: *Status Bar.*

TABLE 4-14: STATUS BAR ITEMS

Item	Description
Status Label	The label shows if there is any device connected to the board. Refer to Table 4-15 for a list of possible labels.
Progress Bar	This bar shows the level of completion for a given command.

TABLE 4-15: STATUS LABELS

Status Label	Description
STATUS: Connected!	This message is shown when the GUI connects to a device.
STATUS: Disconnected!	This message is shown when the GUI does not detect a connected device.

The specific settings for all control areas are detailed in the register map available in the MCP16701 data sheet.

NOTES:

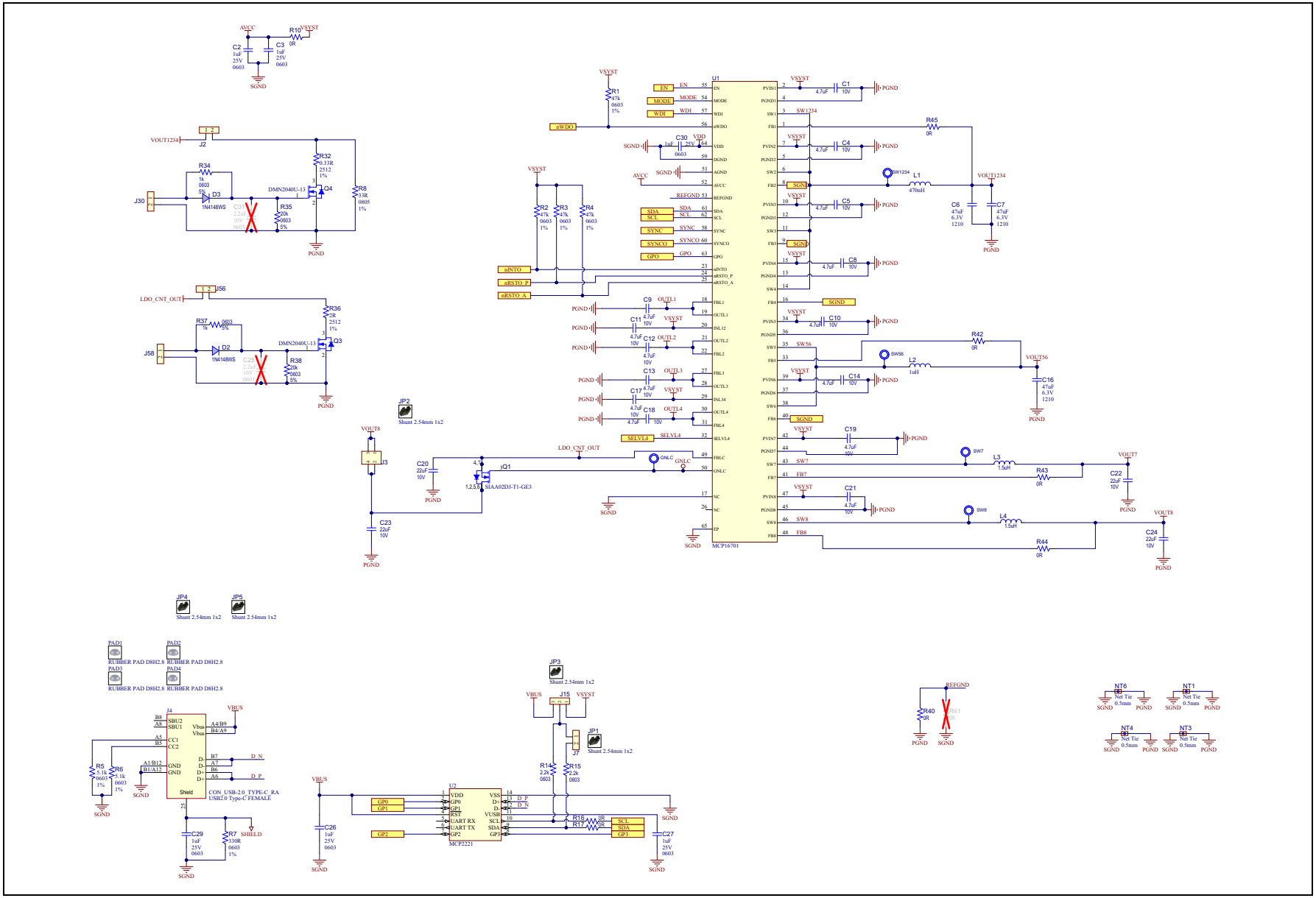
Appendix A. Schematic and Layouts

A.1 INTRODUCTION

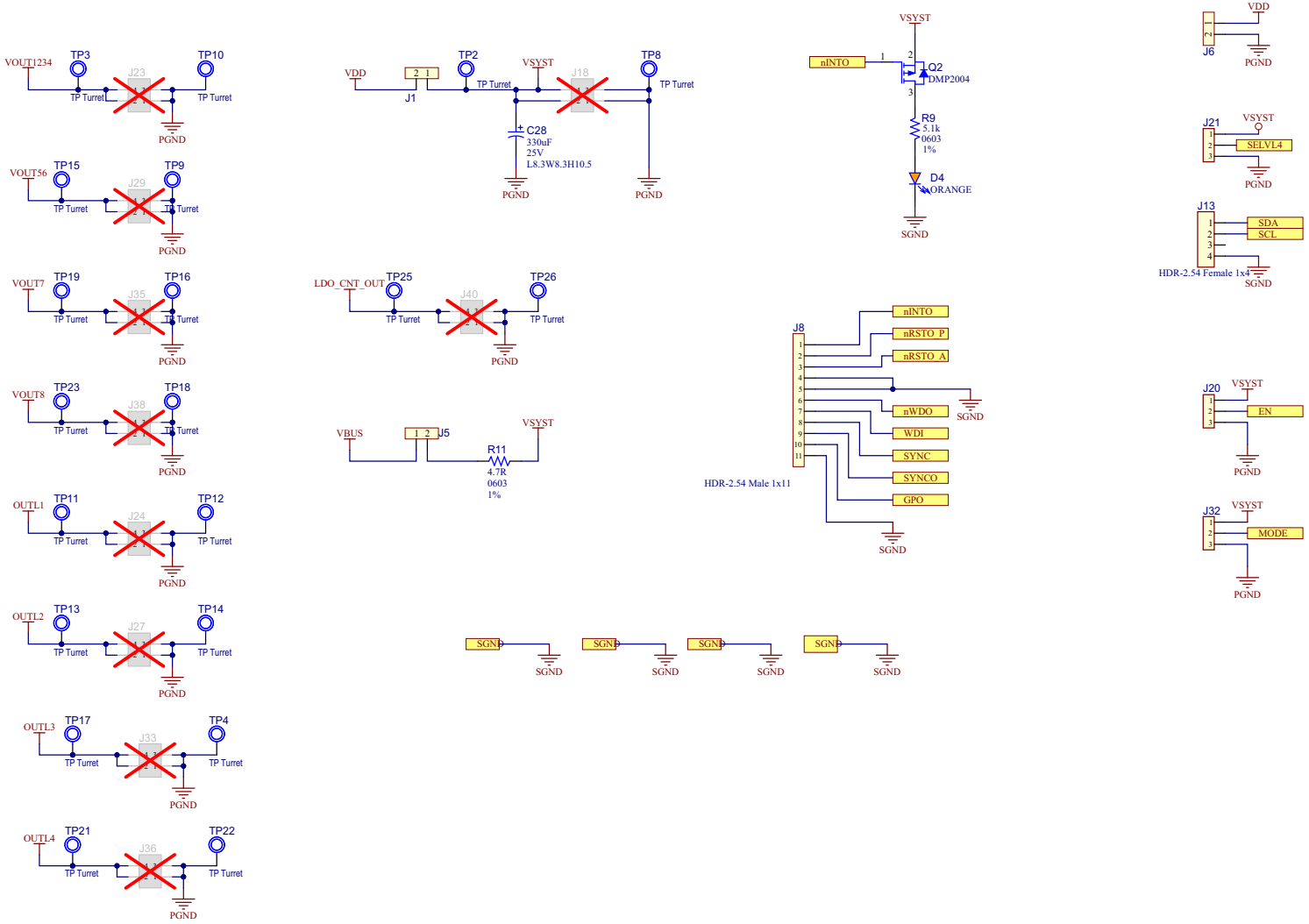
This appendix contains the following schematic and layouts for the MCP16701 (EV23P28A) Evaluation Board:

- Board – Schematic 1
- Board – Schematic 2
- Board – Top Silk
- Board – Top Copper and Silk
- Board – Top Copper
- Board – Mid-Layer 1
- Board – Mid-Layer 2
- Board – Bottom Copper
- Board – Bottom Copper and Silk
- Board – Bottom Silk

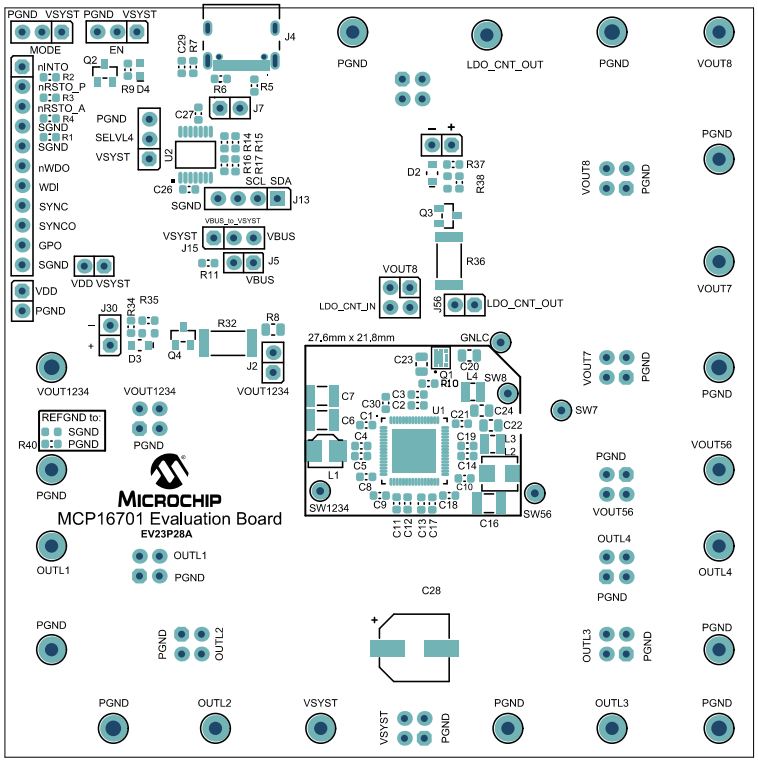
A.2 BOARD – SCHEMATIC 1



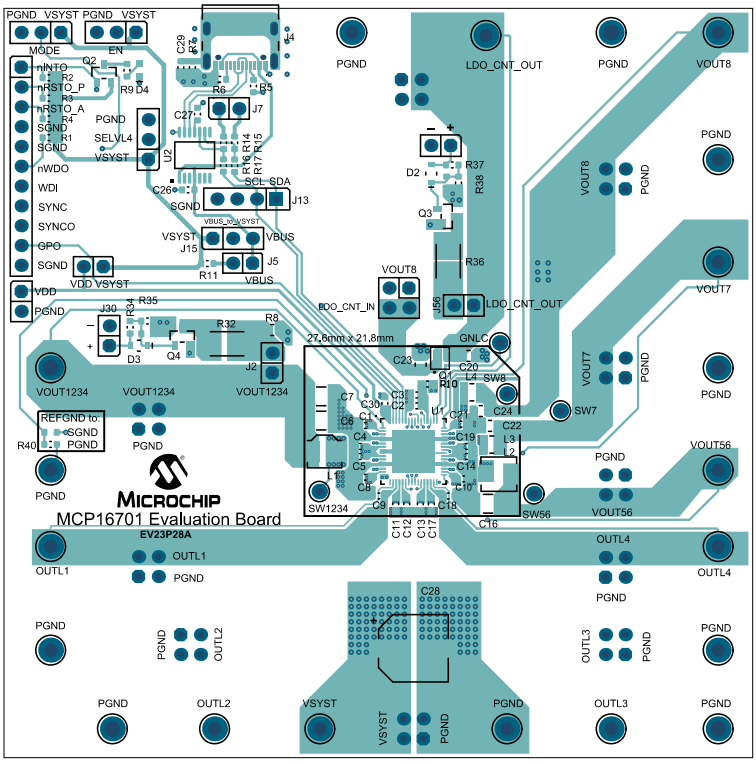
A.3 BOARD – SCHEMATIC 2



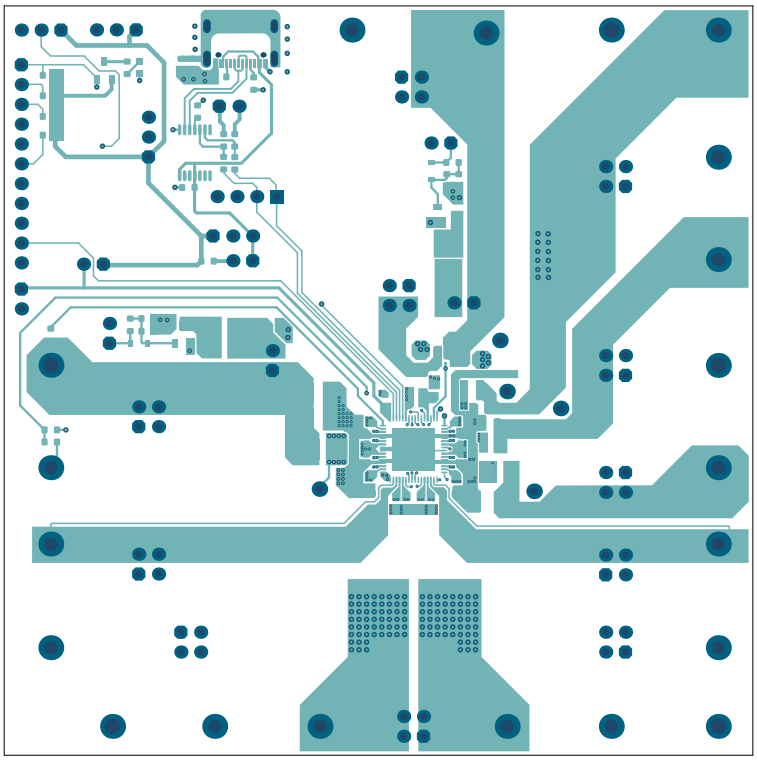
A.4 BOARD – TOP SILK



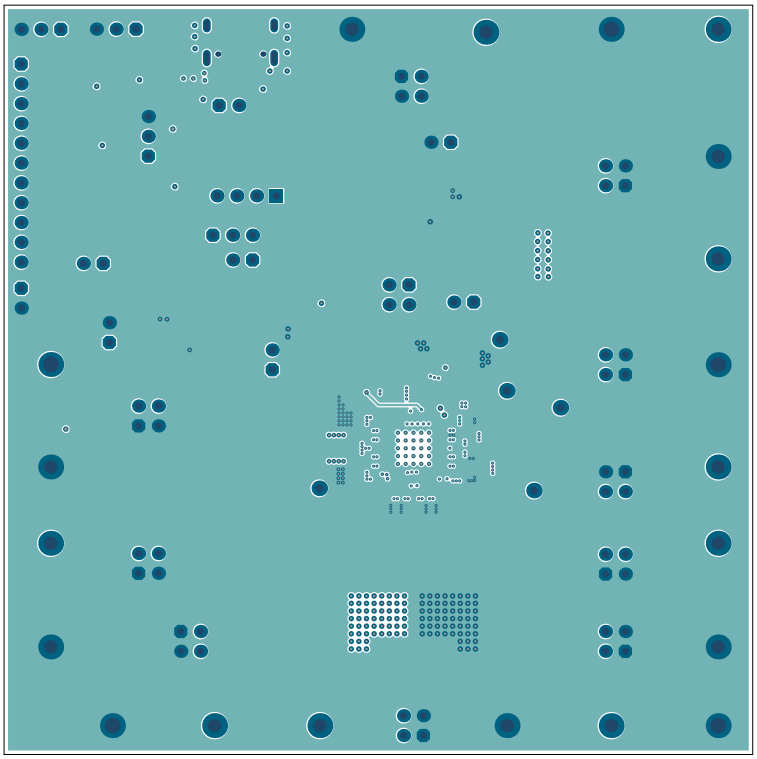
A.5 BOARD – TOP COPPER AND SILK



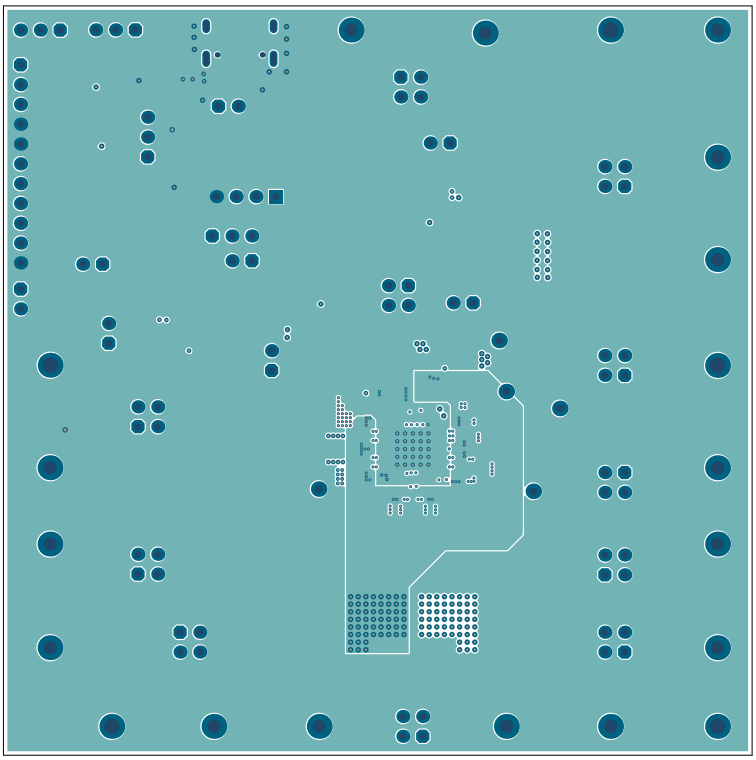
A.6 BOARD – TOP COPPER



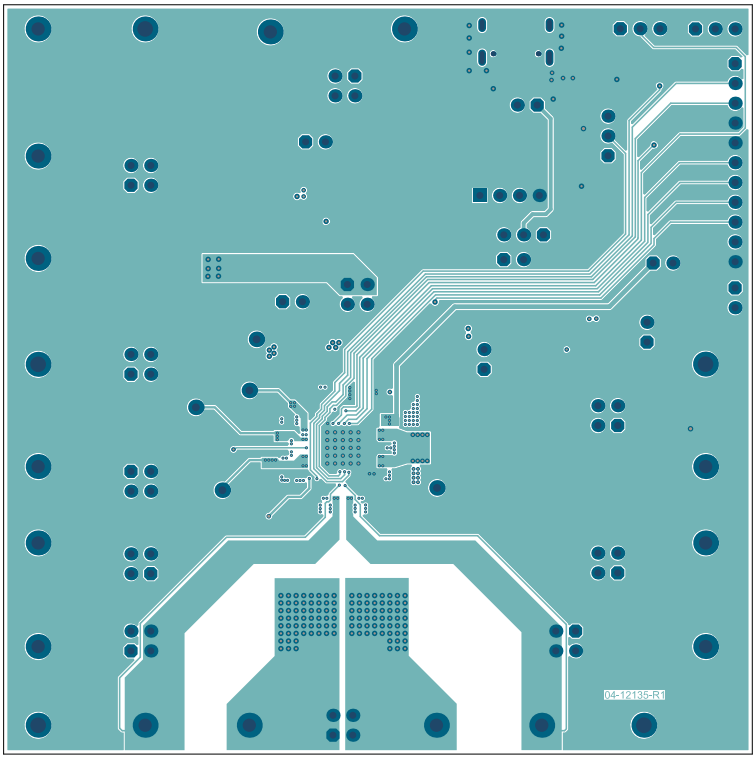
A.7 BOARD – MID-LAYER 1



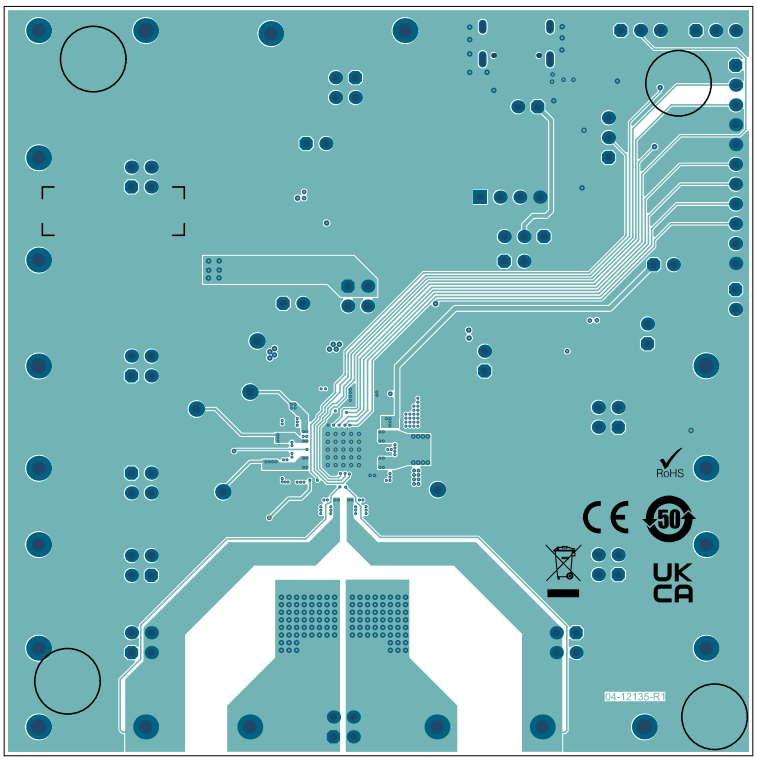
A.8 BOARD – MID-LAYER 2



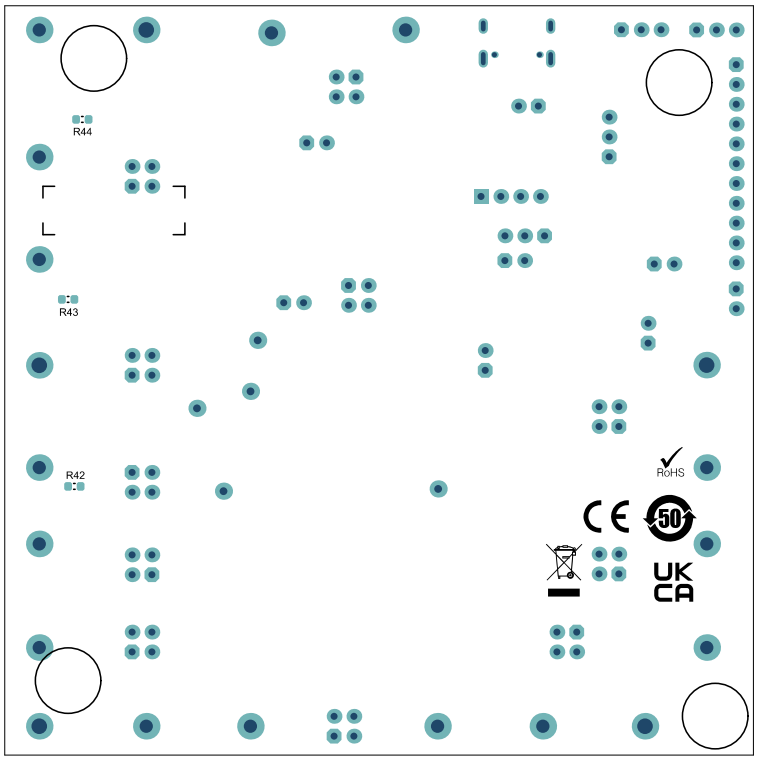
A.9 BOARD – BOTTOM COPPER



A.10 BOARD – BOTTOM COPPER AND SILK



A.11 BOARD – BOTTOM SILK



NOTES:

Appendix B. Bill of Materials (BOM)

TABLE B-1: BILL OF MATERIALS (BOM)

Qty.	Reference	Description	Manufacturer	Part Number
14	C1, C4, C5, C8, C9, C10, C11, C12, C13, C14, C17, C18, C19, C21	Ceramic Capacitor, 4.7 µF, 10V, 10%, X7S, SMD, 0603	TDK Corporation	C1608X7S1A475K080AC
6	C2, C3, C26, C27, C29, C30	Ceramic Capacitor, 1 µF, 25V, 10%, X7S, SMD, 0603	TDK Corporation	C1608X7R1E105K080AB
3	C6, C7, C16	Ceramic Capacitor, 47 µF, 6.3V, 20%, X7S, SMD, 1210	TDK Corporation	C3225X7S0J476M250AC
4	C20, C22, C23, C24	Ceramic Capacitor, 22 µF, 10V, 20%, X7S, SMD, 0805	TDK Corporation	C2012X7S1A226M125AC
1	C28	Aluminum Capacitor, 330 µF, 25V, 20%, SMD, L8.3W8.3H,10.5, AEC-Q200	Wurth Elektronik	865080453014
2	D2, D3	Diode Rectifier, 1.25V, 150 mA, 75V, SOD-323	Diodes Incorporated®	1N4148WS-7-F
1	D4	Diode LED, Orange, 2V, 20 mA, 90 mcd, Clear, SMD, 0603	Lite-On®, Inc.	LTST-C191KFKT
8	J1, J2, J5, J6, J7, J30, J56, J58	Connector Header, 2.54, Male, 1x2, Gold, 5.84 MH, TH, Vertical	FCI	77311-118-02LF
1	J3	Connector Header, 2.54, Male, 2x2, Gold, 5.84 MH, TH, Vertical	Wurth Elektronik	61300421121
1	J4	Connector, USB, 2.0, Type-C, Female, SMD/TH, R/A	GCT	USB4105-GF-A
1	J8	Connector Header, 2.54, Male 1x11, Gold 5.84MH, TH, Vertical	Sullins Connector Solutions	PBC11SAAN
1	J13	Connector Header, 2.54, Female, 1x4, Gold, TH, Vertical	Samtec, Inc.	SSW-104-01-G-S
4	J15, J20, J21, J32	Connector Header, 2.54, Male 1x3 Tin, 5.84MH, TH, Vertical	Samtec, Inc.	TSW-103-07-T-S
1	L1	Inductor, 470 nH, 8.7A, 20%, SMD, L4.4W4.1H2.0	TDK Corporation	SPM4020T-R47M-LR
1	L2	Inductor, 1 µH, 8A, 20%, SMD, L4.2W4H3.0	TDK Corporation	SPM4030T-1R0M
2	L3, L4	Inductor, 1.5 µH, 3.5A, 20%, SMD, 1008	Murata Electronics North America, Inc.	DFE252012P-1R5M=P2
1	Q1	Transistor FET, N-CH, 20V, 22A, 3.5W, (Ta)PowerPAK SC-70-6	Vishay Siliconix	SIAA02DJ-T1-GE3
2	Q2	Transistor FET, P-CH, 20V, 0.6A, 0.9R, 0.55W, SOT-23-3	Diodes Incorporated	DMP2004K-7

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

TABLE B-1: BILL OF MATERIALS (BOM) (CONTINUED)

Qty.	Reference	Description	Manufacturer	Part Number
2	Q3, Q4	Transistor, MOSFET, N-CH, 20V, 6A, 800mW, SOT23-3	Diodes Incorporated	DMN2040U-13
4	R1, R2, R3, R4	Resistor, TKF, 47k, 1%, 1/4W, SMD, 0603	Vishay	CRCW060347K0FKEAHP
3	R5, R6, R9	Resistor, TKF, 5.1k, 1%, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3EKF5101V
1	R7	Resistor, TKF, 330R, 1%, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3EKF3300V
1	R8	Resistor, TKF, 33R, 1%, 1/8W, SMD, 0805, AEC-Q200	Vishay	CRCW080533R0FKEA
4	R10, R16, R17, R40	Resistor, TKF, 0R, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3GSY0R00V
1	R11	Resistor, TKF, 4.7R, 1%, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3RQF4R7V
2	R14, R15	Resistor, TKF, 2.2k, 1%, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3EKF2201V
1	R32	Resistor, TKF, 0.33R, 1%, 1W, SMD, 2512	Vishay	WSL2512R3300FEA
2	R34, R37	Resistor, TKF, 1k, 5%, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3GEYJ102V
2	R35, R38	Resistor, TKF, 20k, 5%, 1/10W, SMD, 0603	Panasonic - ECG	ERJ-3GSYJ203
1	R36	Resistor, TKF, 2R, 1%, 2W, SMD, 2512	Bourns®, Inc.	CRM2512-FX-2R00ELF
5	TP1, TP5, TP6, TP7, TP27	Miscellaneous, Test Point, Multi Purpose, Miniature, White	Keystone® Electronics Corp.	5002
20	TP2, TP3, TP4, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP21, TP22, TP23, TP25, TP26	Connector, TP, PIN, Tin, TH	Harwin Plc.	H2121-01
1	U1	Analog PMIC Switcher, Buck, ADJ, VQFN-64	Microchip Technology Inc.	MCP16701
1	U2	Interface USB, I^2C, UART, TSSOP-14	Microchip Technology Inc.	MCP2221-I/ST
1	PCB1	MCP16701 (EV23P28A) Evaluation Board – Printed Circuit Board	Microchip Technology Inc.	04-12135-R1

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

TABLE B-2: BILL OF MATERIALS (BOM) – MECHANICAL PARTS

Qty.	Reference	Description	Manufacturer	Part Number
5	JP1, JP2, JP3, JP4, JP5	Mechanical, HW Jumper, 2.54 mm, 1 x 2	FCI	63429-202LF
1	LABEL1	Label, PCBA, 18 x 6 mm, Datamatrix Assy# /Rev/Serial/ Date	ACT Logimark AS	505462

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

TABLE B-2: BILL OF MATERIALS (BOM) – MECHANICAL PARTS (CONTINUED)

Qty.	Reference	Description	Manufacturer	Part Number
4	PAD1, PAD2, PAD3, PAD4	Mechanical, HW Rubber Pad Cylindrical flat top D8H2.8 Black	3M	SJ5076BLACK

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

TABLE B-3: BILL OF MATERIALS (BOM) – DO NOT POPULATE PARTS

Qty.	Reference	Description	Manufacturer	Part Number
0	C25, C31	Ceramic Capacitor, 2.2 µF, 10V, 10%, X7R, SMD, 0603	Murata Electronics North America, Inc.	GRM188R71A225KE15D
0	J18, J23, J24, J27, J29, J33, J35, J36, J38, J40	Connector Header, 2.54, Male, 2x2, Gold, 5.84 MH, TH, Vertical	Samtec, Inc.	HTSW-102-07-G-D
0	R41	Resistor, TKF, 0R, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3GSY0R00V

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.