LAN9372/3/4

8-Port AVB/TSN Gigabit Ethernet Switch with Integrated 100BASE-T1 PHYs

Highlights

- Up to 6x 100BASE-T1 ports (5x for LAN9372/3, 6x for LAN9374)
- 1x 100BASE-TX port (LAN9372 only)
- 2x RGMII/RMII/MII ports
- 1x SGMII port (LAN9373 only)
- Cascade mode for higher port count
- Enhanced EMC performance
- Full AVB Audio Video Bridging
- Time Sensitive Networking Support
- High Available Seamless Redundancy (HSR)
- OPEN Alliance TC10 Sleep/Wakeup
- Over-temperature and under-voltage detection
- LinkMD®+ enhanced cable diagnostics
- FlexPWR® technology power management
- Small-footprint 128-pin TQFP (14 x 14 mm) package
- AEC-Q100 automotive product qualification
- Grade 2 Automotive temperature (-40°C to +105°C)

Target Applications

- Advanced Driver-Assistance Systems (ADAS)
- Infotainment
- Telematics & Smart Antennas
- In-Vehicle Backbone
- Gateways

Features

- Switch Management Capabilities
  - Compliant to OPEN TC11 switch requirements
  - 1K MAC table
  - IEEE 802.1Q VLAN support
  - AVB and TSN hardware support:
    -IEEE 802.1AS time synchronization
    -IEEE 1588v2 PTP and clock synchronization
    -IEEE 802.Qav traffic shaping
    -IEEE 802.1Qbv (TSN) time-aware scheduler
    -IEEE 802.1Qci (TSN) ingress filtering and policing
  - 8 shapers per port, one for each queue
  - Smart low-latency cut-through forwarding mode
  - High Availability Seamless Redundancy (HSR)
  - Deep Packet Inspection (DPI) using TCAM
    -TCAM classification of Layers 2,3,4 and beyond
  - SPI or in-band host processor access
  - Wire speed - non-blocking
- Up to 6x Integrated 100BASE-T1 Ethernet PHYs (5x for LAN9372/3, 6x for LAN9374)
  - Compliant with IEEE 802.3bw-2015
  - 100Mbps over single balanced twisted pair cable
  - Extended cable reach >15m
  - On-chip filtering & termination for balanced UTP cable
- 1x Integrated 100BASE-TX/10BASE-T Port (LAN9372 only)
  - Compliant with IEEE 802.3/802.3u
  - Auto-negotiation and Auto-MDI/MDI-X support
  - On-chip termination resistors and internal biasing
- Up to 3x Configurable External MAC Ports
  - Reduced Gigabit Media Independent Interface (RGMII)
  - Reduced Media Independent Interface (RMII) with 50MHz reference clock input/output option
  - Media Independent Interface (MII) in PHY/MAC mode
  - Serial Gigabit Media Independent Interface (SGMII) (LAN9373 only)
- IEEE 1588v2 PTP and Clock Synchronization
  - Transparent Clock (TC) with auto correction update
  - Leader and Follower Ordinary Clock (OC) support
  - End-to-end (E2E) or peer-to-peer (P2P)
  - PTP multicast and unicast message support
  - PTP message transport over IPv4/v6 and IEEE 802.3
  - IEEE 1588v2 PTP packet filtering
  - Time Aware Precision GPIO
- Advanced Diagnostics & Security
  - OPEN Alliance (TC1) advanced diagnostics compliant
  - LinkMD®+ cable diagnostic capabilities
    -Determines cable opens/shorts/length (TX & T1)
    -Signal Quality Indicator (SQI) with MSE, peak values, and peak/threshold interrupt (T1)
  - Self-test packet generator/detector
    -Single burst and continuous traffic stream support
    -Automatic L2 and configurable L3 and L4 headers
  - Loopback modes (per IEEE 802.3bw)
  - Extended MIB performance counters
  - Deep packet inspection support for every packet/port
  - IEEE 802.1AR (802.1x) port and MAC authentication
  - IEEE 802.1Qci per stream ingress filtering & policing
- EtherGREEN™ Energy Efficiency
  - Low-power 100BASE-T1 PHY technology
  - OPEN Alliance TC10 sleep/wakeup (partial networking)
  - Non-TC10 link partner energy detect wake-up support
  - Ultra-Deep-Sleep power down
- Low RF Emissions
  - Integrated transmission filtering
  - xMII data and 125MHz clock include programmable slew rate control
  - OPEN Alliance (TC6) RGMII EPL compliant
  - Exceeds OPEN Alliance Transceiver EMC Test Specification

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Table of Contents

1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
1000BASE-T	1 Gbps Ethernet over twisted pair, IEEE 802.3 compliant
100BASE-T1	100 Mbps Ethernet over single balanced twisted pair, IEEE 802.3bw compliant
100BASE-TX	100 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-T	10 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
ACL	Access Control List
ADAS	Advanced Driver Assistance Systems
ADC	Analog-to-Digital Converter
AFE	Analog Front End
AN, ANEG	Auto-Negotiation
ARP	Address Resolution Protocol
AVB	Audio Video Bridging
BELT	Best Effort Latency Tolerance
BYTE	8-bits
CRC	Cyclic Redundancy Check
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Register
DA	Destination Address
DoD	Delay on Destination
DoS	Delay on Source
DWORD	32-bits
E2E	End to End
EC	Embedded Controller
EEE	Energy Efficient Ethernet
EOF	End of Frame
FCS	Frame Check Sequence
FID	Filter ID
FIFO	First In First Out buffer
FSM	Finite State Machine
FW	Firmware
GMII	Gigabit Media Independent Interface
GPIO	General Purpose I/O
gPTP	Generic Precision Time Protocol
HOST	External system (Includes processor, application software, etc.)

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
HSR	High-availability Seamless Redundancy
HW	Hardware. Refers to function implemented by digital logic.
IEEE	Institute of Electrical and Electronic Engineers
IGMP	Internet Group Management Protocol
IP	Internet Protocol
IPV	Internal Priority Value
ISO	International Standards Organization
ITU	International Telecommunications Union
L2	Layer 2
L3	Layer 3
L4	Layer 4
LDO	Linear Drop-Out Regulator
LIDAR	Light Detection and Ranging
LPM	Link Power Management
lsb	Least Significant Bit
LSB	Least Significant Byte
MAC	Media Access Controller
MDI	Medium Dependent Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MSTP	Multiple Spanning Tree Protocol
N/A	Not Applicable
Nonce	An arbitrary number that is used only once
NoQ	Number of Queues
NumP	Number of Ports
OC	Ordinary Clock
OTP	One Time Programmable
P2P	Peer to Peer
PCS	Physical Coding Sublayer
PIO	Programmable Input and Output
PLL	Phase Locked Loop
PMIC	Power Management IC
POR	Power on Reset.
PPS	Packets Per Second
PSFP	Per-Stream Filtering and Policing
PTF	Port to Forward

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
PTP	Precision Time Protocol
QoS	Quality of Service
QWORD	64-bits
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RMON	Remote Monitoring
RTC	Real Time Clock
SA	Source Address
SCSR	System Control and Status Registers
SDU	Service Data Unit
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame
SNMP	Simple Network Management Protocol
SOF	Start of Frame
STC	System Time Clock
TA	Turn-Around Time
TAS	Time Aware Scheduler
TC	Transparent Clock
TCP	Transport Control Protocol
TMII	Turbo Media Independent Interface
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UTP	Unshielded Twisted Pair
VLAN	Virtual Local Area Network
WORD	16-bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
VIS	Variable Schmitt-triggered input
VIS_VBAT	Variable Schmitt-triggered input in VBAT power domain
IPU	Input with internal pull-up (58 kΩ ±30%)
VO8	Variable Output with 8 mA sink and 8 mA source
VO_VBAT	Variable Output in VBAT power domain
A	Analog
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power
OD	Open-drain output
SGMII-I	SGMII Input
SGMII-O	SGMII Output
RGMII	RGMII Output
PU	70k (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.

Note: All digital input pins have an internal pull-up enabled during power-up/pin reset.

1.3 Reference Documents

1. *IEEE 802.3™-2015 IEEE Standard for Ethernet,*
   http://standards.ieee.org/about/get/802/802.3.html
2. *IEEE 802.3bw™-2015 IEEE Standard for Ethernet Amendment 1,*
   https://standards.ieee.org/findstds/standard/802.3bw-2015.html
3. *RMII Specification Revision 1.2,*
   http://ebook.pldworld.com/_eBook/-Telecommunications,Networks-/TCPIP/RMII/rmii_rev12.pdf
4. *Reduced Gigabit Media Independent Interface (RGMII) Specification Version 2.0,*
   https://web.archive.org/web/20160303171328/http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf
5. *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0*
   http://www.opensig.org//about/specifications/
6. *OPEN Alliance TC10 - Sleep/Wake-up Specification Version 2.0*
   http://www.opensig.org//about/specifications/

2.0 INTRODUCTION

2.1 General Description

The Microchip LAN9372/LAN9373/LAN9374 (LAN9372/3/4) is a scalable, compact and cost-effective, multi-Port AVB/TSN 100BASE-T1 Ethernet Switch based on the IEEE 802.3bw-2015 specification. The LAN9372/3/4 incorporates a layer-2+ managed high-performance Ethernet switch, up to six (five for the LAN9372/3, six for the LAN9374) 100BASE-T1 physical layer transceivers (PHYs), and two MAC ports with individually configurable RGMII/MII/RMII interfaces for direct connection to a host processor/controller, another Ethernet switch, or an Ethernet PHY transceiver. An additional IEEE 802.3/802.3u compliant 100BASE-TX port is provided (LAN9372 only) for applications where an integrated automotive OBD port is required. An additional MAC port with a SGMII interface is also provided (LAN9373 only) for direct connection to a host processor/controller, another Ethernet switch, or an Ethernet PHY transceiver. The LAN9372/3/4 is available in a Grade 2 Automotive (-40°C to +105°C) temperature range and is qualified to AEC-Q100 automotive use cases such as gateways, Automated Driver-Assistance Systems (ADAS), infotainment, telematics and in-vehicle networking.

The LAN9372/3/4 fully supports the IEEE family of Audio Video Bridging (AVB) standards, which provide high Quality of Service (QoS) for latency sensitive traffic streams over Ethernet. Hardware time-stamping and time-keeping features support IEEE 802.1AS (gPTP) and IEEE 1588v2 (PTP) time synchronization. All ports feature eight egress queues and an IEEE 802.1Qav credit based traffic shaper and time aware scheduler, as per the IEEE 802.1Qbv specification.

A host processor can access all LAN9372/3/4 registers for control over all PHY, MAC, and switch functions. Full register access is available via the integrated SMI and SPI interfaces, and by in-band management via any one of the data ports. PHY register access is provided by a MIIM interface. Flexible digital I/O voltage allows the MAC port to interface directly with a 1.8/2.5/3.3V host processor/controller/FPGA.

Additionally, a robust assortment of EtherGREEN™ energy efficiency features are provided, including Open Alliance TC10 sleep/wakeup partial networking, non-TC10 link partner energy detect wake-up, and ultra-deep-sleep power down.

Device specific features that do not pertain to the entire LAN9372/3/4 family are called out independently throughout this document. Table 2-1 provides a summary of the feature differences between members of the LAN937x device family:

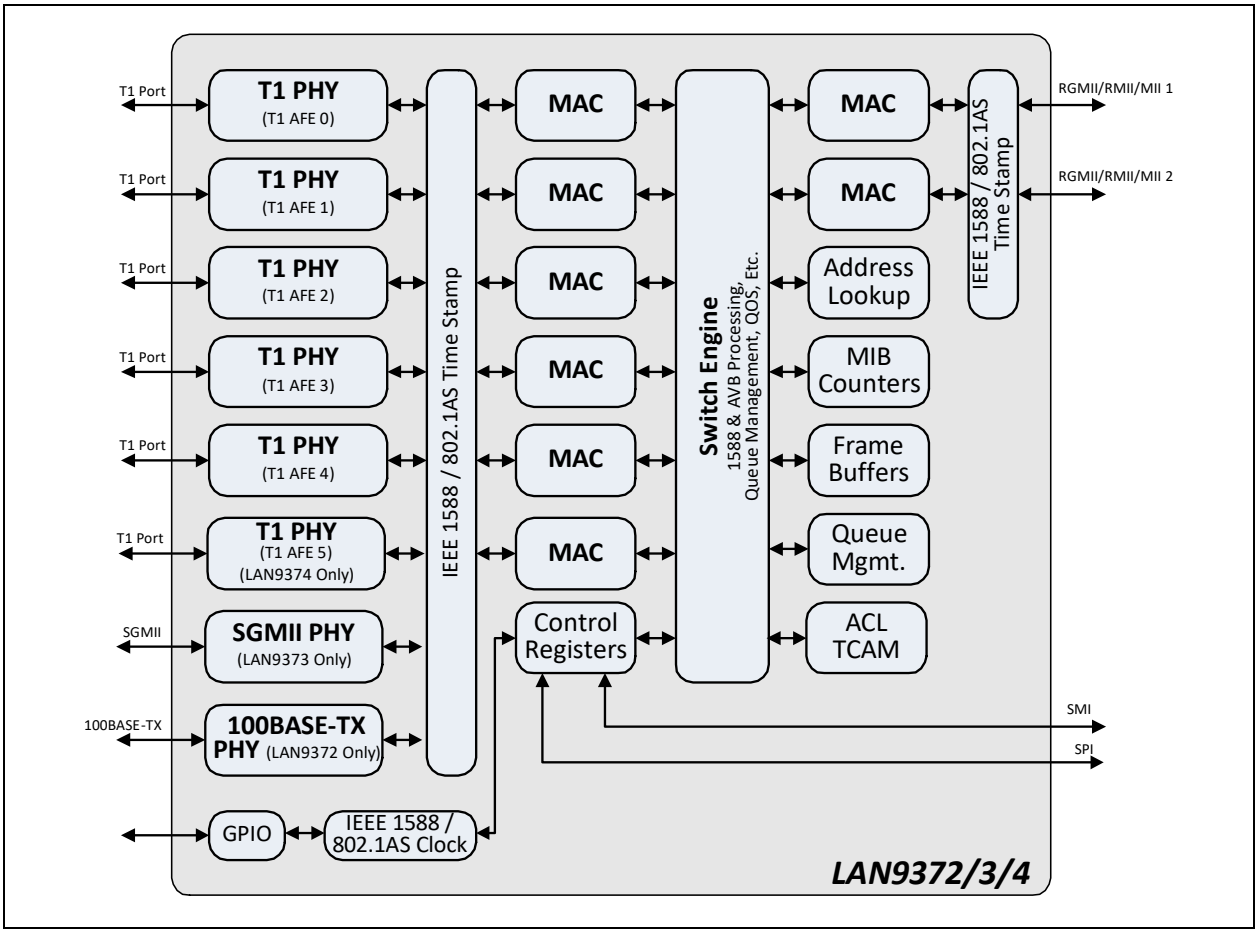
TABLE 2-1: LAN937X FAMILY FEATURE MATRIX

Part Number	Package	# of Integrated 100BASE-T1 PHYs	100BASE-TX Support	SGMII Support	RGMII/RMII/MII Ports	Full AVB Support	Time Sensitive Networking Support	OPEN Alliance TC10 Sleep/Wakeup Energy Efficiency	Cascade Mode Support	AEC-Q100 Qualification	Grade 2 Automotive Temp. (-40° to 105°C)
LAN9370	64-VQFN	4			1	X	X	X	X	X	X
LAN9371	128-TQFP	3	X		2	X	X	X	X	X	X
LAN9372	128-TQFP	5	X		2	X	X	X	X	X	X
LAN9373	128-TQFP	5		X	2	X	X	X	X	X	X
LAN9374	128-TQFP	6			2	X	X	X	X	X	X

Note: All LAN937x devices share a common software driver. All 128-TQFP LAN937x devices are pin compatible.

An internal block diagram of the LAN9372/3/4 is shown in Figure 2-1.

FIGURE 2-1: INTERNAL BLOCK DIAGRAM

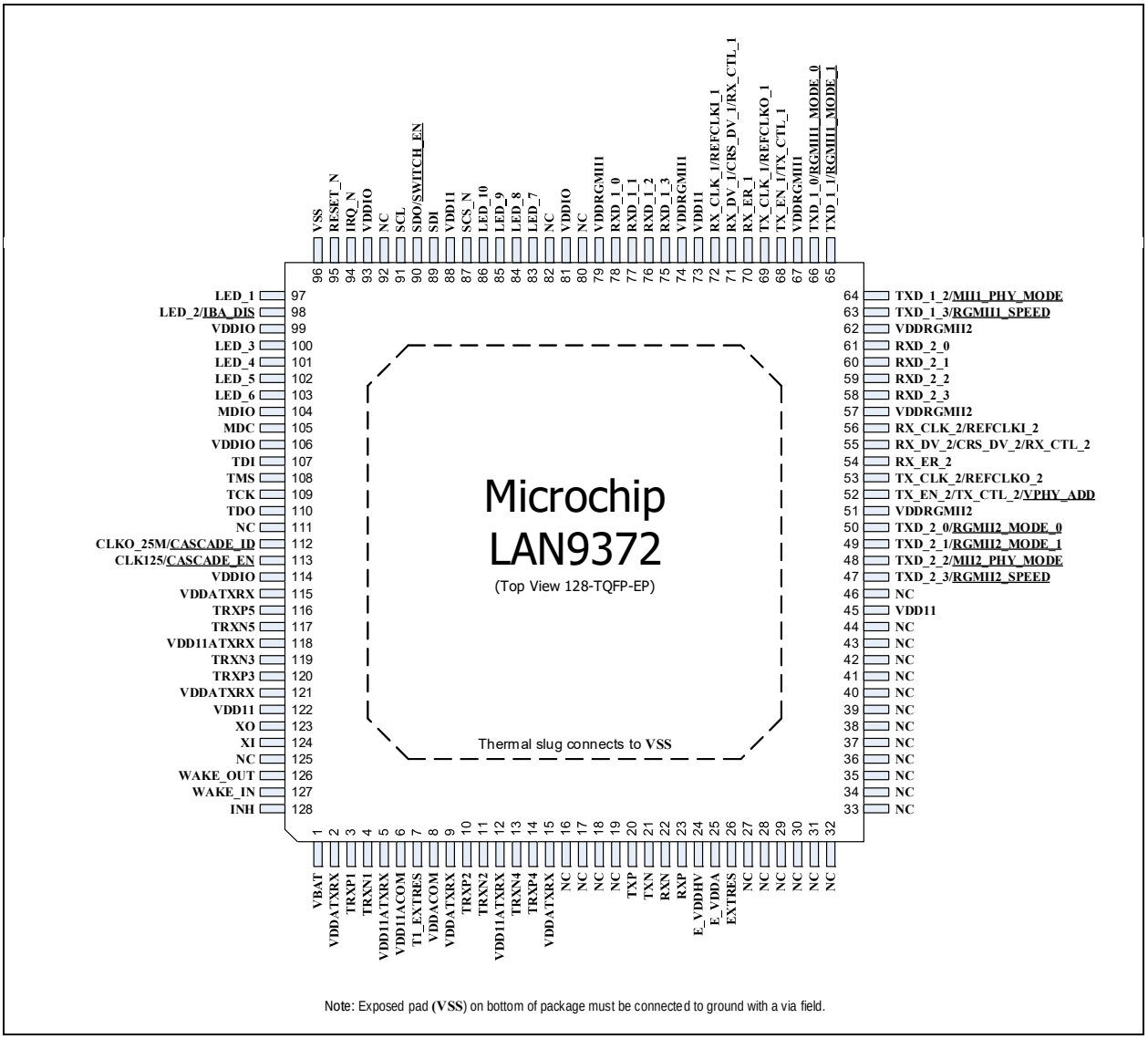


3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

3.1.1 LAN9372 PIN ASSIGNMENTS

FIGURE 3-1: LAN9372 PIN ASSIGNMENTS (TOP VIEW)



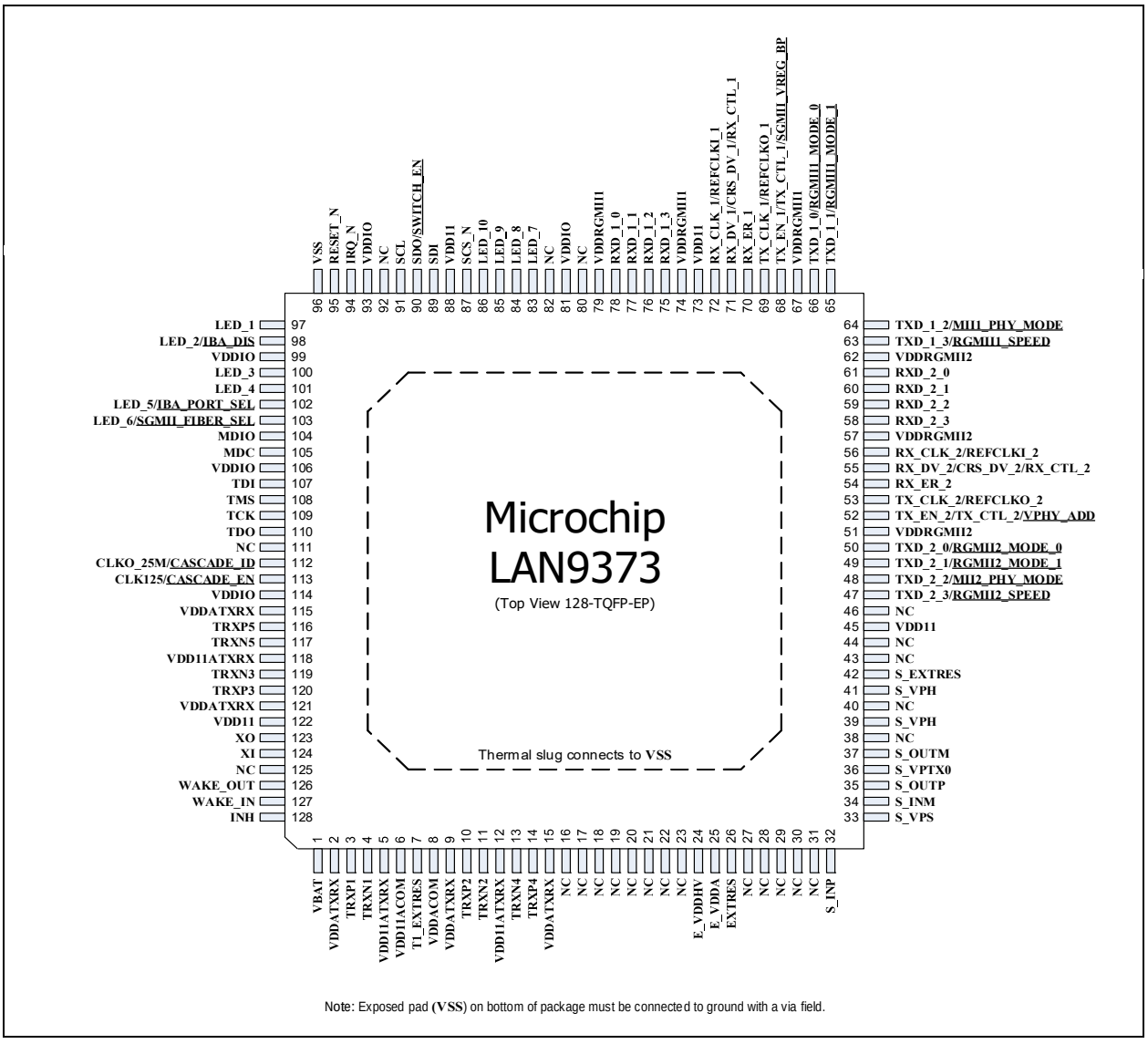
Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

TABLE 3-1: LAN9372 PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	VBAT	33	NC	65	TXD_1_1/ RGMII1_MODE_1	97	LED_1
2	VDDATXRX	34	NC	66	TXD_1_0/ RGMII1_MODE_0	98	LED_2/ IBA_DIS
3	TRXP1	35	NC	67	VDDRGMII1	99	VDDIO
4	TRXN1	36	NC	68	TX_EN_1/TX_CTL_1	100	LED_3
5	VDD11ATXRX	37	NC	69	TX_CLK_1/ REFCLKO_1	101	LED_4
6	VDD11ACOM	38	NC	70	RX_ER_1	102	LED_5
7	T1_EXTRES	39	NC	71	RX_DV_1/CRS_DV_1/ RX_CTL_1	103	LED_6
8	VDDACOM	40	NC	72	RXCLK_1/REFCLKI_1	104	MDIO
9	VDDATXRX	41	NC	73	VDD11	105	MDC
10	TRXP2	42	NC	74	VDDRGMII1	106	VDDIO
11	TRXN2	43	NC	75	RXD_1_3	107	TDI
12	VDD11ATXRX	44	NC	76	RXD_1_2	108	TMS
13	TRXN4	45	VDD11	77	RXD_1_1	109	TCK
14	TRXP4	46	NC	78	RXD_1_0	110	TDO
15	VDDATXRX	47	TXD_2_3/ RGMII2_SPEED	79	VDDRGMII1	111	NC
16	NC	48	TXD_2_2/ MII2_PHY_MODE	80	NC	112	CLKO_25M/ CASCADE_ID
17	NC	49	TXD_2_1/ RGMII2_MODE_1	81	VDDIO	113	CLK125/ CASCADE_EN
18	NC	50	TXD_2_0/ RGMII2_MODE_0	82	NC	114	VDDIO
19	NC	51	VDDRGMII2	83	LED_7	115	VDDATXRX
20	TXP	52	TX_EN_2/TX_CTL_2/ VPHY_ADD	84	LED_8	116	TRXP5
21	TXN	53	TX_CLK_2/ REFCLKO_2	85	LED_9	117	TRXN5
22	RXN	54	RX_ER_2	86	LED_10	118	VDD11ATXRX
23	RXP	55	RX_DV_2/CRS_DV_2/ RX_CTL_2	87	SCS_N	119	TRXN3
24	E_VDDHV	56	RX_CLK_2/REFCLKI_2	88	VDD11	120	TRXP3
25	E_VDDA	57	VDDRGMII2	89	SDI	121	VDDATXRX
26	EXTRES	58	RXD_2_3	90	SDO/ SWITCH_EN	122	VDD11
27	NC	59	RXD_2_2	91	SCL	123	XO
28	NC	60	RXD_2_1	92	NC	124	XI
29	NC	61	RXD_2_0	93	VDDIO	125	NC
30	NC	62	VDDRGMII2	94	IRQ_N	126	WAKE_OUT
31	NC	63	TXD_1_3/ RGMII1_SPEED	95	RESET_N	127	WAKE_IN
32	NC	64	TXD_1_2/ MII1_PHY_MODE	96	VSS	128	INH
Exposed Pad Must be Connected to VSS							

3.1.2 LAN9373 PIN ASSIGNMENTS

FIGURE 3-2: LAN9373 PIN ASSIGNMENTS (TOP VIEW)



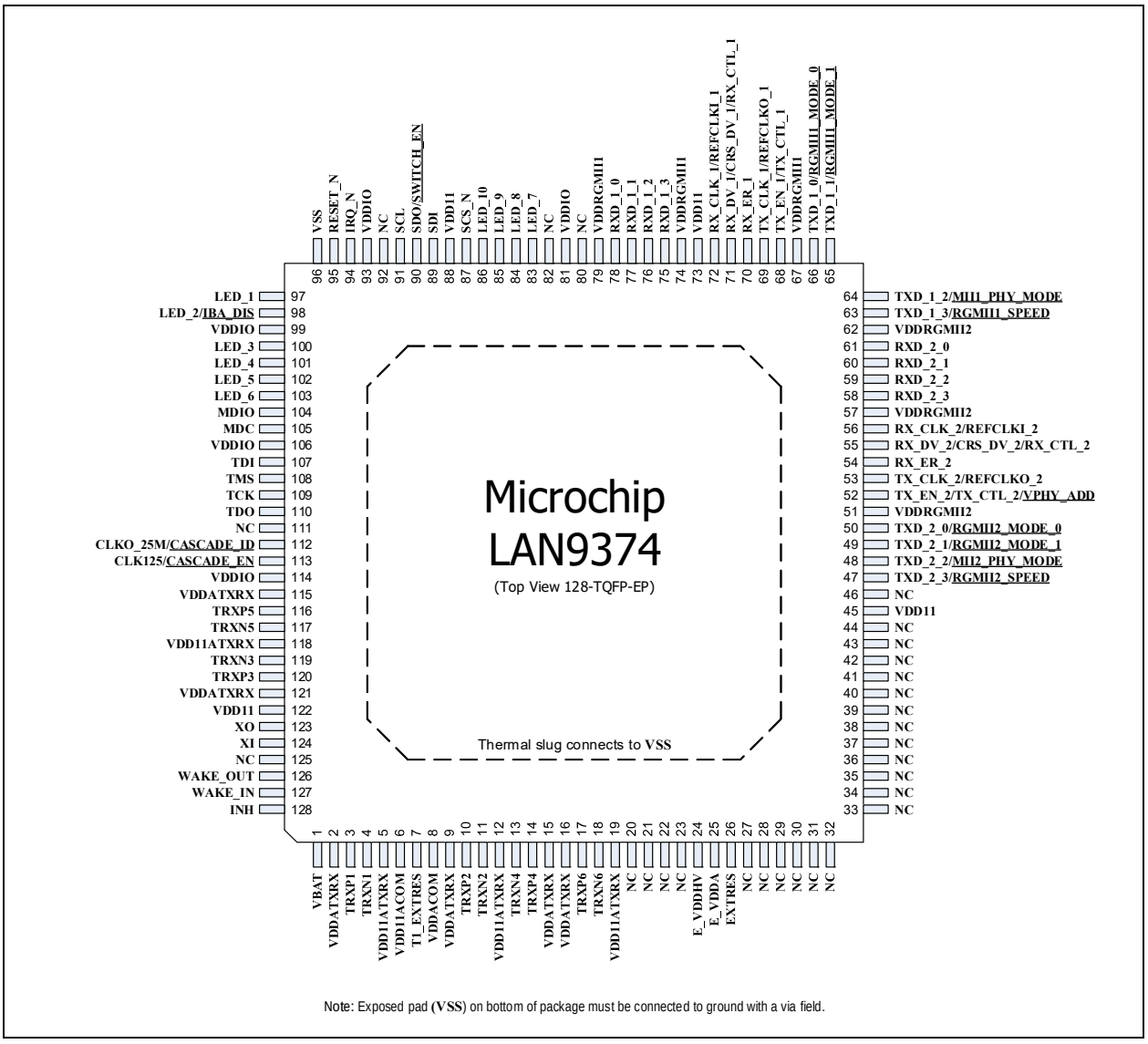
Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

TABLE 3-2: LAN9373 PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	VBAT	33	S_VPS	65	TXD_1_1/ RGMII1_MODE_1	97	LED_1
2	VDDATXRX	34	S_INM	66	TXD_1_0/ RGMII1_MODE_0	98	LED_2/ IBA_DIS
3	TRXP1	35	S_OUTP	67	VDDRGMII1	99	VDDIO
4	TRXN1	36	S_VPTX0	68	TX_EN_1/TX_CTL_1/ SGMII_VREG_BP	100	LED_3
5	VDD11ATXRX	37	S_OUTM	69	TX_CLK_1/ REFCLKO_1	101	LED_4
6	VDD11ACOM	38	NC	70	RX_ER_1	102	LED_5/ IBA_PORT_SEL
7	T1_EXTRES	39	S_VPH	71	RX_DV_1/CRS_DV_1/ RX_CTL_1	103	LED_6/ SGMII_FIBER_SEL
8	VDDACOM	40	NC	72	RXCLK_1/REFCLKI_1	104	MDIO
9	VDDATXRX	41	S_VPH	73	VDD11	105	MDC
10	TRXP2	42	S_EXTRES	74	VDDRGMII1	106	VDDIO
11	TRXN2	43	NC	75	RXD_1_3	107	TDI
12	VDD11ATXRX	44	NC	76	RXD_1_2	108	TMS
13	TRXN4	45	VDD11	77	RXD_1_1	109	TCK
14	TRXP4	46	NC	78	RXD_1_0	110	TDO
15	VDDATXRX	47	TXD_2_3/ RGMII2_SPEED	79	VDDRGMII1	111	NC
16	NC	48	TXD_2_2/ MII2_PHY_MODE	80	NC	112	CLKO_25M/ CASCADE_ID
17	NC	49	TXD_2_1/ RGMII2_MODE_1	81	VDDIO	113	CLK125/ CASCADE_EN
18	NC	50	TXD_2_0/ RGMII2_MODE_0	82	NC	114	VDDIO
19	NC	51	VDDRGMII2	83	LED_7	115	VDDATXRX
20	NC	52	TX_EN_2/TX_CTL_2/ VPHY_ADD	84	LED_8	116	TRXP5
21	NC	53	TX_CLK_2/ REFCLKO_2	85	LED_9	117	TRXN5
22	NC	54	RX_ER_2	86	LED_10	118	VDD11ATXRX
23	NC	55	RX_DV_2/CRS_DV_2/ RX_CTL_2	87	SCS_N	119	TRXN3
24	E_VDDHV	56	RX_CLK_2/REFCLKI_2	88	VDD11	120	TRXP3
25	E_VDDA	57	VDDRGMII2	89	SDI	121	VDDATXRX
26	EXTRES	58	RXD_2_3	90	SDO/ SWITCH_EN	122	VDD11
27	NC	59	RXD_2_2	91	SCL	123	XO
28	NC	60	RXD_2_1	92	NC	124	XI
29	NC	61	RXD_2_0	93	VDDIO	125	NC
30	NC	62	VDDRGMII2	94	IRQ_N	126	WAKE_OUT
31	NC	63	TXD_1_3/ RGMII1_SPEED	95	RESET_N	127	WAKE_IN
32	S_INP	64	TXD_1_2/ MII1_PHY_MODE	96	VSS	128	INH
Exposed Pad Must be Connected to VSS							

3.1.3 LAN9374 PIN ASSIGNMENTS

FIGURE 3-3: LAN9374 PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

TABLE 3-3: LAN9374 PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	VBAT	33	NC	65	TXD_1_1/ RGMII1_MODE_1	97	LED_1
2	VDDATXRX	34	NC	66	TXD_1_0/ RGMII1_MODE_0	98	LED_2/ IBA_DIS
3	TRXP1	35	NC	67	VDDRGMII1	99	VDDIO
4	TRXN1	36	NC	68	TX_EN_1/TX_CTL_1	100	LED_3
5	VDD11ATXRX	37	NC	69	TX_CLK_1/ REFCLKO_1	101	LED_4
6	VDD11ACOM	38	NC	70	RX_ER_1	102	LED_5
7	T1_EXTRES	39	NC	71	RX_DV_1/CRS_DV_1/ RX_CTL_1	103	LED_6
8	VDDACOM	40	NC	72	RXCLK_1/REFCLKI_1	104	MDIO
9	VDDATXRX	41	NC	73	VDD11	105	MDC
10	TRXP2	42	NC	74	VDDRGMII1	106	VDDIO
11	TRXN2	43	NC	75	RXD_1_3	107	TDI
12	VDD11ATXRX	44	NC	76	RXD_1_2	108	TMS
13	TRXN4	45	VDD11	77	RXD_1_1	109	TCK
14	TRXP4	46	NC	78	RXD_1_0	110	TDO
15	VDDATXRX	47	TXD_2_3/ RGMII2_SPEED	79	VDDRGMII1	111	NC
16	VDDATXRX	48	TXD_2_2/ MII2_PHY_MODE	80	NC	112	CLKO_25M/ CASCADE_ID
17	TRXP6	49	TXD_2_1/ RGMII2_MODE_1	81	VDDIO	113	CLK125/ CASCADE_EN
18	TRXN6	50	TXD_2_0/ RGMII2_MODE_0	82	NC	114	VDDIO
19	VDD11ATXRX	51	VDDRGMII2	83	LED_7	115	VDDATXRX
20	NC	52	TX_EN_2/TX_CTL_2/ VPHY_ADD	84	LED_8	116	TRXP5
21	NC	53	TX_CLK_2/ REFCLKO_2	85	LED_9	117	TRXN5
22	NC	54	RX_ER_2	86	LED_10	118	VDD11ATXRX
23	NC	55	RX_DV_2/CRS_DV_2/ RX_CTL_2	87	SCS_N	119	TRXN3
24	E_VDDHV	56	RX_CLK_2/REFCLKI_2	88	VDD11	120	TRXP3
25	E_VDDA	57	VDDRGMII2	89	SDI	121	VDDATXRX
26	EXTRES	58	RXD_2_3	90	SDO/ SWITCH_EN	122	VDD11
27	NC	59	RXD_2_2	91	SCL	123	XO
28	NC	60	RXD_2_1	92	NC	124	XI
29	NC	61	RXD_2_0	93	VDDIO	125	NC
30	NC	62	VDDRGMII2	94	IRQ_N	126	WAKE_OUT
31	NC	63	TXD_1_3/ RGMII1_SPEED	95	RESET_N	127	WAKE_IN
32	NC	64	TXD_1_2/ MII1_PHY_MODE	96	VSS	128	INH
Exposed Pad Must be Connected to VSS							

3.2 Pin Descriptions

This section contains descriptions of the various LAN9372/3/4 pins. Buffer type definitions are detailed in Section 1.2, "Buffer Types".

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are identified by an underlined symbol name and are latched upon Power-On Reset (POR) and pin reset (**RESET_N**). Configuration straps include internal pull-up/pull-down resistors in order to prevent the signal from floating when unconnected.

Note:	Signals that function as configuration straps must be augmented with an external pull-up or pull-down resistor when connected to a load to ensure they reach the required voltage level prior to latching.

TABLE 3-4: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
100BASE-T1 Ethernet PHY Ports			
Port 6-1 100BASE-T1 PHY TX/RX Positive	**TRXP[6:1]**	A	Port 6-1 100BASE-T1 PHY transmit/receive positive. **Note:** Port 6 available only in the LAN9374.
Port 6-1 100BASE-T1 PHY TX/RX Negative	**TRXN[6:1]**	A	Port 6-1 100BASE-T1 PHY transmit/receive negative. **Note:** Port 6 available only in the LAN9374.
100BASE-T1 Reference Resistor	**T1_EXTRES**	A	Reference resistor connection pin for the T1 PHY common block. For proper operation, this pin must be connected to **VSS** through a 6.49kΩ 0.1% resistor.
100BASE-TX Ethernet PHY Port (LAN9372 Only)			
100BASE-TX Ethernet Receive Data Positive	**RXP**	A	100BASE-TX Ethernet Receive Data Positive.
100BASE-TX Ethernet Receive Data Negative	**RXN**	A	100BASE-TX Ethernet Receive Data Negative.
100BASE-TX Ethernet Transmit Data Positive	**TXP**	A	100BASE-TX Ethernet Transmit Data Positive.
100BASE-TX Ethernet Transmit Data Negative	**TXN**	A	100BASE-TX Ethernet Transmit Data Negative.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Reference Resistor	EXTRES	A	Reference resistor connection pin. For proper operation, this pin must be connected to VSS through a 6.49kΩ 0.1% resistor.
SGMII Port (LAN9373 Only)			
SGMII Differential Input Data+	S_INP	SGMII-I	SGMII Differential Input Data+.
SGMII Differential Input Data-	S_INM	SGMII-I	SGMII Differential Input Data-.
SGMII Differential Output Data+	S_OUTP	SGMII-O	SGMII Differential Output Data+.
SGMII Differential Output Data-	S_OUTM	SGMII-O	SGMII Differential Output Data-.
Reference Resistor	S_EXTRES	A	SGMII reference resistor connection pin. For proper operation, this pin must be connected to VSS through a 200Ω 1% resistor using a short trace to avoid noise coupling.
RGMII/RMII/MII Ports			
RGMII/RMII/MII 2-1 Transmit Data 3	TXD_[2:1]_3	RGMII	**MII/RGMII Modes:** Transmit Data bus bit 3 output. **RMII Mode:** Not used. **Note:** These pins also provide configuration strap functions during hardware/software resets.
RGMII/RMII/MII 2-1 Transmit Data 2	TXD_[2:1]_2	RGMII	**MII/RGMII Modes:** Transmit Data bus bit 2 output. **RMII Mode:** Not used. **Note:** These pins also provide configuration strap functions during a hardware reset.
RGMII/RMII/MII 2-1 Transmit Data 1	TXD_[2:1]_1	RGMII	**MII/RMII/RGMII Modes:** Transmit Data bus bit 1 output. **Note:** These pins also provide configuration strap functions during a hardware reset.
RGMII/RMII/MII 2-1 Transmit Data 0	TXD_[2:1]_0	RGMII	**MII/RMII/RGMII Modes:** Transmit Data bus bit 0 output. **Note:** These pins also provide configuration strap functions during a hardware reset.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
RGMII/RMII/MII 2-1 Transmit/ Reference Clock	**TX_CLK_[2:1]/ REFCLKO_[2:1]**	RGMII	**MII Mode: TX_CLK_[2:1]** is the 25/2.5MHz Transmit Clock. In PHY mode this pin is an output, in MAC mode it is an input. **RMII Mode: REFCLKO_[2:1]** is the 50MHz Reference Clock output when in RMII Clock mode. This pin is unused when in RMII Normal mode. **RGMII Mode: TX_CLK_[2:1]** is the 125/25/2.5MHz Transmit Clock output. **Note:** The **TX_CLK_2** pin also provides configuration strap functions during a hardware reset.
RGMII/RMII/MII 2-1 Transmit Enable/ Control	**TX_EN_[2:1]/ TX_CTL_[2:1]**	RGMII	**MII/RMII Modes: TX_EN_[2:1]** is the Transmit Enable output. **RGMII Mode: TX_CTL_[2:1]** is the Transmit Control output. **Note:** The **TX_EN_2** pin also provides configuration strap functions during a hardware reset.
RGMII/RMII/MII 2-1 Receive Data 3	**RXD_[2:1]_3**	RGMII	**MII/RGMII Modes:** Receive Data bus bit 3 input. **RMII Mode:** Not used. Do not connect this pin in this mode of operation.
RGMII/RMII/MII 2-1 Receive Data 2	**RXD_[2:1]_2**	RGMII	**MII/RGMII Modes:** Receive Data bus bit 2 input. **RMII Mode:** Not used. Do not connect this pin in this mode of operation.
RGMII/RMII/MII 2-1 Receive Data 1	**RXD_[2:1]_1**	RGMII	**MII/RMII/RGMII Modes:** Receive Data bus bit 1 input.
RGMII/RMII/MII 2-1 Receive Data 0	**RXD_[2:1]_0**	RGMII	**MII/RMII/RGMII Modes:** Receive Data bus bit 0 input.
RGMII/RMII/MII 2-1 Receive Clock	**RX_CLK_[2:1]/ REFCLKI_[2:1]**	RGMII	**MII Mode: RX_CLK_[2:1]** is the 25/2.5MHz Receive Clock. In PHY mode this pin is an output, in MAC mode it is an input. **RMII Mode: REFCLKI_[2:1]** is the 50MHz Reference Clock input when in RMII Normal mode. This pin is unused when in RMII Clock mode. **RGMII Mode: RX_CLK_[2:1]** is the 125/25/2.5MHz Receive Clock output.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
RGMII/RMII/MII 2-1 Receive Data Valid / Carrier Sense / Control	**RX_DV_[2:1]/ CRS_DV_[2:1]/ RX_CTL_[2:1]**	RGMII	**MII Mode: RX_DV_[2:1]** is the Receive Data Valid / Carrier Sense input. **RMII Mode: CRS_DV_[2:1]** is the Carrier Sense / Receive Data Valid input. **RGMII Mode: RX_CTL_[2:1]** is the Receive Control input.
RGMII/RMII/MII 2-1 Receive Error	**RX_ER_[2:1]**	RGMII	**MII/RMII Modes:** Receive Error input. **RGMII Mode:** Not used. Do not connect this pin in this mode of operation.
RGMII/RMII/MII 2-1 125 MHz Reference Clock Output	**CLK125**	RGMII	125 MHz RGMII reference clock output to SoC MAC. **Note:** This pin also provides configuration strap functions during a hardware reset.
SPI Pins			
SPI Clock	**SCL**	VIS	SPI clock. The maximum supported SPI Clock frequency is 50 MHz.
SPI Chip Select	**SCS_N**	VIS	Active-low SPI chip select input.
SPI Data Out	**SDO**	VO8	SPI output data. **Note:** This pin also provides configuration strap functions during a hardware reset.
SPI Data In	**SDI**	VIS	SPI input data.
MDIO Pins			
SMI Data Input/Output	**MDIO**	VIS/VO8	Serial Management Interface data input/output.
SMI Clock	**MDC**	VIS	Serial Management Interface clock.
LED Pins			
LED Indicator 1	**LED_1**	VIS/VO8	LED Indicator 1. This pin may also function as a programmable input/output. This signal can also be used as an input or output for use by the IEEE 1588 event trigger or time -stamp capture units. It will be synchronized to the internal IEEE 1588 clock.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
LED Indicator 2	**LED_2**	VIS/VO8	LED Indicator 2. This pin may also function as a programmable input/output. **Note:** This pin also provides configuration strap functions during a hardware reset.
LED Indicator 3	**LED_3**	VIS/VO8	LED Indicator 3. This pin may also function as a programmable input/output.
LED Indicator 4	**LED_4**	VIS/VO8	LED Indicator 4. This pin may also function as a programmable input/output.
LED Indicator 5	**LED_5**	VIS/VO8	LED Indicator 5. This pin may also function as a programmable input/output. **Note:** This pin also provides configuration strap functions during a hardware reset.
LED Indicator 6	**LED_6**	VIS/VO8	LED Indicator 6. This pin may also function as a programmable input/output. **Note:** This pin also provides configuration strap functions during a hardware reset.
LED Indicator 7	**LED_7**	VIS/VO8	LED Indicator 7. This pin may also function as a programmable input/output.
LED Indicator 8	**LED_8**	VIS/VO8	LED Indicator 8. This pin may also function as a programmable input/output.
LED Indicator 9	**LED_9**	VIS/VO8	LED Indicator 9. This pin may also function as a programmable input/output.
LED Indicator 10	**LED_10**	VIS/VO8	LED Indicator 10. This pin may also function as a programmable input/output.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
JTAG Pins			
JTAG Test Data Input	**TDI**	VIS	JTAG (IEEE 1149.1) data input. **Note:** When not used, tie this pin to **VDDIO**.
JTAG Test Data Output	**TDO**	VO8	JTAG (IEEE 1149.1) test data output.
JTAG Test Clock	**TCK**	VIS	JTAG (IEEE 1149.1) test clock. **Note:** When not used, tie this pin to **VSS**.
JTAG Test Mode Select	**TMS**	VIS	JTAG (IEEE 1149.1) test mode select. **Note:** When not used, tie this pin to **VSS**.
Miscellaneous Pins			
System Reset	**RESET_N**	VIS	System reset. This pin is active low. **Note:** When not used, this pin should be pulled-up to **VDDIO**.
Wake Input	**WAKE_IN**	VIS_VBAT	Wakeup Input. Asserted to move the part out of sleep. This pin implements the optional wake input described in the OABR TC10 specification. **Note:** This pin operates of off **VBAT** domain.
Wake Output	**WAKE_OUT**	VO_VBAT	Wake Output. Asserted when the part moves out of sleep. This pin implements the optional wake output described in the OABR TC10 specification. **Note:** This pin operates of off **VBAT** domain.
Inhibit	**INH**	VO_VBAT	Inhibit. Used to switch on/off the main external power supply unit. This pin can be configured as an open source or open drain. **Note:** When configured as open source, an external pull-down is required. When configured as open drain, this pin should be connected to **VBAT** via an external pull-up. **Note:** **RESET_N** assertion does not affect the state of this pin.
Interrupt	**IRQ_N**	VOD	Active-low, open drain device interrupt. **Note:** When unused, leave this pin unconnected.
25 MHz Reference Clock	**CLKO_25M/ CASCADE_ID**	VO8	25 MHz reference clock output.
Crystal Clock / Oscillator Input	**XI**	ICLK	25MHz Crystal clock / oscillator input. When using a crystal, this input is connected to one lead of the crystal. When using an oscillator, this pin is the input from the oscillator.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Crystal Clock Output	**XO**	OCLK	25MHz Crystal clock output. When using a crystal, this output is connected to one lead of the crystal. When using an oscillator, this pin is left unconnected.
No Connect	**NC**	-	No Connect. For proper operation, **NC** pins must be left unconnected.
I/O Power pins, Core Power Pins, and Ground Pins			
+1.8 - 3.3V I/O Power Supply Input	**VDDIO**	P	+1.8 - 3.3V variable supply for IOs.
+1.1V Digital Core Power Supply Input	**VDD11**	P	+1.1V digital core power.
+1.1V T1 Common Block Power Supply	**VDD11ACOM**	P	+1.1V analog power supply for T1 common block.
+1.1V TX/RX Analog Power Supply	**VDD11ATXRX**	P	+1.1V analog power supply for T1 PHY.
+2.5 - 3.3V TX/RX Analog Power Supply	**VDDATXRX**	P	+2.5 - 3.3V analog power supply for T1 PHY.
+2.5 - 3.3V T1 Common Block Power Supply	**VDDACOM**	P	+2.5 - 3.3V analog power supply for T1 common block.
+2.5 - 3.3V VBAT Power Supply	**VBAT**	P	+2.5 - 3.3V power supply for the VBAT domain.
+1.8 - 3.3V RGMII/RMII/MII 1 Analog Power Supply	**VDDRGMII1**	P	+1.8 - 3.3V variable power supply for RGMII/MII/RMII 1 interface.
+1.8 - 3.3V RGMII/RMII/MII 2 Analog Power Supply	**VDDRGMII2**	P	+1.8V - 3.3V variable power supply for RGMII/MII/RMII 2 interface.
+1.1V SGMII Low Power Supply	**S_VPS**	P	+1.1V SGMII core power supply. (LAN9373 only) This supply must be isolated on the PCB through a ferrite bead.

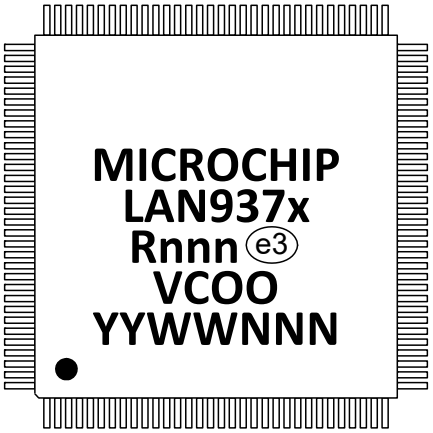
TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+2.5/3.3V SGMII High Power Supply	S_VPH	P	+2.5/3.3V SGMII high power supply. This supply may operate at 2.5V or 3.3V. (LAN9373 only) This supply must be isolated on the PCB through a ferrite bead.
SGMII Transmitter Supply	S_VPTX0	P	+1.1V SGMII Transmitter power supply. (LAN9373 only) This supply must be isolated on the PCB through a ferrite bead.
+2.5 - 3.3V Analog Power	E_VDDHV	P	+2.5 - 3.3V analog power supply.
+1.1V PLL Power	E_VDDA	P	+1.1V PLL digital power supply.
Ground	VSS	P	Ground pad.

4.0 PACKAGE INFORMATION

4.1 Package Marking Information

128-TQFP-EP



Legend:	x	Part number (2, 3, or 4)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	V	Plant assembly
	COO	Country of origin
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

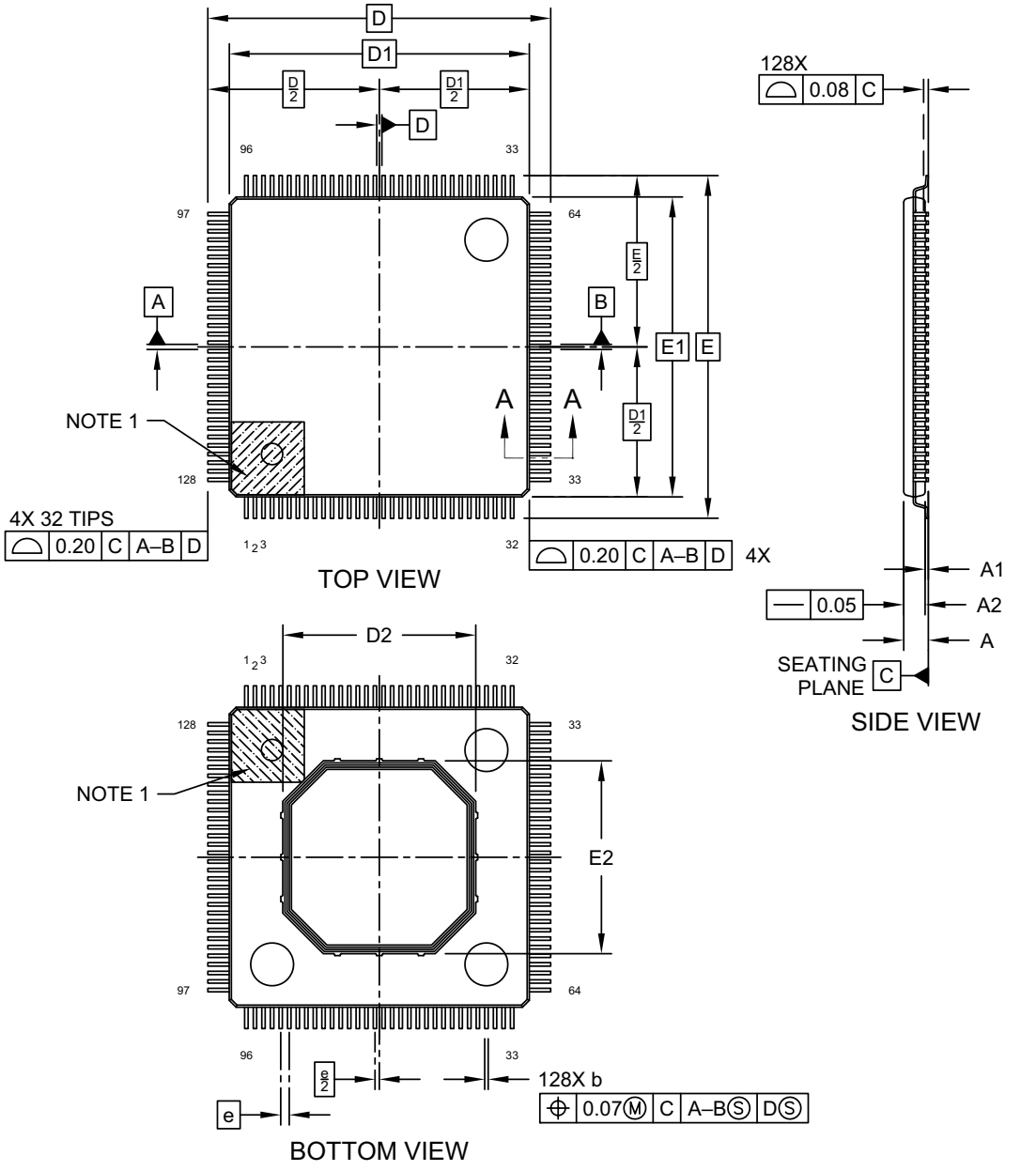
***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

4.2 Package Drawings

FIGURE 4-1: PACKAGE (DRAWING)

128-Lead Thin Quad Flat Pack (ZMX) - 14x14x1.0 mm Body [TQFP]
With 9x9 mm Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

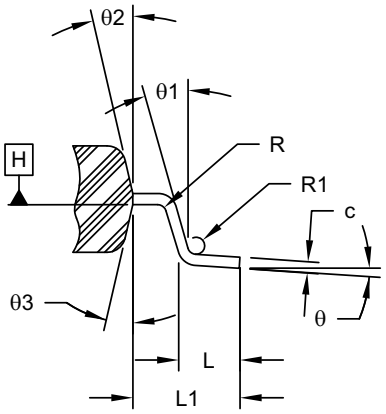


Microchip Technology Drawing C04-502 Rev A Sheet 1 of 2

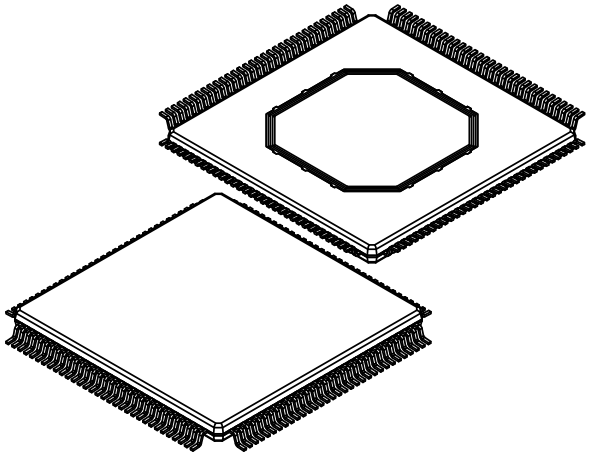
FIGURE 4-2: PACKAGE (DIMENSIONS)

128-Lead Thin Quad Flat Pack (Z2X) - 14x14x1.0 mm Body [TQFP]
With 9x9 mm Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		128	
Lead Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		16.00 BSC	
Molded Package Length	D1		14.00 BSC	
Molded Package Length	D2	8.90	9.00	9.10
Overall Width	E		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Width	E2	8.90	9.00	9.10
Lead Width	b	0.13	0.16	0.23
Lead Thickness	c	0.09	-	0.20
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	-	7°
Lead Angle	θ1	0°	-	-
Mold Draft Angle Top	θ2	11°	12°	13°
Mold Draft Angle Bottom	θ3	11°	12°	13°
Lead Bend Radius	R	0.08	-	-
Lead Bend Radius	R1	0.08	-	0.20

Notes:

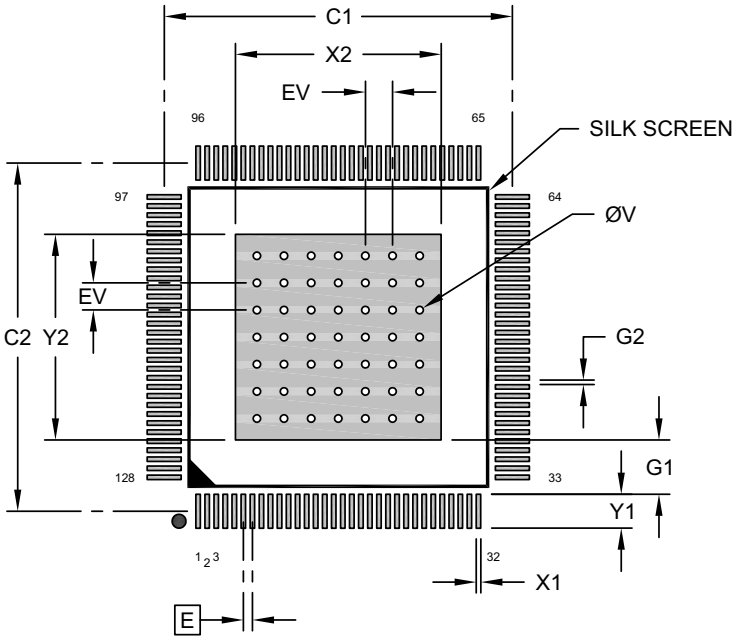
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-181 Rev A Sheet 2 of 2

FIGURE 4-3: PACKAGE (LAND PATTERN)

128-Lead Thin Quad Flat Pack (ZMX) - 14x14x1.0 mm Body [TQFP]
With 9x9 mm Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	X2			9.10
Optional Center Pad Length	Y2			9.10
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X128)	X1			0.20
Contact Pad Length (X128)	Y1			1.50
Contact Pad to Center Pad (X128)	G1	2.40		
Contact Pad to Contact Pad (X124)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2502 Rev A

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003905A (04-06-21)	Public Release	

THE MICROCHIP WEB SITE

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Technical support is available through the web site at: http://www.microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX	XXX
Device	Tape & Reel Option		Temp. Range		Package	Automotive Code

Device:	LAN9372 = 8-Port Switch (2 RGMII/MII/RMII, 1 100BASE-TX) LAN9373 = 8-Port Switch (2 RGMII/MII/RMII, 1 SGMII) LAN9374 = 8-Port Switch (2 RGMII/MII/RMII)	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	-V	= -40°C to +105°C (Grade 2 Automotive)
Package:	ZMX	= 128-pin TQFP-EP
Automotive Code:	Vxx	= 3 character code with “V” prefix, specifying automotive product

Examples:

a) LAN9372-V/ZMXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

b) LAN9372T-V/ZMXVAO
Tape and reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

c) LAN9373-V/ZMXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

d) LAN9373T-V/ZMXVAO
Tape and reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

e) LAN9374-V/ZMXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

f) LAN9374T-V/ZMXVAO
Tape and reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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