
EQCO62R20.3 6.25 Gbps Asymmetric Coax Equalizer/ EQCO31R20.3 3.125 Gbps Asymmetric Coax Equalizer

Features

- Complies with the CoaXPress v1.1 camera standard ⁽¹⁾
- Supports up to 68 meters of cable at 6.25 Gbps using high-quality coax
- Supports up to 212 meters of cable at 1.25 Gbps using high-quality coax
- Single-chip solutions for both the camera side and the frame grabber side, making a bidirectional connection over a single 75Ω coax cable
- Full-Duplex, bidirectional data channel
 - Downlink speeds from 1.25 Gbps up to 6.25 Gbps; differential interfacing straightforward with internal termination resistors
 - Uplink supporting 21 Mbps, allowing nanoseconds precise triggering events driven by the frame grabber
- Supports power distribution over the coax up to 900 mA, powering the camera through the same coax transporting data signals
- Low power consumption (<70 mW, 1.2V supply)
- 16-Pin, 0.65 mm pin pitch, 4 mm QFN package
- Small PCB footprint for EQCO62R20 and off-chip components, with guaranteed RF-performance
- -40°C to +85°C industrial temperature range
- Pb-free and RoHS compliant

Applications

- High-definition/high-bandwidth links to cameras
- Machine vision for semiconductor chips and display panel inspection systems
- Military, aerospace, medical applications
- Broadcast and surveillance camera systems
- Traffic license plate and monitoring systems
- High-Speed inspection systems for food inspection, bottling inspection, panel inspection, etc.
- Any application requiring a single coax cable which carries power, video data and camera control stream.

Introduction

The EQCO62T/R20⁽²⁾ chipset is a driver/equalizer chipset that forms a bidirectional, full-duplex communication link over a single coax cable.

The EQCO62T/R20 chipset is designed to transport up to 6.25 Gbps over the downlink channel and to transport 21 Mbps over the uplink channel. The EQCO62T20 is designed to transmit the downlink signal at up to 6.25 Gbps and receive the uplink signal. The EQCO62R20 is designed to receive the downlink signal at up to 6.25 Gbps and to transmit the uplink signal. Power can be transferred over the same cable via external inductors.

The chipset is designed to work with several types of 75Ω coaxial cables, including legacy cables as well as thin, flexible lightweight cables.

Note 1: CoaXPress V1.1 standard. Free download from the J11A website:

<http://j11a.org/en/standardization/list/>

2: The EQCO31T20 and EQCO31R20 are lower-speed versions of the EQCO62T20 and EQCO62R20, with a maximum bit rate of 3.125 Gbps for the high-speed downlink and the same uplink speed.

EQCO62R20.3/EQCO31R20.3

Typical Link Performance

Table 1, Table 2 and Table 3 give an overview of typical link performance at room temperature for the link containing the EQCO62T20 coax driver in conjunction with the EQCO62R20 receiver, using the downlink channel, uplink channel and power transmission simultaneously. Performance for EQCO62T/R20 and EQCO31T/R20 is equal for bit rates up to 3.125 Gbps.

TABLE 1: BELDEN TYPICAL LINK PERFORMANCE

	Name	Belden 7731A	Belden 1694A	Belden 1505A	Belden 1505F	Belden 1855A
	Type	Long Distance	Industry Standard	Compromise Coax	Flexible	Thinnest Cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
1.25 Gbps	(m)	194	130	107	80	55
2.5 Gbps	(m)	162	110	94	66	55
3.125 Gbps	(m)	147	100	86	60	55
5.0 Gbps	(m)	87	60	52	35	38
6.25 Gbps	(m)	58	40	35	23	25

TABLE 2: GEPKO TYPICAL LINK PERFORMANCE

	Name	Gepco VHD1100	Gepco VSD2001	Gepco VPM2000	Gepco VHD2000M	Gepco VDM230
	Type	Long Distance	Industry Standard	Compromise Coax	Flexible	Thinnest Cable
Diameter	(mm)	10.3	6.91	6.15	6.15	4.16
1.25 Gbps	(m)	212	140	109	81	66
2.5 Gbps	(m)	185	120	94	67	66
3.125 Gbps	(m)	169	110	86	61	62
5.0 Gbps	(m)	102	66	53	36	38
6.25 Gbps	(m)	68	44	35	24	25

TABLE 3: CANARE TYPICAL LINK PERFORMANCE⁽¹⁾

	Name	Canare L-7CFB	Canare L-5CFB	Canare L-4CFB	Canare L-3CFB	Canare L-2.5CFB
	Type	Long Distance	Industry Standard	Compromise Coax	Thin Cable	Thinnest Cable
Diameter	(mm)	10.2	7.7	6.1	5.5	4
1.25 Gbps	(m)	165	118	94	72	43
2.5 Gbps	(m)	135	98	79	66	43
3.125 Gbps	(m)	122	88	71	60	43
5.0 Gbps	(m)	71	52	42	36	30
6.25 Gbps	(m)	46	34	28	24	20

Note 1: Specifications from Canare are only up to 2 GHz. 5 Gbps and 6.25 Gbps performance are by extrapolation.

Table of Contents

1.0	Device Overview	4
2.0	Application Information.....	9
3.0	Electrical Characteristics	16
4.0	Packaging.....	18

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.

EQCO62R20.3/EQCO31R20.3

1.0 DEVICE OVERVIEW

The EQCO62T/R20 single-coax chipset is designed to simultaneously transmit and receive signals on a single 75 Ω coax cable. In one direction, a downlink signal is transmitted. In the opposite direction, a lower-speed uplink is provided. The EQCO62T/R20 chipset consists of two chips. The EQCO62T20 is a high-speed line driver with an integrated low-speed receiver. The EQCO62R20 is a high-speed receiver with an integrated low-speed transmitter. Figure 1-1 illustrates a typical EQCO62T/R20 link setup.

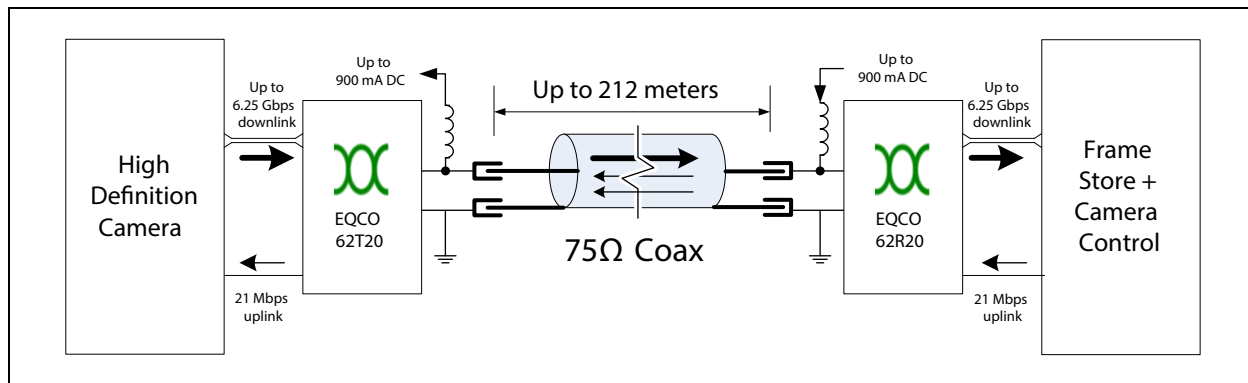
The downlink signal is transmitted with 600 mV transmit amplitude at the EQCO62T20 side. This signal is attenuated in the coax and recovered by an equalizer integrated in the EQCO62R20. The low-speed uplink is transmitted with a lower amplitude of 130 mV to limit the crosstalk with the downlink channel.

The downlink channel is intended for 8B/10B NRZ coded data with bitrates from 1.25 Gbps up to 6.25 Gbps. The low-speed uplink operates at a bit rate of 21 Mbps, and has a single-ended LVTTLL input and output.

In addition to the downlink channel and the low-speed uplink, the system allows power transmission over the coax by using ferrite beads and external inductors. These external inductors give the communication channel a high-pass characteristic. The uplink receiver inside the EQCO62T20 chip recovers the signal lost by this high-pass filter. Appropriate inductors need to be selected for correct operation of the link. Correct operation is only guaranteed with the inductor combination used in Figure 2-1, even though other components might be suited.

The EQCO62T/R20 chipset is compatible with the CoaXPress v1.1 camera standard.

FIGURE 1-1: TYPICAL EQCO62T/R20 LINK SETUP



EQCO62R20.3/EQCO31R20.3

1.1 Pinout and Pin Description

FIGURE 1-2: EQCO62R20.3 PIN DIAGRAM(VIEWED FROM TOP)

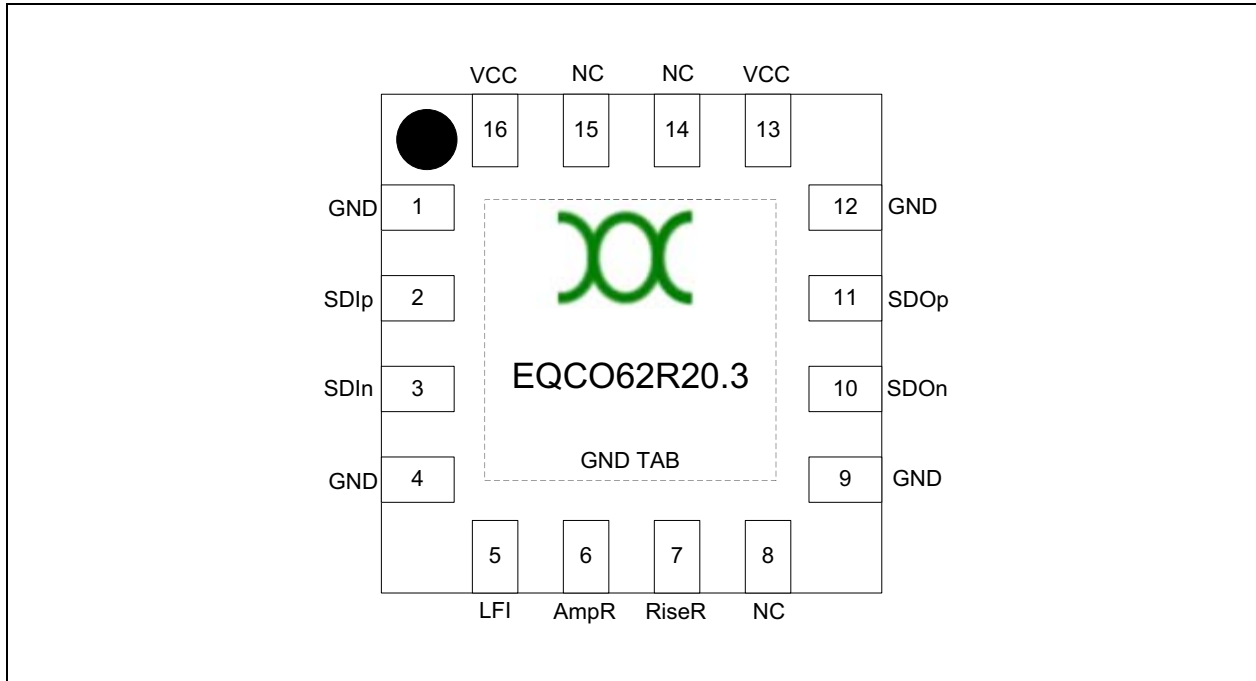


TABLE 1-1: EQCO62R20.3 PIN DESCRIPTIONS

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Use as single-point ground.
13, 16	VCC	Power	Connect to 1.2V of power supply.
1, 4, 9, 12	GND	Power	Connect to ground of power supply.
2, 3	SDIp, SDIn	CML Input	Serial input positive/negative differential serial input. Connect SDIn to shield of cable via termination network. External 15Ω resistors required.
11, 10	SDOp/SDOn	CML Output	Serial output positive/negative differential serial output. Output has a swing of 2x600 mV and has 2x50Ω on-chip termination resistors.
5	LFI	Input	Uplink input signal. LVTTTL signal with 1.2V input swing. External series resistor is required for 2.5V (3.9 kΩ) or 3.3V (6.2 kΩ) input swing.
6	AmpR	Input	Connected to VCC by a resistor that selects output swing of the uplink signal. Typical value is $R_{amp} = 1.2\text{ k}\Omega$ for rise/fall times of 11 ns.
7	RiseR	Input	Connected to VCC by a resistor that selects rise time of the uplink signal. Typical value is $R_{rise} = 10\text{ k}\Omega$ for rise/fall times of 11 ns.
8, 14, 15	NC	—	Do not connect. Leave these pins floating. Used for internal testing.

EQCO62R20.3/EQCO31R20.3

1.1.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. It is the differential voltage between these pins that the EQCO62R20 analyzes and adaptively equalizes for signal level and frequency response. The equalizer automatically detects and adapts to signals with different edge rates, different attenuation levels and different cable characteristics. Both SDIp and SDIn inputs are terminated by 60Ω to VCC on-chip. For each input, an external 15Ω resistor is required in series.

1.1.2 SDOp/SDOn

SDOp/SDOn together form a differential pair, outputting the reconstructed far-end transmit signal. SDOp/SDOn are terminated on-chip with $2 \times 50\Omega$ resistors.

1.1.3 LFI

LFI is the uplink input signal that will be transmitted on the SDIp/SDIn pair. LFI must be a 1.2V LVTTTL signal. For 2.5V and 3.3V input swing, an external resistor is needed in series at the input of the chip.

1.1.4 AmpR

AmpR is a VCC resistor that sets the transmit amplitude of the uplink output driver. The typical value for CoaXPress is $R_{amp} = 1.2\text{ k}\Omega$ for 130 mV transmit amplitude.

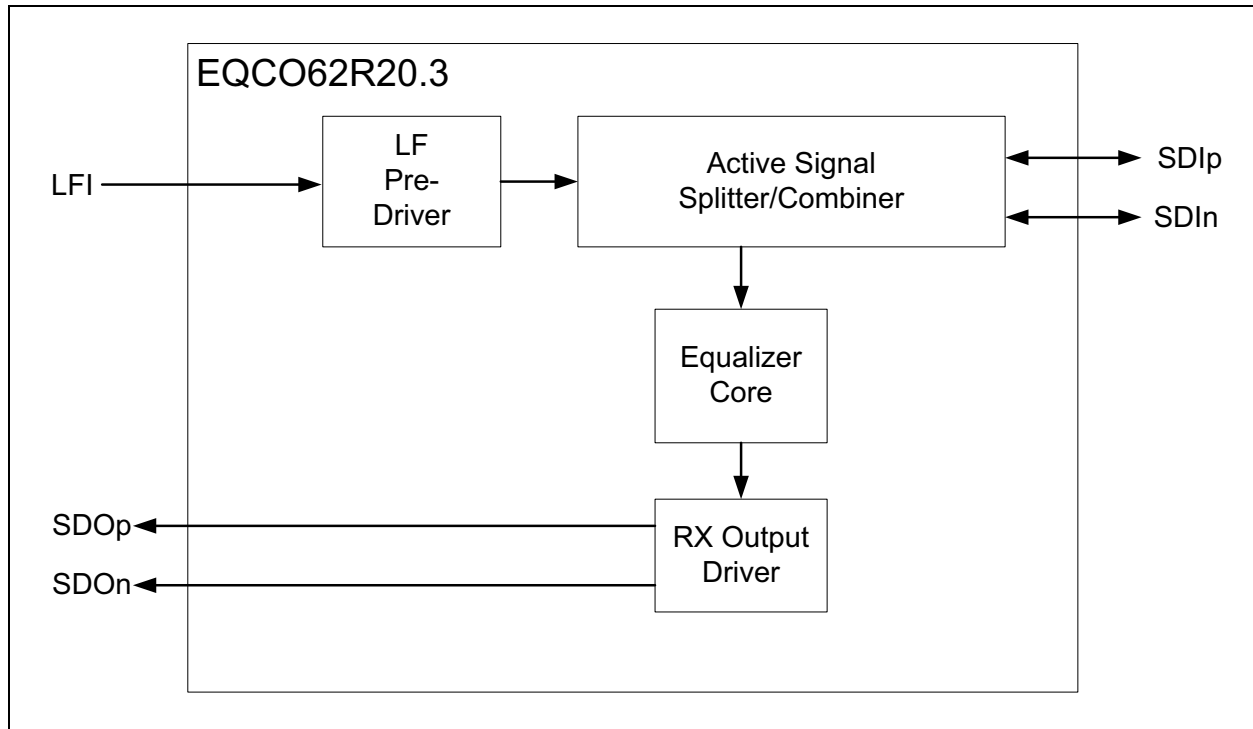
1.1.5 RISER

RiseR is a VCC resistor that selects the rise/fall time of the uplink output driver. The typical value for CoaXPress is $R_{rise} = 10\text{ k}\Omega$ for rise/fall time of 11 ns.

If no R_{amp} and R_{rise} are placed, the LF driver is disabled.

1.2 Circuit Operation

FIGURE 1-3: EQCO62R20.3 BLOCK DIAGRAM SHOWING ELECTRICAL CONNECTIONS



1.2.1 LF PRE-DRIVER

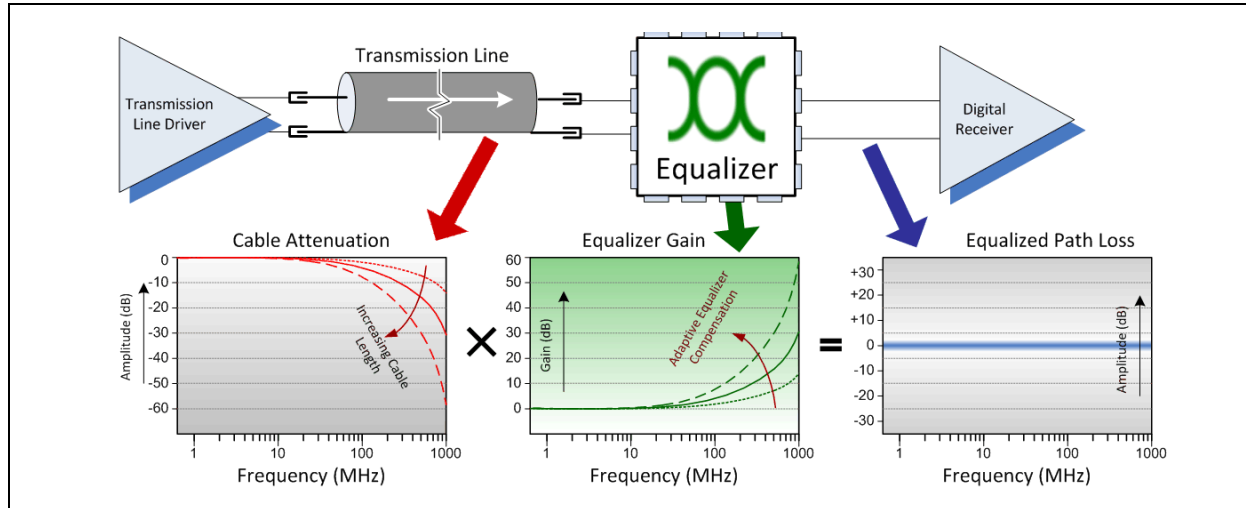
The uplink pre-driver converts the incoming LVTTTL signal at the LFI pin to a signal with well-controlled amplitude and rise/fall times that will be transmitted onto the cable by the active splitter/combiner.

1.2.2 ACTIVE SIGNAL SPLITTER/COMBINER

The active splitter/combiner transmits the outgoing coax signal via an internal 60Ω output termination resistor. The total $(60\Omega + 15\Omega)$ output resistor, when balanced with the coax characteristic impedance, also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDI output to give yield the far-end TX signal.

EQCO62R20.3/EQCO31R20.3

FIGURE 1-4: PRINCIPLE OF EQUALIZER OPERATION



1.2.3 EQUALIZER CORE

The EQCO62R20 has an embedded equalizer in the receive path with the following characteristics:

- Auto-Adaptive

The equalizer controls a multiple-pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 1-4. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable Gain

The EQCO62R20 equalizer has variable gain to compensate for low-frequency attenuation through the coax and variations in transmit amplitude.

- Multi-Speed

The EQCO62R20 works at data rates from 1.25 Gbps to 6.25 Gbps with 8B/10B coding.

Example equalizer performance measurements can be found in Figure B-1.

1.2.4 RX OUTPUT DRIVER

The output driver converts the output of the equalizer core to a LVDS-like signal and sends it onto a 100Ω differential transmission line.

EQCO62R20.3/EQCO31R20.3

Ferrite Beads Fb1 and Fb2 (FBMH1608HM102 from Taiyo Yuden) and inductor L1 (1812PS_103 from Coilcraft [10 μ H]) are recommended for CoaXPress. For other applications, the inductor value can be larger, leading to a physical larger inductor.

Connector BNC1 (75 Ω right angle BNC C-SX-090 from Cambridge) is recommended for CoaXPress.

Other inductors/ferrite beads/BNC connectors can possibly be used, however, they must be selected carefully for their RF-performance, since performance can decrease significantly.

optimal performance, including jitter and return-loss requirements, is to precisely follow the component and layout recommendations. Note that at multi-gigabit speeds, using "equivalent" components or small PCB layout changes (even moving a via) can have significant detrimental effects.

The easiest way for achieving the requirements of the CoaXPress 1.1 specification is to use the recommended circuits, components and layout illustrated in [Figure 2-1](#). For easy implementation, Microchip will provide the Gerber file. Please ask for it by email.

Note: Email address: coaxpress@microchip.com

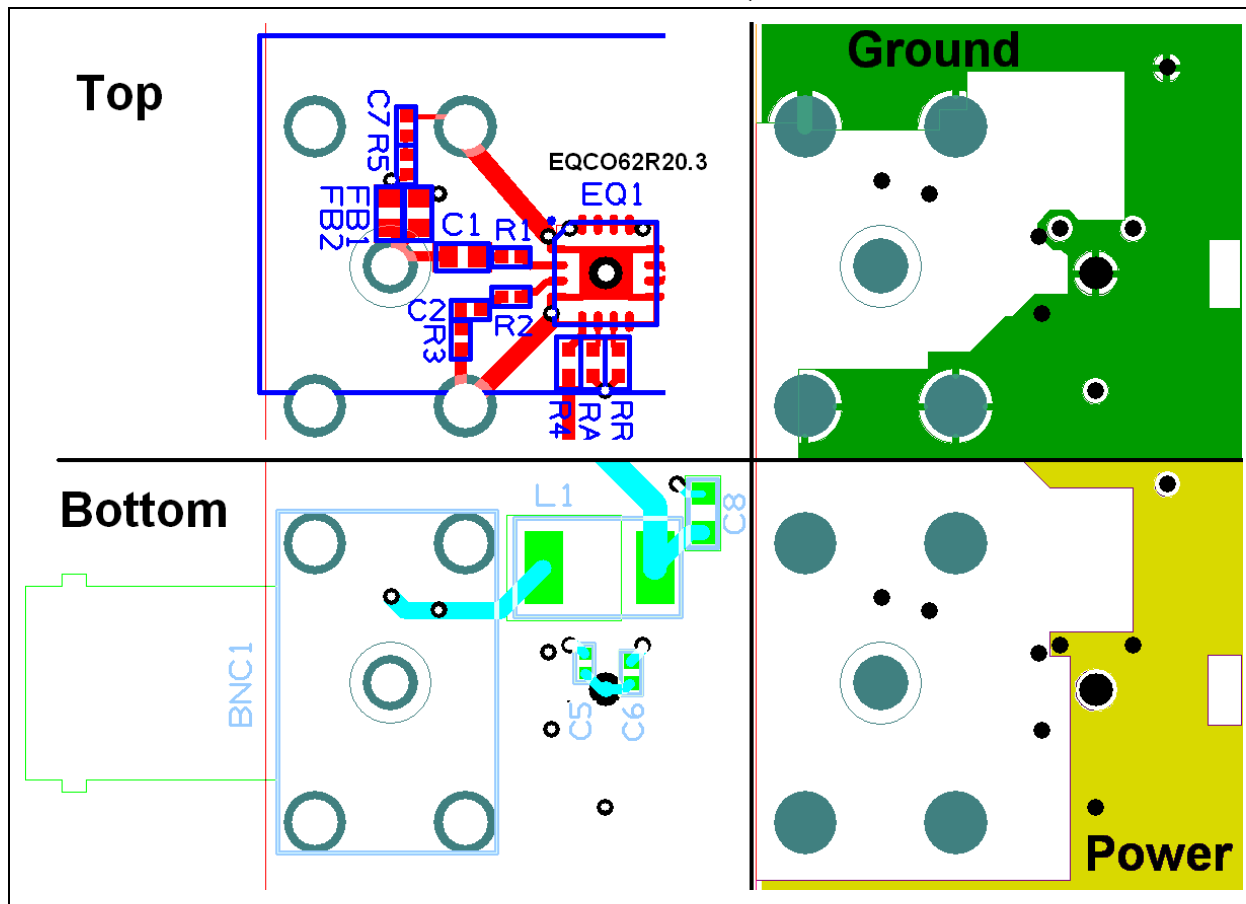
2.1 Guidelines for PCB Layout

When using the EQCO62T/R20 chipset at its full purpose, i.e. including low-speed uplink and power supply transmission, it is important not to disturb the RF-performance of the high-speed downlink channel. Implementing the circuit illustrated in [Figure 2-1](#) with a different PCB layout will in first instance not deliver full data sheet performance. The simplest way of meeting

2.1.1 RIGHT ANGLE BNC

[Figure 2-2](#) below shows the four layers of the recommended footprint for the EQCO62R20.3 chip and the off-chip components that are critical for the RF-performance of the system.

FIGURE 2-2: RECOMMENDED PCB LAYOUT FOR EQCO62R20.3



In this layout, the size of the PCB area needed for the chip is minimized. Approximately two times the BNC footprint area is required for the full bidirectional system: including the necessary elements for the power transport.

The differential output of the chip must be a 100 Ω differential transmission line. To minimize the parasitic capacitance of the input pins, a cut-out of the ground

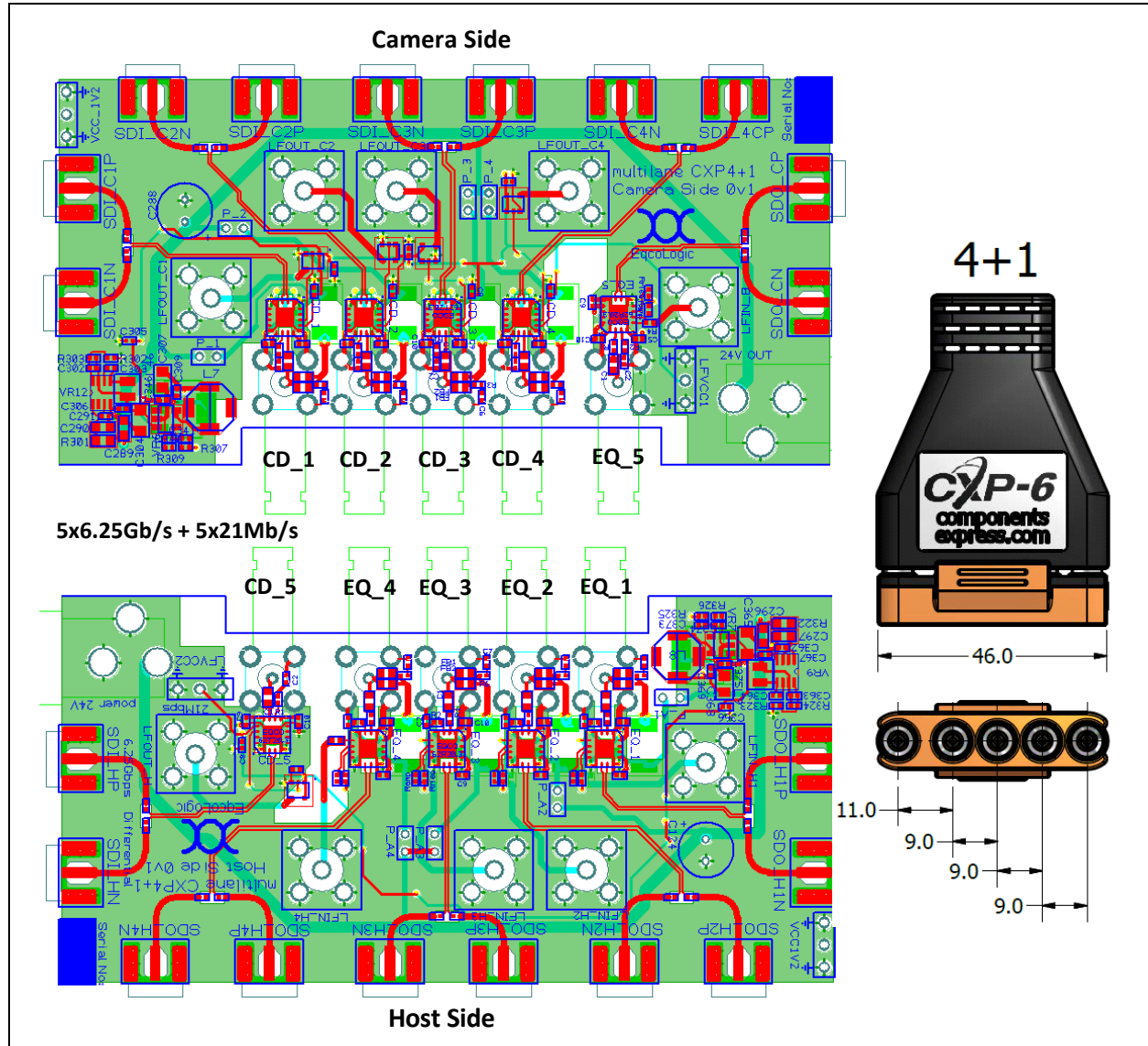
EQCO62R20.3/EQCO31R20.3

and power plane underneath the input pins is recommended. For best performance, no vias should be used in this high-speed signal path.

A large cut-out underneath the right angle BNC connector, the AC coupling capacitors, ferrite beads and inductor is needed for minimal parasitics.

This proposed layout is designed to be largely independent of the used PCB-layer stack. This will work as well for four, six or even higher numbers of layers. Possible extra layers should have cut-outs as large as the full proposed footprint.

FIGURE 2-3: PCB LAYOUT OF MULTILANE COAXPRESS 0V1 DEMO BOARD PAIR



2.1.2 MULTILANE COAXPRESS 4+1 LAYOUT WITH DIN1.0/2.3 CONNECTORS

Figure 2-3 shows an example of a Multilane CoaXPress 4+1 setup. The recommended Din1.0/2.3 connector is the NPF 4076 from Cambridge Connectors. The cable example shows the pitches in millimeters. Figure 2-4 shows the four layers of the recommended footprints and off-chip components that are critical for RF-performance of the cable drivers CD_1 to CD_4 at the camera side, which have Power over CoaXPress (PoCXP). Figure 2-5 shows the variant without PoCXP used for CD_5 at the host side. The exact dimensions in millimeters are given in **Section 4.1 “Package Marking Information”**. It is recommended to copy these dimensions, especially the connection between the DIN1.0/2.3 connector and the chip, as this is a complex entity with coupled currents and compensated parasitic capacitances.

Despite the critical layout, this proposed layout is designed to be largely independent of the used PCB-layer stack, as the critical parts are mainly the top-layer only. This will work as well for four, six or even higher numbers of layers. Possible extra layers should have cut-outs as large as the full proposed footprint.

In these layouts, the size of the PCB area needed for the chip is minimized. This allows multiple lanes close together.

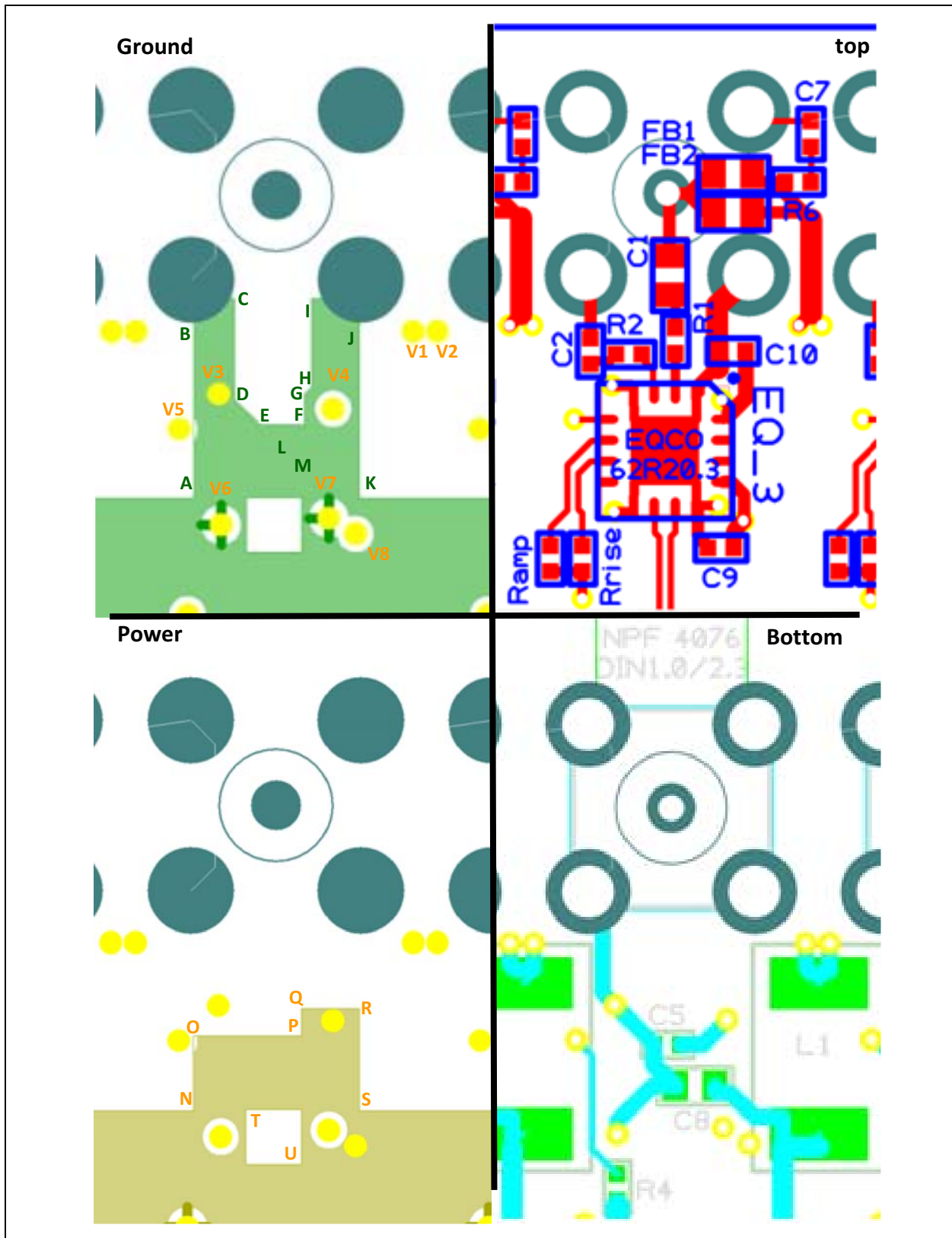
Only two of four connector GND pins are connected to the GND plane to reduce the capacitance.

The differential CD inputs must be a 100Ω differential transmission line. A cut-out of the ground and power plane underneath the input pins is recommended to minimize the parasitic capacitance. For best performance, no vias should be used in this high-speed signal path.

The Components Express 4+1 connector in Figure 2-3 is only shown as an example. Other connector configurations are available with DIN1.0/2.3 connectors such as 6+1, 2+1, 1+1, dual- or single-lane configurations.

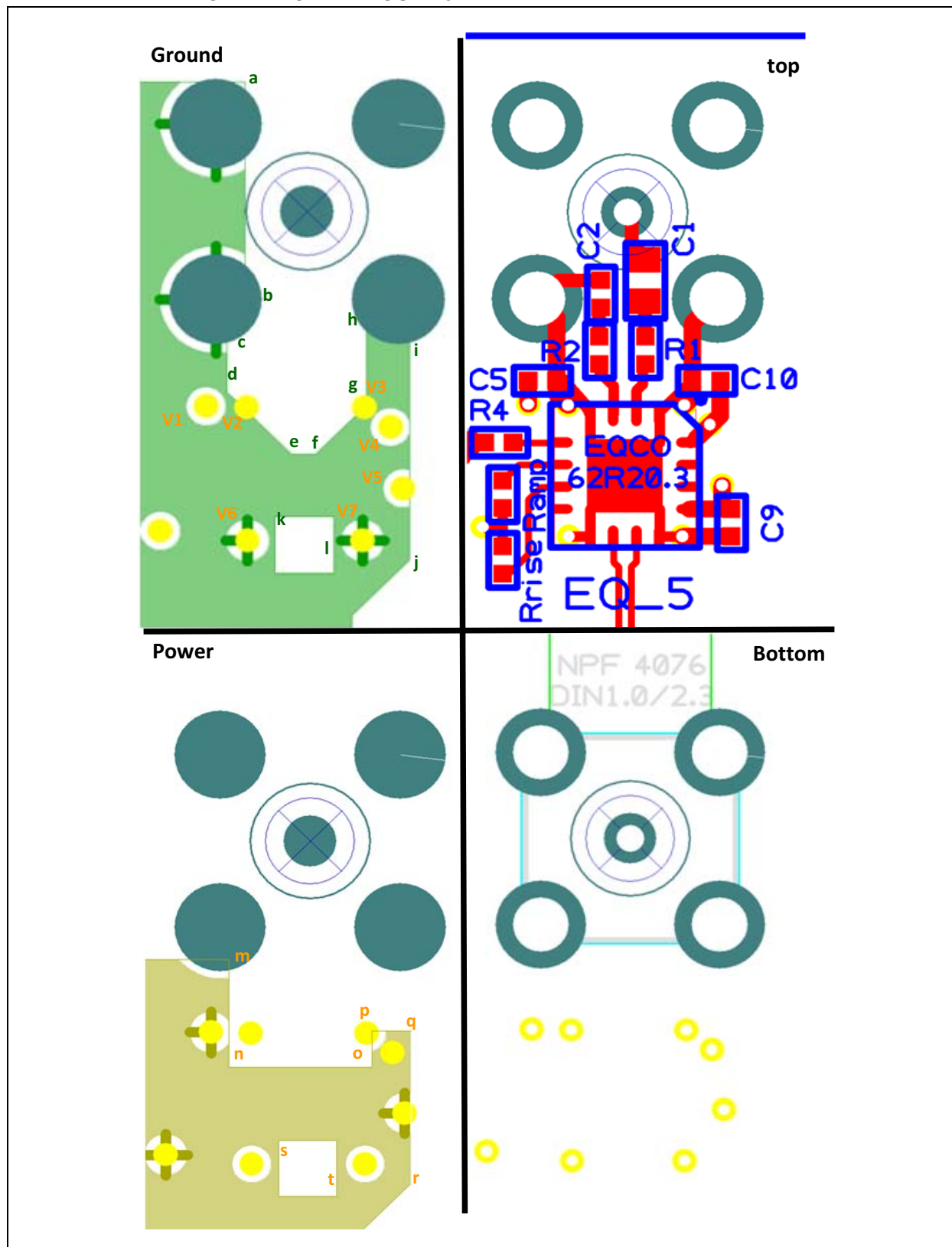
EQCO62R20.3/EQCO31R20.3

FIGURE 2-4: RECOMMENDED PCB LAYOUT FOR EQCO62R20.3 WITH DIN1.0/2.3 CONNECTOR WITH PoCXP



EQCO62R20.3/EQCO31R20.3

FIGURE 2-5: RECOMMENDED PCB LAYOUT FOR EQCO62R20.3 WITH DIN1.0/2.3 CONNECTOR WITHOUT PoCXP



2.2 Guidelines for Power Transmit Unit

At the Power-IN connection, a voltage supply is expected for powering a device (e.g. a camera) at the other end of the cable.

This voltage supply should have low ripple. High-frequency ripple will be rejected by C8/L1/FB1/FB2 filtering in the reference circuit. However, mid-frequency ripple is to be avoided by the power supply itself.

In a typical application, one could want to step-up from a 12V supply (e.g. in a PC) to a 24V power supply for CoaXPress. It is in this case preferred to use a DC-to-DC converter that has a high switching frequency (e.g. 2 MHz) above one that has lower switching frequency (200 kHz). The latter typically induces larger voltage spikes at the Power-IN connection. These will be only partially filtered out by said filter; the remainder will become crosstalk for the uplink channel.

When too much crosstalk remains on the uplink channel, additional power-supply filtering is required. This may be achieved by placing an extra filter network (not shown) in series with the Power-IN node.

2.3 Power Over CoaXPress

The EQCO62R20.3 is compatible with the Power over CoaXPress system (PoCXP) using the circuit from [Figure 2-2](#). Hence, power can be switched on and off by the host (e.g. frame grabber) through the 10 μ H inductor specified by the CXP standard. This switching is supported through a relay and through an electronic switch.

Powering through a wide-band bias-T is also supported.

The EQCO62R20.3 is also protected against the following events:

- Hot plugging by frame grabber: in case the frame grabber has already applied its 24V on the coax when connecting the cable, no damage will occur to the EQCO62R20.3 when connecting the powered coax cable.
- Fast turn-on and turn-off of power supply by frame grabber.

EQCO62R20.3/EQCO31R20.3

3.0 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature		-65	—	+150	°C
Ambient Temperature	Power Applied	-55	—	+125	°C
Operating Temperature	Normal Operation (VCC = 1.2V ±5%)	-40	—	+85	°C
Supply Voltage to Ground		-0.5	—	+1.4	V
DC Input Voltage		-0.5	—	+1.6	V
DC Voltage to Outputs		-0.5	—	+1.6	V
Current into Outputs	Outputs Low	—	—	90	mA

TABLE 3-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE)

Parameter	Description	Min.	Typ.	Max.	Unit
Power Supply					
VCC	Supply Voltage	1.15	1.2	1.25	V
I _s	Supply Current, both Transmitting and Receiving	—	60	—	mA
I _{sr}	Supply Current when only Receiving	—	50	—	mA
LFI Input (LVTTTL-Like)					
ΔV _{ih}	Input High Voltage	—	1.2	1.6	V
V _{il}	Input Low Voltage	-0.5	GND	—	V
R _{input}	Resistance to GND	—	3.6	—	kΩ
SDIp Connection to Coax					
Z _{coax}	Coax Cable Characteristic Impedance	—	75	—	Ω
R _{SDIP}	Input Impedance between SDIp/SDOn and VCC	—	60	—	Ω
V _{LF}	Uplink transmit amplitude for R _{amp} = 1.2 kΩ, measured inside cable after external 15 Ω resistor	110	130	160	mV
t _{rise_if}	Rise/fall time 20% to 80% of LF output on V _{SDIP} with R _{rise} = 10 kΩ and R _{amp} = 1.2 kΩ	7	11	15	ns
RL _{loss}	Coax Return-Loss as Seen on SDIp pin Frequency Range = 5 MHz-1 GHz	—	—	-15	dB
RL _{loss}	Coax Return-Loss as Seen on SDIp pin Frequency Range = 1 GHz-1.5 GHz	—	—	-10	dB
RL _{loss}	Coax Return-Loss as Seen on SDIp pin Frequency Range = 1.5 GHz-3.2 GHz	—	—	-7	dB
ΔV _{TX}	Transmit Amplitude for Downlink Signal	500	600	700	mV

EQCO62R20.3/EQCO31R20.3

TABLE 3-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE) (CONTINUED)

SDOp/SDOn Outputs					
ΔV_o	Output Amplitude $V_{SDOp,n}$ (into 2x50 Ω)	—	2x600	—	mV
R_{output}	Termination Between SDOp/SDOn and GND/VCC	—	2x50	—	Ω
t_{rise_o}	Rise/Fall Time 20% to 80% of $V_{SDOp,n}$	—	40	—	ps

TABLE 3-3: JITTER NUMBERS

Parameter	Conditions	Min.	Typ.	Max.	Units
Additive Jitter on LF Output	8B/10B Coded Signal at 21 Mbps Over Full VCC and Temperature Range	—	—	1	ns
DCD in LF Output	8B/10B Coded Signal at 21 Mbps Over Full VCC and Temperature Range	—	—	3	ns
Jitter in Equalizer Output	At 1.25 Gbps from 0 to 135m Belden 1694A = -22 dB Attenuation at 0.625 GHz ⁽¹⁾	—	—	0.3	UI
Jitter in Equalizer Output	At 2.5 Gbps from 0 to 115m Belden 1694A = -27.2 dB Attenuation at 1.25 GHz ⁽¹⁾	—	—	0.3	UI
Jitter in Equalizer Output	At 3.125 Gbps from 0 to 105m Belden 1694A = -28.1 dB Attenuation at 1.5625 GHz ⁽¹⁾	—	—	0.3	UI
Jitter in Equalizer Output	At 5 Gbps from 0 to 65m Belden 1694A = -22.6 dB Attenuation at 2.5 GHz ⁽¹⁾	—	—	0.3	UI
Jitter in Equalizer Output	At 6.25 Gbps from 0 to 45m Belden 1694A = -17.8 dB Attenuation at 3.125 GHz ⁽¹⁾	—	—	0.35	UI

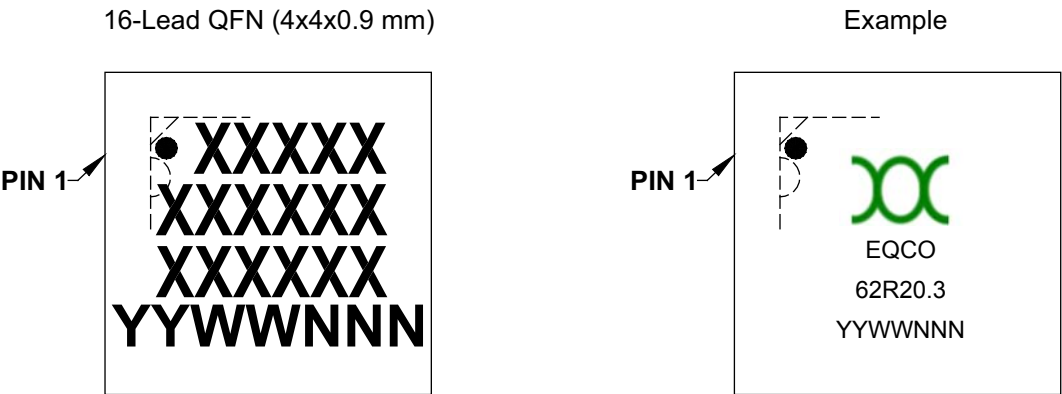
1: Jitter in Equalizer Output measured as 8B/10B coded signal over full transmit amplitude, VCC and temperature range, including uplink and power supply transmission.

EQCO62R20.3/EQCO31R20.3

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-Lead Plastic Quad Flat, No Lead Package – 4x4x0.9 mm Body [QFN]

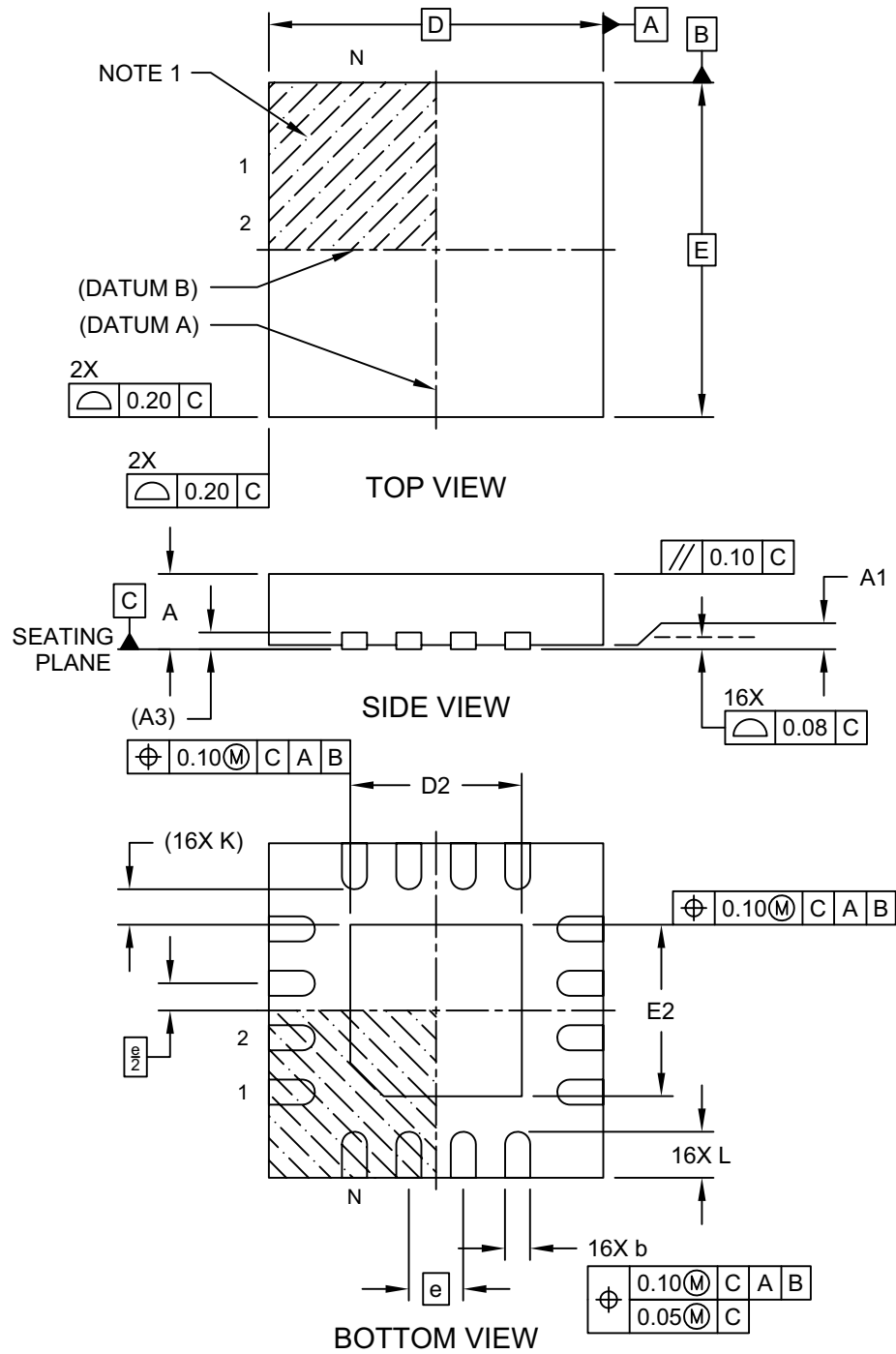


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

EQCO62R20.3/EQCO31R20.3

16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

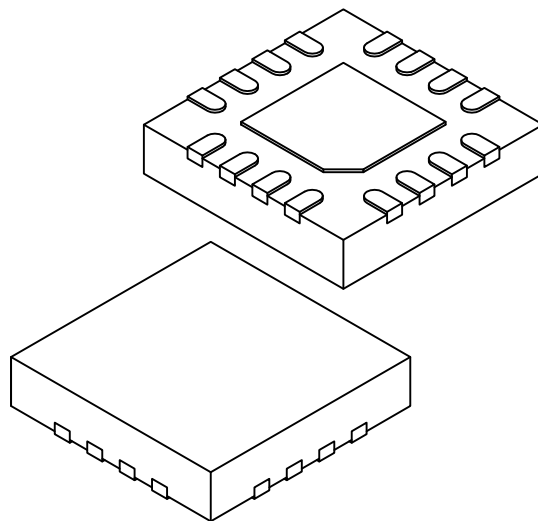


Microchip Technology Drawing C04-259B Sheet 1 of 2

EQCO62R20.3/EQCO31R20.3

16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		16		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.87	0.95
Standoff	A1		0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF		
Overall Width	E		4.00 BSC		
Exposed Pad Width	E2		1.95	2.05	2.15
Overall Length	D		4.00 BSC		
Exposed Pad Length	D2		1.95	2.05	2.15
Terminal Width	b		0.25	0.30	0.35
Terminal Length	L		0.45	0.55	0.65
Terminal-to-Exposed-Pad	K		0.425 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

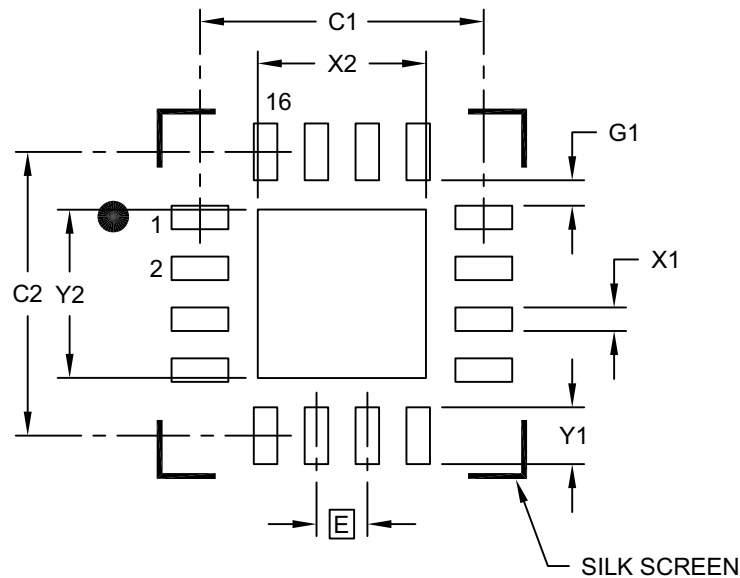
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-259B Sheet 2 of 2

EQCO62R20.3/EQCO31R20.3

16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			2.15
Optional Center Pad Length	Y2			2.15
Contact Pad Spacing	C1		3.625	
Contact Pad Spacing	C2		3.625	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.725
Contact Pad to Center Pad (X16)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2259A

EQCO62R20.3/EQCO31R20.3

APPENDIX A: REVISION HISTORY

Revision C (October 2018)

- Update [Table 3-2](#), Electrical Characteristics
- Update [Table 3-3](#), Jitter Numbers

Revision B (March 2016)

- Updated Package Information section.
- Removed electrostatic discharge ratings from Absolute Maximum Ratings table.
- Minor typographical changes.

Revision A (August 2014)

- This is the initial release of the document in the Microchip format. This replaces EqcoLogic document version 1v2.

TABLE A-1: REVISION HISTORY

Version	Date	Comments
1v2	1/27/14	Added references
1v1	4/10/12	Added Multilane CoaXPress 4+1 layout with DIN1.0/2.3 connectors
1v0	2/9/12	Initial release of this document

APPENDIX B: TYPICAL LINE EQUALIZER CHARACTERISTICS

All measurements at VCC = 1.2V, Temp = +25°C, data pattern = 8B/10B test pattern, 600 mV transmit amplitude using Belden 1694A coaxial cable, and include uplink and power supply transmission over the cable with differential measurement into 2x50Ω.

FIGURE B-1: 1.25 GBPS, 135M BELDEN 1694A

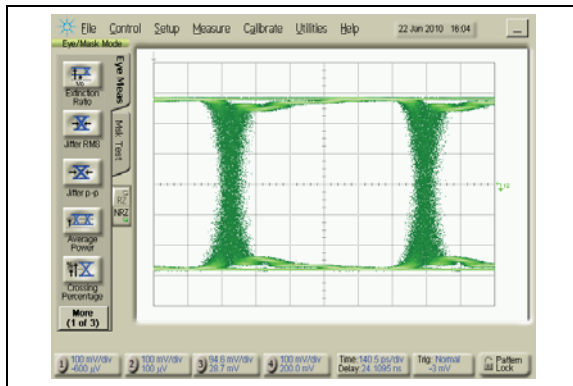


FIGURE B-4: 2.5 GBPS, 115M BELDEN 1694A

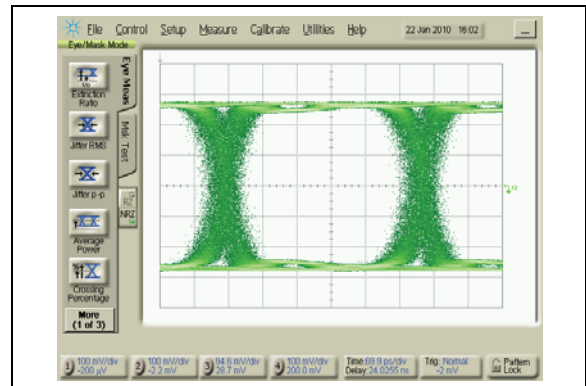


FIGURE B-2: 3.125 GBPS, 105M BELDEN 1694A

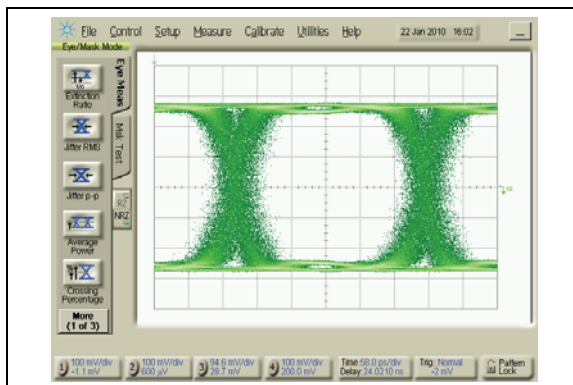


FIGURE B-5: 5 GBPS, 65M BELDEN 1694A (EQCO62R20 ONLY)

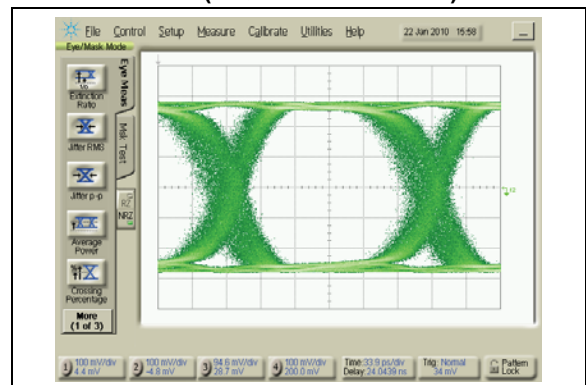
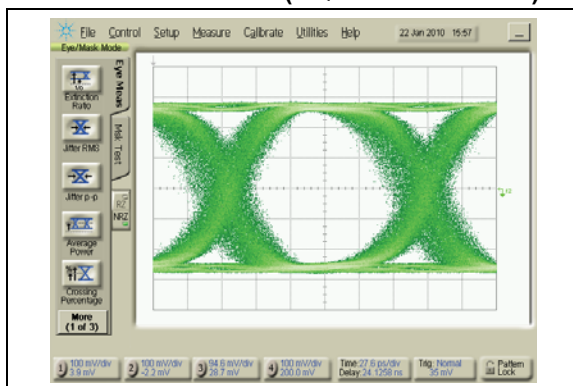


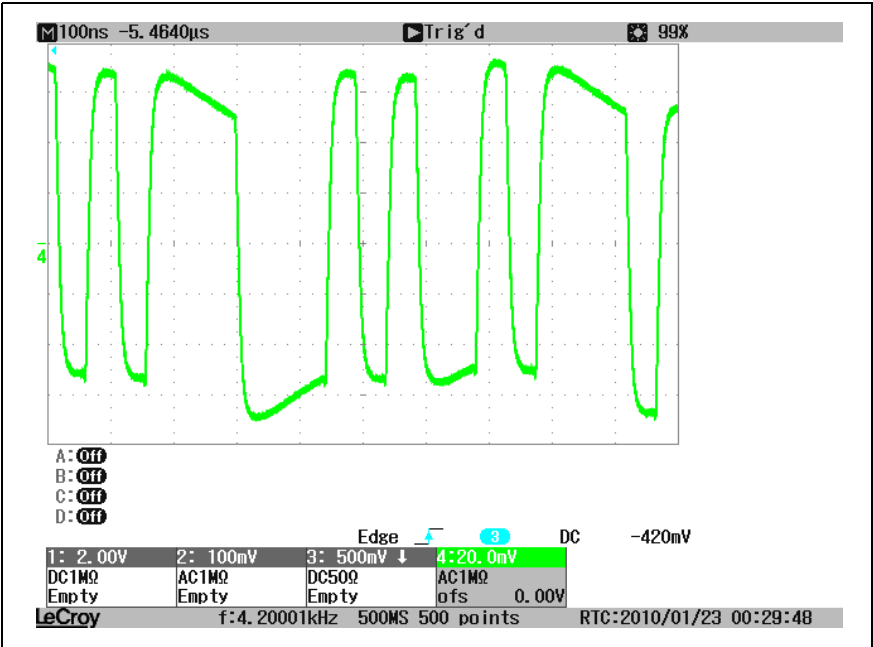
FIGURE B-3: 6.25 GBPS, 45M BELDEN 1694A (EQCO62R20 ONLY)



APPENDIX C: TYPICAL UPLINK CHARACTERISTICS

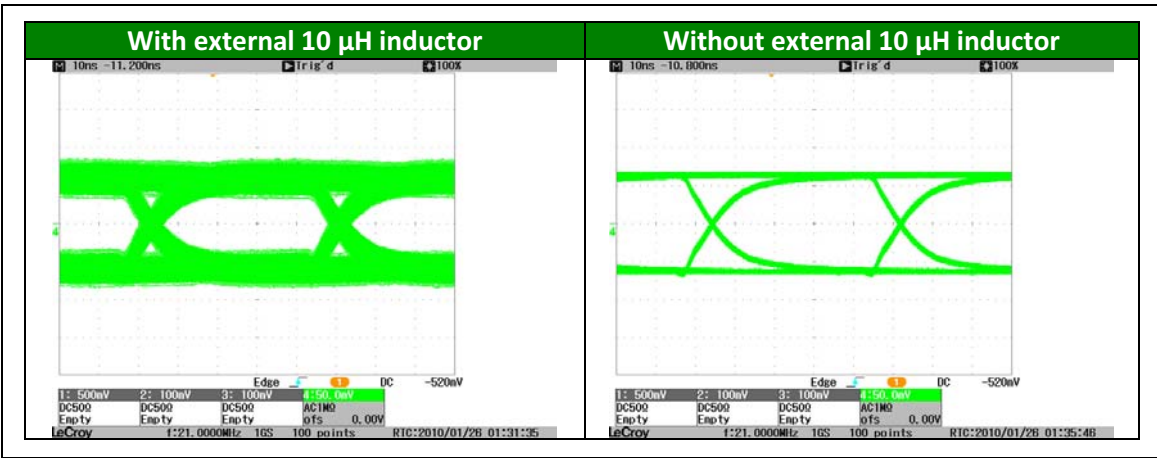
All measurements at VCC = 1.2V, Temp = +25°C, data pattern = 8B/10B test pattern at 21 Mbps, typical R_{amp} and R_{rise}, measured into 75Ω.

FIGURE C-1: SIGNAL TRANSMITTED BY LOW-SPEED DRIVER SHOWING BASLINE WANDER DUE TO EXTERNAL 10 μH INDUCTOR AND FERRITE BEADS⁽¹⁾



- 1: Inductor and ferrite beads at the camera side of the link will double the baseline wandering. This is resolved by the LF-Receiver in the EQCO62T20 chip.

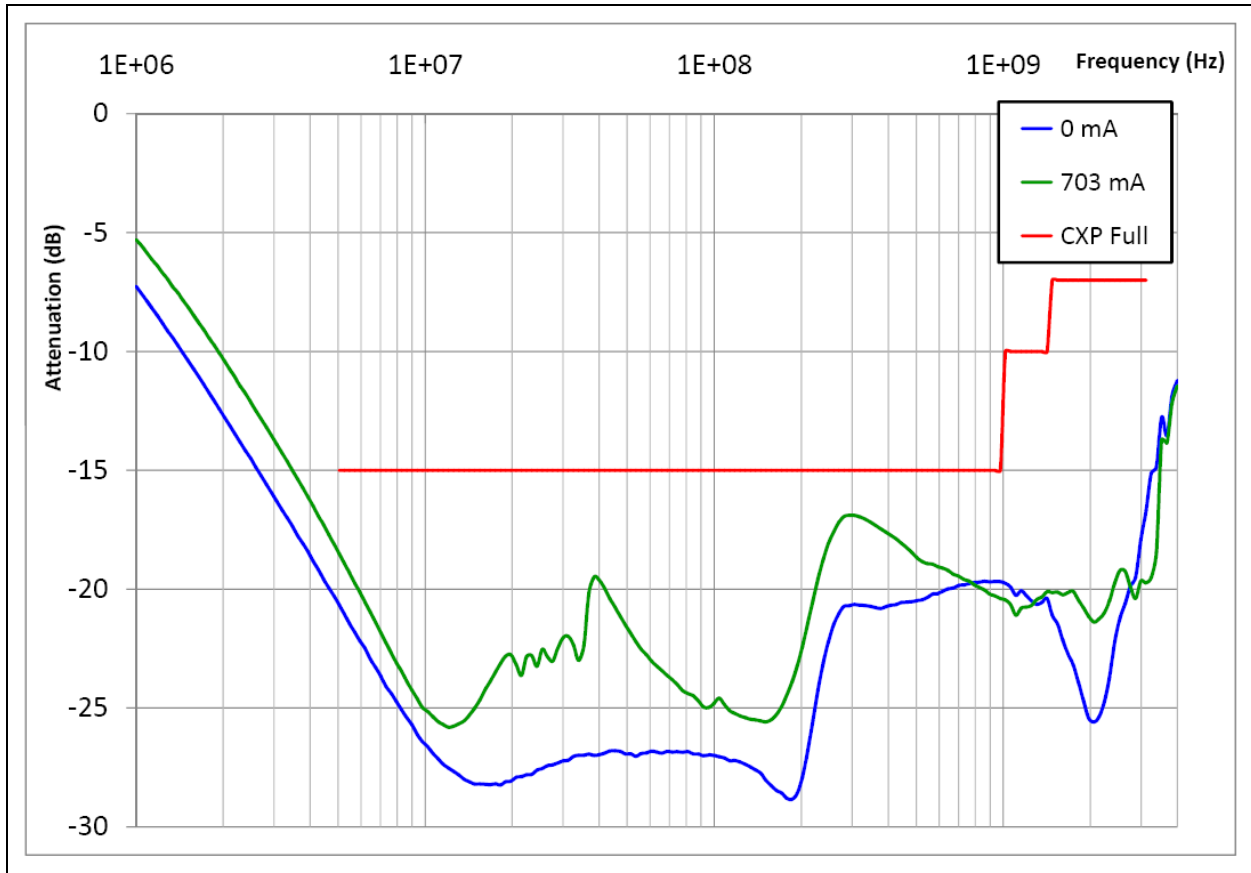
FIGURE C-2: OUTPUT EYE OF LF DRIVER WITH AND WITHOUT EXTERNAL 10 MH INDUCTOR



APPENDIX D: TYPICAL RETURN-LOSS

Figure D-1 shows the return-loss at the BNC connector of the EQCO62R20.3 evaluation board as shown in [Section 2.0 “Application Information”](#) with supply current of 0 mA and 703 mA (maximum supply current for CoaXPress) through the inductor (L1) and the ferrite beads (Fb1 & Fb2) and compares it with the CoaXPress (Full-Speed) return-loss specification.

FIGURE D-1: RETURN-LOSS OF THE EQCO62R20.3 BNC EVALUATION BOARD WITH AND WITHOUT SUPPLY CURRENT



EQCO62R20.3/EQCO31R20.3

APPENDIX E: FOOTPRINTS USED FOR THE MULTILANE COAXPRESS LAYOUT

FIGURE E-1: 0402, 0603 AND VIA WITH THERMAL ISOLATION FOOTPRINTS

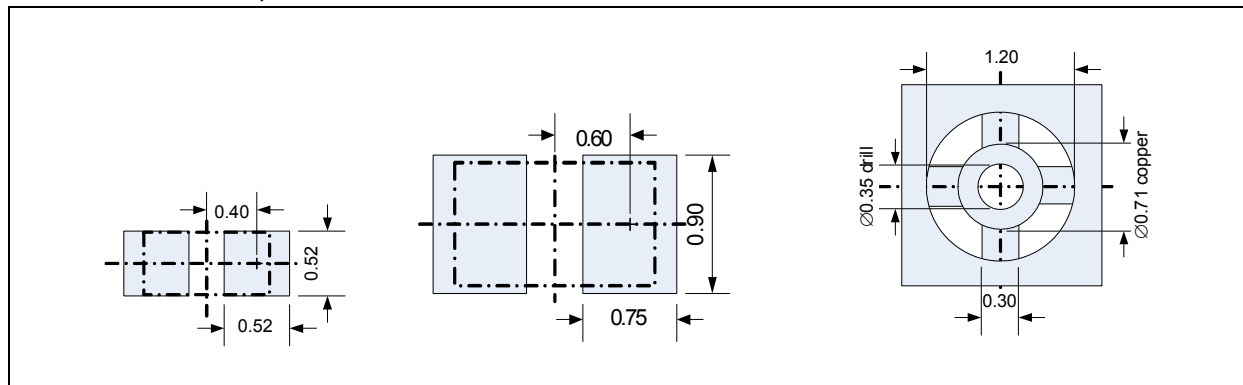


FIGURE E-2: DIN1.0/2.3 AND L1 INDUCTOR 1812 FOOTPRINTS

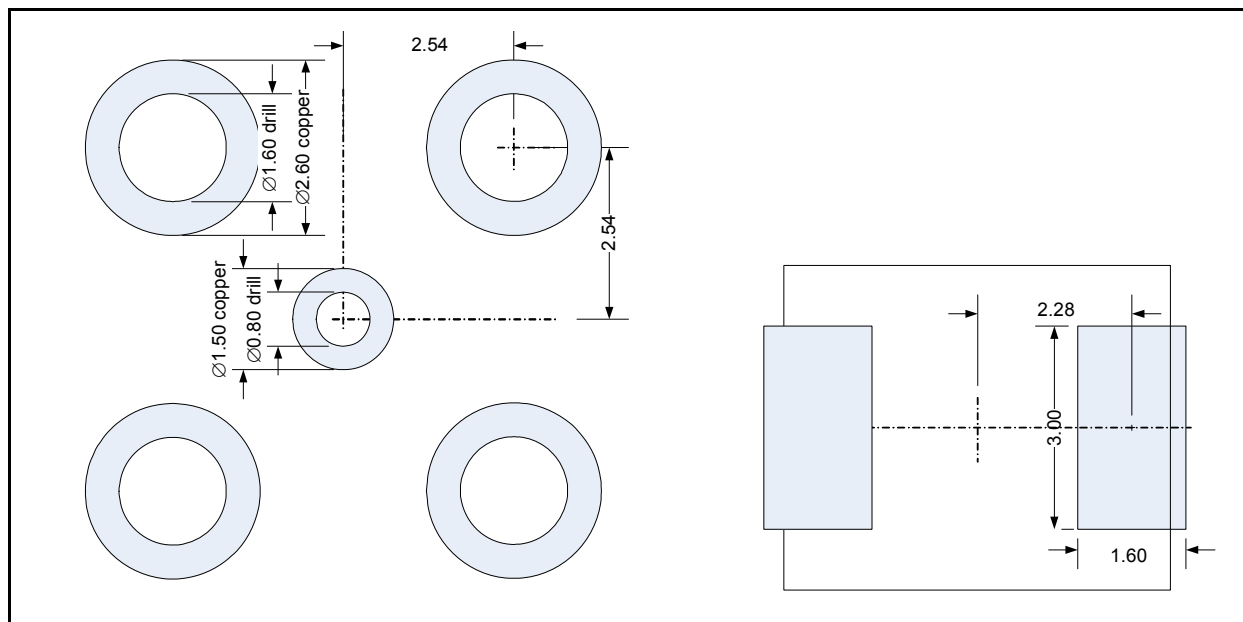


TABLE E-1: COMPONENT POSITIONS OF [Figure 2-4](#)

Component	Footprint	X	Y	Angle	
NPF 4076	DIN1.0/2.3	0	0	—	Bottom
EQCO62R20.3	QFN	-0.075	-8	—	
C1 (50V)	0603	0.075	-2.55	90°	
C2	0402	2.4	-4.9	90°	
R1 (16Ω)	0402	0.25	-4.575	90°	
R2 (91Ω)	0402	-1.2	-5	—	
FB1	0603	-2.05	0.6	—	
FB2	0603	-2.05	-0.6	—	
R6	0402	4.075	0.35	—	
C7 (50V)	0402	4.475	1.850	90°	
C9	0402	1.675	-11.025	—	
C10	0402	2.05	-4.9	—	

EQCO62R20.3/EQCO31R20.3

Component	Footprint	X	Y	Angle	
L1	1812	4.5	-7.6	90°	Bottom
C8 (50V)	0603	-0.725	-8.425	—	Bottom
C5	0402	-0.125	-7.175	—	Bottom

TABLE E-2: VIA POSITIONS OF Figure 2-4

VIA	Thermal	X	Y	Connected To
1	—	4.1	-4.1	Top-Bottom
2	—	4.825	-4.1	Top-Bottom
3	Not Isolated	-1.725	-5.975	Top-GND-Bottom
4	Not Isolated	1.7	-6.425	Top-Power-Bottom
5	—	-2.9	-7.025	Top-Bottom
6	Isolated	1.65	-9.9	Top-GND-Bottom
7	Isolated	1.575	-9.7	Top-GND
8	Not Isolated	2.375	-10.175	Top-Power

TABLE E-3: GROUND AND VCC PLANE POSITION OF Figure 2-4

GND Plane Coordinates	X	Y	VCC Plane Coordinates	X	Y
A	-2.475	-9.1	N	-2.475	-9.125
B	-2.475	-3.1	O	-2.475	-6.875
C	-1.25	-3.1	P	0.75	-6.875
D	-1.25	-6.125	Q	0.75	-6.05
E	-0.475	-6.9	R	2.475	-6.05
F	0.85	-6.9	S	2.475	-9.125
G	0.85	-5.975			
H	1.05	-5.775			
I	1.05	-3.1			
J	-2.475	-3.1			
K	2.475	-9.1			
L	-0.9	-9.075	T	-0.9	-9.075
M	0.75	-10.725	U	0.75	-10.725

FIGURE E-3: TRACK DIMENSIONS OF Figure 2-4

Track	Width	
1	0.3	QFN.1 to Tab (GND)
2	0.4	QFN.1 to C10 (GND)
3	0.3	QFN.2 (SDIp)
4	0.2	QFN.3 (SDIn)
5	0.3	QFN.4 (GND)
6	0.2	QFN.5 (LFin)
7	0.2	QFN.6 (ampR)
8	0.2	QFN.7 (riseR)
9	0.3	QFN.9 (GND)
10	100Ω Diff. ⁽¹⁾	QFN.10-11 (SDIp-SDIn)
11	0.3	QFN.12 to V8/Tab (GND)

Note 1: Width and spaces between lines needs to be calculated based on PCB layer stack. Impedance should be 100Ω differential.

EQCO62R20.3/EQCO31R20.3

FIGURE E-3: TRACK DIMENSIONS OF Figure 2-4

Track	Width	
12	0.4	QFN.12 to C9 (GND)
13	0.4	QFN.13 (VCC)
14	0.5	C9 to V9 (VCC)
15	0.5	QFN.16
16	0.4	C2 to DIN1.0/2.3
17	0.7	C10 to DIN1.0/2.3
18	0.3	R1
19	0.4	C1 to DIN1.0/2.3
20	0.4/0.7	FB
21	0.2	C7
22	0.5	Bottom Tracks

Note 1: Width and spaces between lines needs to be calculated based on PCB layer stack. Impedance should be 100Ω differential.

TABLE E-4: COMPONENT POSITIONS OF Figure 2-5

Component	Footprint	X	Y	Angle	
NPF 4076	DIN1.0/2.3	0	0	—	Bottom
EQCO62R20.3	QFN	-0.075	-7.725	—	
C1 (50V)	0603	0.5	-2	90°	
C2	0402	-0.75	-2.4	90°	
R1 (16Ω)	0402	0.5	-4.05	90°	
R2 (91Ω)	0402	-0.8	-4.05	90°	
C5	0402	-2.4	-4.925	—	
C9	0402	2.925	-9.1	90°	
C10	0402	2.225	-4.925	—	Bottom

TABLE E-5: VIA POSITIONS OF Figure 2-5

VIA	Thermal	X	Y	Connected To
1	Isolated	-2.8	-5.625	Top-Power
2	Not Isolated	-1.675	-5.65	Top-GND
3	Not Isolated	1.6	-5.65	Top-GND
4	Not Isolated	2.325	-6.225	Top-Power
5	Isolated	2.675	-8	Top-Power
6	Isolated	-1.65	-9.5	Top-GND
7	Isolated	1.55	-9.5	Top-GND

EQCO62R20.3/EQCO31R20.3

TABLE E-6: GROUND PLANE POSITION OF Figure 2-5

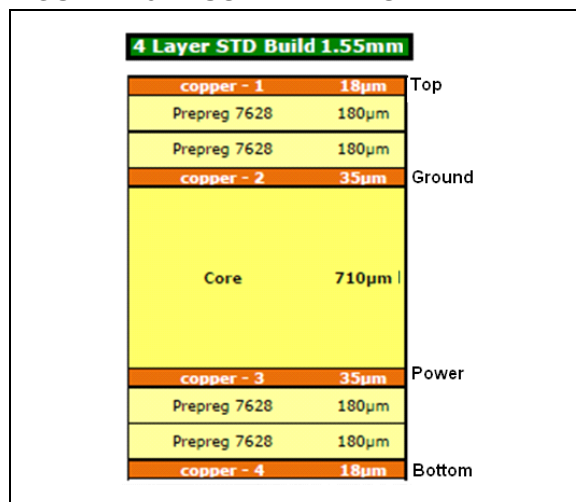
GND Plane Coordinates	X	Y	VCC Plane Coordinates	X	Y
a	-1.725	3.75	m	-2.3	-3.475
b	-1.725	-3	n	-2.3	-6.65
c	-2.25	-3	o	1.75	-6.65
d	-2.25	-5.2	p	1.75	-5.575
e	-0.425	-7	q	2.85	-5.575
f	0.225	-7	r	2.85	-10.075
g	1.65	-5.575			
h	1.65	-3			
i	2.85	-3			
j	2.85	-10.075			
k	-0.9	-8.8	s	-0.9	-8.8
l	0.75	-10.45	t	0.75	-10.45

FIGURE E-4: TRACK WIDTHS OF Figure 2-5

Track	Width	
1	0.3	QFN.1; QFN.4 (GND)
2	0.3	QFN.2 (SDIp)
3	0.3	QFN.3 (SDIn)
4	0.2	QFN.5 (LFin)
5	0.2	QFN.6 (ampR)
6	0.2	QFN.7 (riseR)
7	0.3	QFN.9; QFN.12 (GND)
8	100Ω Diff. ⁽¹⁾	QFN.10-11 (SDIp-SDIn)
9	0.5	QFN.13; QFN.16 (VCC)
10	0.5	C9; C10; C5
11	0.4	C1; C2

Note 1: Width and spaces between lines need to be calculated based on PCB layer stack. Impedance should be 100Ω differential.

FIGURE E-5: USED LAYER STACK



THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

EQCO62R20.3/EQCO31R20.3

PRODUCT IDENTIFICATION SYSTEM

To order parts, including industrial, or obtain information, for e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>I</u>	<u>RM</u>	<u>XXX</u>
Device	Temp. Range	Radio Module	Firmware Revision Number
Device: EQCO62R20.3 Temperature Range: I = -40°C to +85°C (Industrial temperature) Package: TRAY = Tray (Blank) = Tube			
Examples: a) EQCO62R20.3 = Industrial temperature, 16-Lead QFN Tube packaging b) EQCO62R20.3-TRAY = Industrial temperature, 16-Lead QFN Tray packaging			

EQCO62R20.3/EQCO31R20.3

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KeeLoq, Kleeer, LANCheck, LINK MD, maXtremus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntellIMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A. Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleeerNet, KleeerNet logo, memBrain, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2018, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-3687-4

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microchip:](#)

[EQCO62R20.3](#)