USB7206

6-Port USB 3.1 Gen 2 Controller Hub

Highlights

- 6-Port USB Smart Hub with:
  - Five Standard USB 3.1 Gen 2 downstream ports
  - One Standard USB 2.0 downstream port
  - Internal Hub Feature Controller device which enables:
    - USB to I^2C/SPI/I^2S/GPIO bridge endpoint support
    - USB to internal hub register write and read
- USB Link Power Management (LPM) support
- USB-IF Battery Charger revision 1.2 support on downstream ports (DCP, CDP, SDP)
- Enhanced OEM configuration options available through either OTP or SPI ROM
- Available in 100-pin (12mm x 12mm) VQFN RoHS compliant package
- Commercial and industrial grade temperature support

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.1 Gen 2 Peripherals

Key Benefits

- USB 3.1 Gen 2 compliant 10 Gbps, 5 Gbps, 480 Mbps, 12 Mbps, and 1.5Mbps operation
  - 5V tolerant USB 2.0 pins
  - 1.21V tolerant USB 3.1 Gen 2 pins
  - Integrated termination and pull-up/down resistors
- Supports battery charging of most popular battery powered devices on all ports
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006/2009 charger emulation
  - European Union universal mobile charger support
  - Supports additional portable devices
- On-chip Microcontroller
  - manages I/Os, VBUS, and other signals
- 96kB RAM, 256kB ROM
- 8kB One-Time-Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI external memory, or SMBus
- **USB Bridging**
  - USB to I^2C, SPI, I^2S, and GPIO
- **PortSwap**
  - Configurable USB 2.0 differential pair signal swap
- **PHYBoost**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense**
  - Programmable USB receive sensitivity
- **PortSplit**
  - USB 2.0 and USB 3.1 Gen 2 port operation can be split for custom applications using embedded USB 3.x devices in parallel with USB 2.0 devices
- Compatible with Microsoft Windows 10, 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- 100-pin VQFN package (12mm x 12mm)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DFP	Downstream Facing Port
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UFP	Upstream Facing Port
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input.
IS	Input with Schmitt trigger.
O12	Output buffer with 12 mA sink and 12 mA source.
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.
A	Analog.
P	Power pin.

1.3 Reference Documents

1. *Universal Serial Bus Revision 3.1 Specification*, http://www.usb.org
2. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
3. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com/documents/user_manual/UM10204.pdf
4. *I^2S-Bus Specification*, http://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

Note: Additional USB7206 resources can be found on the Microchip USB7206 product page at www.microchip.com/USB7206.

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2.0 INTRODUCTION

2.1 General Description

The Microchip USB7206 hub is a low-power, OEM configurable, USB 3.1 Gen 2 hub controller with 6 downstream ports and advanced features for embedded USB applications. The USB7206 is fully compliant with the Universal Serial Bus Revision 3.1 Specification and USB 2.0 Link Power Management Addendum. The USB7206 supports 10 Gbps SuperSpeed+ (SS+), 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on five standard USB 3.1 Gen 2 downstream ports and only legacy speeds (HS/FS/LS) on one standard USB 2.0 downstream port.

The USB7206 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub controller that is the culmination of seven generations of Microchip hub feature controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub controller operates in parallel with the USB 2.0 controller, decoupling the 10/5 Gbps SS+/SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB7206 enables OEMs to configure their system using “Configuration Straps.” These straps simplify the configuration process assigning default values to USB 3.1 Gen 2 ports and GPIOs. OEMs can disable ports, enable battery charging and define GPIO functions as default assignments on power up removing the need for OTP or external SPI ROM.

The USB7206 supports downstream battery charging. The USB7206 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB7206 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

• DCP: Dedicated Charging Port (Power brick with no data)

• CDP: Charging Downstream Port (1.5A with data)

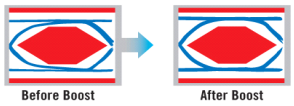
• SDP: Standard Downstream Port (0.5A[USB 2.0]/0.9A[USB 3.1] with data)

Additionally, the USB7206 includes many powerful and unique features such as:

The Hub Feature Controller, an internal USB device dedicated for use as a USB to I^2C/SPI/GPIO interface that allows external circuits or devices to be monitored, controlled, or configured via the USB interface.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment.



VariSense, which controls the Hi-Speed USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

Port Split, which allows for the USB 3.1 Gen 2 and USB 2.0 portions of downstream ports 3, 4, and 5 to operate independently and enumerate two separate devices in parallel in special applications.

The USB7206 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility and are available as GPIOs for customer specific use.

The USB7206 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB7206 in an upstream Type-B application is shown in Figure 2-1.

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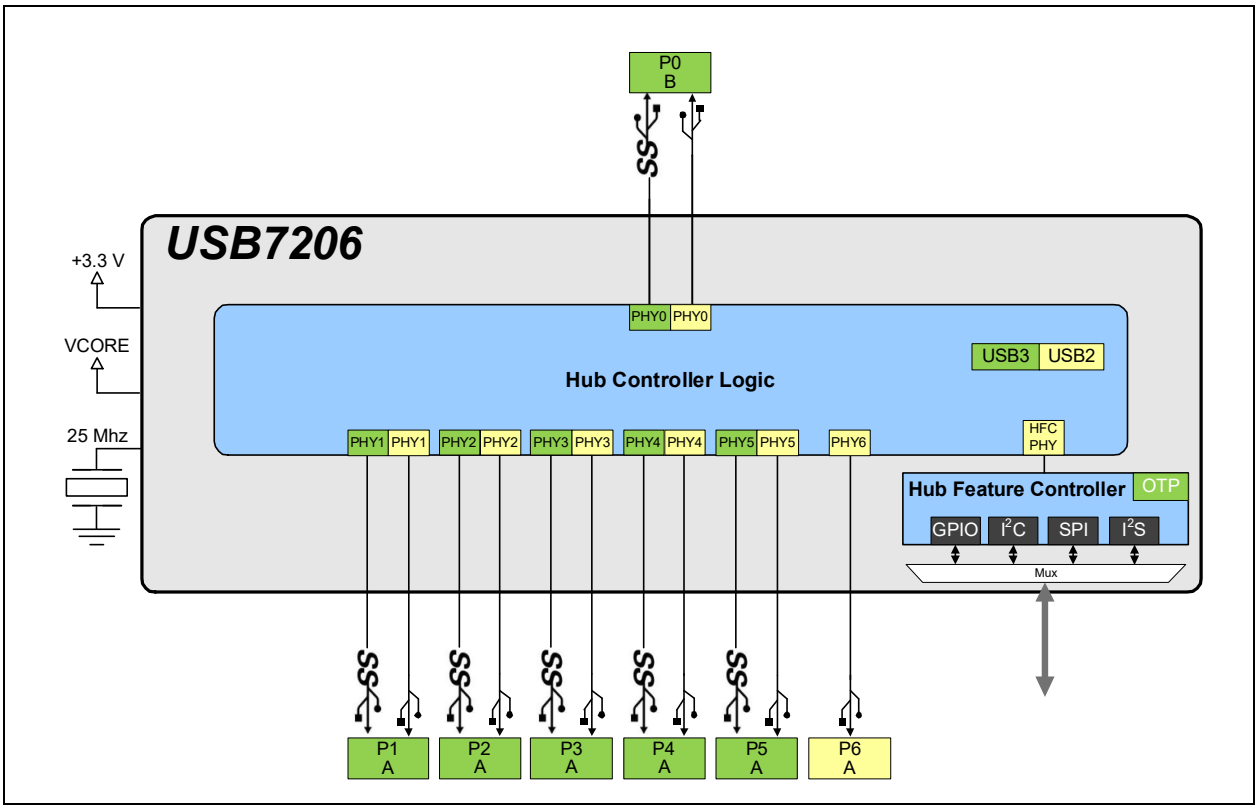
FIGURE 2-1: USB7206 INTERNAL BLOCK DIAGRAM - UPSTREAM TYPE-B APPLICATION



Note: All port numbering in this document is LOGICAL port numbering with the device in the default configuration. LOGICAL port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The PHYSICAL port number is the port number with respect to the physical PHY on the chip. PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. Refer to the “Configuration of USB7202/USB7206/USB725x” application note for details on the LOGICAL vs. PHYSICAL mapping and additional configuration details.

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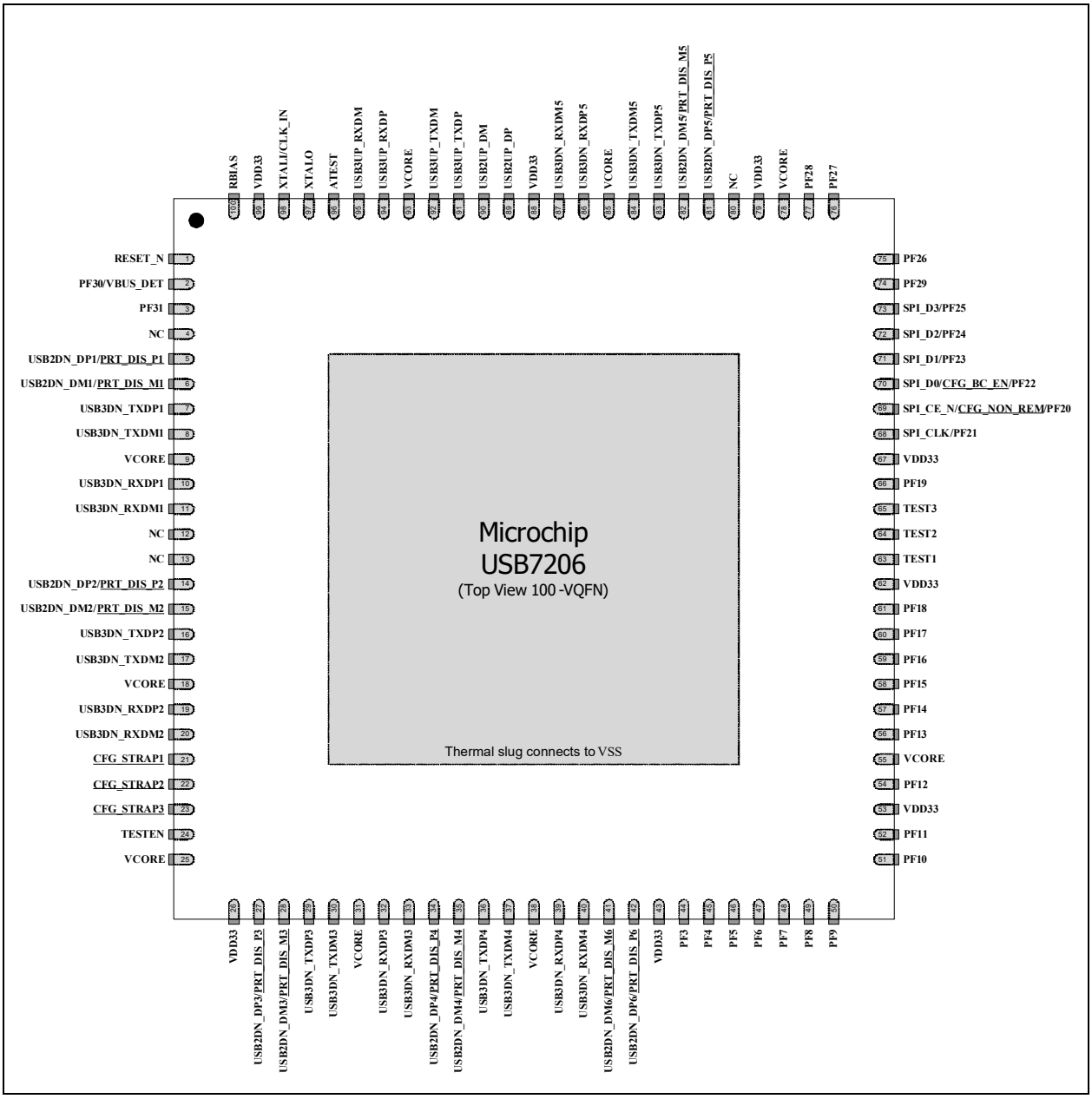
3.0 PIN DESCRIPTIONS

3.1 Pin Assignments

FIGURE 3-1: USB7206 100-VQFN PIN ASSIGNMENTS



Note:	Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

Pin Num	Pin Name	Pin Num	Pin Name
1	RESET_N	51	PF10
2	PF30/VBUS_DET	52	PF11
3	PF31	53	VDD33
4	NC	54	PF12
5	USB2DN_DP1/PRT_DIS_P1	55	VCORE
6	USB2DN_DM1/PRT_DIS_M1	56	PF13
7	USB3DN_TXDP1	57	PF14
8	USB3DN_TXDM1	58	PF15
9	VCORE	59	PF16
10	USB3DN_RXDP1	60	PF17
11	USB3DN_RXDM1	61	PF18
12	NC	62	VDD33
13	NC	63	TEST1
14	USB2DN_DP2/PRT_DIS_P2	64	TEST2
15	USB2DN_DM2/PRT_DIS_M2	65	TEST3
16	USB3DN_TXDP2	66	PF19
17	USB3DN_TXDM2	67	VDD33
18	VCORE	68	SPI_CLK/PF21
19	USB3DN_RXDP2	69	SPI_CE_N/CFG_NON_REM/PF20
20	USB3DN_RXDM2	70	SPI_D0/CFG_BC_EN/PF22
21	CFG_STRAP1	71	SPI_D1/PF23
22	CFG_STRAP2	72	SPI_D2/PF24
23	CFG_STRAP3	73	SPI_D3/PF25
24	TESTEN	74	PF29
25	VCORE	75	PF26
26	VDD33	76	PF27
27	USB2DN_DP3/PRT_DIS_P3	77	PF28
28	USB2DN_DM3/PRT_DIS_M3	78	VCORE
29	USB3DN_TXDP3	79	VDD33
30	USB3DN_TXDM3	80	NC
31	VCORE	81	USB2DN_DP5/PRT_DIS_P5
32	USB3DN_RXDP3	82	USB2DN_DM5/PRT_DIS_M5
33	USB3DN_RXDM3	83	USB3DN_TXDP5
34	USB2DN_DP4/PRT_DIS_P4	84	USB3DN_TXDM5
35	USB2DN_DM4/PRT_DIS_M4	85	VCORE
36	USB3DN_TXDP4	86	USB3DN_RXDP5
37	USB3DN_TXDM4	87	USB3DN_RXDM5
38	VCORE	88	VDD33
39	USB3DN_RXDP4	89	USB2UP_DP
40	USB3DN_RXDM4	90	USB2UP_DM
41	USB2DN_DM6/PRT_DIS_M6	91	USB3UP_TXDP
42	USB2DN_DP6/PRT_DIS_P6	92	USB3UP_TXDM
43	VDD33	93	VCORE
44	PF3	94	USB3UP_RXDP
45	PF4	95	USB3UP_RXDM
46	PF5	96	ATEST
47	PF6	97	XTALO
48	PF7	98	XTALI/CLK_IN
49	PF8	99	VDD33
50	PF9	100	RBIAS
Exposed Pad (VSS) must be connected to ground.			

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3.2 Pin Descriptions

This section contains descriptions of the various USB7206 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Buffer type definitions are detailed in Section 1.2, Buffer Types.

TABLE 3-1: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 2 Interfaces			
Upstream USB 3.1 Gen 2 TX D+	**USB3UP_TXDP**	I/O-U	Upstream USB 3.1 Gen 2 Transmit Data Plus.
Upstream USB 3.1 Gen 2 TX D-	**USB3UP_TXDM**	I/O-U	Upstream USB 3.1 Gen 2 Transmit Data Minus.
Upstream USB 3.1 Gen 2 RX D+	**USB3UP_RXDP**	I/O-U	Upstream USB 3.1 Gen 2 Receive Data Plus.
Upstream USB 3.1 Gen 2 RX D-	**USB3UP_RXDM**	I/O-U	Upstream USB 3.1 Gen 2 Receive Data Minus.
Downstream Ports 1-5 USB 3.1 Gen 2 TX D+	**USB3DN_TXDP[1:5]**	I/O-U	Downstream SuperSpeed+ Transmit Data Plus, ports 1 through 5.
Downstream Ports 1-5 USB 3.1 Gen 2 TX D-	**USB3DN_TXDM[1:5]**	I/O-U	Downstream SuperSpeed+ Transmit Data Minus, ports 1 through 5.
Downstream Ports 1-5 USB 3.1 Gen 2 RX D+	**USB3DN_RXDP[1:5]**	I/O-U	Downstream SuperSpeed+ Receive Data Plus, ports 1 through 5.
Downstream Ports 1-5 USB 3.1 Gen 2 RX D-	**USB3DN_RXDM[1:5]**	I/O-U	Downstream SuperSpeed+ Receive Data Minus, ports 1 through 5.
USB 2.0 Interfaces			
Upstream USB 2.0 D+	**USB2UP_DP**	I/O-U	Upstream USB 2.0 Data Plus (D+).
Upstream USB 2.0 D-	**USB2UP_DM**	I/O-U	Upstream USB 2.0 Data Minus (D-).
Downstream Ports 1-6 USB 2.0 D+	**USB2DN_DP[1:6]**	I/O-U	Downstream USB 2.0 Ports 1-6 Data Plus (D+).
Downstream Ports 1-6 USB 2.0 D-	**USB2DN_DM[1:6]**	I/O-U	Downstream USB 2.0 Ports 1-6 Data Minus (D-)

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TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

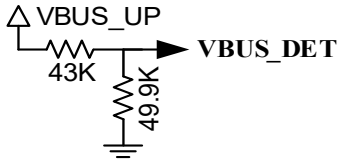
Name	Symbol	Buffer Type	Description
VBUS Detect	**VBUS_DET**	IS	This signal detects the state of the upstream bus power. Externally, VBUS can be as high as 5.25 V, which can be damaging to this pin. The amplitude of VBUS must be reduced by a voltage divider. The recommended voltage divider is shown below.  For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
SPI Interface			
SPI Clock	**SPI_CLK**	I/O-U	SPI clock. If the SPI interface is enabled, this pin must be driven low during reset.
SPI Data 3-0	**SPI_D[3:0]**	I/O-U	SPI Data 3-0. If the SPI interface is enabled, these signals function as Data 3 through 0.
SPI Chip Enable	**SPI_CE_N**	I/O12	Active low SPI chip enable input. If the SPI interface is enabled, this pin must be driven high in powerdown states.
Miscellaneous			
Programmable Function Pins	**PF[31:3]**	I/O12	Programmable function pins.
Test 1	**TEST1**	A	Test 1 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.
Test 2	**TEST2**	A	Test 2 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.
Test 3	**TEST3**	A	Test 3 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.
Reset Input	**RESET_N**	IS	This active low signal is used by the system to reset the device.

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TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Bias Resistor	**RBIAS**	I-R	A 12.0 kΩ ±1.0% resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close the device as possible with a dedicated, low impedance connection to the ground plane.
Test	**TESTEN**	I/O12	Test pin. This signal is used for test purposes and must always be connected to ground.
Analog Test	**ATEST**	A	Analog test pin. This signal is used for test purposes and must always be left unconnected.
External 25 MHz Crystal Input	**XTALI**	ICLK	External 25 MHz crystal input
External 25 MHz Reference Clock Input	**CLK_IN**	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
External 25 MHz Crystal Output	**XTALO**	OCLK	External 25 MHz crystal output
No Connect	**NC**	-	No connect. For proper operation, this pin must be left unconnected.
Configuration Straps			
Port 6-1 D+ Disable Configuration Strap	**PRT_DIS_P[6:1]**	I	Port 6-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[6:1]** straps to disable the related port (6-1). See Note 3-1. Both USB data pins for the corresponding port must be tied to 3.3V to disable the associated downstream port.
Port 6-1 D- Disable Configuration Strap	**PRT_DIS_M[6:1]**	I	Port 6-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[6:1]** straps to disable the related port (6-1). See Note 3-1. Both USB data pins for the corresponding port must be tied to 3.3V to disable the associated downstream port.
Non-Removable Ports Configuration Strap	**CFG_NON_REM**	I	Non-Removable Ports Configuration Strap. This configuration strap controls the number of reported non-removable ports. See Note 3-1.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Battery Charging Configuration Strap	CFG_BC_EN	I/O12	Battery Charging Configuration Strap. This configuration strap controls the number of BC 1.2 enabled downstream ports. See Note 3-1.
Device Mode Configuration Straps 3-1	CFG_STRAP[3:1]	I	Device Mode Configuration Straps 3-1. These configuration straps are used to select the device's mode of operation. See Note 3-1.
Power/Ground			
+3.3V I/O Power Supply Input	VDD33	P	+3.3 V power and internal regulator input.
Digital Core Power Supply Input	VCORE	P	Digital core power supply input.
Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

Note 3-1 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. For additional information, refer to Section 3.3, Configuration Straps and Programmable Functions.

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3.3 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following deassertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note:	The system designer must guarantee that configuration straps meet the timing requirements specified in Section 9.6.2, Power-On and Configuration Strap Timing and Section 9.6.3, Reset and Configuration Strap Timing. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.3.1 PORT DISABLE CONFIGURATION (PRT_DIS_P[6:1] / PRT_DIS_M[6:1])

The **PRT_DIS_P[6:1]** / **PRT_DIS_M[6:1]** configuration straps are used in conjunction to disable the related port (6-1)

For **PRT_DIS_P*x*** (where *x* is the corresponding port 6-1):

0 = Port *x* D+ Enabled

1 = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 6-1):

0 = Port *x* D- Enabled

1 = Port *x* D- Disabled

Note:	Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where ***x*** is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.0 port.

3.3.2 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The **CFG_NON_REM** configuration strap is used to configure the non-removable port settings of the device to one of six settings. These modes are selected by the configuration of an external resistor on the **CFG_NON_REM** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-2.

TABLE 3-2: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	**Setting**
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Ports 1, 2 non-removable
10 kΩ Pull-Up	Ports 1, 2, 3 non-removable
10 Ω Pull-Down	Ports 1, 2, 3, 4 non-removable
10 Ω Pull-Up	Ports 1, 2, 3, 4, 5, 6 non-removable

3.3.3 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The **CFG_BC_EN** configuration strap is used to configure the battery charging port settings of the device to one of six settings. These modes are selected by the configuration of an external resistor on the **CFG_BC_EN** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-3.

TABLE 3-3: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	Battery charging not enable on any port
200 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Port 1
10 kΩ Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2
10 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3
10 Ω Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4
10 Ω Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4, 5, 6

3.3.4 PF[31:3] CONFIGURATION (CFG_STRAP[2:1])

The USB7206 provides 29 programmable function pins (**PF[31:3]**). These pins can only be configured to 1 predefined configuration via the **CFG_STRAP[2:1]** pins. This configuration is selected via external resistors on the **CFG_STRAP[2:1]** pins, as detailed in Table 3-4. Resistor values and combinations not detailed in Table 3-4 are reserved and should not be used.

Note: **CFG_STRAP3** is not used and must be pulled-down to ground via a 200 kΩ resistor.

TABLE 3-4: CFG_STRAP[2:1] RESISTOR ENCODING

Mode	CFG_STRAP2 Resistor Value	CFG_STRAP1 Resistor Value
Configuration 3	200 kΩ Pull-Down	10 kΩ Pull-Down

Note: Configurations 1 and 2 are not used in the USB7206.

A summary of the configuration pin assignments is provided in Table 3-5. For details on behavior of each programmable function, refer to Table 3-6.

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TABLE 3-5: PF[31:3] FUNCTION ASSIGNMENT

Pin	Configuration 3
PF3	I2S_SDI
PF4	I2S_SDO
PF5	I2S_SCK
PF6	I2S_LRCK
PF7	I2S_MCLK
PF8	NC
PF9	NC
PF10	PRT_CTL3_U3
PF11	PRT_CTL4_U3
PF12	PRT_CTL5_U3
PF13	PRT_CTL5
PF14	PRT_CTL4
PF15	PRT_CTL3
PF16	PRT_CTL2
PF17	PRT_CTL1
PF18	MSTR_I2C_CLK
PF19	MIC_DET
PF20	SPI_CE_N
PF21	SPI_CLK
PF22	SPI_D0
PF23	SPI_D1
PF24	SPI_D2
PF25	SPI_D3
PF26	SLV_I2C_CLK
PF27	SLV_I2C_DATA
PF28	PRT_CTL6
PF29	GPIO93
PF30	VBUS_DET
PF31	MSTR_I2C_DATA

Note: The default **PF*x*** pin functions can be overridden with additional configuration by modification of the pin mux registers. These changes can be made during the SMBus configuration stage, by programming to OTP memory, or during runtime (after hub has attached and enumerated) by register writes via the SMBus slave interface or USB commands to the internal Hub Feature Controller Device.

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS

Function	Buffer Type	Description
Master SMBus/I²C Interface		
MSTR_I2C_CLK	I/O12	Bridging Master SMBus/I²C controller clock (SMBus/I²C controller 1)
MSTR_I2C_DATA	I/O12	Bridging Master SMBus/I²C controller data (SMBus/I²C controller 1)
Slave SMBus/I²C Interface		
SLV_I2C_CLK	I/O12	Slave SMBus/I²C controller clock (SMBus/I²C controller 2)
SLV_I2C_DATA	I/O12	Slave SMBus/I²C controller data (SMBus/I²C controller 2)
SPI Interface		
SPI_CLK	I/O-U	SPI clock. If the SPI interface is enabled, this pin must be driven low during reset.
SPI_D[3:0]	I/O-U	SPI Data 3-0. If the SPI interface is enabled, these signals function as Data 3 through 0.
SPI_CE_N	I/O12	Active low SPI chip enable input. If the SPI interface is enabled, this pin must be driven high in powerdown states.
I²S Interface		
I2S_SDI	I	I²S Serial Data In
I2S_SDO	O12	I²S Serial Data Out
I2S_SCK	O12	I²S Continuous Serial Clock
I2S_LRCK	O12	I²S Word Select / Left-Right Clock
I2S_MCLK	O12	I²S Master Clock
MIC_DET	I	I²S Microphone Plug Detect 0 = No microphone plugged into the audio jack 1 = Microphone plugged into the audio jack
Miscellaneous		
PRT_CTL6	I/O12 (PU)	Port 6 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 6. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** This signal controls both the USB 2.0 and USB 3.1 portions of the port.

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TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description
PRT_CTL5	I/O12 (PU)	Port 5 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 5. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.
PRT_CTL4	I/O12 (PU)	Port 4 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 4. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.
PRT_CTL3	I/O12 (PU)	Port 3 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 3. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.
PRT_CTL2	I/O12 (PU)	Port 2 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 2. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description
PRT_CTL1	I/O12 (PU)	Port 1 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 1. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.1 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only.
PRT_CTL5_U3	O12	Port 5 USB 3.1 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.1 portion of the downstream port 5 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.1 device.
PRT_CTL4_U3	O12	Port 4 USB 3.1 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.1 portion of the downstream port 4 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.1 device.
PRT_CTL3_U3	O12	Port 3 USB 3.1 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.1 portion of the downstream port 3 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.1 device.
GPIO93	I/O12	General Purpose Input/Output

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3.4 Physical and Logical Port Mapping

The USB72xx family of devices are based upon a common architecture, but all have different modifications and/or pin bond outs to achieve the various device configurations. The base chip is composed of a total of 6 USB3 PHYs and 7 USB2 PHYs. These PHYs are physically arranged on the chip in a certain way, which is referred to as the PHYSICAL port mapping.

The actual port numbering is remapped by default in different ways on each device in the family. This changes the way that the ports are numbered from the USB host's perspective. This is referred to as LOGICAL mapping.

The various configuration options available for these devices may, at times, be with respect to PHYSICAL mapping or LOGICAL mapping. Each individual configuration option which has a PHYSICAL or LOGICAL dependency is declared as such within the register description.

The PHYSICAL vs. LOGICAL mapping is described for all port related pins in Table 3-7. A system design in schematics and layout is generally performed using the pinout in Section 3.1, Pin Assignments, which is assigned by the default LOGICAL mapping. Hence, it may be necessary to cross reference the PHYSICAL vs. LOGICAL look up tables when determining the hub configuration.

Note:	The MPLAB Connect tool makes configuration simple; the settings can be selected by the user with respect to the LOGICAL port numbering. The tool handles the necessary linking to the PHYSICAL port settings. Refer to Section 6.0, Device Configuration for additional information.

TABLE 3-7: USB7206 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER							PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	6	0	1	2	3	4	5	6
5	USB2DN_DP1		X							X					
6	USB2DN_DM1		X							X					
7	USB3DN_TXDP1		X							X					
8	USB3DN_TXDM1		X							X					
10	USB3DN_RXDP1		X							X					
11	USB3DN_RXDM1		X							X					
14	USB2DN_DP2			X							X				
15	USB2DN_DM2			X							X				
16	USB3DN_TXDP2			X							X				
17	USB3DN_TXDM2			X							X				
19	USB3DN_RXDP2			X							X				
20	USB3DN_RXDM2			X							X				
27	USB2DN_DP3				X							X			
28	USB2DN_DM3				X							X			
29	USB3DN_TXDP3				X							X			
30	USB3DN_TXDM3				X							X			
32	USB3DN_RXDP3				X							X			
33	USB3DN_RXDM3				X							X			
34	USB2DN_DP4					X							X		
35	USB2DN_DM4					X							X		
36	USB3DN_TXDP4					X							X		
37	USB3DN_TXDM4					X							X		
39	USB3DN_RXDP4					X							X		
40	USB3DN_RXDM4					X							X		
41	USB2DN_DM6							X							X
42	USB2DN_DP6							X							X
81	USB2DN_DP5						X							X	
82	USB2DN_DM5						X							X	
83	USB3DN_TXDP5						X							X	
84	USB3DN_TXDM5						X							X	
86	USB3DN_RXDP5						X							X	
87	USB3DN_RXDM5						X							X	
89	USB2UP_DP	X							X						
90	USB2UP_DM	X							X						
91	USB3UP_TXDP	X							X						
92	USB3UP_TXDM	X							X						
94	USB3UP_RXDP	X							X						
95	USB3UP_RXDM	X							X						

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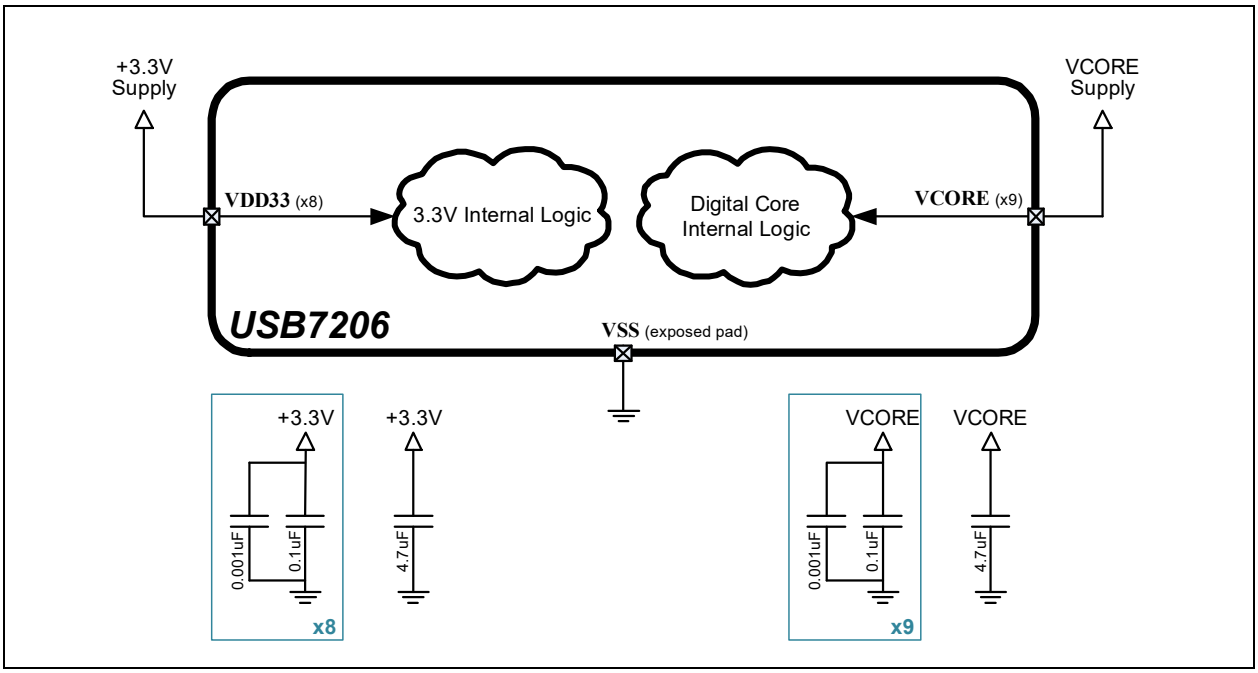
4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

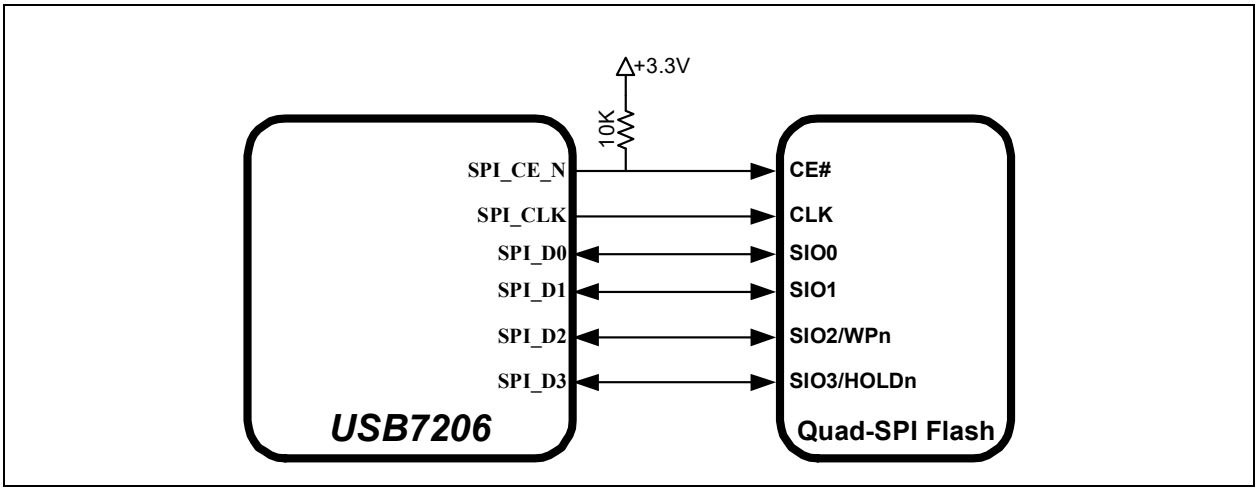
FIGURE 4-1: POWER CONNECTIONS



4.2 SPI Flash Connections

Figure 4-2 illustrates the Quad-SPI flash connections.

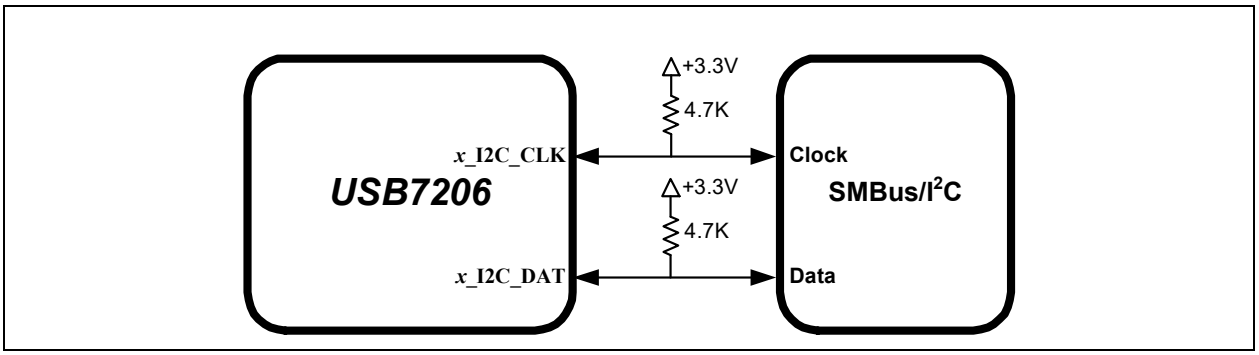
FIGURE 4-2: QUAD-SPI FLASH CONNECTIONS



4.3 SMBus/I2C Connections

Figure 4-3 illustrates the SMBus/I2C connections.

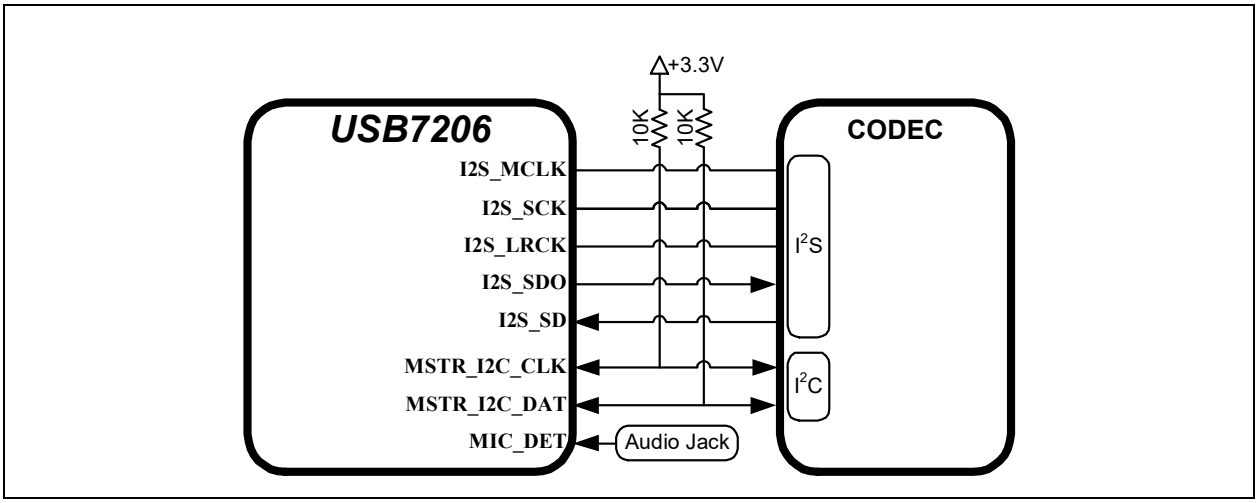
FIGURE 4-3: SMBUS/I2C CONNECTIONS



4.4 I2S Connections

Figure 4-4 illustrates the I2S connections.

FIGURE 4-4: I2S CONNECTIONS



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5.0 MODES OF OPERATION

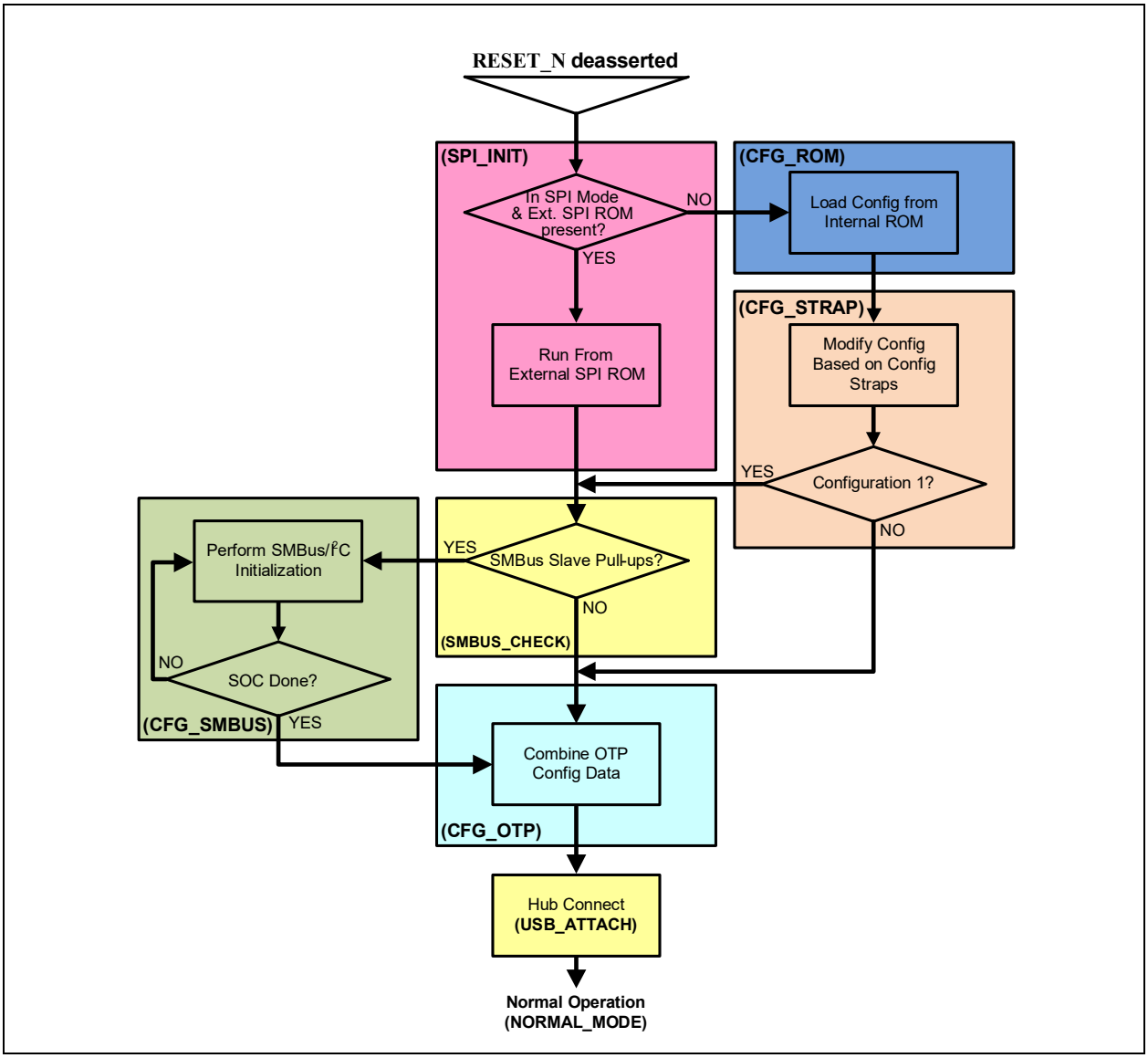
The device provides two main modes of operation: Standby Mode and Hub Mode. These modes are controlled via the RESET_N pin, as shown in Table 5-1.

TABLE 5-1: MODES OF OPERATION

RESET_N Input	Summary
0	**Standby Mode**: This is the lowest power mode of the device. No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance and the PLL is halted. Refer to Section 8.8, Resets for additional information on RESET_N.
1	**Hub (Normal) Mode**: The device operates as a configurable USB hub. This mode has various sub-modes of operation, as detailed in Figure 5-1. Power consumption is based on the number of active ports, their speed, and amount of data received.

The flowchart in Figure 5-1 details the modes of operation and details how the device traverses through the Hub Mode stages (shown in bold). The remaining sub-sections provide more detail on each stage of operation.

FIGURE 5-1: HUB MODE FLOWCHART



5.1 Boot Sequence

5.1.1 STANDBY MODE

If the **RESET_N** pin is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all downstream ports are disabled, the USB data pins are held in a high-impedance state, all transactions immediately terminate (no states saved), all internal registers return to their default state, the PLL is halted, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after **RESET_N** is negated high.

5.1.2 SPI INITIALIZATION STAGE (SPI_INIT)

The first stage, the initialization stage, occurs on the deassertion of **RESET_N**. In this stage, the internal logic is reset, the PLL locks if a valid clock is supplied, and the configuration registers are initialized to their default state. The internal firmware then checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of "2DFU" (device firmware upgrade) beginning at address 0x3FFFA. If a valid signature is found, then the external SPI ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM (CFG_ROM stage).

The required SPI ROM must be a minimum of 1 Mbit, and 60 MHz or faster. Both 1, 2, and 4-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMs are also supported.

If the system is not strapped for SPI Mode, code execution will continue from internal ROM (CFG_ROM stage).

5.1.3 CONFIGURATION FROM INTERNAL ROM STAGE (CFG_ROM)

In this stage, the internal firmware loads the default values from the internal ROM. Most of the hub configuration registers, USB descriptors, electrical settings, etc. will be initialized in this state.

5.1.4 CONFIGURATION STRAP READ STAGE (CFG_STRAP)

In this stage, the firmware reads the following configuration straps to override the default values:

- **CFG_STRAP[3:1]**
- **PRT_DIS_P[6:1]**
- **PRT_DIS_M[6:1]**
- **CFG_NON_REM**
- **CFG_BC_EN**

If the **CFG_STRAP[3:1]** pins are set to Configuration 1, the device will move to the SMBUS_CHECK stage, otherwise it will move to the CFG_OTP stage. Refer to Section 3.3, Configuration Straps and Programmable Functions for information on usage of the various device configuration straps.

5.1.5 SMBUS CHECK STAGE (SMBUS_CHECK)

Based on the **PF[31:3]** configuration selected (refer to Section 3.3.4, PF[31:3] Configuration (CFG_STRAP[2:1])), the firmware will check for the presence of external pull up resistors on the SMBus slave programmable function pins. If 10K pull-ups are detected on both pins, the device will be configured as an SMBus slave, and the next state will be CFG_SMBUS. If a pull-up is not detected in either of the pins, the next state is CFG_OTP.

5.1.6 SMBUS CONFIGURATION STAGE (CFG_SMBUS)

In this stage, the external SMBus master can modify any of the default configuration settings specified in the integrated ROM, such as USB device descriptors, port electrical settings, and control features such as downstream battery charging.

There is no time limit on this mode. In this stage the firmware will wait indefinitely for the SMBus/I^2C configuration. The external SMBus master writes to register 0xFF to end the configuration in legacy mode. In non-legacy mode, the SMBus command USB_ATTACH (opcode 0xAA55) or USB_ATTACH_WITH_SMBUS (opcode 0xAA56) will finish the configuration.

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5.1.7 OTP CONFIGURATION STAGE (CFG_OTP)

Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.

5.1.8 HUB CONNECT STAGE (USB_ATTACH)

Once the hub registers are updated through default values, SMBus master, and OTP, the device firmware will enable attaching the USB host by setting the USB_ATTACH bit in the HUB_CMD_STAT register (for USB 2.0) and the USB3_HUB_ENABLE bit (for USB 3.1). The device will remain in the Hub Connect stage indefinitely.

5.1.9 NORMAL MODE (NORMAL_MODE)

Lastly, the hub enters Normal Mode of operation. In this stage full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.

If **RESET_N** is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated hub stages. Asserting a soft disconnect on the upstream port will cause the hub to return to the Hub Connect stage until the soft disconnect is negated.

6.0 DEVICE CONFIGURATION

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. Microchip provides a comprehensive software programming tool, MPLAB Connect Configurator (formerly ProTouch2), for OTP configuration of various USB7206 functions and registers. All configuration is to be performed via the MPLAB Connect Configurator programming tool. For additional information on this tool, refer to the MPLAB Connect Configurator programming tool product page at http://www.microchip.com/design-centers/usb/mplab-connect-configurator.

Additional information on configuring the USB7206 is also provided in the "*Configuration of the USB7202/USB725x*" application note, which contains details on the hub operational mode, SOC configuration stage, OTP configuration, USB configuration, and configuration register definitions. This application note, along with additional USB7206 resources, can be found on the Microchip USB7206 product page at www.microchip.com/USB7206.

Note:	Device configuration straps and programmable pins are detailed in Section 3.3, Configuration Straps and Programmable Functions. Refer to Section 7.0, Device Interfaces for detailed information on each device interface.

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7.0 DEVICE INTERFACES

The USB7206 provides multiple interfaces for configuration, external memory access, etc.. This section details the various device interfaces:

- SPI/SQI Master Interface
- SMBus/I2C Master/Slave Interfaces
- I2S Interface

Note: For details on how to enable each interface, refer to Section 3.3, Configuration Straps and Programmable Functions.

For information on device connections, refer to Section 4.0, Device Connections. For information on device configuration, refer to Section 6.0, Device Configuration.

Microchip provides a comprehensive software programming tool, MPLAB Connect Configurator (formerly ProTouch2), for configuring the USB7206 functions, registers and OTP memory. All configuration is to be performed via the MPLAB Connect Configurator programming tool. For additional information on this tool, refer to th MPLAB Connect Configurator programming tool product page at http://www.microchip.com/design-centers/usb/mplab-connect-configurator.

7.1 SPI/SQI Master Interface

The SPI/SQI controller has two basic modes of operation: execution of an external hub firmware image, or the USB to SPI bridge. On power up, the firmware looks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0x3FFFA. If a valid signature is found, then the external ROM mode is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM and the SPI interface can be used as a USB to SPI bridge.

The second mode of operation is the USB to SPI bridge operation. Additional details on this feature can be found in Section 8.6, USB to SPI Bridging.

Table 7-1 details how the associated pins are mapped in SPI vs. SQI mode

TABLE 7-1: SPI/SQI PIN USAGE

SPI Mode	SQI Mode	Description
SPI_CE_N	SQI_CE_N	SPI/SQI Chip Enable (Active Low)
SPI_CLK	SQI_CLK	SPI/SQI Clock
SPI_D0	SQI_D0	SPI Data Out; SQI Data I/O 0
SPI_D1	SQI_D1	SPI Data In; SQI Data I/O 1
-	SQI_D2	SQI Data I/O 2
-	SQI_D3	SQI Data I/O 3

Note: For SPI/SQI master timing information, refer to Section 9.6.8, SPI/SQI Master Timing.

7.2 SMBus/I2C Master/Slave Interfaces

The device provides three independent SMBus/I2C controllers (Slave, and Master) which can be used to access internal device run time registers or program the internal OTP memory. The device contains two 128 byte buffers to enable simultaneous master/slave operation and to minimize firmware overhead in processed I2C packets. The I2C interfaces support 100KHz Standard-mode (Sm) and 400KHz Fast Mode (Fm) operation.

The SMBus/I2C interfaces are assigned to programmable pins (**PF*x***). Refer to Section 3.3.4, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

Note: For SMBus/I2C timing information, refer to Section 9.6.5, SMBus Timing and Section 9.6.6, I2C Timing.

7.3 I2S Interface

The device provides an integrated I2S interface to facilitate the connection of digital audio devices. The I2S interface conforms to the voltage, power, and timing characteristics/specifications as set forth in the *I2S-Bus Specification*, and consists of the following signals:

- **I2S_SDI**: Serial Data Input
- **I2S_SDO**: Serial Data Output
- **I2S_SCK**: Serial Clock
- **I2S_LRCK**: Left/Right Clock (SS/FSYNC)
- **I2S_MCLK**: Master Clock
- **MIC_DET**: Microphone Plug Detect

Each audio connection is half-duplex, so **I2S_SDO** exists only on the transmit side and **I2S_SDI** exists only on the receive side of the interface. Some codecs refer to the Serial Clock (**I2S_SCK**) as Baud/Bit Clock (BCLK). Also, the Left/Right Clock is commonly referred to as LRC or LRCK. The I2S and other audio protocols refer to LRC as Word Select (WS).

The following codec is supported by default:

- Analog Devices ADAU1961 (24-bit 96KHz)

The I2S interface is assigned to programmable pins (**PF*x***). Refer to Section 3.3.4, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

Note: For I2S timing information, refer to Section 9.6.7, I2S Timing. For detailed information on utilizing the I2S interface, including support for other codecs, refer to the application note "*USB7202/USB725x I2S Operation*", which can be found on the Microchip USB7206 product page at www.microchip.com/USB7206.

7.3.1 MODES OF OPERATION

The USB audio class operates in three ways: Asynchronous, Synchronous and Adaptive. There are also multiple operating modes, such as hi-res, streaming, etc.. Typically for USB devices, inputs such as microphones are Asynchronous, and output devices such as speakers are Adaptive. The hardware is set up to handle all three modes of operation. It is recommended that the following configuration be used: Asynchronous IN; Adaptive OUT; 48Khz streaming mode; Two channels: 16 bits per channel.

7.3.1.1 Asynchronous IN 48KHz Streaming

In this mode, the codec sampling clock is set to 48Khz based on the local oscillator. This clock is never changed. The data from the codec is fed into the input FIFO. Since the sampling clock is asynchronous to the host clock, the amount of data captured in every USB frame will vary. This issue is left for the host to handle. The input FIFO has two markers, a low water mark (THRESHOLD_LOW_VAL), and a high water mark (THRESHOLD_HIGH_VAL). There are three registers to determine how much data to send back in each frame. If the amount of data in the FIFO exceeds the high water mark, then HI_PKT_SIZE worth of data is sent. If the data is between the high and low water mark, the normal MID_PKT_SIZE amount of data is sent. If the data is below the low water mark, LO_PKT_SIZE worth of data is sent.

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7.3.1.2 Adaptive OUT 48KHz Streaming

In this mode, the codec sampling clock is initially set to 48Khz based on the local oscillator. The host data is fed into the OUT FIFO. The host will send the same amount of data on every frame, i.e. 48KHz of data based on the host clock. The codec sampling clock is asynchronous to the host clock. This will cause the amount of data in the OUT FIFO to vary. If the amount of data in the FIFO exceeds the high water mark, then the sampling clock is increased. If the data is between the high and low water mark, the sampling clock does not change. If the data is below the low water mark, the sampling clock is decreased.

7.3.1.3 Synchronous Operation

For synchronous operation, the internal clock must be synchronized with the host SOF. The Frame SOF is nominally 1mS. Since there is significant jitter in the SOFs, there is circuitry provided to measure the SOFs over a long period of time to get a more accurate reading. The calculated host frequency is used to calculate the codec sampling clock.

8.0 FUNCTIONAL DESCRIPTIONS

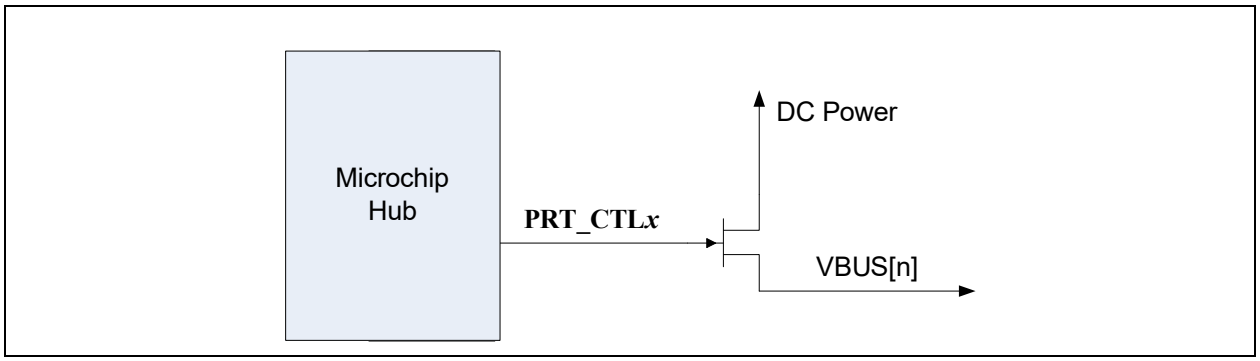
This section details various USB7206 functions, including:

- Downstream Battery Charging
- Port Power Control
- PortSplit
- USB to GPIO Bridging
- USB to I2C Bridging
- USB to SPI Bridging
- Link Power Management (LPM)
- Resets

8.1 Downstream Battery Charging

The device can be configured by an OEM to have any of the downstream ports support battery charging. The hub's role in battery charging is to provide acknowledgment to a device's query as to whether the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided externally by the OEM.

FIGURE 8-1: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply from the device. This indication, via the **PRT_CTL*x*** pins, is on a per port basis. For example, the OEM can configure two ports to support battery charging through high current power FETs and leave the other two ports as standard USB ports.

The port control signals are assigned to programmable pins (**PF*x***) and therefore the device must be programmed into specific configurations to enable the signals. Refer to Section 3.3.4, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

For detailed information on utilizing the battery charging feature, refer to the application note "*USB Battery Charging with Microchip USB7202 and USB725x Hubs*", which can be found on the Microchip USB7206 product page www.microchip.com/USB7206.

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8.2 Port Power Control

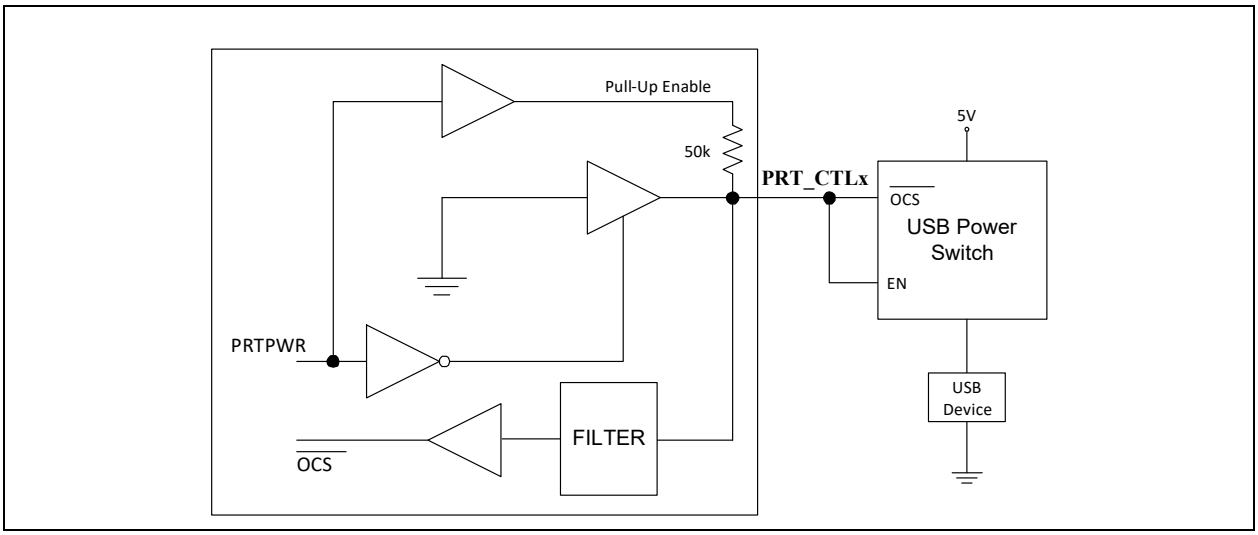
Port power and over-current sense share the same pin (**PRT_CTLx**) for each port. These functions can be controlled directly from the USB hub, or via the processor.

Note:	The **PRT_CTLx** function is assigned to programmable function pins (**PFx**) via configuration straps. Refer to Section 3.3.4, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

8.2.1 PORT POWER CONTROL USING USB POWER SWITCH

When operating in combined mode, the device will have one port power control and over-current sense pin for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the pull-up resistor will be disabled at that time. When port power is enabled, it will disable the output driver and enable the pull-up resistor, making it an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmidt trigger input will recognize that as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions such as low voltage while the device is powering up.

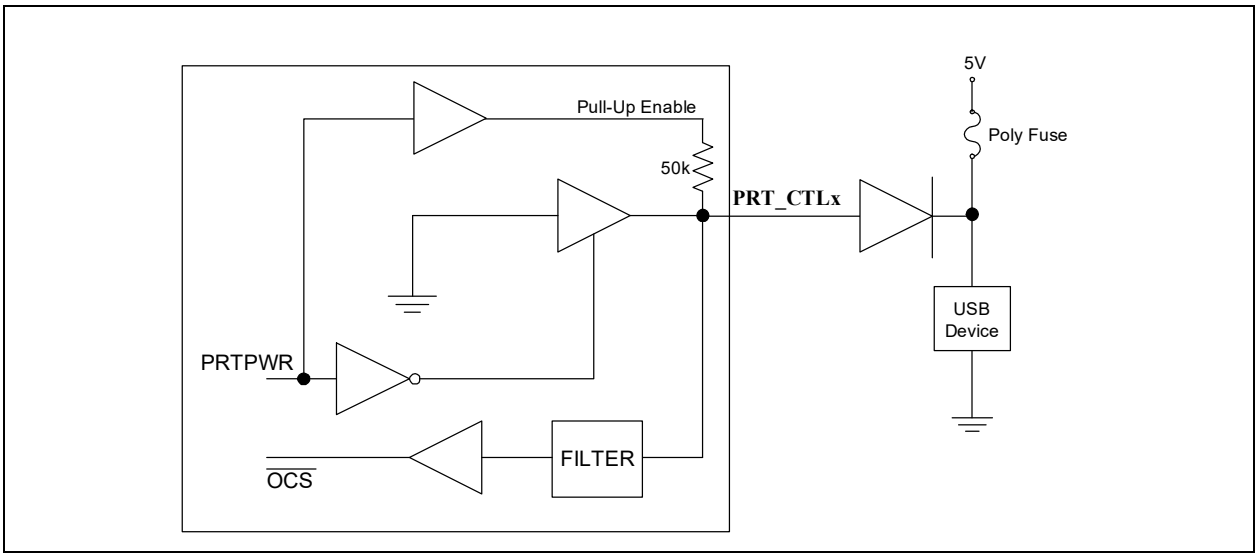
FIGURE 8-2: PORT POWER CONTROL WITH USB POWER SWITCH



8.2.2 PORT POWER CONTROL USING POLY FUSE

When using the device with a poly fuse, there is no need for an output power control. A single port power control and over-current sense for each downstream port is still used from the Hub's perspective. When disabling port power, the driver will actively drive a '0'. This will have no effect as the external diode will isolate pin from the load. When port power is enabled, it will disable the output driver and enable the pull-up resistor. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to 0 volts. The anode of the diode will be at 0.7 volts, and the Schmidt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

FIGURE 8-3: PORT POWER CONTROL USING A POLY FUSE



8.3 PortSplit

The PortSplit feature allows the USB 2.0 and USB 3.1 PHYs associated with a downstream port to be operationally separated. The intention of this feature is to allow a system designer to connect an embedded USB 3.x device to the USB 3.1 PHY, while allowing the USB 2.0 PHY to be used as either a standard USB 2.0 port or with a separate embedded USB 2.0 device. PortSplit can be configured via OTP/SMBus. By default, all ports are configured to non-split mode.

When PortSplit is disabled on a specific port, the corresponding **PRT_CTL*x*** pin controls both the USB 2.0 and USB 3.1 portions of the port (port power and overcurrent condition). When PortSplit is enabled on a specific port, the corresponding **PRT_CTL*x*** pin controls the USB 2.0 portion of the port, and the corresponding **PRT_CTL*x*_U3** pin controls the USB 3.1 portion of the port.

8.4 USB to GPIO Bridging

The USB to GPIO bridging feature provides system designers expanded system control and potential BOM reduction. General Purpose Input/Outputs (GPIOs) may be used for any general 3.3V level digital control and input functions.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Set the direction of the GPIO (input or output)
- Enable a pull-up resistor
- Enable a pull-down resistor
- Read the state
- Set the state

For detailed information on utilizing the USB to GPIO bridging feature, refer to the application note "*USB to GPIO Bridging with Microchip USB7202 and USB725x Hubs*", which can be found on the Microchip USB7206 product page at www.microchip.com/USB7206.

8.5 USB to I^{2}C Bridging

The USB to I^{2}C bridging feature provides system designers expanded system control and potential BOM reduction. The use of a separate USB to I^{2}C device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to I^{2}C device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Configure I^{2}C Pass-Through Interface

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- I^2C Write
- I^2C Read

For detailed information on utilizing the USB to I^2C bridging feature, refer to the application note "*USB to I^2C Bridging with Microchip USB7202 and USB725x Hubs*", which can be found on the Microchip USB7206 product page at www.microchip.com/USB7206.

8.6 USB to SPI Bridging

The USB to SPI bridging feature provides system designers expanded system control and potential BOM reduction. The use of a separate USB to SPI device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to SPI device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable SPI Pass-Through Interface
- SPI Write/Read
- Disable SPI Pass-Through Interface

For detailed information on utilizing the USB to SPI bridging feature, refer to the application note "*USB to SPI Bridging with Microchip USB7202 and USB725x Hubs*", which can be found on the Microchip USB7206 product page at www.microchip.com/USB7206.

8.7 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 8-1.

TABLE 8-1: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms (from start of RESUME)
L1	Sleep	Entry: <10 us Exit: <50 us
L0	Fully Enabled (On)	-

8.8 Resets

The device includes the following chip-level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

8.8.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 9.6.2, Power-On and Configuration Strap Timing.

8.8.2 EXTERNAL CHIP RESET (RESET_N)

A valid hardware reset is defined as assertion of **RESET_N**, after all power supplies are within operating range, per the specifications in Section 9.6.3, Reset and Configuration Strap Timing. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of **RESET_N** causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.

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2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note:	All power supplies must have reached the operating levels mandated in Section 9.2, Operating Conditions**, prior to (or coincident with) the assertion of **RESET_N**.

8.8.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

1. Sets default address to 0.
2. Sets configuration to Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with the USB Specification for behavior after completion of a reset sequence.

The host then configures the device in accordance with the USB Specification.

Note:	The device does not propagate the upstream USB reset to downstream devices.

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9.0 OPERATIONAL CHARACTERISTICS

9.1 Absolute Maximum Ratings*

Digital Core Supply Voltage (**VCORE**) (Note 1) . . . . . -0.5 V to +1.21 V

+3.3 V Supply Voltage (**VDD33**) (Note 1) . . . . . -0.5 V to +4.6 V

Positive voltage on input signal pins, with respect to ground (Note 2) . . . . . +4.6 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Positive voltage on **XTALI/CLK_IN**, with respect to ground . . . . . +3.63 V

Positive voltage on USB DP/DM signal pins, with respect to ground . . . . . +6.0 V

Positive voltage on USB 3.1 Gen 2 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** signal pins, with respect to ground . . . . . 1.21 V

Storage Temperature . . . . . -55°C to +150°C

Junction Temperature . . . . . +125°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . ***TBD***

Note 1: When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 2: This rating does not apply to the following pins: All USB DM/DP pins, **XTAL1/CLK_IN**, and **XTALO**

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 9.2, Operating Conditions**, Section 9.5, DC Specifications, or any other applicable section of this specification is not implied.

9.2 Operating Conditions**

Digital Core Supply Voltage (**VCORE**) . . . . . +1.09 V to +1.21 V

+3.3 V Supply Voltage (**VDD33**) . . . . . +3.0 V to +3.6 V

Input Signal Pins Voltage (Note 2) . . . . . -0.3 V to +3.6 V

XTALI/CLK_IN Voltage . . . . . -0.3 V to +3.6 V

USB 2.0 DP/DM Signal Pins Voltage . . . . . -0.3 V to +5.5 V

USB 3.1 Gen 2 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** Signal Pins Voltage . . . . . -0.3 V to +1.21 V

Ambient Operating Temperature in Still Air (T_A) . . . . . Note 3

Digital Core Supply Voltage Rise Time (T_{RT} in Figure 9-1). . . . . 400 µs

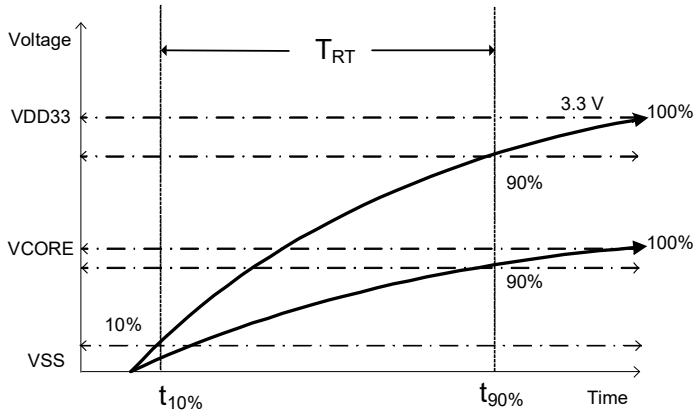
+3.3 V Supply Voltage Rise Time (T_{RT} in Figure 9-1) . . . . . 400 µs

Note 3: 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

Note:	Do not drive input signals without power supplied to the device.

FIGURE 9-1: SUPPLY RISE TIME MODEL



9.3 Package Thermal Specifications

TABLE 9-1: PACKAGE THERMAL PARAMETERS

Symbol	°C/W	Velocity (Meters/s)
Θ_{JA}	19	0
	16	1
	14	2.5
Ψ_{JT}	0.1	0
	0.1	1
Ψ_{JB}	9	0
Θ_{JC}	1.3	0
	1.3	1
Θ_{JB}	10	-

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51. For industrial applications, the USB7206 requires multi-layer 2S4P PCB power dissipation.

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9.4 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

TABLE 9-2: DEVICE POWER CONSUMPTION

	Typical (mA) @ 25°C		Typical Power
	VCORE	VDD33	(mW)
Global Suspend	6.68	2.32	18
No VBUS	7.1	2.6	17
Reset	5.24	0.48	24
Active Idle			
5 SS+ Ports, 1 HS Port	472	22.7	618
4 SS+ Ports, 1 SS Port, 1 HS Port	428	22.7	568
3 SS+ Ports, 2 SS Ports, 1 HS Port	454	22.7	598
2 SS+ Ports, 3 SS Ports, 1 HS Port	445	22.7	587
1 SS+ Port, 4 SS Ports, 1 HS Port	436	22.7	577
Active Data Transfer			
5 SS+ Ports, 1 HS Port	1245	110	1795
4 SS+ Ports, 1 SS Port, 1 HS Port	1076	110	1601
3 SS+ Ports, 2 SS Ports, 1 HS Port	1151	110	1687
2 SS+ Ports, 3 SS Ports, 1 HS Port	1104	110	1633
1 SS+ Port, 4 SS Ports, 1 HS Port	1057	110	1579
Formula for Estimating Active Current			
SS+ Current	(No. of Ports*130) +530	(No. of Ports* 9) +39	
SS Current	(No. of Ports*90) +490	(No. of Ports* 5) +36	
HS Current	(No. of Ports*0.5) +59	(No. of Ports* 4) +24	

Note: In the Active Idle and Active Data Transfer sections of Table 9-2, the various port configurations are indicated via the following acronyms:
SS+ = USB 3.1 SuperSpeed+ (Gen 2)
SS = USB 3.1 SuperSpeed (Gen 1)
HS = USB 2.0 High Speed

9.5 DC Specifications

TABLE 9-3: I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Notes
I Type Input Buffer						
Low Input Level	V_{IL}			Note 4	V	
High Input Level	V_{IH}	1.25			V	
IS Type Input Buffer						
Low Input Level	V_{IL}			Note 4	V	
High Input Level	V_{IH}	1.25			V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	100	160	240	mV	
O12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -12 mA
OD12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
ICLK Type Input Buffer (XTALI Input)						Note 5
Low Input Level	V_{IL}			0.35	V	
High Input Level	V_{IH}	0.9		1.1	V	
IO-U Type Buffer (See Note 6)						Note 6

Note 4: 0.42V for interface using open drain with pull-ups to voltages up to 2.1V, 0.34V for interface using open drain with pull-ups to voltages greater than 2.1V.

Note 5: **XTALI** can optionally be driven from a 25 MHz singled-ended clock oscillator.

Note 6: Refer to the USB 3.1 Gen 2 Specification for USB DC electrical characteristics.

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9.6 AC Specifications

This section details the various AC timing specifications of the device.

9.6.1 POWER SUPPLY AND RESET_N SEQUENCE TIMING

Figure 9-2 illustrates the recommended power supply sequencing for the device. **VCORE** should rise after or at the same time as **VDD33**. Similarly, **RESET_N** and/or **VBUS_DET** should rise after or at the same time as **VDD33**. **VBUS_DET** and **RESET_N** do not have any other timing dependencies. The rise times for **VCORE** and **VDD33** are provided in Section 9.2, Operating Conditions** and Figure 9-1.

FIGURE 9-2: POWER SUPPLY AND RESET_N SEQUENCE TIMING

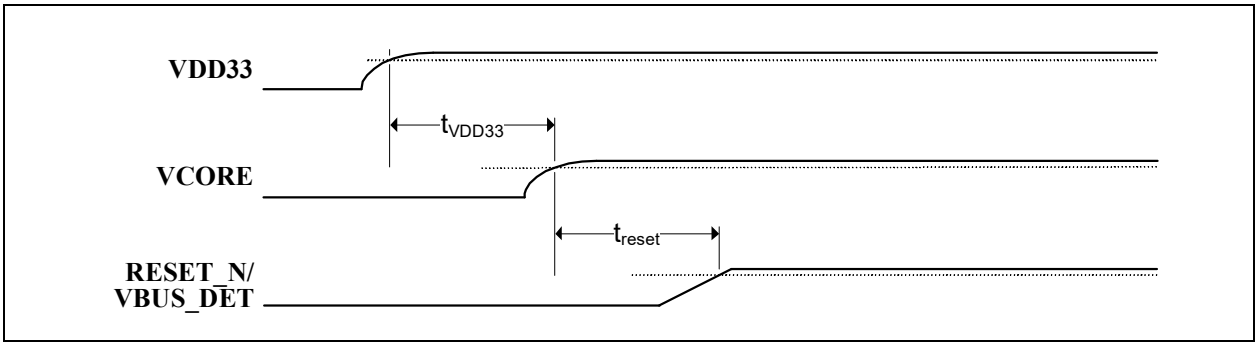

TABLE 9-4: POWER SUPPLY AND RESET_N SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{VDD33}	**VDD33** to **VCORE** rise delay	0			ms
t_{reset}	**VDD33** to **RESET_N/VBUS_DET** rise delay	0			ms

9.6.2 POWER-ON AND CONFIGURATION STRAP TIMING

Figure 9-3 illustrates the configuration strap valid timing requirements in relation to power-on, for applications where **RESET_N** is not used at power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met. The operational levels (V_{opp}) for the external power supplies are detailed in Section 9.2, Operating Conditions**.

FIGURE 9-3: POWER-ON CONFIGURATION STRAP VALID TIMING

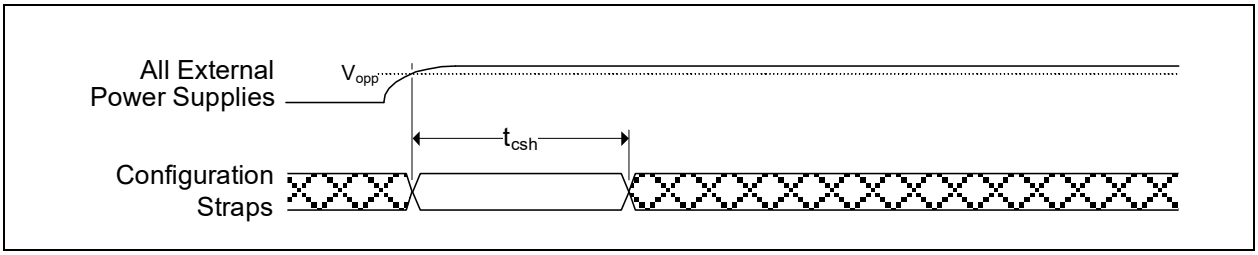

TABLE 9-5: POWER-ON CONFIGURATION STRAP LATCHING TIMING

Symbol	Description	Min	Typ	Max	Units
t_{csh}	Configuration strap hold after external power supplies at operational levels	1			ms

Device configuration straps are also latched as a result of **RESET_N** assertion. Refer to Section 9.6.3, Reset and Configuration Strap Timing for additional details.

9.6.3 RESET AND CONFIGURATION STRAP TIMING

Figure 9-4 illustrates the **RESET_N** pin timing requirements and its relation to the configuration strap pins. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified. Refer to Section 8.8, Resets for additional information on resets. Refer to Section 3.3, Configuration Straps and Programmable Functions for additional information on configuration straps.

FIGURE 9-4: RESET_N CONFIGURATION STRAP TIMING

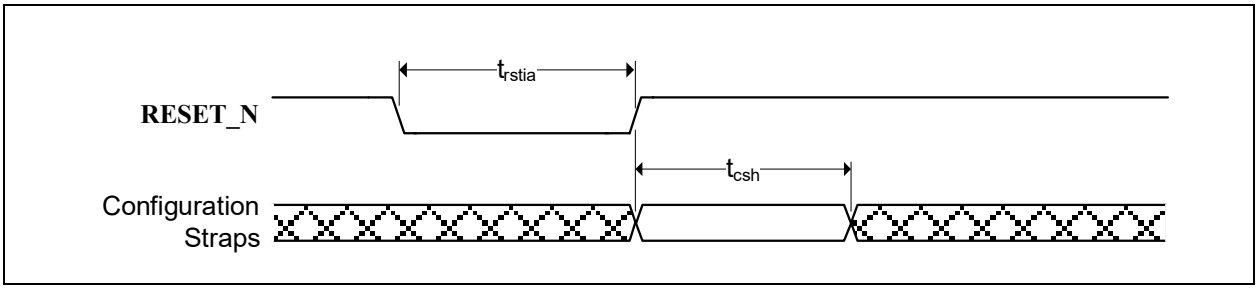

TABLE 9-6: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	5			µs
t_{csh}	Configuration strap pins hold after **RESET_N** deassertion	1			ms

Note: The clock input must be stable prior to **RESET_N** deassertion.

Configuration strap latching and output drive timings shown assume that the Power-On reset has finished first otherwise the timings in Section 9.6.2, Power-On and Configuration Strap Timing apply.

9.6.4 USB TIMING

All device USB signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Specification*. Please refer to the *Universal Serial Bus Revision 3.1 Specification*, available at http://www.usb.org/developers/docs.

9.6.5 SMBUS TIMING

All device SMBus signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification.* Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

9.6.6 I²C TIMING

All device I²C signals conform to the 100KHz Standard-mode (Sm) and 400KHz Fast Mode (Fm) voltage, power, and timing characteristics/specifications as set forth in the *I²C-Bus Specification*. Please refer to the *I²C-Bus Specification*, available at http://www.nxp.com/documents/user_manual/UM10204.pdf.

9.6.7 I²S TIMING

All device I²S signals conform to the voltage, power, and timing characteristics/specifications as set forth in the I²S-Bus Specification. Please refer to the I²S-Bus Specification, available at www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf

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9.6.8 SPI/SQI MASTER TIMING

This section specifies the SPI/SQI master timing requirements for the device.

FIGURE 9-5: SPI/SQI MASTER TIMING

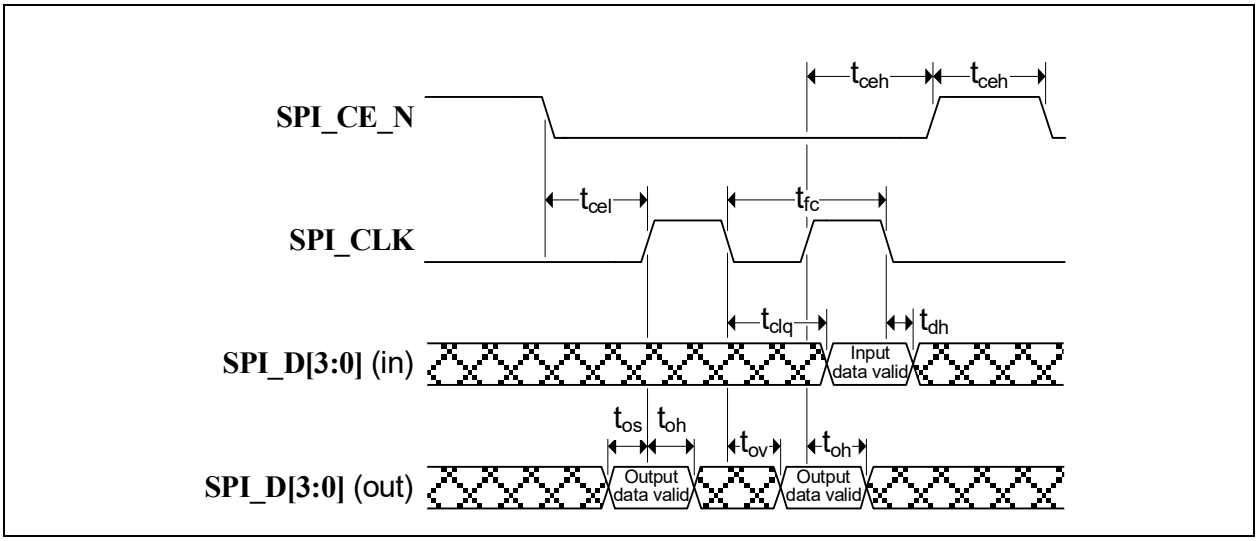


TABLE 9-7: SPI/SQI MASTER TIMING (30 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			30	MHz
t_{ceh}	Chip enable (**SPI_CE_N**) high time	100			ns
t_{clq}	Clock to input data			13	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_N**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_N**) high	12			ns

TABLE 9-8: SPI/SQI MASTER TIMING (60 MHZ OPERATION)

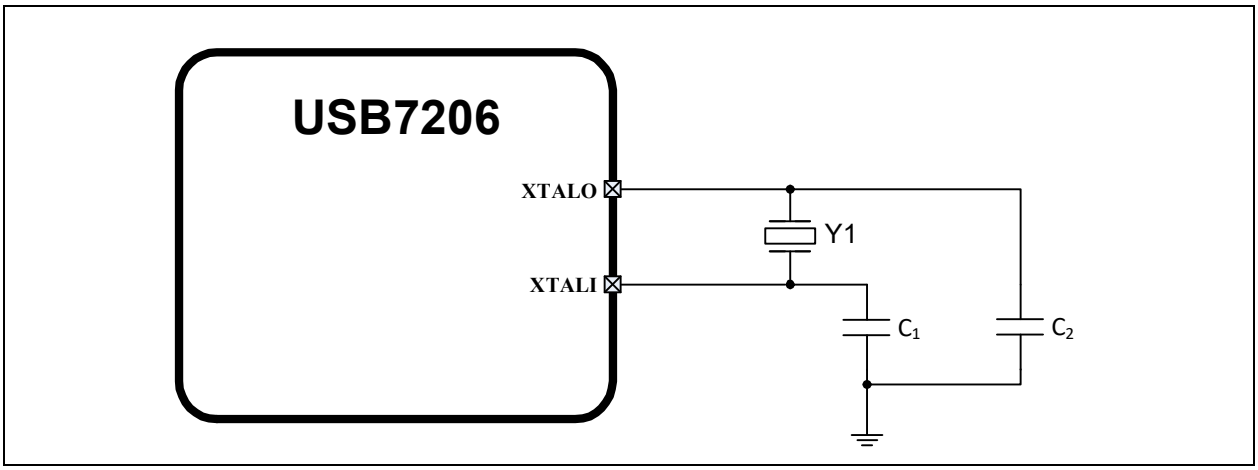
Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			60	MHz
t_{ceh}	Chip enable (**SPI_CE_N**) high time	50			ns
t_{clq}	Clock to input data			9	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_N**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_N**) high	12			ns

9.7 Clock Specifications

The device can accept either a 25MHz crystal or a 25MHz single-ended clock oscillator input. If the single-ended clock oscillator method is implemented, **XTALO** should be left unconnected and **XTALI/CLK_IN** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). The following circuit design (Figure 9-6) and specifications (Table 9-9) are required to ensure proper operation.

FIGURE 9-6: 25MHZ CRYSTAL CIRCUIT



9.7.1 CRYSTAL SPECIFICATIONS

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). Refer to Table 9-9 for the recommended crystal specifications.

TABLE 9-9: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut			AT, typ			
Crystal Oscillation Mode			Fundamental Mode			
Crystal Calibration Mode			Parallel Resonant Mode			
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	±50	PPM	
Frequency Stability Over Temp	F_{temp}	-	-	±50	PPM	
Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	PPM	Note 7
Total Allowable PPM Budget		-	-	±100	PPM	
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	100	-	-	uW	
Equivalent Series Resistance	R_1	-	-	60	Ω	
Operating Temperature Range		Note 8	-	Note 9	°C	
XTALI/CLK_IN Pin Capacitance		-	3 typ	-	pF	Note 10
XTALO Pin Capacitance		-	3 typ	-	pF	Note 10

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Note 7: Frequency Deviation Over Time is also referred to as Aging.

Note 8: 0 °C for commercial version, -40 °C for industrial version.

Note 9: +70 °C for commercial version, +85 °C for industrial version.

Note 10: This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XTALI/CLK_IN** pin, **XTALO** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

9.7.2 EXTERNAL REFERENCE CLOCK (CLK_IN)

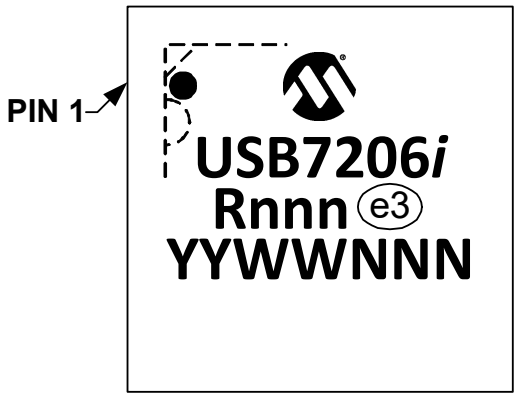
When using an external reference clock, the following clock characteristics are required:

- 25 MHz
- 50% duty cycle ±10%, ±100 ppm
- Jitter < 100 ps RMS

10.0 PACKAGE OUTLINE

10.1 Package Marking Information

100-VQFN (12x12 mm)



Legend:	*i*	Temperature range designator (Blank = commercial, *i* = industrial)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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10.2 Package Drawings

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 10-1: 100-VQFN PACKAGE (DRAWING)

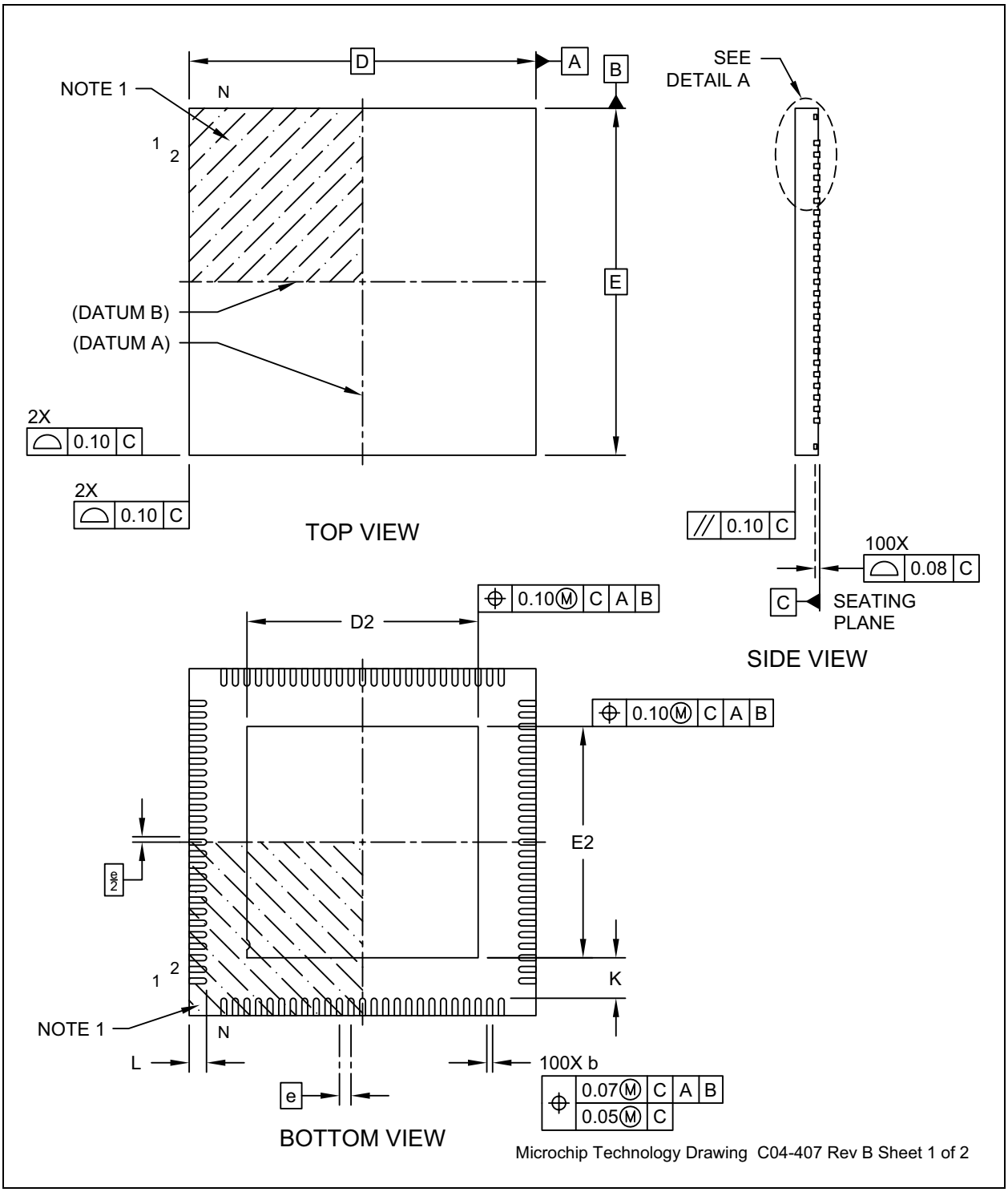
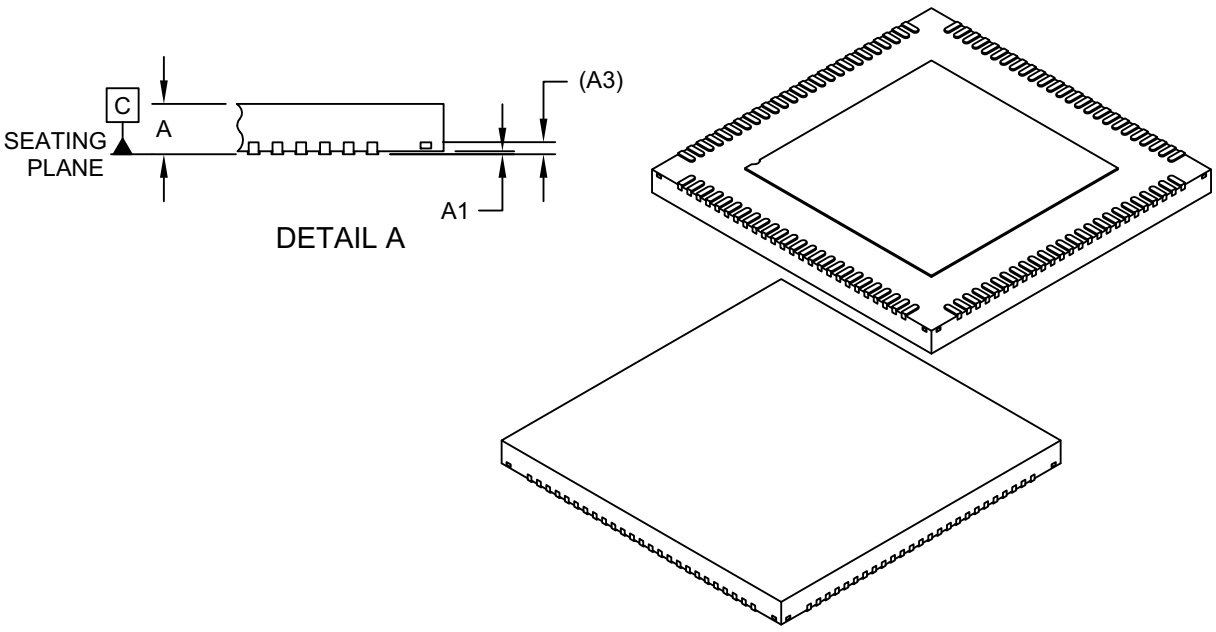


FIGURE 10-2: 100-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		12.00 BSC	
Exposed Pad Length	D2	7.90	8.00	8.10
Overall Width	E		12.00 BSC	
Exposed Pad Width	E2	7.90	8.00	8.10
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	1.30	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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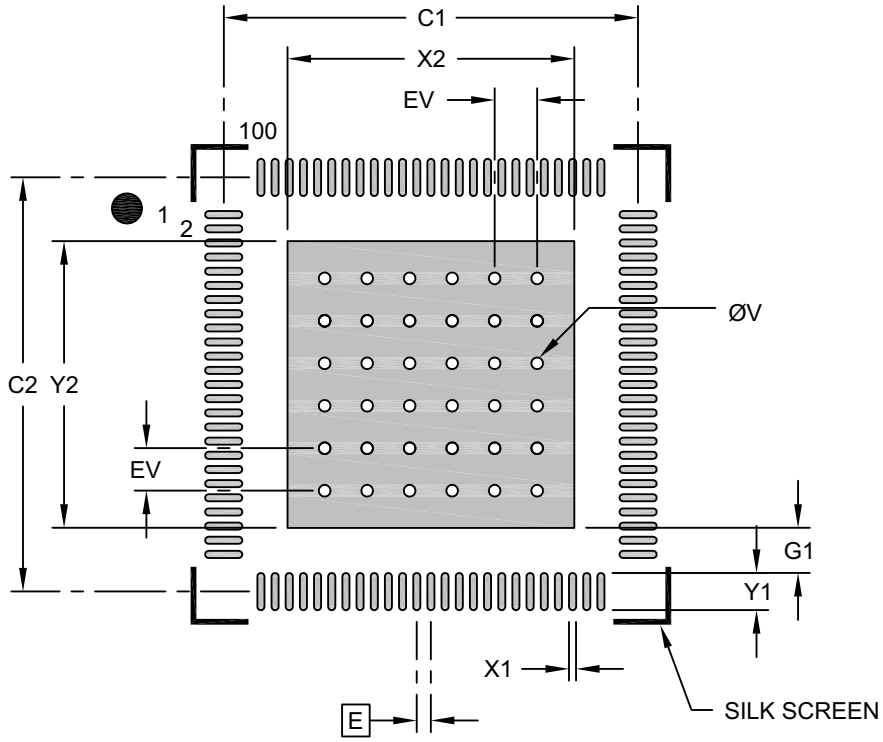
FIGURE 10-3: 100-VQFN PACKAGE (LAND-PATTERN)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			8.10
Optional Center Pad Length	Y2			8.10
Contact Pad Spacing	C1		11.70	
Contact Pad Spacing	C2		11.70	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.05
Contact Pad to Center Pad (X100)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2407A

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002875B (11-01-19)	Section 1.3, Reference Documents	Corrected I2S link
	Cover	Updated Highlight bullets to include “Gen 2” in description of Type-C support.
	All	Updated all “VDD11” and “+1.1V” references to “VCORE” for consistency and clarity. Updated VCORE pin description.
	Section 9.4, Power Consumption	Added power numbers.
	Section 10.1, Package Marking Information	Added package marking information.
	Table 3-4, Table 3-5	Changed “Configuration 1” references to “Configuration 3”. Added note under table indicating Configuration 1 and 2 are not used in the USB7206.
	Section 3.2, Pin Descriptions	Updated **VBUS_DET** description with additional voltage divider information and figure.
	Section 3.4, Physical and Logical Port Mapping	Added new section with physical and logical port mapping.
	Figure 2-1	Updated internal PHY numbering to match physical port numbering detailed in new Section 3.4, Physical and Logical Port Mapping.
	Section 2.1, General Description	Corrected Port Split description to indicate support on ports 3, 4, and 5.
	Section 9.6.1, Power Supply and RESET_N Sequence Timing	Clarified section and added links to the rise time information in Section 9.2, Operating Conditions**.
	Section 9.7.2, External Reference Clock (CLK_IN)	Clarified first sentence.
	Section 9.6.7, I2S Timing	Corrected hyperlink.
DS00002875A (01-15-19)	All	Initial Release

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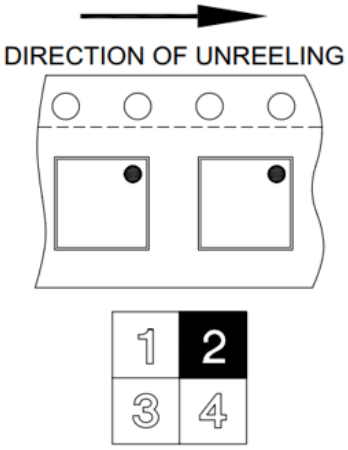
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	[X]	/	XXX
Device	Tape and Reel Option		Temperature Range		Package

Device:	USB7206	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)	
Package:	KDX =	100-pin VQFN



Examples:

a) USB7206/KDX
Tray, 0°C to +70°C, 100-pin VQFN

b) USB7206T/KDX
Tape & reel, 0°C to +70°C, 100-pin VQFN

c) USB7206-I/KDX
Tray, -40°C to +85°C, 100-pin VQFN

d) USB7206T-I/KDX
Tape & reel, -40°C to +85°C, 100-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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