MEC170x

Keyboard and Embedded Controller for Notebook PC

- 3.3V and 1.8V Operation
- ACPI Compliant
- VTR (standby) and VBAT Power Planes
  - Low Standby Current in Sleep Mode
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - EC-Programmable Base Address
- ARM® Cortex®-M4 Processor Core
  - 32-Bit ARM v7-M Instruction Set Architecture
  - Hardware Floating Point Unit (FPU)
  - Single 4GByte Addressing Space (Von Neumann Model)
  - Little-Endian Byte Ordering
  - Bit-Banding Feature Included
  - NVIC Nested Vectored Interrupt Controller
    - Up to 240 Individually-Vectored Interrupt Sources Supported
    - 8 Levels of Priority, Individually Assignable By Vector
    - Chip-Level Interrupt Aggregator supported, to expand number of interrupt sources or reduce number of vectors
  - System Tick Timer
  - Complete ARM-Standard Debug Support
    - JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
    - Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
    - Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
  - Comprehensive ARM-Standard Trace Support
    - Full DWT Hardware Trace Functionality for Watchpoint and Performance Monitoring
    - Full ITM Hardware Trace Functionality for Instrumented Firmware Support and Profiling
    - Full ETM Hardware Trace Functionality for Instruction Trace
    - Full TPIU Functionality for Trace Output Communication
  - MPU Feature
  - 1µS Delay Register
- Internal Memory
  - 64k Boot ROM
  - Two blocks of SRAM, totaling 256KB, 320KB or 480KB
    - Each block can be used for either program or data
    - One block 32KB or 64KB
    - One block 224KB, 288KB or 416KB
  - 128 Bytes Battery Powered SRAM
  - Non-volatile Read/Write Memory
    - 2KB of EEPROM
    - Single byte read/write access
    - 32 Byte page size
    - 1,000,000 write cycle endurance
- LPC Interface
  - Supports LPC Bus frequencies of 19MHz to 33MHz
  - 1.8V and 3.3V Support
  - LPC I/O Cycles Decoded
  - LPC Memory Cycles Decoded
  - Clock Run Support
  - Serial IRQ
  - ACPI SCI interface
  - SMI# output
- Enhanced Serial Peripheral Interface (eSPI)
  - Intel eSPI Specification compliant
  - Supports four channels/interfaces:
    - Peripheral channel Interface
    - Virtual Wire Interface
    - Out of Band Channel Interface
    - Flash Channel Interface
  - Supports EC Bus Master to Host Memory
- Legacy Support
  - Fast GATEA20 and Fast CPU_RESET
- System to EC Message Interface
  - 8042 Style Host Interface
  - ACPI Embedded Controller Interface
    - Five Instances
    - 1 or 4 Byte Data transfer capable
    - Full-duplex Register Access
  - ACPI Power Management Interface
    - SCI Event-Generating Functions
  - Mailbox Registers Interface
    - Thirty-two 8-Bit Scratch Registers
    - Two Register Mailbox Command Interface
    - Two Register SMI Source Interface
  - Three Embedded Memory Interface Instances
    - Host Serial or Parallel IRQ Source
    - Provides Two Windows to On-Chip SRAM for Host Access
    - Two Register Mailbox Command Interface
    - Host Access of Virtual Registers Without EC Intervention
- Battery Backed Resources
  - Power-Fail Status Register
  - 32 KHz Clock Generator
  - Week Alarm Timer Interface
  - Real Time Clock
  - VBAT-Powered Control Interface
    - Five Wake-up Input Signals
    - Optional Latching of Wake-up Inputs
  - VBAT-Backed 128 Byte Memory

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- Four EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Fully Operational on Standby Power
  - DMA-driven I^2C Network Layer Hardware
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speed up to 1MHz
  - Hardware Bus Access “Fairness” Interface
  - SMBus Time-outs Interface
  - AMD-TSI Port
  - 12 Ports Assignable to Any Controller
  - All ports 1.8V-capable
- Five independent Hardware Driven PS/2 Ports
  - Three controllers
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
  - Two ports 5V tolerant
- Two General Purpose Serial Peripheral Interface Controllers (ECGP-SPI)
  - One 3-pin EC-driven Full Duplex Serial Communication Interface
  - One Full Duplex Serial Communication Interface Accessible by Host over LPC
  - Flexible Clock Rates
  - SPI Burst Capable
- One Quad Serial Peripheral Interface (SPI) Controller
  - Master Only SPI Controller
  - Mappable to two ports (only 1 port active at a time)
  - Dual and Quad I/O Support
  - Flexible Clock Rates
  - SPI Burst Capable
  - SPI Controller Operates with Internal DMA Controller with CRC Generation
- 18 x 8 Interrupt Capable Multiplexed Keyboard Scan Matrix
  - Optional Push-Pull Drive for Fast Signal Switching
- Four Breathing/Blinking LED Interfaces
  - Supports three modes of operation:
    - Blinking Mode with Programmable Blink Rates
    - Breathing LED Output
    - 8-bit PWM
  - Breathing LED Supports Piecewise-linear Brightness Curves, Symmetric or Asymmetric
  - Supports Low Power Operation in Blinking and Breathing Modes
    - Operates on Standby Power
    - Operates in Chip's Heavy Sleep State on 32kHz standby clock
    - Operational in EC Sleep State
  - Pin buffers capable of sinking up to 12 mA
- Three Resistor/Capacitor Identification Detection (RC_ID) ports
  - Single Pin Interface to External Inexpensive RC Circuit
  - Replacement for Multiple GPIO’s
  - Provides 8 Quantized States on One Pin
- General Purpose I/O Pins
  - Up to 148 GPIOs
  - 8 GPIO Pass-Through Port (GPTP)
  - Glitch protection on most GPIO pins
  - 6 Battery-powered General Purpose Outputs
  - All GPIOs can be powered by 1.8V
  - Programmable Drive Strength and Slew Rate on all GPIOs
- Programmable 16-bit Counter/Timer Interface
  - Four 16-bit Auto-reloading Counter/Timer Instances
  - Four Operating Modes per Instance: Timer, One-shot, Event and Measurement
    - 4 External Inputs, 4 External Outputs
- Hibernation Timer Interface
  - Two 32.768 KHz Driven 16-bit Timers
    - Programmable Wake-up from 0.5ms to 128 Minutes
  - One 32.768 KHz Driven 32-bit RTOS Timer
    - Programmable Wake-up from 30µS to 35 Hours
    - Auto Reload Option
- System Watch Dog Timer (WDT)
- Input Capture and Compare Timer
  - 32-bit Free-running timer
  - Six 32-bit Capture Registers
  - Two 32-bit Compare Registers
  - Capture, Compare and Overflow Interrupts
  - Toggle Output on Compare Timers
- Week Timer
  - Power-up Event Output
  - Week Alarm Interrupt with 1 Second to 8.5 Year Time-out
  - Sub-Week Alarm Interrupt with 0.50 Seconds - 72.67 hours time-out
  - 1 Second and Sub-second Interrupts
- Real Time Clock (RTC)
  - VBAT Powered
  - 32KHz Crystal Oscillator
  - Time-of-Day and Calendar Registers
  - Programmable Alarms
  - Supports Leap Year and Daylight Savings Time
- Two Microchip BC-Link Interconnection Bus
  - Programmable Bus Clock Rate
- PECI Interface 3.0
- FAN Support
  - Eleven Programmable Pulse-Width Modulator (PWM) Outputs
    - Multiple Clock Rates
    - 16-Bit ‘On’ and 16-Bit ‘Off’ Counters
  - Three Fan Tachometer Inputs
  - Two RPM-Based Fan Speed Controllers
    - Each includes one Tach input and one PWM output
    - 3% accurate from 500 RPM to 16k RPM
    - Automatic Tachometer feedback
    - Aging Fan or Invalid Drive Detection
    - Spin Up Routine
    - Ramp Rate Control
    - RPM-based Fan Speed Control Algorithm

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- ADC Interface
  - 10-bit Conversion in 1μs
  - 16 Channels
  - Integral Non-Linearity of ±1.5 LSB; Differential Non-Linearity of ±1.0 LSB
- Two Standard 16C550 UARTs
  - Accessible from Host and EC
  - One UART with full 8-pin Modem Control
  - One UART with 4-pin Interface
  - Programmable Input/output Pin Polarity Inversion
  - Programmable Main Power or Standby Power Functionality
- Two Port 80h Debug Ports for BIOS Debug
  - Ports, Assignable to Any LPC IO Address
  - 24-bit Timestamp with Adjustable Timebase
  - 16-Entry FIFO
- Trace FIFO Debug Port (TFDP)
- Integrated Standby Power Reset Generator
  - Reset Input Pin
  - Reset Output Pin
- Clock Generator
  - 32.768KHz Clock Source
    - Low power 32KHz crystal oscillator
    - Optional use of a crystal-free silicon oscillator with ±2% Accuracy
    - Optional use of 32.768 KHz input Clock
    - Operational on Suspend Power
  - Programmable Clock Power Management Control and Distribution
  - 48 MHz PLL
- Multi-purpose AES Cryptographic Engine
  - Hardware support for ECB, CTR, CBC and OFB AES modes
  - Support for 128-bit, 192-bit and 256-bit key length
  - DMA interface to SRAM, shared with Hash engine
- Cryptographic Hash Engine
  - Support for SHA-1, SHA-256, SHA-384, SHA-512
  - DMA interface to SRAM, shared with AES engine
- Public Key Cryptographic Engine
  - Hardware support for RSA and Elliptic Curve public key algorithms
  - RSA keys length of 1024 or 2048 bis
  - ECC Prime Field and Binary Field keys up to 640 bits
  - Microcoded support for standard public key algorithms
- Cryptographic Features
  - True Random Number Generator
    - 1K bit FIFO
  - Monotonic Counter
- Packages
  - 144 Pin WFBGA RoHS Compliant package
  - 169 Pin WFBGA RoHS Compliant package
  - 169 Pin XFBGA RoHS Compliant package

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1.0 GENERAL DESCRIPTION

The MEC170x is a family of keyboard and embedded controller designs customized for notebooks and tablet platforms. The family is a highly-configurable, mixed signal, advanced I/O controller architecture. Every device in the family incorporates a 32-bit ARM Cortex M4F Microcontroller core with a closely-coupled SRAM for code and data. A secure bootloader is used to download the custom firmware image from the system's shared SPI Flash device, thereby allowing system designers to customize the device's behavior.

The MEC170x products may be configured to communicate with the system host through one of three host interfaces: Intel Low Pin Count (LPC), eSPI, or I^2C. Note that this functionality is product dependent. To see which features apply to a specific part in the family see Table 1-1, "MEC170x Feature List by Package". The document defines the features for all devices in the family.

The MEC170x products are designed to operate as either a stand-alone I/O device or as an EC Base Component of a split-architecture Advanced I/O Controller system which uses BC-Link communication protocol to access up to two BC bus companion components. The BC-Link protocol is peer-to-peer providing communication between the MEC170x embedded controller and registers located in a companion device.

The MEC170x is directly powered by a minimum of two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on' and system power management functions. There are three voltage supply regions for all GPIO pins. Each region may be either 3.3V or 1.8V. The LPC interface may be operated at either 1.8V or 3.3V; the eSPI interface operates at 1.8V. All the devices are equipped with a Power Management Interface that supports low-power states and are capable of operating in a Connected Standby system.

The MEC170x family of devices offer a software development system interface that includes a Trace FIFO Debug port, a host accessible serial debug port with a 16C550A register interface, a Port 80 BIOS Debug Port, and a JTAG/SWD debug interface.

1.1 Family Features

TABLE 1-1: MEC170X FEATURE LIST BY PACKAGE

MEC170x Product Family	MEC1701	MEC1701	MEC1703	MEC1703	MEC1704	MEC1705
Package	144 WFBGA	169 WFBGA	144 WFBGA	169 XFBGA	144 WFBGA	144 WFBGA
Device ID	2Dh	2Dh	2Eh	2Eh	33h	2Fh
Boundary Scan JTAG ID	021B2445h	021B2445h	021C2445h	021C2445h	02202445h	02202445h
SRAM Block (Primary use: code)	224KB/ 288KB/ 316KB	224KB/ 288KB/ 316KB	224KB/ 288KB/ 316KB	224KB/ 288KB/ 316KB	224KB/ 288KB/ 316KB	224KB/ 288KB/ 316KB
SRAM Block (Primary use: data)	32KB/64KB	32KB/64KB	32KB/64KB	32KB/64KB	32KB/64KB	32KB/64KB
Battery Backed SRAM	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes	128 bytes
EEPROM	0	0	2K bytes	2K bytes	0	2K bytes
LPC Host Interface	Yes	Yes	Yes	Yes	Yes	Yes
eSPI Host Interface	Yes	Yes	Yes	Yes	Yes	Yes
8042 Emulated Keyboard Controller	Yes	Yes	Yes	Yes	Yes	Yes
Embedded Memory Interface (EMI)	3	3	3	3	3	3
Mailbox Register Interface	1	1	1	1	1	1
ACPI Embedded Controller Interface	5	5	5	5	5	5
ACPI PM1 Block Interface	Yes	Yes	Yes	Yes	Yes	Yes
Trace FIFO Debug Port	Yes	Yes	Yes	Yes	Yes	Yes
Internal DMA Channels	14	14	14	14	14	14
16-bit Basic Timer	4	4	4	4	4	4
32-bit Basic Timer	2	2	2	2	2	2
16-bit Counter/Timer	4	4	4	4	4	4
Capture Timer	6	6	6	6	6	6
Compare Timer	2	2	2	2	2	2
Watchdog Timer (WDT)	1	1	1	1	1	1
Hibernation Timer	2	2	2	2	2	2

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TABLE 1-1: MEC170X FEATURE LIST BY PACKAGE (CONTINUED)

MEC170x Product Family	MEC1701	MEC1701	MEC1703	MEC1703	MEC1704	MEC1705
Package	144 WFBGA	169 WFBGA	144 WFBGA	169 XFBGA	144 WFBGA	144 WFBGA
Week Timer	1	1	1	1	1	1
RTC	1	1	1	1	1	1
Battery-Powered General Purpose Output (BGPO)	4	6	4	6	4	4
Active Low VBAT-Powered Control Interface (VCI)	4	6	4	6	4	4
Keyboard Matrix Scan Support	Yes	Yes	Yes	Yes	Yes	Yes
Port 80 BIOS Debug Port	2	2	2	2	2	2
I2C Host Controllers	4	4	4	4	4	4
I2C Ports	10	11	10	11	10	10
PECI 3.0 Interface	Yes	Yes	Yes	Yes	Yes	Yes
PS/2 Device Interface	3 controller/ 4 ports	3 controller/ 5 ports	3 controller/ 4 ports	3 controller/ 5 ports	3 controller/ 4 ports	3 controller/ 4 ports
GPIOs	123	148	123	148	123	123
Pass-through GPIOs	6	8	6	8	6	6
Blinking/Breathing PWM	4	4	4	4	4	4
General Purpose SPI Master Controller	2	2	2	2	2	2
Quad SPI Master Controller	1 controller/ 2 ports	1 controller/ 2 ports	1 controller/ 2 ports	1 controller/ 2 ports	1 controller/ 2 ports	1 controller/ 2 ports
10-bit ADC Channels	8	16	8	16	8	8
16-bit PWMs	8	11	8	11	8	8
16-bit TACHs	3	3	3	3	3	3
UARTs	2 UART0: 2-pin UART1: 2-pin	2 UART0: 8-pin UART1: 4-pin	2 UART0: 2-pin UART1: 2-pin	2 UART0: 8-pin UART1: 4-pin	2 UART0: 8-pin UART1: 4-pin	2 UART0: 8-pin UART1: 4-pin
BC-Link	2	2	2	2	2	2
AES Hardware Support	128-256 bit	128-256 bit	128-256 bit	128-256 bit	128-256 bit	128-256 bit
SHA Hashing Support	SHA-1 to SHA-512	SHA-1 to SHA-512	SHA-1 to SHA-512	SHA-1 to SHA-512	SHA-1 to SHA-512	SHA-1 to SHA-512
Public Key Cryptography Support	RSA: 4K bit ECC: 640 bit	RSA: 4K bit ECC: 640 bit	RSA: 4K bit ECC: 640 bit	RSA: 4K bit ECC: 640 bit	RSA: 4K bit ECC: 640 bit	RSA: 4K bit ECC: 640 bit
True Random Number Generator	1K bit	1K bit	1K bit	1K bit	1K bit	1K bit
UPD Dead Battery Support	No	Yes	No	Yes	No	No

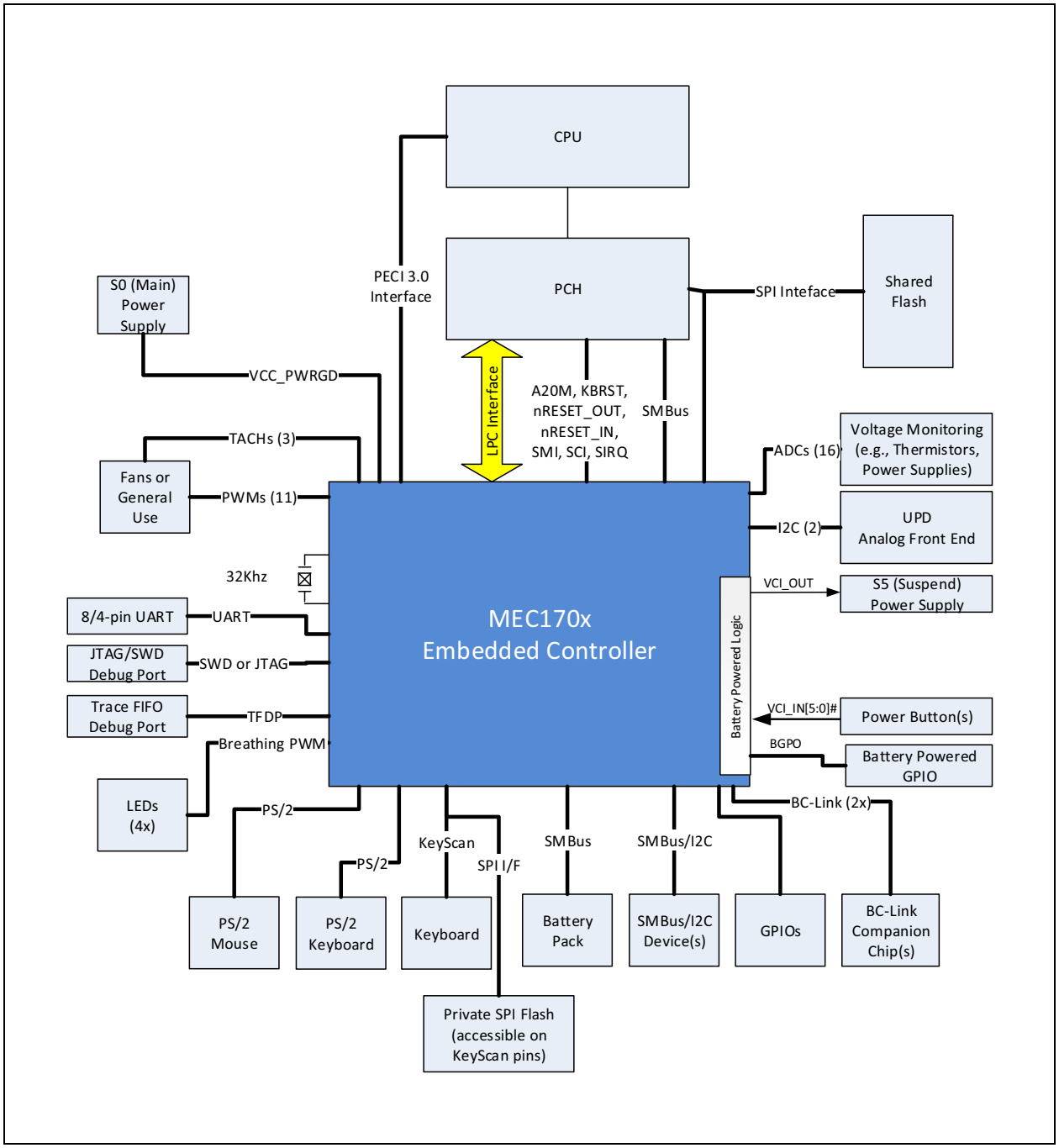
1.2 Boot ROM

Following the release of the RESET_EC signal, the processor will start executing code in the Boot ROM. The Boot ROM executes the SPI Flash Loader, which downloads User Code from an external SPI Flash and stores it in the internal Code RAM. Upon completion, the Boot ROM jumps into the User Code and starts executing as defined in the Boot Loader document.

The Boot ROM call load code from an external SPI Flash device via the Shared Flash Interface, the Private Flash Interface or via the eSPI Flash Channel. The downloaded code must configure the device's pins according to the platform's needs. If the Boot ROM loads code via the eSPI Flash Channel, the pins that constitute the eSPI interface are left in the eSPI state; otherwise, the Boot ROM leaves all pins in their default initial state.

1.3 System Block Diagrams

1.3.1 LPC HOST SYSTEM BLOCK DIAGRAM



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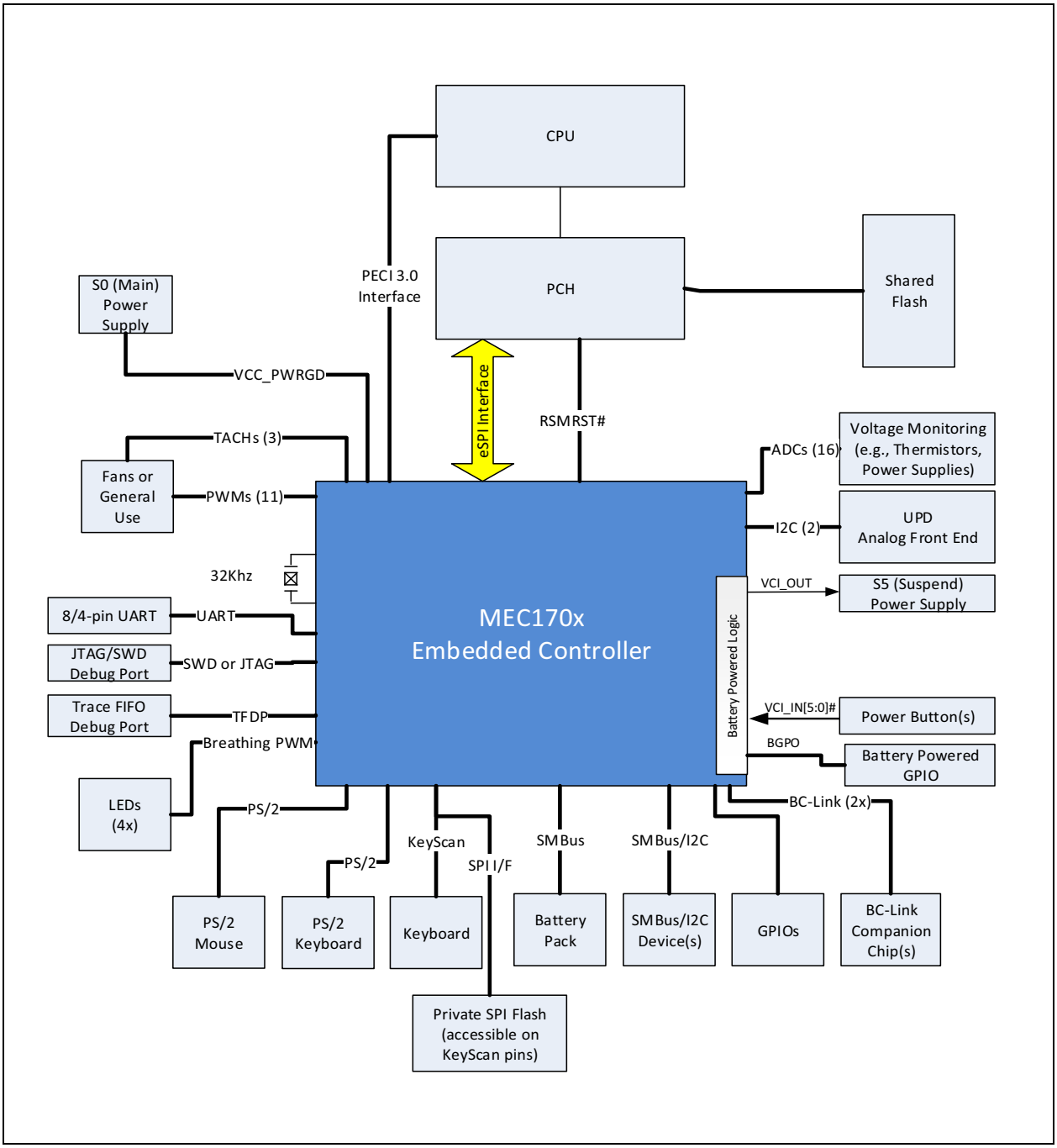
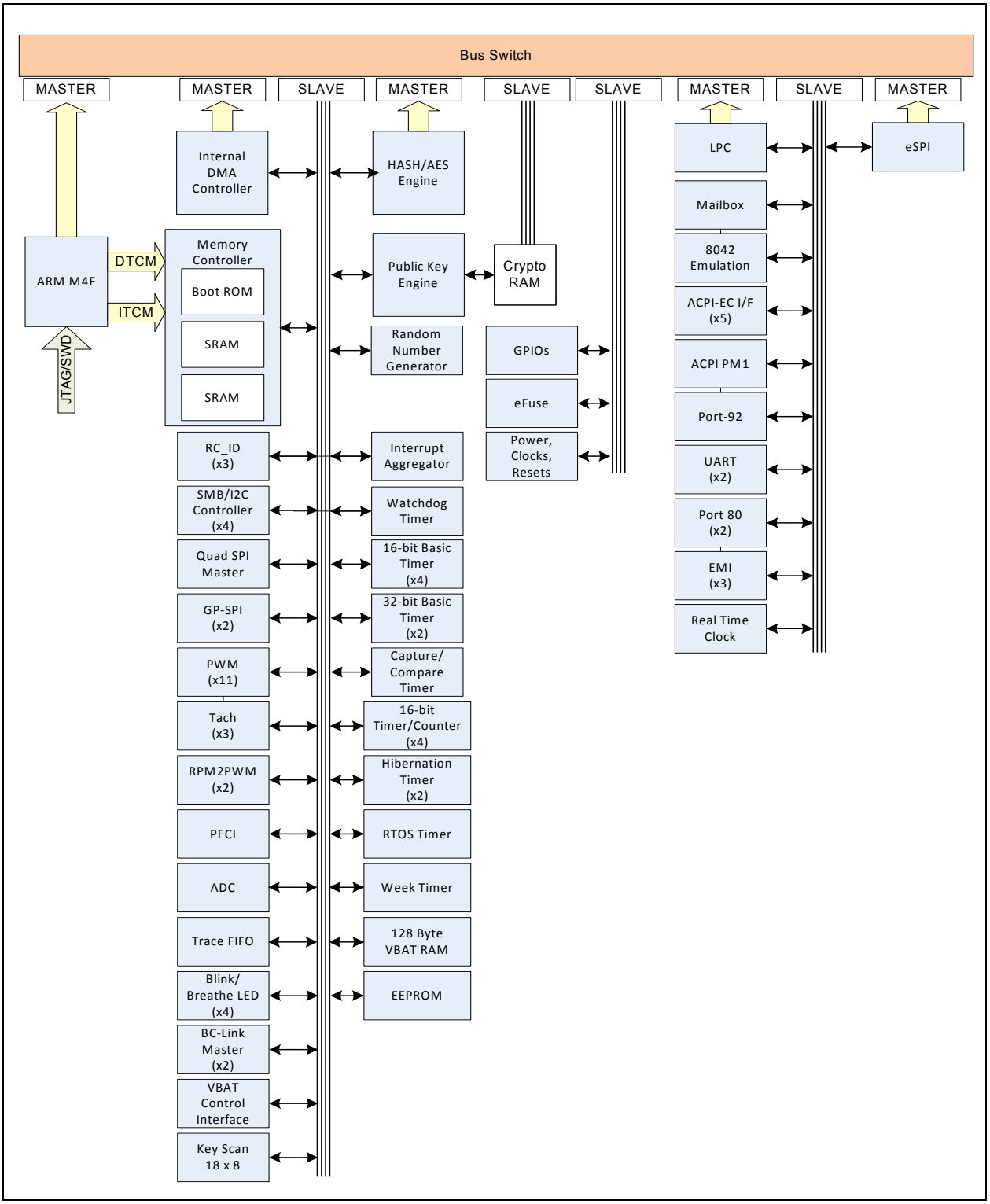
1.3.2 ESPI HOST SYSTEM BLOCK DIAGRAM



1.4 MEC170x Block Diagram

Note: Not all features shown are available on all devices. Refer to Table 1-1, "MEC170x Feature List by Package" for a list of the features by device.



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2.0 PIN CONFIGURATION

2.1 Description

The Pin Configuration chapter includes Pin List By Pin Name, Signal Description by Signal, Notes for Tables in this Chapter, Pin Default State Through Power Transitions, and Packages.

2.2 Terminology and Symbols for Pins/Buffers

2.2.1 BUFFER TERMINOLOGY

Term	Definition
#	The '#' sign at the end of a signal name indicates an active-low signal
n	The lowercase 'n' preceding a signal name indicates an active-low signal
PWR	Power
PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output. Configurable drive strength from 2ma to12ma. **Note:** All GPIOs have programmable drive strength options of 2ma, 4ma, 8ma and 12ma. GPIO pin drive strength is determined by the DRIVE_STRENGTH field in the Pin Control 2 Register.
In	I Type Input Buffer.
O2ma	O-2 mA Type Buffer.
PCI	PCI pin. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PECI	PECI Input/Output. These pins operate at the processor voltage level (VREF_VTT)
SB-TSI	SB-TSI Input/Output. These pins operate at the processor voltage level (VREF_VTT)

Note 1: See the "PCI Local Bus Specification," Revision 2.1, Section 4.2.2.

2: See the "PCI Local Bus Specification," Revision 2.1, Section 4.2.2 and 4.2.3.

2.2.2 PIN NAMING CONVENTIONS

- Pin Name is composed of the multiplexed options separated by '/'. E.g., GPIOxxxx/SignalA/SignalB.
- Parenthesis '()' are used to list aliases or alternate functionality for a single mux option. For example, GPIO062/(RESETO#) has only a single mux option, GPIO062, but the signal GPIO062 can also be used or interpreted as RESETO#.
- Signal Names appended with a numeric value indicates the Instance Number E.g., PWM0, PWM1, etc. indicates that PWM0 is the PWM output for PWM Instance 0, PWM1 is the PWM output for PWM Instance 1, etc. Note that this same instance number is shown in the Register Base Address tables linking the specific PWM block instance to a specific signal on the pinout. The instance number may be omitted if there in only one instance of the IP block implemented.

2.3 Notes for Tables in this Chapter

Note	Description
Note 1	The nEC_SCI pin can be controlled by hardware and EC firmware. The nEC_SCI pin can drive either the ACPI Run-time GPE Chipset input or the Wake GPE Chipset input. Depending how the nEC_SCI pin is used, other ACPI-related SCI functions may be best supplied by other general purpose outputs that can be configured as open-drain drivers.
Note 2	These pins require an external weak pull-up resistors of 10k-100k ohms.
Note 3	A weak pull-up resistor is recommended on the BC-Link data line (100KΩ).
Note 4	The UARTs can be used by the Host or EC. This pin can be VCC protected or not VCC protected under program control by the POWER bit in the Configuration Select Register in Host configuration space (also accessible by the EC).

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Note	Description
Note 5	When the JTAG_RST# pin is not asserted (logic'1'), the pins for the signal functions in the JTAG/SWD interface are unconditionally routed to the interface; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the signal functions in the JTAG/SWD interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers can not route the JTAG interface to the pins. System Board Designer should terminate this pin in all functional state using jumpers and pull-up or pull down resistors, etc.
Note 6	PS/2 ports ending with signal functions ending with "A" or "B" are muxed to a single controller. Only one set of clock and data are intended to used at a time (either "A" or "B" not both. The unused port segment should have its associated pin control register's, Mux Control Field programmed away from the PS2 controller.
Note 7	The GPIO062 pin defaults to output 'low' on RESET_SYS to support the firmware controlled RESETO# feature. RESETO# is not a GPIO alternate function; it is controlled by firmware as a GPIO function.
Note 8	The BGPO pins have a GPIO signal for interrupt/wake-only signal functions. The BGPO alternate function is not selected through the GPIO Pin Control register. Instead, the BGPO alternate function is configured by programming the Week Timer Control register. When configured as the BGPO function the pad is powered by VBAT.
Note 9	The VREF_VTT pin should be disabled by the PECI Disable Register if PECI or SB-TSI are not used.
Note 10	The UART_CLK external baud clock input is connected to all the UARTs in the design. Each UART may select either the external UART_CLK baud clock or the internally generated baud clock.
Note 11	The nEM_INT signal is asserted low if any of the EMI blocks have their nEM_INT signal asserted low. This signal can be routed to nSMI and nPME inputs in the system as required.
Note 12	The Private SPI Interface may be used for Crisis Recovery. Crisis Recovery offers a way to load a SPI Flash image from an external SPI Flash device connected via the Keyboard Scan Interface pins. The GPIO045/KSO01 pin requires a weak external pull-up for normal operation. If this pin is not detected as a high input following a POR the device could enter Crisis Recovery mode in error and fail to boot.
Note 13	VCI_IN# function works even when configured as GPIO.
Note 14	I2C/SMBus Port pins can be mapped to any SMB-I2C Controller. The number in the I2C/SMBus signal names (I2Cxx_DATA) indicates the port value. E.g. I2C01_DATA represents I2C/SMBus Data Port 1
Note 15	The Voltage Regulator Capacitor (VR_CAP) pin requires an external 1uF capacitor and a voltage range of 1.08V (min) to 1.32V (max).
Note 16	The GPTP-OUT always drives at the level of the output buffer regardless of the voltage at the GPTP-IN pin. If GPTP-OUT buffer is powered by 1.8V the signal out will be 1.8V regardless of the voltage on the GPTP-IN pin. So, if GPTP-IN pin is 3.3V then the output essentially level-shifts the voltage down to 1.8V. Similarly if GPTP-OUT is 3.3V then the signal will be 3.3V regardless of the voltage on the GPTP-IN pin. If the GPTP-IN pin is 1.8V the output essentially level-shifts the voltage up to 3.3V.

2.4 Pin List By Pin Name

2.4.1 DEFAULT STATE

The default state for analog pins is Input. The default state for all pins that default to a GPIO function is also input, with pull-up and pull-down resistors disabled. The default state for pins that differ is shown in the following table. Entries for the Default State column are

- O2ma-Low: Push-Pull output, Slow slew rate, 2ma drive strength, grounded
- O2ma-High Push-Pull output, Slow slew rate, 2ma drive strength, high output
- In-PU Input, with pull-up resistor enabled

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Pin Name	Default (if not GPIO)	Default State (if not In)
A5	A5	A5	B4	D6	BGPO0	BGPO0	O2ma-Low
B3	B3	B3	C2	C3	GPIO000/VCI_IN3#	VCI_IN3#	
			N11	R12	GPIO001/PWM4		
M8	M8	M8	N13	L9	GPIO002/PWM5		
F5	F5	F5	C6	B7	GPIO003/I2C00_SDA/SPI0_CS#		
C6	C6	C6	B5	D7	GPIO004/I2C00_SCL/SPI0_MOSI		
			A5	E7	GPIO005/I2C01_SDA/GPTP-OUT4		
			B6	A7	GPIO006/I2C01_SCL/GPTP-OUT7		
B12	B12	B12	B10	A14	GPIO007/I2C03_SDA/PS2_CLK0B		
C10	C10	C10	C10	D11	GPIO010/I2C03_SCL/PS2_DAT0B		
J6	J6	J6	L5	K6	GPIO011/nSMI		
N6	N6	N6	L7	P8	GPIO012/I2C07_SDA/TOUT3		
M7	M7	M7	H7	R8	GPIO013/I2C07_SCL/TOUT2		
M9	M9	M9	M10	P11	GPIO014/PWM6/GPTP-IN6		
J7	J7	J7	M12	J9	GPIO015/PWM7		
N3	N3	N3	N8	M7	GPIO016/GPTP-IN7/SHD_IO3/ICT3		
J8	J8	J8	J9	K11	GPIO017/GPTP-IN5/KSI0		
L7	L7	L7	L9	R9	GPIO020/KSI1		
N9	N9	N9	M9	P10	GPIO021/LPCPD#/KSI2		
E2	E2	E2	D2	D2	GPIO022/GPTP-IN0		
C3	C3	C3	F4	F5	GPIO023/GPTP-IN1		
C2	C2	C2	E2	G4	GPIO024/GPTP-IN2		
M12	M12	M12	K12	H11	GPIO025/TIN0/nEM_INT/UART_CLK		
N13	N13	N13	L11	P12	GPIO026/TIN1/KSI3		
K11	K11	K11	F13	P15	GPIO027/TIN2/KSI4		
J9	J9	J9	J13	N14	GPIO030/TIN3/KSI5		
M11	M11	M11	M13	M11	GPIO031/GPTP-OUT1/KSI6		
L10	L10	L10	K9	M10	GPIO032/GPTP-OUT0/KSI7		
B2	B2	B2	C1	B1	GPIO033/RC_ID0		
H12	H12	H12	E13	H15	GPIO034/RC_ID1/SPI0_CLK		
		E13	G11	G15	GPIO035/PWM8/CTOUT1		
H13	H13	H13	F12	J12	GPIO036/RC_ID2/SPI0_MISO		
M10	M10	M10	M11	L11	GPIO040/GPTP-OUT2/KSO00		
			F2	H4	GPIO041		
J12	J12	J12	H10	J15	GPIO042/PECI_DAT/SB-TSI_DAT		

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Pin Name	Default (if not GPIO)	Default State (if not In)
J13	J13	J13	H11	J14	GPIO043/SB-TSI_CLK		
H11	H11	H11	G9	K12	GPIO044/VREF_VTT		
E8	E8	E8	E8	A11	GPIO045/KSO01		
E9	E9	E9	E10	F10	GPIO046/BCM1_DAT/KSO02		
F13	F13	F13	A12	E15	GPIO047/BCM1_CLK/KSO03		
F3	F3	F3	G2	H5	GPIO050/FAN_TACH0/GTACH0		
B1	B1	B1	F3	F2	GPIO051/FAN_TACH1/GTACH1		
L8	L8	L8	K8	L8	GPIO052/FAN_TACH2/LRESET#		
M13	M13	M13	K11	P14	GPIO053/PWM0/GPWM0		
L12	L12	L12	K10	N15	GPIO054/PWM1/GPWM1		
N4	N4	N4	M8	M8	GPIO055/PWM2/SHD_CS#/(RSMRST#)		
N5	N5	N5	N9	M9	GPIO056/PWM3/SHD_CLK		
D1	D1	D1	F1	G2	GPIO057/VCC_PWRGD		
D2	D2	D2	G5	H7	GPIO060/KBRST/48MHZ_OUT		
N1	N1	N1	M1	M6	GPIO061/LPCPD#/ESPI_RESET#		
A2	A2	A2	D3	C2	GPIO062/(RESETO#)		O2ma-High
M4	M4	M4	N5	P6	GPIO063/SER_IRQ/ESPI_ALERT#		
J5	J5	J5	M3	M5	GPIO064/LRESET#	LRESET#	
M2	M2	M2	N2	R2	GPIO065/PCI_CLK/ESPI_CLK		
M1	M1	M1	N1	P3	GPIO066/LFRAME#/ESPI_CS#		
L2	L2	L2	M5	K5	GPIO067/CLKRUN#		
L3	L3	L3	M4	R3	GPIO070/LAD0/ESPI_IO0		
N2	N2	N2	N3	R4	GPIO071/LAD1/ESPI_IO1		
M3	M3	M3	N4	P5	GPIO072/LAD2/ESPI_IO2		
L4	L4	L4	M6	R5	GPIO073/LAD3/ESPI_IO3		
H7	H7	H7	L4	L6	GPIO100/nEC_SCI		
A4	A4	A4	C5	F6	GPIO101/BGPO1		
B5	B5	B5	B3	A5	GPIO102/BGPO2		
F11	F11	F11	A13	F15	GPIO104/UART0_TX		
F9	F9	F9	F9	F11	GPIO105/UART0_RX		
E3	E3	E3	H6	G7	GPIO106/PWROK		
L13	L13	L13	H13	M14	GPIO107/nSMI/KSO04		
			G13	L15	GPIO110/PS2_CLK2		
			G12	L12	GPIO111/PS2_DAT2		
K13	K13	K13	J12	K15	GPIO112/PS2_CLK1A/KSO05		

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Pin Name	Default (if not GPIO)	Default State (if not In)
J11	J11	J11	J11	L14	GPIO113/PS2_DAT1A/KSO06		
H9	H9	H9	J10	K14	GPIO114/PS2_CLK0A/nEC_SCI		
N12	N12	N12	L13	P13	GPIO115/PS2_DAT0A		
K12	K12	K12	H12	M15	GPIO120/KSO07		
F12	F12	F12	D13	F12	GPIO121/PVT_IO0/KSO08		
E11	E11	E11	D12	F14	GPIO122/BCM0_DAT/PVT_IO1/KSO09		
E12	E12	E12	C13	G12	GPIO123/BCM0_CLK/PVT_IO2/KSO10		
C11	C11	C11	B13	E12	GPIO124/GPTP-OUT6/PVT_CS#/KSO11		
D11	D11	D11	B12	D14	GPIO125/GPTP-OUT5/PVT_CLK/KSO12		
D12	D12	D12	C12	E14	GPIO126/PVT_IO3/KSO13		
D13	D13	D13	A11	D15	GPIO127/A20M/UART0_CTS#		
N8	N8	N8	J8	P9	GPIO130/I2C10_SDA/TOUT1		
N7	N7	N7	N10	R10	GPIO131/I2C10_SCL/TOUT0		
N11	N11	N11	L10	R14	GPIO132/I2C06_SDA/KSO14		
			C11	C14	GPIO133/PWM9		
E13	E13		D11	G14	GPIO134/PWM10/UART1_RTS#		
G9	G9		E12	G9	GPIO135/UART1_CTS#		
L11	L11	L11	K13	J11	GPIO140/I2C06_SCL/ICT5		
B7	B7	B7	A7	B8	GPIO141/I2C05_SDA/SPI1_-CLK/UART0_DCD#/TRACEDAT0		
F7	F7	F7	F7	D8	GPIO142/I2C05_SCL/SPI1_-MOSI/UART0_DSR#/TRACEDAT1		
A7	A7	A7	A6	A8	GPIO143/I2C04_SDA/SPI1_MISO/UART0_DTR#/TRACEDAT2		
E7	E7	E7	D4	E8	GPIO144/I2C04_SCL/SPI1_CS#/UART0_RI#/TRACEDAT3		
A8	A8	A8	D7	G8	GPIO145/I2C09_SDA/JTAG_TDI		
G8	G8	G8	F8	B9	GPIO146/I2C09_SCL/JTAG_TDO		
C7	C7	C7	C7	D9	GPIO147/I2C08_SDA/JTAG_CLK		
F8	F8	F8	E7	A9	GPIO150/I2C08_SCL/JTAG_TMS		
L9	L9	L9	H9	K10	GPIO151/ICT4/KSO15		
N10	N10	N10	N12	R13	GPIO152/GPTP-OUT3/KSO16		
		C12	E9	B14	GPIO153/LED2		
A12	A12	A12	A9	B13	GPIO154/I2C02_SDA/PS2_CLK1B		
C9	C9	C9	C9	E10	GPIO155/I2C02_SCL/PS2_DAT1B		
C12	C12	A13	D9	B15	GPIO156/LED0		

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Pin Name	Default (if not GPIO)	Default State (if not In)
B13	B13	B13	B11	C15	GPIO157/LED1		
C4	C4	C4	C3	E5	GPIO161/VCI_IN2#	VCI_IN2#	
A6	A6	A6	A4	A6	GPIO162/VCI_IN1#	VCI_IN1#	
E6	E6	E6	F6	B6	GPIO163/VCI_IN0#	VCI_IN0#	
A9	A9	A9	B7	A10	GPIO165/32KHZ_IN/CTOUT0/TRACECLK		
			G1	E2	GPIO166		
G13	G13	G12	F11	H12	GPIO170/TFCLK/UART1_TX		
G12	G12	G9	E11	H9	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)		In-PU
B6	B6	B6	F5	E6	GPIO172/BGPO3		
			A2	B5	GPIO173/BGPO4		
			E4	B3	GPIO174/BGPO5		
C13	C13	C13	D10	E11	GPIO175/KSO17		
H3	H3	H3	G3	J2	GPIO200/ADC00	ADC00	
J3	J3	J3	H4	K4	GPIO201/ADC01	ADC01	
J2	J2	J2	H3	L4	GPIO202/ADC02	ADC02	
J1	J1	J1	K2	K2	GPIO203/ADC03	ADC03	
H2	H2	H2	J3	L1	GPIO204/ADC04	ADC04	
K3	K3	K3	L2	M2	GPIO205/ADC05	ADC05	
L1	L1	L1	M2	P1	GPIO206/ADC06	ADC06	
K2	K2	K2	L3	N3	GPIO207/ADC07	ADC07	
			H2	J4	GPIO210/ADC08	ADC08	
			J2	H1	GPIO211/ADC09	ADC09	
			K1	J1	GPIO212/ADC10	ADC10	
			J4	K1	GPIO213/ADC11	ADC11	
			J5	L2	GPIO214/ADC12	ADC12	
			K3	N1	GPIO215/ADC13	ADC13	
			K4	N2	GPIO216/ADC14	ADC14	
			K5	P2	GPIO217/ADC15	ADC15	
C1	C1	C1	G7	E1	GPIO221/GPTP-IN3/32KHZ_OUT		
L5	L5	L5	L6	L7	GPIO222/SER_IRQ		
M6	M6	M6	M7	R7	GPIO223/SHD_IO0		
M5	M5	M5	N6	R6	GPIO224/GPTP-IN4/SHD_IO1		
A13	A13		A10	C13	GPIO225/UART0_RTS#		
F2	F2	F2	E3	F1	GPIO226/LED3		
L6	L6	L6	N7	P7	GPIO227/SHD_IO2		

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Pin Name	Default (if not GPIO)	Default State (if not In)
			L8	R11	GPIO230		
			K7	J8	GPIO231		
			G8	L10	GPIO233		
			B1	E4	GPIO234/VCI_IN4#		
		G13	G10	H14	GPIO240		
B8	B8	B8	D6	B10	GPIO241		
A10	A10	A10	D5	A12	GPIO242		
C8	C8	C8	D8	E9	GPIO243		
A11	A11	A11	B8	A13	GPIO244		
B11	B11	B11	C8	B12	GPIO245		
B10	B10	B10	B9	D10	GPIO246		
B9	B9	B9	A8	B11	GPIO254		
G11	G11	G11	F10	G11	JTAG_RST#	JTAG_RST#	
D3	D3	D3	G6	G5	RESETI#	RESETI#	
E5	E5	E5	E6	D5	VBAT	VBAT	
C5	C5	C5	B2	B4	VCI_OUT	VCI_OUT	O2ma-High
F1	F1	F1	E1	D1	VFLT_PLL	VFLT_PLL	
H1	H1	H1	J1	G1	VR_CAP	VR_CAP	
G2	G2	G2	H5	J5	VREF_ADC	VREF_ADC	
F6	F6	F6	E5	B2	VSS1	VSS1	
G3	G3	G3	J7	H8	VSS2	VSS2	
H5	H5	H5	K6	J7	VSS3	VSS3	
K1	K1	K1	L1	M1	VSS_ADC	VSS_ADC	
B4	B4	B4	C4	A3	VSS_ANALOG	VSS_ANALOG	
G5	G5	G5	G4	F4	VTR1	VTR1	
H8	H8	H8	L12	N13	VTR2	VTR2	
H6	H6	H6	J6	P4	VTR3	VTR3	
G6	G6	G6	H8	L5	VTR_ANALOG	VTR_ANALOG	
E1	E1	E1	D1	C1	VTR_PLL	VTR_PLL	
G1	G1	G1	H1	H2	VTR_REG	VTR_REG	
A3	A3	A3	A3	A4	XTAL1	XTAL1	
A1	A1	A1	A1	A2	XTAL2	XTAL2	

2.5 Pin List by Pin Number

2.5.1 POWER RAIL

The Power Rail column defines the power pin that provides I/O power for the signal pin.

2.5.2 PAD TYPES

The Pad Type column defines the type of pad associated with each signal. Some pins have signals with two different pad types sharing the pin; in this case, the pin is shown with the Pin Name but no pad type, followed by rows showing the pad type for each of the signals that share the pin. Pad Types are defined in the Section 50.0, "Electrical Specifications," on page 592.

- I/O Pad Types are defined in Section 50.2.4, "DC Electrical Characteristics for I/O Buffers," on page 595.
- The abbreviation “PWR” is used to denote power pins. The power supplies are defined in Section 50.2.1, "Power Supply Operational Characteristics," on page 593.

2.5.3 GLITCH PROTECTION

Pins with glitch protection are glitch-free tristate pins and will not drive out while their associated power rail is rising. These glitch-free tristate pins require either an external pull-up or pull-down to set the state of the pin high or low.

Note:	If the pin needs to default low, a 1M ohm (max) external pull-down is required.

Pins without glitch protection may be susceptible to transitory changes as the power rail is rising.

Note:	The power rail must rise monotonically in order for glitch protection to operate.

BGPO GLITCH PROTECTION

All BGPO pins are glitch protected while VBAT power is applied.

The BGPO outputs are glitch protected on VBAT power as well as VTR power. As VBAT rises from ground, the BGPOx output are not driven until the VBAT power rail reaches approximately 1V. Once the VBAT power rail reaches approximately 1V, the BGPO outputs drive low.

Note:	It is recommended that a pull-down resistor be added to the BGPO pins.

2.5.4 OVER-VOLTAGE PROTECTION

For pins that have Over-voltage protection and the VTR*x* power rail that is supplying the pin is 3.3V, the pin can tolerate an input voltage of up to 5.5V without causing an error.

Note:	Pins with over-voltage protection may be pulled up externally to 5V supply. It is recommended to select strong pull-up resistor values (less than 10k ohms) that keep the pull-up voltage on the pin less than 3.8V and above 4.5V. If the voltage is 3.8V $\leq$ x $\leq$ 4.5V the pad current will be higher (65ua -nominal).

For pins with Over-voltage protection and the VTR*x* power rail that is supplying the pin is 1.8V, the pin can tolerate an input voltage of up to 3.6V without causing an error.

An input level that exceeds 105% of the power rail on a pin without Over-voltage protection may cause errors in the logic and may additionally damage internal circuitry.

2.5.5 UNDER-VOLTAGE PROTECTION

Pins that are identified as having Under-voltage PROTECTION may be configured so the will not sink excess current if powered by 3.3V and externally pulled up to 1.8V. The following configuration requirements must be met.

- If the pad is an output only pad type and it is configured as either open drain or the output is disabled.

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- If the pin is a GPIO pin with a PIO pad type then is must be configured as open drain output with the input disabled. The input is disabled by setting the GPIO POWER_GATING bits to 11b.

2.5.6 BACKDRIVE PROTECTION

Assuming that the external voltage on the pin is within the parameters defined for the specific pad type, the backdrive protected pin will not sink excess current when it is at a lower potential than the external circuit. There are two cases where this occurs:

- The pad power is off and the external circuit is powered
- The pad power is on and the external circuitry is pulled to a higher potential than the pad power. This may occur on 3.3V powered pads that are 5V tolerant or on 1.8V powered pads that are 3.6V tolerant.

2.5.7 CONFIGURABLE SIGNAL ROUTING

Several sideband signals associated with the LPC bus are routed on two pins, one that is powered by VTR3 and the second powered by VTR2. By connecting VTR3 to 3.3V, VTR2 to 1.8V and using the sideband signals in the VTR2 region, the LPC bus can operate at 3.3V while sideband signals can operate at 1.8V. This configuration corresponds to Intel Atom platforms where the LPC bus can operate at 3.3V, but the sideband signals must be powered at 1.8V. If the sideband signals operate at the same voltage level as the LPC bus, then the VTR3 powered sideband signals should be used and the alternatives in the VTR2 region can be used as GPIOs or other functions.

The signal routing is determined by the alternate function multiplexer programmed in the pin's GPIO Pin Control Register. Software should not enabled signals on more than one pin.

The signals are:

- SER_IRQ
- LRESET#
- LPCPD#
- nSMI
- nEC_SCI

2.5.8 MEC1705/MEC1704/MEC1701/MEC1703 144 WFBGA

MEC1705/MEC1704-144	MEC1701/MEC1703-144	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
A1	A1	XTAL2	VBAT	I_AN				
A2	A2	GPIO062/RESETO#	VTR1	PIO	X		X	
A3	A3	XTAL1	VBAT	I_AN				
A4	A4	GPIO101/BGPO1	VBAT	PIO	X		X	X
A5	A5	BGPO0	VBAT	O2ma	X		X	X
A6	A6	GPIO162/VCI_IN1#	VBAT	PIO	X		X	X
A7	A7	GPIO143/I2C04_SDA/SPI1_MISO/UART0_DTR#/TRACEDAT2	VTR1	PIO	X		X	X
A8	A8	GPIO145/I2C09_SDA/JTAG_TDI	VTR1	PIO	X		X	X
A9	A9	GPIO165/32KHZ_IN/CTOUT0/TRACECLK	VTR1	PIO	X		X	X
A10	A10	GPIO242	VTR1	PIO	X		X	X
A11	A11	GPIO244	VTR1	PIO	X		X	X
A12	A12	GPIO154/I2C02_SDA/PS2_CLK1B	VTR1	PIO	X	X	X	X
A13		GPIO225/UART0_RTS#	VTR1	PIO	X		X	X
	A13	GPIO156/LED0	VTR1	PIO	X	X	X	X
B1	B1	GPIO051/FAN_TACH1/GTACH1	VTR1	PIO	X	X	X	X
B2	B2	GPIO033/RC_ID0	VTR1					
		GPIO033		PIO	X		X	
		RC_ID0		I_AN	X		X	
B3	B3	GPIO000/VCI_IN3#	VBAT	PIO	X		X	X
B4	B4	VSS_ANALOG		PWR				
B5	B5	GPIO102/BGPO2	VBAT	PIO	X		X	X
B6	B6	GPIO172/BGPO3	VBAT	PIO	X		X	X
B7	B7	GPIO141/I2C05_SDA/SPI1_CLK/UART0_DCD#/TRACEDAT0	VTR1	PIO	X		X	X
B8	B8	GPIO241	VTR1	PIO	X		X	X
B9	B9	GPIO254	VTR1	PIO	X		X	X
B10	B10	GPIO246	VTR1	PIO	X		X	X
B11	B11	GPIO245	VTR1	PIO	X		X	X
B12	B12	GPIO007/I2C03_SDA/PS2_CLK0B	VTR1	PIO	X	X	X	X
B13	B13	GPIO157/LED1	VTR1	PIO	X	X	X	X
C1	C1	GPIO221/GPTP-IN3/32KHZ_OUT	VTR1	PIO	X		X	X
C2	C2	GPIO024/GPTP-IN2	VTR1	PIO	X		X	X
C3	C3	GPIO023/GPTP-IN1	VTR1	PIO	X		X	X
C4	C4	GPIO161/VCI_IN2#	VBAT	PIO	X		X	X
C5	C5	VCI_OUT	VBAT	O2ma			X	X
C6	C6	GPIO004/I2C00_SCL/SPI0_MOSI	VTR1	PIO	X		X	X
C7	C7	GPIO147/I2C08_SDA/JTAG_CLK	VTR1	PIO	X		X	X

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MEC1705/MEC1704-144	MEC1701/MEC1703-144	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
C8	C8	GPIO243	VTR1	PIO	X		X	X
C9	C9	GPIO155/I2C02_SCL/PS2_DAT1B	VTR1	PIO	X	X	X	X
C10	C10	GPIO010/I2C03_SCL/PS2_DAT0B	VTR1	PIO	X	X	X	X
C11	C11	GPIO124/GPTP-OUT6/PVT_CS#/KSO11	VTR1	PIO	X		X	X
C12		GPIO156/LED0	VTR1	PIO	X	X	X	X
	C12	GPIO153/LED2	VTR1	PIO	X	X	X	X
C13	C13	GPIO175/KSO17	VTR1	PIO	X		X	X
D1	D1	GPIO057/VCC_PWRGD	VTR1	PIO	X		X	X
D2	D2	GPIO060/KBRST/48MHZ_OUT	VTR1	PIO	X		X	X
D3	D3	RESETI#	VTR1	In	X		X	X
D11	D11	GPIO125/GPTP-OUT5/PVT_CLK/KSO12	VTR1	PIO	X		X	X
D12	D12	GPIO126/PVT_IO3/KSO13	VTR1	PIO	X		X	X
D13	D13	GPIO127/A20M/UART0_CTS#	VTR1	PIO	X		X	X
E1	E1	VTR_PLL		PWR				
E2	E2	GPIO022/GPTP-IN0	VTR1	PIO	X		X	X
E3	E3	GPIO106/PWROK	VTR1	PIO	X		X	X
E5	E5	VBAT		PWR				
E6	E6	GPIO163/VCI_IN0#	VBAT	PIO	X		X	X
E7	E7	GPIO144/I2C04_SCL/SPI1_CS#/UART0_RI#/TRACEDAT3	VTR1	PIO	X		X	X
E8	E8	GPIO045/KSO01	VTR1	PIO	X		X	X
E9	E9	GPIO046/BCM1_DAT/KSO02	VTR1	PIO	X		X	X
E11	E11	GPIO122/BCM0_DAT/PVT_IO1/KSO09	VTR1	PIO	X		X	X
E12	E12	GPIO123/BCM0_CLK/PVT_IO2/KSO10	VTR1	PIO	X		X	X
E13		GPIO134/PWM10/UART1_RTS#	VTR1	PIO	X		X	X
	E13	GPIO035/PWM8/CTOUT1	VTR1	PIO	X	X	X	X
F1	F1	VFLT_PLL		PWR				
F2	F2	GPIO226/LED3	VTR1	PIO	X	X	X	X
F3	F3	GPIO050/FAN_TACH0/GTACH0	VTR1	PIO	X	X	X	X
F5	F5	GPIO003/I2C00_SDA/SPI0_CS#	VTR1	PIO	X		X	X
F6	F6	VSS1		PWR				
F7	F7	GPIO142/I2C05_SCL/SPI1_MOSI/UART0_DSR#/TRACEDAT1	VTR1	PIO	X		X	X
F8	F8	GPIO150/I2C08_SCL/JTAG_TMS	VTR1	PIO	X		X	X
F9	F9	GPIO105/UART0_RX	VTR1	PIO	X		X	X
F11	F11	GPIO104/UART0_TX	VTR1	PIO	X		X	X
F12	F12	GPIO121/PVT_IO0/KSO08	VTR1	PIO	X		X	X
F13	F13	GPIO047/BCM1_CLK/KSO03	VTR1	PIO	X		X	X
G1	G1	VTR_REG		PWR				

MEC1705/MEC1704-144	MEC1701/MEC1703-144	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
G2	G2	VREF_ADC		PWR			X	
G3	G3	VSS2		PWR				
G5	G5	VTR1		PWR				
G6	G6	VTR_ANALOG		PWR				
G8	G8	GPIO146/I2C09_SCL/JTAG_TDO	VTR1	PIO	X		X	X
G9		GPIO135/UART1_CTS#	VTR1	PIO	X		X	X
	G9	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X
G11	G11	JTAG_RST#	VTR1	In	X		X	X
G12		GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X
G13	G12	GPIO170/TFCLK/UART1_TX	VTR1	PIO	X		X	X
	G13	GPIO240	VTR1	PIO	X		X	X
H1	H1	VR_CAP		PWR				
H2	H2	GPIO204/ADC04	VTR1					
		GPIO204		PIO	X		X	
		ADC04		I_AN	X		X	
H3	H3	GPIO200/ADC00	VTR1					
		GPIO200		PIO	X		X	
		ADC00		I_AN	X		X	
H5	H5	VSS3		PWR				
H6	H6	VTR3		PWR				
H7	H7	GPIO100/nEC_SCI	VTR3	PIO	X		X	X
H8	H8	VTR2		PWR				
H9	H9	GPIO114/PS2_CLK0A/nEC_SCI	VTR2	PIO	X		X	X
H11	H11	GPIO044/VREF_VTT	VTR1					
		GPIO044		PIO	X		X	
		VREF_VTT		I_AN	X		X	
H12	H12	GPIO034/RC_ID1/SPI0_CLK	VTR1					
		GPIO034,SPI0_CLK		PIO	X		X	
		RC_ID1		I_AN	X		X	
H13	H13	GPIO036/RC_ID2/SPI0_MISO	VTR1					
		GPIO036,SPI0_MISO		PIO	X		X	
		RC_ID2		I_AN	X		X	
J1	J1	GPIO203/ADC03	VTR1					
		GPIO203		PIO	X		X	
		ADC03		I_AN	X		X	

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MEC1705/MEC1704-144	MEC1701/MEC1703-144	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
J2	J2	GPIO202/ADC02	VTR1					
		GPIO202		PIO	X		X	
		ADC02		I_AN	X		X	
J3	J3	GPIO201/ADC01	VTR1					
		GPIO201		PIO	X		X	
		ADC01		I_AN	X		X	
J5	J5	GPIO064/LRESET#	VTR3	PIO	X		X	X
J6	J6	GPIO011/nSMI	VTR3	PIO	X		X	X
J7	J7	GPIO015/PWM7	VTR2	PIO	X		X	X
J8	J8	GPIO017/GPTP-IN5/KSI0	VTR2	PIO	X		X	X
J9	J9	GPIO030/TIN3/KSI5	VTR2	PIO	X		X	X
J11	J11	GPIO113/PS2_DAT1A/KSO06	VTR2	PIO	X		X	X
J12	J12	GPIO042/PECI_DAT/SB-TSI_DAT	VTR1					
		GPIO042		PIO	X		X	
		PECI_DAT/SB-TSI_DAT		PECI	X		X	
J13	J13	GPIO043/SB-TSI_CLK	VTR1					
		GPIO043		PIO	X		X	
		SB-TSI_CLK		PECI	X		X	
K1	K1	VSS_ADC		PWR				
K2	K2	GPIO207/ADC07	VTR1					
		GPIO207		PIO	X		X	
		ADC07		I_AN	X		X	
K3	K3	GPIO205/ADC05	VTR1					
		GPIO205		PIO	X		X	
		ADC05		I_AN	X		X	
K11	K11	GPIO027/TIN2/KSI4	VTR2	PIO	X		X	X
K12	K12	GPIO120/KSO07	VTR2	PIO	X		X	X
K13	K13	GPIO112/PS2_CLK1A/KSO05	VTR2	PIO	X		X	X
L1	L1	GPIO206/ADC06	VTR1					
		GPIO206		PIO	X		X	
		ADC06		I_AN	X		X	
L2	L2	GPIO067/CLKRUN#	VTR3	PIO	X		X	X
L3	L3	GPIO070/LAD0/ESPI_IO0	VTR3					
		GPIO070/ESPI_IO0		PIO				
		LAD0		PCI				

MEC1705/MEC1704-144	MEC1701/MEC1703-144	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
L4	L4	GPIO073/LAD3/ESPI_IO3	VTR3					
		GPIO073,ESPI_IO3		PIO				
		LAD3		PCI				
L5	L5	GPIO222/SER_IRQ	VTR2					
		GPIO222		PIO				
		SER_IRQ		PCI				
L6	L6	GPIO227/SHD_IO2	VTR2	PIO	X		X	X
L7	L7	GPIO020/KSI1	VTR2	PIO	X		X	X
L8	L8	GPIO052/FAN_TACH2/LRESET#	VTR2	PIO	X		X	X
L9	L9	GPIO151/ICT4/KSO15	VTR2	PIO	X		X	X
L10	L10	GPIO032/GPTP-OUT0/KSI7	VTR2	PIO	X		X	X
L11	L11	GPIO140/I2C06_SCL/ICT5	VTR2	PIO	X		X	X
L12	L12	GPIO054/PWM1/GPWM1	VTR2	PIO	X	X	X	X
L13	L13	GPIO107/nSMI/KSO04	VTR2	PIO	X		X	X
M1	M1	GPIO066/LFRAME#/ESPI_CS#	VTR3	PIO	X		X	X
M2	M2	GPIO065/PCI_CLK/ESPI_CLK	VTR3	PIO	X		X	X
M3	M3	GPIO072/LAD2/ESPI_IO2	VTR3					
		GPIO072/ESPI_IO2		PIO				
		LAD2		PCI				
M4	M4	GPIO063/SER_IRQ/ESPI_ALERT#	VTR3					
		GPIO063/ESPI_ALERT#		PIO				
		SER_IRQ		PCI				
M5	M5	GPIO224/GPTP-IN4/SHD_IO1	VTR2	PIO	X		X	X
M6	M6	GPIO223/SHD_IO0	VTR2	PIO	X		X	X
M7	M7	GPIO013/I2C07_SCL/TOUT2	VTR2	PIO	X		X	X
M8	M8	GPIO002/PWM5	VTR2	PIO	X		X	X
M9	M9	GPIO014/PWM6/GPTP-IN6	VTR2	PIO	X		X	X
M10	M10	GPIO040/GPTP-OUT2/KSO00	VTR2	PIO	X		X	X
M11	M11	GPIO031/GPTP-OUT1/KSI6	VTR2	PIO	X		X	X
M12	M12	GPIO025/TIN0/nEM_INT/UART_CLK	VTR2	PIO	X		X	X
M13	M13	GPIO053/PWM0/GPWM0	VTR2	PIO	X	X	X	X
N1	N1	GPIO061/LPCPD#/ESPI_RESET#	VTR3	PIO	X		X	X
N2	N2	GPIO071/LAD1/ESPI_IO1	VTR3					
		GPIO071/ESPI_IO1		PIO				
		LAD1		PCI				
N3	N3	GPIO016/GPTP-IN7/SHD_IO3/ICT3	VTR2	PIO	X		X	X
N4	N4	GPIO055/PWM2/SHD_CS#/RSMRST#	VTR2	PIO	X		X	X

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MEC1705/MEC1704-144	MEC1701/MEC1703-144	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
N5	N5	GPIO056/PWM3/SHD_CLK	VTR2	PIO	X		X	X
N6	N6	GPIO012/I2C07_SDA/TOUT3	VTR2	PIO	X		X	X
N7	N7	GPIO131/I2C10_SCL/TOUT0	VTR2	PIO	X		X	X
N8	N8	GPIO130/I2C10_SDA/TOUT1	VTR2	PIO	X		X	X
N9	N9	GPIO021/LPCPD#/KSI2	VTR2	PIO	X		X	X
N10	N10	GPIO152/GPTP-OUT3/KSO16	VTR2	PIO	X		X	X
N11	N11	GPIO132/I2C06_SDA/KSO14	VTR2	PIO	X		X	X
N12	N12	GPIO115/PS2_DAT0A	VTR2	PIO	X		X	X
N13	N13	GPIO026/TIN1/KSI3	VTR2	PIO	X		X	X

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MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
A1	XTAL2	VBAT	I_AN				
A2	GPIO173/BGPO4	VBAT	PIO	X		X	X
A3	XTAL1	VBAT	I_AN				
A4	GPIO162/VCI_IN1#	VBAT	PIO	X		X	X
A5	GPIO005/I2C01_SDA/GPTP-OUT4	VTR1	PIO	X		X	X
A6	GPIO143/I2C04_SDA/SPI1_MISO/UART0_DTR#/TRACEDAT2	VTR1	PIO	X		X	X
A7	GPIO141/I2C05_SDA/SPI1_CLK/UART0_DCD#/TRACEDAT0	VTR1	PIO	X		X	X
A8	GPIO254	VTR1	PIO	X		X	X
A9	GPIO154/I2C02_SDA/PS2_CLK1B	VTR1	PIO	X	X	X	X
A10	GPIO225/UART0_RTS#	VTR1	PIO	X		X	X
A11	GPIO127/A20M/UART0_CTS#	VTR1	PIO	X		X	X
A12	GPIO047/BCM1_CLK/KSO03	VTR1	PIO	X		X	X
A13	GPIO104/UART0_TX	VTR1	PIO	X		X	X
B1	GPIO234/VCI_IN4#	VBAT	PIO	X		X	X
B2	VCI_OUT	VBAT	O2ma			X	X

MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
B3	GPIO102/BGPO2	VBAT	PIO	X		X	X
B4	BGPO0	VBAT	O2ma	X		X	X
B5	GPIO004/I2C00_SCL/SPI0_MOSI	VTR1	PIO	X		X	X
B6	GPIO006/I2C01_SCL/GPTP-OUT7	VTR1	PIO	X		X	X
B7	GPIO165/32KHZ_IN/CTOUT0/TRACECLK	VTR1	PIO	X		X	X
B8	GPIO244	VTR1	PIO	X		X	X
B9	GPIO246	VTR1	PIO	X		X	X
B10	GPIO007/I2C03_SDA/PS2_CLK0B	VTR1	PIO	X	X	X	X
B11	GPIO157/LED1	VTR1	PIO	X	X	X	X
B12	GPIO125/GPTP-OUT5/PVT_CLK/KSO12	VTR1	PIO	X		X	X
B13	GPIO124/GPTP-OUT6/PVT_CS#/KSO11	VTR1	PIO	X		X	X
C1	GPIO033/RC_ID0	VTR1					
	GPIO033		PIO	X		X	
	RC_ID0		I_AN	X		X	
C2	GPIO000/VCI_IN3#	VBAT	PIO	X		X	X
C3	GPIO161/VCI_IN2#	VBAT	PIO	X		X	X
C4	VSS_ANALOG		PWR				
C5	GPIO101/BGPO1	VBAT	PIO	X		X	X
C6	GPIO003/I2C00_SDA/SPI0_CS#	VTR1	PIO	X		X	X
C7	GPIO147/I2C08_SDA/JTAG_CLK	VTR1	PIO	X		X	X
C8	GPIO245	VTR1	PIO	X		X	X
C9	GPIO155/I2C02_SCL/PS2_DAT1B	VTR1	PIO	X	X	X	X
C10	GPIO010/I2C03_SCL/PS2_DAT0B	VTR1	PIO	X	X	X	X
C11	GPIO133/PWM9	VTR1	PIO	X	X	X	X
C12	GPIO126/PVT_IO3/KSO13	VTR1	PIO	X		X	X
C13	GPIO123/BCM0_CLK/PVT_IO2/KSO10	VTR1	PIO	X		X	X
D1	VTR_PLL		PWR				
D2	GPIO022/GPTP-IN0	VTR1	PIO	X		X	X
D3	GPIO062/(RESETO#)	VTR1	PIO	X		X	
D4	GPIO144/I2C04_SCL/SPI1_CS#/UART0_RI#/TRACEDAT3	VTR1	PIO	X		X	X
D5	GPIO242	VTR1	PIO	X		X	X
D6	GPIO241	VTR1	PIO	X		X	X
D7	GPIO145/I2C09_SDA/JTAG_TDI	VTR1	PIO	X		X	X
D8	GPIO243	VTR1	PIO	X		X	X
D9	GPIO156/LED0	VTR1	PIO	X	X	X	X

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MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
D10	GPIO175/KSO17	VTR1	PIO	X		X	X
D11	GPIO134/PWM10/UART1_RTS#	VTR1	PIO	X		X	X
D12	GPIO122/BCM0_DAT/PVT_IO1/KSO09	VTR1	PIO	X		X	X
D13	GPIO121/PVT_IO0/KSO08	VTR1	PIO	X		X	X
E1	VFLT_PLL		PWR				
E2	GPIO024/GPTP-IN2	VTR1	PIO	X		X	X
E3	GPIO226/LED3	VTR1	PIO	X	X	X	X
E4	GPIO174/BGPO5	VBAT	PIO	X		X	X
E5	VSS1		PWR				
E6	VBAT		PWR				
E7	GPIO150/I2C08_SCL/JTAG_TMS	VTR1	PIO	X		X	X
E8	GPIO045/KSO01	VTR1	PIO	X		X	X
E9	GPIO153/LED2	VTR1	PIO	X	X	X	X
E10	GPIO046/BCM1_DAT/KSO02	VTR1	PIO	X		X	X
E11	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X
E12	GPIO135/UART1_CTS#	VTR1	PIO	X		X	X
E13	GPIO034/RC_ID1/SPI0_CLK	VTR1					
	GPIO034/SPI0_CLK		PIO	X		X	
	RC_ID1		I_AN	X		X	
F1	GPIO057/VCC_PWRGD	VTR1	PIO	X		X	X
F2	GPIO041	VTR1	PIO	X		X	X
F3	GPIO051/FAN_TACH1/GTACH1	VTR1	PIO	X	X	X	X
F4	GPIO023/GPTP-IN1	VTR1	PIO	X		X	X
F5	GPIO172/BGPO3	VBAT	PIO	X		X	X
F6	GPIO163/VCI_IN0#	VBAT	PIO	X		X	X
F7	GPIO142/I2C05_SCL/SPI1_MOSI/UART0_DSR#/TRACEDAT1	VTR1	PIO	X		X	X
F8	GPIO146/I2C09_SCL/JTAG_TDO	VTR1	PIO	X		X	X
F9	GPIO105/UART0_RX	VTR1	PIO	X		X	X
F10	JTAG_RST#	VTR1	In	X		X	X
F11	GPIO170/TFCLK/UART1_TX	VTR1	PIO	X		X	X
F12	GPIO036/RC_ID2/SPI0_MISO	VTR1					
	GPIO036/SPI0_MISO		PIO	X		X	
	RC_ID2		I_AN	X		X	
F13	GPIO027/TIN2/KSI4	VTR2	PIO	X		X	X
G1	GPIO166	VTR1	PIO	X		X	X

MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
G2	GPIO050/FAN_TACH0/GTACH0	VTR1	PIO	X	X	X	X
G3	GPIO200/ADC00	VTR1					
	GPIO200		PIO	X		X	
	ADC00		I_AN	X		X	
G4	VTR1		PWR				
G5	GPIO060/KBRST/48MHZ_OUT	VTR1	PIO	X		X	X
G6	RESETI#	VTR1	In	X		X	X
G7	GPIO221/GPTP-IN3/32KHZ_OUT	VTR1	PIO	X		X	X
G8	GPIO233	VTR2	PIO	X		X	X
G9	GPIO044/VREF_VTT	VTR1					
	GPIO044		PIO	X		X	
	VREF_VTT		I_AN	X		X	
G10	GPIO240	VTR1	PIO	X		X	X
G11	GPIO035/PWM8/CTOUT1	VTR1	PIO	X	X	X	X
G12	GPIO111/PS2_DAT2	VTR2	PIO	X		X	X
G13	GPIO110/PS2_CLK2	VTR2	PIO	X		X	X
H1	VTR_REG		PWR				
H2	GPIO210/ADC08	VTR1					
	GPIO210		PIO	X		X	
	ADC08		I_AN	X		X	
H3	GPIO202/ADC02	VTR1					
	GPIO202		PIO	X		X	
	ADC02		I_AN	X		X	
H4	GPIO201/ADC01	VTR1					
	GPIO201		PIO	X		X	
	ADC01		I_AN	X		X	
H5	VREF_ADC		PWR			X	
H6	GPIO106/PWROK	VTR1	PIO	X		X	X
H7	GPIO013/I2C07_SCL/TOUT2	VTR2	PIO	X		X	X
H8	VTR_ANALOG		PWR				
H9	GPIO151/ICT4/KSO15	VTR2	PIO	X		X	X
H10	GPIO042/PECI_DAT/SB-TSI_DAT	VTR1					
	GPIO042		PIO	X		X	
	PECI_DAT/SB-TSI_DAT		PECI	X		X	

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MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
H11	GPIO043/SB-TSI_CLK	VTR1					
	GPIO043		PIO	X		X	
	SB-TSI_CLK		PECI	X		X	
H12	GPIO120/KSO07	VTR2	PIO	X		X	X
H13	GPIO107/nSMI/KSO04	VTR2	PIO	X		X	X
J1	VR_CAP		PWR				
J2	GPIO211/ADC09	VTR1					
	GPIO211		PIO	X		X	
	ADC09		I_AN	X		X	
J3	GPIO204/ADC04	VTR1					
	GPIO204		PIO	X		X	
	ADC04		I_AN	X		X	
J4	GPIO213/ADC11	VTR1					
	GPIO213		PIO	X		X	
	ADC11		I_AN	X		X	
J5	GPIO214/ADC12	VTR1					
	GPIO214		PIO	X		X	
	ADC12		I_AN	X		X	
J6	VTR3		PWR				
J7	VSS2		PWR				
J8	GPIO130/I2C10_SDA/TOUT1	VTR2	PIO	X		X	X
J9	GPIO017/GPTP-IN5/KSI0	VTR2	PIO	X		X	X
J10	GPIO114/PS2_CLK0A/nEC_SCI	VTR2	PIO	X		X	X
J11	GPIO113/PS2_DAT1A/KSO06	VTR2	PIO	X		X	X
J12	GPIO112/PS2_CLK1A/KSO05	VTR2	PIO	X		X	X
J13	GPIO030/TIN3/KSI5	VTR2	PIO	X		X	X
K1	GPIO212/ADC10	VTR1					
	GPIO212		PIO	X		X	
	ADC10		I_AN	X		X	
K2	GPIO203/ADC03	VTR1					
	GPIO203		PIO	X		X	
	ADC03		I_AN	X		X	
K3	GPIO215/ADC13	VTR1					
	GPIO215		PIO	X		X	
	ADC13		I_AN	X		X	

MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
K4	GPIO216/ADC14	VTR1					
	GPIO216		PIO	X		X	
	ADC14		I_AN	X		X	
K5	GPIO217/ADC15	VTR1					
	GPIO217		PIO	X		X	
	ADC15		I_AN	X		X	
K6	VSS3		PWR				
K7	GPIO231	VTR2	PIO	X		X	X
K8	GPIO052/FAN_TACH2/LRESET#	VTR2	PIO	X		X	X
K9	GPIO032/GPTP-OUT0/KSI7	VTR2	PIO	X		X	X
K10	GPIO054/PWM1/GPWM1	VTR2	PIO	X	X	X	X
K11	GPIO053/PWM0/GPWM0	VTR2	PIO	X	X	X	X
K12	GPIO025/TIN0/nEM_INT/UART_CLK	VTR2	PIO	X		X	X
K13	GPIO140/I2C06_SCL/ICT5	VTR2	PIO	X		X	X
L1	VSS_ADC		PWR				
L2	GPIO205/ADC05	VTR1					
	GPIO205		PIO	X		X	
	ADC05		I_AN	X		X	
L3	GPIO207/ADC07	VTR1					
	GPIO207		PIO	X		X	
	ADC07		I_AN	X		X	
L4	GPIO100/nEC_SCI	VTR3	PIO	X		X	X
L5	GPIO011/nSMI	VTR3	PIO	X		X	X
L6	GPIO222/SER_IRQ	VTR2					
	GPIO222		PIO				
	SER_IRQ		PCI				
L7	GPIO012/I2C07_SDA/TOUT3	VTR2	PIO	X		X	X
L8	GPIO230	VTR2	PIO	X		X	X
L9	GPIO020/KSI1	VTR2	PIO	X		X	X
L10	GPIO132/I2C06_SDA/KSO14	VTR2	PIO	X		X	X
L11	GPIO026/TIN1/KSI3	VTR2	PIO	X		X	X
L12	VTR2		PWR				
L13	GPIO115/PS2_DAT0A	VTR2	PIO	X		X	X
M1	GPIO061/LPCPD#/ESPI_RESET#	VTR3	PIO	X		X	X

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MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
M2	GPIO206/ADC06	VTR1					
	GPIO206		PIO	X		X	
	ADC06		I_AN	X		X	
M3	GPIO064/LRESET#	VTR3	PIO	X		X	X
M4	GPIO070/LAD0/ESPI_IO0	VTR3					
	GPIO070/ESPI_IO0		PIO				
	LAD0		PCI				
M5	GPIO067/CLKRUN#	VTR3	PIO	X		X	X
M6	GPIO073/LAD3/ESPI_IO3	VTR3					
	GPIO073/ESPI_IO3		PIO				
	LAD3		PCI				
M7	GPIO223/SHD_IO0	VTR2	PIO	X		X	X
M8	GPIO055/PWM2/SHD_CS#/(RSMRST#)	VTR2	PIO	X		X	X
M9	GPIO021/LPCPD#/KSI2	VTR2	PIO	X		X	X
M10	GPIO014/PWM6/GPTP-IN6	VTR2	PIO	X		X	X
M11	GPIO040/GPTP-OUT2/KSO00	VTR2	PIO	X		X	X
M12	GPIO015/PWM7	VTR2	PIO	X		X	X
M13	GPIO031/GPTP-OUT1/KSI6	VTR2	PIO	X		X	X
N1	GPIO066/LFRAME#/ESPI_CS#	VTR3	PIO	X		X	X
N2	GPIO065/PCI_CLK/ESPI_CLK	VTR3	PIO	X		X	X
N3	GPIO071/LAD1/ESPI_IO1	VTR3					
	GPIO071/ESPI_IO1		PIO				
	LAD1		PCI				
N4	GPIO072/LAD2/ESPI_IO2	VTR3					
	GPIO072/ESPI_IO2		PIO				
	LAD2		PCI				
N5	GPIO063/SER_IRQ/ESPI_ALERT#	VTR3					
	GPIO063/ESPI_ALERT#		PIO				
	SER_IRQ		PCI				
N6	GPIO224/GPTP-IN4/SHD_IO1	VTR2	PIO	X		X	X
N7	GPIO227/SHD_IO2	VTR2	PIO	X		X	X
N8	GPIO016/GPTP-IN7/SHD_IO3/ICT3	VTR2	PIO	X		X	X
N9	GPIO056/PWM3/SHD_CLK	VTR2	PIO	X		X	X
N10	GPIO131/I2C10_SCL/TOUT0	VTR2	PIO	X		X	X
N11	GPIO001/PWM4	VTR2	PIO	X		X	X

MEC1701/MEC1703-169 WFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
N12	GPIO152/GPTP-OUT3/KSO16	VTR2	PIO	X		X	X
N13	GPIO002/PWM5	VTR2	PIO	X		X	X

2.5.10 MEC1701/MEC1703 169 XFBGA

MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
A2	XTAL2	VBAT	I_AN				
A3	VSS_ANALOG		PWR				
A4	XTAL1	VBAT	I_AN				
A5	GPIO102/BGPO2	VBAT	PIO	X		X	X
A6	GPIO162/VCI_IN1#	VBAT	PIO	X		X	X
A7	GPIO006/I2C01_SCL/GPTP-OUT7	VTR1	PIO	X		X	X
A8	GPIO143/I2C04_SDA/SPI1_MISO/UART0_DTR#/TRACEDAT2	VTR1	PIO	X		X	X
A9	GPIO150/I2C08_SCL/JTAG_TMS	VTR1	PIO	X		X	X
A10	GPIO165/32KHZ_IN/CTOUT0/TRACECLK	VTR1	PIO	X		X	X
A11	GPIO045/KSO01	VTR1	PIO	X		X	X
A12	GPIO242	VTR1	PIO	X		X	X
A13	GPIO244	VTR1	PIO	X		X	X
A14	GPIO007/I2C03_SDA/PS2_CLK0B	VTR1	PIO	X	X	X	X
B1	GPIO033/RC_ID0	VTR1					
	GPIO033		PIO	X		X	
	RC_ID0		I_AN	X		X	
B2	VSS1		PWR				
B3	GPIO174/BGPO5	VBAT	PIO	X		X	X
B4	VCI_OUT	VBAT	O2ma			X	X
B5	GPIO173/BGPO4	VBAT	PIO	X		X	X

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MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
B6	GPIO163/VCI_IN0#	VBAT	PIO	X		X	X
B7	GPIO003/I2C00_SDA/SPI0_CS#	VTR1	PIO	X		X	X
B8	GPIO141/I2C05_SDA/SPI1_CLK/UART0_DCD#/TRACEDAT0	VTR1	PIO	X		X	X
B9	GPIO146/I2C09_SCL/JTAG_TDO	VTR1	PIO	X		X	X
B10	GPIO241	VTR1	PIO	X		X	X
B11	GPIO254	VTR1	PIO	X		X	X
B12	GPIO245	VTR1	PIO	X		X	X
B13	GPIO154/I2C02_SDA/PS2_CLK1B	VTR1	PIO	X	X	X	X
B14	GPIO153/LED2	VTR1	PIO	X	X	X	X
B15	GPIO156/LED0	VTR1	PIO	X	X	X	X
C1	VTR_PLL		PWR				
C2	GPIO062/(RESETO#)	VTR1	PIO	X		X	
C3	GPIO000/VCI_IN3#	VBAT	PIO	X		X	X
C13	GPIO225/UART0_RTS#	VTR1	PIO	X		X	X
C14	GPIO133/PWM9	VTR1	PIO	X	X	X	X
C15	GPIO157/LED1	VTR1	PIO	X	X	X	X
D1	VFLT_PLL		PWR				
D2	GPIO022/GPTP-IN0	VTR1	PIO	X		X	X
D5	VBAT		PWR				
D6	BGPO0	VBAT	O2ma	X		X	X
D7	GPIO004/I2C00_SCL/SPI0_MOSI	VTR1	PIO	X		X	X
D8	GPIO142/I2C05_SCL/SPI1_MOSI/UART0_DSR#/TRACEDAT1	VTR1	PIO	X		X	X
D9	GPIO147/I2C08_SDA/JTAG_CLK	VTR1	PIO	X		X	X
D10	GPIO246	VTR1	PIO	X		X	X
D11	GPIO010/I2C03_SCL/PS2_DAT0B	VTR1	PIO	X	X	X	X
D14	GPIO125/GPTP-OUT5/PVT_CLK/KSO12	VTR1	PIO	X		X	X
D15	GPIO127/A20M/UART0_CTS#	VTR1	PIO	X		X	X
E1	GPIO221/GPTP-IN3/32KHZ_OUT	VTR1	PIO	X		X	X
E2	GPIO166	VTR1	PIO	X		X	X
E4	GPIO234/VCI_IN4#	VBAT	PIO	X		X	X
E5	GPIO161/VCI_IN2#	VBAT	PIO	X		X	X
E6	GPIO172/BGPO3	VBAT	PIO	X		X	X
E7	GPIO005/I2C01_SDA/GPTP-OUT4	VTR1	PIO	X		X	X
E8	GPIO144/I2C04_SCL/SPI1_CS#/UART0_RI#/TRACEDAT3	VTR1	PIO	X		X	X
E9	GPIO243	VTR1	PIO	X		X	X

MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
E10	GPIO155/I2C02_SCL/PS2_DAT1B	VTR1	PIO	X	X	X	X
E11	GPIO175/KSO17	VTR1	PIO	X		X	X
E12	GPIO124/GPTP-OUT6/PVT_CS#/KSO11	VTR1	PIO	X		X	X
E14	GPIO126/PVT_IO3/KSO13	VTR1	PIO	X		X	X
E15	GPIO047/BCM1_CLK/KSO03	VTR1	PIO	X		X	X
F1	GPIO226/LED3	VTR1	PIO	X	X	X	X
F2	GPIO051/FAN_TACH1/GTACH1	VTR1	PIO	X	X	X	X
F4	VTR1		PWR				
F5	GPIO023/GPTP-IN1	VTR1	PIO	X		X	X
F6	GPIO101/BGPO1	VBAT	PIO	X		X	X
F10	GPIO046/BCM1_DAT/KSO02	VTR1	PIO	X		X	X
F11	GPIO105/UART0_RX	VTR1	PIO	X		X	X
F12	GPIO121/PVT_IO0/KSO08	VTR1	PIO	X		X	X
F14	GPIO122/BCM0_DAT/PVT_IO1/KSO09	VTR1	PIO	X		X	X
F15	GPIO104/UART0_TX	VTR1	PIO	X		X	X
G1	VR_CAP		PWR				
G2	GPIO057/VCC_PWRGD	VTR1	PIO	X		X	X
G4	GPIO024/GPTP-IN2	VTR1	PIO	X		X	X
G5	RESETI#	VTR1	In	X		X	X
G7	GPIO106/PWROK	VTR1	PIO	X		X	X
G8	GPIO145/I2C09_SDA/JTAG_TDI	VTR1	PIO	X		X	X
G9	GPIO135/UART1_CTS#	VTR1	PIO	X		X	X
G11	JTAG_RST#	VTR1	In	X		X	X
G12	GPIO123/BCM0_CLK/PVT_IO2/KSO10	VTR1	PIO	X		X	X
G14	GPIO134/PWM10/UART1_RTS#	VTR1	PIO	X		X	X
G15	GPIO035/PWM8/CTOUT1	VTR1	PIO	X	X	X	X
H1	GPIO211/ADC09	VTR1					
	GPIO211		PIO	X		X	
	ADC09		I_AN	X		X	
H2	VTR_REG		PWR				
H4	GPIO041	VTR1	PIO	X		X	X
H5	GPIO050/FAN_TACH0/GTACH0	VTR1	PIO	X	X	X	X
H7	GPIO060/KBRST/48MHZ_OUT	VTR1	PIO	X		X	X
H8	VSS2		PWR				
H9	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X

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MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
H11	GPIO025/TIN0/nEM_INT/UART_CLK	VTR2	PIO	X		X	X
H12	GPIO170/TFCLK/UART1_TX	VTR1	PIO	X		X	X
H14	GPIO240	VTR1	PIO	X		X	X
H15	GPIO034/RC_ID1/SPI0_CLK	VTR1					
	GPIO034/SPI0_CLK		PIO	X		X	
	RC_ID1		I_AN	X		X	
J1	GPIO212/ADC10	VTR1					
	GPIO212		PIO	X		X	
	ADC10		I_AN	X		X	
J2	GPIO200/ADC00	VTR1					
	GPIO200		PIO	X		X	
	ADC00		I_AN	X		X	
J4	GPIO210/ADC08	VTR1					
	GPIO210		PIO	X		X	
	ADC08		I_AN	X		X	
J5	VREF_ADC		PWR			X	
J7	VSS3		PWR				
J8	GPIO231	VTR2	PIO	X		X	X
J9	GPIO015/PWM7	VTR2	PIO	X		X	X
J11	GPIO140/I2C06_SCL/ICT5	VTR2	PIO	X		X	X
J12	GPIO036/RC_ID2/SPI0_MISO	VTR1					
	GPIO036/SPI0_MISO		PIO	X		X	
	RC_ID2		I_AN	X		X	
J14	GPIO043/SB-TSI_CLK	VTR1					
	GPIO043		PIO	X		X	
	SB-TSI_CLK		PECI	X		X	
J15	GPIO042/PECI_DAT/SB-TSI_DAT	VTR1					
	GPIO042		PIO	X		X	
	PECI_DAT/SB-TSI_DAT		PECI	X		X	
K1	GPIO213/ADC11	VTR1					
	GPIO213		PIO	X		X	
	ADC11		I_AN	X		X	
K2	GPIO203/ADC03	VTR1					
	GPIO203		PIO	X		X	
	ADC03		I_AN	X		X	

MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
K4	GPIO201/ADC01	VTR1					
	GPIO201		PIO	X		X	
	ADC01		I_AN	X		X	
K5	GPIO067/CLKRUN#	VTR3	PIO	X		X	X
K6	GPIO011/nSMI	VTR3	PIO	X		X	X
K10	GPIO151/ICT4/KSO15	VTR2	PIO	X		X	X
K11	GPIO017/GPTP-IN5/KSI0	VTR2	PIO	X		X	X
K12	GPIO044/VREF_VTT	VTR1					
	GPIO044		PIO	X		X	
	VREF_VTT		I_AN	X		X	
K14	GPIO114/PS2_CLK0A/nEC_SCI	VTR2	PIO	X		X	X
K15	GPIO112/PS2_CLK1A/KSO05	VTR2	PIO	X		X	X
L1	GPIO204/ADC04	VTR1					
	GPIO204		PIO	X		X	
	ADC04		I_AN	X		X	
L2	GPIO214/ADC12	VTR1					
	GPIO214		PIO	X		X	
	ADC12		I_AN	X		X	
L4	GPIO202/ADC02	VTR1					
	GPIO202		PIO	X		X	
	ADC02		I_AN	X		X	
L5	VTR_ANALOG		PWR				
L6	GPIO100/nEC_SCI	VTR3	PIO	X		X	X
L7	GPIO222/SER_IRQ	VTR2					
	GPIO222		PIO				
	SER_IRQ		PCI				
L8	GPIO052/FAN_TACH2/LRESET#	VTR2	PIO	X		X	X
L9	GPIO002/PWM5	VTR2	PIO	X		X	X
L10	GPIO233	VTR2	PIO	X		X	X
L11	GPIO040/GPTP-OUT2/KSO00	VTR2	PIO	X		X	X
L12	GPIO111/PS2_DAT2	VTR2	PIO	X		X	X
L14	GPIO113/PS2_DAT1A/KSO06	VTR2	PIO	X		X	X
L15	GPIO110/PS2_CLK2	VTR2	PIO	X		X	X
M1	VSS_ADC		PWR				

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MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
M2	GPIO205/ADC05	VTR1					
	GPIO205		PIO	X		X	
	ADC05		I_AN	X		X	
M5	GPIO064/LRESET#	VTR3	PIO	X		X	X
M6	GPIO061/LPCPD#/ESPI_RESET#	VTR3	PIO	X		X	X
M7	GPIO016/GPTP-IN7/SHD_IO3/ICT3	VTR2	PIO	X		X	X
M8	GPIO055/PWM2/SHD_CS#/(RSMRST#)	VTR2	PIO	X		X	X
M9	GPIO056/PWM3/SHD_CLK	VTR2	PIO	X		X	X
M10	GPIO032/GPTP-OUT0/KSI7	VTR2	PIO	X		X	X
M11	GPIO031/GPTP-OUT1/KSI6	VTR2	PIO	X		X	X
M14	GPIO107/nSMI/KSO04	VTR2	PIO	X		X	X
M15	GPIO120/KSO07	VTR2	PIO	X		X	X
N1	GPIO215/ADC13	VTR1					
	GPIO215		PIO	X		X	
	ADC13		I_AN	X		X	
N2	GPIO216/ADC14	VTR1					
	GPIO216		PIO	X		X	
	ADC14		I_AN	X		X	
N3	GPIO207/ADC07	VTR1					
	GPIO207		PIO	X		X	
	ADC07		I_AN	X		X	
N13	VTR2		PWR				
N14	GPIO030/TIN3/KSI5	VTR2	PIO	X		X	X
N15	GPIO054/PWM1/GPWM1	VTR2	PIO	X	X	X	X
P1	GPIO206/ADC06	VTR1					
	GPIO206		PIO	X		X	
	ADC06		I_AN	X		X	
P2	GPIO217/ADC15	VTR1					
	GPIO217		PIO	X		X	
	ADC15		I_AN	X		X	
P3	GPIO066/LFRAME#/ESPI_CS#	VTR3	PIO	X		X	X
P4	VTR3		PWR				
P5	GPIO072/LAD2/ESPI_IO2	VTR3					
	GPIO072/ESPI_IO2		PIO				
	LAD2		PCI				

MEC1701/MEC1703-169 XFBGA	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
P6	GPIO063/SER_IRQ/ESPI_ALERT#	VTR3					
	GPIO063/ESPI_ALERT#		PIO				
	SER_IRQ		PCI				
P7	GPIO227/SHD_IO2	VTR2	PIO	X		X	X
P8	GPIO012/I2C07_SDA/TOUT3	VTR2	PIO	X		X	X
P9	GPIO130/I2C10_SDA/TOUT1	VTR2	PIO	X		X	X
P10	GPIO021/LPCPD#/KSI2	VTR2	PIO	X		X	X
P11	GPIO014/PWM6/GPTP-IN6	VTR2	PIO	X		X	X
P12	GPIO026/TIN1/KSI3	VTR2	PIO	X		X	X
P13	GPIO115/PS2_DAT0A	VTR2	PIO	X		X	X
P14	GPIO053/PWM0/GPWM0	VTR2	PIO	X	X	X	X
P15	GPIO027/TIN2/KSI4	VTR2	PIO	X		X	X
R2	GPIO065/PCI_CLK/ESPI_CLK	VTR3	PIO	X		X	X
R3	GPIO070/LAD0/ESPI_IO0	VTR3					
	GPIO070/ESPI_IO0		PIO				
	LAD0		PCI				
R4	GPIO071/LAD1/ESPI_IO1	VTR3					
	GPIO071/ESPI_IO1		PIO				
	LAD1		PCI				
R5	GPIO073/LAD3/ESPI_IO3	VTR3					
	GPIO073/ESPI_IO3		PIO				
	LAD3		PCI				
R6	GPIO224/GPTP-IN4/SHD_IO1	VTR2	PIO	X		X	X
R7	GPIO223/SHD_IO0	VTR2	PIO	X		X	X
R8	GPIO013/I2C07_SCL/TOUT2	VTR2	PIO	X		X	X
R9	GPIO020/KSI1	VTR2	PIO	X		X	X
R10	GPIO131/I2C10_SCL/TOUT0	VTR2	PIO	X		X	X
R11	GPIO230	VTR2	PIO	X		X	X
R12	GPIO001/PWM4	VTR2	PIO	X		X	X
R13	GPIO152/GPTP-OUT3/KSO16	VTR2	PIO	X		X	X
R14	GPIO132/I2C06_SDA/KSO14	VTR2	PIO	X		X	X

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2.6 Signal Description by Signal

EMULATED POWER WELL

Power well emulation for GPIOs and for signals that are multiplexed with GPIO signals is controlled by the POWER_-GATING field in the GPIO Pin Control Register. Power well emulation for signals that are not multiplexed with GPIO signals is defined by the entries in this column.

GATED STATE

This column defines the internal value of an input signal when either its emulated power well is inactive or it is not selected by the GPIO alternate function MUX. A value of “No Gate” means that the internal signal always follows the pin even when the emulated power well is inactive.

Note: Gated state is only meaningful to the operation of input signals. A gated state on an output pin defines the internal behavior of the GPIO MUX and does not imply pin behavior.

Signal	Emulated Power Rail	Gated State	Notes
32KHZ_IN	VTR	Low	
32KHZ_OUT	VTR	Low	
48MHZ_OUT	VTR	Low	
A20M	VTR	Low	
ADC00	VTR	Low	
ADC01	VTR	Low	
ADC02	VTR	Low	
ADC03	VTR	Low	
ADC04	VTR	Low	
ADC05	VTR	Low	
ADC06	VTR	Low	
ADC07	VTR	Low	
ADC08	VTR	Low	
ADC09	VTR	Low	
ADC10	VTR	Low	
ADC11	VTR	Low	
ADC12	VTR	Low	
ADC13	VTR	Low	
ADC14	VTR	Low	
ADC15	VTR	Low	
BCM0_CLK	VTR	Low	
BCM0_DAT	VTR	Low	Note 3
BCM1_CLK	VTR	Low	
BCM1_DAT	VTR	Low	Note 3
BGPO0	VTR	Low	
BGPO1	VTR	Low	Note 8
BGPO2	VTR	Low	Note 8
BGPO3	VTR	Low	Note 8
BGPO4	VTR	Low	Note 8

Signal	Emulated Power Rail	Gated State	Notes
BGPO5	VTR	Low	Note 8
CLKRUN#	VTR	High	
CTOUT0	VTR	Low	
CTOUT1	VTR	Low	
ESPI_ALERT#	VTR	High	
ESPI_CLK	VTR	Low	
ESPI_CS#	VTR	High	
ESPI_IO0	VTR	Low	
ESPI_IO1	VTR	Low	
ESPI_IO2	VTR	Low	
ESPI_IO3	VTR	Low	
ESPI_RESET#	VTR	High	
FAN_TACH0	VTR	Low	
FAN_TACH1	VTR	Low	
FAN_TACH2	VTR	Low	
GPIO000	VTR	No Gate	
GPIO001	VTR	No Gate	
GPIO002	VTR	No Gate	
GPIO003	VTR	No Gate	
GPIO004	VTR	No Gate	
GPIO005	VTR	No Gate	
GPIO006	VTR	No Gate	
GPIO007	VTR	No Gate	
GPIO010	VTR	No Gate	
GPIO011	VTR	No Gate	
GPIO012	VTR	No Gate	
GPIO013	VTR	No Gate	
GPIO014	VTR	No Gate	
GPIO015	VTR	No Gate	
GPIO016	VTR	No Gate	
GPIO017	VTR	No Gate	
GPIO020	VTR	No Gate	
GPIO021	VTR	No Gate	
GPIO022	VTR	No Gate	
GPIO023	VTR	No Gate	
GPIO024	VTR	No Gate	
GPIO025	VTR	No Gate	
GPIO026	VTR	No Gate	
GPIO027	VTR	No Gate	
GPIO030	VTR	No Gate	
GPIO031	VTR	No Gate	
GPIO032	VTR	No Gate	
GPIO033	VTR	No Gate	

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Signal	Emulated Power Rail	Gated State	Notes
GPIO034	VTR	No Gate	
GPIO035	VTR	No Gate	
GPIO036	VTR	No Gate	
GPIO040	VTR	No Gate	
GPIO041	VTR	No Gate	
GPIO042	VTR	No Gate	
GPIO043	VTR	No Gate	
GPIO044	VTR	No Gate	
GPIO045	VTR	No Gate	
GPIO046	VTR	No Gate	
GPIO047	VTR	No Gate	
GPIO050	VTR	No Gate	
GPIO051	VTR	No Gate	
GPIO052	VTR	No Gate	
GPIO053	VTR	No Gate	
GPIO054	VTR	No Gate	
GPIO055	VTR	No Gate	
GPIO056	VTR	No Gate	
GPIO057	VTR	No Gate	
GPIO060	VTR	No Gate	
GPIO061	VTR	No Gate	
GPIO062	VTR	No Gate	Note 7
GPIO063	VTR	No Gate	
GPIO064	VTR	No Gate	
GPIO065	VTR	No Gate	
GPIO066	VTR	No Gate	
GPIO067	VTR	No Gate	
GPIO070	VTR	No Gate	
GPIO071	VTR	No Gate	
GPIO072	VTR	No Gate	
GPIO073	VTR	No Gate	
GPIO100	VTR	No Gate	
GPIO101	VTR	No Gate	
GPIO102	VTR	No Gate	
GPIO104	VTR	No Gate	
GPIO105	VTR	No Gate	
GPIO106	VTR	No Gate	
GPIO107	VTR	No Gate	
GPIO110	VTR	No Gate	
GPIO111	VTR	No Gate	
GPIO112	VTR	No Gate	
GPIO113	VTR	No Gate	
GPIO114	VTR	No Gate	

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Signal	Emulated Power Rail	Gated State	Notes
GPIO115	VTR	No Gate	
GPIO120	VTR	No Gate	
GPIO121	VTR	No Gate	
GPIO122	VTR	No Gate	
GPIO123	VTR	No Gate	
GPIO124	VTR	No Gate	
GPIO125	VTR	No Gate	
GPIO126	VTR	No Gate	
GPIO127	VTR	No Gate	
GPIO130	VTR	No Gate	
GPIO131	VTR	No Gate	
GPIO132	VTR	No Gate	
GPIO133	VTR	No Gate	
GPIO134	VTR	No Gate	
GPIO135	VTR	No Gate	
GPIO140	VTR	No Gate	
GPIO141	VTR	No Gate	
GPIO142	VTR	No Gate	
GPIO143	VTR	No Gate	
GPIO144	VTR	No Gate	
GPIO145	VTR	No Gate	
GPIO146	VTR	No Gate	
GPIO147	VTR	No Gate	
GPIO150	VTR	No Gate	
GPIO151	VTR	No Gate	
GPIO152	VTR	No Gate	
GPIO153	VTR	No Gate	
GPIO154	VTR	No Gate	
GPIO155	VTR	No Gate	
GPIO156	VTR	No Gate	
GPIO157	VTR	No Gate	
GPIO160	VTR	No Gate	
GPIO161	VTR	No Gate	
GPIO162	VTR	No Gate	
GPIO163	VTR	No Gate	
GPIO165	VTR	No Gate	
GPIO166	VTR	No Gate	
GPIO170	VTR	No Gate	
GPIO171	VTR	No Gate	
GPIO172	VTR	No Gate	
GPIO173	VTR	No Gate	
GPIO174	VTR	No Gate	
GPIO175	VTR	No Gate	

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Signal	Emulated Power Rail	Gated State	Notes
GPIO200	VTR	No Gate	
GPIO201	VTR	No Gate	
GPIO202	VTR	No Gate	
GPIO203	VTR	No Gate	
GPIO204	VTR	No Gate	
GPIO205	VTR	No Gate	
GPIO206	VTR	No Gate	
GPIO207	VTR	No Gate	
GPIO210	VTR	No Gate	
GPIO211	VTR	No Gate	
GPIO212	VTR	No Gate	
GPIO213	VTR	No Gate	
GPIO214	VTR	No Gate	
GPIO215	VTR	No Gate	
GPIO216	VTR	No Gate	
GPIO217	VTR	No Gate	
GPIO221	VTR	No Gate	
GPIO222	VTR	No Gate	
GPIO223	VTR	No Gate	
GPIO224	VTR	No Gate	
GPIO225	VTR	No Gate	
GPIO226	VTR	No Gate	
GPIO227	VTR	No Gate	
GPIO230	VTR	No Gate	
GPIO231	VTR	No Gate	
GPIO233	VTR	No Gate	
GPIO234	VTR	No Gate	
GPIO240	VTR	No Gate	
GPIO241	VTR	No Gate	
GPIO242	VTR	No Gate	
GPIO243	VTR	No Gate	
GPIO244	VTR	No Gate	
GPIO245	VTR	No Gate	
GPIO246	VTR	No Gate	
GPIO254	VTR	No Gate	
GPTP-IN0	VTR	No Gate	
GPTP-IN1	VTR	No Gate	
GPTP-IN2	VTR	No Gate	
GPTP-IN3	VTR	No Gate	
GPTP-IN4	VTR	No Gate	
GPTP-IN5	VTR	No Gate	
GPTP-IN6	VTR	No Gate	
GPTP-IN7	VTR	No Gate	

Signal	Emulated Power Rail	Gated State	Notes
GPTP-OUT0	VTR	No Gate	Note 16
GPTP-OUT1	VTR	No Gate	Note 16
GPTP-OUT2	VTR	No Gate	Note 16
GPTP-OUT3	VTR	No Gate	Note 16
GPTP-OUT4	VTR	No Gate	Note 16
GPTP-OUT5	VTR	No Gate	Note 16
GPTP-OUT6	VTR	No Gate	Note 16
GPTP-OUT7	VTR	No Gate	Note 16
GPWM0	VTR	Low	
GPWM1	VTR	Low	
GTACH0	VTR	Low	
GTACH1	VTR	Low	
I2C00_SCL	VTR	High	Note 14
I2C00_SDA	VTR	High	Note 14
I2C01_SCL	VTR	High	Note 14
I2C01_SDA	VTR	High	Note 14
I2C02_SCL	VTR	High	Note 14
I2C02_SDA	VTR	High	Note 14
I2C03_SCL	VTR	High	Note 14
I2C03_SDA	VTR	High	Note 14
I2C04_SCL	VTR	High	Note 14
I2C04_SDA	VTR	High	Note 14
I2C05_SCL	VTR	High	Note 14
I2C05_SDA	VTR	High	Note 14
I2C06_SCL	VTR	High	Note 14
I2C06_SDA	VTR	High	Note 14
I2C07_SCL	VTR	High	Note 14
I2C07_SDA	VTR	High	Note 14
I2C08_SCL	VTR	High	Note 14
I2C08_SDA	VTR	High	Note 14
I2C09_SCL	VTR	High	Note 14
I2C09_SDA	VTR	High	Note 14
I2C10_SCL	VTR	High	Note 14
I2C10_SDA	VTR	High	Note 14
ICT3	VTR	Low	
ICT4	VTR	Low	
ICT5	VTR	Low	
JTAG_CLK	VTR	Low	
JTAG_RST#	VTR	High	Note 5
JTAG_TDI	VTR	Low	
JTAG_TDO	VTR	Low	
JTAG_TMS	VTR	Low	
KBRST	VTR	Low	

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Signal	Emulated Power Rail	Gated State	Notes
KSI0	VTR	Low	
KSI1	VTR	Low	
KSI2	VTR	Low	
KSI3	VTR	Low	
KSI4	VTR	Low	
KSI5	VTR	Low	
KSI6	VTR	Low	
KSI7	VTR	Low	
KSO00	VTR	Low	
KSO01	VTR	Low	
KSO02	VTR	Low	
KSO03	VTR	Low	
KSO04	VTR	Low	
KSO05	VTR	Low	
KSO06	VTR	Low	
KSO07	VTR	Low	
KSO08	VTR	Low	
KSO09	VTR	Low	
KSO10	VTR	Low	
KSO11	VTR	Low	
KSO12	VTR	Low	
KSO13	VTR	Low	
KSO14	VTR	Low	
KSO15	VTR	Low	
KSO16	VTR	Low	
KSO17	VTR	Low	
LAD0	VCC	No Gate	Note 2
LAD1	VCC	No Gate	Note 2
LAD2	VCC	No Gate	Note 2
LAD3	VCC	No Gate	Note 2
LED0	VTR	Low	
LED1	VTR	Low	
LED2	VTR	Low	
LED3	VTR	Low	
LFRAME#	VCC	High	
LPCPD#	VCC	High	
LRESET#	VTR	High	
nEC_SCI	VTR	High	Note 1
nEM_INT	VTR	High	
nSMI	VTR	High	
PCI_CLK	VCC	Low	
PECI_DAT	VTR	Low	
PS2_CLK0A	VTR	High	Note 6

Signal	Emulated Power Rail	Gated State	Notes
PS2_CLK0B	VTR	High	Note 6
PS2_CLK1A	VTR	High	Note 6
PS2_CLK1B	VTR	High	Note 6
PS2_CLK2	VTR	High	
PS2_DAT0A	VTR	High	Note 6
PS2_DAT0B	VTR	High	Note 6
PS2_DAT1A	VTR	High	Note 6
PS2_DAT1B	VTR	High	Note 6
PS2_DAT2	VTR	High	
PVT_CLK	VTR	Low	
PVT_CS#	VTR	High	
PVT_IO0	VTR	Low	
PVT_IO1	VTR	Low	
PVT_IO2	VTR	Low	
PVT_IO3	VTR	Low	
PWM0	VTR	Low	
PWM1	VTR	Low	
PWM2	VTR	Low	
PWM3	VTR	Low	
PWM4	VTR	Low	
PWM5	VTR	Low	
PWM6	VTR	Low	
PWM7	VTR	Low	
PWM8	VTR	Low	
PWM9	VTR	Low	
PWM10	VTR	Low	
PWROK	VTR	High	
RC_ID0	VTR	Low	
RC_ID1	VTR	Low	
RC_ID2	VTR	Low	
RESETI#	VTR	High	
RESETO#	VTR	High	
SB-TSI_CLK	VTR	High	
SB-TSI_DAT	VTR	High	
SER_IRQ	VTR	Low	Note 2
SHD_CLK	VTR	Low	
SHD_CS#	VTR	High	
SHD_IO0	VTR	Low	
SHD_IO1	VTR	Low	
SHD_IO2	VTR	Low	
SHD_IO3	VTR	Low	
SPI0_CLK	VTR	Low	
SPI0_CS#	VTR	High	

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Signal	Emulated Power Rail	Gated State	Notes
SPI0_MISO	VTR	Low	
SPI0_MOSI	VTR	Low	
SPI1_CLK	VTR	Low	
SPI1_CS#	VTR	High	
SPI1_MOSI	VTR	Low	
SPI1_MSIO	VTR	Low	
TFCLK	VTR	Low	
TFDATA	VTR	Low	
TIN0	VTR	Low	
TIN1	VTR	Low	
TIN2	VTR	Low	
TIN3	VTR	Low	
TOUT0	VTR	Low	
TOUT1	VTR	Low	
TOUT2	VTR	Low	
TOUT3	VTR	Low	
TRACECLK	VTR	Low	
TRACEDAT0	VTR	Low	
TRACEDAT1	VTR	Low	
TRACEDAT2	VTR	Low	
TRACEDAT3	VTR	Low	
UART_CLK	VTR	Low	
UART0_CTS#	VTR	Low	Note 4
UART0_DCD#	VTR	High	Note 4
UART0_DSR#	VTR	High	Note 4
UART0_DTR#	VTR	High	Note 4
UART0_RI#	VTR	High	Note 4
UART0_RTS#	VTR	Low	Note 4
UART0_RX	VTR	Low	Note 4
UART0_TX	VTR	Low	Note 4
UART1_CTS#	VTR	Low	Note 4
UART1_RTS#	VTR	Low	Note 4
UART1_RX	VTR	Low	Note 4
UART1_TX	VTR	Low	Note 4
VBAT			
VCC_PWRGD	VTR	High	
VCI_IN0#	VTR	No Gate	Note 13
VCI_IN1#	VTR	No Gate	Note 13
VCI_IN2#	VTR	No Gate	Note 13
VCI_IN3#	VTR	No Gate	Note 13
VCI_IN4#	VTR	No Gate	Note 13
VCI_OUT	VTR	Low	
VFLT_PLL			

Signal	Emulated Power Rail	Gated State	Notes
VR_CAP			Note 15
VREF_ADC			
VREF_VTT			
VSS_ADC			
VSS_ANALOG			
VSS_REG			
VSS1			
VSS2			
VSS3			
VTR_ANALOG			
VTR_PLL			
VTR_REG			
VTR1			
VTR2			
VTR3			
XTAL1			
XTAL2			

2.7 Signal Description by Interface

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
16-Bit Counter/Timer Interface							
M12	M12	M12	K12	H11	TIN0	16-Bit Counter/Timer Input 1	
N13	N13	N13	L11	P12	TIN1	16-Bit Counter/Timer Input 2	
K11	K11	K11	F13	P15	TIN2	16-Bit Counter/Timer Input 3	
J9	J9	J9	J13	N14	TIN3	16-Bit Counter/Timer Input 4	
N7	N7	N7	N10	R10	TOUT0	16-Bit Counter/Timer Output 1	
N8	N8	N8	J8	P9	TOUT1	16-Bit Counter/Timer Output 2	
M7	M7	M7	H7	R8	TOUT2	16-Bit Counter/Timer Output 3	
N6	N6	N6	L7	P8	TOUT3	16-Bit Counter/Timer Output 4	
Analog Data Acquisition Interface							
H3	H3	H3	G3	J2	ADC00	ADC Channel 0	
J3	J3	J3	H4	K4	ADC01	ADC Channel 1	

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
J2	J2	J2	H3	L4	ADC02	ADC Channel 2	
J1	J1	J1	K2	K2	ADC03	ADC Channel 3	
H2	H2	H2	J3	L1	ADC04	ADC Channel 4	
K3	K3	K3	L2	M2	ADC05	ADC Channel 5	
L1	L1	L1	M2	P1	ADC06	ADC Channel 6	
K2	K2	K2	L3	N3	ADC07	ADC Channel 7	
			H2	J4	ADC08	ADC Channel 8	
			J2	H1	ADC09	ADC Channel 9	
			K1	J1	ADC10	ADC Channel 10	
			J4	K1	ADC11	ADC Channel 11	
			J5	L2	ADC12	ADC Channel 12	
			K3	N1	ADC13	ADC Channel 13	
			K4	N2	ADC14	ADC Channel 14	
			K5	P2	ADC15	ADC Channel 15	
G2	G2	G2	H5	J5	VREF_ADC	ADC Voltage Reference	
BC-Link Interface							
E12	E12	E12	C13	G12	BCM0_CLK	BC-Link Master clock	
E11	E11	E11	D12	F14	BCM0_DAT	BC-Link Master data I/O	
F13	F13	F13	A12	E15	BCM1_CLK	BC-Link Master clock	
E9	E9	E9	E10	F10	BCM1_DAT	BC-Link Master data I/O	
Capture/Compare Timer Interface							
A9	A9	A9	B7	A10	CTOUT0	Compare Timer 0 Toggle Output	
		E13	G11	G15	CTOUT1	Compare Timer 1 Toggle Output	
N3	N3	N3	N8	M7	ICT3	Input Capture Timer Input 3	
L9	L9	L9	H9	K10	ICT4	Input Capture Timer Input 4	
L11	L11	L11	K13	J11	ICT5	Input Capture Timer Input 5	
eSPI Host Interface							
M4	M4	M4	N5	P6	ESPI_ALERT#		
M2	M2	M2	N2	R2	ESPI_CLK		
M1	M1	M1	N1	P3	ESPI_CS#		
L3	L3	L3	M4	R3	ESPI_IO0		
N2	N2	N2	N3	R4	ESPI_IO1		
M3	M3	M3	N4	P5	ESPI_IO2		
L4	L4	L4	M6	R5	ESPI_IO3		

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
N1	N1	N1	M1	M6	ESPI_RESET#		
Fan PWM and Tachometer Interface							
F3	F3	F3	G2	H5	FAN_TACH0	Fan Tachometer Input 0/Input Capture Timer Input 0	
B1	B1	B1	F3	F2	FAN_TACH1	Fan Tachometer Input 1/Input Capture Timer Input 1	
L8	L8	L8	K8	L8	FAN_TACH2	Fan Tachometer Input 2/Input Capture Timer Input 2	
M13	M13	M13	K11	P14	GPWM0	PWM Output from RPM-based Fan Speed Control Algorithm, PWM 0	
L12	L12	L12	K10	N15	GPWM1	PWM Output from RPM-based Fan Speed Control Algorithm, PWM 1	
F3	F3	F3	G2	H5	GTACH0	Tach Input to RPM-based Fan Speed Control Algorithm, Tach 0	
B1	B1	B1	F3	F2	GTACH1	Tach Input to RPM-based Fan Speed Control Algorithm, Tach 1	
M13	M13	M13	K11	P14	PWM0	Pulse Width Modulator Output 0	
L12	L12	L12	K10	N15	PWM1	Pulse Width Modulator Output 1	
N4	N4	N4	M8	M8	PWM2	Pulse Width Modulator Output 2	
N5	N5	N5	N9	M9	PWM3	Pulse Width Modulator Output 3	
			N11	R12	PWM4	Pulse Width Modulator Output 4	
M8	M8	M8	N13	L9	PWM5	Pulse Width Modulator Output 5	
M9	M9	M9	M10	P11	PWM6	Pulse Width Modulator Output 6	
J7	J7	J7	M12	J9	PWM7	Pulse Width Modulator Output 7	
		E13	G11	G15	PWM8	Pulse Width Modulator Output 8	
			C11	C14	PWM9	Pulse Width Modulator Output 9	
E13	E13		D11	G14	PWM10	Pulse Width Modulator Output 10	
General Purpose Input/Outputs							
B3	B3	B3	C2	C3	GPIO000	General Purpose Input/Output Port	
			N11	R12	GPIO001	General Purpose Input/Output Port	
M8	M8	M8	N13	L9	GPIO002	General Purpose Input/Output Port	
F5	F5	F5	C6	B7	GPIO003	General Purpose Input/Output Port	
C6	C6	C6	B5	D7	GPIO004	General Purpose Input/Output Port	
			A5	E7	GPIO005	General Purpose Input/Output Port	
			B6	A7	GPIO006	General Purpose Input/Output Port	
B12	B12	B12	B10	A14	GPIO007	General Purpose Input/Output Port	
C10	C10	C10	C10	D11	GPIO010	General Purpose Input/Output Port	
J6	J6	J6	L5	K6	GPIO011	General Purpose Input/Output Port	
N6	N6	N6	L7	P8	GPIO012	General Purpose Input/Output Port	
M7	M7	M7	H7	R8	GPIO013	General Purpose Input/Output Port	

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
M9	M9	M9	M10	P11	GPIO014	General Purpose Input/Output Port	
J7	J7	J7	M12	J9	GPIO015	General Purpose Input/Output Port	
N3	N3	N3	N8	M7	GPIO016	General Purpose Input/Output Port	
J8	J8	J8	J9	K11	GPIO017	General Purpose Input/Output Port	
L7	L7	L7	L9	R9	GPIO020	General Purpose Input/Output Port	
N9	N9	N9	M9	P10	GPIO021	General Purpose Input/Output Port	
E2	E2	E2	D2	D2	GPIO022	General Purpose Input/Output Port	
C3	C3	C3	F4	F5	GPIO023	General Purpose Input/Output Port	
C2	C2	C2	E2	G4	GPIO024	General Purpose Input/Output Port	
M12	M12	M12	K12	H11	GPIO025	General Purpose Input/Output Port	
N13	N13	N13	L11	P12	GPIO026	General Purpose Input/Output Port	
K11	K11	K11	F13	P15	GPIO027	General Purpose Input/Output Port	
J9	J9	J9	J13	N14	GPIO030	General Purpose Input/Output Port	
M11	M11	M11	M13	M11	GPIO031	General Purpose Input/Output Port	
L10	L10	L10	K9	M10	GPIO032	General Purpose Input/Output Port	
B2	B2	B2	C1	B1	GPIO033	General Purpose Input/Output Port	
H12	H12	H12	E13	H15	GPIO034	General Purpose Input/Output Port	
		E13	G11	G15	GPIO035	General Purpose Input/Output Port	
H13	H13	H13	F12	J12	GPIO036	General Purpose Input/Output Port	
M10	M10	M10	M11	L11	GPIO040	General Purpose Input/Output Port	
			F2	H4	GPIO041	General Purpose Input/Output Port	
J12	J12	J12	H10	J15	GPIO042	General Purpose Input/Output Port	
J13	J13	J13	H11	J14	GPIO043	General Purpose Input/Output Port	
H11	H11	H11	G9	K12	GPIO044	General Purpose Input/Output Port	
E8	E8	E8	E8	A11	GPIO045	General Purpose Input/Output Port	
E9	E9	E9	E10	F10	GPIO046	General Purpose Input/Output Port	
F13	F13	F13	A12	E15	GPIO047	General Purpose Input/Output Port	
F3	F3	F3	G2	H5	GPIO050	General Purpose Input/Output Port	
B1	B1	B1	F3	F2	GPIO051	General Purpose Input/Output Port	
L8	L8	L8	K8	L8	GPIO052	General Purpose Input/Output Port	
M13	M13	M13	K11	P14	GPIO053	General Purpose Input/Output Port	
L12	L12	L12	K10	N15	GPIO054	General Purpose Input/Output Port	
N4	N4	N4	M8	M8	GPIO055	General Purpose Input/Output Port	
N5	N5	N5	N9	M9	GPIO056	General Purpose Input/Output Port	
D1	D1	D1	F1	G2	GPIO057	General Purpose Input/Output Port	

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
D2	D2	D2	G5	H7	GPIO060	General Purpose Input/Output Port	
N1	N1	N1	M1	M6	GPIO061	General Purpose Input/Output Port	
A2	A2	A2	D3	C2	GPIO062	General Purpose Input/Output Port	Note 7
M4	M4	M4	N5	P6	GPIO063	General Purpose Input/Output Port	
J5	J5	J5	M3	M5	GPIO064	General Purpose Input/Output Port	
M2	M2	M2	N2	R2	GPIO065	General Purpose Input/Output Port	
M1	M1	M1	N1	P3	GPIO066	General Purpose Input/Output Port	
L2	L2	L2	M5	K5	GPIO067	General Purpose Input/Output Port	
L3	L3	L3	M4	R3	GPIO070	General Purpose Input/Output Port	
N2	N2	N2	N3	R4	GPIO071	General Purpose Input/Output Port	
M3	M3	M3	N4	P5	GPIO072	General Purpose Input/Output Port	
L4	L4	L4	M6	R5	GPIO073	General Purpose Input/Output Port	
H7	H7	H7	L4	L6	GPIO100	General Purpose Input/Output Port	
A4	A4	A4	C5	F6	GPIO101	General Purpose Input/Output Port	
B5	B5	B5	B3	A5	GPIO102	General Purpose Input/Output Port	
F11	F11	F11	A13	F15	GPIO104	General Purpose Input/Output Port	
F9	F9	F9	F9	F11	GPIO105	General Purpose Input/Output Port	
E3	E3	E3	H6	G7	GPIO106	General Purpose Input/Output Port	
L13	L13	L13	H13	M14	GPIO107	General Purpose Input/Output Port	
			G13	L15	GPIO110	General Purpose Input/Output Port	
			G12	L12	GPIO111	General Purpose Input/Output Port	
K13	K13	K13	J12	K15	GPIO112	General Purpose Input/Output Port	
J11	J11	J11	J11	L14	GPIO113	General Purpose Input/Output Port	
H9	H9	H9	J10	K14	GPIO114	General Purpose Input/Output Port	
N12	N12	N12	L13	P13	GPIO115	General Purpose Input/Output Port	
K12	K12	K12	H12	M15	GPIO120	General Purpose Input/Output Port	
F12	F12	F12	D13	F12	GPIO121	General Purpose Input/Output Port	
E11	E11	E11	D12	F14	GPIO122	General Purpose Input/Output Port	
E12	E12	E12	C13	G12	GPIO123	General Purpose Input/Output Port	
C11	C11	C11	B13	E12	GPIO124	General Purpose Input/Output Port	
D11	D11	D11	B12	D14	GPIO125	General Purpose Input/Output Port	
D12	D12	D12	C12	E14	GPIO126	General Purpose Input/Output Port	
D13	D13	D13	A11	D15	GPIO127	General Purpose Input/Output Port	
N8	N8	N8	J8	P9	GPIO130	General Purpose Input/Output Port	
N7	N7	N7	N10	R10	GPIO131	General Purpose Input/Output Port	

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
N11	N11	N11	L10	R14	GPIO132	General Purpose Input/Output Port	
			C11	C14	GPIO133	General Purpose Input/Output Port	
E13	E13		D11	G14	GPIO134	General Purpose Input/Output Port	
G9	G9		E12	G9	GPIO135	General Purpose Input/Output Port	
L11	L11	L11	K13	J11	GPIO140	General Purpose Input/Output Port	
B7	B7	B7	A7	B8	GPIO141	General Purpose Input/Output Port	
F7	F7	F7	F7	D8	GPIO142	General Purpose Input/Output Port	
A7	A7	A7	A6	A8	GPIO143	General Purpose Input/Output Port	
E7	E7	E7	D4	E8	GPIO144	General Purpose Input/Output Port	
A8	A8	A8	D7	G8	GPIO145	General Purpose Input/Output Port	
G8	G8	G8	F8	B9	GPIO146	General Purpose Input/Output Port	
C7	C7	C7	C7	D9	GPIO147	General Purpose Input/Output Port	
F8	F8	F8	E7	A9	GPIO150	General Purpose Input/Output Port	
L9	L9	L9	H9	K10	GPIO151	General Purpose Input/Output Port	
N10	N10	N10	N12	R13	GPIO152	General Purpose Input/Output Port	
		C12	E9	B14	GPIO153	General Purpose Input/Output Port	
A12	A12	A12	A9	B13	GPIO154	General Purpose Input/Output Port	
C9	C9	C9	C9	E10	GPIO155	General Purpose Input/Output Port	
C12	C12	A13	D9	B15	GPIO156	General Purpose Input/Output Port	
B13	B13	B13	B11	C15	GPIO157	General Purpose Input/Output Port	
C4	C4	C4	C3	E5	GPIO161	General Purpose Input/Output Port	
A6	A6	A6	A4	A6	GPIO162	General Purpose Input/Output Port	
E6	E6	E6	F6	B6	GPIO163	General Purpose Input/Output Port	
A9	A9	A9	B7	A10	GPIO165	General Purpose Input/Output Port	
			G1	E2	GPIO166	General Purpose Input/Output Port	
G13	G13	G12	F11	H12	GPIO170	General Purpose Input/Output Port	
G12	G12	G9	E11	H9	GPIO171	General Purpose Input/Output Port	
B6	B6	B6	F5	E6	GPIO172	General Purpose Input/Output Port	
			A2	B5	GPIO173	General Purpose Input/Output Port	
			E4	B3	GPIO174	General Purpose Input/Output Port	
C13	C13	C13	D10	E11	GPIO175	General Purpose Input/Output Port	
H3	H3	H3	G3	J2	GPIO200	General Purpose Input/Output Port	
J3	J3	J3	H4	K4	GPIO201	General Purpose Input/Output Port	
J2	J2	J2	H3	L4	GPIO202	General Purpose Input/Output Port	
J1	J1	J1	K2	K2	GPIO203	General Purpose Input/Output Port	

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
H2	H2	H2	J3	L1	GPIO204	General Purpose Input/Output Port	
K3	K3	K3	L2	M2	GPIO205	General Purpose Input/Output Port	
L1	L1	L1	M2	P1	GPIO206	General Purpose Input/Output Port	
K2	K2	K2	L3	N3	GPIO207	General Purpose Input/Output Port	
			H2	J4	GPIO210	General Purpose Input/Output Port	
			J2	H1	GPIO211	General Purpose Input/Output Port	
			K1	J1	GPIO212	General Purpose Input/Output Port	
			J4	K1	GPIO213	General Purpose Input/Output Port	
			J5	L2	GPIO214	General Purpose Input/Output Port	
			K3	N1	GPIO215	General Purpose Input/Output Port	
			K4	N2	GPIO216	General Purpose Input/Output Port	
			K5	P2	GPIO217	General Purpose Input/Output Port	
C1	C1	C1	G7	E1	GPIO221	General Purpose Input/Output Port	
L5	L5	L5	L6	L7	GPIO222	General Purpose Input/Output Port	
M6	M6	M6	M7	R7	GPIO223	General Purpose Input/Output Port	
M5	M5	M5	N6	R6	GPIO224	General Purpose Input/Output Port	
A13	A13		A10	C13	GPIO225	General Purpose Input/Output Port	
F2	F2	F2	E3	F1	GPIO226	General Purpose Input/Output Port	
L6	L6	L6	N7	P7	GPIO227	General Purpose Input/Output Port	
			L8	R11	GPIO230	General Purpose Input/Output Port	
			K7	J8	GPIO231	General Purpose Input/Output Port	
			G8	L10	GPIO233	General Purpose Input/Output Port	
			B1	E4	GPIO234	General Purpose Input/Output Port	
		G13	G10	H14	GPIO240	General Purpose Input/Output Port	
B8	B8	B8	D6	B10	GPIO241	General Purpose Input/Output Port	
A10	A10	A10	D5	A12	GPIO242	General Purpose Input/Output Port	
C8	C8	C8	D8	E9	GPIO243	General Purpose Input/Output Port	
A11	A11	A11	B8	A13	GPIO244	General Purpose Input/Output Port	
B11	B11	B11	C8	B12	GPIO245	General Purpose Input/Output Port	
B10	B10	B10	B9	D10	GPIO246	General Purpose Input/Output Port	
B9	B9	B9	A8	B11	GPIO254	General Purpose Input/Output Port	
General Purpose Pass-Through Ports							
E2	E2	E2	D2	D2	GPTP-IN0	General Purpose Pass Through Port Input 0	
C3	C3	C3	F4	F5	GPTP-IN1	General Purpose Pass Through Port Input 1	
C2	C2	C2	E2	G4	GPTP-IN2	General Purpose Pass Through Port Input 2	

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MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
C1	C1	C1	G7	E1	GPTP-IN3	General Purpose Pass Through Port Input 3	
M5	M5	M5	N6	R6	GPTP-IN4	General Purpose Pass Through Port Input 4	
J8	J8	J8	J9	K11	GPTP-IN5	General Purpose Pass Through Port Input 5	
M9	M9	M9	M10	P11	GPTP-IN6	General Purpose Pass Through Port Input 6	
N3	N3	N3	N8	M7	GPTP-IN7	General Purpose Pass Through Port Input 7	
L10	L10	L10	K9	M10	GPTP-OUT0	General Purpose Pass Through Port Output 0	
M11	M11	M11	M13	M11	GPTP-OUT1	General Purpose Pass Through Port Output 1	
M10	M10	M10	M11	L11	GPTP-OUT2	General Purpose Pass Through Port Output 2	
N10	N10	N10	N12	R13	GPTP-OUT3	General Purpose Pass Through Port Output 3	
			A5	E7	GPTP-OUT4	General Purpose Pass Through Port Output 4	
D11	D11	D11	B12	D14	GPTP-OUT5	General Purpose Pass Through Port Output 5	
C11	C11	C11	B13	E12	GPTP-OUT6	General Purpose Pass Through Port Output 6	
			B6	A7	GPTP-OUT7	General Purpose Pass Through Port Output 7	
I2C/SMBus Interface							
C6	C6	C6	B5	D7	I2C00_SCL	SMB-I2C Controller Port 0 Clock	Note 14
F5	F5	F5	C6	B7	I2C00_SDA	SMB-I2C Controller Port 0 Data	Note 14
			B6	A7	I2C01_SCL	SMB-I2C Controller Port 1 Clock	Note 14
			A5	E7	I2C01_SDA	SMB-I2C Controller Port 1 Data	Note 14
C9	C9	C9	C9	E10	I2C02_SCL	SMB-I2C Controller Port 2 Clock	Note 14
A12	A12	A12	A9	B13	I2C02_SDA	SMB-I2C Controller Port 2 Data	Note 14
C10	C10	C10	C10	D11	I2C03_SCL	SMB-I2C Controller Port 3 Clock	Note 14
B12	B12	B12	B10	A14	I2C03_SDA	SMB-I2C Controller Port 3 Data	Note 14
E7	E7	E7	D4	E8	I2C04_SCL	SMB-I2C Controller Port 4 Clock	Note 14
A7	A7	A7	A6	A8	I2C04_SDA	SMB-I2C Controller Port 4 Data	Note 14
F7	F7	F7	F7	D8	I2C05_SCL	SMB-I2C Controller Port 5 Clock	Note 14
B7	B7	B7	A7	B8	I2C05_SDA	SMB-I2C Controller Port 5 Data	Note 14
L11	L11	L11	K13	J11	I2C06_SCL	SMB-I2C Controller Port 6 Clock	Note 14
N11	N11	N11	L10	R14	I2C06_SDA	SMB-I2C Controller Port 6 Data	Note 14
M7	M7	M7	H7	R8	I2C07_SCL	SMB-I2C Controller Port 7 Clock	Note 14
N6	N6	N6	L7	P8	I2C07_SDA	SMB-I2C Controller Port 7 Data	Note 14
F8	F8	F8	E7	A9	I2C08_SCL	SMB-I2C Controller Port 8 Clock	Note 14
C7	C7	C7	C7	D9	I2C08_SDA	SMB-I2C Controller Port 8 Data	Note 14
G8	G8	G8	F8	B9	I2C09_SCL	SMB-I2C Controller Port 9 Clock	Note 14
A8	A8	A8	D7	G8	I2C09_SDA	SMB-I2C Controller Port 9 Data	Note 14
N7	N7	N7	N10	R10	I2C10_SCL	SMB-I2C Controller Port 10 Clock	Note 14

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N8	N8	N8	J8	P9	I2C10_SDA	SMB-I2C Controller Port 10 Data	Note 14
J13	J13	J13	H11	J14	SB-TSI_CLK	SMB-I2C Controller AMD-TSI Port Clock	
J12	J12	J12	H10	J15	SB-TSI_DAT	SMB-I2C Controller AMD-TSI Port Data	
JTAG and Debug Interface							
C7	C7	C7	C7	D9	JTAG_CLK	JTAG Test Clock. Also ARM SWDCLK	
G11	G11	G11	F10	G11	JTAG_RST#	JTAG Test Reset (active low)	Note 5
A8	A8	A8	D7	G8	JTAG_TDI	JTAG Test Data In	
G8	G8	G8	F8	B9	JTAG_TDO	JTAG Test Data Out. Also ARM SWO	
F8	F8	F8	E7	A9	JTAG_TMS	JTAG Test Mode Select. Also ARM SWDIO	
G13	G13	G12	F11	H12	TFCLK	Trace FIFO debug port - clock	
G12	G12	G9	E11	H9	TFDATA	Trace FIFO debug port - data	
A9	A9	A9	B7	A10	TRACECLK	ARM Embedded Trace Macro Clock	
B7	B7	B7	A7	B8	TRACEDAT0	ARM Embedded Trace Macro Data 0	
F7	F7	F7	F7	D8	TRACEDAT1	ARM Embedded Trace Macro Data 1	
A7	A7	A7	A6	A8	TRACEDAT2	ARM Embedded Trace Macro Data 2	
E7	E7	E7	D4	E8	TRACEDAT3	ARM Embedded Trace Macro Data 3	
Keyboard Scan Interface							
J8	J8	J8	J9	K11	KSI0	Keyboard Scan Matrix Input 0	
L7	L7	L7	L9	R9	KSI1	Keyboard Scan Matrix Input 1	
N9	N9	N9	M9	P10	KSI2	Keyboard Scan Matrix Input 2	
N13	N13	N13	L11	P12	KSI3	Keyboard Scan Matrix Input 3	
K11	K11	K11	F13	P15	KSI4	Keyboard Scan Matrix Input 4	
J9	J9	J9	J13	N14	KSI5	Keyboard Scan Matrix Input 5	
M11	M11	M11	M13	M11	KSI6	Keyboard Scan Matrix Input 6	
L10	L10	L10	K9	M10	KSI7	Keyboard Scan Matrix Input 7	
M10	M10	M10	M11	L11	KSO00	Keyboard Scan Matrix Output 0	
E8	E8	E8	E8	A11	KSO01	Keyboard Scan Matrix Output 1	
E9	E9	E9	E10	F10	KSO02	Keyboard Scan Matrix Output 2	
F13	F13	F13	A12	E15	KSO03	Keyboard Scan Matrix Output 3	
L13	L13	L13	H13	M14	KSO04	Keyboard Scan Matrix Output 4	
K13	K13	K13	J12	K15	KSO05	Keyboard Scan Matrix Output 5	
J11	J11	J11	J11	L14	KSO06	Keyboard Scan Matrix Output 6	
K12	K12	K12	H12	M15	KSO07	Keyboard Scan Matrix Output 7	
F12	F12	F12	D13	F12	KSO08	Keyboard Scan Matrix Output 8	

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E11	E11	E11	D12	F14	KSO09	Keyboard Scan Matrix Output 9	
E12	E12	E12	C13	G12	KSO10	Keyboard Scan Matrix Output 10	
C11	C11	C11	B13	E12	KSO11	Keyboard Scan Matrix Output 11	
D11	D11	D11	B12	D14	KSO12	Keyboard Scan Matrix Output 12	
D12	D12	D12	C12	E14	KSO13	Keyboard Scan Matrix Output 13	
N11	N11	N11	L10	R14	KSO14	Keyboard Scan Matrix Output 14	
L9	L9	L9	H9	K10	KSO15	Keyboard Scan Matrix Output 15	
N10	N10	N10	N12	R13	KSO16	Keyboard Scan Matrix Output 16	
C13	C13	C13	D10	E11	KSO17	Keyboard Scan Matrix Output 17	
LPC Host Interface							
D13	D13	D13	A11	D15	A20M	Keyboard GATEA20 Output	
L2	L2	L2	M5	K5	CLKRUN#	PCI Clock Control	
D2	D2	D2	G5	H7	KBRST	Keyboard CPU Reset	
L3	L3	L3	M4	R3	LAD0	LPC Multiplexed command, address and data bus Bit 0.	
N2	N2	N2	N3	R4	LAD1	LPC Multiplexed command, address and data bus Bit 1.	
M3	M3	M3	N4	P5	LAD2	LPC Multiplexed command, address and data bus Bit 2.	
L4	L4	L4	M6	R5	LAD3	LPC Multiplexed command, address and data bus Bit 3.	
M1	M1	M1	N1	P3	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	
N1, N9	N1, N9	N1, N9	M1, M9	M6, P10	LPCPD#	LPC Bus Powerdown Signal.	
J5, L8	J5, L8	J5, L8	K8, M3	L8, M5	LRESET#	LPC Reset. Same as the system PCI reset, PCIRST#	
H7, H9	H7, H9	H7, H9	J10, L4	K14, L6	nEC_SCI	Power Management Event	Note 1
M12	M12	M12	K12	H11	nEM_INT	EM Interface Interrupt Output	
L13, J6	L13, J6	L13, J6	H13, L5	K6, M14	nSMI	SMI Output	
M2	M2	M2	N2	R2	PCI_CLK	LPC Clock	
L5, M4	L5, M4	L5, M4	L6, N5	L7, P6	SER_IRQ	Serial IRQ	
Master Clock Interface							
A9	A9	A9	B7	A10	32KHZ_IN	32.768 KHz Digital Input	
C1	C1	C1	G7	E1	32KHZ_OUT	32.768 KHz Digital Output	
D2	D2	D2	G5	H7	48MHZ_OUT	Main System Clock Output	
A3	A3	A3	A3	A4	XTAL1	32.768 KHz Crystal Input	

MEC1704-144 WFBGA	MEC1705-144 WFBGA	MEC1701/MEC1703-144 WFBGA	MEC1701/MEC1703-169 WFBGA	MEC1701/MEC1703-169 XFBGA	Interface		Notes
A1	A1	A1	A1	A2	XTAL2	32.768 KHz Crystal Output (single-ended clock input)	
Miscellaneous Functions							
C12	C12	A13	D9	B15	LED0	LED Output 0	
B13	B13	B13	B11	C15	LED1	LED Output 1	
		C12	E9	B14	LED2	LED Output 2	
F2	F2	F2	E3	F1	LED3	LED Output 3	
E3	E3	E3	H6	G7	PWROK	VCC, Main Power Rail, Powered	
B2	B2	B2	C1	B1	RC_ID0	RC Identification Detection 0	
H12	H12	H12	E13	H15	RC_ID1	RC Identification Detection 1	
H13	H13	H13	F12	J12	RC_ID2	RC Identification Detection 2	
D3	D3	D3	G6	G5	RESETI#	System Reset Input	
A2	A2	A2	D3	C2	(RESETO#)	System Reset Output	
N4	N4	N4	M8	M8	(RSMRST#)	Core logic RSMRST# input; re-balled GPIO	
D1	D1	D1	F1	G2	VCC_PWRGD	System Main Power Indication	
PECI Interface							
J12	J12	J12	H10	J15	PECI_DAT	PECI Bus	
H11	H11	H11	G9	K12	VREF_VTT	Processor Interface Voltage Reference	
Power							
E5	E5	E5	E6	D5	VBAT	VBAT supply	
F1	F1	F1	E1	D1	VFLT_PLL	Filtered power input for PLL	
H1	H1	H1	J1	G1	VR_CAP	Internal Voltage Regulator Output (Capacitor Required)	Note 15
K1	K1	K1	L1	M1	VSS_ADC	Analog ADC VTR associated ground	
B4	B4	B4	C4	A3	VSS_ANALOG	VTR associated ground for Internal Analog Logic	
F6	F6	F6	E5	B2	VSS1	VTR I/O Ground pin region 1	
G3	G3	G3	J7	H8	VSS2	VTR I/O Ground pin region 2	
H5	H5	H5	K6	J7	VSS3	VTR I/O Ground pin region 3	
G6	G6	G6	H8	L5	VTR_ANALOG	VTR Power Supply for Internal Analog Logic	
E1	E1	E1	D1	C1	VTR_PLL	VTR associated power used for PLL	
G1	G1	G1	H1	H2	VTR_REG	VTR Internal Voltage Regulator Power Supply	
G5	G5	G5	G4	F4	VTR1	VTR I/O Power, pin region 1	
H8	H8	H8	L12	N13	VTR2	VTR I/O Power, pin region 2	
H6	H6	H6	J6	P4	VTR3	VTR I/O Power, pin region 3	
PS/2 Interface							
H9	H9	H9	J10	K14	PS2_CLK0A	PS/2 Controller 0, Port A, Clock output	Note 6

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B12	B12	B12	B10	A14	PS2_CLK0B	PS/2 Controller 0, Port B, Clock output	Note 6
K13	K13	K13	J12	K15	PS2_CLK1A	PS/2 Controller 1, Port A, Clock output	Note 6
A12	A12	A12	A9	B13	PS2_CLK1B	PS/2 Controller 1, Port B, Clock output	Note 6
			G13	L15	PS2_CLK2	PS/2 Controller 2, Clock output	
N12	N12	N12	L13	P13	PS2_DAT0A	PS/2 Controller 0, Port A, Data	Note 6
C10	C10	C10	C10	D11	PS2_DAT0B	PS/2 Controller 0, Port B, Data	Note 6
J11	J11	J11	J11	L14	PS2_DAT1A	PS/2 Controller 1, Port A, Data	Note 6
C9	C9	C9	C9	E10	PS2_DAT1B	PS/2 Controller 1, Port B, Data	Note 6
			G12	L12	PS2_DAT2	PS/2 Controller 2, Data	
Serial Ports							
M12	M12	M12	K12	H11	UART_CLK	External Baud Clock for UARTs	
D13	D13	D13	A11	D15	UART0_CTS#	UART 0, Clear to Send Input	Note 4
B7	B7	B7	A7	B8	UART0_DCD#	UART 0, Data Carrier Detect Input	Note 4
F7	F7	F7	F7	D8	UART0_DSR#	UART 0, Data Set Ready Input	Note 4
A7	A7	A7	A6	A8	UART0_DTR#	UART 0, Data Terminal Ready Output	Note 4
E7	E7	E7	D4	E8	UART0_RI#	UART 0, Ring Indicator	Note 4
A13	A13		A10	C13	UART0_RTS#	UART 0, Request to Send Output	Note 4
F9	F9	F9	F9	F11	UART0_RX	UART 0, Receive Data	Note 4
F11	F11	F11	A13	F15	UART0_TX	UART 0, Transmit Data	Note 4
G9	G9		E12	G9	UART1_CTS#	UART 1, Clear to Send Input	Note 4
E13	E13		D11	G14	UART1_RTS#	UART 1, Request to Send Output	Note 4
G12	G12	G9	E11	H9	UART1_RX	UART 1, Receive Data	Note 4
G13	G13	G12	F11	H12	UART1_TX	UART 1, Transmit Data	Note 4
SPI Controllers							
D11	D11	D11	B12	D14	PVT_CLK	Quad SPI Controller Clock, Private SPI port	
C11	C11	C11	B13	E12	PVT_CS#	Quad SPI Controller Chip Select, Private SPI port	
F12	F12	F12	D13	F12	PVT_IO0	Quad SPI Controller Data 0, Private SPI port	
E11	E11	E11	D12	F14	PVT_IO1	Quad SPI Controller Data 1, Private SPI port	
E12	E12	E12	C13	G12	PVT_IO2	Quad SPI Controller Data 2, Private SPI port	
D12	D12	D12	C12	E14	PVT_IO3	Quad SPI Controller Data 3, Private SPI port	
N5	N5	N5	N9	M9	SHD_CLK	Quad SPI Controller Clock, Shared SPI port	
N4	N4	N4	M8	M8	SHD_CS#	Quad SPI Controller Chip Select, Shared SPI port	
M6	M6	M6	M7	R7	SHD_IO0	Quad SPI Controller Data 0, Shared SPI port	
M5	M5	M5	N6	R6	SHD_IO1	Quad SPI Controller Data 1, Shared SPI port	

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L6	L6	L6	N7	P7	SHD_IO2	Quad SPI Controller Data 2, Shared SPI port	
N3	N3	N3	N8	M7	SHD_IO3	Quad SPI Controller Data 3, Shared SPI port	
H12	H12	H12	E13	H15	SPI0_CLK	GP-SPI SPI Clock	
F5	F5	F5	C6	B7	SPI0_CS#	GP-SPI Chip Select	
H13	H13	H13	F12	J12	SPI0_MISO	GP-SPI SPI Output	
C6	C6	C6	B5	D7	SPI0_MOSI	GP-SPI SPI Input	
B7	B7	B7	A7	B8	SPI1_CLK	GP-SPI SPI Clock	
E7	E7	E7	D4	E8	SPI1_CS#	GP-SPI Chip Select	
F7	F7	F7	F7	D8	SPI1_MOSI	GP-SPI SPI Output	
A7	A7	A7	A6	A8	SPI1_MISO	GP-SPI SPI Input	
VBAT-Powered Control Interface							
A5	A5	A5	B4	D6	BGPO0	VBAT driven GPO	
A4	A4	A4	C5	F6	BGPO1	VBAT driven GPO	Note 8
B5	B5	B5	B3	A5	BGPO2	VBAT driven GPO	Note 8
B6	B6	B6	F5	E6	BGPO3	VBAT driven GPO	Note 8
			A2	B5	BGPO4	VBAT driven GPO	Note 8
			E4	B3	BGPO5	VBAT driven GPO	Note 8
E6	E6	E6	F6	B6	VCI_IN0#	Input can cause wakeup or interrupt event, active low	Note 13
A6	A6	A6	A4	A6	VCI_IN1#	Input can cause wakeup or interrupt event, active low	Note 13
C4	C4	C4	C3	E5	VCI_IN2#	Input can cause wakeup or interrupt event, active low	Note 13
B3	B3	B3	C2	C3	VCI_IN3#	Input can cause wakeup or interrupt event, active low	Note 13
			B1	E4	VCI_IN4#	Input can cause wakeup or interrupt event, active low	Note 13
C5	C5	C5	B2	B4	VCI_OUT	Output from combinational logic and/or EC	

2.8 UPD Dead Battery Interface Pins

TABLE 2-1: "UPD Dead Battery Support Pins" lists the pins and interfaces used for UPD dead battery interface.

Note: For more details about dead battery changing interface and usage, please refer to MEC170X_ROM_Description.pdf.

TABLE 2-1: UPD DEAD BATTERY SUPPORT PINS

Signal	Interface	Pin Name	Default Pin State
I2C10_SCL	I2C	GPIO131/I2C10_SCL/TOUT0	Tristate Input. Pulled High externally to VTR2 power supply.

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Signal	Interface	Pin Name	Default Pin State
I2C10_SDA	I2C	GPIO130/I2C10_SDA/TOUT1	Tristate Input. Pulled High externally to VTR2 power supply.
UPD_Alert1#	I2C	GPIO001/PWM4	Tristate Input. Pulled High externally to VTR2 power supply.
UPD_Alert2#	I2C	GPIO002/PWM5	Tristate Input. Pulled High externally to VTR2 power supply.
UPD_RST1#	RESET_N for UPD[1]	GPIO231	Tristate Input. Pulled High externally to VTR2 power supply.
UPD_RST2#	RESET_N for UPD[2]	GPIO233	Tristate Input. Pulled High externally to VTR2 power supply.

2.9 Strapping Options

GPIO171 is used for the TAP Controller select strap. If any of the JTAG TAP controllers are used, GPIO171 must only be configured as an output to a VTR powered external function. GPIO171 may only be configured as an input when the JTAG TAP controllers are not needed or when an external driver does not violate the Slave Select Timing.See Section 48.2.1, "TAP Controller Select Strap Option".

TABLE 2-2: STRAPS AND MEANING

Pin	Function	Definition
GPIO233	UPD[2] RESET_N	Pull-down (0) = UPD Port 2 Not Present Pull-up (1) = UPD Port 2 Present **Note:** 10k to 100k ohm pull-up or pull-down required.
GPIO246	UPD_Enable	Pull-down (0) = No UPD devices are connected Pull-up (1) = One or more UPD devices are connected **Note:** 10k to 100k ohm pull-up or pull-down required.
GPIO045/KSO1	Private SPI Selection	1=Use GPIO055 to select between the Shared SPI pins and the eSPI Flash Channel for Boot 0=Use the Private SPI pins for Boot **Note:** This pin requires an external pull-up for normal operation.
GPIO055/SHD_CS#	Shared SPI vs. eSPI Selection	1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot **Note:** See application specific recommendation in Section 2.9.1, "Shared SPI Flash Chip Select Pull-up Resistor Recommendation " after this table.
GPIO171/TFDATA/ UART1_RX	JTAG Boundary Scan	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug

Note: Please refer to MEC170X_ROM_Description.pdf for more details about UPD strap pins and there functioning.

2.9.1 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/PWM2/SHD_CS#/RSMRST# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/PWM2/SHD_CS#/RSMRST# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS# pin on the board if the Shared SPI flash interface is used so that the SPI_CS# is detected high while RSMRST# is low.

The recommended value of the pull-up resistor on the SHD_CS# pin may vary depending on the version of the Intel PCH that is used.

This is based on information in the current Intel PCH device specifications regarding the SPI0_CS0# pin. This information, as well as the information regarding other PCH devices, must be verified with Intel:

Skylake PCH LP: the signal is tri-stated with no pull-up or pull-down

- Use a resistor in the 4.7K-100K range (pulled-up to the 3.3V rail that powers the SPI device)

Skylake PCH H: the signal is tri-stated with a weak pull down (~ 20K)

- Use a resistor in the 4.7K-8K range (pulled-up to the 3.3V rail that powers the SPI device).

These pull-up values must ensure the voltage on the pin is detected as a high (i.e., VTR*0.7).

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2.10 Pin Default State Through Power Transitions

The power state and power state transitions illustrated in the following tables are defined in Section 4.0, "Power, Clocks, and Resets". Pin behavior in this table assumes no specific programming to change the pin state. All GPIO default pins that have the same behavior are described in the table generically as GPIOXXX.

TABLE 2-3: PIN DEFAULT STATE THROUGH POWER TRANSITIONS

Signal	VBAT Applied	VBAT Stable	VTR Applied	RESET_SYS De-asserted	VCC_PWRGD Asserted	VCC_PWRGD De-asserted	RESET_SYS Asserted	VTR Un-powered	VBAT Un-powered	Note
GPIO042	un-powered	un-powered	low	In	In	In	Z	glitch	un-powered	
GPIO043	un-powered	un-powered	low	In	In	In	Z	glitch	un-powered	
GPIO062	un-powered	un-powered	low	Out=0	Out	Out	Out	glitch	un-powered	
GPIOXXX	un-powered	un-powered	In	In	In	In	Z	glitch	un-powered	Note E
SER_IRQ	un-powered	un-powered	glitch	In	Z>I/O (*P*)>Z	In	In	glitch	un-powered	Note A
LRESET#	un-powered	un-powered	glitch	In	In	In	Z	glitch	un-powered	Note A
PCI_CLK	un-powered	un-powered	glitch	In	In	In	Z	glitch	un-powered	
LFRAME#	un-powered	un-powered	glitch	In	In	In	Z	glitch	un-powered	
LAD0	un-powered	un-powered	glitch	In	In>I/O (*P*)>In	In	Z	glitch	un-powered	
LAD1	un-powered	un-powered	glitch	In	In>I/O (*P*)>In	In	Z	glitch	un-powered	
LAD2	un-powered	un-powered	glitch	In	In>I/O (*P*)>In	In	Z	glitch	un-powered	
LAD3	un-powered	un-powered	glitch	In	In>I/O (*P*)>In	In	Z	glitch	un-powered	
CLKRUN#	un-powered	un-powered	glitch	In	Z>I/O (*P*)>Z	In	Z	glitch	un-powered	
BGPOx	Out=0	Out=0	Retain	Retain	Retain	Retain	Retain	Retain	un-powered	Note B
VCI_INx#	In	In	In	In	In	In	In	In	un-powered	
VCI_OUT	Out logic	Out logic	Out logic	Out logic	Out logic	Out logic	Out logic	Out logic	un-powered	Note C
XTAL1	Crystal In	Crystal In	Crystal In	Crystal In	Crystal In	Crystal In	Crystal In	Crystal In	Crystal In	
XTAL2	Crystal Out	Crystal Out	Crystal Out	Crystal Out	Crystal Out	Crystal Out	Crystal Out	Crystal Out	Crystal Out	

Legend	Notes
(P) = I/O state is driven by protocol while power is applied. **Z** = Tristate **In** = Input	Note A: Pin exhibits "VCC" power domain emulation. Note B: Pin is programmable by the EC and retains its value through a VTR power cycle. Note C: Pin is programmable by the EC and affected by other VBAT inputs pins. Note D: Pin exhibits "VTR" power domain emulation. Note E: Does not include GPIO042, GPIO043, and GPIO062

TABLE 2-4: PIN DEFAULT STATE THROUGH POWER TRANSITIONS

Signal	VBAT Applied	VBAT Stable	VTR Applied	nSYS _ RST De-asserted	VCC_ PWRGD Asserted	VCC_ PWRGD De-asserted	nSYS_ RST Asserted	VTR Un-powered	VBAT Un-powered	Note
nSMI	N/A	N/A	N/A	N/A	1> OD(P)> 1	OD(1)	In	glitch	N/A	
KBRST	N/A	N/A	N/A	N/A	1> OD(P)> 1	Z	Z>In	glitch	N/A	Note F
A20M	N/A	N/A	N/A	N/A	1> OD(P)> 1	Z	Z	glitch	N/A	Note F
LPCPD#	N/A	N/A	N/A	N/A	In	Z	Z	glitch	N/A	Note F

Legend	Notes
(P) = I/O state is driven by protocol while power is applied. **Z** = Tristate **In** = Input **OD** = Open Drain Output Undriven (1) or driven (0)	Note F: Pin is programmable by the EC and retains its value through a VTR power cycle

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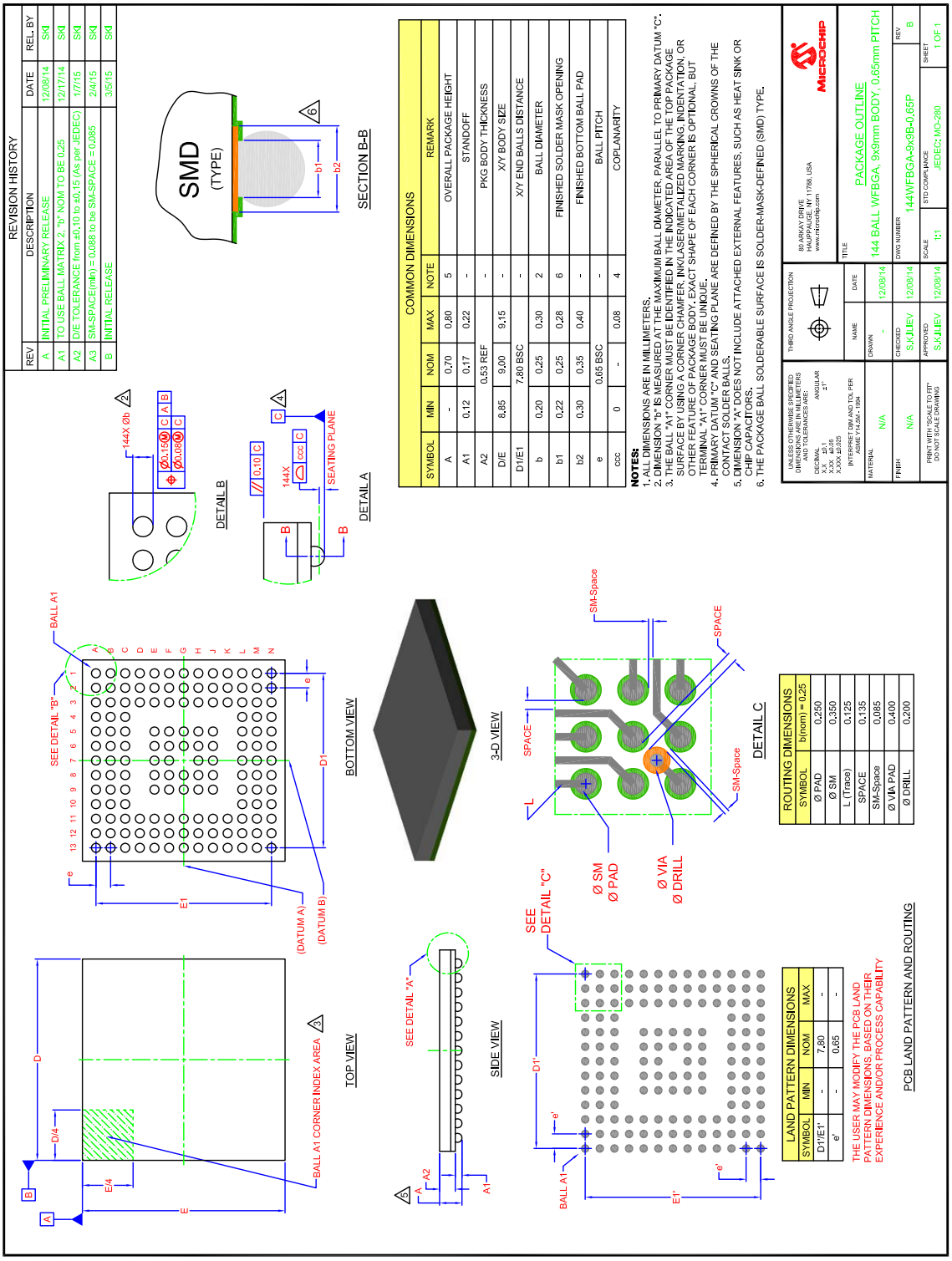
2.11 Packages

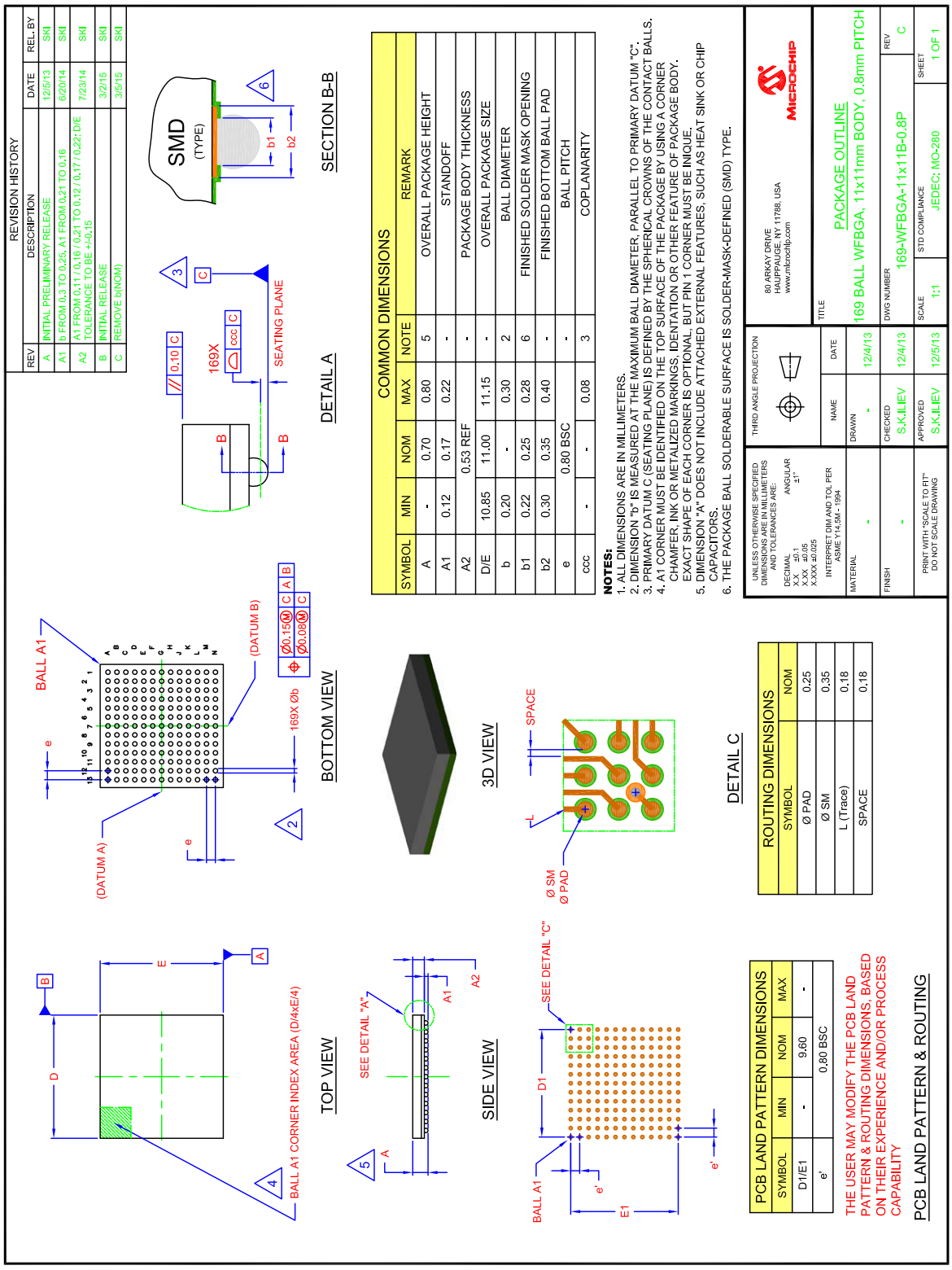
2.11.1 144 PIN WFBGA PACKAGE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.



2.11.2 169 PIN WFBGA PACKAGE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.



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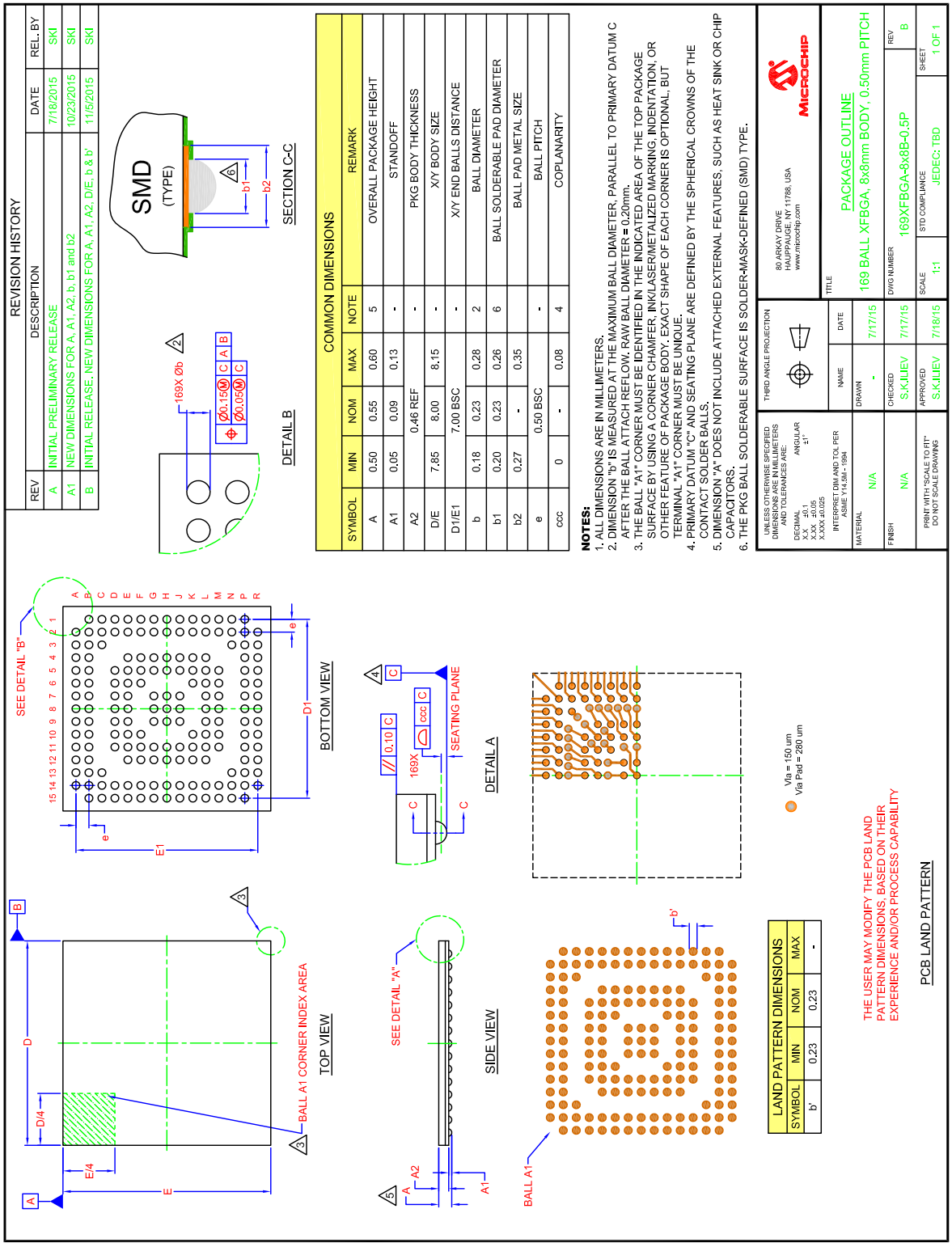
2.11.3 169 PIN XFBGA PACKAGE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.



3.0 DEVICE INVENTORY

3.1 Conventions

Term	Definition
Block	Used to identify or describe the logic or IP Blocks implemented in the device.
Reserved	Reserved registers and bits defined in the following table are read only values that return 0 when read. Writes to these reserved registers have no effect.
TEST	Microchip Reserved locations which should not be modified from their default value. Changing a TEST register or a TEST field within a register may cause unwanted results.
b	The letter ‘b’ following a number denotes a binary number.
h	The letter ‘h’ following a number denotes a hexadecimal number.

Register access notation is in the form “Read / Write”. A Read term without a Write term means that the bit is read-only and writing has no effect. A Write term without a Read term means that the bit is write-only, and assumes that reading returns all zeros.

Register Field Type	Field Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RS	**Read to Set:** This bit is set on read.
RC	**Read to Clear:** Content is cleared after the read. Writes have no effect.
WC	**Write One to Clear:** writing a one clears the value. Writing a zero has no effect.
WZC	**Write Zero to Clear:** writing a zero clears the value. Writing a one has no effect.
WS	**Write One to Set:** writing a one sets the value to 1. Writing a zero has no effect.
WZS	**Write Zero to Set:** writing a zero sets the value to 1. Writing a one has no effect.

3.2 GPIO Documentation Conventions

The GPIO registers and bits are allocated for the full GPIO complement. Therefore, even GPIOs that are not implemented in the package will appear in the GPIO register lists. Please refer to the pinout to determine which GPIOs are bonded out in the package. GPIOs that are not available in the package should not have their configuration register altered.

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3.3 Block Overview and Base Addresses

Feature	Instance	Logical Device Number (LDN)	Base Address
Watchdog Timer			4000_0000h
16-bit Basic Timer	0		4000_0C00h
16-bit Basic Timer	1		4000_0C20h
16-bit Basic Timer	2		4000_0C40h
16-bit Basic Timer	3		4000_0C60h
32-bit Basic Timer	0		4000_0C80h
32-bit Basic Timer	1		4000_0CA0h
16-bit Timer-Counter	0		4000_0D00h
16-bit Timer-Counter	1		4000_0D20h
16-bit Timer-Counter	2		4000_0D40h
16-bit Timer-Counter	3		4000_0D60h
Capture-Compare Timers			4000_1000h
RC-ID	0		4000_1400h
RC-ID	1		4000_1480h
RC-ID	2		4000_1500h
DMA Controller			4000_2400h
EEPROM Controller			4000_2C00h
SMB-I2C Controller	0		4000_4000h
SMB-I2C Controller	1		4000_4400h
SMB-I2C Controller	2		4000_4800h
SMB-I2C Controller	3		4000_4C00h
Quad Master SPI			4000_5400h
16-bit PWM	0		4000_5800h
16-bit PWM	1		4000_5810h
16-bit PWM	2		4000_5820h
16-bit PWM	3		4000_5830h
16-bit PWM	4		4000_5840h
16-bit PWM	5		4000_5850h
16-bit PWM	6		4000_5860h
16-bit PWM	7		4000_5870h
16-bit PWM	8		4000_5880h
16-bit PWM	9		4000_5890h
16-bit PWM	10		4000_58A0h
16-bit Tach	0		4000_6000h
16-bit Tach	1		4000_6010h
16-bit Tach	2		4000_6020h
PECI			4000_6400h
RTOS Timer			4000_7400h
ADC			4000_7C00h
Trace FIFO			4000_8C00h
Note 1: The eSPI block occupies two logical devices, Dh and Eh			

Feature	Instance	Logical Device Number (LDN)	Base Address
PS-2	0		4000_9000h
PS-2	1		4000_9040h
PS-2	2		4000_9080h
GP-SPI	0		4000_9400h
GP-SPI	1		4000_9480h
Hibernation Timer	0		4000_9800h
Hibernation Timer	1		4000_9820h
Keyboard Matrix Scan			4000_9C00h
RPM to PWM Fan Controller	0		4000_A000h
RPM to PWM Fan Controller	1		4000_A080h
VBAT Register Bank			4000_A400h
VBAT Powered RAM			4000_A800h
Week Timer			4000_AC80h
VBAT-Powered Control Interface			4000_AE00h
Blinking-Breathing LED	0		4000_B800h
Blinking-Breathing LED	1		4000_B900h
Blinking-Breathing LED	2		4000_BA00h
Blinking-Breathing LED	3		4000_BB00h
Public Key Engine			4000_BD00h
Random Number Generator			4000_BE00h
BC-Link Master	0		4000_CD00h
BC-Link Master	1		4000_CD20h
Hash Engine			4000_D000h
Symmetric Encryption Engine			4000_D200h
Interrupt Aggregator			4000_E000h
EC Subsystem Registers			4000_FC00h
JTAG			4008_0000h
Power, Clocks and Resets			4008_0100h
GPIOs			4008_1000h
eFuse			4008_2000h
Mailbox		0h	400F_0000h
8042 Emulated Keyboard Controller		1h	400F_0400h
ACPI EC Channel	0	2h	400F_0800h
ACPI EC Channel	1	3h	400F_0C00h
ACPI EC Channel	2	4h	400F_1000h
ACPI EC Channel	3	5h	400F_1400h
ACPI EC Channel	4	6h	400F_1800h
ACPI PM1		7h	400F_1C00h
Port 92-Legacy		8h	400F_2000h
UART	0	9h	400F_2400h
UART	1	Ah	400F_2800h
LPC Interface		Ch	400F_3000h
Note 1: The eSPI block occupies two logical devices, Dh and Eh			

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Feature	Instance	Logical Device Number (LDN)	Base Address
eSPI Interface IO Component	Note 1	Dh	400F_3400h
eSPI Interface Memory Component	Note 1	Eh	400F_3800h
Embedded Memory Interface (EMI)	0	10h	400F_4000h
Embedded Memory Interface (EMI)	1	11h	400F_4400h
Embedded Memory Interface (EMI)	2	12h	400F_4800h
Real Time Clock		14h	400F_5000h
BIOS Debug Port (Port 80)	0	20h	400F_8000h
BIOS Debug Port (Port 80)	1	21h	400F_8400h
eSPI Virtual Wires			400F_9C00h
Global Configuration		3Fh	400F_FF00h
Note 1: The eSPI block occupies two logical devices, Dh and Eh			

3.4 Sleep Enable Register Assignments

Block	Instance	Bit Position	Sleep Enable Register	Clock Required Register	Reset Enable Register
TEST		0	Sleep Enable 0	Clock Required 0	Reset Enable 0
eFuse		1	Sleep Enable 0	Clock Required 0	Reset Enable 0
ISPI		2	Sleep Enable 0	Clock Required 0	Reset Enable 0
Interrupt		0	Sleep Enable 1	Clock Required 1	Reset Enable 1
PECI		1	Sleep Enable 1	Clock Required 1	Reset Enable 1
Tach	0	2	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	0	4	Sleep Enable 1	Clock Required 1	Reset Enable 1
PMC		5	Sleep Enable 1	Clock Required 1	Reset Enable 1
DMA		6	Sleep Enable 1	Clock Required 1	Reset Enable 1
TFDP		7	Sleep Enable 1	Clock Required 1	Reset Enable 1
PROCESSOR		8	Sleep Enable 1	Clock Required 1	Reset Enable 1
WDT		9	Sleep Enable 1	Clock Required 1	Reset Enable 1
SMB-I2C	0	10	Sleep Enable 1	Clock Required 1	Reset Enable 1
Tach	1	11	Sleep Enable 1	Clock Required 1	Reset Enable 1
Tach	2	12	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	1	20	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	2	21	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	3	22	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	4	23	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	5	24	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	6	25	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	7	26	Sleep Enable 1	Clock Required 1	Reset Enable 1
PWM	8	27	Sleep Enable 1	Clock Required 1	Reset Enable 1
EC Register Bank		29	Sleep Enable 1	Clock Required 1	Reset Enable 1
Basic Timer 16	0	30	Sleep Enable 1	Clock Required 1	Reset Enable 1
Basic Timer 16	1	31	Sleep Enable 1	Clock Required 1	Reset Enable 1
LPC		0	Sleep Enable 2	Clock Required 2	Reset Enable 2
UART	0	1	Sleep Enable 2	Clock Required 2	Reset Enable 2
UART	1	2	Sleep Enable 2	Clock Required 2	Reset Enable 2
Global Configuration		12	Sleep Enable 2	Clock Required 2	Reset Enable 2
ACPI EC	0	13	Sleep Enable 2	Clock Required 2	Reset Enable 2
ACPI EC	1	14	Sleep Enable 2	Clock Required 2	Reset Enable 2
ACPI PM1		15	Sleep Enable 2	Clock Required 2	Reset Enable 2
8042 Emulation		16	Sleep Enable 2	Clock Required 2	Reset Enable 2
Mailbox		17	Sleep Enable 2	Clock Required 2	Reset Enable 2
RTC		18	Sleep Enable 2	Clock Required 2	Reset Enable 2
eSPI		19	Sleep Enable 2	Clock Required 2	
Reserved		19			Reset Enable 2
ACPI EC	2	21	Sleep Enable 2	Clock Required 2	
Reserved		21			Reset Enable 2
ACPI EC	3	22	Sleep Enable 2	Clock Required 2	
Reserved		22			Reset Enable 2
ACPI EC	4	23	Sleep Enable 2	Clock Required 2	

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Block	Instance	Bit Position	Sleep Enable Register	Clock Required Register	Reset Enable Register
Reserved		23			Reset Enable 2
Port 80	0	25	Sleep Enable 2	Clock Required 2	
Reserved		25			Reset Enable 2
Port 80	1	26	Sleep Enable 2	Clock Required 2	
Reserved		26			Reset Enable 2
ADC		3	Sleep Enable 3	Clock Required 3	Reset Enable 3
PS2	0	5	Sleep Enable 3	Clock Required 3	Reset Enable 3
PS2	1	6	Sleep Enable 3	Clock Required 3	Reset Enable 3
PS2	2	7	Sleep Enable 3	Clock Required 3	Reset Enable 3
GP-SPI	0	9	Sleep Enable 3	Clock Required 3	Reset Enable 3
Hibernation Timer	0	10	Sleep Enable 3	Clock Required 3	Reset Enable 3
Keyscan		11	Sleep Enable 3	Clock Required 3	Reset Enable 3
RPM2PWM	0	12	Sleep Enable 3	Clock Required 3	Reset Enable 3
SMB-I2C	1	13	Sleep Enable 3	Clock Required 3	Reset Enable 3
SMB-I2C	2	14	Sleep Enable 3	Clock Required 3	Reset Enable 3
SMB-I2C	3	15	Sleep Enable 3	Clock Required 3	Reset Enable 3
LED	0	16	Sleep Enable 3	Clock Required 3	Reset Enable 3
LED	1	17	Sleep Enable 3	Clock Required 3	Reset Enable 3
LED	2	18	Sleep Enable 3	Clock Required 3	Reset Enable 3
BC Master	0	19	Sleep Enable 3	Clock Required 3	Reset Enable 3
GP-SPI	1	20	Sleep Enable 3	Clock Required 3	Reset Enable 3
Basic Timer 16	2	21	Sleep Enable 3	Clock Required 3	Reset Enable 3
Basic Timer 16	3	22	Sleep Enable 3	Clock Required 3	Reset Enable 3
Basic Timer 32	0	23	Sleep Enable 3	Clock Required 3	Reset Enable 3
Basic Timer 32	1	24	Sleep Enable 3	Clock Required 3	Reset Enable 3
LED	3	25	Sleep Enable 3	Clock Required 3	Reset Enable 3
PKE		26	Sleep Enable 3	Clock Required 3	Reset Enable 3
RNG		27	Sleep Enable 3	Clock Required 3	Reset Enable 3
AES-Hash		28	Sleep Enable 3	Clock Required 3	Reset Enable 3
Hibernation Timer	1	29	Sleep Enable 3	Clock Required 3	Reset Enable 3
Capture Compare Timer		30	Sleep Enable 3	Clock Required 3	Reset Enable 3
PWM	9	31	Sleep Enable 3	Clock Required 3	Reset Enable 3
PWM	10	0	Sleep Enable 4	Clock Required 4	Reset Enable 4
PWM	11	1	Sleep Enable 4	Clock Required 4	Reset Enable 4
16-bit Counter/Timer	0	2	Sleep Enable 4	Clock Required 4	Reset Enable 4
16-bit Counter/Timer	1	3	Sleep Enable 4	Clock Required 4	Reset Enable 4
16-bit Counter/Timer	2	4	Sleep Enable 4	Clock Required 4	Reset Enable 4
16-bit Counter/Timer	3	5	Sleep Enable 4	Clock Required 4	Reset Enable 4
RTOS Timer		6	Sleep Enable 4	Clock Required 4	Reset Enable 4
RPM2PWM	1	7	Sleep Enable 4	Clock Required 4	Reset Enable 4
Quad SPI Master		8	Sleep Enable 4	Clock Required 4	Reset Enable 4
BC Master	1	9	Sleep Enable 4	Clock Required 4	Reset Enable 4
RC_ID	0	10	Sleep Enable 4	Clock Required 4	Reset Enable 4
RC_ID	1	11	Sleep Enable 4	Clock Required 4	Reset Enable 4

Block	Instance	Bit Position	Sleep Enable Register	Clock Required Register	Reset Enable Register
RC_ID	2	12	Sleep Enable 4	Clock Required 4	Reset Enable 4
EEPROM		14	Sleep Enable 4	Clock Required 4	Reset Enable 4

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3.5 Interrupt Aggregator Bit Assignments

Note: Interrupt Aggregator bits associated with GPIOs not present in the pinout for a particular device are Reserved.

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ8	0	GPIO140	GPIO Event	Yes	GPIO Interrupt Event	0	N/A
	1	GPIO141	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO142	GPIO Event	Yes	GPIO Interrupt Event		
	3	GPIO143	GPIO Event	Yes	GPIO Interrupt Event		
	4	GPIO144	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO145	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO146	GPIO Event	Yes	GPIO Interrupt Event		
	7	GPIO147	GPIO Event	Yes	GPIO Interrupt Event		
	8	GPIO150	GPIO Event	Yes	GPIO Interrupt Event		
	9	GPIO151	GPIO Event	Yes	GPIO Interrupt Event		
	10	GPIO152	GPIO Event	Yes	GPIO Interrupt Event		
	11	GPIO153	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO154	GPIO Event	Yes	GPIO Interrupt Event		
	13	GPIO155	GPIO Event	Yes	GPIO Interrupt Event		
	14	GPIO156	GPIO Event	Yes	GPIO Interrupt Event		
	15	GPIO157	GPIO Event	Yes	GPIO Interrupt Event		
	16	GPIO160	GPIO Event	Yes	GPIO Interrupt Event		
	17	GPIO161	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO162	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO163	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO164	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO165	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO166	GPIO Event	Yes	GPIO Interrupt Event		
	23	Reserved	-	-			
	24	GPIO170	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO171	GPIO Event	Yes	GPIO Interrupt Event		
	26	GPIO172	GPIO Event	Yes	GPIO Interrupt Event		
	27	GPIO173	GPIO Event	Yes	GPIO Interrupt Event		
	28	GPIO174	GPIO Event	Yes	GPIO Interrupt Event		
	29	GPIO175	GPIO Event	Yes	GPIO Interrupt Event		
	30	Reserved	-	-			
	31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ9	0	GPIO100	GPIO Event	Yes	GPIO Interrupt Event	1	N/A
	1	GPIO101	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO102	GPIO Event	Yes	GPIO Interrupt Event		
	3	Reserved	-	-			
	4	GPIO104	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO105	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO106	GPIO Event	Yes	GPIO Interrupt Event		
	7	GPIO107	GPIO Event	Yes	GPIO Interrupt Event		
	8	GPIO110	GPIO Event	Yes	GPIO Interrupt Event		
	9	GPIO111	GPIO Event	Yes	GPIO Interrupt Event		
	10	GPIO112	GPIO Event	Yes	GPIO Interrupt Event		
	11	GPIO113	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO114	GPIO Event	Yes	GPIO Interrupt Event		
	13	GPIO115	GPIO Event	Yes	GPIO Interrupt Event		
	14	Reserved	-	-			
	15	Reserved	-	-			
	16	GPIO120	GPIO Event	Yes	GPIO Interrupt Event		
	17	GPIO121	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO122	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO123	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO124	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO125	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO126	GPIO Event	Yes	GPIO Interrupt Event		
	23	GPIO127	GPIO Event	Yes	GPIO Interrupt Event		
	24	GPIO130	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO131	GPIO Event	Yes	GPIO Interrupt Event		
	26	GPIO132	GPIO Event	Yes	GPIO Interrupt Event		
	27	GPIO133	GPIO Event	Yes	GPIO Interrupt Event		
	28	GPIO134	GPIO Event	Yes	GPIO Interrupt Event		
	29	GPIO135	GPIO Event	Yes	GPIO Interrupt Event		
	30	Reserved	-	-			
	31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ10	0	GPIO040	GPIO Event	Yes	GPIO Interrupt Event	2	N/A
	1	GPIO041	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO042	GPIO Event	Yes	GPIO Interrupt Event		
	3	GPIO043	GPIO Event	Yes	GPIO Interrupt Event		
	4	GPIO044	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO045	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO046	GPIO Event	Yes	GPIO Interrupt Event		
	7	GPIO047	GPIO Event	Yes	GPIO Interrupt Event		
	8	GPIO050	GPIO Event	Yes	GPIO Interrupt Event		
	9	GPIO051	GPIO Event	Yes	GPIO Interrupt Event		
	10	GPIO052	GPIO Event	Yes	GPIO Interrupt Event		
	11	GPIO053	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO054	GPIO Event	Yes	GPIO Interrupt Event		
	13	GPIO055	GPIO Event	Yes	GPIO Interrupt Event		
	14	GPIO056	GPIO Event	Yes	GPIO Interrupt Event		
	15	GPIO057	GPIO Event	Yes	GPIO Interrupt Event		
	16	GPIO060	GPIO Event	Yes	GPIO Interrupt Event		
	17	GPIO061	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO062	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO063	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO064	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO065	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO066	GPIO Event	Yes	GPIO Interrupt Event		
	23	GPIO067	GPIO Event	Yes	GPIO Interrupt Event		
	24	GPIO070	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO071	GPIO Event	Yes	GPIO Interrupt Event		
	26	GPIO072	GPIO Event	Yes	GPIO Interrupt Event		
	27	GPIO073	GPIO Event	Yes	GPIO Interrupt Event		
	28	Reserved	-	-			
	29	Reserved	-	-			
	30	Reserved	-	-			
	31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ11	0	GPIO000	GPIO Event	Yes	GPIO Interrupt Event	3	N/A
	1	GPIO001	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO002	GPIO Event	Yes	GPIO Interrupt Event		
	3	GPIO003	GPIO Event	Yes	GPIO Interrupt Event		
	4	GPIO004	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO005	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO006	GPIO Event	Yes	GPIO Interrupt Event		
	7	GPIO007	GPIO Event	Yes	GPIO Interrupt Event		
	8	GPIO010	GPIO Event	Yes	GPIO Interrupt Event		
	9	GPIO011	GPIO Event	Yes	GPIO Interrupt Event		
	10	GPIO012	GPIO Event	Yes	GPIO Interrupt Event		
	11	GPIO013	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO014	GPIO Event	Yes	GPIO Interrupt Event		
	13	GPIO015	GPIO Event	Yes	GPIO Interrupt Event		
	14	GPIO016	GPIO Event	Yes	GPIO Interrupt Event		
	15	GPIO017	GPIO Event	Yes	GPIO Interrupt Event		
	16	GPIO020	GPIO Event	Yes	GPIO Interrupt Event		
	17	GPIO021	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO022	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO023	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO024	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO025	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO026	GPIO Event	Yes	GPIO Interrupt Event		
	23	GPIO027	GPIO Event	Yes	GPIO Interrupt Event		
	24	GPIO030	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO031	GPIO Event	Yes	GPIO Interrupt Event		
	26	GPIO032	GPIO Event	Yes	GPIO Interrupt Event		
	27	GPIO033	GPIO Event	Yes	GPIO Interrupt Event		
	28	GPIO034	GPIO Event	Yes	GPIO Interrupt Event		
	29	GPIO035	GPIO Event	Yes	GPIO Interrupt Event		
	30	GPIO036	GPIO Event	Yes	GPIO Interrupt Event		
	31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ12	0	GPIO200	GPIO Event	Yes	GPIO Interrupt Event	4	N/A
	1	GPIO201	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO202	GPIO Event	Yes	GPIO Interrupt Event		
	3	GPIO203	GPIO Event	Yes	GPIO Interrupt Event		
	4	GPIO204	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO205	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO206	GPIO Event	Yes	GPIO Interrupt Event		
	7	GPIO207	GPIO Event	Yes	GPIO Interrupt Event		
	8	GPIO210	GPIO Event	Yes	GPIO Interrupt Event		
	9	GPIO211	GPIO Event	Yes	GPIO Interrupt Event		
	10	GPIO212	GPIO Event	Yes	GPIO Interrupt Event		
	11	GPIO213	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO214	GPIO Event	Yes	GPIO Interrupt Event		
	13	GPIO215	GPIO Event	Yes	GPIO Interrupt Event		
	14	GPIO216	GPIO Event	Yes	GPIO Interrupt Event		
	15	GPIO217	GPIO Event	Yes	GPIO Interrupt Event		
	16	Reserved	-	-			
	17	GPIO221	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO222	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO223	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO224	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO225	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO226	GPIO Event	Yes	GPIO Interrupt Event		
	23	GPIO227	GPIO Event	Yes	GPIO Interrupt Event		
	24	GPIO230	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO231	GPIO Event	Yes	GPIO Interrupt Event		
	26	Reserved	-	-			
	27	GPIO233	GPIO Event	Yes	GPIO Interrupt Event		
	28	GPIO234	GPIO Event	Yes	GPIO Interrupt Event		
	29	Reserved	-	-			
	30	Reserved	-	-			
	31	Reserved					
GIRQ13	0	SMB-I2C Controller 0	SMB-I2C	No	SMB-I2C Controller 0 Interrupt Event	5	20
	1	SMB-I2C Controller 1	SMB-I2C	No	SMB-I2C Controller 1 Interrupt Event		21
	2	SMB-I2C Controller 2	SMB-I2C	No	SMB-I2C Controller 2 Interrupt Event		22
	3	SMB-I2C Controller 3	SMB-I2C	No	SMB-I2C Controller 3 Interrupt Event		23
	4-31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ14	0	DMA Controller	DMA0	No	DMA Controller - Channel 0 Interrupt Event	6	24
	1	DMA Controller	DMA1	No	DMA Controller - Channel 1 Interrupt Event		25
	2	DMA Controller	DMA2	No	DMA Controller - Channel 2 Interrupt Event		26
	3	DMA Controller	DMA3	No	DMA Controller - Channel 3 Interrupt Event		27
	4	DMA Controller	DMA4	No	DMA Controller - Channel 4 Interrupt Event		28
	5	DMA Controller	DMA5	No	DMA Controller - Channel 5 Interrupt Event		29
	6	DMA Controller	DMA6	No	DMA Controller - Channel 6 Interrupt Event		30
	7	DMA Controller	DMA7	No	DMA Controller - Channel 7 Interrupt Event		31
	8	DMA Controller	DMA8	No	DMA Controller - Channel 8 Interrupt Event		32
	9	DMA Controller	DMA9	No	DMA Controller - Channel 9 Interrupt Event		33
	10	DMA Controller	DMA10	No	DMA Controller - Channel 10 Interrupt Event		34
	11	DMA Controller	DMA11	No	DMA Controller - Channel 11 Interrupt Event		35
	12	DMA Controller	DMA12	No	DMA Controller - Channel 12 Interrupt Event		36
	13	DMA Controller	DMA13	No	DMA Controller - Channel 13 Interrupt Event		37
	14-31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ15	0	UART 0	UART	No	UART Interrupt Event	7	40
	1	UART 1	UART	No	UART Interrupt Event		41
	2	EMI 0	Host-to-EC	No	Embedded Memory Interface 0 - Host-to-EC Interrupt		42
	3	EMI 1	Host-to-EC	No	Embedded Memory Interface 1 - Host-to-EC Interrupt		43
	4	EMI 2	Host-to-EC	No	Embedded Memory Interface 2- Host-to-EC Interrupt		44
	5	ACPI EC Interface 0	IBF	No	ACPI EC Interface 0 - Input Buffer Full Event		45
	6	ACPI EC Interface 0	OBE	No	ACPI EC Interface 0 - Output Buffer Empty Event, asserted when OBE flag goes to 1		46
	7	ACPI EC Interface 1	IBF	No	ACPI EC Interface 1 - Input Buffer Full Event		47
	8	ACPI EC Interface 1	OBE	No	ACPI EC Interface 1 - Output Buffer Empty Event, asserted when OBE flag goes to 1		48
	9	ACPI EC Interface 2	IBF	No	ACPI EC Interface 2 - Input Buffer Full Event		49
	10	ACPI EC Interface 2	OBE	No	ACPI EC Interface 2 - Output Buffer Empty Event, asserted when OBE flag goes to 1		50
	11	ACPI EC Interface 3	IBF	No	ACPI EC Interface 3 - Input Buffer Full Event		51
	12	ACPI EC Interface 3	OBE	No	ACPI EC Interface 3 - Output Buffer Empty Event, asserted when OBE flag goes to 1		52
	13	ACPI EC Interface 4	IBF	No	ACPI EC Interface 4 - Input Buffer Full Event		53
	14	ACPI EC Interface 4	OBE	No	ACPI EC Interface 4- Output Buffer Empty Event, asserted when OBE flag goes to 1		54
	15	ACPI_PM1 Interface	PM1_CTL	No	ACPI_PM1 Interface - PM1_CTL2 Interrupt Event		55
	16	ACPI_PM1 Interface	PM1_EN	No	ACPI_PM1 Interface - PM1_EN2 Interrupt Event		56
	17	ACPI_PM1 Interface	PM1_STS	No	ACPI_PM1 Interface - PM1_STS2 Interrupt Event		57
	18	8042 Keyboard Controller	OBE	No	8042 Keyboard Controller - Output Buffer Empty Event, asserted when OBE flag goes to 1		58
	19	8042 Keyboard Controller	IBF	No	8042 Keyboard Controller - Input Buffer Full Event		59
	20	Mailbox Interface	MBX	No	Mailbox Interface - Host-to-EC Interrupt Event		60
	21	Reserved					
	22	Port 80 Debug 0	BDP_INT	No	Port 80h BIOS Debug Port Event		62
	23	Port 80 Debug 1	BDP_INT	No	Port 80h BIOS Debug Port Event		63
	24	Test	Test	-	-		64

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ16	0	Public Key Engine	PKE ERROR	No	PKE core error detected	8	65
	1	Public Key Engine	PKE END	No	PKE completed processing		66
	2	Random Number Generator	RNG	No	RNG completed processing		67
	3	AES	AES	No	Interrupt from AES block		68
	4	Hash	HASH	No	Interrupt from SHA block		69
	5-31	Reserved					
GIRQ17	0	PECI	PECI_INT	No	PECI Host Event	9	70
	1	TACH 0	TACH	No	Tachometer 0 Interrupt Event		71
	2	TACH 1	TACH	No	Tachometer 1 Interrupt Event		72
	3	TACH 2	TACH	No	Tachometer 2 Interrupt Event		73
	4	RPM2PWM 0	FAN_FAIL	No	Failure to achieve target RPM		74
	5	RPM2PWM 0	FAN_STALL	No	Fan stall condition		75
	6	RPM2PWM 1	FAN_FAIL	No	Failure to achieve target RPM		76
	7	RPM2PWM 1	FAN_STALL	No	Fan stall condition		77
	8	ADC Controller	ADC_Single_Int	No	ADC Controller - Single-Sample ADC Conversion Event		78
	9	ADC Controller	ADC_Repeat_Int	No	ADC Controller - Repeat-Sample ADC Conversion Event		79
	10	RC-ID 0	RCID	No	0-1 transition of RC-ID done flag		80
	11	RC-ID 1	RCID	No	0-1 transition of RC-ID done flag		81
	12	RC-ID 2	RCID	No	0-1 transition of RC-ID done flag		82
	13	Breathing LED 0	PWM_WDT	No	Blinking LED 0 Watchdog Event		83
	14	Breathing LED 1	PWM_WDT	No	Blinking LED 1 Watchdog Event		84
	15	Breathing LED 2	PWM_WDT	No	Blinking LED 2 Watchdog Event		85
	16	Breathing LED 3	PWM_WDT	No	Blinking LED 3 Watchdog Event		86
	17-24		Reserved				
	25	RTOS Timer	SWI_0	No	Soft Interrupt request 0		
	26	RTOS Timer	SWI_1	No	Soft Interrupt request 1		
	27	RTOS Timer	SWI_2	No	Soft Interrupt request 2		
	28	RTOS Timer	SWI_3	No	Soft Interrupt request 3		
	29-31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ18	0	LPC	LPC_INTERNAL_ ERROR	No	LPC BAR conflict or internal bus error	10	90
	1	Quad Master SPI Controller	QMSPI_INT	No	Master SPI Controller Requires Servicing		91
	2	GP-SPI 0	TXBE_STS	No	SPI TX buffer empty		92
	3	GP-SPI 0	RXBF_STS	No	SPI RX buffer full		93
	4	GP-SPI 1	TXBE_STS	No	SPI TX buffer empty		94
	5	GP-SPI 1	RXBF_STS	No	SPI RX buffer full		95
	6	BC-Link 0	BCM_BUSY_CLR	No	BC-Link Busy Clear Flag		97
	7	BC-Link 0	BCM_ERR	No	BC-Link Error Flag Interrupt		96
	8	BC-Link 1	BCM_BUSY_CLR	No	BC-Link Busy Clear Flag		99
	9	BC-Link 1	BCM_ERR	No	BC-Link Error Flag Interrupt		98
	10	PS2 Interface 0	PS2_ACT	No	PS/2 Device Interface 0 - Activity Interrupt Event		100
	11	PS2 Interface 1	PS2_ACT	No	PS/2 Device Interface 1 - Activity Interrupt Event		101
	12	PS2 Interface 2	PS2_ACT	No	PS/2 Device Interface 2 - Activity Interrupt Event		102
	13	EEPROM	EEPROM	No	EEPROM Transfer Complete		155
	14-31	Reserved					
GIRQ19	0	eSPI_Slave	INTR_PC	No	Peripheral Channel Interrupt	11	103
	1	eSPI_Slave	INTR_BM1	No	Bus Mastering Channel 1 Interrupt		104
	2	eSPI_Slave	INTR_BM2	No	Bus Mastering Channel 2 Interrupt		105
	3	eSPI_Slave	INTR_LTR	No	Peripheral Message (LTR) Interrupt		106
	4	eSPI_Slave	INTR_OOB_ UP	No	Out of Band Channel Up Interrupt		107
	5	eSPI_Slave	INTR_OOB_ DOWN	No	Out of Band Channel Down Interrupt		108
	6	eSPI_Slave	INTR_FLASH	No	Flash Channel Interrupt		109
	7	eSPI_Slave	eSPI_RESET	No	eSPI_RESET		110
	8	eSPI_Slave	VWIRE_ENABLE	No	Virtual Wire Channel Enable Asserted		156
	9-31	Reserved					
GIRQ20	0-8	Test	Test	-	-	12	N/A
	9-31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ21	0	RTOS Timer	RTOS_TIMER	Yes	32-bit RTOS Timer Event	13	111
	1	Hibernation Timer 0	HTIMER	Yes	Hibernation Timer Event		112
	2	Hibernation Timer 1	HTIMER	Yes	Hibernation Timer Event		113
	3	Week Alarm	WEEK_ALARM_INT	Yes	Week Alarm Interrupt.		114
	4	Week Alarm	SUB_WEEK_ ALARM_INT	Yes	Sub-Week Alarm Interrupt		115
	5	Week Alarm	ONE_SECOND	Yes	Week Alarm - One Second Interrupt		116
	6	Week Alarm	SUB_SECOND	Yes	Week Alarm - Sub-second Interrupt		117
	7	Reserved					-
	8	RTC	RTC	Yes	Real Time Clock Interrupt		119
	9	RTC	RTC ALARM	Yes	Real Time Clock Alarm Interrupt		120
	10	Reserved					-
	11	VBAT-Powered Control Interface	VCI_IN0	Yes	VCI_IN0 Active-low Input Pin Interrupt		122
	12	VBAT-Powered Control Interface	VCI_IN1	Yes	VCI_IN1 Active-low Input Pin Interrupt		123
	13	VBAT-Powered Control Interface	VCI_IN2	Yes	VCI_IN2 Active-low Input Pin Interrupt		124
	14	VBAT-Powered Control Interface	VCI_IN3	Yes	VCI_IN3 Active-low Input Pin Interrupt		125
	15	VBAT-Powered Control Interface	VCI_IN4	Yes	VCI_IN4 Active-low Input Pin Interrupt		126
	16	VBAT-Powered Control Interface	VCI_IN5	Yes	VCI_IN5 Active-low Input Pin Interrupt		127
	17	VBAT-Powered Control Interface	VCI_IN6	Yes	VCI_IN6 Active-low Input Pin Interrupt		128
	18	PS2 Port	PS2_0A_WK	Yes	PS2 Wake Event. Start bit detect.		129
	19	PS2 Port	PS2_0B_WK	Yes	PS2 Wake Event. Start bit detect.		130
	20	PS2 Port	PS2_1A_WK	Yes	PS2 Wake Event. Start bit detect.		131
	21	PS2 Port	PS2_1B_WK	Yes	PS2 Wake Event. Start bit detect.		132
	22	PS2 Port	PS2_2_WK	Yes	PS2 Wake Event. Start bit detect.		133
	23-24	Reserved					
	25	Keyscan	KSC_INT	Yes	Keyboard Scan Interface Runtime Interrupt		135
	26-31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ22	0	LPC Interface	LPC_WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - LPC Traffic Detected	N/A	N/A
	1	SMB-I2C Controller 0	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.0 START Detected		
	2	SMB-I2C Controller 1	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.1 START Detected		
	3	SMB-I2C Controller 2	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.2 START Detected		
	4	SMB-I2C Controller 3	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.3 START Detected		
	5-8	Reserved					
	9	ESPI Interface	ESPI_WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - ESPI Traffic Detected		
	10-31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ23	0	16-Bit Basic Timer 0	Timer_Event	No	Basic Timer Event	14	136
	1	16-Bit Basic Timer 1	Timer_Event	No	Basic Timer Event		137
	2	16-Bit Basic Timer 2	Timer_Event	No	Basic Timer Event		138
	3	16-Bit Basic Timer 3	Timer_Event	No	Basic Timer Event		139
	4	32-Bit Basic Timer 0	Timer_Event	No	Basic Timer Event		140
	5	32-Bit Basic Timer 1	Timer_Event	No	Basic Timer Event		141
	6	Counter/Timer 0	Timer_Event	No	16-bit Timer/Counter Event		142
	7	Counter/Timer 1	Timer_Event	No	16-bit Timer/Counter Event		143
	8	Counter/Timer 2	Timer_Event	No	16-bit Timer/Counter Event		144
	9	Counter/Timer 3	Timer_Event	No	16-bit Timer/Counter Event		145
	10	Capture Compare Timer	CAPTURE TIMER	No	CCT Counter Event		146
	11	Capture Compare Timer	CAPTURE 0	No	CCT Capture 0 Event		147
	12	Capture Compare Timer	CAPTURE 1	No	CCT Capture 1 Event		148
	13	Capture Compare Timer	CAPTURE 2	No	CCT Capture 2 Event		149
	14	Capture Compare Timer	CAPTURE 3	No	CCT Capture 3 Event		150
	15	Capture Compare Timer	CAPTURE 4	No	CCT Capture 4 Event		151
	16	Capture Compare Timer	CAPTURE 5	No	CCT Capture 5 Event		152
	17	Capture Compare Timer	COMPARE 0	No	CCT Compare 0 Event		153
	18	Capture Compare Timer	COMPARE 1	No	CCT Compare 1 Event		154
	19-31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ24	0	eSPI_Slave	MSVW00_SRC0	Yes	M-to-S VW Interrupt Event	15	N/A
	1	eSPI_Slave	MSVW00_SRC1	Yes	M-to-S VW Interrupt Event		
	2	eSPI_Slave	MSVW00_SRC2	Yes	M-to-S VW Interrupt Event		
	3	eSPI_Slave	MSVW00_SRC3	Yes	M-to-S VW Interrupt Event		
	4	eSPI_Slave	MSVW01_SRC0	Yes	M-to-S VW Interrupt Event		
	5	eSPI_Slave	MSVW01_SRC1	Yes	M-to-S VW Interrupt Event		
	6	eSPI_Slave	MSVW01_SRC2	Yes	M-to-S VW Interrupt Event		
	7	eSPI_Slave	MSVW01_SRC3	Yes	M-to-S VW Interrupt Event		
	8	eSPI_Slave	MSVW02_SRC0	Yes	M-to-S VW Interrupt Event		
	9	eSPI_Slave	MSVW02_SRC1	Yes	M-to-S VW Interrupt Event		
	10	eSPI_Slave	MSVW02_SRC2	Yes	M-to-S VW Interrupt Event		
	11	eSPI_Slave	MSVW02_SRC3	Yes	M-to-S VW Interrupt Event		
	12	eSPI_Slave	MSVW03_SRC0	Yes	M-to-S VW Interrupt Event		
	13	eSPI_Slave	MSVW03_SRC1	Yes	M-to-S VW Interrupt Event		
	14	eSPI_Slave	MSVW03_SRC2	Yes	M-to-S VW Interrupt Event		
	15	eSPI_Slave	MSVW03_SRC3	Yes	M-to-S VW Interrupt Event		
	16	eSPI_Slave	MSVW04_SRC0	Yes	M-to-S VW Interrupt Event		
	17	eSPI_Slave	MSVW04_SRC1	Yes	M-to-S VW Interrupt Event		
	18	eSPI_Slave	MSVW04_SRC2	Yes	M-to-S VW Interrupt Event		
	19	eSPI_Slave	MSVW04_SRC3	Yes	M-to-S VW Interrupt Event		
	20	eSPI_Slave	MSVW05_SRC0	Yes	M-to-S VW Interrupt Event		
	21	eSPI_Slave	MSVW05_SRC1	Yes	M-to-S VW Interrupt Event		
	22	eSPI_Slave	MSVW05_SRC2	Yes	M-to-S VW Interrupt Event		
	23	eSPI_Slave	MSVW05_SRC3	Yes	M-to-S VW Interrupt Event		
	24	eSPI_Slave	MSVW06_SRC0	Yes	M-to-S VW Interrupt Event		
	25	eSPI_Slave	MSVW06_SRC1	Yes	M-to-S VW Interrupt Event		
	26	eSPI_Slave	MSVW06_SRC2	Yes	M-to-S VW Interrupt Event		
	27	eSPI_Slave	MSVW06_SRC3	Yes	M-to-S VW Interrupt Event		
	28-31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ25	0	eSPI_Slave	MSVW07_SRC0	Yes	M-to-S VW Interrupt Event	16	N/A
	1	eSPI_Slave	MSVW07_SRC1	Yes	M-to-S VW Interrupt Event		
	2	eSPI_Slave	MSVW07_SRC2	Yes	M-to-S VW Interrupt Event		
	3	eSPI_Slave	MSVW07_SRC3	Yes	M-to-S VW Interrupt Event		
	4	eSPI_Slave	MSVW08_SRC0	Yes	M-to-S VW Interrupt Event		
	5	eSPI_Slave	MSVW08_SRC1	Yes	M-to-S VW Interrupt Event		
	6	eSPI_Slave	MSVW08_SRC2	Yes	M-to-S VW Interrupt Event		
	7	eSPI_Slave	MSVW08_SRC3	Yes	M-to-S VW Interrupt Event		
	8	eSPI_Slave	MSVW09_SRC0	Yes	M-to-S VW Interrupt Event		
	9	eSPI_Slave	MSVW09_SRC1	Yes	M-to-S VW Interrupt Event		
	10	eSPI_Slave	MSVW09_SRC2	Yes	M-to-S VW Interrupt Event		
	11	eSPI_Slave	MSVW09_SRC3	Yes	M-to-S VW Interrupt Event		
	12	eSPI_Slave	MSVW10_SRC0	Yes	M-to-S VW Interrupt Event		
	13	eSPI_Slave	MSVW10_SRC1	Yes	M-to-S VW Interrupt Event		
	14	eSPI_Slave	MSVW10_SRC2	Yes	M-to-S VW Interrupt Event		
	15	eSPI_Slave	MSVW10_SRC3	Yes	M-to-S VW Interrupt Event		
	16-31	Reserved					

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Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ26	0	GPIO240	GPIO Event	Yes	GPIO Interrupt Event	17	N/A
	1	GPIO241	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO242	GPIO Event	Yes	GPIO Interrupt Event		
	3	GPIO243	GPIO Event	Yes	GPIO Interrupt Event		
	4	GPIO244	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO245	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO246	GPIO Event	Yes	GPIO Interrupt Event		
	7	Reserved					
	8	GPIO250	GPIO Event	Yes	GPIO Interrupt Event		
	9	Reserved					
	10	Reserved					
	11	GPIO253	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO254	GPIO Event	Yes	GPIO Interrupt Event		
	13	Reserved					
	14	Reserved					
	15	Reserved					
	16	GPIO260	GPIO Event	Yes	GPIO Interrupt Event		
	17	GPIO261	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO262	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO263	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO264	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO265	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO266	GPIO Event	Yes	GPIO Interrupt Event		
	23	GPIO267	GPIO Event	Yes	GPIO Interrupt Event		
	24	GPIO270	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO271	GPIO Event	Yes	GPIO Interrupt Event		
	26	GPIO272	GPIO Event	Yes	GPIO Interrupt Event		
	27	GPIO273	GPIO Event	Yes	GPIO Interrupt Event		
	28	GPIO274	GPIO Event	Yes	GPIO Interrupt Event		
	29	GPIO275	GPIO Event	Yes	GPIO Interrupt Event		
	30	GPIO276	GPIO Event	Yes	GPIO Interrupt Event		
	31	Reserved					

3.6 GPIO Register Assignments

TABLE 3-1: GPIO MULTIPLEXING

GPIO	MUX_CONTROL= 00b	MUX_CONTROL= 01b	MUX_CONTROL= 10b	MUX_CONTROL = 11b
GPIO000	GPIO000	VCI_IN3#		
GPIO001	GPIO001	PWM4		
GPIO002	GPIO002	PWM5		
GPIO003	GPIO003	I2C00_SDA	SPI0_CS#	
GPIO004	GPIO004	I2C00_SCL	SPI0_MOSI	
GPIO005	GPIO005	I2C01_SDA	GPTP-OUT4	
GPIO006	GPIO006	I2C01_SCL	GPTP-OUT7	
GPIO007	GPIO007	I2C03_SDA	PS2_CLK0B	
GPIO010	GPIO010	I2C03_SCL	PS2_DAT0B	
GPIO011	GPIO011	nSMI		
GPIO012	GPIO012	I2C07_SDA	TOUT3	
GPIO013	GPIO013	I2C07_SCL	TOUT2	
GPIO014	GPIO014	PWM6	GPTP-IN6	
GPIO015	GPIO015	PWM7		
GPIO016	GPIO016	GPTP-IN7	SHD_IO3	ICT3
GPIO017	GPIO017	GPTP-IN5		KSI0
GPIO020	GPIO020			KSI1
GPIO021	GPIO021	LPCPD#		KSI2
GPIO022	GPIO022	GPTP-IN0		
GPIO023	GPIO023	GPTP-IN1		
GPIO024	GPIO024	GPTP-IN2		
GPIO025	GPIO025	TIN0	nEM_INT	UART_CLK
GPIO026	GPIO026	TIN1		KSI3
GPIO027	GPIO027	TIN2		KSI4
GPIO030	GPIO030	TIN3		KSI5
GPIO031	GPIO031	GPTP-OUT1		KSI6
GPIO032	GPIO032	GPTP-OUT0		KSI7
GPIO033	GPIO033	RC_ID0		
GPIO034	GPIO034	RC_ID1	SPI0_CLK	
GPIO035	GPIO035	PWM8	CTOUT1	
GPIO036	GPIO036	RC_ID2	SPI0_MISO	
GPIO040	GPIO040	GPTP-OUT2		KSO0
GPIO041	GPIO041			
GPIO042	GPIO042		PECI_DAT	SB-TSI_DAT
GPIO043	GPIO043			SB-TSI_CLK
GPIO044	GPIO044	VREF_VTT		
GPIO045	GPIO045			KSO1
GPIO046	GPIO046	BCM1_DAT		KSO2
GPIO047	GPIO047	BCM1_CLK		KSO3
GPIO050	GPIO050	FAN_TACH0	GTACH0	

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TABLE 3-1: GPIO MULTIPLEXING (CONTINUED)

GPIO	MUX_CONTROL= 00b	MUX_CONTROL= 01b	MUX_CONTROL= 10b	MUX_CONTROL = 11b
GPIO051	GPIO051	FAN_TACH1	GTACH1	
GPIO052	GPIO052	FAN_TACH2	LRESET#	
GPIO053	GPIO053	PWM0	GPWM0	
GPIO054	GPIO054	PWM1	GPWM1	
GPIO055	GPIO055	PWM2	SHD_CS#	
GPIO056	GPIO056	PWM3	SHD_CLK	
GPIO057	GPIO057	VCC_PWRGD		
GPIO060	GPIO060	KBRST	48MHZ_OUT	
GPIO061	GPIO061	LPCPD#	ESPI_RESET#	
GPIO062	GPIO062			
GPIO063	GPIO063	SER_IRQ	ESPI_ALERT#	
GPIO064	GPIO064	LRESET#		
GPIO065	GPIO065	PCI_CLK	ESPI_CLK	
GPIO066	GPIO066	LFRAME#	ESPI_CS#	
GPIO067	GPIO067	CLKRUN#		
GPIO070	GPIO070	LAD0	ESPI_IO0	
GPIO071	GPIO071	LAD1	ESPI_IO1	
GPIO072	GPIO072	LAD2	ESPI_IO2	
GPIO073	GPIO073	LAD3	ESPI_IO3	
GPIO100	GPIO100	nEC_SCI		
GPIO101	GPIO101			
GPIO102	GPIO102			
GPIO104	GPIO104	UART0_TX		
GPIO105	GPIO105	UART0_RX		
GPIO106	GPIO106	PWROK		
GPIO107	GPIO107	nSMI		KSO4
GPIO110	GPIO110	PS2_CLK2		
GPIO111	GPIO111	PS2_DAT2		
GPIO112	GPIO112	PS2_CLK1A		KSO5
GPIO113	GPIO113	PS2_DAT1A		KSO6
GPIO114	GPIO114	PS2_CLK0A	nEC_SCI	
GPIO115	GPIO115	PS2_DAT0A		
GPIO120	GPIO120			KSO7
GPIO121	GPIO121		PVT_IO0	KSO8
GPIO122	GPIO122	BCM0_DAT	PVT_IO1	KSO9
GPIO123	GPIO123	BCM0_CLK	PVT_IO2	KSO10
GPIO124	GPIO124	GPTP-OUT6	PVT_CS#	KSO11
GPIO125	GPIO125	GPTP-OUT5	PVT_CLK	KSO12
GPIO126	GPIO126		PVT_IO3	KSO13
GPIO127	GPIO127	A20M	UART0_CTS	
GPIO130	GPIO130	I2C10_SDA	TOUT1	
GPIO131	GPIO131	I2C10_SCL	TOUT0	

TABLE 3-1: GPIO MULTIPLEXING (CONTINUED)

GPIO	MUX_CONTROL= 00b	MUX_CONTROL= 01b	MUX_CONTROL= 10b	MUX_CONTROL = 11b
GPIO132	GPIO132	I2C06_SDA		KSO14
GPIO133	GPIO133	PWM9		
GPIO134	GPIO134	PWM10	UART1_RTS	
GPIO135	GPIO135		UART1_CTS	
GPIO140	GPIO140	I2C06_SCL	ICT5	
GPIO141	GPIO141	I2C05_SDA	SPI1_CLK	UART0_DCD#
GPIO142	GPIO142	I2C05_SCL	SPI1_MOSI	UART0_DSR#
GPIO143	GPIO143	I2C04_SDA	SPI1_MSIO	UART0_DTR#
GPIO144	GPIO144	I2C04_SCL	SPI1_CS#	UART0_RI#
GPIO145	GPIO145	I2C09_SDA		
GPIO146	GPIO146	I2C09_SCL		
GPIO147	GPIO147	I2C08_SDA		
GPIO150	GPIO150	I2C08_SCL		
GPIO151	GPIO151	ICT4		KSO15
GPIO152	GPIO152	GPTP-OUT3		KSO16
GPIO153	GPIO153	LED2		
GPIO154	GPIO154	I2C02_SDA	PS2_CLK1B	
GPIO155	GPIO155	I2C02_SCL	PS2_DAT1B	
GPIO156	GPIO156	LED0		
GPIO157	GPIO157	LED1		
GPIO160	GPIO160			
GPIO161	GPIO161	VCI_IN2#		
GPIO162	GPIO162	VCI_IN1#		
GPIO163	GPIO163	VCI_IN0#		
GPIO165	GPIO165	32KHZ_IN	CTOUT0	
GPIO166	GPIO166			
GPIO170	GPIO170	TFCLK	UART1_TX	
GPIO171	GPIO171	TFDATA	UART1_RX	
GPIO172	GPIO172			
GPIO173	GPIO173			
GPIO174	GPIO174			
GPIO175	GPIO175			KSO17
GPIO200	GPIO200	ADC00		
GPIO201	GPIO201	ADC01		
GPIO202	GPIO202	ADC02		
GPIO203	GPIO203	ADC03		
GPIO204	GPIO204	ADC04		
GPIO205	GPIO205	ADC05		
GPIO206	GPIO206	ADC06		
GPIO207	GPIO207	ADC07		
GPIO210	GPIO210	ADC08		
GPIO211	GPIO211	ADC09		

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TABLE 3-1: GPIO MULTIPLEXING (CONTINUED)

GPIO	MUX_CONTROL= 00b	MUX_CONTROL= 01b	MUX_CONTROL= 10b	MUX_CONTROL = 11b
GPIO212	GPIO212	ADC10		
GPIO213	GPIO213	ADC11		
GPIO214	GPIO214	ADC12		
GPIO215	GPIO215	ADC13		
GPIO216	GPIO216	ADC14		
GPIO217	GPIO217	ADC15		
GPIO221	GPIO221	GPTP-IN3	32KHZ_OUT	
GPIO222	GPIO222	SER_IRQ		
GPIO223	GPIO223		SHD_IO0	
GPIO224	GPIO224	GPTP-IN4	SHD_IO1	
GPIO225	GPIO225	UART0_RTS		
GPIO226	GPIO226	LED3		
GPIO227	GPIO227		SHD_IO2	
GPIO230	GPIO230			
GPIO231	GPIO231			
GPIO233	GPIO233			
GPIO234	GPIO234	VCI_IN4#		
GPIO240	GPIO240			
GPIO241	GPIO241			
GPIO242	GPIO242			
GPIO243	GPIO243			
GPIO244	GPIO244			
GPIO245	GPIO245			
GPIO246	GPIO246			
GPIO250	GPIO250			
GPIO253	GPIO253			
GPIO254	GPIO254			

TABLE 3-2: GPIO PIN CONTROL REGISTERS DEFAULTS

GPIO Name	Pin Control Register Offset (Hex)	Pin Control Register Default Value (Hex)	Pin Control Register Default Function	Pin Control 2 Register Offset (Hex)	Pin Control 2 Register Default Value (Hex)
GPIO000	0000	00001040	VCI_IN3#	500	000
GPIO001	0004	00000040	GPIO001	504	000
GPIO002	0008	00000040	GPIO002	508	000
GPIO003	000C	00000040	GPIO003	50C	000
GPIO004	0010	00000040	GPIO004	510	000
GPIO005	0014	00000040	GPIO005	514	000
GPIO006	0018	00000040	GPIO006	518	000
GPIO007	001C	00000040	GPIO007	51C	000
GPIO010	0020	00000040	GPIO010	520	000
GPIO011	0024	00000040	GPIO011	524	000

TABLE 3-2: GPIO PIN CONTROL REGISTERS DEFAULTS (CONTINUED)

GPIO Name	Pin Control Register Offset (Hex)	Pin Control Register Default Value (Hex)	Pin Control Register Default Function	Pin Control 2 Register Offset (Hex)	Pin Control 2 Register Default Value (Hex)
GPIO012	0028	00000040	GPIO012	528	000
GPIO013	002C	00000040	GPIO013	52C	000
GPIO014	0030	00000040	GPIO014	530	000
GPIO015	0034	00000040	GPIO015	534	000
GPIO016	0038	00000040	GPIO016	538	000
GPIO017	003C	00000040	GPIO017	53C	000
GPIO020	0040	00000040	GPIO020	540	000
GPIO021	0044	00000040	GPIO021	544	000
GPIO022	0048	00000040	GPIO022	548	000
GPIO023	004C	00000040	GPIO023	54C	000
GPIO024	0050	00000040	GPIO024	550	000
GPIO025	0054	00000040	GPIO025	554	000
GPIO026	0058	00000040	GPIO026	558	000
GPIO027	005C	00000040	GPIO027	55C	000
GPIO030	0060	00000040	GPIO030	560	000
GPIO031	0064	00000040	GPIO031	564	000
GPIO032	0068	00000040	GPIO032	568	000
GPIO033	006C	00000040	GPIO033	56C	000
GPIO034	0070	00000040	GPIO034	570	000
GPIO035	0074	00000040	GPIO035	574	000
GPIO036	0078	00000040	GPIO036	578	000
GPIO040	0080	00000040	GPIO040	580	000
GPIO041	0084	00000040	GPIO041	584	000
GPIO042	0088	00000040	GPIO042	588	000
GPIO043	008C	00000040	GPIO043	58C	000
GPIO044	0090	00000040	GPIO044	590	000
GPIO045	0094	00000040	GPIO045	594	000
GPIO046	0098	00000040	GPIO046	598	000
GPIO047	009C	00000040	GPIO047	59C	000
GPIO050	00A0	00000040	GPIO050	5A0	000
GPIO051	00A4	00000040	GPIO051	5A4	000
GPIO052	00A8	00000040	GPIO052	5A8	000
GPIO053	00AC	00000040	GPIO053	5AC	000
GPIO054	00B0	00000040	GPIO054	5B0	000
GPIO055	00B4	00000040	GPIO055	5B4	000
GPIO056	00B8	00000040	GPIO056	5B8	000
(GPIO057)	00BC	00001040	VCC_PWRGD	5BC	000
GPIO060	00C0	00000040	GPIO060	5C0	000
GPIO061	00C4	00000040	GPIO061	5C4	000
GPIO062	00C8	00000240	GPIO062	5C8	000
GPIO063	00CC	00000040	GPIO063	5CC	000
GPIO064	00D0	00001000	LRESET#	5D0	000

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TABLE 3-2: GPIO PIN CONTROL REGISTERS DEFAULTS (CONTINUED)

GPIO Name	Pin Control Register Offset (Hex)	Pin Control Register Default Value (Hex)	Pin Control Register Default Function	Pin Control 2 Register Offset (Hex)	Pin Control 2 Register Default Value (Hex)
GPIO065	00D4	00000040	GPIO065	5D4	000
GPIO066	00D8	00000040	GPIO066	5D8	000
GPIO067	00DC	00000040	GPIO067	5DC	000
GPIO070	00E0	00000040	GPIO070	5E0	000
GPIO071	00E4	00000040	GPIO071	5E4	000
GPIO072	00E8	00000040	GPIO072	5E8	000
GPIO073	00EC	00000040	GPIO073	5EC	000
GPIO100	0100	00000040	GPIO100	600	000
GPIO101	0104	00000040	GPIO101	604	000
GPIO102	0108	00000040	GPIO102	608	000
GPIO104	0110	00000040	GPIO104	610	000
GPIO105	0114	00000040	GPIO105	614	000
GPIO106	0118	00000040	GPIO106	618	000
GPIO107	011C	00000040	GPIO107	61C	000
GPIO110	0120	00000040	GPIO110	620	000
GPIO111	0124	00000040	GPIO111	624	000
GPIO112	0128	00000040	GPIO112	628	000
GPIO113	012C	00000040	GPIO113	62C	000
GPIO114	0130	00000040	GPIO114	630	000
GPIO115	0134	00000040	GPIO115	634	000
GPIO120	0140	00000040	GPIO120	640	000
GPIO121	0144	00000040	GPIO121	644	000
GPIO122	0148	00000040	GPIO122	648	000
GPIO123	014C	00000040	GPIO123	64C	000
GPIO124	0150	00000040	GPIO124	650	000
GPIO125	0154	00000040	GPIO125	654	000
GPIO126	0158	00000040	GPIO126	658	000
GPIO127	015C	00000040	GPIO127	65C	000
GPIO130	0160	00000040	GPIO130	660	000
GPIO131	0164	00000040	GPIO131	664	000
GPIO132	0168	00000040	GPIO132	668	000
GPIO133	016C	00000040	GPIO133	66C	000
GPIO134	0170	00000040	GPIO134	670	000
GPIO135	0174	00000040	GPIO135	674	000
GPIO140	0180	00000040	GPIO140	680	000
GPIO141	0184	00000040	GPIO141	684	000
GPIO142	0188	00000040	GPIO142	688	000
GPIO143	018C	00000040	GPIO143	68C	000
GPIO144	0190	00000040	GPIO144	690	000
GPIO145	0194	00000040	GPIO145	694	000
GPIO146	0198	00000040	GPIO146	698	000
GPIO147	019C	00000040	GPIO147	69C	000

TABLE 3-2: GPIO PIN CONTROL REGISTERS DEFAULTS (CONTINUED)

GPIO Name	Pin Control Register Offset (Hex)	Pin Control Register Default Value (Hex)	Pin Control Register Default Function	Pin Control 2 Register Offset (Hex)	Pin Control 2 Register Default Value (Hex)
GPIO150	01A0	00000040	GPIO150	6A0	000
GPIO151	01A4	00000040	GPIO151	6A4	000
GPIO152	01A8	00000040	GPIO152	6A8	000
GPIO153	01AC	00000040	GPIO153	6AC	000
GPIO154	01B0	00000040	GPIO154	6B0	000
GPIO155	01B4	00000040	GPIO155	6B4	000
GPIO156	01B8	00000040	GPIO156	6B8	000
GPIO157	01BC	00000040	GPIO157	6BC	000
GPIO160	01C0	00000040	GPIO160	6C0	000
GPIO161	01C4	00001040	VCI_IN2#	6C4	000
GPIO162	01C8	00001040	VCI_IN1#	6C8	000
GPIO163	01CC	00001040	VCI_IN0#	6CC	000
GPIO165	01D4	00000040	GPIO165	6D4	000
GPIO166	01D8	00000040	GPIO166	6D8	000
GPIO170	01E0	00000040	GPIO170	6E0	000
GPIO171	01E4	00000041	GPIO171	6E4	000
GPIO172	01E8	00000040	GPIO172	6E8	000
GPIO173	01EC	00000040	GPIO173	6EC	000
GPIO174	01F0	00000040	GPIO174	6F0	000
GPIO175	01F4	00000040	GPIO175	6F4	000
GPIO200	0200	00001040	ADC00	700	000
GPIO201	0204	00001040	ADC01	704	000
GPIO202	0208	00001040	ADC02	708	000
GPIO203	020C	00001040	ADC03	70C	000
GPIO204	0210	00001040	ADC04	710	000
GPIO205	0214	00001040	ADC05	714	000
GPIO206	0218	00001040	ADC06	718	000
GPIO207	021C	00001040	ADC07	71C	000
GPIO210	0220	00001040	ADC08	720	000
GPIO211	0224	00001040	ADC09	724	000
GPIO212	0228	00001040	ADC10	728	000
GPIO213	022C	00001040	ADC11	72C	000
GPIO214	0230	00001040	ADC12	730	000
GPIO215	0234	00001040	ADC13	734	000
GPIO216	0238	00001040	ADC14	738	000
GPIO217	023C	00001040	ADC15	73C	000
GPIO221	0244	00000040	GPIO221	744	000
GPIO222	0248	00000040	GPIO222	748	000
GPIO223	024C	00000040	GPIO223	74C	000
GPIO224	0250	00000040	GPIO224	750	000
GPIO225	0254	00000040	GPIO225	754	000
GPIO226	0258	00000040	GPIO226	758	000

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TABLE 3-2: GPIO PIN CONTROL REGISTERS DEFAULTS (CONTINUED)

GPIO Name	Pin Control Register Offset (Hex)	Pin Control Register Default Value (Hex)	Pin Control Register Default Function	Pin Control 2 Register Offset (Hex)	Pin Control 2 Register Default Value (Hex)
GPIO227	025C	00000040	GPIO227	75C	000
GPIO230	0260	00000040	GPIO230	760	000
GPIO231	0264	00000040	GPIO231	764	000
GPIO233	026C	00000040	GPIO233	76C	000
GPIO234	0270	00000040	VCI_IN4#	770	000
GPIO240	0280	00000040	GPIO140	780	000
GPIO241	0284	00000040	GPIO241	784	000
GPIO242	0288	00000040	GPIO242	788	000
GPIO243	028C	00000040	GPIO243	78C	000
GPIO244	0290	00000040	GPIO244	790	000
GPIO245	0294	00000040	GPIO245	794	000
GPIO246	0298	00000040	GPIO246	798	000
GPIO250	02A0	00000040	GPIO250	7A0	000
GPIO253	02AC	00000040	GPIO253	7AC	000
GPIO254	02B0	00000040	GPIO254	7B0	000

TABLE 3-3: GPIO INPUT AND OUTPUT REGISTERS

Offset	Register Name
300h	Input GPIO[036:000] Register
304h	Input GPIO[076:040] Register
308h	Input GPIO[136:100] Register
30Ch	Input GPIO[176:140] Register
310h	Input GPIO[236:200] Register
314h	Input GPIO[276:240] Register
380h	Output GPIO[036:000] Register
384h	Output GPIO[076:040] Register
388h	Output GPIO[136:100] Register
38Ch	Output GPIO[176:140] Register
390h	Output GPIO[236:200] Register
394h	Output GPIO[276:240] Register

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3.7 Register Map

Block	Instance	Register	Register Address
Watchdog Timer	0	WDT Load Register	40000000h
Watchdog Timer	0	WDT Control Register	40000004h
Watchdog Timer	0	WDT Kick Register	40000008h
Watchdog Timer	0	WDT Count Register	4000000Ch
16-bit Basic Timer	0	Timer Count Register	40000C00h
16-bit Basic Timer	0	Timer Preload Register	40000C04h
16-bit Basic Timer	0	Timer Status Register	40000C08h
16-bit Basic Timer	0	Timer Int Enable Register	40000C0Ch
16-bit Basic Timer	0	Timer Control Register	40000C10h
16-bit Basic Timer	1	Timer Count Register	40000C20h
16-bit Basic Timer	1	Timer Preload Register	40000C24h
16-bit Basic Timer	1	Timer Status Register	40000C28h
16-bit Basic Timer	1	Timer Int Enable Register	40000C2Ch
16-bit Basic Timer	1	Timer Control Register	40000C30h
16-bit Basic Timer	2	Timer Count Register	40000C40h
16-bit Basic Timer	2	Timer Preload Register	40000C44h
16-bit Basic Timer	2	Timer Status Register	40000C48h
16-bit Basic Timer	2	Timer Int Enable Register	40000C4Ch
16-bit Basic Timer	2	Timer Control Register	40000C50h
16-bit Basic Timer	3	Timer Count Register	40000C60h
16-bit Basic Timer	3	Timer Preload Register	40000C64h
16-bit Basic Timer	3	Timer Status Register	40000C68h
16-bit Basic Timer	3	Timer Int Enable Register	40000C6Ch
16-bit Basic Timer	3	Timer Control Register	40000C70h
32-bit Basic Timer	0	Timer Count Register	40000C80h
32-bit Basic Timer	0	Timer Preload Register	40000C84h
32-bit Basic Timer	0	Timer Status Register	40000C88h
32-bit Basic Timer	0	Timer Int Enable Register	40000C8Ch
32-bit Basic Timer	0	Timer Control Register	40000C90h
32-bit Basic Timer	1	Timer Count Register	40000CA0h
32-bit Basic Timer	1	Timer Preload Register	40000CA4h
32-bit Basic Timer	1	Timer Status Register	40000CA8h
32-bit Basic Timer	1	Timer Int Enable Register	40000CACh
32-bit Basic Timer	1	Timer Control Register	40000CB0h
16-bit Counter Timer	0	Timer x Control Register	40000D00h
16-bit Counter Timer	0	Timer x Clock and Event Control Register	40000D04h
16-bit Counter Timer	0	Timer x Reload Register	40000D08h
16-bit Counter Timer	0	Timer x Count Register	40000D0Ch
16-bit Counter Timer	1	Timer x Control Register	40000D20h
16-bit Counter Timer	1	Timer x Clock and Event Control Register	40000D24h
16-bit Counter Timer	1	Timer x Reload Register	40000D28h

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Block	Instance	Register	Register Address
16-bit Counter Timer	1	Timer x Count Register	40000D2Ch
16-bit Counter Timer	2	Timer x Control Register	40000D40h
16-bit Counter Timer	2	Timer x Clock and Event Control Register	40000D44h
16-bit Counter Timer	2	Timer x Reload Register	40000D48h
16-bit Counter Timer	2	Timer x Count Register	40000D4Ch
16-bit Counter Timer	3	Timer x Control Register	40000D60h
16-bit Counter Timer	3	Timer x Clock and Event Control Register	40000D64h
16-bit Counter Timer	3	Timer x Reload Register	40000D68h
16-bit Counter Timer	3	Timer x Count Register	40000D6Ch
Capture Compare Timer	0	Capture and Compare Timer Control Register	40001000h
Capture Compare Timer	0	Capture Control 0 Register	40001004h
Capture Compare Timer	0	Capture Control 1 Register	40001008h
Capture Compare Timer	0	Free Running Timer Register	4000100Ch
Capture Compare Timer	0	Capture 0 Register	40001010h
Capture Compare Timer	0	Capture 1 Register	40001014h
Capture Compare Timer	0	Capture 2 Register	40001018h
Capture Compare Timer	0	Capture 3 Register	4000101Ch
Capture Compare Timer	0	Capture 4 Register	40001020h
Capture Compare Timer	0	Capture 5 Register	40001024h
Capture Compare Timer	0	Compare 0 Register	40001028h
Capture Compare Timer	0	Compare 1 Register	4000102Ch
RC-ID	0	RC_ID Control Register	40001400h
RC-ID	0	RC_ID Data Register	40001404h
RC-ID	1	RC_ID Control Register	40001480h
RC-ID	1	RC_ID Data Register	40001484h
RC-ID	2	RC_ID Control Register	40001500h
RC-ID	2	RC_ID Data Register	40001504h
DMA Controller	0	DMA Main Control Register	40002400h
DMA Controller	0	DMA Data Packet Register	40002404h
DMA Controller	0	TEST	40002408h
DMA Channel	0	DMA Channel N Activate Register	40002440h
DMA Channel	0	DMA Channel N Memory Start Address Register	40002444h
DMA Channel	0	DMA Channel N Memory End Address Register	40002448h
DMA Channel	0	DMA Channel N Device Address	4000244Ch
DMA Channel	0	DMA Channel N Control Register	40002450h
DMA Channel	0	DMA Channel N Interrupt Status Register	40002454h
DMA Channel	0	DMA Channel N Interrupt Enable Register	40002458h
DMA Channel	0	TEST	4000245Ch
DMA Channel	0	Channel N CRC Enable Register	40002460h
DMA Channel	0	Channel N CRC Data Register	40002464h
DMA Channel	0	Channel N CRC Post Status Register	40002468h
DMA Channel	0	TEST	4000246Ch
DMA Channel	1	DMA Channel N Activate Register	40002480h

Block	Instance	Register	Register Address
DMA Channel	1	DMA Channel N Memory Start Address Register	40002484h
DMA Channel	1	DMA Channel N Memory End Address Register	40002488h
DMA Channel	1	DMA Channel N Device Address	4000248Ch
DMA Channel	1	DMA Channel N Control Register	40002490h
DMA Channel	1	DMA Channel N Interrupt Status Register	40002494h
DMA Channel	1	DMA Channel N Interrupt Enable Register	40002498h
DMA Channel	1	TEST	4000249Ch
DMA Channel	1	Channel N Fill Enable Register	400024A0h
DMA Channel	1	Channel N Fill Data Register	400024A4h
DMA Channel	1	Channel N Fill Status Register	400024A8h
DMA Channel	1	TEST	400024ACh
DMA Channel	2	DMA Channel N Activate Register	400024C0h
DMA Channel	2	DMA Channel N Memory Start Address Register	400024C4h
DMA Channel	2	DMA Channel N Memory End Address Register	400024C8h
DMA Channel	2	DMA Channel N Device Address	400024CCh
DMA Channel	2	DMA Channel N Control Register	400024D0h
DMA Channel	2	DMA Channel N Interrupt Status Register	400024D4h
DMA Channel	2	DMA Channel N Interrupt Enable Register	400024D8h
DMA Channel	2	TEST	400024DCh
DMA Channel	3	DMA Channel N Activate Register	40002500h
DMA Channel	3	DMA Channel N Memory Start Address Register	40002504h
DMA Channel	3	DMA Channel N Memory End Address Register	40002508h
DMA Channel	3	DMA Channel N Device Address	4000250Ch
DMA Channel	3	DMA Channel N Control Register	40002510h
DMA Channel	3	DMA Channel N Interrupt Status Register	40002514h
DMA Channel	3	DMA Channel N Interrupt Enable Register	40002518h
DMA Channel	3	TEST	4000251Ch
DMA Channel	4	DMA Channel N Activate Register	40002540h
DMA Channel	4	DMA Channel N Memory Start Address Register	40002544h
DMA Channel	4	DMA Channel N Memory End Address Register	40002548h
DMA Channel	4	DMA Channel N Device Address	4000254Ch
DMA Channel	4	DMA Channel N Control Register	40002550h
DMA Channel	4	DMA Channel N Interrupt Status Register	40002554h
DMA Channel	4	DMA Channel N Interrupt Enable Register	40002558h
DMA Channel	4	TEST	4000255Ch
DMA Channel	5	DMA Channel N Activate Register	40002580h
DMA Channel	5	DMA Channel N Memory Start Address Register	40002584h
DMA Channel	5	DMA Channel N Memory End Address Register	40002588h
DMA Channel	5	DMA Channel N Device Address	4000258Ch
DMA Channel	5	DMA Channel N Control Register	40002590h
DMA Channel	5	DMA Channel N Interrupt Status Register	40002594h
DMA Channel	5	DMA Channel N Interrupt Enable Register	40002598h
DMA Channel	5	TEST	4000259Ch

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Block	Instance	Register	Register Address
DMA Channel	6	DMA Channel N Activate Register	400025C0h
DMA Channel	6	DMA Channel N Memory Start Address Register	400025C4h
DMA Channel	6	DMA Channel N Memory End Address Register	400025C8h
DMA Channel	6	DMA Channel N Device Address	400025CCh
DMA Channel	6	DMA Channel N Control Register	400025D0h
DMA Channel	6	DMA Channel N Interrupt Status Register	400025D4h
DMA Channel	6	DMA Channel N Interrupt Enable Register	400025D8h
DMA Channel	6	TEST	400025DCh
DMA Channel	7	DMA Channel N Activate Register	40002600h
DMA Channel	7	DMA Channel N Memory Start Address Register	40002604h
DMA Channel	7	DMA Channel N Memory End Address Register	40002608h
DMA Channel	7	DMA Channel N Device Address	4000260Ch
DMA Channel	7	DMA Channel N Control Register	40002610h
DMA Channel	7	DMA Channel N Interrupt Status Register	40002614h
DMA Channel	7	DMA Channel N Interrupt Enable Register	40002618h
DMA Channel	7	TEST	4000261Ch
DMA Channel	8	DMA Channel N Activate Register	40002640h
DMA Channel	8	DMA Channel N Memory Start Address Register	40002644h
DMA Channel	8	DMA Channel N Memory End Address Register	40002648h
DMA Channel	8	DMA Channel N Device Address	4000264Ch
DMA Channel	8	DMA Channel N Control Register	40002650h
DMA Channel	8	DMA Channel N Interrupt Status Register	40002654h
DMA Channel	8	DMA Channel N Interrupt Enable Register	40002658h
DMA Channel	8	TEST	4000265Ch
DMA Channel	9	DMA Channel N Activate Register	40002680h
DMA Channel	9	DMA Channel N Memory Start Address Register	40002684h
DMA Channel	9	DMA Channel N Memory End Address Register	40002688h
DMA Channel	9	DMA Channel N Device Address	4000268Ch
DMA Channel	9	DMA Channel N Control Register	40002690h
DMA Channel	9	DMA Channel N Interrupt Status Register	40002694h
DMA Channel	9	DMA Channel N Interrupt Enable Register	40002698h
DMA Channel	9	TEST	4000269Ch
DMA Channel	10	DMA Channel N Activate Register	400026C0h
DMA Channel	10	DMA Channel N Memory Start Address Register	400026C4h
DMA Channel	10	DMA Channel N Memory End Address Register	400026C8h
DMA Channel	10	DMA Channel N Device Address	400026CCh
DMA Channel	10	DMA Channel N Control Register	400026D0h
DMA Channel	10	DMA Channel N Interrupt Status Register	400026D4h
DMA Channel	10	DMA Channel N Interrupt Enable Register	400026D8h
DMA Channel	10	TEST	400026DCh
DMA Channel	11	DMA Channel N Activate Register	40002700h
DMA Channel	11	DMA Channel N Memory Start Address Register	40002704h
DMA Channel	11	DMA Channel N Memory End Address Register	40002708h

Block	Instance	Register	Register Address
DMA Channel	11	DMA Channel N Device Address	4000270Ch
DMA Channel	11	DMA Channel N Control Register	40002710h
DMA Channel	11	DMA Channel N Interrupt Status Register	40002714h
DMA Channel	11	DMA Channel N Interrupt Enable Register	40002718h
DMA Channel	11	TEST	4000271Ch
DMA Channel	12	DMA Channel N Activate Register	40002740h
DMA Channel	12	DMA Channel N Memory Start Address Register	40002744h
DMA Channel	12	DMA Channel N Memory End Address Register	40002748h
DMA Channel	12	DMA Channel N Device Address	4000274Ch
DMA Channel	12	DMA Channel N Control Register	40002750h
DMA Channel	12	DMA Channel N Interrupt Status Register	40002754h
DMA Channel	12	DMA Channel N Interrupt Enable Register	40002758h
DMA Channel	12	TEST	4000275Ch
DMA Channel	13	DMA Channel N Activate Register	40002780h
DMA Channel	13	DMA Channel N Memory Start Address Register	40002784h
DMA Channel	13	DMA Channel N Memory End Address Register	40002788h
DMA Channel	13	DMA Channel N Device Address	4000278Ch
DMA Channel	13	DMA Channel N Control Register	40002790h
DMA Channel	13	DMA Channel N Interrupt Status Register	40002794h
DMA Channel	13	DMA Channel N Interrupt Enable Register	40002798h
DMA Channel	13	TEST	4000279Ch
EEPROM Controller	0	EEPROM Mode Register	40002C00h
EEPROM Controller	0	EEPROM Execute Register	40002C04h
EEPROM Controller	0	EEPROM Status Register	40002C08h
EEPROM Controller	0	EEPROM Interrupt Enable Register	40002C0Ch
EEPROM Controller	0	EEPROM Password Register	40002C10h
EEPROM Controller	0	EEPROM Unlock Register	40002C14h
EEPROM Controller	0	EEPROM lock Register	40002C18h
EEPROM Controller	0	TEST	40002C1Ch
EEPROM Controller	0	EEPROM Buffer Register	40002C20h
SMB-I2C	0	Control Register	40004000h
SMB-I2C	0	Status Register	40004000h
SMB-I2C	0	Own Address Register	40004004h
SMB-I2C	0	Data Register	40004008h
SMB-I2C	0	Master Command Register	4000400Ch
SMB-I2C	0	Slave Command Register	40004010h
SMB-I2C	0	PEC Register	40004014h
SMB-I2C	0	Repeated START Hold Time Register	40004018h
SMB-I2C	0	Completion Register	40004020h
SMB-I2C	0	Idle Scaling Register	40004024h
SMB-I2C	0	Configuration Register	40004028h
SMB-I2C	0	Bus Clock Register	4000402Ch
SMB-I2C	0	Block ID Register	40004030h

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Block	Instance	Register	Register Address
SMB-I2C	0	Revision Register	40004034h
SMB-I2C	0	Bit-Bang Control Register	40004038h
SMB-I2C	0	TEST	4000403Ch
SMB-I2C	0	Data Timing Register	40004040h
SMB-I2C	0	Time-Out Scaling Register	40004044h
SMB-I2C	0	Slave Transmit Buffer Register	40004048h
SMB-I2C	0	Slave Receive Buffer Register	4000404Ch
SMB-I2C	0	Master Transmit Buffer Register	40004050h
SMB-I2C	0	Master Receive Buffer Register	40004054h
SMB-I2C	0	TEST	40004058h
SMB-I2C	0	TEST	4000405Ch
SMB-I2C	0	Wake Status Register	40004060h
SMB-I2C	0	Wake Enable Register	40004064h
SMB-I2C	0	TEST	40004068h
SMB-I2C	1	Control Register	40004400h
SMB-I2C	1	Status Register	40004400h
SMB-I2C	1	Own Address Register	40004404h
SMB-I2C	1	Data Register	40004408h
SMB-I2C	1	Master Command Register	4000440Ch
SMB-I2C	1	Slave Command Register	40004410h
SMB-I2C	1	PEC Register	40004414h
SMB-I2C	1	Repeated START Hold Time Register	40004418h
SMB-I2C	1	Completion Register	40004420h
SMB-I2C	1	Idle Scaling Register	40004424h
SMB-I2C	1	Configuration Register	40004428h
SMB-I2C	1	Bus Clock Register	4000442Ch
SMB-I2C	1	Block ID Register	40004430h
SMB-I2C	1	Revision Register	40004434h
SMB-I2C	1	Bit-Bang Control Register	40004438h
SMB-I2C	1	TEST	4000443Ch
SMB-I2C	1	Data Timing Register	40004440h
SMB-I2C	1	Time-Out Scaling Register	40004444h
SMB-I2C	1	Slave Transmit Buffer Register	40004448h
SMB-I2C	1	Slave Receive Buffer Register	4000444Ch
SMB-I2C	1	Master Transmit Buffer Register	40004450h
SMB-I2C	1	Master Receive Buffer Register	40004454h
SMB-I2C	1	TEST	40004458h
SMB-I2C	1	TEST	4000445Ch
SMB-I2C	1	Wake Status Register	40004460h
SMB-I2C	1	Wake Enable Register	40004464h
SMB-I2C	1	TEST	40004468h
SMB-I2C	2	Control Register	40004800h
SMB-I2C	2	Status Register	40004800h

Block	Instance	Register	Register Address
SMB-I2C	2	Own Address Register	40004804h
SMB-I2C	2	Data Register	40004808h
SMB-I2C	2	Master Command Register	4000480Ch
SMB-I2C	2	Slave Command Register	40004810h
SMB-I2C	2	PEC Register	40004814h
SMB-I2C	2	Repeated START Hold Time Register	40004818h
SMB-I2C	2	Completion Register	40004820h
SMB-I2C	2	Idle Scaling Register	40004824h
SMB-I2C	2	Configuration Register	40004828h
SMB-I2C	2	Bus Clock Register	4000482Ch
SMB-I2C	2	Block ID Register	40004830h
SMB-I2C	2	Revision Register	40004834h
SMB-I2C	2	Bit-Bang Control Register	40004838h
SMB-I2C	2	TEST	4000483Ch
SMB-I2C	2	Data Timing Register	40004840h
SMB-I2C	2	Time-Out Scaling Register	40004844h
SMB-I2C	2	Slave Transmit Buffer Register	40004848h
SMB-I2C	2	Slave Receive Buffer Register	4000484Ch
SMB-I2C	2	Master Transmit Buffer Register	40004850h
SMB-I2C	2	Master Receive Buffer Register	40004854h
SMB-I2C	2	TEST	40004858h
SMB-I2C	2	TEST	4000485Ch
SMB-I2C	2	Wake Status Register	40004860h
SMB-I2C	2	Wake Enable Register	40004864h
SMB-I2C	2	TEST	40004868h
SMB-I2C	3	Control Register	40004C00h
SMB-I2C	3	Status Register	40004C00h
SMB-I2C	3	Own Address Register	40004C04h
SMB-I2C	3	Data Register	40004C08h
SMB-I2C	3	Master Command Register	40004C0Ch
SMB-I2C	3	Slave Command Register	40004C10h
SMB-I2C	3	PEC Register	40004C14h
SMB-I2C	3	Repeated START Hold Time Register	40004C18h
SMB-I2C	3	Completion Register	40004C20h
SMB-I2C	3	Idle Scaling Register	40004C24h
SMB-I2C	3	Configuration Register	40004C28h
SMB-I2C	3	Bus Clock Register	40004C2Ch
SMB-I2C	3	Block ID Register	40004C30h
SMB-I2C	3	Revision Register	40004C34h
SMB-I2C	3	Bit-Bang Control Register	40004C38h
SMB-I2C	3	TEST	40004C3Ch
SMB-I2C	3	Data Timing Register	40004C40h
SMB-I2C	3	Time-Out Scaling Register	40004C44h

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Block	Instance	Register	Register Address
SMB-I2C	3	Slave Transmit Buffer Register	40004C48h
SMB-I2C	3	Slave Receive Buffer Register	40004C4Ch
SMB-I2C	3	Master Transmit Buffer Register	40004C50h
SMB-I2C	3	Master Receive Buffer Register	40004C54h
SMB-I2C	3	TEST	40004C58h
SMB-I2C	3	TEST	40004C5Ch
SMB-I2C	3	Wake Status Register	40004C60h
SMB-I2C	3	Wake Enable Register	40004C64h
SMB-I2C	3	TEST	40004C68h
QMSPI	0	QMSPI Mode Register	40005400h
QMSPI	0	QMSPI Control Register	40005404h
QMSPI	0	QMSPI Execute Register	40005408h
QMSPI	0	QMSPI Interface Control Register	4000540Ch
QMSPI	0	QMSPI Status Register	40005410h
QMSPI	0	QMSPI Buffer Count Status Register	40005414h
QMSPI	0	QMSPI Interrupt Enable Register	40005418h
QMSPI	0	QMSPI Buffer Count Trigger Register	4000541Ch
QMSPI	0	QMSPI Transmit Buffer Register	40005420h
QMSPI	0	QMSPI Receive Buffer Register	40005424h
QMSPI	0	QMSPI Description Buffer 0 Register	40005430h
QMSPI	0	QMSPI Description Buffer 1 Register	40005434h
QMSPI	0	QMSPI Description Buffer 2 Register	40005438h
QMSPI	0	QMSPI Description Buffer 3 Register	4000543Ch
QMSPI	0	QMSPI Description Buffer 4 Register	40005440h
16-bit PWM	0	PWMx Counter ON Time Register	40005800h
16-bit PWM	0	PWMx Counter OFF Time Register	40005804h
16-bit PWM	0	PWMx Configuration Register	40005808h
16-bit PWM	0	TEST	4000580Ch
16-bit PWM	1	PWMx Counter ON Time Register	40005810h
16-bit PWM	1	PWMx Counter OFF Time Register	40005814h
16-bit PWM	1	PWMx Configuration Register	40005818h
16-bit PWM	1	TEST	4000581Ch
16-bit PWM	2	PWMx Counter ON Time Register	40005820h
16-bit PWM	2	PWMx Counter OFF Time Register	40005824h
16-bit PWM	2	PWMx Configuration Register	40005828h
16-bit PWM	2	TEST	4000582Ch
16-bit PWM	3	PWMx Counter ON Time Register	40005830h
16-bit PWM	3	PWMx Counter OFF Time Register	40005834h
16-bit PWM	3	PWMx Configuration Register	40005838h
16-bit PWM	3	TEST	4000583Ch
16-bit PWM	4	PWMx Counter ON Time Register	40005840h
16-bit PWM	4	PWMx Counter OFF Time Register	40005844h
16-bit PWM	4	PWMx Configuration Register	40005848h

Block	Instance	Register	Register Address
16-bit PWM	4	TEST	4000584Ch
16-bit PWM	5	PWMx Counter ON Time Register	40005850h
16-bit PWM	5	PWMx Counter OFF Time Register	40005854h
16-bit PWM	5	PWMx Configuration Register	40005858h
16-bit PWM	5	TEST	4000585Ch
16-bit PWM	6	PWMx Counter ON Time Register	40005860h
16-bit PWM	6	PWMx Counter OFF Time Register	40005864h
16-bit PWM	6	PWMx Configuration Register	40005868h
16-bit PWM	6	TEST	4000586Ch
16-bit PWM	7	PWMx Counter ON Time Register	40005870h
16-bit PWM	7	PWMx Counter OFF Time Register	40005874h
16-bit PWM	7	PWMx Configuration Register	40005878h
16-bit PWM	7	TEST	4000587Ch
16-bit PWM	8	PWMx Counter ON Time Register	40005880h
16-bit PWM	8	PWMx Counter OFF Time Register	40005884h
16-bit PWM	8	PWMx Configuration Register	40005888h
16-bit PWM	8	TEST	4000588Ch
16-bit PWM	9	PWMx Counter ON Time Register	40005890h
16-bit PWM	9	PWMx Counter OFF Time Register	40005894h
16-bit PWM	9	PWMx Configuration Register	40005898h
16-bit PWM	9	TEST	4000589Ch
16-bit PWM	10	PWMx Counter ON Time Register	400058A0h
16-bit PWM	10	PWMx Counter OFF Time Register	400058A4h
16-bit PWM	10	PWMx Configuration Register	400058A8h
16-bit PWM	10	TEST	400058ACh
16-bit Tach	0	TACHx Control Register	40006000h
16-bit Tach	0	TACHx Status Register	40006004h
16-bit Tach	0	TACHx High Limit Register	40006008h
16-bit Tach	0	TACHx Low Limit Register	4000600Ch
16-bit Tach	1	TACHx Control Register	40006010h
16-bit Tach	1	TACHx Status Register	40006014h
16-bit Tach	1	TACHx High Limit Register	40006018h
16-bit Tach	1	TACHx Low Limit Register	4000601Ch
16-bit Tach	2	TACHx Control Register	40006020h
16-bit Tach	2	TACHx Status Register	40006024h
16-bit Tach	2	TACHx High Limit Register	40006028h
16-bit Tach	2	TACHx Low Limit Register	4000602Ch
PECI	0	Write Data Register	40006400h
PECI	0	Read Data Register	40006404h
PECI	0	Control Register	40006408h
PECI	0	Status Register 1	4000640Ch
PECI	0	Status Register 2	40006410h
PECI	0	Error Register	40006414h

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Block	Instance	Register	Register Address
PECI	0	Interrupt Enable 1 Register	40006418h
PECI	0	Interrupt Enable 2 Register	4000641Ch
PECI	0	Optimal Bit Time Register (Low Byte)	40006420h
PECI	0	Optimal Bit Time Register (High Byte)	40006424h
PECI	0	TEST	40006428h
PECI	0	TEST	4000642Ch
PECI	0	Block ID Register	40006440h
PECI	0	Revision Register	40006444h
RTOS Timer	0	RTOS Timer Count Register	40007400h
RTOS Timer	0	RTOS Timer Preload Register	40007404h
RTOS Timer	0	RTOS Timer Control Register	40007408h
RTOS Timer	0	Soft Interrupt Register	4000740Ch
ADC	0	ADC Control Register	40007C00h
ADC	0	ADC Delay Register	40007C04h
ADC	0	ADC Status Register	40007C08h
ADC	0	ADC Single Register	40007C0Ch
ADC	0	ADC Repeat Register	40007C10h
ADC	0	ADC Channel 0 Reading Register	40007C14h
ADC	0	ADC Channel 1 Reading Register	40007C18h
ADC	0	ADC Channel 2 Reading Register	40007C1Ch
ADC	0	ADC Channel 3 Reading Register	40007C20h
ADC	0	ADC Channel 4 Reading Register	40007C24h
ADC	0	ADC Channel 5 Reading Register	40007C28h
ADC	0	ADC Channel 6 Reading Register	40007C2Ch
ADC	0	ADC Channel 7 Reading Register	40007C30h
ADC	0	ADC Channel 8 Reading Register	40007C34h
ADC	0	ADC Channel 9 Reading Register	40007C38h
ADC	0	ADC Channel 10 Reading Register	40007C3Ch
ADC	0	ADC Channel 11 Reading Register	40007C40h
ADC	0	ADC Channel 12 Reading Register	40007C44h
ADC	0	ADC Channel 13 Reading Register	40007C48h
ADC	0	ADC Channel 14 Reading Register	40007C4Ch
ADC	0	ADC Channel 15 Reading Register	40007C50h
ADC	0	ADC Test Register	40007C78h
ADC	0	ADC Configuration Register	40007C7Ch
TFDP	0	Debug Data Register	40008C00h
TFDP	0	Debug Control Register	40008C04h
PS2	0	PS2 Transmit Buffer Register	40009000h
PS2	0	PS2 Receive Buffer Register	40009000h
PS2	0	PS2 Control Register	40009004h
PS2	0	PS2 Status Register	40009008h
PS2	1	PS2 Transmit Buffer Register	40009040h
PS2	1	PS2 Receive Buffer Register	40009040h

Block	Instance	Register	Register Address
PS2	1	PS2 Control Register	40009044h
PS2	1	PS2 Status Register	40009048h
PS2	2	PS2 Transmit Buffer Register	40009080h
PS2	2	PS2 Receive Buffer Register	40009080h
PS2	2	PS2 Control Register	40009084h
PS2	2	PS2 Status Register	40009088h
GP-SPI	0	SPI Enable Register	40009400h
GP-SPI	0	SPI Control Register	40009404h
GP-SPI	0	SPI Status Register	40009408h
GP-SPI	0	SPI TX_Data Register	4000940Ch
GP-SPI	0	SPI RX_Data Register	40009410h
GP-SPI	0	SPI Clock Control Register	40009414h
GP-SPI	0	SPI Clock Generator Register	40009418h
GP-SPI	0	TESET	40009420h
GP-SPI	1	SPI Enable Register	40009480h
GP-SPI	1	SPI Control Register	40009484h
GP-SPI	1	SPI Status Register	40009488h
GP-SPI	1	SPI TX_Data Register	4000948Ch
GP-SPI	1	SPI RX_Data Register	40009490h
GP-SPI	1	SPI Clock Control Register	40009494h
GP-SPI	1	SPI Clock Generator Register	40009498h
GP-SPI	1	TESET	400094A0h
Hibernation Timer	0	HTimer Preload Register	40009800h
Hibernation Timer	0	HTimer Control Register	40009804h
Hibernation Timer	0	HTimer Count Register	40009808h
Hibernation Timer	1	HTimer Preload Register	40009820h
Hibernation Timer	1	HTimer Control Register	40009824h
Hibernation Timer	1	HTimer Count Register	40009828h
Keyscan	0	KSO Select Register	40009C04h
Keyscan	0	KSI INPUT Register	40009C08h
Keyscan	0	KSI STATUS Register	40009C0Ch
Keyscan	0	KSI INTERRUPT ENABLE Register	40009C10h
Keyscan	0	Keyscan Extended Control Register	40009C14h
RPM2PWM	0	Fan Setting Register	4000A000h
RPM2PWM	0	PWM Divide Register	4000A001h
RPM2PWM	0	Fan Configuration 1 Register	4000A002h
RPM2PWM	0	Fan Configuration 2 Register	4000A003h
RPM2PWM	0	Reserved	4000A004h
RPM2PWM	0	Gain Register	4000A005h
RPM2PWM	0	Fan Spin Up Configuration Register	4000A006h
RPM2PWM	0	Fan Step Register	4000A007h
RPM2PWM	0	Fan Minimum Drive Register	4000A008h
RPM2PWM	0	Valid TACH Count Register	4000A009h

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Block	Instance	Register	Register Address
RPM2PWM	0	Fan Drive Fail Band Register	4000A00Ah
RPM2PWM	0	TACH Target Register	4000A00Ch
RPM2PWM	0	TACH Reading Register	4000A00Eh
RPM2PWM	0	PWM Driver Base Frequency Register	4000A010h
RPM2PWM	0	Fan Status Register	4000A011h
RPM2PWM	0	TEST	4000A012h
RPM2PWM	0	TEST	4000A014h
RPM2PWM	0	TEST	4000A015h
RPM2PWM	0	TEST	4000A016h
RPM2PWM	0	TEST	4000A017h
RPM2PWM	1	Fan Setting Register	4000A080h
RPM2PWM	1	PWM Divide Register	4000A081h
RPM2PWM	1	Fan Configuration 1 Register	4000A082h
RPM2PWM	1	Fan Configuration 2 Register	4000A083h
RPM2PWM	1	Reserved	4000A084h
RPM2PWM	1	Gain Register	4000A085h
RPM2PWM	1	Fan Spin Up Configuration Register	4000A086h
RPM2PWM	1	Fan Step Register	4000A087h
RPM2PWM	1	Fan Minimum Drive Register	4000A088h
RPM2PWM	1	Valid TACH Count Register	4000A089h
RPM2PWM	1	Fan Drive Fail Band Register	4000A08Ah
RPM2PWM	1	TACH Target Register	4000A08Ch
RPM2PWM	1	TACH Reading Register	4000A08Eh
RPM2PWM	1	PWM Driver Base Frequency Register	4000A090h
RPM2PWM	1	Fan Status Register	4000A091h
RPM2PWM	1	TEST	4000A092h
RPM2PWM	1	TEST	4000A094h
RPM2PWM	1	TEST	4000A095h
RPM2PWM	1	TEST	4000A096h
RPM2PWM	1	TEST	4000A097h
VBAT Register Bank	0	Power-Fail and Reset Status Register	4000A400h
VBAT Register Bank	0	TEST	4000A404h
VBAT Register Bank	0	Clock Enable Register	4000A408h
VBAT Register Bank	0	TEST	4000A40Ch
VBAT Register Bank	0	TEST	4000A410h
VBAT Register Bank	0	TEST	4000A414h
VBAT Register Bank	0	TEST	4000A418h
VBAT Register Bank	0	TEST	4000A41Ch
VBAT Register Bank	0	Monotonic Counter Register	4000A420h
VBAT Register Bank	0	Counter HiWord Register	4000A424h
VBAT Register Bank	0	VWire Backup Register	4000A428h
VBAT Register Bank	0	TEST	4000A42Ch
VBAT Powered RAM	0	Registers	4000A800h

Block	Instance	Register	Register Address
Week Timer	0	Control Register	4000AC80h
Week Timer	0	Week Alarm Counter Register	4000AC84h
Week Timer	0	Week Timer Compare Register	4000AC88h
Week Timer	0	Clock Divider Register	4000AC8Ch
Week Timer	0	Sub-Second Programmable Interrupt Select Register	4000AC90h
Week Timer	0	Sub-Week Control Register	4000AC94h
Week Timer	0	Sub-Week Alarm Counter Register	4000AC98h
Week Timer	0	BGPO Data Register	4000AC9Ch
Week Timer	0	BGPO Power Register	4000ACA0h
Week Timer	0	BGPO Reset Register	4000ACA4h
VBAT-Powered Control Interface	0	VCI Register	4000AE00h
VBAT-Powered Control Interface	0	Latch Enable Register	4000AE04h
VBAT-Powered Control Interface	0	Latch Resets Register	4000AE08h
VBAT-Powered Control Interface	0	VCI Input Enable Register	4000AE0Ch
VBAT-Powered Control Interface	0	Holdoff Count Register	4000AE10h
VBAT-Powered Control Interface	0	VCI Polarity Register	4000AE14h
VBAT-Powered Control Interface	0	VCI Posedge Detect Register	4000AE18h
VBAT-Powered Control Interface	0	VCI Negedge Detect Register	4000AE1Ch
VBAT-Powered Control Interface	0	VCI Buffer Enable Register	4000AE20h
Blinking-Breathing PWM	0	LED Configuration Register	4000B800h
Blinking-Breathing PWM	0	LED Limits Register	4000B804h
Blinking-Breathing PWM	0	LED Delay Register	4000B808h
Blinking-Breathing PWM	0	LED Update Stepsize Register	4000B80Ch
Blinking-Breathing PWM	0	LED Update Interval Register	4000B810h
Blinking-Breathing PWM	0	LED Output Delay	4000B814h
Blinking-Breathing PWM	1	LED Configuration Register	4000B900h
Blinking-Breathing PWM	1	LED Limits Register	4000B904h
Blinking-Breathing PWM	1	LED Delay Register	4000B908h
Blinking-Breathing PWM	1	LED Update Stepsize Register	4000B90Ch
Blinking-Breathing PWM	1	LED Update Interval Register	4000B910h
Blinking-Breathing PWM	1	LED Output Delay	4000B914h
Blinking-Breathing PWM	2	LED Configuration Register	4000BA00h
Blinking-Breathing PWM	2	LED Limits Register	4000BA04h
Blinking-Breathing PWM	2	LED Delay Register	4000BA08h
Blinking-Breathing PWM	2	LED Update Stepsize Register	4000BA0Ch
Blinking-Breathing PWM	2	LED Update Interval Register	4000BA10h
Blinking-Breathing PWM	2	LED Output Delay	4000BA14h
Blinking-Breathing PWM	3	LED Configuration Register	4000BB00h
Blinking-Breathing PWM	3	LED Limits Register	4000BB04h
Blinking-Breathing PWM	3	LED Delay Register	4000BB08h
Blinking-Breathing PWM	3	LED Update Stepsize Register	4000BB0Ch
Blinking-Breathing PWM	3	LED Update Interval Register	4000BB10h

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Block	Instance	Register	Register Address
Blinking-Breathing PWM	3	LED Output Delay	4000BB14h
Public Key Engine	0	Configuration Register	4000BD00h
Public Key Engine	0	Command Register	4000BD04h
Public Key Engine	0	Control Register	4000BD08h
Public Key Engine	0	Status Register	4000BD0Ch
Public Key Engine	0	Version Register	4000BD10h
Random Number Generator	0	Control Register	4000BE00h
Random Number Generator	0	FIFOLevel Register	4000BE04h
Random Number Generator	0	Version Register	4000BE08h
BC-Link Master	0	BC-Link Status Register	4000CD00h
BC-Link Master	0	BC-Link Address Register	4000CD04h
BC-Link Master	0	BC-Link Data Register	4000CD08h
BC-Link Master	0	BC-Link Clock Select Register	4000CD0Ch
BC-Link Master	1	BC-Link Status Register	4000CD20h
BC-Link Master	1	BC-Link Address Register	4000CD24h
BC-Link Master	1	BC-Link Data Register	4000CD28h
BC-Link Master	1	BC-Link Clock Select Register	4000CD2Ch
Hash Engine	0	SHAMode Register	4000D000h
Hash Engine	0	NbBlock Register	4000D004h
Hash Engine	0	Config Register	4000D008h
Hash Engine	0	Status Register	4000D00Ch
Hash Engine	0	Version Register	4000D010h
Symmetric Encryption Engine	0	Configuration Register	4000D200h
Symmetric Encryption Engine	0	Command Register	4000D204h
Symmetric Encryption Engine	0	Control Register	4000D208h
Symmetric Encryption Engine	0	Status Register	4000D20Ch
Symmetric Encryption Engine	0	Version Register	4000D210h
Symmetric Encryption Engine	0	Number of header data Register	4000D214h
Symmetric Encryption Engine	0	Last header data size Register	4000D218h
Symmetric Encryption Engine	0	Number of block data Register	4000D21Ch
Symmetric Encryption Engine	0	Last block data size Register	4000D220h
Symmetric Encryption Engine	0	DMA Input Base Address Register	4000D224h
Symmetric Encryption Engine	0	DMA Output Base Address Register	4000D228h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[159:128]	4000D300h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[191:160]	4000D304h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[223:192]	4000D308h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[255:224]	4000D30Ch
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[31:0]	4000D310h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[63:32]	4000D314h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[95:64]	4000D318h
Symmetric Encryption Engine	0	Key1 Register – access to KeyIn1[127:96]	4000D31Ch
Symmetric Encryption Engine	0	IV Register – access to IV[31:0]	4000D320h
Symmetric Encryption Engine	0	IV Register – access to IV[63:32]	4000D324h

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Block	Instance	Register	Register Address
Symmetric Encryption Engine	0	IV Register – access to IV[95:64]	4000D328h
Symmetric Encryption Engine	0	IV Register – access to IV[127:96]	4000D32Ch
Symmetric Encryption Engine	0	unused	4000D330h
Symmetric Encryption Engine	0	unused	4000D334h
Symmetric Encryption Engine	0	unused	4000D338h
Symmetric Encryption Engine	0	unused	4000D33Ch
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[159:128]	4000D340h
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[191:160]	4000D344h
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[223:192]	4000D348h
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[255:224]	4000D34Ch
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[31:0]	4000D350h
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[63:32]	4000D354h
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[95:64]	4000D358h
Symmetric Encryption Engine	0	Key2 Register – access to KeyIn2[127:96]	4000D35Ch
Interrupt Aggregator	0	GIRQ8 Source Register	4000E000h
Interrupt Aggregator	0	GIRQ8 Enable Set Register	4000E004h
Interrupt Aggregator	0	GIRQ8 Result Register	4000E008h
Interrupt Aggregator	0	GIRQ8 Enable Clear Register	4000E00Ch
Interrupt Aggregator	0	GIRQ9 Source Register	4000E014h
Interrupt Aggregator	0	GIRQ9 Enable Set Register	4000E018h
Interrupt Aggregator	0	GIRQ9 Result Register	4000E01Ch
Interrupt Aggregator	0	GIRQ9 Enable Clear Register	4000E020h
Interrupt Aggregator	0	GIRQ10 Source Register	4000E028h
Interrupt Aggregator	0	GIRQ10 Enable Set Register	4000E02Ch
Interrupt Aggregator	0	GIRQ10 Result Register	4000E030h
Interrupt Aggregator	0	GIRQ10 Enable Clear Register	4000E034h
Interrupt Aggregator	0	GIRQ11 Source Register	4000E03Ch
Interrupt Aggregator	0	GIRQ11 Enable Set Register	4000E040h
Interrupt Aggregator	0	GIRQ11 Result Register	4000E044h
Interrupt Aggregator	0	GIRQ11 Enable Clear Register	4000E048h
Interrupt Aggregator	0	GIRQ12 Source Register	4000E050h
Interrupt Aggregator	0	GIRQ12 Enable Set Register	4000E054h
Interrupt Aggregator	0	GIRQ12 Result Register	4000E058h
Interrupt Aggregator	0	GIRQ12 Enable Clear Register	4000E05Ch
Interrupt Aggregator	0	GIRQ13 Source Register	4000E064h
Interrupt Aggregator	0	GIRQ13 Enable Set Register	4000E068h
Interrupt Aggregator	0	GIRQ13 Result Register	4000E06Ch
Interrupt Aggregator	0	GIRQ13 Enable Clear Register	4000E070h
Interrupt Aggregator	0	GIRQ14 Source Register	4000E078h
Interrupt Aggregator	0	GIRQ14 Enable Set Register	4000E07Ch
Interrupt Aggregator	0	GIRQ14 Result Register	4000E080h
Interrupt Aggregator	0	GIRQ14 Enable Clear Register	4000E084h
Interrupt Aggregator	0	GIRQ15 Source Register	4000E08Ch

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Block	Instance	Register	Register Address
Interrupt Aggregator	0	GIRQ15 Enable Set Register	4000E090h
Interrupt Aggregator	0	GIRQ15 Result Register	4000E094h
Interrupt Aggregator	0	GIRQ15 Enable Clear Register	4000E098h
Interrupt Aggregator	0	GIRQ16 Source Register	4000E0A0h
Interrupt Aggregator	0	GIRQ16 Enable Set Register	4000E0A4h
Interrupt Aggregator	0	GIRQ16 Result Register	4000E0A8h
Interrupt Aggregator	0	GIRQ16 Enable Clear Register	4000E0ACh
Interrupt Aggregator	0	GIRQ17 Source Register	4000E0B4h
Interrupt Aggregator	0	GIRQ17 Enable Set Register	4000E0B8h
Interrupt Aggregator	0	GIRQ17 Result Register	4000E0BCh
Interrupt Aggregator	0	GIRQ17 Enable Clear Register	4000E0C0h
Interrupt Aggregator	0	GIRQ18 Source Register	4000E0C8h
Interrupt Aggregator	0	GIRQ18 Enable Set Register	4000E0CCh
Interrupt Aggregator	0	GIRQ18 Result Register	4000E0D0h
Interrupt Aggregator	0	GIRQ18 Enable Clear Register	4000E0D4h
Interrupt Aggregator	0	GIRQ19 Source Register	4000E0DCh
Interrupt Aggregator	0	GIRQ19 Enable Set Register	4000E0E0h
Interrupt Aggregator	0	GIRQ19 Result Register	4000E0E4h
Interrupt Aggregator	0	GIRQ19 Enable Clear Register	4000E0E8h
Interrupt Aggregator	0	GIRQ20 Source Register	4000E0F0h
Interrupt Aggregator	0	GIRQ20 Enable Set Register	4000E0F4h
Interrupt Aggregator	0	GIRQ20 Result Register	4000E0F8h
Interrupt Aggregator	0	GIRQ20 Enable Clear Register	4000E0FCh
Interrupt Aggregator	0	GIRQ21 Source Register	4000E104h
Interrupt Aggregator	0	GIRQ21 Enable Set Register	4000E108h
Interrupt Aggregator	0	GIRQ21 Result Register	4000E10Ch
Interrupt Aggregator	0	GIRQ21 Enable Clear Register	4000E110h
Interrupt Aggregator	0	GIRQ22 Source Register	4000E118h
Interrupt Aggregator	0	GIRQ22 Enable Set Register	4000E11Ch
Interrupt Aggregator	0	GIRQ22 Result Register	4000E120h
Interrupt Aggregator	0	GIRQ22 Enable Clear Register	4000E124h
Interrupt Aggregator	0	GIRQ23 Source Register	4000E12Ch
Interrupt Aggregator	0	GIRQ23 Enable Set Register	4000E130h
Interrupt Aggregator	0	GIRQ23 Result Register	4000E134h
Interrupt Aggregator	0	GIRQ23 Enable Clear Register	4000E138h
Interrupt Aggregator	0	GIRQ24 Source Register	4000E140h
Interrupt Aggregator	0	GIRQ24 Enable Set Register	4000E144h
Interrupt Aggregator	0	GIRQ24 Result Register	4000E148h
Interrupt Aggregator	0	GIRQ24 Enable Clear Register	4000E14Ch
Interrupt Aggregator	0	GIRQ25 Source Register	4000E154h
Interrupt Aggregator	0	GIRQ25 Enable Set Register	4000E158h
Interrupt Aggregator	0	GIRQ25 Result Register	4000E15Ch
Interrupt Aggregator	0	GIRQ25 Enable Clear Register	4000E160h

Block	Instance	Register	Register Address
Interrupt Aggregator	0	GIRQ26 Source Register	4000E168h
Interrupt Aggregator	0	GIRQ26 Enable Set Register	4000E16Ch
Interrupt Aggregator	0	GIRQ26 Result Register	4000E170h
Interrupt Aggregator	0	GIRQ26 Enable Clear Register	4000E174h
Interrupt Aggregator	0	Block Enable Set Register	4000E200h
Interrupt Aggregator	0	Block Enable Clear Register	4000E204h
Interrupt Aggregator	0	Block IRQ Vector Register	4000E208h
EC Register Bank	0	TEST	4000FC00h
EC Register Bank	0	AHB Error Address Register	4000FC04h
EC Register Bank	0	TEST	4000FC08h
EC Register Bank	0	TEST	4000FC0Ch
EC Register Bank	0	TEST	4000FC10h
EC Register Bank	0	AHB Error Control Register	4000FC14h
EC Register Bank	0	Interrupt Control Register	4000FC18h
EC Register Bank	0	ETM TRACE Enable Register	4000FC1Ch
EC Register Bank	0	Debug Enable Register	4000FC20h
EC Register Bank	0	OTP Lock Register	4000FC24h
EC Register Bank	0	WDT Event Count Register	4000FC28h
EC Register Bank	0	AES HASH Byte Swap Control Register	4000FC2Ch
EC Register Bank	0	TEST	4000FC30h
EC Register Bank	0	TEST	4000FC34h
EC Register Bank	0	Reserved	4000FC38h
EC Register Bank	0	TEST	4000FC3Ch
EC Register Bank	0	PECI Disable Register	4000FC40h
EC Register Bank	0	TEST	4000FC44h
EC Register Bank	0	TEST	4000FC48h
EC Register Bank	0	Crypto Soft Reset Register	4000FC5Ch
EC Register Bank	0	TEST	4000FC60h
EC Register Bank	0	GPIO Bank Power Register	4000FC64h
EC Register Bank	0	TEST	4000FC68h
EC Register Bank	0	TEST	4000FC6Ch
EC Register Bank	0	JTAG Master Configuration Register	4000FC70h
EC Register Bank	0	JTAG Master Status Register	4000FC74h
EC Register Bank	0	JTAG Master TDO Register	4000FC78h
EC Register Bank	0	JTAG Master TDI Register	4000FC7Ch
EC Register Bank	0	JTAG Master TMS Register	4000FC80h
EC Register Bank	0	JTAG Master Command Register	4000FC84h
Power Clocks and Resets	0	System Sleep Control Register	40080100h
Power Clocks and Resets	0	Processor Clock Control Register	40080104h
Power Clocks and Resets	0	Slow Clock Control Register	40080108h
Power Clocks and Resets	0	Oscillator ID Register	4008010Ch
Power Clocks and Resets	0	PCR Power Reset Status Register	40080110h
Power Clocks and Resets	0	Power Reset Control Register	40080114h

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Block	Instance	Register	Register Address
Power Clocks and Resets	0	System Reset Register	40080118h
Power Clocks and Resets	0	TEST	4008011Ch
Power Clocks and Resets	0	TEST	40080120h
Power Clocks and Resets	0	Sleep Enable 0 Register	40080130h
Power Clocks and Resets	0	Sleep Enable 1 Register	40080134h
Power Clocks and Resets	0	Sleep Enable 2 Register	40080138h
Power Clocks and Resets	0	Sleep Enable 3 Register	4008013Ch
Power Clocks and Resets	0	Sleep Enable 4 Register	40080140h
Power Clocks and Resets	0	Clock Required 0 Register	40080150h
Power Clocks and Resets	0	Clock Required 1 Register	40080154h
Power Clocks and Resets	0	Clock Required 2 Register	40080158h
Power Clocks and Resets	0	Clock Required 3 Register	4008015Ch
Power Clocks and Resets	0	Clock Required 4 Register	40080160h
Power Clocks and Resets	0	Reset Enable 0 Register	40080170h
Power Clocks and Resets		Reset Enable 1 Register	40080174h
Power Clocks and Resets		Reset Enable 2 Register	40080178h
Power Clocks and Resets		Reset Enable 3 Register	4008017Ch
Power Clocks and Resets		Reset Enable 4 Register	40080180h
GPIO	0	GPIO000 Pin Control Register	40081000h
GPIO	0	GPIO001 Pin Control Register	40081004h
GPIO	0	GPIO002 Pin Control Register	40081008h
GPIO	0	GPIO003 Pin Control Register	4008100Ch
GPIO	0	GPIO004 Pin Control Register	40081010h
GPIO	0	GPIO005 Pin Control Register	40081014h
GPIO	0	GPIO006 Pin Control Register	40081018h
GPIO	0	GPIO007 Pin Control Register	4008101Ch
GPIO	0	GPIO010 Pin Control Register	40081020h
GPIO	0	GPIO011 Pin Control Register	40081024h
GPIO	0	GPIO012 Pin Control Register	40081028h
GPIO	0	GPIO013 Pin Control Register	4008102Ch
GPIO	0	GPIO014 Pin Control Register	40081030h
GPIO	0	GPIO015 Pin Control Register	40081034h
GPIO	0	GPIO016 Pin Control Register	40081038h
GPIO	0	GPIO017 Pin Control Register	4008103Ch
GPIO	0	GPIO020 Pin Control Register	40081040h
GPIO	0	GPIO021 Pin Control Register	40081044h
GPIO	0	GPIO022 Pin Control Register	40081048h
GPIO	0	GPIO023 Pin Control Register	4008104Ch
GPIO	0	GPIO024 Pin Control Register	40081050h
GPIO	0	GPIO025 Pin Control Register	40081054h
GPIO	0	GPIO026 Pin Control Register	40081058h
GPIO	0	GPIO027 Pin Control Register	4008105Ch
GPIO	0	GPIO030 Pin Control Register	40081060h

Block	Instance	Register	Register Address
GPIO	0	GPIO031 Pin Control Register	40081064h
GPIO	0	GPIO032 Pin Control Register	40081068h
GPIO	0	GPIO033 Pin Control Register	4008106Ch
GPIO	0	GPIO034 Pin Control Register	40081070h
GPIO	0	GPIO035 Pin Control Register	40081074h
GPIO	0	GPIO036 Pin Control Register	40081078h
GPIO	0	GPIO040 Pin Control Register	40081080h
GPIO	0	GPIO041 Pin Control Register	40081084h
GPIO	0	GPIO042 Pin Control Register	40081088h
GPIO	0	GPIO043 Pin Control Register	4008108Ch
GPIO	0	GPIO044 Pin Control Register	40081090h
GPIO	0	GPIO045 Pin Control Register	40081094h
GPIO	0	GPIO046 Pin Control Register	40081098h
GPIO	0	GPIO047 Pin Control Register	4008109Ch
GPIO	0	GPIO050 Pin Control Register	400810A0h
GPIO	0	GPIO051 Pin Control Register	400810A4h
GPIO	0	GPIO052 Pin Control Register	400810A8h
GPIO	0	GPIO053 Pin Control Register	400810ACh
GPIO	0	GPIO054 Pin Control Register	400810B0h
GPIO	0	GPIO055 Pin Control Register	400810B4h
GPIO	0	GPIO056 Pin Control Register	400810B8h
GPIO	0	(GPIO057) Pin Control Register	400810BCh
GPIO	0	GPIO060 Pin Control Register	400810C0h
GPIO	0	GPIO061 Pin Control Register	400810C4h
GPIO	0	GPIO062 Pin Control Register	400810C8h
GPIO	0	GPIO063 Pin Control Register	400810CCh
GPIO	0	GPIO064 Pin Control Register	400810D0h
GPIO	0	GPIO065 Pin Control Register	400810D4h
GPIO	0	GPIO066 Pin Control Register	400810D8h
GPIO	0	GPIO067 Pin Control Register	400810DCh
GPIO	0	GPIO070 Pin Control Register	400810E0h
GPIO	0	GPIO071 Pin Control Register	400810E4h
GPIO	0	GPIO072 Pin Control Register	400810E8h
GPIO	0	GPIO073 Pin Control Register	400810ECh
GPIO	0	GPIO100 Pin Control Register	40081100h
GPIO	0	GPIO101 Pin Control Register	40081104h
GPIO	0	GPIO102 Pin Control Register	40081108h
GPIO	0	GPIO104 Pin Control Register	40081110h
GPIO	0	GPIO105 Pin Control Register	40081114h
GPIO	0	GPIO106 Pin Control Register	40081118h
GPIO	0	GPIO107 Pin Control Register	4008111Ch
GPIO	0	GPIO110 Pin Control Register	40081120h
GPIO	0	GPIO111 Pin Control Register	40081124h

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Block	Instance	Register	Register Address
GPIO	0	GPIO112 Pin Control Register	40081128h
GPIO	0	GPIO113 Pin Control Register	4008112Ch
GPIO	0	GPIO114 Pin Control Register	40081130h
GPIO	0	GPIO115 Pin Control Register	40081134h
GPIO	0	GPIO120 Pin Control Register	40081140h
GPIO	0	GPIO121 Pin Control Register	40081144h
GPIO	0	GPIO122 Pin Control Register	40081148h
GPIO	0	GPIO123 Pin Control Register	4008114Ch
GPIO	0	GPIO124 Pin Control Register	40081150h
GPIO	0	GPIO125 Pin Control Register	40081154h
GPIO	0	GPIO126 Pin Control Register	40081158h
GPIO	0	GPIO127 Pin Control Register	4008115Ch
GPIO	0	GPIO130 Pin Control Register	40081160h
GPIO	0	GPIO131 Pin Control Register	40081164h
GPIO	0	GPIO132 Pin Control Register	40081168h
GPIO	0	GPIO133 Pin Control Register	4008116Ch
GPIO	0	GPIO134 Pin Control Register	40081170h
GPIO	0	GPIO135 Pin Control Register	40081174h
GPIO	0	GPIO140 Pin Control Register	40081180h
GPIO	0	GPIO141 Pin Control Register	40081184h
GPIO	0	GPIO142 Pin Control Register	40081188h
GPIO	0	GPIO143 Pin Control Register	4008118Ch
GPIO	0	GPIO144 Pin Control Register	40081190h
GPIO	0	GPIO145 Pin Control Register	40081194h
GPIO	0	GPIO146 Pin Control Register	40081198h
GPIO	0	GPIO147 Pin Control Register	4008119Ch
GPIO	0	GPIO150 Pin Control Register	400811A0h
GPIO	0	GPIO151 Pin Control Register	400811A4h
GPIO	0	GPIO152 Pin Control Register	400811A8h
GPIO	0	GPIO153 Pin Control Register	400811ACh
GPIO	0	GPIO154 Pin Control Register	400811B0h
GPIO	0	GPIO155 Pin Control Register	400811B4h
GPIO	0	GPIO156 Pin Control Register	400811B8h
GPIO	0	GPIO157 Pin Control Register	400811BCh
GPIO	0	GPIO160 Pin Control Register	400811C0h
GPIO	0	GPIO161 Pin Control Register	400811C4h
GPIO	0	GPIO162 Pin Control Register	400811C8h
GPIO	0	GPIO163 Pin Control Register	400811CCh
GPIO	0	GPIO165 Pin Control Register	400811D4h
GPIO	0	GPIO166 Pin Control Register	400811D8h
GPIO	0	GPIO170 Pin Control Register	400811E0h
GPIO	0	GPIO171 Pin Control Register	400811E4h
GPIO	0	GPIO172 Pin Control Register	400811E8h

Block	Instance	Register	Register Address
GPIO	0	GPIO173 Pin Control Register	400811ECh
GPIO	0	GPIO174 Pin Control Register	400811F0h
GPIO	0	GPIO175 Pin Control Register	400811F4h
GPIO	0	GPIO200 Pin Control Register	40081200h
GPIO	0	GPIO201 Pin Control Register	40081204h
GPIO	0	GPIO202 Pin Control Register	40081208h
GPIO	0	GPIO203 Pin Control Register	4008120Ch
GPIO	0	GPIO204 Pin Control Register	40081210h
GPIO	0	GPIO205 Pin Control Register	40081214h
GPIO	0	GPIO206 Pin Control Register	40081218h
GPIO	0	GPIO207 Pin Control Register	4008121Ch
GPIO	0	GPIO210 Pin Control Register	40081220h
GPIO	0	GPIO211 Pin Control Register	40081224h
GPIO	0	GPIO212 Pin Control Register	40081228h
GPIO	0	GPIO213 Pin Control Register	4008122Ch
GPIO	0	GPIO214 Pin Control Register	40081230h
GPIO	0	GPIO215 Pin Control Register	40081234h
GPIO	0	GPIO216 Pin Control Register	40081238h
GPIO	0	GPIO217 Pin Control Register	4008123Ch
GPIO	0	GPIO221 Pin Control Register	40081244h
GPIO	0	GPIO222 Pin Control Register	40081248h
GPIO	0	GPIO223 Pin Control Register	4008124Ch
GPIO	0	GPIO224 Pin Control Register	40081250h
GPIO	0	GPIO225 Pin Control Register	40081254h
GPIO	0	GPIO226 Pin Control Register	40081258h
GPIO	0	GPIO227 Pin Control Register	4008125Ch
GPIO	0	GPIO230 Pin Control Register	40081260h
GPIO	0	GPIO231 Pin Control Register	40081264h
GPIO	0	GPIO233 Pin Control Register	4008126Ch
GPIO	0	GPIO234 Pin Control Register	40081270h
GPIO	0	GPIO240 Pin Control Register	40081280h
GPIO	0	GPIO241 Pin Control Register	40081284h
GPIO	0	GPIO242 Pin Control Register	40081288h
GPIO	0	GPIO243 Pin Control Register	4008128Ch
GPIO	0	GPIO244 Pin Control Register	40081290h
GPIO	0	GPIO245 Pin Control Register	40081294h
GPIO	0	GPIO246 Pin Control Register	40081298h
GPIO	0	GPIO250 Pin Control Register	400812A0h
GPIO	0	GPIO253 Pin Control Register	400812ACh
GPIO	0	GPIO254 Pin Control Register	400812B0h
GPIO	0	Input GPIO[000:036]	40081300h
GPIO	0	Input GPIO[040:076]	40081304h
GPIO	0	Input GPIO[100:127]	40081308h

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Block	Instance	Register	Register Address
GPIO	0	Input GPIO[140:176]	4008130Ch
GPIO	0	Input GPIO[200:236]	40081310h
GPIO	0	Input GPIO[240:276]	40081314h
GPIO	0	Output GPIO[000:036]	40081380h
GPIO	0	Output GPIO[040:076]	40081384h
GPIO	0	Output GPIO[100:127]	40081388h
GPIO	0	Output GPIO[140:176]	4008138Ch
GPIO	0	Output GPIO[200:236]	40081390h
GPIO	0	Output GPIO[240:276]	40081394h
GPIO	0	GPIO000 Pin Control 2 Register	40081500h
GPIO	0	GPIO001 Pin Control 2 Register	40081504h
GPIO	0	GPIO002 Pin Control 2 Register	40081508h
GPIO	0	GPIO003 Pin Control 2 Register	4008150Ch
GPIO	0	GPIO004 Pin Control 2 Register	40081510h
GPIO	0	GPIO005 Pin Control 2 Register	40081514h
GPIO	0	GPIO006 Pin Control 2 Register	40081518h
GPIO	0	GPIO007 Pin Control 2 Register	4008151Ch
GPIO	0	GPIO010 Pin Control 2 Register	40081520h
GPIO	0	GPIO011 Pin Control 2 Register	40081524h
GPIO	0	GPIO012 Pin Control 2 Register	40081528h
GPIO	0	GPIO013 Pin Control 2 Register	4008152Ch
GPIO	0	GPIO014 Pin Control 2 Register	40081530h
GPIO	0	GPIO015 Pin Control 2 Register	40081534h
GPIO	0	GPIO016 Pin Control 2 Register	40081538h
GPIO	0	GPIO017 Pin Control 2 Register	4008153Ch
GPIO	0	GPIO020 Pin Control 2 Register	40081540h
GPIO	0	GPIO021 Pin Control 2 Register	40081544h
GPIO	0	GPIO022 Pin Control 2 Register	40081548h
GPIO	0	GPIO023 Pin Control 2 Register	4008154Ch
GPIO	0	GPIO024 Pin Control 2 Register	40081550h
GPIO	0	GPIO025 Pin Control 2 Register	40081554h
GPIO	0	GPIO026 Pin Control 2 Register	40081558h
GPIO	0	GPIO027 Pin Control 2 Register	4008155Ch
GPIO	0	GPIO030 Pin Control 2 Register	40081560h
GPIO	0	GPIO031 Pin Control 2 Register	40081564h
GPIO	0	GPIO032 Pin Control 2 Register	40081568h
GPIO	0	GPIO033 Pin Control 2 Register	4008156Ch
GPIO	0	GPIO034 Pin Control 2 Register	40081570h
GPIO	0	GPIO035 Pin Control 2 Register	40081574h
GPIO	0	GPIO036 Pin Control 2 Register	40081578h
GPIO	0	GPIO040 Pin Control 2 Register	40081580h
GPIO	0	GPIO041 Pin Control 2 Register	40081584h
GPIO	0	GPIO042 Pin Control 2 Register	40081588h

Block	Instance	Register	Register Address
GPIO	0	GPIO043 Pin Control 2 Register	4008158Ch
GPIO	0	GPIO044 Pin Control 2 Register	40081590h
GPIO	0	GPIO045 Pin Control 2 Register	40081594h
GPIO	0	GPIO046 Pin Control 2 Register	40081598h
GPIO	0	GPIO047 Pin Control 2 Register	4008159Ch
GPIO	0	GPIO050 Pin Control 2 Register	400815A0h
GPIO	0	GPIO051 Pin Control 2 Register	400815A4h
GPIO	0	GPIO052 Pin Control 2 Register	400815A8h
GPIO	0	GPIO053 Pin Control 2 Register	400815ACh
GPIO	0	GPIO054 Pin Control 2 Register	400815B0h
GPIO	0	GPIO055 Pin Control 2 Register	400815B4h
GPIO	0	GPIO056 Pin Control 2 Register	400815B8h
GPIO	0	(GPIO057) Pin Control 2 Register	400815BCh
GPIO	0	GPIO060 Pin Control 2 Register	400815C0h
GPIO	0	GPIO061 Pin Control 2 Register	400815C4h
GPIO	0	GPIO062 Pin Control 2 Register	400815C8h
GPIO	0	GPIO063 Pin Control 2 Register	400815CCh
GPIO	0	GPIO064 Pin Control 2 Register	400815D0h
GPIO	0	GPIO065 Pin Control 2 Register	400815D4h
GPIO	0	GPIO066 Pin Control 2 Register	400815D8h
GPIO	0	GPIO067 Pin Control 2 Register	400815DCh
GPIO	0	GPIO070 Pin Control 2 Register	400815E0h
GPIO	0	GPIO071 Pin Control 2 Register	400815E4h
GPIO	0	GPIO072 Pin Control 2 Register	400815E8h
GPIO	0	GPIO073 Pin Control 2 Register	400815ECh
GPIO	0	GPIO100 Pin Control 2 Register	40081600h
GPIO	0	GPIO101 Pin Control 2 Register	40081604h
GPIO	0	GPIO102 Pin Control 2 Register	40081608h
GPIO	0	GPIO104 Pin Control 2 Register	40081610h
GPIO	0	GPIO105 Pin Control 2 Register	40081614h
GPIO	0	GPIO106 Pin Control 2 Register	40081618h
GPIO	0	GPIO107 Pin Control 2 Register	4008161Ch
GPIO	0	GPIO110 Pin Control 2 Register	40081620h
GPIO	0	GPIO111 Pin Control 2 Register	40081624h
GPIO	0	GPIO112 Pin Control 2 Register	40081628h
GPIO	0	GPIO113 Pin Control 2 Register	4008162Ch
GPIO	0	GPIO114 Pin Control 2 Register	40081630h
GPIO	0	GPIO115 Pin Control 2 Register	40081634h
GPIO	0	GPIO120 Pin Control 2 Register	40081640h
GPIO	0	GPIO121 Pin Control 2 Register	40081644h
GPIO	0	GPIO122 Pin Control 2 Register	40081648h
GPIO	0	GPIO123 Pin Control 2 Register	4008164Ch
GPIO	0	GPIO124 Pin Control 2 Register	40081650h

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Block	Instance	Register	Register Address
GPIO	0	GPIO125 Pin Control 2 Register	40081654h
GPIO	0	GPIO126 Pin Control 2 Register	40081658h
GPIO	0	GPIO127 Pin Control 2 Register	4008165Ch
GPIO	0	GPIO130 Pin Control 2 Register	40081660h
GPIO	0	GPIO131 Pin Control 2 Register	40081664h
GPIO	0	GPIO132 Pin Control 2 Register	40081668h
GPIO	0	GPIO133 Pin Control 2 Register	4008166Ch
GPIO	0	GPIO134 Pin Control 2 Register	40081670h
GPIO	0	GPIO135 Pin Control 2 Register	40081674h
GPIO	0	GPIO140 Pin Control 2 Register	40081680h
GPIO	0	GPIO141 Pin Control 2 Register	40081684h
GPIO	0	GPIO142 Pin Control 2 Register	40081688h
GPIO	0	GPIO143 Pin Control 2 Register	4008168Ch
GPIO	0	GPIO144 Pin Control 2 Register	40081690h
GPIO	0	GPIO145 Pin Control 2 Register	40081694h
GPIO	0	GPIO146 Pin Control 2 Register	40081698h
GPIO	0	GPIO147 Pin Control 2 Register	4008169Ch
GPIO	0	GPIO150 Pin Control 2 Register	400816A0h
GPIO	0	GPIO151 Pin Control 2 Register	400816A4h
GPIO	0	GPIO152 Pin Control 2 Register	400816A8h
GPIO	0	GPIO153 Pin Control 2 Register	400816ACh
GPIO	0	GPIO154 Pin Control 2 Register	400816B0h
GPIO	0	GPIO155 Pin Control 2 Register	400816B4h
GPIO	0	GPIO156 Pin Control 2 Register	400816B8h
GPIO	0	GPIO157 Pin Control 2 Register	400816BCh
GPIO	0	GPIO160 Pin Control 2 Register	400816C0h
GPIO	0	GPIO161 Pin Control 2 Register	400816C4h
GPIO	0	GPIO162 Pin Control 2 Register	400816C8h
GPIO	0	GPIO163 Pin Control 2 Register	400816CCh
GPIO	0	GPIO165 Pin Control 2 Register	400816D4h
GPIO	0	GPIO166 Pin Control 2 Register	400816D8h
GPIO	0	GPIO170 Pin Control 2 Register	400816E0h
GPIO	0	GPIO171 Pin Control 2 Register	400816E4h
GPIO	0	GPIO172 Pin Control 2 Register	400816E8h
GPIO	0	GPIO173 Pin Control 2 Register	400816ECh
GPIO	0	GPIO174 Pin Control 2 Register	400816F0h
GPIO	0	GPIO175 Pin Control 2 Register	400816F4h
GPIO	0	GPIO200 Pin Control 2 Register	40081700h
GPIO	0	GPIO201 Pin Control 2 Register	40081704h
GPIO	0	GPIO202 Pin Control 2 Register	40081708h
GPIO	0	GPIO203 Pin Control 2 Register	4008170Ch
GPIO	0	GPIO204 Pin Control 2 Register	40081710h
GPIO	0	GPIO205 Pin Control 2 Register	40081714h

Block	Instance	Register	Register Address
GPIO	0	GPIO206 Pin Control 2 Register	40081718h
GPIO	0	GPIO207 Pin Control 2 Register	4008171Ch
GPIO	0	GPIO210 Pin Control 2 Register	40081720h
GPIO	0	GPIO211 Pin Control 2 Register	40081724h
GPIO	0	GPIO212 Pin Control 2 Register	40081728h
GPIO	0	GPIO213 Pin Control 2 Register	4008172Ch
GPIO	0	GPIO214 Pin Control 2 Register	40081730h
GPIO	0	GPIO215 Pin Control 2 Register	40081734h
GPIO	0	GPIO216 Pin Control 2 Register	40081738h
GPIO	0	GPIO217 Pin Control 2 Register	4008173Ch
GPIO	0	GPIO221 Pin Control 2 Register	40081744h
GPIO	0	GPIO222 Pin Control 2 Register	40081748h
GPIO	0	GPIO223 Pin Control 2 Register	4008174Ch
GPIO	0	GPIO224 Pin Control 2 Register	40081750h
GPIO	0	GPIO225 Pin Control 2 Register	40081754h
GPIO	0	GPIO226 Pin Control 2 Register	40081758h
GPIO	0	GPIO227 Pin Control 2 Register	4008175Ch
GPIO	0	GPIO230 Pin Control 2 Register	40081760h
GPIO	0	GPIO231 Pin Control 2 Register	40081764h
GPIO	0	GPIO233 Pin Control 2 Register	4008176Ch
GPIO	0	GPIO234 Pin Control 2 Register	40081770h
GPIO	0	GPIO240 Pin Control 2 Register	40081800h
GPIO	0	GPIO241 Pin Control 2 Register	40081804h
GPIO	0	GPIO242 Pin Control 2 Register	40081808h
GPIO	0	GPIO243 Pin Control 2 Register	4008180Ch
GPIO	0	GPIO244 Pin Control 2 Register	40081810h
GPIO	0	GPIO245 Pin Control 2 Register	40081814h
GPIO	0	GPIO246 Pin Control 2 Register	40081818h
GPIO	0	GPIO250 Pin Control 2 Register	40081820h
GPIO	0	GPIO253 Pin Control 2 Register	4008182Ch
GPIO	0	GPIO254 Pin Control 2 Register	40081830h
eFuse	0	Control Register	40082000h
eFuse	0	Manual Control Register	40082004h
eFuse	0	Manual Mode Address Register	40082006h
eFuse	0	Manual Mode Data Register	4008200Ch
eFuse	0	eFUSE Memory	40082010h
Mailbox	0	MBX_INDEX Register	400F0000h
Mailbox	0	MBX_DATA Register	400F0001h
Mailbox	0	HOST-to-EC Mailbox Register	400F0100h
Mailbox	0	EC-to-Host Mailbox Register	400F0104h
Mailbox	0	SMI Interrupt Source Register	400F0108h
Mailbox	0	SMI Interrupt Mask Register	400F010Ch
Mailbox	0	Mailbox register [3:0]	400F0110h

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Block	Instance	Register	Register Address
Mailbox	0	Mailbox register [7:4]	400F0114h
Mailbox	0	Mailbox register [B:8]	400F0118h
Mailbox	0	Mailbox register [F:C]	400F011Ch
Mailbox	0	Mailbox register [13:10]	400F0120h
Mailbox	0	Mailbox register [17:14]	400F0124h
Mailbox	0	Mailbox register [1B:18]	400F0128h
Mailbox	0	Mailbox register [1F:1C]	400F012Ch
8042	0	EC_HOST Data / AUX Data Register	400F0400h
8042	0	Keyboard Status Read Register	400F0404h
8042	0	HOST2EC Data Register	400F0500h
8042	0	EC Data Register	400F0500h
8042	0	EC Keyboard Status Register	400F0504h
8042	0	Keyboard Control Register	400F0508h
8042	0	EC AUX Data Register	400F050Ch
8042	0	PCOBF Register	400F0514h
8042	0	Activate Register	400F0730h
ACPI EC Channel	0	ACPI OS Data Register Byte 0 Register	400F0800h
ACPI EC Channel	0	ACPI OS Data Register Byte 1 Register	400F0801h
ACPI EC Channel	0	ACPI OS Data Register Byte 2 Register	400F0802h
ACPI EC Channel	0	ACPI OS Data Register Byte 3 Register	400F0803h
ACPI EC Channel	0	ACPI OS COMMAND Register	400F0804h
ACPI EC Channel	0	OS STATUS OS Register	400F0804h
ACPI EC Channel	0	OS Byte Control Register	400F0805h
ACPI EC Channel	0	Reserved	400F0806h
ACPI EC Channel	0	Reserved	400F0807h
ACPI EC Channel	0	EC2OS Data EC Byte 0 Register	400F0900h
ACPI EC Channel	0	EC2OS Data EC Byte 1 Register	400F0901h
ACPI EC Channel	0	EC2OS Data EC Byte 2 Register	400F0902h
ACPI EC Channel	0	EC2OS Data EC Byte 3 Register	400F0903h
ACPI EC Channel	0	EC STATUS Register	400F0904h
ACPI EC Channel	0	EC Byte Control Register	400F0905h
ACPI EC Channel	0	Reserved	400F0906h
ACPI EC Channel	0	Reserved	400F0907h
ACPI EC Channel	0	OS2EC Data EC Byte 0 Register	400F0908h
ACPI EC Channel	0	OS2EC Data EC Byte 1 Register	400F0909h
ACPI EC Channel	0	OS2EC Data EC Byte 2 Register	400F090Ah
ACPI EC Channel	0	OS2EC Data EC Byte 3 Register	400F090Bh
ACPI EC Channel	1	ACPI OS Data Register Byte 0 Register	400F0C00h
ACPI EC Channel	1	ACPI OS Data Register Byte 1 Register	400F0C01h
ACPI EC Channel	1	ACPI OS Data Register Byte 2 Register	400F0C02h
ACPI EC Channel	1	ACPI OS Data Register Byte 3 Register	400F0C03h
ACPI EC Channel	1	ACPI OS COMMAND Register	400F0C04h
ACPI EC Channel	1	OS STATUS OS Register	400F0C04h

Block	Instance	Register	Register Address
ACPI EC Channel	1	OS Byte Control Register	400F0C05h
ACPI EC Channel	1	Reserved	400F0C06h
ACPI EC Channel	1	Reserved	400F0C07h
ACPI EC Channel	1	EC2OS Data EC Byte 0 Register	400F0D00h
ACPI EC Channel	1	EC2OS Data EC Byte 1 Register	400F0D01h
ACPI EC Channel	1	EC2OS Data EC Byte 2 Register	400F0D02h
ACPI EC Channel	1	EC2OS Data EC Byte 3 Register	400F0D03h
ACPI EC Channel	1	EC STATUS Register	400F0D04h
ACPI EC Channel	1	EC Byte Control Register	400F0D05h
ACPI EC Channel	1	Reserved	400F0D06h
ACPI EC Channel	1	Reserved	400F0D07h
ACPI EC Channel	1	OS2EC Data EC Byte 0 Register	400F0D08h
ACPI EC Channel	1	OS2EC Data EC Byte 1 Register	400F0D09h
ACPI EC Channel	1	OS2EC Data EC Byte 2 Register	400F0D0Ah
ACPI EC Channel	1	OS2EC Data EC Byte 3 Register	400F0D0Bh
ACPI EC Channel	2	ACPI OS Data Register Byte 0 Register	400F1000h
ACPI EC Channel	2	ACPI OS Data Register Byte 1 Register	400F1001h
ACPI EC Channel	2	ACPI OS Data Register Byte 2 Register	400F1002h
ACPI EC Channel	2	ACPI OS Data Register Byte 3 Register	400F1003h
ACPI EC Channel	2	ACPI OS COMMAND Register	400F1004h
ACPI EC Channel	2	OS STATUS OS Register	400F1004h
ACPI EC Channel	2	OS Byte Control Register	400F1005h
ACPI EC Channel	2	Reserved	400F1006h
ACPI EC Channel	2	Reserved	400F1007h
ACPI EC Channel	2	EC2OS Data EC Byte 0 Register	400F1100h
ACPI EC Channel	2	EC2OS Data EC Byte 1 Register	400F1101h
ACPI EC Channel	2	EC2OS Data EC Byte 2 Register	400F1102h
ACPI EC Channel	2	EC2OS Data EC Byte 3 Register	400F1103h
ACPI EC Channel	2	EC STATUS Register	400F1104h
ACPI EC Channel	2	EC Byte Control Register	400F1105h
ACPI EC Channel	2	Reserved	400F1106h
ACPI EC Channel	2	Reserved	400F1107h
ACPI EC Channel	2	OS2EC Data EC Byte 0 Register	400F1108h
ACPI EC Channel	2	OS2EC Data EC Byte 1 Register	400F1109h
ACPI EC Channel	2	OS2EC Data EC Byte 2 Register	400F110Ah
ACPI EC Channel	2	OS2EC Data EC Byte 3 Register	400F110Bh
ACPI EC Channel	3	ACPI OS Data Register Byte 0 Register	400F1400h
ACPI EC Channel	3	ACPI OS Data Register Byte 1 Register	400F1401h
ACPI EC Channel	3	ACPI OS Data Register Byte 2 Register	400F1402h
ACPI EC Channel	3	ACPI OS Data Register Byte 3 Register	400F1403h
ACPI EC Channel	3	ACPI OS COMMAND Register	400F1404h
ACPI EC Channel	3	OS STATUS OS Register	400F1404h
ACPI EC Channel	3	OS Byte Control Register	400F1405h

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Block	Instance	Register	Register Address
ACPI EC Channel	3	Reserved	400F1406h
ACPI EC Channel	3	Reserved	400F1407h
ACPI EC Channel	3	EC2OS Data EC Byte 0 Register	400F1500h
ACPI EC Channel	3	EC2OS Data EC Byte 1 Register	400F1501h
ACPI EC Channel	3	EC2OS Data EC Byte 2 Register	400F1502h
ACPI EC Channel	3	EC2OS Data EC Byte 3 Register	400F1503h
ACPI EC Channel	3	EC STATUS Register	400F1504h
ACPI EC Channel	3	EC Byte Control Register	400F1505h
ACPI EC Channel	3	Reserved	400F1506h
ACPI EC Channel	3	Reserved	400F1507h
ACPI EC Channel	3	OS2EC Data EC Byte 0 Register	400F1508h
ACPI EC Channel	3	OS2EC Data EC Byte 1 Register	400F1509h
ACPI EC Channel	3	OS2EC Data EC Byte 2 Register	400F150Ah
ACPI EC Channel	3	OS2EC Data EC Byte 3 Register	400F150Bh
ACPI EC Channel	4	ACPI OS Data Register Byte 0 Register	400F1800h
ACPI EC Channel	4	ACPI OS Data Register Byte 1 Register	400F1801h
ACPI EC Channel	4	ACPI OS Data Register Byte 2 Register	400F1802h
ACPI EC Channel	4	ACPI OS Data Register Byte 3 Register	400F1803h
ACPI EC Channel	4	ACPI OS COMMAND Register	400F1804h
ACPI EC Channel	4	OS STATUS OS Register	400F1804h
ACPI EC Channel	4	OS Byte Control Register	400F1805h
ACPI EC Channel	4	Reserved	400F1806h
ACPI EC Channel	4	Reserved	400F1807h
ACPI EC Channel	4	EC2OS Data EC Byte 0 Register	400F1900h
ACPI EC Channel	4	EC2OS Data EC Byte 1 Register	400F1901h
ACPI EC Channel	4	EC2OS Data EC Byte 2 Register	400F1902h
ACPI EC Channel	4	EC2OS Data EC Byte 3 Register	400F1903h
ACPI EC Channel	4	EC STATUS Register	400F1904h
ACPI EC Channel	4	EC Byte Control Register	400F1905h
ACPI EC Channel	4	Reserved	400F1906h
ACPI EC Channel	4	Reserved	400F1907h
ACPI EC Channel	4	OS2EC Data EC Byte 0 Register	400F1908h
ACPI EC Channel	4	OS2EC Data EC Byte 1 Register	400F1909h
ACPI EC Channel	4	OS2EC Data EC Byte 2 Register	400F190Ah
ACPI EC Channel	4	OS2EC Data EC Byte 3 Register	400F190Bh
ACPI PM1	0	Power Management 1 Status 1 Register	400F1C00h
ACPI PM1	0	Power Management 1 Status 2 Register	400F1C01h
ACPI PM1	0	Power Management 1 Enable 1 Register	400F1C02h
ACPI PM1	0	Power Management 1 Enable 2 Register	400F1C03h
ACPI PM1	0	Power Management 1 Control 1 Register	400F1C04h
ACPI PM1	0	Power Management 1 Control 2 Register	400F1C05h
ACPI PM1	0	Power Management 2 Control 1 Register	400F1C06h
ACPI PM1	0	Power Management 2 Control 2 Register	400F1C07h

Block	Instance	Register	Register Address
ACPI PM1	0	Power Management 1 Status 1 Register	400F1D00h
ACPI PM1	0	Power Management 1 Status 2 Register	400F1D01h
ACPI PM1	0	Power Management 1 Enable 1 Register	400F1D02h
ACPI PM1	0	Power Management 1 Enable 2 Register	400F1D03h
ACPI PM1	0	Power Management 1 Control 1 Register	400F1D04h
ACPI PM1	0	Power Management 1 Control 2 Register	400F1D05h
ACPI PM1	0	Power Management 2 Control 1 Register	400F1D06h
ACPI PM1	0	Power Management 2 Control 2 Register	400F1D07h
ACPI PM1	0	EC_PM_STS Register	400F1D10h
Port92-Legacy	0	Port 92 Register	400F2000h
Port92-Legacy	0	GATEA20 Control Register	400F2100h
Port92-Legacy	0	SETGA20L Register	400F2108h
Port92-Legacy	0	RSTGA20L Register	400F210Ch
Port92-Legacy	0	Port 92 Enable	400F2330h
UART	0	Receive Buffer Register	400F2400h
UART	0	Transmit Buffer Register	400F2400h
UART	0	Programmable Baud Rate Generator LSB Register	400F2400h
UART	0	Programmable Baud Rate Generator MSB Register	400F2401h
UART	0	Interrupt Enable Register	400F2401h
UART	0	FIFO Control Register	400F2402h
UART	0	Interrupt Identification Register	400F2402h
UART	0	Line Control Register	400F2403h
UART	0	Modem Control Register	400F2404h
UART	0	Line Status Register	400F2405h
UART	0	Modem Status Register	400F2406h
UART	0	Scratchpad Register	400F2407h
UART	0	Activate Register	400F2730h
UART	0	Configuration Select Register	400F27F0h
UART	1	Receive Buffer Register	400F2800h
UART	1	Transmit Buffer Register	400F2800h
UART	1	Programmable Baud Rate Generator LSB Register	400F2800h
UART	1	Programmable Baud Rate Generator MSB Register	400F2801h
UART	1	Interrupt Enable Register	400F2801h
UART	1	FIFO Control Register	400F2802h
UART	1	Interrupt Identification Register	400F2802h
UART	1	Line Control Register	400F2803h
UART	1	Modem Control Register	400F2804h
UART	1	Line Status Register	400F2805h
UART	1	Modem Status Register	400F2806h
UART	1	Scratchpad Register	400F2807h

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Block	Instance	Register	Register Address
UART	1	Activate Register	400F2B30h
UART	1	Configuration Select Register	400F2BF0h
LPC Interface	0	LPC Bus Monitor Register	400F3104h
LPC Interface	0	Host Bus Error Register	400F3108h
LPC Interface	0	EC SERIRQ Register	400F310Ch
LPC Interface	0	EC Clock Control Register	400F3110h
LPC Interface	0	MCHP Test Register	400F3114h
LPC Interface	0	MCHP Test Register	400F3118h
LPC Interface	0	BAR Inhibit Register	400F3120h
LPC Interface	0	TEST	400F3124h
LPC Interface	0	TEST	400F3128h
LPC Interface	0	TEST	400F312Ch
LPC Interface	0	LPC BAR Init Register	400F3130h
LPC Interface	0	SRAM 0 BAR	400F31F8h
LPC Interface	0	SRAM 1 BAR	400F31FCh
LPC Interface	0	LPC Activate Register	400F3330h
LPC Interface	0	SERIRQ IRQ0 Configuration	400F3340h
LPC Interface	0	SERIRQ IRQ1 Configuration	400F3341h
LPC Interface	0	SERIRQ IRQ2 Configuration	400F3342h
LPC Interface	0	SERIRQ IRQ3 Configuration	400F3343h
LPC Interface	0	SERIRQ IRQ4 Configuration	400F3344h
LPC Interface	0	SERIRQ IRQ5 Configuration	400F3345h
LPC Interface	0	SERIRQ IRQ6 Configuration	400F3346h
LPC Interface	0	SERIRQ IRQ7 Configuration	400F3347h
LPC Interface	0	SERIRQ IRQ8 Configuration	400F3348h
LPC Interface	0	SERIRQ IRQ9 Configuration	400F3349h
LPC Interface	0	SERIRQ IRQ10 Configuration	400F334Ah
LPC Interface	0	SERIRQ IRQ11 Configuration	400F334Bh
LPC Interface	0	SERIRQ IRQ12 Configuration	400F334Ch
LPC Interface	0	SERIRQ IRQ13 Configuration	400F334Dh
LPC Interface	0	SERIRQ IRQ14 Configuration	400F334Eh
LPC Interface	0	SERIRQ IRQ15 Configuration	400F334Fh
LPC Interface	0	LPC Interface BAR	400F3360h
LPC Interface	0	Mailbox BAR	400F3364h
LPC Interface	0	8042 Emulated Keyboard Controller BAR	400F3368h
LPC Interface	0	ACPI EC Channel 0 BAR	400F336Ch
LPC Interface	0	ACPI EC Channel 1 BAR	400F3370h
LPC Interface	0	ACPI EC Channel 2 BAR	400F3374h
LPC Interface	0	ACPI EC Channel 3 BAR	400F3378h
LPC Interface	0	ACPI EC Channel 4 BAR	400F337Ch
LPC Interface	0	ACPI PM1 BAR	400F3380h
LPC Interface	0	Legacy (Fast Keyboard) BAR	400F3384h
LPC Interface	0	UART 0 BAR	400F3388h

Block	Instance	Register	Register Address
LPC Interface	0	UART 1 BAR	400F338Ch
LPC Interface	0	EMI 0 BAR	400F3390h
LPC Interface	0	EMI 1 BAR	400F3394h
LPC Interface	0	EMI 2 BAR	400F3398h
LPC Interface	0	BIOS Debug Port (Port 80) 0 BAR	400F339Ch
LPC Interface	0	BIOS Debug Port (Port 80) 1 BAR	400F33A0h
LPC Interface	0	RTC BAR	400F33A4h
LPC Interface	0	SRAM BAR 0	400F33B0h
LPC Interface	0	SRAM BAR 1	400F33B8h
LPC Interface	0	Mailbox	400F33C0h
LPC Interface	0	ACPI EC Channel 0	400F33C6h
LPC Interface	0	ACPI EC Channel 1	400F33CCh
LPC Interface	0	ACPI EC Channel 2	400F33D2h
LPC Interface	0	ACPI EC Channel 3	400F33D8h
LPC Interface	0	ACPI EC Channel 4	400F33DEh
LPC Interface	0	Embedded Memory Interface (EMI) 0	400F33E4h
LPC Interface	0	Embedded Memory Interface (EMI) 1	400F33EAh
LPC Interface	0	Embedded Memory Interface (EMI) 2	400F33F0h
eSPI IO Component	0	Peripheral Channel Last Cycle Register	400F3500h
eSPI IO Component	0	Peripheral Channel Error Address Register	400F350Ch
eSPI IO Component	0	Peripheral Channel Status Register	400F3514h
eSPI IO Component	0	Peripheral Channel Interrupt Enable Register	400F3518h
eSPI IO Component	0	Reserved	400F351Ch
eSPI IO Component	0	BAR Inhibit Register	400F3520h
eSPI IO Component	0	eSPI BAR Init Register	400F3528h
eSPI IO Component	0	EC IRQ Register	400F352Ch
eSPI IO Component	0	TEST	400F3530h
eSPI IO Component	0	eSPI IO Component BAR	400F3534h
eSPI IO Component	0	eSPI Memory Component BAR	400F3538h
eSPI IO Component	0	Mailbox BAR	400F353Ch
eSPI IO Component	0	8042 Emulated Keyboard Controller BAR	400F3540h
eSPI IO Component	0	ACPI EC Channel 0 BAR	400F3544h
eSPI IO Component	0	ACPI EC Channel 1 BAR	400F3548h
eSPI IO Component	0	ACPI EC Channel 2 BAR	400F354Ch
eSPI IO Component	0	ACPI EC Channel 3 BAR	400F3550h
eSPI IO Component	0	ACPI EC Channel 4 BAR	400F3554h
eSPI IO Component	0	ACPI PM1 BAR	400F3558h
eSPI IO Component	0	Legacy (Fast Keyboard) BAR	400F355Ch
eSPI IO Component	0	UART 0 BAR	400F3560h
eSPI IO Component	0	UART 1 BAR	400F3564h
eSPI IO Component	0	Embedded Memory Interface (EMI) 0 BAR	400F3568h
eSPI IO Component	0	Embedded Memory Interface (EMI) 1 BAR	400F356Ch
eSPI IO Component	0	Embedded Memory Interface (EMI) 2 BAR	400F3570h

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Block	Instance	Register	Register Address
eSPI IO Component	0	BIOS Debug Port (Port 80) 0 BAR	400F3574h
eSPI IO Component	0	BIOS Debug Port (Port 80) 1 BAR	400F3578h
eSPI IO Component	0	RTC BAR	400F357Ch
eSPI IO Component	0	LTR Peripheral Status Register	400F3620h
eSPI IO Component	0	LTR Peripheral Enable Register	400F3624h
eSPI IO Component	0	LTR Peripheral Control Register	400F3628h
eSPI IO Component	0	LTR Peripheral Message Register	400F362Ch
eSPI IO Component	0	OOB Channel Receive Address Register	400F3640h
eSPI IO Component	0	OOB Channel Transmit Address Register	400F3648h
eSPI IO Component	0	OOB Channel Receive Length Register	400F3650h
eSPI IO Component	0	OOB Channel Transmit Length Register	400F3654h
eSPI IO Component	0	OOB Channel Receive Control Register	400F3658h
eSPI IO Component	0	OOB Channel Receive Interrupt Enable Register	400F365Ch
eSPI IO Component	0	OOB Channel Receive Status Register	400F3660h
eSPI IO Component	0	OOB Channel Transmit Control Register	400F3664h
eSPI IO Component	0	OOB Channel Transmit Interrupt Enable Register	400F3668h
eSPI IO Component	0	OOB Channel Transmit Status Register	400F366Ch
eSPI IO Component	0	Flash Access Channel Flash Address Register	400F3680h
eSPI IO Component	0	Flash Access Channel Buffer Address Register	400F3688h
eSPI IO Component	0	Flash Access Channel Transfer Length Register	400F3690h
eSPI IO Component	0	Flash Access Channel Control Register	400F3694h
eSPI IO Component	0	Flash Access Channel Interrupt Enable Register	400F3698h
eSPI IO Component	0	Flash Access Channel Configuration Register	400F369Ch
eSPI IO Component	0	Flash Access Channel Status Register	400F36A0h
eSPI IO Component	0	Virtual Wire Status	400F36B0h
eSPI IO Component	0	eSPI Capabilities ID Register	400F36E0h
eSPI IO Component	0	eSPI Capabilities Global Capabilities 0 Register	400F36E1h
eSPI IO Component	0	eSPI Capabilities Global Capabilities 1 Register	400F36E2h
eSPI IO Component	0	eSPI Peripheral Channel Capabilities Register	400F36E3h
eSPI IO Component	0	eSPI Virtual Wire Channel Capabilities Register	400F36E4h
eSPI IO Component	0	eSPI OOB Channel Capabilities Register	400F36E5h
eSPI IO Component	0	eSPI Flash Channel Capabilities Register	400F36E6h
eSPI IO Component	0	eSPI Peripheral Channel Ready Register	400F36E7h
eSPI IO Component	0	eSPI OOB Channel Ready Register	400F36E8h
eSPI IO Component	0	eSPI Flash Channel Ready Register	400F36E9h
eSPI IO Component	0	eSPI Reset Interrupt Status Register	400F36EAh
eSPI IO Component	0	eSPI Reset Interrupt Enable Register	400F36EBh
eSPI IO Component	0	PLTRST Source Register	400F36ECh
eSPI IO Component	0	eSPI Virtual Wire Channel Ready Register	400F36EDh
eSPI IO Component	0	eSPI Activate Register	400F3730h
eSPI IO Component	0	eSPI IO Component BAR	400F3734h
eSPI IO Component	0	eSPI Memory Component BAR	400F3738h
eSPI IO Component	0	Mailbox BAR	400F373Ch

Block	Instance	Register	Register Address
eSPI IO Component	0	8042 Emulated Keyboard Controller BAR	400F3740h
eSPI IO Component	0	ACPI EC Channel 0 BAR	400F3744h
eSPI IO Component	0	ACPI EC Channel 1 BAR	400F3748h
eSPI IO Component	0	ACPI EC Channel 2 BAR	400F374Ch
eSPI IO Component	0	ACPI EC Channel 3 BAR	400F3750h
eSPI IO Component	0	ACPI EC Channel 4 BAR	400F3754h
eSPI IO Component	0	ACPI PM1 BAR	400F3758h
eSPI IO Component	0	Legacy (Fast Keyboard) BAR	400F375Ch
eSPI IO Component	0	UART 0 BAR	400F3760h
eSPI IO Component	0	UART 1 BAR	400F3764h
eSPI IO Component	0	Embedded Memory Interface (EMI) 0 BAR	400F3768h
eSPI IO Component	0	Embedded Memory Interface (EMI) 1 BAR	400F376Ch
eSPI IO Component	0	Embedded Memory Interface (EMI) 2 BAR	400F3770h
eSPI IO Component	0	BIOS Debug Port (Port 80) 0 BAR	400F3774h
eSPI IO Component	0	BIOS Debug Port (Port 80) 1 BAR	400F3778h
eSPI IO Component	0	RTC BAR	400F3778h
eSPI IO Component	0	Mailbox SERIRQ 0	400F37ACh
eSPI IO Component	0	Mailbox SERIRQ 1	400F37ADh
eSPI IO Component	0	8042 SERIRQ 0	400F37AEh
eSPI IO Component	0	8042 SERIRQ 1	400F37AFh
eSPI IO Component	0	ACPI EC 0 SERIRQ	400F37B0h
eSPI IO Component	0	ACPI EC 1 SERIRQ	400F37B1h
eSPI IO Component	0	ACPI EC 2 SERIRQ	400F37B2h
eSPI IO Component	0	ACPI EC 3 SERIRQ	400F37B3h
eSPI IO Component	0	ACPI EC 4 SERIRQ	400F37B4h
eSPI IO Component	0	UART 0 SERIRQ	400F37B5h
eSPI IO Component	0	UART 1 SERIRQ	400F37B6h
eSPI IO Component	0	EMI 0 SERIRQ 0	400F37B7h
eSPI IO Component	0	EMI 0 SERIRQ 1	400F37B8h
eSPI IO Component	0	EMI 1 SERIRQ 0	400F37B9h
eSPI IO Component	0	EMI 1 SERIRQ 1	400F37BAh
eSPI IO Component	0	EMI 2 SERIRQ 0	400F37BBh
eSPI IO Component	0	EMI 2 SERIRQ 1	400F37BCh
eSPI IO Component	0	RTC SERIRQ	400F37BDh
eSPI IO Component	0	EC SERIRQ	400F37BEh
eSPI IO Component	0	eSPI Virtual Wire Error	400F37F0h
eSPI Memory Component	0	Mailbox BAR	400F3930h
eSPI Memory Component	0	ACPI EC Channel 0 BAR	400F393Ah
eSPI Memory Component	0	ACPI EC Channel 1 BAR	400F3944h
eSPI Memory Component	0	ACPI EC Channel 2 BAR	400F394Eh
eSPI Memory Component	0	ACPI EC Channel 3 BAR	400F3958h
eSPI Memory Component	0	ACPI EC Channel 4 BAR	400F3962h
eSPI Memory Component	0	Embedded Memory Interface (EMI) 0 BAR	400F396Ch

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Block	Instance	Register	Register Address
eSPI Memory Component	0	Embedded Memory Interface (EMI) 1 BAR	400F3976h
eSPI Memory Component	0	Embedded Memory Interface (EMI) 2 BAR	400F3980h
eSPI Memory Component	0	SRAM BAR 0	400F39ACh
eSPI Memory Component	0	SRAM BAR 1	400F39B6h
eSPI Memory Component	0	Bus Master Status Register	400F3A00h
eSPI Memory Component	0	Bus Master Interrupt Enable Register	400F3A04h
eSPI Memory Component	0	Bus Master Configuration Register	400F3A08h
eSPI Memory Component	0	Bus Master 1 Control Register	400F3A10h
eSPI Memory Component	0	Bus Master 1 Host Address Register	400F3A14h
eSPI Memory Component	0	Bus Master 1 Internal Address Register	400F3A1Ch
eSPI Memory Component	0	Bus Master 2 Control Register	400F3A24h
eSPI Memory Component	0	Bus Master 2 Host Address Register	400F3A28h
eSPI Memory Component	0	Bus Master 2 Internal Address Register	400F3A30h
eSPI Memory Component	0	Mailbox BAR	400F3B30h
eSPI Memory Component	0	ACPI EC Channel 0 BAR	400F3B3Ah
eSPI Memory Component	0	ACPI EC Channel 1 BAR	400F3B44h
eSPI Memory Component	0	ACPI EC Channel 2 BAR	400F3B4Eh
eSPI Memory Component	0	ACPI EC Channel 3 BAR	400F3B58h
eSPI Memory Component	0	ACPI EC Channel 4 BAR	400F3B62h
eSPI Memory Component	0	Embedded Memory Interface (EMI) 0 BAR	400F3B6Ch
eSPI Memory Component	0	Embedded Memory Interface (EMI) 1 BAR	400F3B76h
eSPI Memory Component	0	Embedded Memory Interface (EMI) 2 BAR	400F3B80h
eSPI Memory Component	0	SRAM BAR 0	400F3BACh
eSPI Memory Component	0	SRAM BAR 1	400F3BB6h
EMI	0	HOST-to-EC Mailbox Register	400F4000h
EMI	0	EC-to-HOST Mailbox Register	400F4001h
EMI	0	EC Address LSB Register	400F4002h
EMI	0	EC Address MSB Register	400F4003h
EMI	0	EC Data Byte 0 Register	400F4004h
EMI	0	EC Data Byte 1 Register	400F4005h
EMI	0	EC Data Byte 2 Register	400F4006h
EMI	0	EC Data Byte 3 Register	400F4007h
EMI	0	Interrupt Source LSB Register	400F4008h
EMI	0	Interrupt Source MSB Register	400F4009h
EMI	0	Interrupt Mask LSB Register	400F400Ah
EMI	0	Interrupt Mask MSB Register	400F400Bh
EMI	0	Application ID Register	400F400Ch
EMI	0	HOST-to-EC Mailbox Register	400F4100h
EMI	0	EC-to-HOST Mailbox Register	400F4101h
EMI	0	Memory Base Address 0 Register	400F4104h
EMI	0	Memory Read Limit 0 Register	400F4108h
EMI	0	Memory Write Limit 0 Register	400F410Ah
EMI	0	Memory Base Address 1 Register	400F410Ch

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Block	Instance	Register	Register Address
EMI	0	Memory Read Limit 1 Register	400F4110h
EMI	0	Memory Write Limit 1 Register	400F4112h
EMI	0	Interrupt Set Register	400F4114h
EMI	0	Host Clear Enable Register	400F4116h
EMI	1	HOST-to-EC Mailbox Register	400F4400h
EMI	1	EC-to-HOST Mailbox Register	400F4401h
EMI	1	EC Address LSB Register	400F4402h
EMI	1	EC Address MSB Register	400F4403h
EMI	1	EC Data Byte 0 Register	400F4404h
EMI	1	EC Data Byte 1 Register	400F4405h
EMI	1	EC Data Byte 2 Register	400F4406h
EMI	1	EC Data Byte 3 Register	400F4407h
EMI	1	Interrupt Source LSB Register	400F4408h
EMI	1	Interrupt Source MSB Register	400F4409h
EMI	1	Interrupt Mask LSB Register	400F440Ah
EMI	1	Interrupt Mask MSB Register	400F440Bh
EMI	1	Application ID Register	400F440Ch
EMI	1	HOST-to-EC Mailbox Register	400F4500h
EMI	1	EC-to-HOST Mailbox Register	400F4501h
EMI	1	Memory Base Address 0 Register	400F4504h
EMI	1	Memory Read Limit 0 Register	400F4508h
EMI	1	Memory Write Limit 0 Register	400F450Ah
EMI	1	Memory Base Address 1 Register	400F450Ch
EMI	1	Memory Read Limit 1 Register	400F4510h
EMI	1	Memory Write Limit 1 Register	400F4512h
EMI	1	Interrupt Set Register	400F4514h
EMI	1	Host Clear Enable Register	400F4516h
EMI	2	HOST-to-EC Mailbox Register	400F4800h
EMI	2	EC-to-HOST Mailbox Register	400F4801h
EMI	2	EC Address LSB Register	400F4802h
EMI	2	EC Address MSB Register	400F4803h
EMI	2	EC Data Byte 0 Register	400F4804h
EMI	2	EC Data Byte 1 Register	400F4805h
EMI	2	EC Data Byte 2 Register	400F4806h
EMI	2	EC Data Byte 3 Register	400F4807h
EMI	2	Interrupt Source LSB Register	400F4808h
EMI	2	Interrupt Source MSB Register	400F4809h
EMI	2	Interrupt Mask LSB Register	400F480Ah
EMI	2	Interrupt Mask MSB Register	400F480Bh
EMI	2	Application ID Register	400F480Ch
EMI	2	HOST-to-EC Mailbox Register	400F4900h
EMI	2	EC-to-HOST Mailbox Register	400F4901h
EMI	2	Memory Base Address 0 Register	400F4904h

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Block	Instance	Register	Register Address
EMI	2	Memory Read Limit 0 Register	400F4908h
EMI	2	Memory Write Limit 0 Register	400F490Ah
EMI	2	Memory Base Address 1 Register	400F490Ch
EMI	2	Memory Read Limit 1 Register	400F4910h
EMI	2	Memory Write Limit 1 Register	400F4912h
EMI	2	Interrupt Set Register	400F4914h
EMI	2	Host Clear Enable Register	400F4916h
Real Time Clock	0	Seconds Register	400F5000h
Real Time Clock	0	Seconds Alarm Register	400F5001h
Real Time Clock	0	Minutes Register	400F5002h
Real Time Clock	0	Minutes Alarm Register	400F5003h
Real Time Clock	0	Hours Register	400F5004h
Real Time Clock	0	Hours Alarm Register	400F5005h
Real Time Clock	0	Day of Week Register	400F5006h
Real Time Clock	0	Day of Month Register	400F5007h
Real Time Clock	0	Month Register	400F5008h
Real Time Clock	0	Year Register	400F5009h
Real Time Clock	0	Register A	400F500Ah
Real Time Clock	0	Register B	400F500Bh
Real Time Clock	0	Register C	400F500Ch
Real Time Clock	0	Register D	400F500Dh
Real Time Clock	0	Reserved	400F500Eh
Real Time Clock	0	Reserved	400F500Fh
Real Time Clock	0	RTC Control Register	400F5010h
Real Time Clock	0	Week Alarm Register	400F5014h
Real Time Clock	0	Daylight Savings Forward Register	400F5018h
Real Time Clock	0	Daylight Savings Backward Register	400F501Ch
Real Time Clock	0	TEST	400F5020h
Port 80	0	Host Data Register	400F8000h
Port 80	0	EC Data Register	400F8100h
Port 80	0	Configuration Register	400F8104h
Port 80	0	Status Register	400F8108h
Port 80	0	Count Register	400F810Ch
Port 80	0	Activate Register	400F8330h
Port 80	1	Host Data Register	400F8400h
Port 80	1	EC Data Register	400F8500h
Port 80	1	Configuration Register	400F8504h
Port 80	1	Status Register	400F8508h
Port 80	1	Count Register	400F850Ch
Port 80	1	Activate Register	400F8730h
eSPI Virtual Wires	0	MSVW00 Register	400F9C00h
eSPI Virtual Wires	0	MSVW01 Register	400F9C0Ch
eSPI Virtual Wires	0	MSVW02 Register	400F9C18h

Block	Instance	Register	Register Address
eSPI Virtual Wires	0	MSVW03 Register	400F9C24h
eSPI Virtual Wires	0	MSVW04 Register	400F9C30h
eSPI Virtual Wires	0	MSVW05 Register	400F9C3Ch
eSPI Virtual Wires	0	MSVW06 Register	400F9C48h
eSPI Virtual Wires	0	MSVW07 Register	400F9C54h
eSPI Virtual Wires	0	MSVW08 Register	400F9C60h
eSPI Virtual Wires	0	MSVW09 Register	400F9C6Ch
eSPI Virtual Wires	0	MSVW10 Register	400F9C78h
eSPI Virtual Wires	0	SMVW00 Register	400F9E00h
eSPI Virtual Wires	0	SMVW01 Register	400F9E08h
eSPI Virtual Wires	0	SMVW02 Register	400F9E10h
eSPI Virtual Wires	0	SMVW03 Register	400F9E18h
eSPI Virtual Wires	0	SMVW04 Register	400F9E20h
eSPI Virtual Wires	0	SMVW05 Register	400F9E28h
eSPI Virtual Wires	0	SMVW06 Register	400F9E30h
eSPI Virtual Wires	0	SMVW07 Register	400F9E38h
eSPI Virtual Wires	0	TEST	400F9FF0h
eSPI Virtual Wires	0	TEST	400F9FF2h
eSPI Virtual Wires	0	TEST	400F9FF8h
eSPI Virtual Wires	0	TEST	400F9FFAh
Global Configuration	0	Global Configuration Reserved	400FFF00h
Global Configuration	0	Logical Device Number	400FFF07h
Global Configuration	0	Device ID	400FFF20h
Global Configuration	0	Revision	400FFF21h
Global Configuration	0	TEST	400FFF24h
Global Configuration	0	TEST	400FFF28h
Global Configuration	0	TEST	400FFF29h
Global Configuration	0	TEST	400FFF2Ch

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4.0 POWER, CLOCKS, AND RESETS

4.1 Introduction

The Power, Clocks, and Resets (PCR) chapter identifies all the power supplies, clock sources, and reset inputs to the chip and defines all the derived power, clock, and reset signals. In addition, this section identifies Power, Clock, and Reset events that may be used to generate an interrupt event, as well as, the Chip Power Management Features.

4.2 References

No references have been cited for this chapter.

4.3 Interrupts

The Power, Clocks, and Resets logic generates no events

4.4 Power

TABLE 4-1: POWER SOURCE DEFINITIONS

Power Well	Nominal Voltage	Description	Source
VTR_REG	1.8V - 3.3V	This supply is used to derive the chip's core power.	Pin Interface
VTR_ANALOG	3.3V	3.3V Analog Power Supply. This is typically connected to the "Always-on" or "Suspend" supply rails in system. This supply must be on prior to the system RSMRST# signal being deasserted. This supply is used to power the chip's analog circuitry, including the reset generator.	Pin Interface
VTR_PLL	3.3V	3.3V Power Supply for the 48MHz PLL. This must be connected to the same supply as VTR_ANALOG.	Pin Interface
VFLT_PLL	3.3V	Filtered Power for the 48MHz PLL. This is connected to VTR_PLL through a capacitor.	Pin Interface
VTR1	3.3V or 1.8V	Variable voltage I/O Power Supply. Power supply for a bank of I/O pins. See Note 1. This supply must be 3.3V if an EEPROM is included.	Pin Interface:
VTR2	3.3V or 1.8V	Variable voltage I/O Power Supply. Power supply for a bank of I/O pins. See Note 1.	Pin Interface:
VTR3	3.3V or 1.8V	Variable voltage I/O Power Supply. Power supply for a bank of I/O pins. See Note 1.	Pin Interface:
VTR	1.2V	The main power well for internal logic	Internal regulator
Note 1: See Section 4.4.1, "I/O Rail Requirements" for connection requirements for VTRx			

TABLE 4-1: POWER SOURCE DEFINITIONS (CONTINUED)

Power Well	Nominal Voltage	Description	Source
VBAT	3.0V - 3.3V	System Battery Back-up Power Well. This is the “coin-cell” battery. GPIOs that share pins with VBAT signals are powered by this supply.	Pin Interface VBAT
VSS	0V	Digital Ground	Pin Interface
Note 1: See Section 4.4.1, "I/O Rail Requirements" for connection requirements for VTRx			

4.4.1 I/O RAIL REQUIREMENTS

All pins are powered by four power supply pins: VBAT, VTR1, VTR2 and VTR3. The VBAT supply must be 3V to 3.6V maximum, as shown in the following section. The VTRx pins, however, may be connected to either a 3.3V or a 1.8V power supply. The device must be able to determine the voltage when the internal RESET_SYS is de-asserted in order to configure the pins properly. The device remains in reset until VTR_ANALOG has ramped to 3.3V and VTR_REG has ramped to at least 1.6V. In addition, VTR1 must ramp to its desired voltage, 1.8V or 3.3V, in order for the Boundary Scan strap to be detected properly, and VTR2 must ramp to its desired voltage, 1.8V or 3.3V, in order for the Shared SPI/eSPI strap to be detected properly, or for booting from a Shared SPI Flash. VTR3 must ramp to 1.8V before booting of the eSPI Flash Channel can be executed.

Software can determine whether a VTRx region is 1.8V or 3.3V by examining the GPIO Bank Power Register.

If a power rail is not powered and stable when RESET_SYS is de-asserted and is not required for booting, software can configure the pins on that bank appropriately by setting the corresponding bit in the GPIO Bank Power Register, once software can determine that the power supply is up and stable. All GPIOs in the bank must be left in their default state and not modified until the Bank Power is configured properly.

4.4.2 BATTERY CIRCUIT REQUIREMENTS

VBAT must always be present if VTR_ANALOG is present.

Microchip recommends removing all power sources to the device defined in Table 4-1, "Power Source Definitions" and all external voltage references defined in Table 4-2, "Voltage Reference Definitions" before removing and replacing the battery. In addition, upon removing the battery, discharge the battery pin before replacing the battery.

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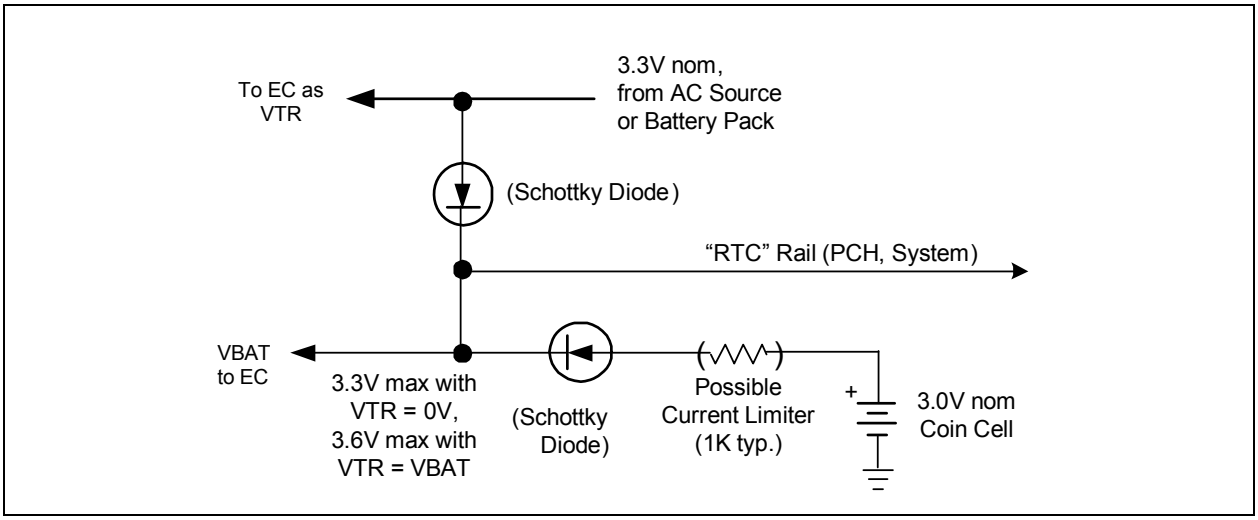
The following external circuit is recommended to fulfill this requirement:

FIGURE 4-1: RECOMMENDED BATTERY CIRCUIT



4.4.3 VOLTAGE REFERENCES

Table 4-2 lists the External Voltage References to which the MEC170x provides high impedance interfaces.

TABLE 4-2: VOLTAGE REFERENCE DEFINITIONS

Power Well	Nominal Input Voltage	Scaling Ratio	Nominal Monitored Voltage	Description	Source
VREF_VTT	Variable	n/a	Variable	Processor Voltage External Voltage Reference Used to scale Processor Interface signals. (See Note 1)	Pin Interface
VREF_ADC	Variable	n/a	Variable	ADC Reference Voltage	Pin Interface
Note 1: The MUX_CONTROL field for GPIO044 should be set to GPIO in order to minimize leakage current when VREF_VTT is not required (e.g., when neither PECI nor AMD-TSI are active).					

4.4.4 POWER GOOD SIGNALS

The power good timing and thresholds are defined in the Section 51.9, "VCC_PWRGD Timing".

TABLE 4-3: POWER GOOD SIGNAL DEFINITIONS

Power Good Signal	Description	Source
VCC_PWRGD	VCC_PWRGD is an input signal used to indicate when the main system power rail voltage is on and stable.	VCC_PWRGD Input pin
PWROK	PWROK is an output signal used to indicate that the main system power rail voltage is on and the Host may access Host devices in the EC.	The PWROK pin is asserted high whenever both the VCC_PWRGD input is asserted high and the PWR_INV bit in the Power Reset Control Register is de-asserted low.

TABLE 4-3: POWER GOOD SIGNAL DEFINITIONS (CONTINUED)

Power Good Signal	Description	Source
PRIMPWROK	PRIMPWROK is an input signal that is asserted when the four Primary power rails in an Intel system (VCC_Prim 1.8V, VCC_Prim 3.3V, VCCPRIM_CORE and VCC_Prim 1.0V) are up. It is only used by Boot ROM code when booting over the eSPI Flash Channel.	GPIO227/SHD_IO2 pin. There is no special hardware associated with this signal

4.4.5 SYSTEM POWER SEQUENCING

The following table defines the behavior of the main power rails in each of the defined ACPI power states.

TABLE 4-4: TYPICAL POWER SUPPLIES VS. ACPI POWER STATES

Supply Name	ACPI Power State						Description
	S0 (FULL ON)	S1 (POS)	S3 (STR)	S4 (STD)	S5 (Soft Off)	G3 (MECH Off)	
VTR	ON	ON	ON	ON	ON	OFF	“Always-on” Supply
VBAT	ON	ON	ON	ON	ON	ON	Battery Back-up Supply

4.5 Clocks

The following section defines the clocks that are generated and derived.

4.5.1 RAW CLOCK SOURCES

The table defines raw clocks that are either generated externally or via an internal oscillator.

TABLE 4-5: SOURCE CLOCK DEFINITIONS

Clock Name	Frequency	Description	Source
32KHZ_IN	32.768 kHz (nominal)	Single-ended external clock input pin	32KHZ_IN pin
32.768 kHz Crystal Oscillator	32.768 kHz	A 32.768 kHz parallel resonant crystal connected between the XTAL1 and XTAL2 pins. The accuracy of the clock depends on the accuracy of the crystal and the characteristics of the analog components used as part of the oscillator The crystal oscillator source can bypass the crystal with a single-ended clock input. This option is configured with the Clock Enable Register.	Pin Interface (XTAL1 and XTAL2) When used singled-ended, pin XTAL2
32.768 kHz Silicon Oscillator	32.768 kHz	32.768 kHz low power Internal Oscillator. The frequency is 32.768KHz ±2%	Internal Oscillator powered by VBAT

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TABLE 4-5: SOURCE CLOCK DEFINITIONS (CONTINUED)

Clock Name	Frequency	Description	Source
32 MHz Ring Oscillator	32MHz	The 32MHz Ring Oscillator is used to supply a clock for the 48MHz main clock domain while the 48MHz PLL is not locked. Its frequency can range from 16Mhz to 48MHz.	Powered by VTR.
48 MHz PLL	48MHz	The 48 MHz Phase Locked Loop generates a 48MHz clock locked to the Always-on Internal 32KHz Clock Source	Powered by VTR. May be stopped by Chip Power Management Features.
LPC Clock	18MHz to 33MHz	LPC bus clock This clock is only used in the LPC interface.	PCI_CLK pin
eSPI Clock	20MHz to 50MHz	eSPI bus clock This clock is only used in the eSPI interface.	ESPI_CLK pin

4.5.2 CLOCK DOMAINS

TABLE 4-6: CLOCK DOMAIN DEFINITIONS

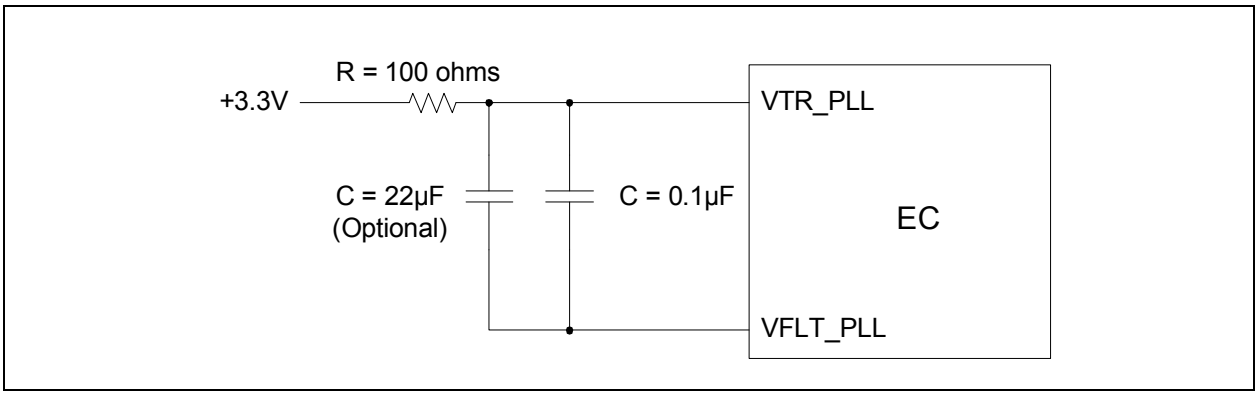
Clock Domain	Description
32KHz	The clock source used by internal blocks that require an always-on low speed clock
48MHz	The main clock source used by most internal blocks
96MHz	The clock source used by the Public Key Cryptographic Engine. It is derived from the same PLL as the 48MHz clock source.
100KHz	A low-speed clock derived from the 48MHz clock domain. Used as a time base for PWMs and Tachs.
EC_CLK	The clock used by the EC processor. The frequency is determined by the Processor Clock Control Register.

4.5.3 48MHZ PLL

The 48MHz clock domain is primarily driven by a 48MHz PLL, which derives 48MHz from the 32KHz always-on clock domain. In Heavy Sleep mode, the 48MHz PLL is shut off. When the PLL is started, either from waking from the Heavy Sleep mode, or after a Power On Reset, the 32MHz ring oscillator becomes the clock source for the 48MHz clock domain until the PLL is stable. The PLL becomes stable after about 3ms; until that time, the 48MHz clock domain may range from 16MHz to 48MHz, as this is the accuracy range of the 32MHz ring.

The PLL requires its own power 3.3V power supply, VTR_PLL. This power rail must be active and stable no later than the latest of VTR_REG and VTR_ANALOG. There is no hardware detection of VTR_PLL power good in the reset generator. The VTR_PLL supply must be filtered, as shown in Figure 4-2, "Power Supply Filtering for PLL". There is no special ground connection required for the PLL.

FIGURE 4-2: POWER SUPPLY FILTERING FOR PLL



4.5.4 32KHZ CLOCK SWITCHING

The 32KHz Clock Domain may be sourced by a crystal oscillator, using an external crystal, by an internal 32KHz oscillator, or from a single-ended clock input. The external single-ended clock source can itself be sourced either from the 32KHZ_IN signal that is a GPIO alternate function or from the XTAL2 crystal pin. The Clock Enable Register is used to configure the source for the 32 kHz clock domain.

When VTR is off, the 32 kHz clock domain can be disabled, for lowest standby power, or it can be kept running in order to provide a clock for the Real Time Clock or the Week Timer.

An external single-ended clock input for 32KHZ_IN may be supplied by any accurate 32KHz clock source in the system. The SUSCLK output from the chipset may be used as the 32KHz source whenever RSMRST# is de-asserted. See chipset documentation for details on the use of SUSCLK.

If firmware switches the 32KHz clock source, the 48MHz PLL will be shut off and then restarted. The 48MHz clock domain will become unlocked and be sourced from the 32 MHz Ring Oscillator until the 48MHz PLL is on and locked.

4.5.4.1 Always-on Internal 32KHz Clock Source

The 32Khz clock domain can be driven from an internal 32KHz clock source that is always on. This clock source is used to drive the 48MHz PLL and remains on at all times, even when an external input is selected as the source. The internal source provides a reference for the Activity Detect that monitors the external clock input, as well as providing a low latency backup clock source when the Activity Detector cannot detect a clock on the external input.

The Always-on 32KHz Internal Clock Source can be driven either by the 32.768 kHz Silicon Oscillator or the 32.768 kHz Crystal Oscillator.

Note:	If the 32KHZ_SOURCE field in the Clock Enable Register selects the crystal oscillator as the source for the always-on clock source, and the XOSEL field selects a single-ended input for the crystal oscillator, the system must ensure that the single-ended input remains on at all times. The Activity Detector will not monitor the single-ended input to the crystal oscillator.

4.5.4.2 External 32KHz Clock Activity Detector

When the EXT_32K field in the Clock Enable Register is set for an external clock source an Activity Detector monitors the external 32KHz signal at all times. If there is no clock detected on the pin, the 32KHZ clock domain is switched to the internal 32KHz silicon oscillator. If a clock is again detected on the pin, the 32KHz clock domain is switched to the pin

The following figure illustrates the 32KHz clock domain sourcing.

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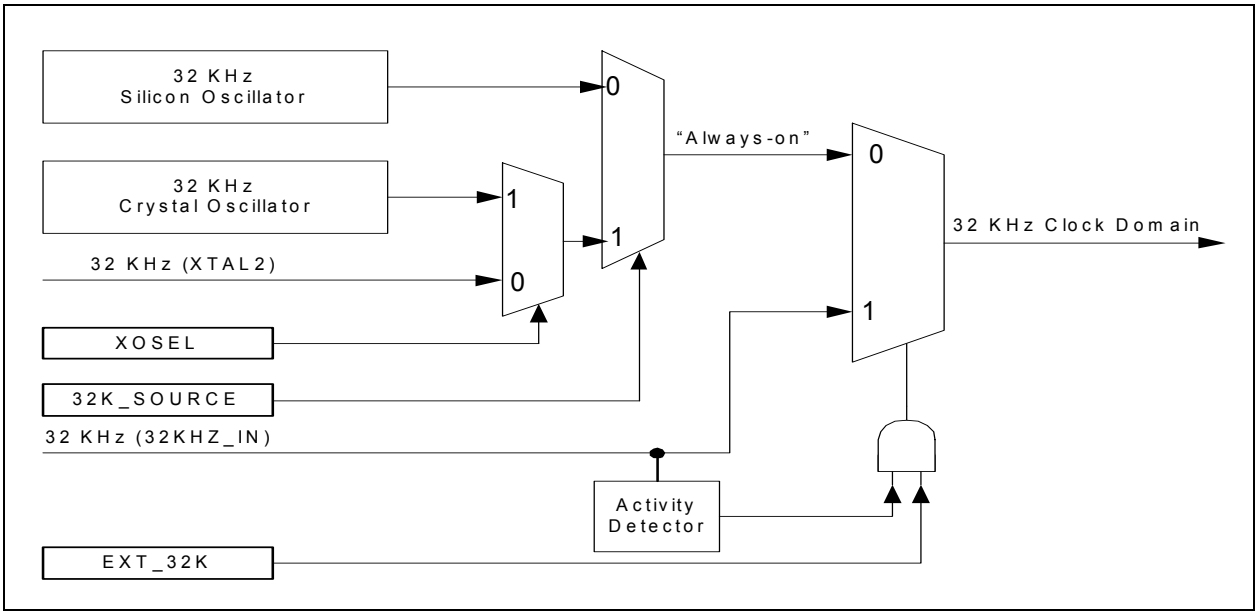
FIGURE 4-3: 32KHZ ACTIVITY DETECTOR



Note: Once the internal 32KHz clock domain switches to an external single-ended clock source, the external source **must** remain active until VTR power is removed, or internal clocking may not function correctly.

4.5.4.3 32KHz Crystal Oscillator

If the 32KHz source will never be the crystal oscillator, then the XTAL2 pin should be grounded. The XTAL1 pin should be left unconnected.

4.6 Resets

TABLE 4-7: DEFINITION OF RESET SIGNALS

Reset	Description	Source
RESET_VBAT	Internal VBAT Reset signal. This signal is used to reset VBAT powered registers.	RESET_VBAT is a pulse that is asserted at the rising edge of VTR power if the VBAT voltage is below a nominal 1.25V. RESET_VBAT is also asserted as a level if, while VTR power is not present, the coin cell is replaced with a new cell that delivers at least a nominal 1.25V. In this latter case RESET_VBAT is de-asserted when VTR power is applied. No action is taken if the coin cell is replaced, or if the VBAT voltage falls below 1.25 V nominal, while VTR power is present.
RESET_VTR	Internal VTR Reset signal.	This internal reset signal is asserted as long as the reset generator determines that the output of the internal regulator is stable at its target voltage and that the voltage rail supplying the main clock PLL is at 3.3V. Although most VTR-powered registers are reset on RESET_SYS, some registers are only reset on this reset.

TABLE 4-7: DEFINITION OF RESET SIGNALS (CONTINUED)

Reset	Description	Source
RESET_SYS	Internal Reset signal. This signal is used to reset VTR powered registers.	RESET_SYS is the main global reset signal. This reset signal will be asserted if: • RESET_VTR is asserted • The RESETI# pin asserted • A WDT Event event is asserted • A soft reset is asserted by the SOFT_SYS-_RESET bit in the System Reset Register • ARM M4 SYSRESETREQ
RESET_eSPI	System reset signal connected to the eSPI ESPI_RESET# pin.	Pin Interface, ESPI_RESET# pin.
RESET_VCC	Performs a reset when Host power (VCC) is turned off	This signal is asserted if • RESET_SYS is asserted • VCC_PWRGD is low • The PWR_INV bit in the Power Reset Control Register is '1b' The PWROK output pin is an inverted version of this reset; it is asserted when VCC_PWRGD is high and the PWR_INV bit is '0b'. **Note:** This reset is referred to as RESET_-SIO in the eSPI Block Specification.
RESET_HOST	Performs a reset when VCC_PWRGD is low or when the system host resets the Host Interface.	This signal is asserted if • RESET_SYS is asserted • VCC_PWRGD is low • The PWR_INV bit in the Power Reset Control Register is '1b' • The HOST_RESET_SELECT bit in the Power Reset Control Register is configured for LRESET# and the LRESET# signal is asserted • The HOST_RESET_SELECT bit in the Power Reset Control Register is configured for eSPI_PLTRST# and the eSPI_PLTRST# signal from the eSPI block is asserted.
WDT Event	A WDT Event generates the RESET_SYS event. This signal resets VTR powered registers with the exception of the WDT Event Count Register register. Note that the glitch protect circuits do not activate on a WDT reset. WDT Event does not reset VBAT registers or logic.	This reset signal will be asserted if: • A WDT Event event is asserted This event is indicated by the WDT bit in the Power-Fail and Reset Status Register
RESET_SYS_nWDT	Internal Reset signal. This signal is used to reset VTR powered registers not effected by a WDT Event A RESET_SYS_nWDT is used to reset registers that need to be preserved through a WDT Event like a WDT Event Count Register.	This reset signal will be asserted if: • RESET_VTR is asserted • The RESETI# pin asserted

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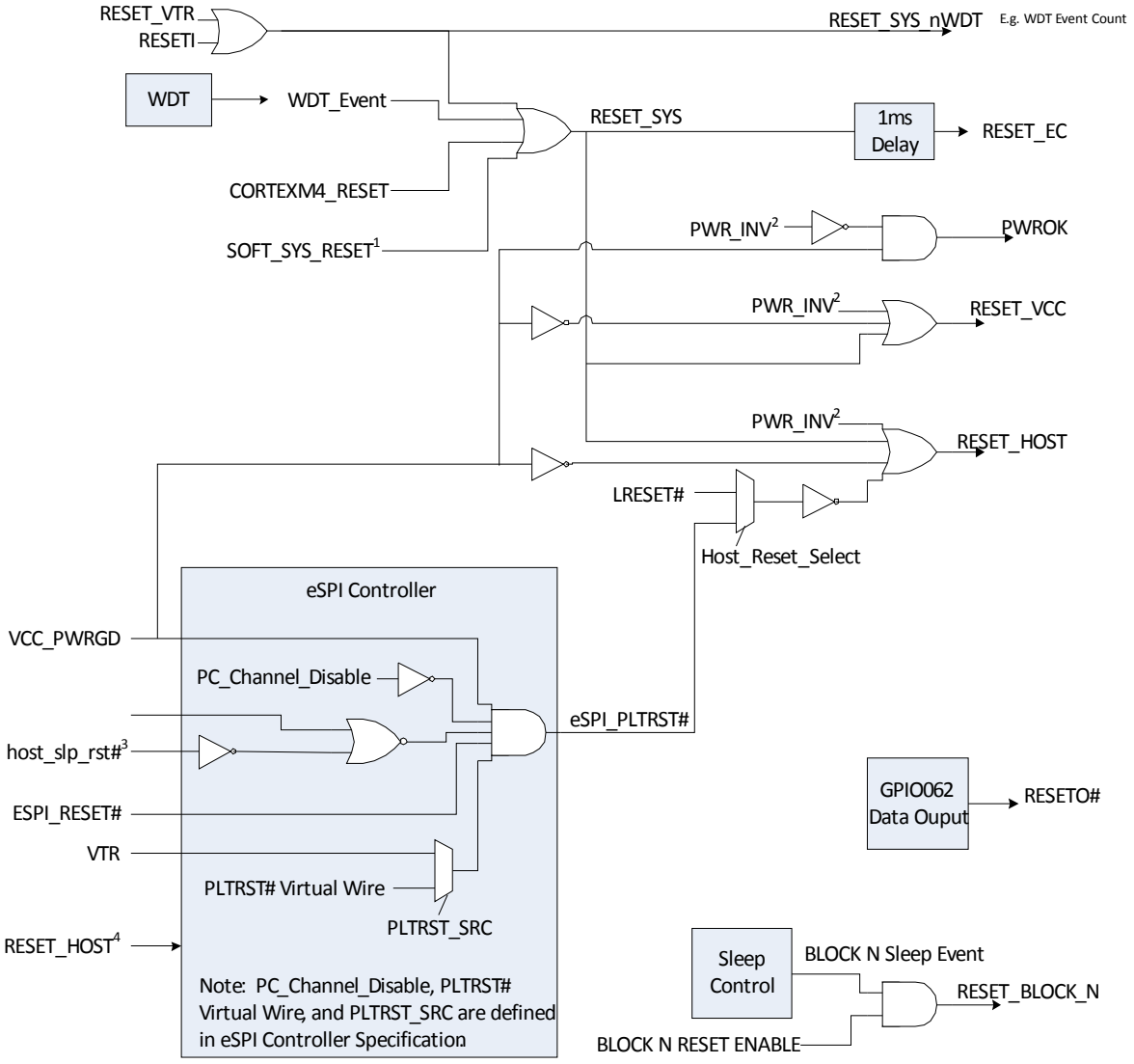
TABLE 4-7: DEFINITION OF RESET SIGNALS (CONTINUED)

Reset	Description	Source
RESET_EC	Internal reset signal to reset the processor in the EC Subsystem.	This reset is a stretched version of RESET_SYS. This reset asserts at the same time that RESET_SYS asserts and is held asserted for 1ms after RESET_SYS deasserts.
RESET_BLOCK_N	Each IP block in the device may be configured to be reset when it enters the Low Power Mode referred to as SLEEP.	This reset signal will be asserted if Block N SLEEP_ENABLE and Block N RESET_ENABLE are all set to 1, Block N CLOCK_REQUIRED signal is low, and Block N Enters Sleep.

FIGURE 4-4: RESETS BLOCK DIAGRAM



Note 1: SOFT_SYS_RESET is implemented in bit[8] of the System Reset Register
Note 2: PWR_INV is implemented in bit[0] of the Power Reset Control Register
Note 3: host_slp_rst# is asserted if the Host Sleep Enable bit and Host Reset Enable bit are set and the eSPI Controller is put to sleep
Note 4: RESET_HOST is fed back into the eSPI Controller to reset select registers/bits

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4.7 Chip Power Management Features

This device is designed to always operate in its lowest power state during normal operation. In addition, this device offers additional programmable options to put individual logical blocks to sleep as defined in the following section, Section 4.7.1.

4.7.1 BLOCK LOW POWER MODES

All power related control signals are generated and monitored centrally in the chip's Power, Clocks, and Resets (PCR) block. The power manager of the PCR block uses a sleep interface to communicate with all the blocks. The sleep interface consists of three signals:

- **SLEEP_ENABLE (request to sleep the block)** is generated by the PCR block. A group of SLEEP_ENABLE signals are generated for every clock segment. Each group consists of a SLEEP_ENABLE signal for every block in that clock segment.
- **CLOCK_REQUIRED (request clock on)** is generated by every block. They are grouped by blocks on the same clock segment. The PCR monitors these signals to see when it can gate off clocks.
- **RESET_ENABLE (reset on sleep)** bits determine if the block (including registers) will be reset when it enters sleep mode.

A block can always drive CLOCK_REQUIRED low synchronously, but it *must* drive it high asynchronously since its internal clocks are gated and it has to assume that the clock input itself is gated. Therefore the block can only drive CLOCK_REQUIRED high as a result of a register access or some other input signal.

The following table defines a block's power management protocol:

TABLE 4-8: POWER MANAGEMENT PROTOCOL

Power State	SLEEP_ENABLE	CLOCK_REQUIRED	Description
Normal operation	Low	Low	Block is idle and NOT requesting clocks. The block gates its own internal clock.
Normal operation	Low	High	Block is NOT idle and requests clocks.
Request sleep	Rising Edge	Low	Block is IDLE and enters sleep mode immediately. The block gates its own internal clock. The block cannot request clocks again until SLEEP_ENABLE goes low.
Request sleep	Rising Edge	High then Low	Block is not IDLE and will stop requesting clocks and enter sleep when it finishes what it is doing. This delay is block specific, but should be less than 1 ms. The block gates its own internal clock. After driving CLOCK_REQUIRED low, the block cannot request clocks again until SLEEP_ENABLE goes low.
Register Access	X	High	Register access to a block is always available regardless of SLEEP_ENABLE. Therefore the block ungates its internal clock and drives CLOCK_REQUIRED high during the access. The block will regate its internal clock and drive CLOCK_REQUIRED low when the access is done.

A wake event clears all SLEEP_ENABLE bits momentarily, and then returns the SLEEP_ENABLE bits back to their original state. The block that needs to respond to the wake event will do so.

The Sleep Enable, Clock Required and Reset Enable Registers are defined in Section 4.8.

4.7.2 CONFIGURING THE CHIP'S SLEEP STATES

The chip supports two sleep states: LIGHT SLEEP and HEAVY SLEEP. The chip will enter one of these two sleep states only when all the blocks have been commanded to sleep and none of them require a 48MHz clock source (i.e., all CLOCK_REQUIRED status bits are 0), and the processor has executed its sleep instruction. These sleep states must be selected by firmware via the System Sleep Control bits implemented in the System Sleep Control Register prior to issuing the sleep instruction. Table 4-10, "System Sleep Modes" defines each of these sleep states.

There are two ways to command the chip blocks to enter sleep.

1. Assert the SLEEP_ALL bit located in the System Sleep Control Register
2. Assert all the individual block sleep enable bits

Blocks will only enter sleep after their sleep signal is asserted and they no longer require the 48MHz source. Each block has a corresponding clock required status bit indicating when the block has entered sleep. The general operation is that a block will keep the 48MHz clock source on until it completes its current transaction. Once the block has completed its work, it deasserts its clock required signal. Blocks like timers, PWMs, etc. will de-assert their clock required signals immediately. See the individual block Low Power Mode sections to determine how each individual block enters sleep.

4.7.3 DETERMINING WHEN THE CHIP IS SLEEPING

The 48MHZ_OUT pin can be used to verify the chip's clock has stopped, which indicates the device is in LIGHT SLEEP or HEAVY SLEEP, as determined by the System Sleep Control Register. If the clock is toggling the chip is in the full on running state. if the clock is not toggling the chip has entered the programmed sleep state.

4.7.4 WAKING THE CHIP FROM SLEEPING STATE

The chip will remain in the configured sleep state until it detects either a wake event or a full VTR POR. A wake event occurs when a wake-capable interrupt is enabled and triggered. Interrupts that are not wake-capable cannot occur while the system is in LIGHT SLEEP or HEAVY SLEEP.

In LIGHT SLEEP, the 48MHz clock domain is gated off, but the 48 MHz PLL remains operational and locked to the 32KHz clock domain. On wake, the PLL output is ungated and the 48MHz clock domain starts immediately, with the PLL_LOCK bit in the Oscillator ID Register set to '1'. Any device that requires an accurate clock, such as a UART, me be used immediately on wake.

In HEAVY SLEEP, the 48 MHz PLL is shut down. On wake, the 32 MHz Ring Oscillator is used to provide a clock source for the 48MHz clock domain until the PLL locks to the 32KHz clock domain. The ring oscillator starts immediately on wake, so there is no latency for the EC to start after a wake, However, the ring oscillator is only accurate to ±50%, so any device that requires an accurate 48MHz clock will not operate correctly until the PLL locks.The time to lock latency for the PLL is shown in Table 4-10, "System Sleep Modes".

The SLEEP_ALL bit is automatically cleared when the processor responds to an interrupt. This applies to non-wake interrupts as well as wake interrupts, in the event an interrupt occurs between the time the processor issued a WAIT FOR INTERRUPT instruction and the time the system completely enters the sleep state.

4.7.4.1 Wake-Only Events

Some devices which respond to an external master require the 48MHz clock domain to operate but do not necessarily require and immediate processing by the EC. For example, an LPC Host may read a register in an LPC logical device, with no side effects. Wake-only events provide the means to start the 48MHz clock domain without triggering an EC interrupt service routine. This events are grouped into a single GIRQ, GIRQ22. Events that are enabled in that GIRQ will start the clock domain when the event occurs, but will not invoke an EC interrupt. The SLEEP_ENABLE flags all remain asserted. If the activity for the event does not in turn trigger another EC interrupt, the CLOCK_REQUIRED for the block will re-assert and the configured sleep state will be re-entered.

Example: LPC I/O Traffic targeting EMI block.

The LPC Interface detects traffic on the bus and requires the clock to be on to process the incoming data. If the LPC_WAKE_ONLY interrupt in GIRQ22 is enabled, the LPC block will be able to autonomously receive data for the programmed I/O ranges without processor intervention. Once the data is loaded into the HOST-to-EC Mailbox Register the Host-to-EC IRQ will trigger an interrupt to the embedded controller to service this command.

4.8 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the Power, Clocks, and Resets Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

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TABLE 4-9: REGISTER SUMMARY

Offset	Name
0h	System Sleep Control Register
4h	Processor Clock Control Register
8h	Slow Clock Control Register
Ch	Oscillator ID Register
10h	PCR Power Reset Status Register
14h	Power Reset Control Register
18h	System Reset Register
1Ch	TEST
20h	TEST
30h	Sleep Enable 0 Register
34h	Sleep Enable 1 Register
38h	Sleep Enable 2 Register
3Ch	Sleep Enable 3 Register
40h	Sleep Enable 4 Register
50h	Clock Required 0 Register
54h	Clock Required 1 Register
58h	Clock Required 2 Register
5Ch	Clock Required 3 Register
60h	Clock Required 4 Register
70h	Reset Enable 0 Register
74h	Reset Enable 1 Register
78h	Reset Enable 2 Register
7Ch	Reset Enable 3 Register
80h	Reset Enable 4 Register

All register addresses are naturally aligned on 32-bit boundaries. Offsets for registers that are smaller than 32 bits are reserved and must not be used for any other purpose.

The bit definitions for the Sleep Enable, Clock Required and Reset Enable Registers are defined in the Sleep Enable Register Assignments Table in Section 3.0, "Device Inventory".

4.9 Sleep Enable *n* Registers

4.9.1 SLEEP ENABLE *N* REGISTER FORMAT

Offset	See Sleep Enable Register Assignments Table in Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	SLEEP_ENABLE 1=Block is commanded to sleep at next available moment 0=Block is free to use clocks as necessary Unassigned bits are reserved. They must be set to ‘1b’ when written. When read, unassigned bits return the last value written.	R/W	0h	RESET_SYS

4.9.2 CLOCK REQUIRED *N* REGISTER FORMAT

Offset	See Sleep Enable Register Assignments Table in Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CLOCK_REQUIRED 1=Bock requires clocks 0=Block does not require clocks Unassigned bits are reserved and always return 0 when read.	R	0h	RESET_SYS

4.9.3 RESET ENABLE *N* REGISTER FORMAT

Note:	If a block is configured such that it is to be reset when it goes to sleep, then registers within the block may not be writable when the block is asleep.

Offset	See Sleep Enable Register Assignments Table in Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	RESET_ENABLE 1=Bock will reset on sleep 0=Block will not reset on sleep Unassigned bits are reserved and always return 0 when read.	R/W	0h	RESET_SYS

4.9.4 SYSTEM SLEEP CONTROL REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3	SLEEP_ALL By setting this bit to '1b' and then issuing a WAIT FOR INTERRUPT instruction, the EC can initiate the System Sleep mode. When no device requires the main system clock, the system enters the sleep mode defined by the field SLEEP_MODE. This bit is automatically cleared when the processor vectors to an interrupt. 1=Assert all sleep enables 0=Do not sleep all	R/W	0h	RESET_SYS

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Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	TEST Test bit. Should always be written with a '0b'.	R/W	0h	RESET_SYS
1	Reserved	R	-	-
0	SLEEP_MODE Sleep modes differ only in the time it takes for the 48MHz clock domain to lock to 48MHz. The wake latency in all sleep modes is 0ms. Table 4-10 shows the time to lock latency for the different sleep modes. 1=Heavy Sleep 0=Light Sleep	R/W	0h	RESET_SYS

TABLE 4-10: SYSTEM SLEEP MODES

SLEEP_MODE	Sleep State	Latency to Lock	Description
0	LIGHT SLEEP	0	Output of the PLL is gated in sleep. The PLL remains on.
1	HEAVY SLEEP	3ms	The PLL is shut down while in sleep.

4.9.5 PROCESSOR CLOCK CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	PROCESSOR_CLOCK_DIVIDE The following list shows examples of settings for this field and the resulting EC clock rate. 48=divide the 48MHz clock by 48 (1MHz processor clock) 16=divide the 48MHz clock by 16 (4MHz processor clock) 4=divide the 48MHz clock by 4 (12MHz processor clock) 3=divide the 48MHz clock by 3 (16MHz processor clock) 1=divide the 48MHz clock by 1 (48MHz processor clock) No other values are supported.	R/W	4h	RESET_SYS

4.9.6 SLOW CLOCK CONTROL REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:0	SLOW_CLOCK_DIVIDE Configures the 100KHz clock domain. n=Divide by n 0=Clock off The default setting is for 100KHz.	R/W	1E0h	RESET_SYS

4.9.7 OSCILLATOR ID REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:9	Reserved	R	-	-
8	PLL_LOCK Phase Lock Loop Lock Status	R	0h	RESET_SYS
7:0	TEST	R	N/A	RESET_SYS

4.9.8 PCR POWER RESET STATUS REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:12	Reserved	R	-	-
11	ESPI_CLK_ACTIVE This bit monitors the state of the eSPI clock input. This status bit detects edges on the clock input but does not validate the frequency. 1=The eSPI clock is present. 0=The eSPI clock input is not present.	R	-	RESET_SYS
Note 1: This read-only status bit always reflects the current status of the event and is not affected by any Reset events.				

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Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
11	PCICLK_ACTIVE This bit monitors the state of the PCI clock input. This status bit detects edges on the clock input but does not validate the frequency. 1=The PCI clock is present. 0=The PCI clock input is not present.	R	-	RESET_SYS
10	32K_ACTIVE This bit monitors the state of the 32K clock input. This status bit detects edges on the clock input but does not validate the frequency. 1=The 32K clock input is present. The internal 32K clock is derived from the pin and the ring oscillator is synchronized to the external 32K clock 0=The 32K clock input is not present. The internal 32K clock is derived from the ring oscillator	R	-	RESET_SYS
9:8	Reserved	R	-	-
7	JTAG_RESET_STATUS Indicates that aRESET_SYS was triggered by a JTAG action. The bit will not clear if a write 1 is attempted at the same time that a VTR_RST_N occurs, this way a reset event is never missed. 1=A reset occurred because of a JTAG command 0=No JTAG reset occurred since the last time this bit was cleared	R/WC	1h	RESET_SYS
6	VTR_RESET_STATUS Indicates the status of RESET_SYS. The bit will not clear if a write 1 is attempted at the same time that a RESET_VTR occurs; this way a reset event is never missed. 1=A reset occurred 0=No reset occurred since the last time this bit was cleared	R/WC	1h	RESET_SYS
5	VBAT_RESET_STATUS Indicates the status of RESET_VTR. The bit will not clear if a write of ‘1’b is attempted at the same time that a VBAT_RST_N occurs, this way a reset event is never missed. 1=A reset occurred 0=No reset occurred while VTR was off or since the last time this bit was cleared	R/WC	-	RESET_SYS
4	Reserved	R	-	-
Note 1: This read-only status bit always reflects the current status of the event and is not affected by any Reset events.				

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	RESET_HOST_STATUS Indicates the status of RESET_VCC. 1=Reset not active 0=Reset active	R	-	Note 1
2	VCC_PWRGD_STATUS Indicates the status of VCC_PWRGD. 1=VCC_PWRGD asserted 0=VCC_PWRGD not asserted	R	xh	Note 1
1:0	Reserved	R	-	-
Note 1:	This read-only status bit always reflects the current status of the event and is not affected by any Reset events.			

4.9.9 POWER RESET CONTROL REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:9	Reserved	R	-	-
8	HOST_RESET_SELECT This bit determines the platform reset signal. It should be set to ‘0b’ if the eSPI interface is in use. 1=The LRESET# pin is used to generate the internal Platform Reset 0=The eSPI_PLTRST# signal from the eSPI block is used to generate the internal Platform Reset	R/W	1h	RESET_SYS
7:1	Reserved	R	-	-
0	PWR_INV This bit allows firmware to control when the Host receives an indication that the VCC power is valid, by controlling the state of the PWROK pin. This bit is used by firmware to control the internal RESET_VCC signal function and the external PWROK pin. This bit is read-only when VCC_PWRGD is de-asserted low. The internal RESET_VCC signal is asserted when this bit is asserted even if the PWROK pin is configured as an alternate function.	R / R/W	1h	RESET_SYS

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4.9.10 SYSTEM RESET REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:9	Reserved	R	-	-
8	SOFT_SYS_RESET A write of a '1' to this bit will force an assertion of the RESET_SYS reset signal, resetting the device. A write of a '0' has no effect. Reads always return '0'.	W	-	-
7:0	Reserved	R	-	-

5.0 ARM M4F BASED EMBEDDED CONTROLLER

5.1 Introduction

This chapter contains a description of the ARM M4F Embedded Controller (EC).

The EC is built around an ARM® Cortex®-M4F Processor provided by Arm Ltd. (the “ARM M4F IP”). The ARM Cortex® M4F is a full-featured 32-bit embedded processor, implementing the ARMv7-M THUMB instruction set and FPU instruction set in hardware.

The ARM M4F IP is configured as a Von Neumann, Byte-Addressable, Little-Endian architecture. It provides a single unified 32-bit byte-level address, for a total direct addressing space of 4GByte. It has multiple bus interfaces, but these express priorities of access to the chip-level resources (Instruction Fetch vs. Data RAM vs. others), and they do not represent separate addressing spaces.

The ARM M4F is configured as follows.

- **Little-Endian** byte ordering is selected at all times
- **Bit Banding** is included for efficient bit-level access
- **Floating-Point Unit (FPU)** is included, to implement the Floating-Point instruction set in hardware
- **Debug** features are included at “Ex+” level, defined as follows:
  - **DWT** Unit provides 4 Data Watchpoint comparators and Execution Monitoring
  - **FPB** Unit provides HW Breakpointing with 6 Instruction and 2 Literal (Read-Only Data) address comparators. The FPB comparators are also available for Patching: remapping Instruction and Literal Data addresses.
- **Trace** features are included at “Full” level, defined as follows:
  - **DWT** for reporting breakpoints and watchpoints
  - **ITM** for profiling and to timestamp and output messages from instrumented firmware builds
  - **ETM** for instruction tracing, and for enhanced reporting of Core and DWT events
  - The ARM-defined **HTM** trace feature is **not included**
- **NVIC** Interrupt controller with 8 priority levels and up to 240 individually-vectored interrupt inputs
  - A Microchip-defined Interrupt Aggregator function (at chip level) may be used to group multiple interrupts onto single NVIC inputs
  - The ARM-defined **WIC** feature is **not included**. The Microchip Interrupt Aggregator function (at chip level) provides Wake control
- **MPU** (Memory Protection Unit) is included for memory access control
- Single entry **Write Buffer** is incorporated

5.2 References

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5.3 Terminology

5.3.1 ARM IP TERMS AND ACRONYMS

- AHB

  Advanced High-Performance Bus, a system-level on-chip **AMBA 2** bus standard. See Reference[5], ARM Limited: AMBA® Specification (Rev 2.0), IHI0011A, 13 May 1999.

- AHB-AP

  AHB Access Port, the **AP** option selected by Microchip for the **DAP**

- AHB-Lite

  A Single-Master subset of the **AHB** bus standard: defined in the **AMBA 3** bus standard. See Reference[6], ARM Limited: AMBA® 3 AHB-Lite Protocol Specification, IHI0033A, 6 June 2006.

- AMBA

  The collective term for bus standards originated by ARM Limited.

  AMBA 3 defines the IP's **AHB-Lite** and **ATB** bus interfaces.

  AMBA 2 (AMBA Rev. 2.0) defines the EC's **AHB** bus interface.

- AP

  Any of the ports on the **DAP** subblock for accessing on-chip resources on behalf of the Debugger, independent of processor operations. A single **AHB-AP** option is currently selected for this function.

- APB

  Advanced Peripheral Bus, a limited 32-bit-only bus defined in **AMBA 2** for I/O register accesses. This term is relevant only to describe the **PPB** bus internal to the EC core. See Reference [5], ARM Limited: AMBA® Specification (Rev 2.0), IHI0011A, 13 May 1999.

- ARMv7

  The identifying name for the general architecture implemented by the **Cortex-M** family of IP products.

  The **ARMv7** architecture has no relationship to the older "ARM 7" product line, which is classified as an "ARMv3" architecture, and is very different.

- ATB

  Interface standard for Trace data to the **TPIU** from **ETM** and/or **ITM** blocks, Defined in **AMBA 3**. See Reference[7], ARM Limited: AMBA® 3 ATB Protocol Specification, IHI0032A, 19 June 2006.

- Cortex-M4F

  The ARM designation for the specific IP selected for this product: a Cortex M4 processor core containing a hardware Floating Point Unit (FPU).

- DAP

  Debug Access Port, a subblock consisting of **DP** and **AP** subblocks.

- DP

  Any of the ports in the **DAP** subblock for connection to an off-chip Debugger. A single **SWJ-DP** option is currently selected for this function, providing **JTAG** connectivity.

- DWT

  Data Watchdog and Trace subblock. This contains comparators and counters used for data watchpoints and Core activity tracing.

- ETM

  Embedded Trace Macrocell subblock. Provides enhancements for Trace output reporting, mostly from the **DWT** subblock. It adds enhanced instruction tracing, filtering, triggering and timestamping.

- FPB

  FLASH Patch Breakpoint subblock. Provides either Remapping (Address substitution) or Breakpointing (Exception or Halt) for a set of Instruction addresses and Data addresses. See Section 8.3 of Reference [1], ARM Limited: Cortex®-M4 Technical Reference Manual, DDI0439C, 29 June 2010.

- FPU

  Floating-Point Unit: a subblock included in the Core for implementing the Floating Point instruction set in hardware.

- HTM

  AHB Trace Macrocell. This is an optional subblock that is **not included**.

- ITM

  Instrumentation Trace Macrocell subblock. Provides a HW Trace interface for “printf”-style reports from instrumented firmware builds, with timestamping also provided.

- MEM-AP

  A generic term for an **AP** that connects to a memory-mapped bus on-chip. For this product, this term is synonymous with the AHB Access Port, **AHB-AP.**

- MPU

  Memory Protection Unit.

- NVIC

  Nested Vectored Interrupt Controller subblock. Accepts external interrupt inputs. See References [2], ARM Limited: ARM®v7-M Architecture Reference Manual, DDI0403D, November 2010 and [4], ARM® Generic Interrupt Controller Architecture version 1.0 Architecture Specification, IHI0048A, September 2008.

- PPB

  Private Peripheral Bus: A specific **APB** bus with local connectivity within the EC.

- ROM Table

  A ROM-based data structure in the Debug section that allows an external Debugger and/or a FW monitor to determine which of the Debug features are present.

- SWJ-DP

  Serial Wire / **JTAG** Debug Port, the **DP** option selected by Microchip for the **DAP**.

- TPA

  Trace Port Analyzer: any off-chip device that uses the TPIU output.

- TPIU

  Trace Port Interface Unit subblock. Multiplexes and buffers Trace reports from the ETM and ITM subblocks.

- WIC

  Wake-Up Interrupt Controller. This is an optional subblock that is **not included**.

5.3.2 MICROCHIP TERMS AND ACRONYMS

- Interrupt Aggregator

  This is a module that may be present at the chip level, which can combine multiple interrupt sources onto single interrupt inputs at the EC, causing them to share a vector.

- PMU

  Processor Memory Unit, this is a module that may be present at the chip level containing any memory resources that are closely-coupled to the MEC170x EC. It manages accesses from both the EC processor and chip-level bus masters.

5.4 ARM M4F IP Interfaces

This section defines only the interfaces to the ARM IP itself. For the interfaces of the entire block, see Section 5.5, "Block External Interfaces".

The MEC170x IP has the following major external interfaces, as shown in Figure 5-1, "ARM M4F Based Embedded Controller I/O Block Diagram":

- ICode AHB-Lite Interface
- DCode AHB-Lite Interface
- System AHB-Lite Interface

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- Debug (JTAG) Interface
- Trace Port Interface
- Interrupt Interface

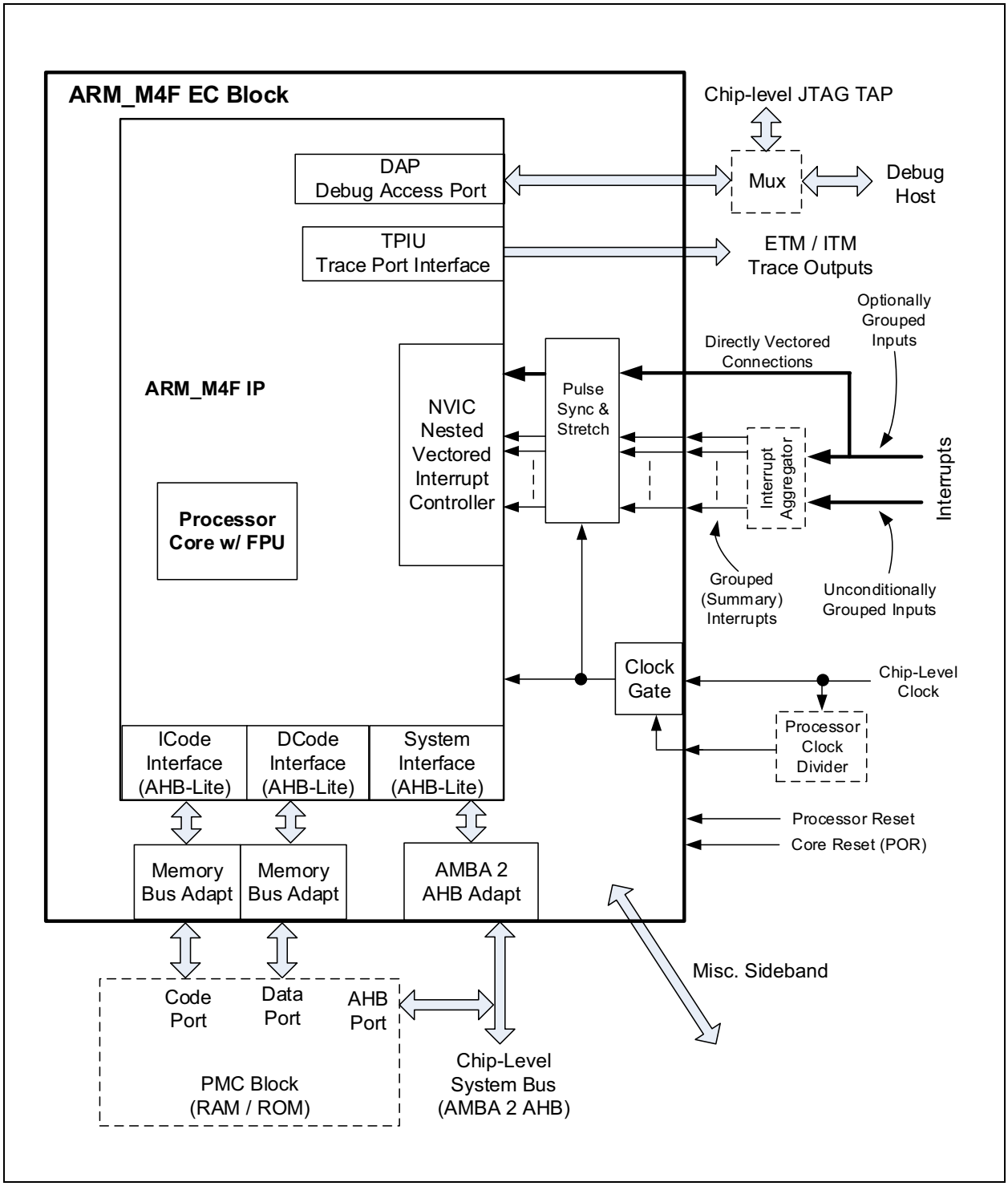
The EC operates on the model of a single 32-bit addressing space of byte addresses (4Gbytes, Von Neumann architecture) with Little-Endian byte ordering. On the basis of an internal decoder (part of the Bus Matrix shown in Figure 5-1), it routes Read/Write/Fetch accesses to one of three external interfaces, or in some cases internally (shown as the PPB interface).

The EC executes instructions out of closely-coupled memory via the ICode Interface. Data accesses to closely-coupled memory are handled via the DCode Interface. The EC accesses the rest of the on-chip address space via the System AHB-Lite interface. The Debugger program in the host can probe the EC and all EC addressable memory via the JTAG debug interface.

Aliased addressing spaces are provided at the chip level so that specific bus interfaces can be selected explicitly where needed. For example, the EC's Bit Banding feature uses the System AHB-Lite bus to access resources normally accessed via the DCode or ICode interface.

5.5 Block External Interfaces

FIGURE 5-1: ARM M4F BASED EMBEDDED CONTROLLER I/O BLOCK DIAGRAM



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5.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

5.6.1 POWER DOMAINS

TABLE 5-1: POWER SOURCES

Name	Description
VTR	The ARM M4F Based Embedded Controller is powered by VTR.

5.6.2 CLOCK INPUTS

5.6.2.1 Basic Clocking

The basic clocking comes from a free-running Clock signal provided from the chip level.

TABLE 5-2: CLOCK INPUTS

Name	Description
48MHz	The clock source to the EC. Division of the clock rate is determined by the PROCESSOR_CLOCK_DIVIDE field in the Processor Clock Control Register.

5.6.2.2 System Tick Clocking

The System Tick clocking is controlled by a signal from chip-level logic. It is the 48MHz divided by the following:

- ((PROCESSOR_CLOCK_DIVIDE)x2)+1

5.6.2.3 Debug JTAG Clocking

The Debug JTAG clocking comes from chip-level logic, which may multiplex or gate this clock. See Section 5.10, "Debugger Access Support".

5.6.2.4 Trace Clocking

The Clock for the Trace interface is identical to the 48MHz input.

5.6.3 RESETS

The reset interface from the chip level is given below.

TABLE 5-3: RESET SIGNALS

Name	Description
RESET_EC	The ARM M4F Based Embedded Controller is reset by RESET_EC.

5.7 Interrupts

The ARM M4F Based Embedded Controller is equipped with an Interrupt Interface to respond to interrupts. These inputs go to the IP's NVIC block after a small amount of hardware processing to ensure their detection at varying clock rates. See Figure 5-1, "ARM M4F Based Embedded Controller I/O Block Diagram".

As shown in Figure 5-1, an Interrupt Aggregator block may exist at the chip level, to allow multiple related interrupts to be grouped onto the same NVIC input, and so allowing them to be serviced using the same vector. This may allow the same interrupt handler to be invoked for a group of related interrupt inputs. It may also be used to expand the total number of interrupt inputs that can be serviced.

The NMI (Non-Maskable Interrupt) connection is tied off and not used.

5.7.1 NVIC INTERRUPT INTERFACE

The NVIC interrupt unit can be wired to up to 240 interrupt inputs from the chip level. The interrupts that are actually connected from the chip level are defined in the Interrupt section.

All NVIC interrupt inputs can be programmed as either pulse or level triggered. They can also be individually masked, and individually assigned to their own hardware-managed priority level.

5.7.2 NVIC RELATIONSHIP TO EXCEPTION VECTOR TABLE ENTRIES

The Vector Table consists of 4-byte entries, one per vector. Entry 0 is not a vector, but provides an initial Reset value for the Main Stack Pointer. Vectors start with the Reset vector, at Entry #1. Entries up through #15 are dedicated for internal exceptions, and do not involve the NVIC.

NVIC entries in the Vector Table start with Entry #16, so that NVIC Interrupt #0 is at Entry #16, and all NVIC interrupt numbers are incremented by 16 before accessing the Vector Table.

The number of connections to the NVIC determines the necessary minimum size of the Vector Table, as shown below. It can extend as far as 256 entries (255 vectors, plus the non-vector entry #0).

A Vector entry is used to load the Program Counter (PC) and the EPSR.T bit. Since the Program Counter only expresses code addresses in units of two-byte Halfwords, bit[0] of the vector location is used to load the EPSR.T bit instead, selecting THUMB mode for exception handling. Bit[0] must be '1' in all vectors, otherwise a UsageFault exception will be posted (INVSTATE, unimplemented instruction set). If the Reset vector is at fault, the exception posted will be HardFault instead.

TABLE 5-4: EXCEPTION AND INTERRUPT VECTOR TABLE LAYOUT

Table Entry	Exception Number	Exception
Special Entry for Reset Stack Pointer		
0	(none)	Holds Reset Value for the Main Stack Pointer. Not a Vector.
Core Internal Exception Vectors start here		
1	1	Reset Vector (PC + EPSR.T bit)
2	2	NMI (Non-Maskable Interrupt) Vector
3	3	HardFault Vector
4	4	MemManage Vector
5	5	BusFault Vector
6	6	UsageFault Vector
7	(none)	(Reserved by ARM Ltd.)
8	(none)	(Reserved by ARM Ltd.)
9	(none)	(Reserved by ARM Ltd.)
10	(none)	(Reserved by ARM Ltd.)
11	11	SVCall Vector
12	12	Debug Monitor Vector
13	(none)	(Reserved by ARM Ltd.)
14	14	PendSV Vector
15	15	SysTick Vector
NVIC Interrupt Vectors start here		
16	16	NVIC Interrupt #0 Vector
. . .	. . .	. . .
n + 16	n + 16	NVIC Interrupt #n Vector
. . .	. . .	. . .
max + 16	max + 16	NVIC Interrupt #max Vector (Highest-numbered NVIC connection.)
. . .	. . .	. Table size may (but need not) extend further. . .
255	255	NVIC Interrupt #239 (Architectural Limit of Exception Table)

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5.8 Low Power Modes

The ARM processor can enter Sleep or Deep Sleep modes internally. This action will cause an output signal Clock Required to be turned off, allowing clocks to be stopped from the chip level. However, Clock Required will still be held active, or set to active, unless all of the following conditions exist:

- No interrupt is pending.
- An input signal Sleep Enable from the chip level is active.
- The Debug JTAG port is inactive (reset or configured not present).

In addition, regardless of the above conditions, a chip-level input signal Force Halt may halt the processor and remove Clock Required.

5.9 Description

5.9.1 BUS CONNECTIONS

There are three bus connections used from MEC170x EC block, which are directly related to the IP bus ports. See Figure 5-1, "ARM M4F Based Embedded Controller I/O Block Diagram".

For the mapping of addresses at the chip level, see Section 3.0, "Device Inventory".

5.9.1.1 Closely Coupled Instruction Fetch Bus

As shown in Figure 5-1, the AHB-Lite ICode port from the IP is converted to a more conventional SRAM memory-style bus and connected to the on-chip memory resources with routing priority appropriate to Instruction Fetches.

5.9.1.2 Closely Coupled Data Bus

As shown in Figure 5-1, the AHB-Lite DCode port from the IP is converted to a more conventional SRAM memory-style bus and connected to the on-chip memory resources with routing priority appropriate to fast Data Read/Write accesses.

5.9.1.3 Chip-Level System Bus

As shown in Figure 5-1, the AHB-Lite System port from the IP is converted from AHB-Lite to fully arbitrated multi-master capability (the AMBA 2 defined AHB bus: see Reference [5], ARM Limited: AMBA® Specification (Rev 2.0), IHI0011A, 13 May 1999). Using this bus, all addressable on-chip resources are available. The multi-mastering capability supports the Microchip DMA and EMI features if present, as well as the Bit-Banding feature of the IP itself.

As also shown in Figure 5-1, the Closely-Coupled memory resources are also available through this bus connection using aliased addresses. This is required in order to allow Bit Banding to be used in these regions, but it also allows them to be accessed by DMA and other bus masters at the chip level.

Note:	Registers with properties such as Write-1-to-Clear (W1C), Read-to-Clear and FIFOs need to be handled with appropriate care when being used with the bit band alias addressing scheme. Accessing such a register through a bit band alias address will cause the hardware to perform a read-modify-write, and if a W1C-type bit is set, it will get cleared with such an access. For example, using a bit band access to the Interrupt Aggregator, including the Interrupt Enables and Block Interrupt Status to clear an IRQ will clear all active IRQs.

5.9.2 INSTRUCTION PIPELINING

There are no special considerations except as defined by ARM documentation.

5.10 Debugger Access Support

An external Debugger accesses the chip through a JTAG standard interface. The ARM Debug Access Port supports both the 2-pin SWD (Serial Wire Debug) interface and the 4-pin JTAG interface.

As shown in Figure 5-1, "ARM M4F Based Embedded Controller I/O Block Diagram", other resources at the chip level that share the JTAG port pins; for example chip-level Boundary Scan.

By default, debug access is disabled when the EC begins executing code. EC code enables debugging by writing the Debug Enable Register in the EC Subsystem Registers block.

TABLE 5-5: ARM JTAG ID

ARM Debug Mode	JTAG ID
SW-DP (2-wire)	0x2BA01477
JTAG (4-wire)	0x4BA00477

5.10.1 DEBUG AND ACCESS PORTS (SWJ-DP AND AHB-AP SUBBLOCKS)

These two subblocks work together to provide access to the chip for the Debugger using the Debug JTAG connection, as described in Chapter 4 of the ARM Limited: ARM® Debug Interface v5 Architecture Specification, IHI0031A, 8 February 2006.

5.10.2 BREAKPOINT, WATCHPOINT AND TRACE SUPPORT

See References [11], ARM Limited: ARM® Debug Interface v5 Architecture Specification, IHI0031A, 8 February 2006 and [12], ARM Limited: ARM® Debug Interface v5 Architecture Specification ADIv5.1 Supplement, DSA09-PRDC-008772, 17 August 2009. A summary of functionality follows.

Breakpoint and Watchpoint facilities can be programmed to do one of the following:

- Halt the processor. This means that the external Debugger will detect the event by periodically polling the state of the EC.
- Transfer control to an internal Debug Monitor firmware routine, by triggering the Debug Monitor exception (see Table 5-4, "Exception and Interrupt Vector Table Layout").

5.10.2.1 Instrumentation Support (ITM Subblock)

The Instrumentation Trace Macrocell (ITM) is for profiling software. This uses non-blocking register accesses, with a fixed low-intrusion overhead, and can be added to a Real-Time Operating System (RTOS), application, or exception handler. If necessary, product code can retain the register access instructions, avoiding probe effects.

5.10.2.2 HW Breakpoints and ROM Patching (FPB Subblock)

The Flash Patch and Breakpoint (FPB) block. This block can remap sections of ROM, typically Flash memory, to regions of RAM, and can set breakpoints on code in ROM. This block can be used for debug, and to provide a code or data patch to an application that requires field updates to a product in ROM.

5.10.2.3 Data Watchpoints and Trace (DWT Subblock)

The Debug Watchpoint and Trace (DWT) block provides watchpoint support, program counter sampling for performance monitoring, and embedded trace trigger control.

5.10.2.4 Trace Interface (ETM and TPIU)

The Embedded Trace Macrocell (ETM) provides instruction tracing capability. For details of functionality and usage, see References [13], ARM Limited: Embedded Trace Macrocell™ (ETMv1.0 to ETMv3.5) Architecture Specification, IHI0014Q, 23 September 2011 and [14], ARM Limited: CoreSight™ ETM™-M4 Technical Reference Manual, DDI0440C, 29 June 2010.

The Trace Port Interface Unit (TPIU) provides the external interface for the ITM, DWT and ETM.

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5.11 Delay Register

5.11.1 DELAY REGISTER

Offset	1000_0000h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:5	Reserved	R	-	-
4:0	DELAY Writing a value *n,* from 0h to 31h, to this register will cause the ARM processor to stall for (*n*+1) microseconds (that is, from 1µS to 32µS). Reads will return the last value read immediately. There is no delay.	R/W	0h	RESET_SYS

6.0 RAM AND ROM

6.1 References

None.

6.2 SRAM

The MEC170x contains two blocks of SRAM. he two SRAM blocks in the MEC170x total 480KB. Both SRAM blocks can be used for either program or data accesses. Performance is enhanced when program fetches and data accesses are to different SRAM blocks, but a program will operate correctly even if both program and data accesses are targeting the same block simultaneously.

- he first SRAM, which is optimized for code access, is 416KB
- The second SRAM, which is optimized for data access, is 64KB

6.3 ROM

The MEC170x contains a 64KB block of ROM, located at address 00000000h in the ARM address space. The ROM contains boot code that is executed after the de-assertion of RESET_SYS. The boot code loads an executable code image into SRAM. The ROM also includes a set of API functions that can be used for cryptographic functions, as well as loading SRAM with programs or data.

6.4 Additional Memory Regions

6.4.1 ALIAS RAM

The Alias RAM region, starting at address 20000000h, is an alias of the SRAM located at 118000h, and is the same size as that SRAM block. EC software can access memory in either the primary address or in the alias region; however, access is considerably slower to the alias region. The alias region exists in order to enable the ARM bit-band region located at address 20000000h.

6.4.2 RAM BIT-BAND REGION

The RAM bit-band region is an alias of the SRAM located at 118000h, except that each bit is aliased to bit 0 of a 32-bit doubleword in the bit-band region. The upper 31 bits in each doubleword of the bit-band region are always 0. The bit-band region is therefore 32 times the size of the SRAM region. It can be used for atomic updates of individual bits of the SRAM, and is a feature of the ARM architecture.

The bit-band region can only be accessed by the ARM processor. Accesses by any other bus master will cause a memory fault.

6.4.3 CRYPTOGRAPHIC RAM

The cryptographic RAM is used by the cryptographic API functions in the ROM

6.4.4 REGISTER BIT-BAND REGION

The Register bit-band region is an 32-to-1 alias of the device register space starting at address 40000000h and ending with the Host register space at 400FFFFF. Every bit in the register space is aliased to a byte in the Register bit-band region, and like the RAM bit-band region, can be used by EC software to read and write individual register bits. Only the EC Device Registers and the GPIO Registers can be accessed via the bit-band region.

A one bit write operation to a register bit in the bit-band region is implemented by the ARM processor by performing a read, a bit modification, followed by a write back to the same register. Software must be careful when using bit-banding if a register contains bits have side effects triggered by a read.

The bit-band region can only be accessed by the ARM processor. Accesses by any other bus master will cause a memory fault.

6.5 Memory Map

The memory map of the RAM and ROM is represented as follows:

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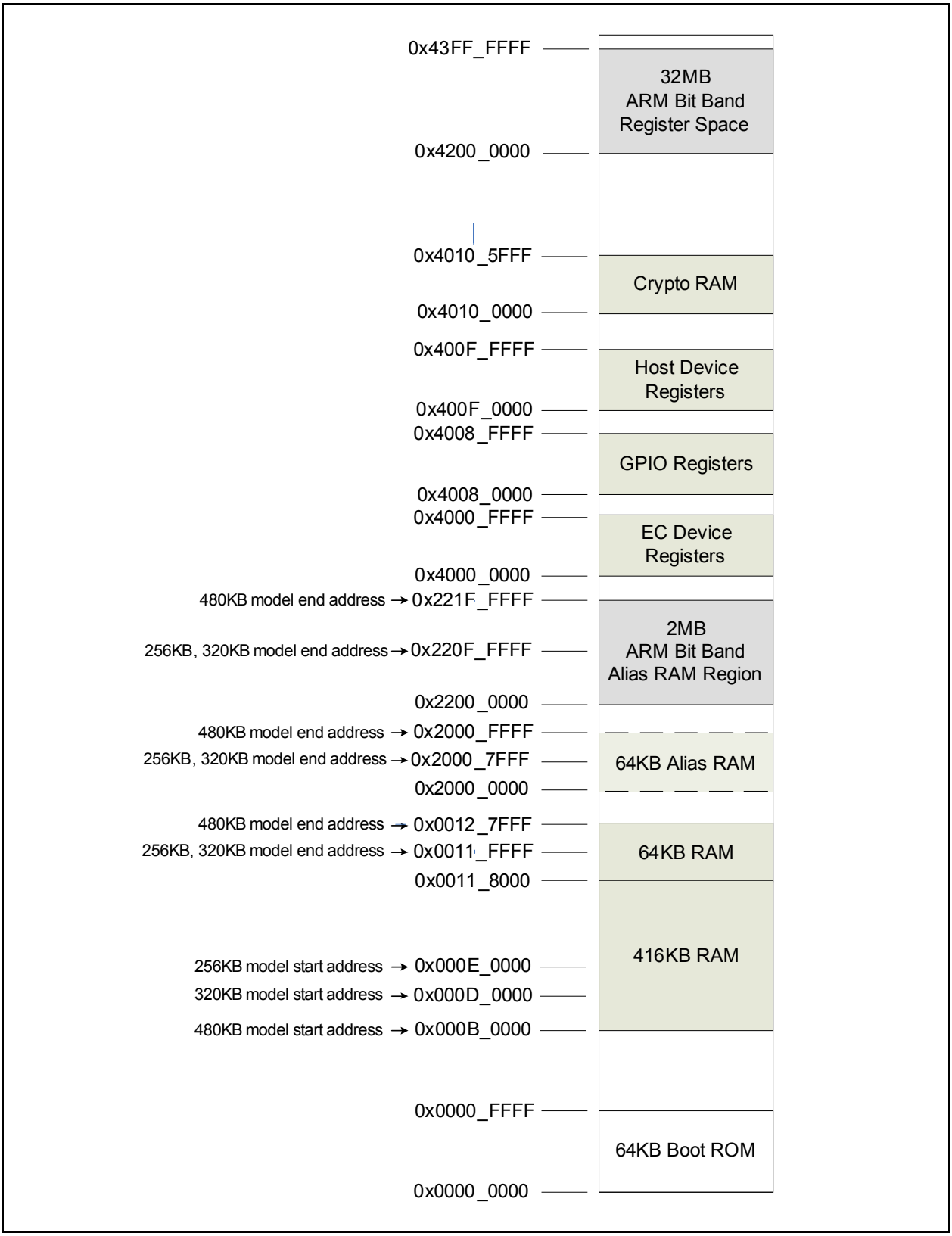
FIGURE 6-1: MEMORY LAYOUT



7.0 INTERNAL DMA CONTROLLER

7.1 Introduction

The Internal DMA Controller transfers data to/from the source from/to the destination. The firmware is responsible for setting up each channel. Afterwards either the firmware or the hardware may perform the flow control. The hardware flow control exists entirely inside the source device. Each transfer may be 1, 2, or 4 bytes in size, so long as the device supports a transfer of that size. Every device must be on the internal 32-bit address space.

7.2 References

No references have been cited for this chapter.

7.3 Terminology

TABLE 7-1: TERMINOLOGY

Term	Definition
DMA Transfer	This is a complete **DMA Transfer** which is done after the **Master Device** terminates the transfer, the Firmware Aborts the transfer or the DMA reaches its transfer limit. A DMA Transfer may consist of one or more data packets.
Data Packet	Each data packet may be composed of 1, 2, or 4 bytes. The size of the data packet is limited by the max size supported by both the source and the destination. Both source and destination will transfer the same number of bytes per packet.
Channel	The Channel is responsible for end-to-end (source-to-destination) Data Packet delivery.
Device	A Device may refer to a Master or Slave connected to the DMA Channel. Each DMA Channel may be assigned one or more devices.
Master Device	This is the master of the DMA, which determines when it is active. The Firmware is the master while operating in Firmware Flow Control. The Hardware is the master while operating in Hardware Flow Control. The Master Device in Hardware Mode is selected by **DMA Channel Control:Hardware Flow Control Device**. It is the index of the **Flow Control** Port.
Slave Device	The Slave Device is defined as the device associated with the targeted Memory Address.
Source	The DMA Controller moves data from the Source to the Destination. The Source provides the data. The Source may be either the Master or Slave Controller.
Destination	The DMA Controller moves data from the Source to the Destination. The Destination receives the data. The Destination may be either the Master or Slave Controller.

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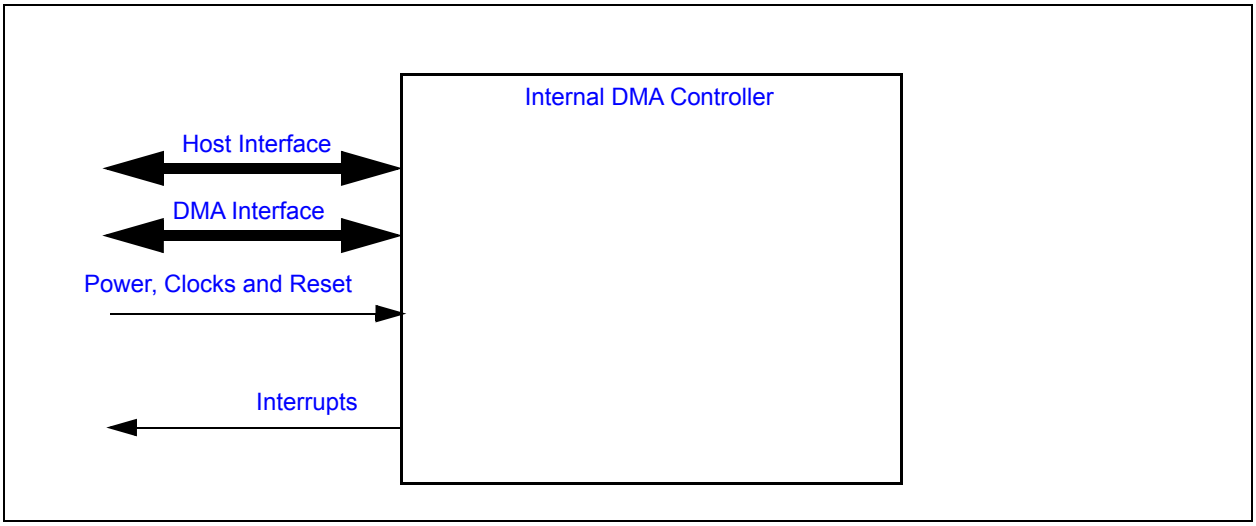
7.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 7-1: INTERNAL DMA CONTROLLER I/O DIAGRAM



7.4.1 SIGNAL DESCRIPTION

This block doesn't have any external signals that may be routed to the pin interface. This DMA Controller is intended to be used internally to transfer large amounts of data without the embedded controller being actively involved in the transfer.

7.4.2 HOST INTERFACE

The registers defined for the Internal DMA Controller are accessible by the various hosts as indicated in Section 7.9, "EC Registers".

7.4.3 DMA INTERFACE

Each DMA Master Device that may engage in a DMA transfer must have a compliant DMA interface. The following table lists the DMA Devices in the MEC170x.

TABLE 7-2: DMA CONTROLLER DEVICE SELECTION

Device Name	Device Number (Note 1)	Controller Source
SMB-I2C 0 Controller	0	Slave
	1	Master
SMB-I2C 1 Controller	2	Slave
	3	Master
SMB-I2C 2 Controller	4	Slave
	5	Master
SMB-I2C 3 Controller	6	Slave
	7	Master
SPI 0 Controller	8	Transmit
	9	Receive
SPI 1 Controller	10	Transmit
	11	Receive

Note 1: The Device Number is programmed into field HARDWARE_FLOW_CONTROL_DEVICE of the DMA Channel N Control Register register.

TABLE 7-3: DMA CONTROLLER MASTER DEVICES SIGNAL LIST

Device Name	Dev Num	Device Signal Name	Direction	Description
SMB-I2C 0 Controller	0	SMB-I2C_SDMA_Req	INPUT	DMA request control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Term	INPUT	DMA termination control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Done	OUTPUT	DMA termination control from DMA Controller to Slave channel.
	1	SMB-I2C_MDMA_Req	INPUT	DMA request control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Term	INPUT	DMA termination control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Done	OUTPUT	DMA termination control from DMA Controller to Master channel.
SMB-I2C 1 Controller	2	SMB-I2C_SDMA_Req	INPUT	DMA request control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Term	INPUT	DMA termination control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Done	OUTPUT	DMA termination control from DMA Controller to Slave channel.
	3	SMB-I2C_MDMA_Req	INPUT	DMA request control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Term	INPUT	DMA termination control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Done	OUTPUT	DMA termination control from DMA Controller to Master channel.
SMB-I2C 2 Controller	4	SMB-I2C_SDMA_Req	INPUT	DMA request control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Term	INPUT	DMA termination control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Done	OUTPUT	DMA termination control from DMA Controller to Slave channel.
	5	SMB-I2C_MDMA_Req	INPUT	DMA request control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Term	INPUT	DMA termination control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Done	OUTPUT	DMA termination control from DMA Controller to Master channel.

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TABLE 7-3: DMA CONTROLLER MASTER DEVICES SIGNAL LIST (CONTINUED)

Device Name	Dev Num	Device Signal Name	Direction	Description
SMB-I2C 3 Controller	6	SMB-I2C_SDMA_Req	INPUT	DMA request control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Term	INPUT	DMA termination control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Done	OUTPUT	DMA termination control from DMA Controller to Slave channel.
	7	SMB-I2C_MDMA_Req	INPUT	DMA request control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Term	INPUT	DMA termination control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Done	OUTPUT	DMA termination control from DMA Controller to Master channel.
SPI 0 Controller	8	SPI_TDMA_Req	INPUT	DMA request control from GP-SPI TX channel.
	9	SPI_RDMA_Req	INPUT	DMA request control from GP-SPI RX channel.
SPI 1 Controller	10	SPI_TDMA_Req	INPUT	DMA request control from GP-SPI TX channel.
	11	SPI_RDMA_Req	INPUT	DMA request control from GP-SPI RX channel.
Quad SPI Controller	12	QSPI_TDMA_Req	INPUT	DMA request control from Quad SPI TX channel.
	13	QSPI_RDMA_Req	INPUT	DMA request control from Quad SPI RX channel.

7.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

7.5.1 POWER DOMAINS

TABLE 7-4: POWER SOURCES

Name	Description
VTR	This power well sources the registers and logic in this block.

7.5.2 CLOCK INPUTS

TABLE 7-5: CLOCK INPUTS

Name	Description
48MHz	This clock signal drives selected logic (e.g., counters).

7.5.3 RESETS

TABLE 7-6: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in this block.
RESET	This reset is generated if either the RESET_SYS is asserted or the SOFT_RESET bit is asserted.

7.6 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 7-7: INTERRUPTS

Source	Description
DMA0	Direct Memory Access Channel 0 This signal is generated by the STATUS_DONE bit.
DMA1	Direct Memory Access Channel 1 This signal is generated by the STATUS_DONE bit.
DMA2	Direct Memory Access Channel 2 This signal is generated by the STATUS_DONE bit.
DMA3	Direct Memory Access Channel 3 This signal is generated by the STATUS_DONE bit.
DMA4	Direct Memory Access Channel 4 This signal is generated by the STATUS_DONE bit.
DMA5	Direct Memory Access Channel 5 This signal is generated by the STATUS_DONE bit.
DMA6	Direct Memory Access Channel 6 This signal is generated by the STATUS_DONE bit.
DMA7	Direct Memory Access Channel 7 This signal is generated by the STATUS_DONE bit.
DMA8	Direct Memory Access Channel 8 This signal is generated by the STATUS_DONE bit.
DMA9	Direct Memory Access Channel 9 This signal is generated by the STATUS_DONE bit.
DMA10	Direct Memory Access Channel 10 This signal is generated by the STATUS_DONE bit.
DMA11	Direct Memory Access Channel 11 This signal is generated by the STATUS_DONE bit.
DMA12	Direct Memory Access Channel 12 This signal is generated by the STATUS_DONE bit.
DMA13	Direct Memory Access Channel 13 This signal is generated by the STATUS_DONE bit.

7.7 Low Power Modes

The Internal DMA Controller may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

When the block is commanded to go to sleep it will place the DMA block into sleep mode only after all transactions on the DMA have been completed. For Firmware Flow Controlled transactions, the DMA will wait until it hits its terminal count and clears the Go control bit. For Hardware Flow Control, the DMA will go to sleep after either the terminal count is hit, or the Master device flags the terminate signal.

7.8 Description

The MEC170x features a 14 channel DMA controller. The DMA controller can autonomously move data from/to any DMA capable master device to/from any populated memory location. This mechanism allows hardware IP blocks to transfer large amounts of data into or out of memory without EC intervention.

The DMA has the following characteristics:

- Data is only moved 1 Data Packet at a time
- Data only moves between devices on the accessible via the internal 32-bit address space
- The DMA Controller has 14 DMA Channels
- Each DMA Channel may be configured to communicate with any DMA capable device on the 32-bit internal address space. Each device has been assigned a device number. See Section 7.4.3, "DMA Interface".

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The controller will accesses SRAM buffers only with incrementing addresses (that is, it cannot start at the top of a buffer, nor does it handle circular buffers automatically). The controller does not handle chaining (that is, automatically starting a new DMA transfer when one finishes).

7.8.1 CONFIGURATION

The DMA Controller is enabled via the ACTIVATE bit in DMA Main Control Register register.

Each DMA Channel must also be individually enabled via the CHANNEL_ACTIVATE bit in the DMA Channel N Activate Register to be operational.

Before starting a DMA transaction on a DMA Channel the host must assign a DMA Master to the channel via HARDWARE_FLOW_CONTROL_DEVICE. The host must not configure two different channels to the same DMA Master at the same time.

Data will be transfered between the DMA Master, starting at the programmed DEVICE_ADDRESS, and the targeted memory location, starting at the MEMORY_START_ADDRESS. The address for either the DMA Master or the targeted memory location may remain static or it may increment. To enable the DMA Master to increment its address set the INCREMENT_DEVICE_ADDRESS bit. To enable the targeted memory location to increment its addresses set the INCREMENT_MEMORY_ADDRESS. The DMA transfer will continue as long as the target memory address being accessed is less than the MEMORY_END_ADDRESS. If the DMA Controller detects that the memory location it is attempting to access on the Target is equal to the MEMORY_END_ADDRESS it will notify the DMA Master that the transaction is done. Otherwise the Data will be transferred in packets. The size of the packet is determined by the TRANSFER_SIZE.

7.8.2 OPERATION

The DMA Controller is designed to move data from one memory location to another.

7.8.2.1 Establishing a Connection

A DMA Master will initiate a DMA Transaction by requesting access to a channel. The DMA arbiter, which evaluates each channel request using a basic round robin algorithm, will grant access to the DMA master. Once granted, the channel will hold the grant until it decides to release it, by notifying the DMA Controller that it is done.

If Firmware wants to prevent any other channels from being granted while it is active it can set the LOCK_CHANNEL bit.

7.8.2.2 Initiating a Transfer

Once a connection is established the DMA Master will issue a DMA request to start a DMA transfer. If Firmware wants to have a transfer request serviced it must set the RUN bit to have its transfer requests serviced.

Firmware can initiate a transaction by setting the TRANSFER_GO bit. The DMA transfer will remain active until either the Master issues a Terminate or the DMA Controller signals that the transfer is DONE. Firmware may terminate a transaction by setting the TRANSFER_ABORT bit.

Note:	Before initiating a DMA transaction via firmware the hardware flow control must be disabled via the DISABLE_HARDWARE_FLOW_CONTROL bit.

Data may be moved from the DMA Master to the targeted Memory address or from the targeted Memory Address to the DMA Master. The direction of the transfer is determined by the TRANSFER_DIRECTION bit.

Once a transaction has been initiated firmware can use the STATUS_DONE bit to determine when the transaction is completed. This status bit is routed to the interrupt interface. In the same register there are additional status bits that indicate if the transaction completed successfully or with errors. These bits are OR'd together with the STATUS_DONE bit to generate the interrupt event. Each status be may be individually enabled/disabled from generating this event.

7.8.2.3 Reusing a DMA Channel

After a DMA Channel controller has completed, firmware **must** clear both the DMA Channel N Control Register and the DMA Channel N Interrupt Status Register. After both have been cleared to 0, the Channel Control Register can then be configured for the next transaction.

7.8.2.4 CRC Generation

A CRC generator can be attached to a DMA channel in order to generate a CRC on the data as it is transfered from the source to the destination. The CRC used is the CRC-32 algorithm used in IEEE 802.3 and many other protocols, using the polynomial $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$. The CRC generation takes

place in parallel with the data transfer; enabling CRC will not increase the time to complete a DMA transaction. The CRC generator has the optional ability to automatically transfer the generated CRC to the destination after the data transfer has completed.

CRC generation is subject to a number of restrictions:

- The CRC is only generated on channels that have the CRC hardware. See Table 7-10, "Channel Register Summary" for a definition of which channels have the ability to generate a CRC
- The DMA transfer must be 32-bits
- If CRC is enabled, DMA interrupts are inhibited until the CRC is completed, including the optional post-transfer copy of it is enabled
- The CRC must be initialized by firmware. The value FFFFFFFFh must be written to the Data Register in order to initialize the generator for the standard CRC-32-IEEE algorithm
- The CRC will bit-order reverse In and Out, and Invert Out, as required by the CRC algorithm

7.8.2.5 Block Fill Option

A Fill engine can be attached to a DMA channel in order to provide a fast mechanism to set a block of memory to a fixed value (for example, clearing a block of memory to zero). The block fill operation runs approximately twice as fast as a memory-to-memory copy.

In order to fill memory with a constant value, firmware **must** configure the channel in the following order:

1. Set the DMA Channel N Fill Data Register to the desired fill value
2. Set the DMA Channel N Fill Enable Register to '1b', enabling the Fill engine
3. Set the DMA Channel N Control Register to the following values:
   - RUN = 0
   - TRANSFER_DIRECTION = 0 (memory destination)
   - INCREMENT_MEMORY_ADDRESS = 1 (increment memory address after each transfer)
   - INCREMENT_DEVICE_ADDRESS = 1
   - DISABLE_HARDWARE_FLOW_CONTROL = 1 (no hardware flow control)
   - TRANSFER_SIZE = 1, 2 or 4 (as required)
   - TRANSFER_ABORT = 0
   - TRANSFER_GO = 1 (this starts the transfer)

7.9 EC Registers

The DMA Controller consists of a Main Block and a number of Channels. Table 7-9, "Main Register Summary" lists the registers in the Main Block and Table 7-10, "Channel Register Summary" lists the registers in each channel. Addresses for each register are determined by adding the offset to the Base Address for the DMA Controller Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

Registers are listed separately for the Main Block of the DMA Controller and for a DMA Channel. Each Channel has the same set of registers. The absolute register address for registers in each channel are defined by adding the Base Address for the DMA Controller Block, the Offset for the Channel shown in Table 7-8, "DMA Channel Offsets" to the offsets listed in Table 7-9, "Main Register Summary" or Table 7-10, "Channel Register Summary".

TABLE 7-8: DMA CHANNEL OFFSETS

Instance Name	Channel Number	Offset
DMA Controller	Main Block	000h
DMA Controller	0	040h
DMA Controller	1	080h
DMA Controller	2	0C0h
DMA Controller	3	100h
DMA Controller	4	140h
DMA Controller	5	180h
DMA Controller	6	1C0h
DMA Controller	7	200h

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TABLE 7-8: DMA CHANNEL OFFSETS (CONTINUED)

Instance Name	Channel Number	Offset
DMA Controller	8	240h
DMA Controller	9	28h
DMA Controller	10	2C0h
DMA Controller	11	300h
DMA Controller	12	340h
DMA Controller	13	380h

TABLE 7-9: MAIN REGISTER SUMMARY

Offset	Register Name
00h	DMA Main Control Register
04h	DMA Data Packet Register

7.9.1 DMA MAIN CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	-	-
1	SOFT_RESET Soft reset the entire module. This bit is self-clearing.	W	0b	-
0	ACTIVATE Enable the blocks operation. 1=Enable block. Each individual channel must be enabled separately. 0=Disable all channels.	R/WS	0b	RESET

7.9.2 DMA DATA PACKET REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	DATA_PACKET Debug register that has the data that is stored in the Data Packet. This data is read data from the currently active transfer source.	R	0000h	-

TABLE 7-10: CHANNEL REGISTER SUMMARY

Offset	Register Name (Note 1)
00h	DMA Channel N Activate Register

Note 1: The letter 'N' following DMA Channel indicates the Channel Number. Each Channel implemented will have these registers to determine that channel's operation.

2: These registers are only present on DMA Channel 0. They are reserved on all other channels.

3: These registers are only present on DMA Channel 1. They are reserved on all other channels.

TABLE 7-10: CHANNEL REGISTER SUMMARY (CONTINUED)

Offset	Register Name (Note 1)
04h	DMA Channel N Memory Start Address Register
08h	DMA Channel N Memory End Address Register
0Ch	DMA Channel N Device Address
10h	DMA Channel N Control Register
14h	DMA Channel N Interrupt Status Register
18h	DMA Channel N Interrupt Enable Register
1Ch	TEST
20h (Note 2)	DMA Channel N CRC Enable Register
24h (Note 2)	DMA Channel N CRC Data Register
28h (Note 2)	DMA Channel N CRC Post Status Register
2Ch (Note 2)	TEST
20h (Note 3)	DMA Channel N Fill Enable Register
24h (Note 3)	DMA Channel N Fill Data Register
28h (Note 3)	DMA Channel N Fill Status Register
2Ch (Note 3)	TEST

Note 1: The letter 'N' following DMA Channel indicates the Channel Number. Each Channel implemented will have these registers to determine that channel's operation.

2: These registers are only present on DMA Channel 0. They are reserved on all other channels.

3: These registers are only present on DMA Channel 1. They are reserved on all other channels.

7.9.3 DMA CHANNEL N ACTIVATE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	CHANNEL_ACTIVATE Enable this channel for operation. The DMA Main Control:Activate must also be enabled for this channel to be operational.	R/W	0h	RESET

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7.9.4 DMA CHANNEL N MEMORY START ADDRESS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	MEMORY_START_ADDRESS This is the starting address for the Memory device. This field is updated by Hardware after every packet transfer by the size of the transfer, as defined by DMA Channel Control:Channel Transfer Size while the DMA Channel Control:Increment Memory Address is Enabled. The Memory device is defined as the device that is the slave device in the transfer. With Hardware Flow Control, the Memory device is the device that is not connected to the Hardware Flow Controlling device.	R/W	0000h	RESET

7.9.5 DMA CHANNEL N MEMORY END ADDRESS REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	MEMORY_END_ADDRESS This is the ending address for the Memory device. This will define the limit of the transfer, so long as DMA Channel Control:Increment Memory Address is Enabled. When the Memory Start Address is equal to this value, the DMA will terminate the transfer and flag the status DMA Channel Interrupt:Status Done. **Note:** If the TRANSFER_SIZE field in the DMA Channel N Control Register is set to 2 (for 2-byte transfers, this address **must** be evenly divisible by 2 or the transfer will not terminate properly. If the TRANSFER_SIZE field is set to 4 (for 4-byte transfers, this address **must** be evenly divisible by 4 or the transfer will not terminate properly.	R/W	0000h	RESET

7.9.6 DMA CHANNEL N DEVICE ADDRESS

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	DEVICE_ADDRESS This is the Master Device address. This is used as the address that will access the Device on the DMA. The Device is defined as the Master of the DMA transfer; as in the device that is controlling the Hardware Flow Control. This field is updated by Hardware after every Data Packet transfer by the size of the transfer, as defined by DMA Channel Control:Transfer Size while the DMA Channel Control:Increment Device Address is Enabled.	R/W	0000h	RESET

7.9.7 DMA CHANNEL N CONTROL REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:26	Reserved	R	-	-
25	TRANSFER_ABORT This is used to abort the current transfer on this DMA Channel. The aborted transfer will be forced to terminate immediately.	R/W	0h	RESET
24	TRANSFER_GO This is used for the **Firmware Flow Control** DMA transfer. This is used to start a transfer under the **Firmware Flow Control**. Do not use this in conjunction with the **Hardware Flow Control**; DISABLE_HARDWARE_FLOW_CONTROL must be set in order for this field to function correctly.	R/W	0h	RESET
23	Reserved	R	-	-
22:20	TRANSFER_SIZE This is the transfer size in Bytes of each Data Packet transfer. The transfer size must be a legal transfer size. Valid sizes are 1, 2 and 4 Bytes.	R/W	0h	RESET
19	DISABLE_HARDWARE_FLOW_CONTROL Setting this bit to '1'b will Disable **Hardware Flow Control**. When disabled, any DMA Master device attempting to communicate to the DMA over the DMA Flow Control Interface will be ignored. This should be set before using the DMA channel in **Firmware Flow Control** mode.	R/W	0h	RESET
18	LOCK_CHANNEL This is used to lock the arbitration of the Channel Arbiter on this channel once this channel is granted. Once this is locked, it will remain on the arbiter until it has completed it transfer (either the Transfer Aborted, Transfer Done or Transfer Terminated conditions). **Note:** This setting may starve other channels if the locked channel takes an excessive period of time to complete.	R/W	0h	RESET
17	INCREMENT_DEVICE_ADDRESS If this bit is '1'b, the DEVICE_ADDRESS will be incremented by TRANSFER_SIZE after every Data Packet transfer	R/W	0h	RESET
16	INCREMENT_MEMORY_ADDRESS If this bit is '1'b, the MEMORY_START_ADDRESS will be incremented by TRANSFER_SIZE after every Data Packet transfer **Note:** If this is not set, the DMA will never terminate the transfer on its own. It will have to be terminated through the Hardware Flow Control or through a DMA Channel Control:Transfer Abort.	R/W	0h	RESET

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Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:9	HARDWARE_FLOW_CONTROL_DEVICE This is the device that is connected to this channel as its Hardware Flow Control master. The Flow Control Interface is a bus with each master concatenated onto it. This selects which bus index of the concatenated Flow Control Interface bus is targeted towards this channel.	R/W	0h	RESET
8	TRANSFER_DIRECTION This determines the direction of the DMA Transfer. 1=Data Packet Read from MEMORY_START_ADDRESS followed by Data Packet Write to DEVICE_ADDRESS 0=Data Packet Read from DEVICE_ADDRESS followed by Data Packet Write to MEMORY_START_ADDRESS	R/W	0h	RESET
7:6	Reserved	R	-	-
5	BUSY This is a status signal. 1=The DMA Channel is busy (FSM is not IDLE) 0=The DMA Channel is not busy (FSM is IDLE)	R	0h	RESET
4:3	TEST	R	0h	RESET
2	DONE This is a status signal. It is only valid while RUN is Enabled. This is the inverse of the **DMA Channel Control:Busy** field, except this is qualified with the **DMA Channel Control:Run** field. 1=Channel is done 0=Channel is not done or it is OFF	R	0h	RESET
1	REQUEST This is a status field. 1=There is a transfer request from the Master Device 0=There is no transfer request from the Master Device	R	0h	RESET
0	RUN This is a control field. It only applies to **Hardware Flow Control** mode. 1=This channel is enabled and will service transfer requests 0=This channel is disabled. All transfer requests are ignored	R/W	0h	RESET

7.9.8 DMA CHANNEL N INTERRUPT STATUS REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:3	Reserved	R	-	-
2	STATUS_DONE This is an interrupt source register. This flags when the DMA Channel has completed a transfer successfully on its side. A completed transfer is defined as when the DMA Channel reaches its limit; **Memory Start Address** equals **Memory End Address**. A completion due to a **Hardware Flow Control Terminate** will not flag this interrupt. 1=MEMORY_START_ADDRESS equals MEMORY_END_ADDRESS 0=MEMORY_START_ADDRESS does not equal MEMORY_END_ADDRESS	R/WC	0h	RESET
1	STATUS_FLOW_CONTROL This is an interrupt source register. This flags when the DMA Channel has encountered a **Hardware Flow Control Request** after the DMA Channel has completed the transfer. This means the Master Device is attempting to overflow the DMA. 1=Hardware Flow Control is requesting after the transfer has completed 0=No Hardware Flow Control event		0h	RESET
0	STATUS_BUS_ERROR This is an interrupt source register. This flags when there is an Error detected over the internal 32-bit Bus. 1=Error detected.	R/WC	0h	RESET

7.9.9 DMA CHANNEL N INTERRUPT ENABLE REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:3	Reserved	R	-	-
2	STATUS_ENABLE_DONE This is an interrupt enable for STATUS_DONE. 1=Enable Interrupt 0=Disable Interrupt	R/W	0h	RESET
1	STATUS_ENABLE_FLOW_CONTROL_ERROR This is an interrupt enable for STATUS_FLOW_CONTROL. 1=Enable Interrupt 0=Disable Interrupt	R/W	0h	RESET

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Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	STATUS_ENABLE_BUS_ERROR This is an interrupt enable for STATUS_BUS_ERROR. 1=Enable Interrupt 0=Disable Interrupt	R/W	0h	RESET

7.9.10 DMA CHANNEL N CRC ENABLE REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	CRC_POST_TRANSFER_ENABLE The bit enables the transfer of the calculated CRC-32 after the completion of the DMA transaction. If the DMA transaction is aborted by either firmware or an internal bus error, the transfer will not occur. If the target of the DMA transfer is a device and the device signaled the termination of the DMA transaction, the CRC post transfer will not occur. 1=Enable the transfer of CRC-32 for DMA Channel N after the DMA transaction completes 0=Disable the automatic transfer of the CRC	R/W	0h	RESET
0	CRC_MODE_ENABLE 1=Enable the calculation of CRC-32 for DMA Channel N 0=Disable the calculation of CRC-32 for DMA Channel N	R/W	0h	RESET

7.9.11 DMA CHANNEL N CRC DATA REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CRC Writes to this register initialize the CRC generator. Reads from this register return the output of the CRC that is calculated from the data transfered by DMA Channel N. The output of the CRC generator is bit-reversed and inverted on reads, as required by the CRC-32-IEEE definition. A CRC can be accumulated across multiple DMA transactions on Channel N. If it is necessary to save the intermediate CRC value, the result of the read of this register must be bit-reversed and inverted before being written back to this register.	R/W	0h	RESET

7.9.12 DMA CHANNEL N CRC POST STATUS REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3	CRC_DATA_READY This bit is set to ‘1b’ when the DMA controller is processing the post-transfer of the CRC data. This bit is cleared to ‘0b’ when the post-transfer completes.	R	0h	RESET
2	CRC_DATA_DONE This bit is set to ‘1b’ when the DMA controller has completed the post-transfer of the CRC data. This bit is cleared to ‘0b’ when the a new DMA transfer starts.	R	0h	RESET
1	CRC_RUNNING This bit is set to ‘1b’ when the DMA controller starts the post-transfer transmission of the CRC. It is only set when the post-transfer is enabled by the CRC_POST_TRANSFER_ENABLE field. This bit is cleared to ‘0b’ when the post-transfer completes.	R	0h	RESET
0	CRC_DONE This bit is set to ‘1b’ when the CRC calculation has completed from either normal or forced termination. It is cleared to ‘0b’ when the DMA controller starts a new transfer on the channel.	R	0h	RESET

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7.9.13 DMA CHANNEL N FILL ENABLE REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	FILL_MODE_ENABLE 1=Enable the calculation of CRC-32 for DMA Channel N 0=Disable the calculation of CRC-32 for DMA Channel N	R/W	0h	RESET

7.9.14 DMA CHANNEL N FILL DATA REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	DATA This is the data pattern used to fill memory.	R/W	0h	RESET

7.9.15 DMA CHANNEL N FILL STATUS REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	FILL_RUNNING This bit is ‘1b’ when the Fill operation starts and is cleared to ‘0b’ when the Fill operation completes.	R	0h	RESET
0	FILL_DONE This bit is set to ‘1b’ when the Fill operation has completed from either normal or forced termination. It is cleared to ‘0b’ when the DMA controller starts a new transfer on the channel.	R	0h	RESET

8.0 EC INTERRUPT AGGREGATOR

8.1 Introduction

The EC Interrupt Aggregator works in conjunction with the processor's interrupt interface to handle hardware interrupts and exceptions.

Exceptions are synchronous to instructions, are not maskable, and have higher priority than interrupts. All three exceptions - reset, memory error, and instruction error - are hardwired directly to the processor. Interrupts are typically asynchronous and are maskable.

Interrupts classified as wake events can be recognized without a running clock, e.g., while the MEC170x is in sleep state.

This chapter focuses on the EC Interrupt Aggregator. Please refer to embedded controller's documentation for more information on interrupt and exception handling.

8.2 References

None

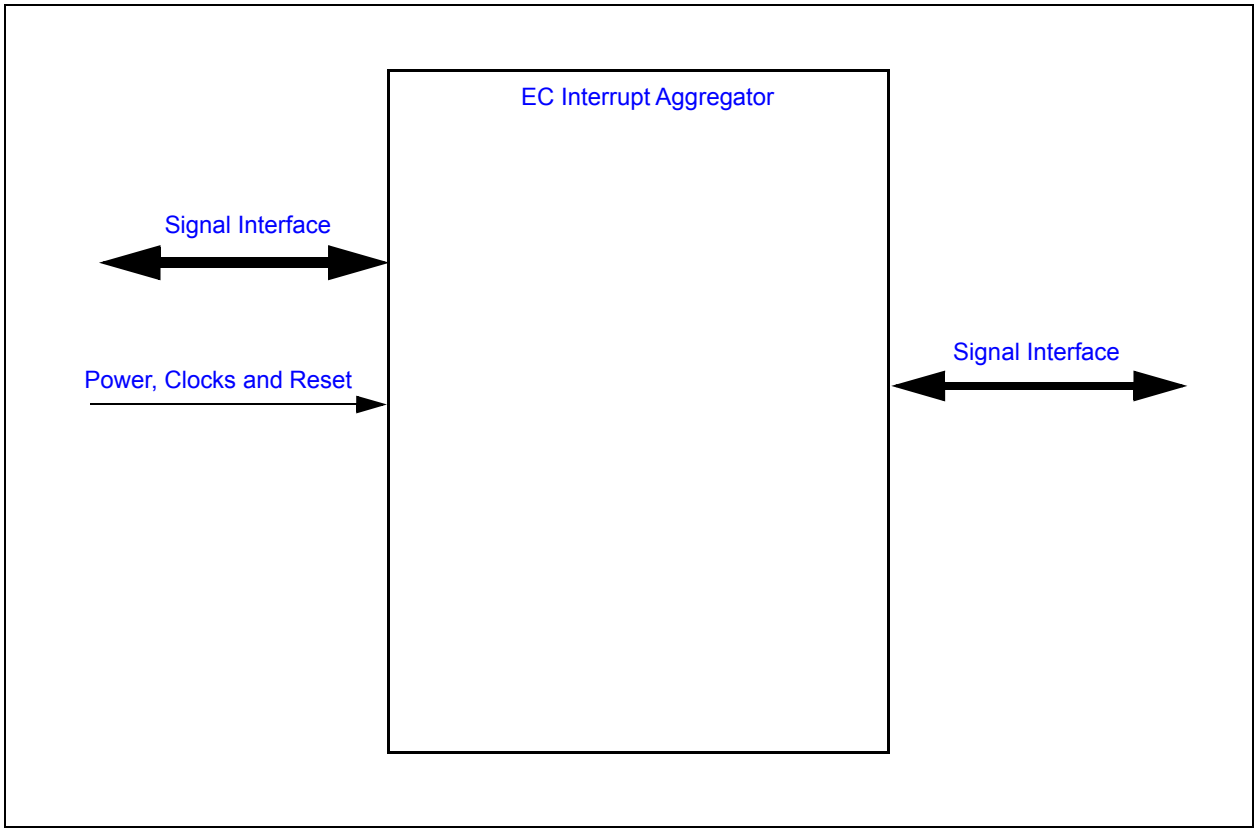
8.3 Terminology

None

8.4 Interface

This block is an IP block designed to be incorporated into a chip. It is designed to be accessed externally via the pin interface and internally via a registered host interface. The following diagram illustrates the various interfaces to the block.

FIGURE 8-1: EC INTERRUPT AGGREGATOR INTERFACE DIAGRAM



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8.5 Signal Description

8.5.1 SIGNAL INTERFACE

There are no external signals for this block.

8.6 Host Interface

The registers defined for the EC Interrupt Aggregator are only accessible by the embedded controller via the EC Registers.

8.7 Power, Clocks and Reset

8.7.1 BLOCK POWER DOMAIN

TABLE 8-1: BLOCK POWER

Power Well Source	Effect on Block
VTR	The EC Interrupt Aggregator block and registers operate on this single power well.

8.7.2 BLOCK CLOCKS

None

8.7.3 BLOCK RESET

TABLE 8-2: BLOCK RESETS

Reset Name	Reset Description
RESET_SYS	This signal is used to indicate when the VTR logic and registers in this block are reset.

8.8 Interrupts

This block aggregates all the interrupts targeted for the embedded controller into the Source Registers defined in Section 8.11, "EC Registers". The unmasked bits of each source register are then OR'd together and routed to the embedded controller's interrupt interface. The name of each Source Register identifies the IRQ number of the interrupt port on the embedded controller.

8.9 Low Power Modes

This block always automatically adjusts to operate in the lowest power mode.

8.10 Description

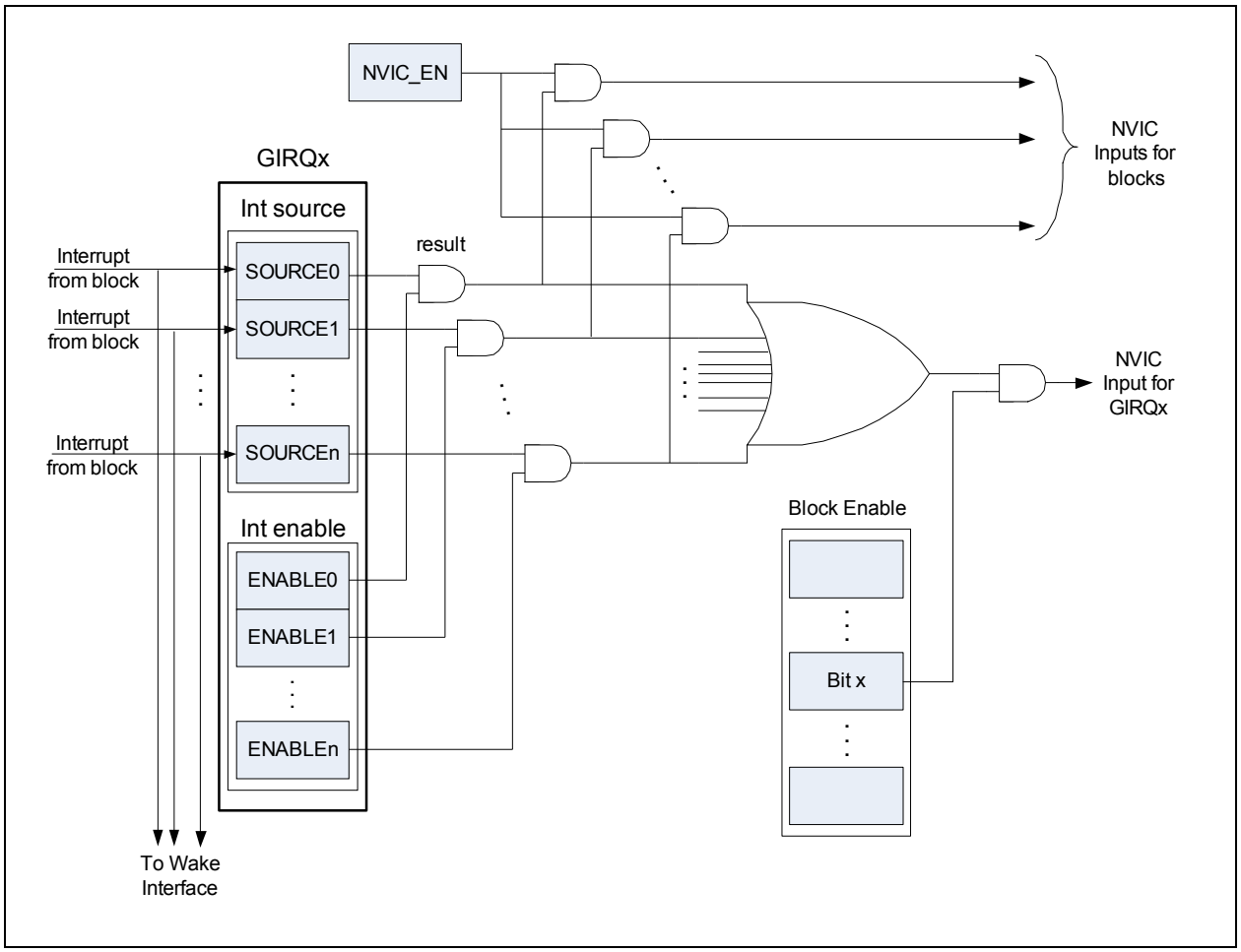
The interrupt generation logic is made of groups of signals, each of which consist of a Status register, a Enable Set register, and Enable Clear register and a Result register.

The Status and Enable are latched registers. There is one set of Enable register bits; both the Enable Set and Enable Clear registers return the same result when read. The Enable Set interface is used to set individual bits in the Enable register, and the Enable Clear is used to clear individual bits. The Result register is a bit by bit AND function of the Source and Enable registers. All the bits of the Result register are OR'ed together and AND'ed with the corresponding bit in the Block Select register to form the interrupt signal that is routed to the ARM interrupt controller.

The Result register bits may also be enabled to the NVIC block via the NVIC_EN bit in the Interrupt Control Register register. See Chapter 46.0, "EC Subsystem Registers"

Section 8.10.1 shows a representation of the interrupt structure.

FIGURE 8-2: INTERRUPT STRUCTURE



8.10.1 AGGREGATED INTERRUPTS

All interrupts are routed to the ARM processor through the ARM Nested Vectored Interrupt Controller (NVIC). As shown in Figure 8-2, "Interrupt Structure", all interrupt sources are aggregated into the GIRQx Source registers. In many cases, the Result bit for an individual interrupt source is tied directly to the NVIC. These interrupts are shown in the “Direct NVIC” column in the Interrupt Bit Assignments table. In addition, all GIRQx can also generate an interrupt to the NVIC when any of the enabled interrupts in its group is asserted. The NVIC vectors for the aggregated GIRQ interrupts are shown tin the “Agg NVIC” column.

Firmware should not enable the group GIRQ NVIC interrupt at the same time individual direct interrupts for members of the group are enabled. If both are enabled, the processor will receive two interrupts for an event, one from the GIRQ and one from the direct interrupt.

Note:	The four Soft Interrupts that are defined by the RTOS Timer do not have individual NVIC vectors. If the use of the SWI interrupts is required, then all interrupts in the GIRQ must disable the individual NVIC vectors.

8.10.2 WAKE GENERATION

The EC Interrupt Aggregator notifies the Chip Power Management Features to wake the system when it detects a wake capable event has occurred. This logic requires no clocks.

The interrupt sources AND’ed with the corresponding Enable bit will be OR’ed to produce a wake event

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The wake up sources are identified with a “Y” in the “WAKE” column of the Bit definitions table for each IRQ’s Source Register.

8.10.2.1 Configuring Wake Interrupts

All GPIO inputs are wake-capable. In order for a GPIO input to wake the MEC170x from a sleep state, the Interrupt Detection field of the GPIO Pin Control Register must be set to Rising Edge Triggered, Falling Edge Triggered, or Either Edge Triggered. If the Interrupt Detection field is set to any other value, a GPIO input will not trigger a wake interrupt.

Some of the Wake Capable Interrupts are triggered by activity on pins that are shared with a GPIO. These interrupts will only trigger a wake if the Interrupt Detection field of the corresponding GPIO Pin Control Register is set to Rising Edge Triggered, Falling Edge Triggered, or Either Edge Triggered.

8.10.3 INTERRUPT SUMMARY

Interrupt bit assignments, including wake capabilities and NVIC vector locations, are shown in the Interrupt Aggregator Bit Assignments Table in Section 3.0, "Device Inventory". The table lists all possible interrupt sources; the register bits for any interrupt source, such as a GPIO, that is not implemented in a particular part are reserved.

8.10.4 DISABLING INTERRUPTS

The Block Enable Clear Register and Block Enable Set Register should not be used for disabling and enabling interrupts for software operations i.e., critical sections. The ARM enable disable mechanisms should be used.

8.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for of the EC Interrupt Aggregator Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 8-3: REGISTER SUMMARY

Offset	Register Name
00h	GIRQ8 Source Register
04h	GIRQ8 Enable Set Register
08h	GIRQ8 Result Register
0Ch	GIRQ8 Enable Clear Register
10h	Reserved
14h	GIRQ9 Source Register
18h	GIRQ9 Enable Set Register
1Ch	GIRQ9 Result Register
20h	GIRQ9 Enable Clear Register
24h	Reserved
28h	GIRQ10 Source Register
2Ch	GIRQ10 Enable Set Register
30h	GIRQ10 Result Register
34h	GIRQ10 Enable Clear Register
38h	Reserved
3Ch	GIRQ11 Source Register
40h	GIRQ11 Enable Set Register
44h	GIRQ11 Result Register
48h	GIRQ11 Enable Clear Register
4Ch	Reserved
50h	GIRQ12 Source Register
54h	GIRQ12 Enable Set Register
58h	GIRQ12 Result Register

TABLE 8-3: REGISTER SUMMARY (CONTINUED)

Offset	Register Name
5Ch	GIRQ12 Enable Clear Register
60h	Reserved
64h	GIRQ13 Source Register
68h	GIRQ13 Enable Set Register
6Ch	GIRQ13 Result Register
70h	GIRQ13 Enable Clear Register
74h	Reserved
78h	GIRQ14 Source Register
7Ch	GIRQ14 Enable Set Register
80h	GIRQ14 Result Register
84h	GIRQ14 Enable Clear Register
88h	Reserved
8Ch	GIRQ15 Source Register
90h	GIRQ15 Enable Set Register
94h	GIRQ15 Result Register
98h	GIRQ15 Enable Clear Register
9Ch	Reserved
A0h	GIRQ16 Source Register
A4h	GIRQ16 Enable Set Register
A8h	GIRQ16 Result Register
ACh	GIRQ16 Enable Clear Register
B0h	Reserved
B4h	GIRQ17 Source Register
B8h	GIRQ17 Enable Set Register
BCh	GIRQ17 Result Register
C0h	GIRQ17 Enable Clear Register
C4h	Reserved
C8h	GIRQ18 Source Register
CCh	GIRQ18 Enable Set Register
D0h	GIRQ18 Result Register
D4h	GIRQ18 Enable Clear Register
D8h	Reserved
DCh	GIRQ19 Source Register
E0h	GIRQ19 Enable Set Register
E4h	GIRQ19 Result Register
E8h	GIRQ19 Enable Clear Register
ECh	Reserved
F0h	GIRQ20 Source Register
F4h	GIRQ20 Enable Set Register
F8h	GIRQ20 Result Register
FCh	GIRQ20 Enable Clear Register
100h	Reserved
104h	GIRQ21 Source Register
108h	GIRQ21 Enable Set Register

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TABLE 8-3: REGISTER SUMMARY (CONTINUED)

Offset	Register Name
10Ch	GIRQ21 Result Register
110h	GIRQ21 Enable Clear Register
114h	Reserved
118h	GIRQ22 Source Register
11Ch	GIRQ22 Enable Set Register
120h	GIRQ22 Result Register
124h	GIRQ22 Enable Clear Register
128h	Reserved
12Ch	GIRQ23 Source Register
130h	GIRQ23 Enable Set Register
134h	GIRQ23 Result Register
138h	GIRQ23 Enable Clear Register
13Ch	Reserved
140h	GIRQ24 Source Register
144h	GIRQ24 Enable Set Register
148h	GIRQ24 Result Register
14Ch	GIRQ24 Enable Clear Register
150h	Reserved
154h	GIRQ25 Source Register
158h	GIRQ25 Enable Set Register
15Ch	GIRQ25 Result Register
160h	GIRQ25 Enable Clear Register
164h	Reserved
168h	GIRQ26 Source Register
16Ch	GIRQ26 Enable Set Register
170h	GIRQ26 Result Register
174h	GIRQ26 Enable Clear Register
200h	Block Enable Set Register
204h	Block Enable Clear Register
208h	Block IRQ Vector Register

All of the GIRQx Source, Enable Set, Enable Clear and Result registers have the same format. The following tables define the generic format for each of these registers. The bit definitions are defined in the sections that follow.

The behavior of the enable bit controlled by the GIRQx Enable Set and GIRQx Enable Clear Registers, the GIRQx Source bit, and the GIRQx Result bit is illustrated in Section 8.10.1, "Aggregated Interrupts".

8.11.1 GIRQ SOURCE REGISTERS

All of the GIRQx Source registers have the same format. The following table defines the generic format for each of these registers. The bit definitions are defined in the Interrupt Aggregator Bit Assignments Table in Section 3.0, "Device Inventory". Unassigned bits are Reserved and return 0.

Note:	If a GPIO listed in the tables does not appear in the pin list of a particular device, then the bits for that GPIO in the GIRQx Source, GIRQx Enable Clear, GIRQx Enable Set and GIRQx Result are reserved.

Offset	See Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:0	GIRQX_SOURCE The GIRQx Source bits are R/WC sticky status bits indicating the state of interrupt before the interrupt enable bit.	R/WC	0h	RESET_SYS

8.11.2 GIRQ ENABLE SET REGISTERS

All of the GIRQx Enable Set registers have the same format. The following table defines the generic format for each of these registers. Unassigned bits are Reserved and return 0.

Offset	See Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:0	GIRQX_ENABLE_SET Each GIRQx bit can be individually enabled to assert an interrupt event. Reads always return the current value of the internal GIRQX_ENABLE bit. The state of the GIRQX_ENABLE bit is determined by the corresponding GIRQX_ENABLE_SET bit and the GIRQX_ENABLE_CLEAR bit. (0=disabled, 1-enabled) 1=The corresponding interrupt in the GIRQx Source Register is enabled 0=No effect	R/WS	0h	RESET_SYS

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8.11.3 GIRQ ENABLE CLEAR REGISTERS

All of the GIRQx Enable Clear registers have the same format. The following table defines the generic format for each of these registers. Unassigned bits are Reserved and return 0.

Offset	See Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:0	GIRQX_ENABLE_CLEAR Each GIRQx bit can be individually enabled to assert an interrupt event. Reads always return the current value of the internal GIRQX_ENABLE bit. The state of the GIRQX_ENABLE bit is determined by the corresponding GIRQX_ENABLE_SET bit and the GIRQX_ENABLE_CLEAR bit. (0=disabled, 1-enabled) 1=The corresponding interrupt in the GIRQx Source Register is disabled 0=No effect	R/WC	0h	RESET_SYS

8.11.4 GIRQ RESULT REGISTERS

Offset	See Section 3.0, "Device Inventory"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	1h	-
30:0	GIRQX_RESULT The GIRQX_RESULT bits are Read-Only status bits indicating the state of an interrupt. The RESULT is asserted ‘1’b when both the GIRQX_SOURCE bit and the corresponding GIRQX_ENABLE bit are ‘1’b.	R	0h	RESET_SYS

8.11.5 BLOCK ENABLE SET REGISTER

Offset	200h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:27	Reserved	R	-	-
26:8	IRQ_VECTOR_ENABLE_SET Each GIRQx register can be individually enabled to assert an interrupt event. Reads always return the current value of the enable bits for each of the GIRQs. The state of the GIRQX_ENABLE bit is determined by the corresponding GIRQX_ENABLE_SET bit and the GIRQX_ENABLE_CLEAR bit. (0=disabled, 1-enabled) 1=Interrupts in the GIRQx Source Register may be enabled 0=No effect	R/WS	0h	RESET_SYS
7:0	Reserved	R	-	-

8.11.6 BLOCK ENABLE CLEAR REGISTER

Offset	204h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:27	Reserved	R	-	-
26:8	IRQ_VECTOR_ENABLE_CLEAR Each GIRQx register can be individually disabled to inhibit interrupt events. Reads always return the current value of the internal GIRQX_ENABLE bit. The state of the GIRQX_ENABLE bit is determined by the corresponding GIRQX_ENABLE_SET bit and the GIRQX_ENABLE_CLEAR bit. (0=disabled, 1-enabled) 1=All interrupts in the GIRQx Source Register are disabled 0=No effect	R/WC	0h	RESET_SYS
7:0	Reserved	R	-	-

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8.11.7 BLOCK IRQ VECTOR REGISTER

Offset	208h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:27	Reserved	R	0h	-
26:8	IRQ_VECTOR Each bit in this field reports the status of the group GIRQ interrupt assertion to the NVIC. If the GIRQx interrupt is disabled as a group, by the Block Enable Clear Register, then the corresponding bit will be ‘0’b and no interrupt will be asserted.	R	0h	RESET_SYS
7:0	Reserved	R	0h	-

9.0 LPC INTERFACE

9.1 Introduction

The Intel® Low Pin Count (LPC) Interface is the LPC Interface used by the system host to configure the chip and communicate with the logical devices implemented in the design through a series of read/write registers. Register access is accomplished through the LPC transfer cycles defined in Table 9-6, "LPC Cycle Types Supported".

The Logical Devices implemented in the design are identified in Table 9-10, "I/O Base Address Register Default Values". The Base Address Registers allow any logical device's runtime registers to be relocated in LPC I/O space. All chip configuration registers for the device are accessed indirectly through the LPC I/O Configuration Port (see Section 9.8.6, "Configuration Port").

LPC memory cycles may also be used to access the Base Address Registers of certain devices.

9.2 References

- Intel® Low Pin Count (LPC) Interface Specification, v1.1
- PCI Local Bus Specification, Rev. 2.2
- Serial IRQ Specification for PCI Systems Version 6.0.
- PCI Mobile Design Guide Rev 1.0

9.3 Terminology

This table defines specialized terms localized to this feature.

TABLE 9-1: TERMINOLOGY

Term	Definition
System Host	Refers to the external CPU that communicates with this device via the LPC Interface.
Logical Devices	Logical Devices are LPC accessible features that are allocated a Base Address and range in LPC I/O address space
Runtime Register	Runtime Registers are register that are directly I/O accessible by the System Host via the LPC interface. These registers are defined in Section 9.10, "Runtime Registers".
Configuration Registers	Registers that are only accessible in CONFIG_MODE. These registers are defined in Section 9.9, "Configuration Registers".
EC_Only Registers	Registers that are not accessible by the System Host. They are only accessible by an internal embedded controller. These registers are defined in Section 9.11, "EC Registers".

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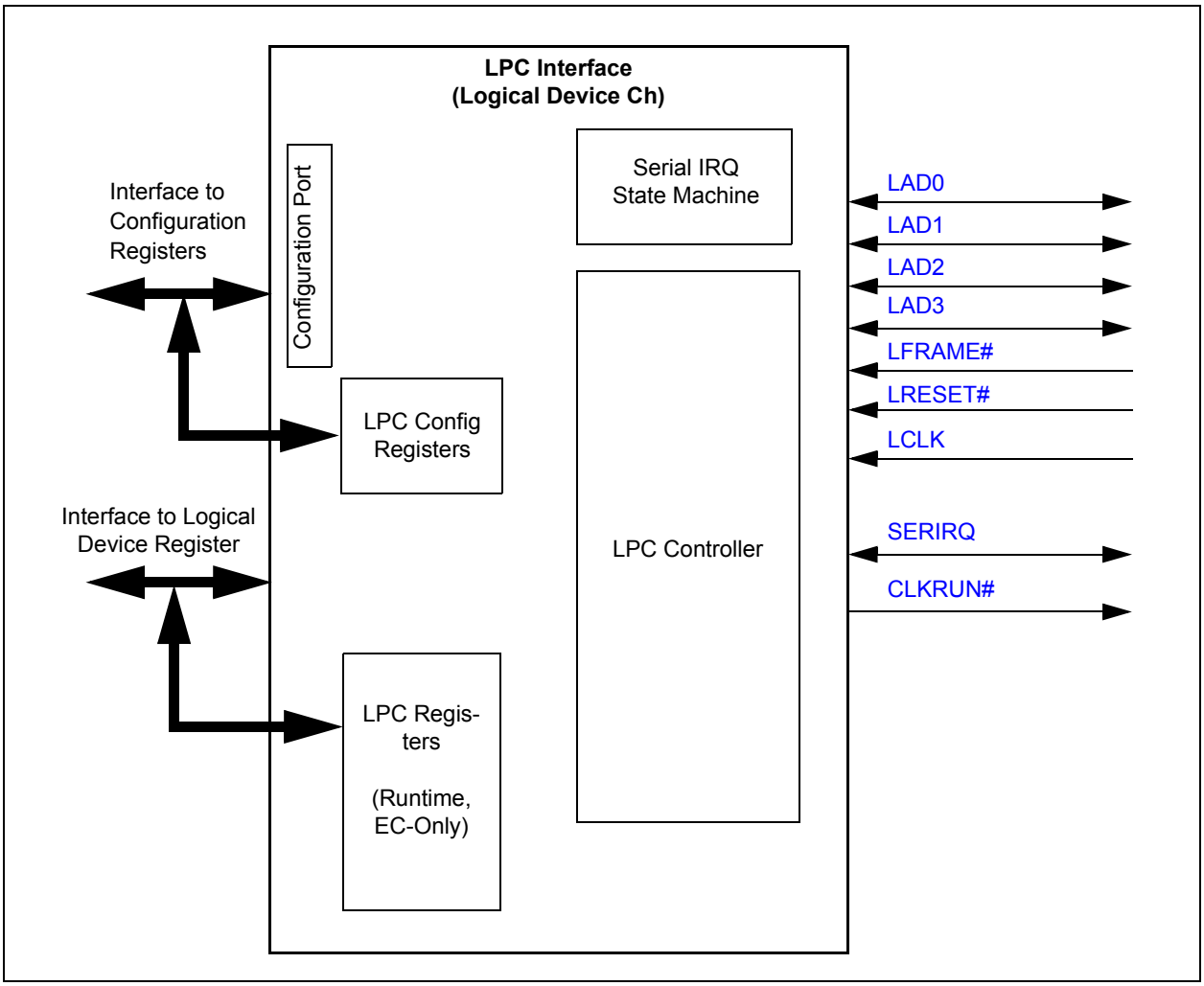
9.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 9-1: BLOCK DIAGRAM OF LPC INTERFACE CONTROLLER WITH CLKRUN# SUPPORT



9.4.1 SIGNAL DESCRIPTION

TABLE 9-2: SIGNAL DESCRIPTION

Name	Direction	Description
LAD0	Input/Output	Bit[0] of the LPC multiplexed command, address, and data bus.
LAD1	Input/Output	Bit[1] of the LPC multiplexed command, address, and data bus.
LAD2	Input/Output	Bit[2] of the LPC multiplexed command, address, and data bus.
LAD3	Input/Output	Bit[3] of the LPC multiplexed command, address, and data bus.

TABLE 9-2: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
LFRAME#	Input	Active low signal indicates start of new cycle and termination of broken cycle.
LRESET#	Input	Active low signal used as LPC Interface Reset. Same as PCI Reset on host. This signal can be monitored using the LPC Bus Monitor Register. **Note:** LRESET# is typically connected to the host PCI RESET (PCIRST#) signal.
LCLK	Input	PCI clock input (PCI_CLK)
SERIRQ	Input/Output	Serial IRQ pin used with the LCLK signal to transfer interrupts to the host.
CLKRUN#	Open-Drain Output	Clock Control for LCLK
LPCPD#	Input	Power Down: Indicates that the device should prepare for power to be removed from the LPC I/F.

9.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

9.5.1 POWER DOMAINS

TABLE 9-3: POWER SOURCES

Name	Description
VTR_PLL	Registers and control logic for this block are powered by this rail.

9.5.2 CLOCK INPUTS

TABLE 9-4: CLOCK INPUTS

Name	Description
48MHz	Control logic for the internal logic in this block is clocked by the main clock domain.
LCLK	Host-facing logic for the LPC Interface is clocked on the LPC clock

9.5.3 RESETS

Name	Description
RESET_SYS	Reset signal used to indicate when the main internal power rail is applied. This reset is also asserted on a Watchdog Timer timeout.
RESET_VCC	This signal is used to indicate when the main power rail in the system is reset. It is asserted when: • The internal RESET_SYS reset signal is asserted • The external VCC_PWRGD signal indicates the main system power rail is unpowered
RESET_HOST	This signal is used to indicate when the main power rail in the system is reset. It is asserted when: • The RESET_VCC is asserted • The LPC interface is enabled and the external LRESET# reset signal is asserted

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In system, the LPC Interface is required to be operational in ACPI Sleep States S0 - S2. When the system enters Sleep States S3 - S5 the LPC interface must tristate its outputs. The following table shows the behavior of LPC output and input/output signals under reset conditions.

TABLE 9-5: LPC INTERFACE SIGNALS BEHAVIOR ON RESET

Pins	RESET_SYS	RESET_VCC	LRESET#
LAD[3:0]	Tri-state	Tri-state	Tri-State
SERIRQ	Tri-state	Tri-state	Tri-State
CLKRUN#	Tri-state	Tri-state	Tri-State

9.6 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
LPC_INTERNAL_ERR	The LPC_INTERNAL_ERR event is sourced by bit D0 of the Host Bus Error Register.
LPC_WAKE	This interrupt event is triggered when the Host initiates an LPC transaction targeting the EC. The EC interrupt handler for this event only needs to clear the interrupt SOURCE bit and return; if the transaction results in an action that requires EC processing, that action will trigger its own interrupt.

9.7 Low Power Modes

The LPC Controller may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

The LPC Block has implemented an EC Clock Control Register to determine how the internal clocks are effected by the supported low power modes. See Section 9.11.4, "EC Clock Control Register" for a description of these options.

9.8 Description

This LPC Controller is compliant with the Intel® Low Pin Count (LPC) Interface Specification, v1.1. The LPC Controller claims only LPC transactions targeted for one of its peripherals, either via LPC I/O Cycles or LPC Memory Cycles. LPC transactions may be used to communicate directly with logical devices on the device using Runtime Registers. LPC transactions can also be used to configure the Host logical devices. The mechanism to configure the chip is described in Section 9.8.6, "Configuration Port". Once a logical device is configured, it may use Serial Interrupt Requests to notify the host of an event.

Note:	In order to use the LPC bus, software must individually configure the mux control for every GPIO associated with an LPC bus signal to the LPC function. Pins are **not** automatically configured for LPC operation when the LPC Controller is enabled.

9.8.1 CYCLE TYPES SUPPORTED

The following cycle types are supported by the LPC Interface Controller. All cycles that are not supported are ignored.

TABLE 9-6: LPC CYCLE TYPES SUPPORTED

Cycle Type	Transfer Size
I/O Read	1 byte
I/O Write	1 byte
Memory Read	1 byte
Memory Write	1 byte

9.8.1.1 LPC I/O Cycles

The system host may use LPC I/O cycles to read/write the I/O mapped configuration and runtime registers implemented in this device. See the Intel® Low Pin Count (LPC) Interface Specification, v1.1, Section 5.2 for definition of LPC I/O Cycles.

9.8.1.2 LPC Memory Cycles

The system host may use LPC memory cycles to access memory mapped registers and internal RAMs implemented in this device. See the Intel® Low Pin Count (LPC) Interface Specification, v1.1, Section 5.1 for definition of LPC Memory Cycles.

9.8.1.3 LAD[3:0] Fields

The LAD[3:0] signals support multiple fields for each protocol as defined in section 4.2.1 LAD[3:0] of the Intel® Low Pin Count (LPC) Interface Specification, v1.1. The following sections further qualify the fields supported.

9.8.1.4 SYNCs on LPC

LPC transactions that access registers located on the device will require a minimum of two wait SYNCs on the LPC bus. The number of SYNCs may be larger if the internal bus is in use by the embedded controller, of if the data referenced by the host is not present in a register. The device always uses Long Wait SYNCs, rather than Short Wait SYNCs, when responding to an LPC bus request.

Note:	All LPC transactions are synchronized to the LCLK and will complete with a maximum of 8 wait states, unless otherwise noted.

The device does not issue ERROR SYNC cycles.

9.8.2 LPC POWER DOWN

The MEC170x tolerates the LPCPD# signal going active and then inactive again without LRESET# going active. This is a requirement for notebook power management functions.

The Intel® Low Pin Count (LPC) Interface Specification, v1.1, Section 8.2 states that “After LPCPD# goes back inactive, the LPC interface will always be reset using LRESET#”. This text must be qualified for mobile systems where it is possible that when exiting a “light” sleep state (ACPI S1, APM POS), LPCPD# may be asserted but the LPC Bus power may not be removed, in which case LRESET# will not occur. When exiting a “deeper” sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRESET# will occur.

The LPCPD# pin is implemented as a “local” powergood for the LPC bus. It is not to be used as a global powergood for the chip. It is used to minimize the LPC power dissipation.

Prior to going to a low-power state, the system asserts the LPCPD# signal. LPCPD# goes active at least 30 microseconds prior to the LCLK signal stopping low and power being shut to the other LPC interface signals. Upon recognizing LPCPD# active, there are no further transactions on the LPC interface.

9.8.3 LPC CLOCK RUN

The CLKRUN# pin is an open drain output and input. The CLKRUN# function is described in the PCI Mobile Design Guide Rev 1.0. CLKRUN# is used to indicate the status of the LPC bus clock LCLK, as well as to request that LCLK be started if it is stopped. The following figure shows a typical system implementation incorporating CLKRUN#.

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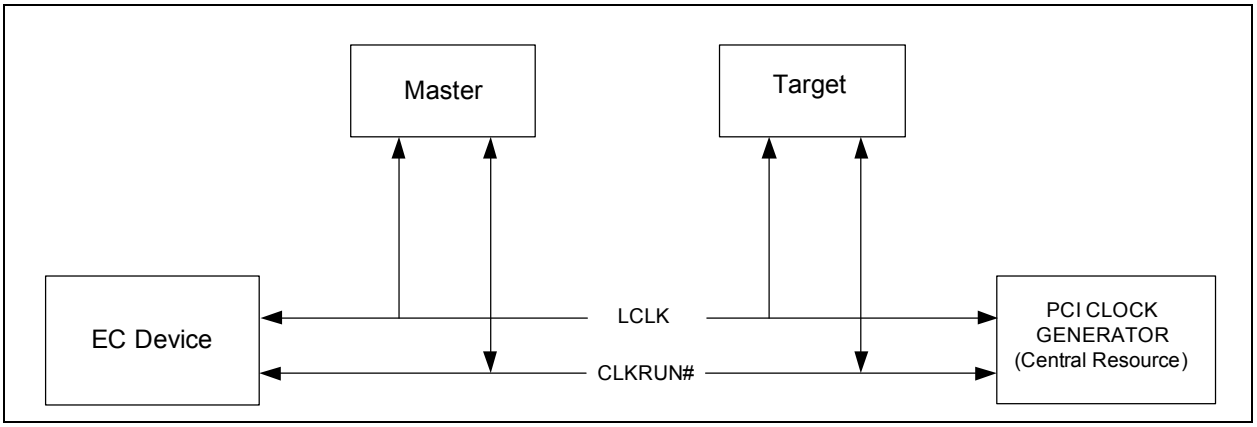
FIGURE 9-2: CLKRUN# SYSTEM IMPLEMENTATION EXAMPLE



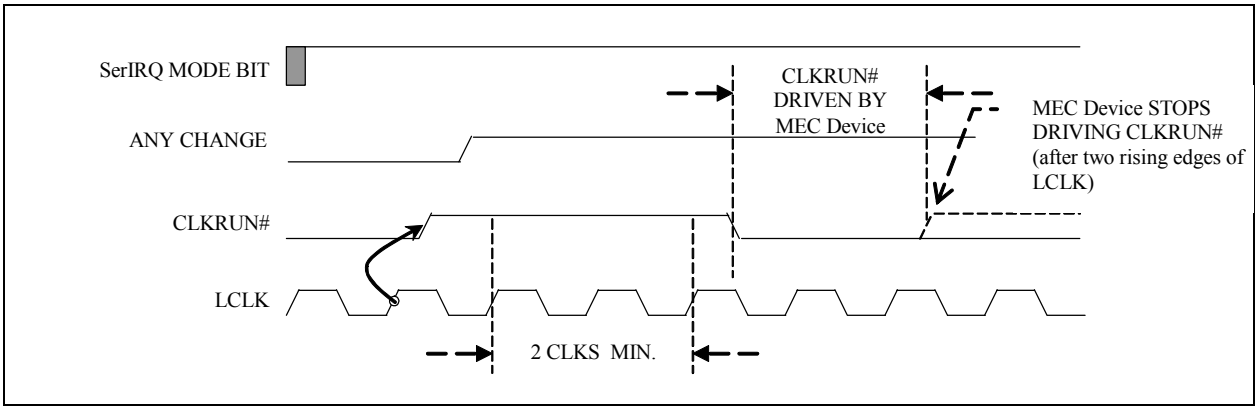
If CLKRUN# is sampled “high”, LCLK is stopped or stopping. If CLKRUN# is sampled “low”, LCLK is starting or started (running).

If the MEC170x needs to send a Serial Interrupt Request to the Host while the LPC bus clock it stopped, it can assert CLKRUN# in order to start the idle LCLK. The MEC170x will only assert CLKRUN# under the following conditions:

- Serial IRQ support is enabled. This occurs when the SerIRQ Mode bit in the DEVICE Global Configuration Register is set to ‘1’.
- The assertion level changes on at least one SERIRQ Host interrupt signal from any enabled Host Logical Device in the MEC170x.
- The CLKRUN# pin is high (i.e., the LPC clock is stopped or will stop soon).

The LPC Controller does not assert CLKRUN# until the CLKRUN# has been de-asserted for a minimum of two successive clocks. The Controller holds CLKRUN# low until it detects two rising edges of the clock. After the second clock edge, the controller disables the open drain driver for the CLKRUN# pin. The following figure illustrates the mechanism for asserting CLKRUN#. In the figure, “ANY CHANGE” means that there is either a high-to-low or a low-to-high edge on any of the SERIRQ interrupt signals from any of the internal Host Logical Devices:

FIGURE 9-3: CLOCK START ILLUSTRATION



9.8.4 CLAIMING I/O TRANSACTIONS

The system host will generate I/O commands to communicate with I/O peripherals, such as Keyboard Controller, UART, etc. The LPC Controller will claim only I/O transactions targeted to it and it will ignore all others. The following sections describe how I/O transactions are claimed and forwarded to access the Runtime and Configuration registers.

The LPC Controller will claim an I/O transaction that is targeted for one of its peripherals (also referred to as logical devices). A Base Address Register has been implemented for each logical device. See Section 9.9.3, "I/O Base Address Registers". If one of the addresses programmed in the Logical Device Base Address Registers matches an LPC I/O address using the following relationship, the LPC Controller will claim the LPC bus cycle:

(LPC Address & ~BAR.MASK) == (BAR.LPC_Address & ~BAR.MASK) && (BAR.Valid == 1)

Note:	The LPC Controller's Base Address register is used to define the Base I/O Address of the Configuration Port.

To access the Runtime registers with I/O cycles, the Host must configure the I/O Base Address Registers, which are accessible via the Configuration Port. The Configuration Port, Logical Device Ch, is located at the Base I/O Address programmed in the BAR Configuration register located at offset 60h.

If the I/O transaction matches the BAR of Logical Device Ch, the transaction will be forwarded to the Configuration Port, otherwise the transaction will be forwarded to the Runtime Registers of the targeted logical device.

Each Logical Device may have up to 256 Contiguous Runtime Registers. The Runtime Registers are located at a defined offset from the Logical Device's base address. The host can directly access these registers with a standard LPC I/O command.
The Logical Device number for the matching device is located in the Frame field of the BAR.
When matching LPC I/O addresses, the LPC Controller ignores address bits that correspond to '1b' bits in the MASK field.

LPC I/O address matching is illustrated in the following two examples:

Example 1:

The Keyboard Controller (8042 Interface) Base Address Register has 60h in the LPC Address field, the Frame field is 01h, and the MASK field is 04h. Because of the single '1b' bit in MASK, the BAR will match LPC I/O patterns in the form '0000_0000_0110_0x00b', so both 60h and 64h will be matched and claimed by the LPC Controller.

Example 2:

If a standard 16550 UART was located at LPC I/O address 238h, then the UART Receive buffer would appear at address 238h and the Line Status register at 23Dh. If the BAR for the UART was set to 0238_7047h, then the UART will be matched at I/O address 238h and the example registers will be claimed by the LPC Controller.

9.8.5 CLAIMING MEMORY TRANSACTIONS

LPC Memory cycles are single byte read or writes that occur in a 32-bit address range. The LPC block will claim a memory transaction that is targeted for a Logical Device in the MEC170x. Table 9-13, "Memory Base Address Register Default Values" lists the Logical Devices that can be accessed by the Host using LPC Memory cycles.

On every LPC bus Memory access all of the Memory Base Address Registers are checked in parallel and if any matches the LPC memory address the LPC Interface claims the bus cycle. The memory address is claimed as described in Section 9.8.4, "Claiming I/O Transactions" except that the LPC memory cycle address is 32 bits instead of the 16 bit I/O cycle address.

Software should insure that no two BARs map the same LPC memory address. If two BARs do map to the same address, the BAR_CONFLICT bit in the Host Bus Error Register is set when an LPC access targeting the BAR Conflict address. An EC interrupt can be generated.

Each Memory BAR is 48 bits wide. The format of each Device Memory BAR is summarized in Memory Base Address Register Format. An LPC memory request is translated by the Device Memory BAR into an 8-bit read or write transaction on the internal bus.

To access the Runtime registers with Memory cycles, the Host must configure the Memory Base Address Registers, which are accessible via the Configuration Port. The Configuration Port, Logical Device Ch, is located at the Base I/O Address programmed in the I/O BAR Configuration register located at offset 60h.

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9.8.5.1 SRAM Memory Transactions

In addition to mapping LPC Memory transactions into Logical Devices, Memory transactions can be mapped into internal address space, as configured by the SRAM Memory BARs. LPC Memory cycles are single byte read or writes that occur in a 32-bit address range. The LPC block will claim LPC memory cycles that match the programmed Host SRAM Base Address Registers address if the VALID in the SRAM BAR is set to 1. No memory cycles will be claimed if this bit is cleared.

The LPC interface can claim two blocks of memory addresses, each up to a 4 KB, and map them to the internal address space. The location of the block of memory in the 32-bit internal space, as well as access to it, is controlled by the EC, using the EC-OnlySRAM Base Address Registers.

The block of memory in the internal 32-bit address space must start on any size-byte address boundary. For example, if the memory is 4k bytes than it is only relocatable on 4k byte boundaries.

CLAIMING LPC MEMORY TRANSACTIONS

A Base Address Register will match an LPC Memory address, and thus the device will claim the LPC bus cycle, if the following relation holds:

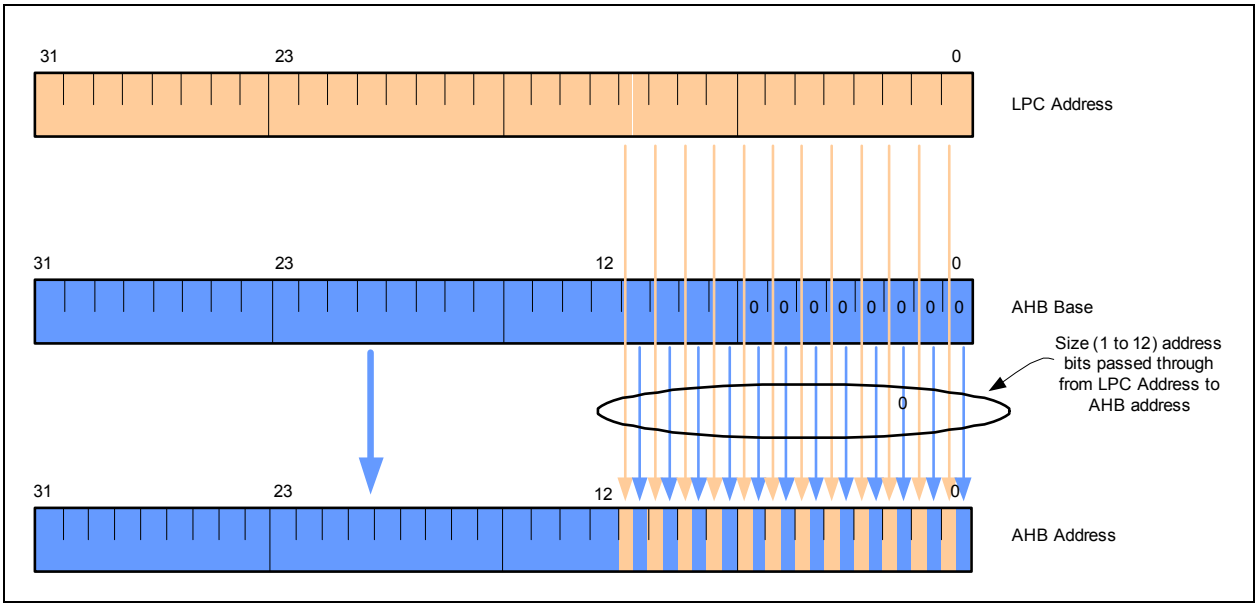
(LPC Address & ~(BAR.2^{SIZE}-1) == (BAR.Host_Address & ~(BAR.2^{SIZE}-1)) && (BAR.Valid == 1)

If the BAR matches, the LPC cycle will be claimed by the device. The LPC request will be translated to an AHB address according to the following formula:

AHB Address = (BAR.AHB_Base & ~(BAR.2^{SIZE}-1)) | (LPC_Address & (BAR.2^{SIZE}-1))

The mapping is also illustrated in Figure 9-4.

FIGURE 9-4: AHB ADDRESS BIT MAPPING



FORWARDING SRAM MEMORY TRANSACTIONS

For each SRAM BAR, the LPC interface can claim up to a 4 KB block of memory addresses and map them to the internal address space.

The firmware programs the base address of the internal memory space in the EC-Only SRAM Base Address Registers, which is mapped to the LPC memory address programmed by the host in the Host SRAM Base Address Registers. The firmware also programs the size of the memory to be accessed. The LPC block uses the size field to determine which memory addresses to claim (see Section , "Claiming LPC Memory Transactions"), as well as to prevent reading/writing an unmapped internal memory location.

9.8.6 CONFIGURATION PORT

The LPC Host can access the Chip's Configuration Registers through the Configuration Port when CONFIG MODE is enabled. The device defaults to CONFIG MODE being disabled.

Note:	The data read from the Configuration Port Data register is undefined when CONFIG MODE is not enabled.

The Configuration Port is composed of an INDEX and DATA Register. The INDEX register is used as an address pointer to an 8-bit configuration register and the DATA register is used to read or write the data value from the indexed configuration register. Once CONFIG MODE is enabled, reading the Configuration Port Data register will return the data value that is in the indexed Configuration Register.

If no value was written to the INDEX register, reading the Data Register in the Configuration Port will return the value in Configuration Address location 00h (default).

The Configuration Port registers are defined in Section 9.10, "Runtime Registers".

9.8.6.1 Enable CONFIG MODE

The INDEX and DATA registers are effective only when the chip is in CONFIG MODE. CONFIG MODE is enabled when the Config Entry Key is successfully written to the I/O address of the INDEX register of the CONFIG PORT while the CONFIG MODE is disabled (see Section 9.8.6.2, "Disable CONFIG MODE").

Config Entry Key = < 55h>

9.8.6.2 Disable CONFIG MODE

CONFIG MODE defaults to disabled on a RESET_SYS, RESET_VCC, and when LRESET# is asserted. CONFIG MODE is also disabled when the following Config Exit Key is successfully written to the I/O address of the INDEX PORT of the CONFIG PORT while CONFIG MODE is enabled.

Config Exit Key = < AAh>

9.8.6.3 Configuration Sequence Example

To program the configuration registers, the following sequence must be followed:

1. Enable Configuration State
2. Program the Configuration Registers
3. Disable Configuration State.

The following is an example of a configuration program in Intel 8086 assembly language.

```
;----------------------------.
; ENABLE CONFIGURATION STATE
;----------------------------'
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AX,055H; Config Entry Key
OUT     DX,AL
;----------------------------.
; CONFIGURE BASE ADDRESS,    |
; LOGICAL DEVICE 8           |
;----------------------------'
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AL,07H
OUT     DX,AL; Point to LD# Config Reg
MOV     DX,CONFIG_PORT_BASE_ADDRESS+1
MOV     AL, 08H
OUT DX,AL; Point to Logical Device 8
;
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AL,60H
OUT     DX,AL   ; Point to BASE ADDRESS REGISTER
MOV     DX,CONFIG_PORT_BASE_ADDRESS+1
MOV     AL,02H
OUT     DX,AL   ; Update BASE ADDRESS REGISTER
;----------------------------.
```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```
; DISABLE CONFIGURATION STATE
;----------------------------'
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AX,0AAH; Config Exit Key
OUT     DX,AL.
```

9.8.7 SERIAL INTERRUPT REQUESTS

The device supports the Serial Interrupt Request (SERIRQ or SIRQ) scheme, which is adopted by several companies, to transmit interrupt information to the system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems Version 6.0.

Each Serial IRQ channel defaults to disabled. To enable a Serial IRQ channel the host must program the Serial IRQ Configuration Registers.

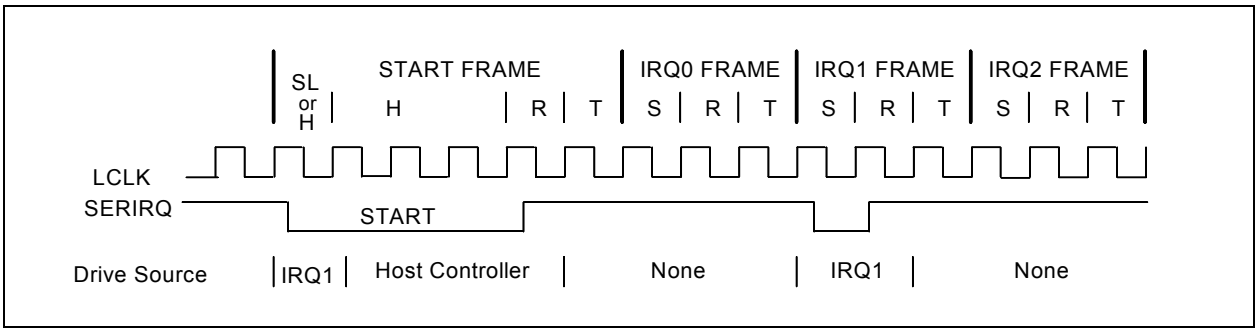
9.8.7.1 TIMING DIAGRAMS for SERIRQ CYCLE

LCLK = LCLK pin

SERIRQ = Serial IRQ pin

Start Frame timing with source sampled a low pulse on IRQ1.

FIGURE 9-5: SERIAL INTERRUPTS WAVEFORM “START FRAME”

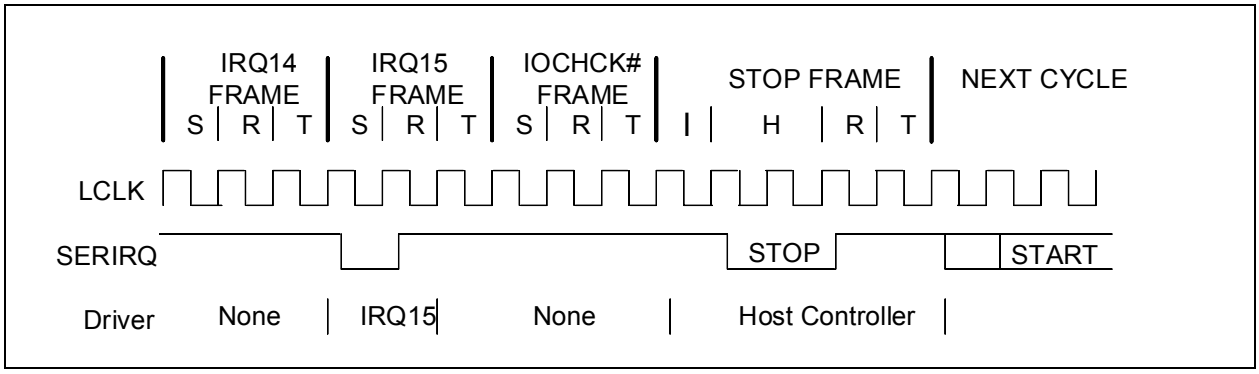


H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 SERIRQ sampling period.

FIGURE 9-6: SERIAL INTERRUPT WAVEFORM "STOP FRAME"



H=Host Control R=Recovery T=Turn-around S=Sample I= Idle

Stop pulse is two clocks wide for Quiet mode, three clocks wide for Continuous mode.

There may be none, one, or more Idle states during the Stop Frame.

The next SERIRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

9.8.7.2 SERIRQ Cycle Control

SERIRQ START FRAME

There are two modes of operation for the SERIRQ Start Frame.

Quiet (Active) Mode

Any device may initiate a Start Frame by driving the SERIRQ low for one clock, while the SERIRQ is Idle. After driving low for one clock, the SERIRQ must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the SERIRQ is active. The SERIRQ is Idle between Stop and Start Frames. The SERIRQ is active between Start and Stop Frames. This mode of operation allows the SERIRQ to be Idle when there are no IRQ/Data transitions, which is typically the most common case.

Once a Start Frame has been initiated, the host controller will take over driving the SERIRQ low in the next clock and will continue driving the SERIRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the host controller will drive the SERIRQ back high for one clock then tri-state.

Any SERIRQ Device which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the host controller unless the SERIRQ is already in an SERIRQ Cycle and the IRQ/Data transition can be delivered in that SERIRQ Cycle.

Continuous (Idle) Mode

Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SERIRQ agents become passive and may not initiate a Start Frame. SERIRQ will be driven low for four to eight clocks by host controller. This mode has two functions. It can be used to stop or idle the SERIRQ or the host controller can operate SERIRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SERIRQ mode transition can only occur during the Stop Frame. Upon reset, SERIRQ bus is defaulted to continuous mode, therefore only the host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SERIRQ Cycle's mode.

SERIRQ DATA FRAME

Once a Start Frame has been initiated, the LPC Controller will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the sample phase, the LPC Controller must drive the SERIRQ (SIRQ pin) low, if and only if, its

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last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SERIRQ must be left tri-stated. During the recovery phase, the LPC Controller must drive the SERIRQ high, if and only if, it had driven the SERIRQ low during the previous sample phase. During the turn-around phase, the controller must tri-state the SERIRQ. The device drives the SERIRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the start frame.

The Sample phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, then the sample phase is {(6 x 3) - 1 = 17} the seventeenth clock after the rising edge of the Start Pulse.

TABLE 9-7: SERIRQ SAMPLING PERIODS

SERIRQ Period	Signal Sampled	# of Clocks Past Start
1	Not Used	2
2	IRQ1	5
3	IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SIRQ data frame will now support IRQ2 from a logical device; previously SERIRQ Period 3 was reserved for use by the System Management Interrupt (LSMI#). When using Period 3 for IRQ2, the user should mask off the SMI via the ESMI Mask Register. Likewise, when using Period 3 for LSMI#, the user should not configure any logical devices as using IRQ2.

SERIRQ Period 14 is used to transfer IRQ13. Each Logical devices will have IRQ13 as a choice for their primary interrupt.

STOP CYCLE CONTROL

Once all IRQ/Data Frames have completed, the host controller will terminate SERIRQ activity by initiating a Stop Frame. Only the host controller can initiate the Stop Frame. A Stop Frame is indicated when the SERIRQ is low for two or three clocks. If the Stop Frame's low time is two clocks, then the next SERIRQ cycle's sampled mode is the Quiet mode; and any SERIRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks, then the next SERIRQ cycle's sampled mode is the continuous mode, and only the host controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

9.8.7.3 Latency

Latency for IRQ/Data updates over the SERIRQ bus in bridge-less systems with the minimum IRQ/Data Frames of 17 will range up to 96 clocks (3.84μS with a 25 MHz LCLK or 2.88μs with a 33 MHz LCLK).

Note:	If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

9.8.7.4 EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SERIRQ Cycle latency in order to ensure that these events do not occur out of order.

9.8.7.5 AC/DC Specification Issue

All Serial IRQ agents must drive/sample SERIRQ synchronously related to the rising edge of LCLK. The SERIRQ pin uses the electrical specification of the PCI bus. Electrical parameters will follow the PCI Local Bus Specification, Rev. 2.2 definition of “sustained tri-state.”

9.8.7.6 Reset and Initialization

The SERIRQ bus uses LRESET# as its reset signal and follows the PCI bus reset mechanism. The SERIRQ pin is tri-stated by all agents while LRESET# is active. With reset, SERIRQ slaves and bridges are put into the (continuous) Idle mode. The host controller is responsible for starting the initial SERIRQ cycle to collect system’s IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SERIRQ cycles. It is the host controller’s responsibility to provide the default values to the 8259’s and other system logic before the first SERIRQ cycle is performed. For SERIRQ system suspend, insertion, or removal application, the host controller should be programmed into Continuous (IDLE) mode first. This is to ensure the SERIRQ bus is in Idle state before the system configuration changes.

9.8.7.7 SERIRQ Interrupts

The LPC Controller routes Logical Device interrupts onto SIRQ stream frames IRQ[0:15]. Routing is controlled by the SIRQ Interrupt Configuration Registers. There is one SIRQ Interrupt Configuration Register for each accessible SIRQ Frame (IRQ); all 16 registers are listed in Table 9-9, "Configuration Register Summary".

The format for each SIRQ Interrupt Configuration Register is described in Section 9.9.2.1, "SIRQ Configuration Register Format". Each Logical Device can have up to two LPC SERIRQ interrupts. When the device is polled by the host, each SIRQ frame routes the level of the Logical Device interrupt (selected by the corresponding SIRQ Interrupt Configuration Register) to the SIRQ stream.

Each SIRQ Interrupt Configuration Register controls a series of multiplexers which route to a single Logical Device interrupt as illustrated in Figure 9-7, "SIRQ Routing Internal Logical Devices". The following table defines the Serial IRQ routing for each logical device implemented in the chip.

TABLE 9-8: LOGICAL DEVICE SIRQ ROUTING

SIRQ Interrupt Configuration Register		Logical Device Interrupt Source	
Select	**Frame**	**Logical Device (Block Instance)**	**Interrupt Source**
0h	0h	Mailbox	MBX_Host_SIRQ
1h	0h	Mailbox	MBX_Host_SMI
0h	1h	Keyboard Controller (8042)	KIRQ
1h	1h	Keyboard Controller (8042)	MIRQ
0h	2h	ACPI-EC 0	EC_OBE
0h	3h	ACPI-EC 1	EC_OBE
0h	4h	ACPI-EC 2	EC_OBE
0h	5h	ACPI-EC 3	EC_OBE
0h	6h	ACPI-EC 4	EC_OBE
0h	9h	UART 0	UART
0h	Ah	UART 1	UART
0h	Ch	LPC Interface 0	EC_IRQ
0h	10h	EM Interface 0	EC-to-Host

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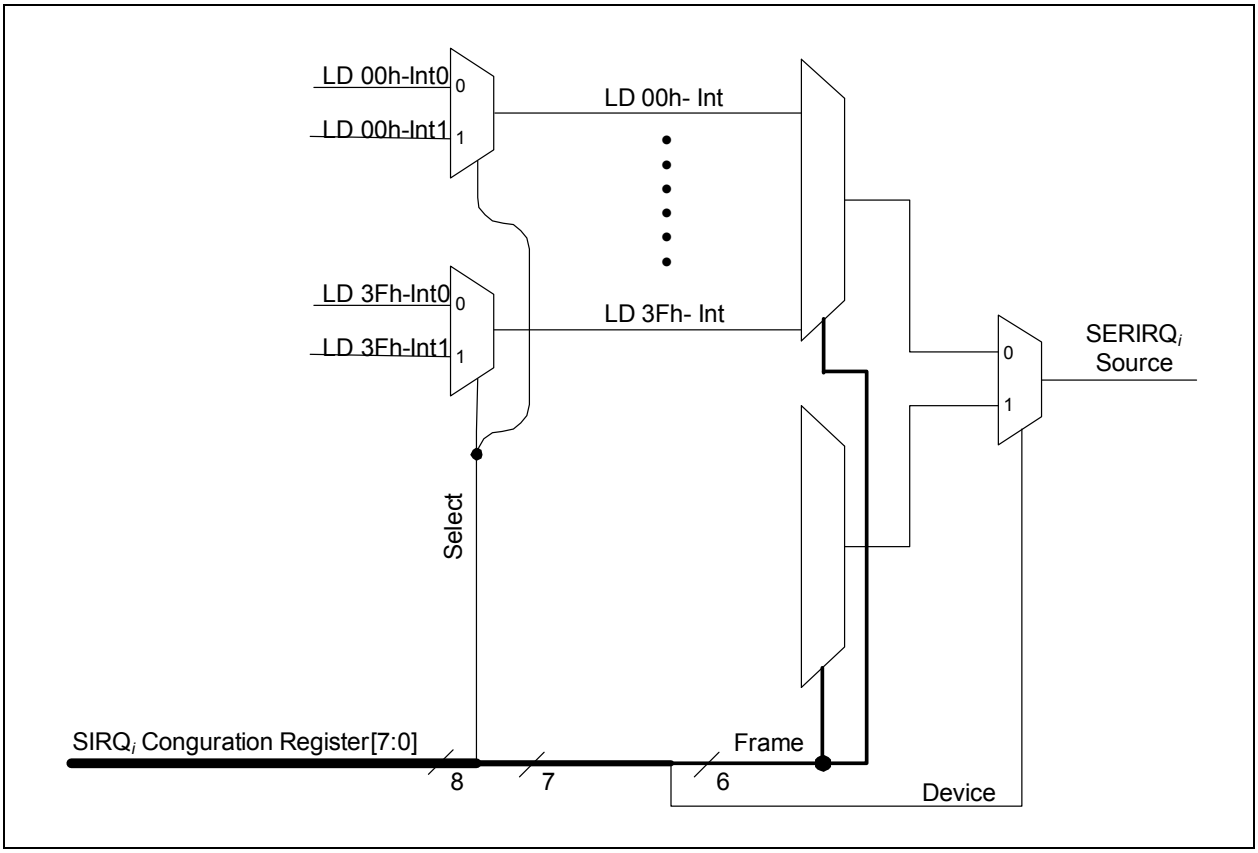
TABLE 9-8: LOGICAL DEVICE SIRQ ROUTING (CONTINUED)

SIRQ Interrupt Configuration Register		Logical Device Interrupt Source	
Select	**Frame**	**Logical Device (Block Instance)**	**Interrupt Source**
1h	10h	EM Interface 0	Host Event
0h	11h	EM Interface 1	EC-to-Host
1h	11h	EM Interface 1	Host Event
0h	12h	EM Interface 2	EC-to-Host
1h	12h	EM Interface 2	Host Event
0h	14h	RTC	RTC

FIGURE 9-7: SIRQ ROUTING INTERNAL LOGICAL DEVICES



Note: Two Logical Devices cannot share a Serial IRQ.

9.9 Configuration Registers

Configuration Registers for the LPC Interface are listed in Table 9-9, "Configuration Register Summary". Host access to Configuration Registers is through the Configuration Port using the Logical Device Number of the LPC Interface and the Index shown in the “Host Index” column of the table. The EC can access Configuration Registers directly. The EC address for each register is formed by adding the Base Address for the LPC Interface shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the “EC Offset” column.

TABLE 9-9: CONFIGURATION REGISTER SUMMARY

EC Offset	Host Index	Register Name
330h	30h	LPC Activate Register
340h	40h	Serial IRQ Configuration Registers -- IRQ0
341h	41h	Serial IRQ Configuration Registers -- IRQ1
342h	42h	Serial IRQ Configuration Registers -- IRQ2
343h	43h	Serial IRQ Configuration Registers -- IRQ3
344h	44h	Serial IRQ Configuration Registers -- IRQ4
345h	45h	Serial IRQ Configuration Registers -- IRQ5
346h	46h	Serial IRQ Configuration Registers -- IRQ6
347h	47h	Serial IRQ Configuration Registers -- IRQ7
348h	48h	Serial IRQ Configuration Registers -- IRQ8
349h	49h	Serial IRQ Configuration Registers -- IRQ9
34Ah	4Ah	Serial IRQ Configuration Registers -- IRQ10
34Bh	4Bh	Serial IRQ Configuration Registers -- IRQ11
34Ch	4Ch	Serial IRQ Configuration Registers -- IRQ12
34Dh	4Dh	Serial IRQ Configuration Registers -- IRQ13
34Eh	4Eh	Serial IRQ Configuration Registers -- IRQ14
34Fh	4Fh	Serial IRQ Configuration Registers -- IRQ15
360h - 3AF	60h -AFh	See Table 9-10, "I/O Base Address Register Default Values"
3B0h - 3BFh	B0h - BFh	See Table 9-11, "SRAM Base Address Register Default Values, LPC Config"
3C0h - 3FFh	C0h - FFh	See Table 9-13, "Memory Base Address Register Default Values"

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9.9.1 LPC ACTIVATE REGISTER

The LPC Activate Register controls the LPC device itself. The Host can shut down the LPC Logical Device by clearing the Activate bit, but it cannot restart the LPC interface, since once the LPC interface is inactive the Host has no access to any registers on the device. The Embedded Controller can set or clear the Activate bit at any time.

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	ACTIVATE When this bit is 0, the logical device is powered down and inactive. Except for the LPC Activate Register itself, clocks to the block are gated and the LPC Logical Device will permit the ring oscillator to be shut down (see Section 9.11.4, "EC Clock Control Register"). LPC bus output pads will be tri-stated. The Host should not write this bit to '0' over the LPC bus. 1=Activated. The LPC Logical Device is powered and functional 0=Deactivated	R/W	0b	RESET_SYS

9.9.2 SERIAL IRQ CONFIGURATION REGISTERS

The LPC Controller implements 16 IRQ channels that may be configured to be asserted by any logical device.

For a list of the SIRQ sources see Table 9-8, "Logical Device SIRQ Routing".

9.9.2.1 SIRQ Configuration Register Format

Offset	See Table 9-9, "Configuration Register Summary".			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	SELECT If this bit is 0, the first interrupt signal from the Logical Device is selected for the SERIRQ vector. If this bit is 1, the second interrupt signal from the Logical Device is selected. The Keyboard Controller is an example of a Logical Devices that requires a second interrupt signal. Most Logical Devices require only a single interrupt and ignore this field as result.	R/W	FFh	RESET_HOST
6	DEVICE This field should always be set to 0 in order to enable a SERIRQ.	R/W	FFh	RESET_HOST
5:0	FRAME These six bits select the Logical Device for on-chip devices as the source for the interrupt. The LPC Logical Device (Logical Device Number 0Ch) can be used by the Embedded Controller to generate a Serial Interrupt Request to the Host under software control.	R/W	FFh	RESET_HOST

Note: A SERIRQ interrupt is deactivated by setting the SERIRQ Configuration Register for the SERIRQ channel to FFh, which is the default reset value.

9.9.3 I/O BASE ADDRESS REGISTERS

The LPC Controller has implemented an I/O Base Address Register (BAR) for each Logical Device in the LPC Configuration space.

- For a description of the I/O Base Address Register format see Section 9.9.3.1, "I/O Base Address Register Format".
- For a description of the I/O BARs per Logical Device see Table 9-10, "I/O Base Address Register Default Values".

On every LPC bus I/O access the unmasked portion of the programmed LPC Host Address in each of the Base Address Registers are checked in parallel and if any matches the LPC I/O address the LPC Controller claims the bus cycle.

Note: Software should that insure that no two I/O BARs map the same LPC I/O address. If two I/O BARs do map to the same address, the LPC_INTERNAL_ERR and BAR_CONFLICT status bits are set when an LPC access is targeting the address with the BAR conflict.

The format of each BAR is summarized in Section 9.9.3.1, "I/O Base Address Register Format".

9.9.3.1 I/O Base Address Register Format

Each LPC accessible logical device has a programmable I/O Base Address Register. The following table defines the generic format used for all of these registers.

Offset	See Table 9-10, "I/O Base Address Register Default Values"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	LPC_HOST_ADDRESS These 16 bits are used to match LPC I/O addresses. See Section 9.8.4, "Claiming I/O Transactions" for a description of how host addresses are claimed.	R/W (See Note 1)	See Table 9-10	Note 2
15	VALID If this bit is 1, the BAR is valid and will participate in LPC matches. If it is 0 this BAR is ignored	R/W	See Table 9-10	Note 2
14	Reserved	R	-	-

Note 1: Bits[31:16] LPC Host Address bit field in the LPC Base Address register at offset 60h must be written LSB then MSB. This particular register has a shadow that lets the Host come in and write to the lower byte of the 16-bit address, and the resulting 16-bit LPC Host address field does not update. Writing to the upper byte triggers a full 16-bit field update

2: The BARs for all Logical Devices except the BAR for the LPC Interface, at offset 60h, are reset on RESET_HOST. The BAR for the LPC Interface is reset on RESET_SYS.

3: The Mask and Frame fields of all logical devices are read-only except for the ACPI EC0 interface. For this interface, the Mask field is readable and writable.

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Offset	See Table 9-10, "I/O Base Address Register Default Values"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
13:8	FRAME These 6 bits are used to specify a logical device frame number within a bus. This field is multiplied by 400h to provide the frame address within the peripheral bus address. Frame values for frames corresponding to logical devices that are not present on the device are invalid.	R	See Table 9-10	Note 2
7:0	MASK These 8 bits are used to mask off address bits in the address match between an LPC I/O address and the Host Address field of the BARs, as described in Section 9.8.4, "Claiming I/O Transactions". A block of up to 256 8-bit registers can be assigned to one base address.	R (See Note 3)	See Table 9-10	Note 2

Note 1: Bits[31:16] LPC Host Address bit field in the LPC Base Address register at offset 60h must be written LSB then MSB. This particular register has a shadow that lets the Host come in and write to the lower byte of the 16-bit address, and the resulting 16-bit LPC Host address field does not update. Writing to the upper byte triggers a full 16-bit field update

2: The BARs for all Logical Devices except the BAR for the LPC Interface, at offset 60h, are reset on RESET_HOST. The BAR for the LPC Interface is reset on RESET_SYS.

3: The Mask and Frame fields of all logical devices are read-only except for the ACPI EC0 interface. For this interface, the Mask field is readable and writable.

The following table defines the IO_BAR of each logical device implemented in the design.

TABLE 9-10: I/O BASE ADDRESS REGISTER DEFAULT VALUES

LPC Index	EC Offset	Logical Device	Reset Default	Default LPC I/O Address	Valid	LDN	Mask
60h	360h	LPC Interface (Configuration Port)	002E_0C01h	002Eh	0h	Ch	1h
64h	364h	Mailbox	0000_0001h	0000h	0h	0h	1h
68h	368h	8042 Emulated Keyboard Controller	0060_0104h	0060h	0h	1h	4h
6Ch	36Ch	ACPI EC Channel 0	0062_0204h	0062h	0h	2h	4h
70h	370h	ACPI EC Channel 1	0000_0307h	0000h	0h	3h	7h
74h	374h	ACPI EC Channel 2	0000_0407h	0000h	0h	4h	7h
78h	378h	ACPI EC Channel 3	0000_0507h	0000h	0h	5h	7h
7Ch	37Ch	ACPI EC Channel 4	0000_0607h	0000h	0h	6h	7h
80h	380h	ACPI PM1	0000_0707h	0000h	0h	7h	7h
84h	384h	Legacy (Fast Keyboard)	0092_0800h	0092h	0h	8h	0h
88h	388h	UART 0	0000_0907h	0000h	0h	9h	7h
8Ch	38Ch	UART 1	0000_0A07h	0000h	0h	Ah	7h
90h	390h	Embedded Memory Interface (EMI) 0	0000_100Fh	0000h	0h	10h	Fh
94h	394h	Embedded Memory Interface (EMI) 1	0000_110Fh	0000h	0h	11h	Fh

TABLE 9-10: I/O BASE ADDRESS REGISTER DEFAULT VALUES (CONTINUED)

LPC Index	EC Offset	Logical Device	Reset Default	Default LPC I/O Address	Valid	LDN	Mask
98h	398h	Embedded Memory Interface (EMI) 2	0000_120Fh	0000h	0h	12h	Fh
9Ch	39Ch	BIOS Debug Port (Port 80) 0	0000_2000h	0000h	0h	20h	0h
A0h	3A0h	BIOS Debug Port (Port 80) 1	0000_2100h	0000h	0h	21h	0h
A4h	3A4h	RTC	0000_141Fh	0000h	0h	14h	1Fh

9.9.4 SRAM BASE ADDRESS REGISTERS

9.9.4.1 SRAM Base Address Register Format, LPC Configuration Register Format

Offset	See Table 9-11, "SRAM Base Address Register Default Values, LPC Config"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
63:32	LPC_HOST_ADDRESS These 32 bits are used to match LPC Memory addresses	R/W	0h	RESET_HOST
31:8	Reserved	R	-	-
7	VALID If this bit is 1, this SRAM Memory BAR is valid and will participate in LPC matches. If it is 0 this BAR is ignored.	R/W	0h	RESET_HOST
6:0	Reserved	R	-	-

9.9.4.2 SRAM Base Address Register Format, EC-Only Register Format

Offset	See Table 9-12, "SRAM Base Address Register Default Values, EC-Only"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	AHB_BASE These 24 bits define the base of a region in AHB address space that will be mapped to the LPC Memory space. Valid AHB addresses are integer multiples of the memory size. For example, if the memory is 4k bytes than the AHB Base address must be located on a 4k byte boundary. The 24 bits in this field are left-shifted by 8 bits to form a 32-bit AHB address, so all memory blocks begin on a 256-byte boundary.	R/W	0h	RESET_SYS
7	INHIBIT Host access to the memory block is inhibited when this bit is 1. The Host can access the memory region mapped by the fields AHB Base and Size when this bit is 0.	R/W	0h	RESET_SYS
6:4	Reserved	R	-	-

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Offset	See Table 9-12, "SRAM Base Address Register Default Values, EC-Only"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3:0	SIZE The number of address bits to pass unchanged when translating an LPC address to an AHB address. These 4 bits in effect define the size of the block to be claimed by the LPC bridge, defined as a power of 2. A value of 0 defines a 2^0 or a 1-byte region starting at LPC Host Address. A value of 12 defines a 2^{12} or a 4K-byte region. Values larger than 12 are undefined.	R/W	0h	RESET_SYS

The following tables define the SRAM BARs implemented in the design.

TABLE 9-11: SRAM BASE ADDRESS REGISTER DEFAULT VALUES, LPC CONFIG

LPC Index	EC Offset	Logical Device	Reset Default	LPC Host Address [63:32]	Valid [7]
B0h	3B0h	SRAM BAR 0	0h	0h	0h
B8h	3B8h	SRAM BAR 1	0h	0h	0h

TABLE 9-12: SRAM BASE ADDRESS REGISTER DEFAULT VALUES, EC-ONLY

EC Offset	Logical Device	Reset Default	AHB Base Address [31:8]	Inhibit [7]	Size [3:0]
1F8h	SRAM BAR 0	80h	0h	1h	0h
1FCh	SRAM BAR 1	80h	0h	1h	0h

9.9.5 MEMORY BASE ADDRESS REGISTERS

Some Logical Devices have a Memory Base Address Register. These Device Memory BARs are located in blocks of Configuration Registers in Logical Device 0Ch. An LPC memory request is translated by the Memory BAR into an 8-bit read or write transaction on the AHB bus. The 32-bit LPC memory address is translated into a 24-bit AHB address.

The following table defines the generic format used for all of these registers.

9.9.5.1 Memory Base Address Register Format

Offset	See Table 9-13, "Memory Base Address Register Default Values"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
47:16	LPC_HOST_ADDRESS These 32 bits are used to match LPC memory addresses	R/W	See Table 9-13	RESET_HOST
15	VALID If this bit is 1, the BAR is valid and will participate in LPC matches. If it is 0 this BAR is ignored	R/W	See Table 9-13	RESET_HOST
14	Reserved	R	-	-
Note 1: The Mask and Frame fields of all logical devices are read-only except for the ACPI EC0 interface. For this interface, the Mask field is readable and writable.				

Offset	See Table 9-13, "Memory Base Address Register Default Values"			
Bits	**Description**	**Type**	**Default**	**Reset Event**
13:8	FRAME These 6 bits are used to specify a logical device frame number within a bus. This field is multiplied by 400h to provide the frame address within the peripheral bus address.Frame values for frames corresponding to logical devices that are not present on the device are invalid.	R	See Table 9-13	RESET_HOST
7:0	MASK These 8 bits are used to mask off address bits in the address match between an LPC I/O address and the Host Address field of the BARs, as described in Section 9.8.1.2, "LPC Memory Cycles". A block of up to 256 8-bit registers can be assigned to one base address.	R or R/W (See Note 1)	See Table 9-13	RESET_HOST
Note 1: The Mask and Frame fields of all logical devices are read-only except for the ACPI EC0 interface. For this interface, the Mask field is readable and writable.				

The following table defines the Memory BAR of each logical device implemented in the design.

TABLE 9-13: MEMORY BASE ADDRESS REGISTER DEFAULT VALUES

LPC Index	EC Offset	Logical Device	Reset Default	Default LPC I/O Address	Valid	Frame	Mask
C0h	3C0h	Mailbox	0000_0001h	0000h	0h	0h	1h
C6h	3C6h	ACPI EC Channel 0	0062_0204h	0062h	0h	2h	4h
CCh	3CCh	ACPI EC Channel 1	0000_0307h	0000h	0h	3h	7h
D2h	3D2h	ACPI EC Channel 2	0000_0407h	0000h	0h	4h	7h
D8h	3D8h	ACPI EC Channel 3	0000_0507h	0000h	0h	5h	7h
DEh	3DEh	ACPI EC Channel 4	0000_0607h	0000h	0h	6h	7h
E4h	3E4h	Embedded Memory Interface (EMI) 0	0000_100Fh	0000h	0h	10h	Fh
EAh	3EAh	Embedded Memory Interface (EMI) 1	0000_110Fh	0000h	0h	11	Fh
F0h	3F0h	Embedded Memory Interface (EMI) 2	0000_120Fh	0000h	0h	12h	Fh

9.10 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the LPC Interface. Host access for each register listed in this table is defined as an offset in the Host address space to the LPC Block's Base Address, as defined by the instance's Base Address Register.

Note: The LPC Runtime registers are only accessible from the LPC interface and are used to access the LPC Configuration Port. They are not accessible by the EC.

TABLE 9-14: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	INDEX Register
01h	DATA Register

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For a description of accessing the Configuration Port see Section 9.8.6, "Configuration Port".

9.10.1 INDEX REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	INDEX The INDEX register, which is part of the Configuration Port, is used as a pointer to a Configuration Register Address.	R/W	0h	RESET_SYS

9.10.2 DATA REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DATA The DATA register, which is part of the Configuration Port, is used to read or write data to the register currently being selected by the INDEX Register.	R/W	0h	RESET_SYS

9.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the LPC Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 9-15: REGISTER SUMMARY

Offset	Register Name
104h	LPC Bus Monitor Register
108h	Host Bus Error Register
10Ch	EC SERIRQ Register
110h	EC Clock Control Register
114h	MCHP Test Register
118h	MCHP Test Register
120h	BAR Inhibit Register
124h	TEST
128h	TEST
12Ch	TEST
130h	LPC BAR Init Register
1F8h - 1FCh	See Table 9-12, "SRAM Base Address Register Default Values, EC-Only"

Note: TEST registers are read/write registers. Modifying these registers may have unwanted results.

9.11.1 LPC BUS MONITOR REGISTER

Offset	104h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	LRESET_STATUS This bit reflects the state of the LRESET# input pin. The LRESET_Status is the inverse of the LRESET# pin. When the LRESET_Status bit is '0b', the LRESET# input pin is de-asserted (that is, the pin has the value '1b'). When the LRESET_Status bit is '1b', the LRESET# input pin is asserted (that is, the pin has the value '0b').	R	0h	RESET_SYS
0	TEST	R	0h	RESET_SYS

9.11.2 HOST BUS ERROR REGISTER

Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	ERROR_ADDRESS This 24-bit field captures the 24-bit internal address of every LPC transaction whenever the bit LPC_INTERNAL_ERR in this register is 0. When LPC_INTERNAL_ERR is 1 this register is not updated but retains its previous value. When bus errors occur this field saves the address of the first address that caused an error.	R	0h	RESET_SYS
5	DMA_ERR This bit is set to 1 whenever EN_INTERNAL_ERR is 1 and an LPC DMA access causes an internal bus error. Once set, it remains set until cleared by being written with a 1.	R/WC	0h	RESET_SYS
4	CONFIG_ERR This bit is set to 1 whenever EN_INTERNAL_ERR is 1 and an LPC Configuration access causes an internal bus error. Once set, it remains set until cleared by being written with a 1.	R/WC	0h	RESET_SYS
3	RUNTIME_ERR This bit is set to 1 whenever EN_INTERNAL_ERR is 1 and an LPC I/O access causes an internal bus error. This error will only occur if a BAR is misconfigured. Once set, it remains set until cleared by being written with a 1.	R/WC	0h	RESET_SYS
2	BAR_CONFLICT This bit is set to 1 whenever a BAR conflict occurs on an LPC address. A Bar conflict occurs when more than one BAR matches the address during of an LPC cycle access. Once this bit is set, it remains set until cleared by being written with a 1.	R/WC	0h	RESET_SYS
1	EN_INTERNAL_ERR When this bit is 0, only a BAR conflict, which occurs when two BARs match the same LPC I/O address, will cause LPC_INTERNAL_ERR to be set. When this bit is 1, internal bus errors will also cause LPC_INTERNAL_ERR to be set.	R/W	0h	RESET_SYS

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Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	LPC_INTERNAL_ERR This bit is set whenever a BAR conflict or an internal bus error occurs as a result of an LPC access. Once set, it remains set until cleared by being written with a 1. This signal may be used to generate interrupts.	R/WC	0h	RESET_SYS

9.11.3 EC SERIRQ REGISTER

Offset	10Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	EC_IRQ If the LPC Logical Device is selected as the source for a Serial Interrupt Request by an Interrupt Configuration register (see Section 9.8.7.7, "SERIRQ Interrupts"), this bit is used as the interrupt source.	R/W	0h	RESET_SYS

9.11.4 EC CLOCK CONTROL REGISTER

Offset	110h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	-
2	TEST This bit **must** be set to '1b' whenever this register is written.	R/W	1h	RESET_SYS
1:0	CLOCK_CONTROL This field controls when the host interface will permit the internal ring oscillator to be shut down. The choices are as follows: 3=Sleep modes are inhibited as long as the host interface is active. When the ACTIVATE bit in the LPC Activate Register is 0, the Host Interface will permit the ring oscillator to be shut down and the CLOCK_CONTROL Field is ignored. The CLOCK_CONTROL Field only effects the Host Interface when the ACTIVATE bit in the LPC Activate Register is 1 2=Sleep modes can be entered after the completion of every LPC transaction. This mode may cause an increase in the time to respond to LPC transactions if the main oscillator is off when the LPC transaction is detected. 1=The host interface will permit sleep if the CLKRUN# signals "CLOCK STOP" and there are no pending serial interrupt request or DMA requests from devices associated with the device. The CLKRUN# signals "CLOCK STOP" by CLKRUN# being high for 5 LPCCLK's after the raising edge of CLKRUN# 0=The Host interface will permit sleep if the LPCPD# signal is asserted low	R/W	0h	RESET_SYS

9.11.5 MCHP TEST REGISTER

Offset	114h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	TEST	R	0h	RESET_SYS

9.11.6 MCHP TEST REGISTER

Offset	118h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	TEST	R/W	0h	RESET_SYS
0	TEST	R/W	0h	RESET_SYS

9.11.7 BAR INHIBIT REGISTER

Offset	120h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
63:0	BAR_INHIBIT When bit *Di* of BAR_Inhibit is 1, the BAR for Logical Device *i* is disabled and its addresses will not be claimed on the LPC bus, independent of the value of the Valid bit in the BAR.The association between bits in BAR_Inhibit and Logical Devices is illustrated in Table 9-16, "BAR Inhibit Device Map".	R/W	0h	RESET_SYS

TABLE 9-16: BAR INHIBIT DEVICE MAP

Bar Inhibit Bit	Logical Device Number
0	0h
1	1h
. . .	. . .
31	1Fh
. . .	. . .
63	3Fh

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9.11.8 LPC BAR INIT REGISTER

Offset	130h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:0	BAR_INIT This field is loaded into the LPC BAR at offset 60h on RESET_HOST.	R/W	002Eh	RESET_SYS

10.0 ENHANCED SERIAL PERIPHERAL INTERFACE (ESPI)

10.1 Introduction

The Intel® Enhanced Serial Peripheral Interface (eSPI) is used by the system host to configure the chip and communicate with the logical devices implemented in the design through a series of read/write registers. It is Intel's successor to the Low Pin Count (LPC) bus, used in previous devices to provide System Host access to devices internal to the Embedded Controller.

10.2 References

1. Intel, *Enhanced Serial Peripheral Interface (eSPI): Interface Specification (for Client Platforms)*
2. Intel, *Skylake U and Y Platform Design Guide*, Revision 2.0
3. Microchip "eSPI Controller" Specification, DS00000A

10.3 Terminology

This table defines specialized terms localized to this feature.

TABLE 10-1: TERMINOLOGY

Term	Definition
System Host	Refers to the external CPU that communicates with this device via the eSPi Interface.
Logical Devices	Logical Devices are System Host-accessible features that are allocated a Base Address and range in the System Host I/O address space
Runtime Register	Runtime Registers are registers that are directly I/O accessible by the System Host via the eSPI interface.
Configuration Registers	Registers that are only accessible in CONFIG_MODE.
EC_Only Registers	Registers that are not accessible by the System Host. They are only accessible by an internal embedded controller.

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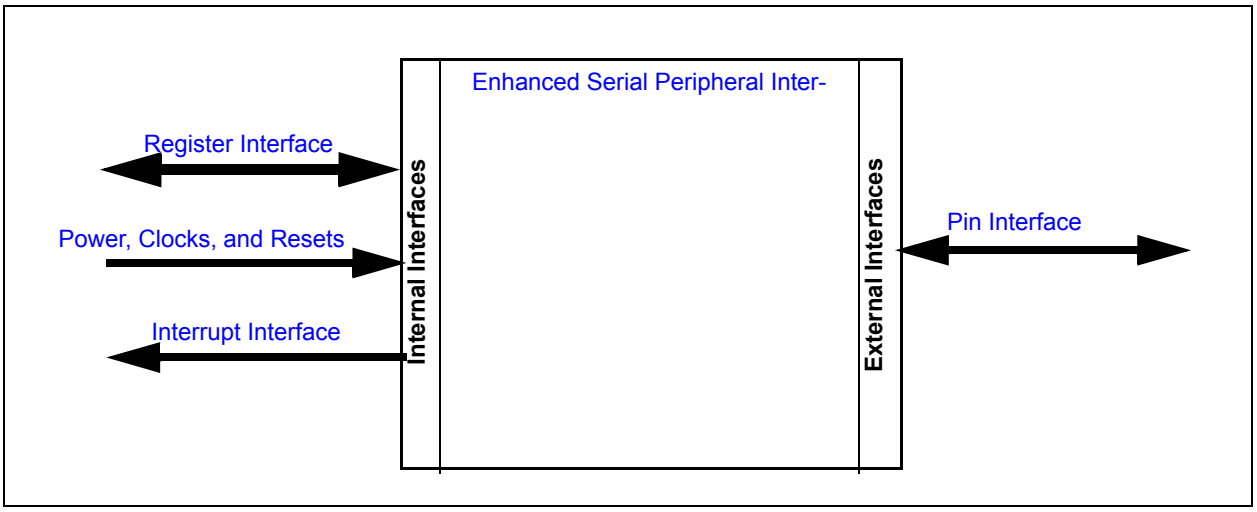
10.4 Interface

FIGURE 10-1: Enhanced Serial Peripheral Interface (eSPI) INTERFACE DIAGRAM



10.4.1 PIN INTERFACE

Table 10-2, "Signal Description Table" lists the signals that are typically routed to the pin interface.

TABLE 10-2: SIGNAL DESCRIPTION TABLE

Signal Name	Direction	Description
eSPI_CS#	Input	eSPI Chip Select, Low-Active
eSPI_CLOCK	Input	eSPI Clock
eSPI_ALERT#	Output	eSPI Alert signal, Low-Active. Exercised only if ALERT# is configured to be presented separately from the IO1 pin.
eSPI_RESET#	Input	POR for eSPI bus power domain, and a Reset for serious errors. Low-Active.
eSPI_IO0	Input/Output	eSPI Data Bus, bit 0. Input (MOSI) in x1 Bus Mode. Else, it holds the LS data bit.
eSPI_IO1	Input/Output	eSPI Data Bus, bit 1. Output (MISO) in x1 Bus Mode. Also, by default, presents ALERT# state between frames.
eSPI_IO2	Input/Output	eSPI Data Bus, bit 2. Used only in x4 mode.
eSPI_IO3	Input/Output	eSPI Data Bus, bit 3. Used only in x4 mode, as MS bit.
GPIO055/ SHD_CS#/ (RSMRST#)	Input/Output	eSPI/Shared SPI selection strap RSMRST# signal to core logic
GPIO227/ SHD_IO2	Input	Primary rail power good input

The signal interface pins are connected to the external pin interface. This table maps the block signal names to the external pinout names.

10.4.2 REGISTER INTERFACE

Each of the four channels contains registers that may be accessed by both the Host and the EC, as well as a set of registers than only be accessed by the EC.

10.4.3 POWER, CLOCKS, AND RESETS

This section defines the Power, Clock, and Reset parameters associated with this IP block.

10.4.3.1 Power

Name	Description
VTR	The Enhanced Serial Peripheral Interface (eSPI) block and registers are powered by VTR. This power rail may be present to the block while external power to the eSPI pins is not present. Therefore, this block remains passive on the eSPI bus pins whenever eSPI_RESET# is low.

10.4.3.2 Clocks

This section describes all the clocks in the block, including those that are derived from the I/O Interface as well as the ones that are derived or generated internally.

Name	Description
48MHz	The main internal clock
eSPI_CLOCK	The eSPI clock provided by the System Host core logic **Note:** Max frequency supported is 50MHz.

10.4.3.3 Resets

This section describes all the resets associated with this IP block, including those that are derived from the I/O Interface as well as the ones that are derived or generated internally.

Name	Description
RESET_SYS	This is the power-on-reset signal, which is asserted when VTR power is applied. Asserting this reset signal resets the eSPI IP block, including all registers, FIFOs, and state machines to their initial POR state.
RESET_eSPI	A general reset signal for the eSPI block. This reset is asserted with the eSPI_RESET# pin is asserted by the System Host core logic. When this reset is asserted all eSPI Output signals and Input/Output signals are tri-stated. Any transaction in progress is terminated and all FIFOs are flushed. All interrupt status flags are reset and all interrupts to the EC except RESET_eSPI are suppressed. When this reset is asserted, all eSPI Configuration Registers in the slave device are set to the default values, as per the Intel eSPI Specification. Fields in the eSPI Configuration Registers that are set from the eSPI Capabilities registers (see Section 10.7, "eSPI Register Summary") are not modified. This reset is also asserted in the following cases: RESET_SYS is asserted
RESET_VCC	Performs a reset when the system main power rail is turned off.
RESET_HOST	Performs a reset when the system main power rail is turned off or when the system host resets the Host Interface.

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Name	Description
eSPI_PLTRST#	This is a reset that affects the Peripheral Channel. It is received by the Slave as a Virtual Wire (PLTRST#). This reset is also asserted in the following cases: • RESET_SYS is asserted • RESET_eSPI is asserted • VCC_PWRGD is de-asserted • The Peripheral Channel is disabled

10.4.4 INTERRUPT INTERFACE

This section defines the interrupt Interface signals routed to the chip interrupt aggregator.

Source	Description
Wake Only Event	
ESPI_WAKE_ONLY	This signal is asserted when the eSPI interface detects eSPI traffic. If enabled, it may be used to wake the main clock domain when the chip is in a sleep state.
Peripheral Channel	
INTR_PC	Peripheral Channel Interrupt
INTR_BM1	Bus Mastering Channel 1 Interrupt
INTR_BM2	Bus Mastering Channel 2 Interrupt
INTR_LTR	Peripheral Message (LTR) Interrupt
OOB Channel	
INTR_OOB_UP	Out of Band Channel Up Interrupt
INTR_OOB_DOWN	Out of Band Channel Down Interrupt
Flash Channel	
INTR_FLASH	Flash Channel Interrupt
Virtual Wires Channel	
MSVW[00:09]_SRC[3:0]	Master-to-Slave Virtual Wire Interrupts
eSPI Global	
eSPI_RESET	eSPI Reset Interrupt This interrupt is generated whenever the external eSPI_RESET# pin changes state.

10.5 Low Power Modes

The eSPI block can enter a low power state when it is not in operation. When the eSPI block is operational it will keep the main system clock from shutting down and entering its sleep state. When the eSPI_CS# pin is asserted the eSPI block will wake the main system clock, if it is in a sleep state, and keep the system clock in its active state until the transaction started by the Master has completed.

The low power behavior of the block is controlled by the BAR Inhibit Register. The block is not affected by a SLEEP_ENABLE signal from the chip's Power, Clocks and Resets unit.

10.6 Description

The Intel® eSPI Interface is used by the system host to configure the chip and communicate with the logical devices implemented in the design through a series of read/write registers.

Note:	In order to use eSPI, software must individually configure the mux control for every GPIO associated with an eSPI bus signal to the eSPI function. Pins are **not** automatically configured for eSPI operation when the eSPI Controller is enabled.

10.6.1 SYSTEM INTERFACE

The EC has the option of loading its code image over the eSPI Flash Channel. In order to do so, the Boot ROM code must:

1. Determine that booting using the eSPI Flash Channel is required
2. Determine that the Primary power rails for the Intel PCH have ramped and are stable
3. Take the PCH out of reset so that the eSPI block in the PCH is operational

The following sections describe each of these three steps.

10.6.1.1 Determining that the Flash Channel is required

In order to select between a SPI Flash directly attached to the Shared SPI Flash port and the eSPI Flash Channel as the source for EC code, the EC examines a strap after a reset. The strap is the pin:

- GPIO055/PWM2/SHD_CS#/(RSMRST#)

This pin is on the VTR2 rail; VTR2 must be ramped and stable before the EC samples its state. If booting from the Shared SPI Flash is required, then this pin must be connected to the SPI Flash power supply through a weak pull-up resistor. If booting from the eSPI Flash Channel is required, then this pin must be connected to ground through a weak pull-down resistor.

If booting over a Shared SPI Flash, the EC switches the pin to the SHD_CS# pin function and proceeds to load over the Shared SPI Flash port. De-asserting RSMRST# is the responsibility of the loaded code and not the Boot ROM code; the RSMRST# function may be assigned to any GPIO which would then be controlled by the EC.

If booting over the eSPI Flash Channel is selected, the GPIO055/PWM2/SHD_CS#/(RSMRST#) pin must be used as the RSMRST# signal to the PCH. The EC will keep the pin as a GPIO; RSMRST# timing and behavior is covered in the next two sections.

10.6.1.2 Determining that the Primary power rails are stable

Intel requires four Primary power rails to be ramped and stable before taking the PCH out of reset:

- VCC_Prim 1.8V
- VCC_Prim 3.3V
- VCCPRIM_CORE
- VCC_Prim 1.0V

According to Intel's requirements[2], all four rails must be ramped and stable for at least 20ms before RSMRST# can be de-asserted. The EC determines that at least one of the four rails has ramped by examining the following pin:

- GPIO227/SHD_IO2

The EC will only examine this pin if loading code over the eSPI Flash Channel is required. This pin is on the VTR2 rail; VTR2 must be ramped and stable before the EC samples its state. If VTR2 is 1.8V, then this pin can be connected to VCC_Prim 1.8V. If VTR2 is 3.3V, then this pin can be connected to VCC_Prim 3.3V. This pin may be connected to any other signal that indicates at least one of the four Primary rails is up, as long as that signal is at the same voltage level as VTR2.

10.6.1.3 Taking the PCH out of reset

Once the EC detects a high on GPIO227/SHD_IO2, it waits a sufficient time to satisfy Intel's requirements for the de-assertion of RSMRST#. After the time has expired, the EC drives the pin high, which has the effect of de-asserting RSMRST#, enables the eSPI interface, and then waits for the Host to begin eSPI operation.

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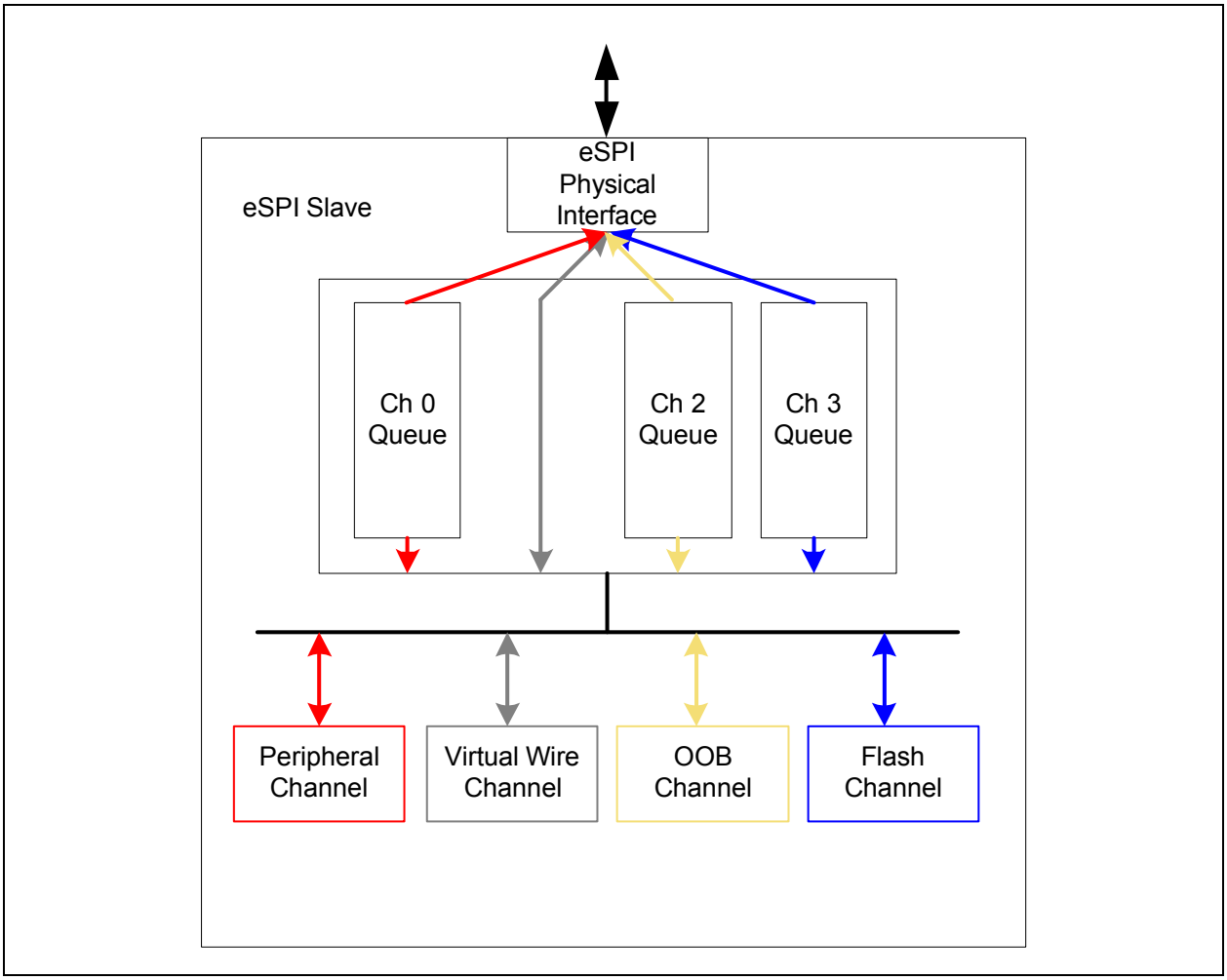
10.6.2 ESPI CHANNELS

The eSPI interface consists of four channels:

- eSPI Peripheral Channel Interface
- eSPI Out Of Band Channel Interface
- eSPI Flash Channel Interface
- eSPI Virtual Wires Interface

These four channels are multiplexed onto the eSPI physical interface that connects the Embedded Controller device with the core logic of the Host. The following figure illustrates this multiplexing:

FIGURE 10-2: ESPI BLOCK DIAGRAM



The Flash Channel permits the EC to access the System SPI Flash through the eSPI interface.

The Out of Band (OOB) Channel enables messaging between the Out-Of-Band Processor in the system chipset and the EC. This messaging is implemented by tunneling SMBus packets over the eSPI port.

The Peripheral Channel (PC) enables the system Host to read and write locations inside the EC. The PC encapsulates legacy I/O operation as well as generic memory read and write operations. Like the Flash and the OOB Channels, all PC accesses are multiplexed over the eSPI port.

The Virtual Wire Channel provides in-band emulation of sideband pin signals between the system Core Logic and the EC, including the legacy SERIRQ interrupt signal to the system Host.

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10.7 eSPI Register Summary

The following sections list the registers associated with the eSPI logic. The eSPI logic required three Logical Devices in order to provide access to all the required registers. These Logical Devices are called the I/O Component, the Memory Component and the Virtual Wire Component. The Base Addresses for these three blocks are shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

The EC may access all registers in all three Logical Devices. Host access is restricted to three ranges: Runtime Registers, located at offsets 00h through FFh from the Logical Device Base Address of the I/O Component, and Configuration Registers, located at offsets 330h through 3FFh in both the I/O Component and the Memory Component. The Runtime Registers may be mapped into the Hosts address space, either I/O or Memory, by setting the associated BAR for the Logical Device. The Configuration Registers are accessed through the Configuration Port. Registers located at offsets 330h through 3FFh are mapped to Configuration Port offsets 30h through FFh. Configuration Port offsets 00h through 2Fh, for all Host Logical Devices, are mapped to the Global Configuration Registers.

10.7.1 ESPI I/O COMPONENT

TABLE 10-3: ESPI I/O COMPONENT REGISTER SUMMARY

Host Offset	EC Offset	Register Name
RUNTIME REGISTERS		
Peripheral Channel		
00h	00h	INDEX Register
01h	01h	DATA Register
EC PRIVATE REGISTERS		
Peripheral Channel		
-	100h	Peripheral Channel Last Cycle Register
-	10Ch	Peripheral Channel Error Address Register
-	114h	Peripheral Channel Status Register
-	118h	Peripheral Channel Interrupt Enable Register
-	11Ch	Reserved
-	120h	BAR Inhibit Register
-	128h	eSPI BAR Init Register
-	12Ch	EC IRQ Register
-	130h	TEST
-	134h - 1A7h	I/O Base Address Register Format, Internal Component See Table 10-6, "ESPI I/O Base Address Register Default Values"
-	220h	LTR Peripheral Status Register
-	224h	LTR Peripheral Enable Register
-	228h	LTR Peripheral Control Register
-	22Ch	LTR Peripheral Message Register
OOB Channel		
-	240h	OOB Channel Receive Address Register
-	248h	OOB Channel Transmit Address Register
-	250h	OOB Channel Receive Length Register
-	254h	OOB Channel Transmit Length Register
-	258h	OOB Channel Receive Control Register
-	25Ch	OOB Channel Receive Interrupt Enable Register
-	260h	OOB Channel Receive Status Register
-	264h	OOB Channel Transmit Control Register
-	268h	OOB Channel Transmit Interrupt Enable Register
-	26Ch	OOB Channel Transmit Status Register

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TABLE 10-3: ESPI I/O COMPONENT REGISTER SUMMARY (CONTINUED)

Host Offset	EC Offset	Register Name
Flash Channel		
-	280h	Flash Access Channel Flash Address Register
-	288h	Flash Access Channel Buffer Address Register
-	290h	Flash Access Channel Transfer Length Register
-	294h	Flash Access Channel Control Register
-	298h	Flash Access Channel Interrupt Enable Register
-	29Ch	Flash Access Channel Configuration Register
-	2A0h	Flash Access Channel Status Register
Virtual Wire Channel		
-	2B0h	Virtual Wire Status
eSPI Global		
-	2E0h	eSPI Capabilities ID Register
-	2E1h	eSPI Capabilities Global Capabilities 0 Register
-	2E2h	eSPI Capabilities Global Capabilities 1 Register
-	2E3h	eSPI Peripheral Channel Capabilities Register
-	2E4h	eSPI Virtual Wire Channel Capabilities Register
-	2E5h	eSPI OOB Channel Capabilities Register
-	2E6h	eSPI Flash Channel Capabilities Register
-	2E7h	eSPI Peripheral Channel Ready Register
-	2E8h	eSPI OOB Channel Ready Register
-	2E9h	eSPI Flash Channel Ready Register
-	2EAh	eSPI Reset Interrupt Status Register
-	2EBh	eSPI Reset Interrupt Enable Register
-	2ECh	PLTRST Source Register
-	2F0h	TEST
-	2F8h	TEST
CONFIGURATION REGISTERS		
Peripheral Channel		
30h	330h	eSPI Activate Register
34h - A7h	334h - 3A7h	I/O Space Base Address Registers (BARs) See Table 10-6, "ESPI I/O Base Address Register Default Values"
Virtual Wire Channel		
ACh - CFh	3ACh - 3CFh	IRQ Selection. See Table 10-10, "IRQ Assignment Table"
D0h-EFh	3D0h-3EFh	Reserved
F0h	3F0h	eSPI Virtual Wire Errors

10.7.2 ESPI, MEMORY COMPONENT REGISTERS

TABLE 10-4: ESPI MEMORY COMPONENT REGISTER SUMMARY

Host Offset	EC Offset	Host Offset
EC PRIVATE REGISTERS		
Peripheral Channel		
-	130h-193h	Memory Base Address Register, Internal Component See Table 10-7, "ESPI Memory Base Address Register Default Values"
-	1F8h-1FFh	SRAM Base Address Register Format, Internal Component See Table 10-8, "SRAM Base Address Register Default Values, Host Config"
-	200h	Bus Master Status Register
-	204h	Bus Master Interrupt Enable Register
-	208h	Bus Master Configuration Register
-	210h	Bus Master 1 Control Register
-	214h	Bus Master 1 Host Address Register
-	21Ch	Bus Master 1 Internal Address Register
-	224h	Bus Master 2 Control Register
-	228h	Bus Master 2 Host Address Register
-	230h	Bus Master 2 Internal Address Register
-	2E0h	TEST
-	2E4h	TEST
CONFIGURATION REGISTERS		
30h-A7h	330h-3A7h	Memory Base Address Configuration Register See Table 10-7, "ESPI Memory Base Address Register Default Values"
ACh-F7h	3ACh-3F7h	SRAM Base Address Configuration Register See Table 10-9, "SRAM Base Address Register Default Values, EC-Only"
B2h - F7h	3B2h - 3F7h	Reserved

10.7.3 VIRTUAL WIRE REGISTERS

TABLE 10-5: VIRTUAL WIRES REGISTER SUMMARY

EC Offset	Register Name
0h	MSVW00 Register
Ch	MSVW01 Register
18h	MSVW02 Register
24h	MSVW03 Register
30h	MSVW04 Register
3Ch	MSVW05 Register
48h	MSVW06 Register
54h	MSVW07 Register
60h	MSVW08 Register
6Ch	MSVW09 Register
78h	MSVW10 Register
84h - 1FFh	Reserved
200h	SMVW00 Register

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TABLE 10-5: VIRTUAL WIRES REGISTER SUMMARY (CONTINUED)

EC Offset	Register Name
208h	SMVW01 Register
210h	SMVW02 Register
218h	SMVW03 Register
220h	SMVW04 Register
228h	SMVW05 Register
230h	SMVW06 Register
238h	SMVW07 Register
240h	SMVW08 Register
248h	SMVW09 Register
250h	SMVW10 Register
242h - 3EFh	Reserved
3F0h	TEST
3F2h	TEST
3F8h	TEST
3FAh	TEST

10.8 Base Address Register Tables

TABLE 10-6: ESPI I/O BASE ADDRESS REGISTER DEFAULT VALUES

Host Config Index	EC Offset	Logical Device	Reset Default	EC-Only Offset	Reset Default	LDN	Mask (Note 1)
34h	334h	eSPI I/O Component (Configuration Port)	002E_0000h	134h	0000_0D01h	Dh	1h
38h	338h	eSPI Memory Component	0000_0000h	138h	0000_0E00h	Eh	0h
3Ch	33Ch	Mailbox	0000_0000h	13Ch	0000_0001h	0h	1h
40h	340h	8042 Emulated Key-board Controller	0060_0000h	140h	0000_0104h	1h	4h
44h	344h	ACPI EC Channel 0	0062_0000h	144h	0000_0204h	2h	4h
48h	348h	ACPI EC Channel 1	0000_0000h	148h	0000_0307h	3h	7h
4Ch	34Ch	ACPI EC Channel 2	0000_0000h	14Ch	0000_0407h	4h	7h
50h	350h	ACPI EC Channel 3	0000_0000h	150h	0000_0507h	5h	7h
54h	354h	ACPI EC Channel 4	0000_0000h	154h	0000_0607h	6h	7h
58h	358h	ACPI PM1	0000_0000h	158h	0000_0707h	7h	7h
5Ch	35Ch	Legacy (Fast Keyboard)	0092_0000h	15Ch	0000_0800h	8h	
60h	360h	UART 0	0000_0000h	160h	0000_0907h	9h	7h
64h	364h	UART 1	0000_0000h	164h	0000_0A07h	Ah	7h
68h	368h	Embedded Memory Interface (EMI) 0	0000_0000h	168h	0000_100Fh	10h	Fh
6Ch	36Ch	Embedded Memory Interface (EMI) 1	0000_0000h	16Ch	0000_110Fh	11h	Fh
70h	370h	Embedded Memory Interface (EMI) 2	0000_0000h	170h	0000_120Fh	12h	Fh

Note 1: The ACPI-EC0 Mask bit field is a read/write bit field. All other MASK bit fields are read-only as defined in the register description

TABLE 10-6: ESPI I/O BASE ADDRESS REGISTER DEFAULT VALUES (CONTINUED)

Host Config Index	EC Offset	Logical Device	Reset Default	EC-Only Offset	Reset Default	LDN	Mask (Note 1)
74h	374h	BIOS Debug Port (Port 80) 0	0000_0000h	174h	0000_2000h	20h	0h
78h	378h	BIOS Debug Port (Port 80) 1	0000_0000h	178h	0000_2100h	21h	0h
7Ch	37Ch	RTC	0000_0000h	17Ch	0000_141Fh	14h	1Fh
Note 1: The ACPI-EC0 Mask bit field is a read/write bit field. All other MASK bit fields are read-only as defined in the register description							

TABLE 10-7: ESPI MEMORY BASE ADDRESS REGISTER DEFAULT VALUES

Host Config Index	EC Offset	Logical Device	Reset Default	EC-Only Offset	Reset Default	LDN	Mask (Note 1)
30h	330h	Mailbox	00_0000h	130h	0000_0001h	0h	1h
3Ah	33Ah	ACPI EC Channel 0	62_0000h	13Ah	0000_0204h	2h	4h
44h	344h	ACPI EC Channel 1	00_0000h	144h	0000_0307h	3h	7h
4Eh	34Eh	ACPI EC Channel 2	00_0000h	14Eh	0000_0407h	4h	7h
58h	358h	ACPI EC Channel 3	00_0000h	158h	0000_0507h	5h	7h
62h	362h	ACPI EC Channel 4	00_0000h	162h	0000_0607h	6h	7h
6Ch	376h	Embedded Memory Interface (EMI) 0	00_0000h	16Ch	0000_100Fh	10h	Fh
76h	380h	Embedded Memory Interface (EMI) 1	00_0000h	176h	0000_110Fh	11h	Fh
80h	38Ah	Embedded Memory Interface (EMI) 2	00_0000h	180h	0000_120Fh	12h	Fh
Note 1: The ACPI-EC0 Mask bit field is a read/write bit field. All other MASK bit fields are read-only as defined in the register description							

TABLE 10-8: SRAM BASE ADDRESS REGISTER DEFAULT VALUES, HOST CONFIG

Host Config Index	EC Offset	Logical Device	Reset Default	LPC Host Address [79:16]	Size [7:4]	Access [2:1]
ACh	3ACh	SRAM BAR 0	0h	0h	0h	0h
B6h	3B6h	SRAM BAR 1	0h	0h	0h	0h

TABLE 10-9: SRAM BASE ADDRESS REGISTER DEFAULT VALUES, EC-ONLY

EC Offset	Logical Device	Reset Default	Base Address [47:16]	Size [7:4]	Access [2:1]	Valid [0]
1ACh	SRAM BAR 0	80h	0h	0h	0h	1h
1B6h	SRAM BAR 1	80h	0h	0h	0h	1h

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10.9 IRQ Table

TABLE 10-10: IRQ ASSIGNMENT TABLE

Host Config Index	EC Offset	Instance Name	Instance Number	Interrupt Source	Default Value
ACh	3ACh	Mailbox	0	MBX_Host_SIRQ	FFh
ADh	3ADh	Mailbox	0	MBX_Host_SMI	FFh
AEh	3AEh	8042	0	KIRQ	FFh
AFh	3AFh	8042	0	MIRQ	FFh
B0h	3B0h	ACPI EC	0	EC_OBE	FFh
B1h	3B1h	ACPI EC	1	EC_OBE	FFh
B2h	3B2h	ACPI EC	2	EC_OBE	FFh
B3h	3B3h	ACPI EC	3	EC_OBE	FFh
B4h	3B4h	ACPI EC	4	EC_OBE	FFh
B5h	3B5h	UART	0	UART	FFh
B6h	3B6h	UART	1	UART	FFh
B7h	3B7h	EMI	0	Host Event	FFh
B8h	3B8h	EMI	0	EC-to-Host	FFh
B9h	3B9h	EMI	1	Host Event	FFh
BAh	3BAh	EMI	1	EC-to-Host	FFh
BBh	3BBh	EMI	2	Host Event	FFh
BCh	3BCh	EMI	2	EC-to-Host	FFh
BDh	3BDh	RTC	0	RTC	FFh
BEh	3BEh	EC	0	EC_IRQ	FFh

10.10 Virtual Wires Table

TABLE 10-11: MASTER-TO-SLAVE VIRTUAL WIRE REGISTERS

Offset	Instance Name	Default Value
0h	MSVW00	00000000_04040404_00000102h
Ch	MSVW01	00000000_04040404_00000003h
18h	MSVW02	00000000_04040404_00000307h
24h	MSVW03	00000000_04040404_00000041h
30h	MSVW04	00000000_04040404_00000142h
3Ch	MSVW05	00000000_04040404_00000043h
48h	MSVW06	00000000_04040404_00000044h
54h	MSVW07	00000000_04040404_00000347h
60h	MSVW08	00000000_04040404_00000000h
6Ch	MSVW09	00000000_04040404_00000000h
78h	MSVW10	00000000_04040404_00000000h

TABLE 10-12: SLAVE-TO-MASTER VIRTUAL WIRE REGISTERS

Offset	Instance Name	Default Value
200h	SMVW00	01010000_0000C004h
208h	SMVW01	00000000_00000005h
210h	SMVW02	00010101_00007306h

TABLE 10-12: SLAVE-TO-MASTER VIRTUAL WIRE REGISTERS (CONTINUED)

Offset	Instance Name	Default Value
218h	SMVW03	00000000_00000040h
220h	SMVW04	00000000_00000045h
228h	SMVW05	00000000_00000046h
230h	SMVW06	00000000_00000000h
238h	SMVW07	00000000_00000000h
240h	SMVW08	00000000_00000000h
248h	SMVW09	00000000_00000000h
250h	SMVW10	00000000_00000000h

TABLE 10-13: RESERVED VIRTUAL WIRE REGISTERS

Index	Instance Name	Bit Number	Signal
02h	MSVW00	0	SLP_S3#
		1	SLP_S4#
		2	SLP_S5#
		3	Reserved
03h	MSVW01	0	SUS_STAT#
		1	PLTRST#
		2	OOB_RST_WARN
		3	Reserved
42h	MSVW04	0	SLP_LAN#
		1	SLP_WLAN#
		2	Reserved
		3	Reserved
06h	SMVW02	0	SCI#
		1	SMI#
		2	RC_IN#
		3	Reserved

10.10.1 RESERVED MASTER-TO-SLAVE VIRTUAL WIRES

Of the four signals associated with Master-to-Slave Index 03h, the PLTRST# may be used as part of the hardware that generates the reset signals eSPI_PLTRST# and RESET_HOST. This is due to eSPI timing requirements, which limit the amount of time available between the assertion of the PLTRST# Virtual Wire and the resetting of Peripheral Channel registers. The register PLTRST Source Register is used to select between the Virtual Wire and a pin as the source for eSPI_PLTRST#.

If firmware re-assigns the index for MSVW01 to 0h (i.e, invalidating the entry), firmware can assign a different MSVWxx register to Virtual Wire index 03h. In that case, firmware can assert PLTRST# by writing bit 1 of MSVW01, since the PLTRST# signal will still be connected to that register bit.

In order to maintain synchronization with the core logic in Deep S5 power states, the Boot ROM updates the SRC bits in two of the Master-to-Slave Virtual Wire registers on power on reset. Source for the copies is maintained in the VWire Backup Register in the VBAT Register Bank. Customer software is responsible for maintaining the backup register properly. The two Master-to-Slave Virtual Wire registers that are restored from the battery-backed register are MSVW00, which contains the signals SLP_S3#, SLP_S4# and SLP_S5#, associated with VWire index 2h, and MSVW04, which contains the signals SLP_LAN# and SLP_WLAN#, associated with the VWire index 42h.

Because the three registers described in this section are manipulated by either hardware or Boot ROM firmware, customer software should not modify the INDEX field in these registers.

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10.10.2 RESERVED SLAVE-TO-MASTER VIRTUAL WIRES

The Slave-to-Master Virtual Wire Register SMVW02 is hard wired to internally generated signals. Reset CPU INIT# (RCIN#) (Index 6h, bit 2), SMI# (Index 6h, bit 1) and SCI# (Index 6h, bit 0) are connected to the hardware blocks that generate the corresponding signals (the 8042 Emulation block, The Mailbox block and the ACPI PM1 block respectively). Firmware should **not** update the SRC bits for SMVW02 directly. If firmware control of the bits in Slave-to-Master Index 06h is required, then the INDEX field of SMVW02 should be set to 0h (disabling the register) and a different SMVWxx register should be configured for index 06h.

11.0 CHIP CONFIGURATION

11.1 Introduction

This chapter defines the mechanism to configure the device. Each logical device or block in the design has their own set of configuration registers. The Global Configuration Registers are use for chip-level configuration. The chip's Device ID and Revision are located in the Global Configuration space and may be used to uniquely identify this chip.

11.2 Terminology

This section documents terms used locally in this chapter. Common terminology that is used in the chip specification is captured in the Chip-Level Terminology section.

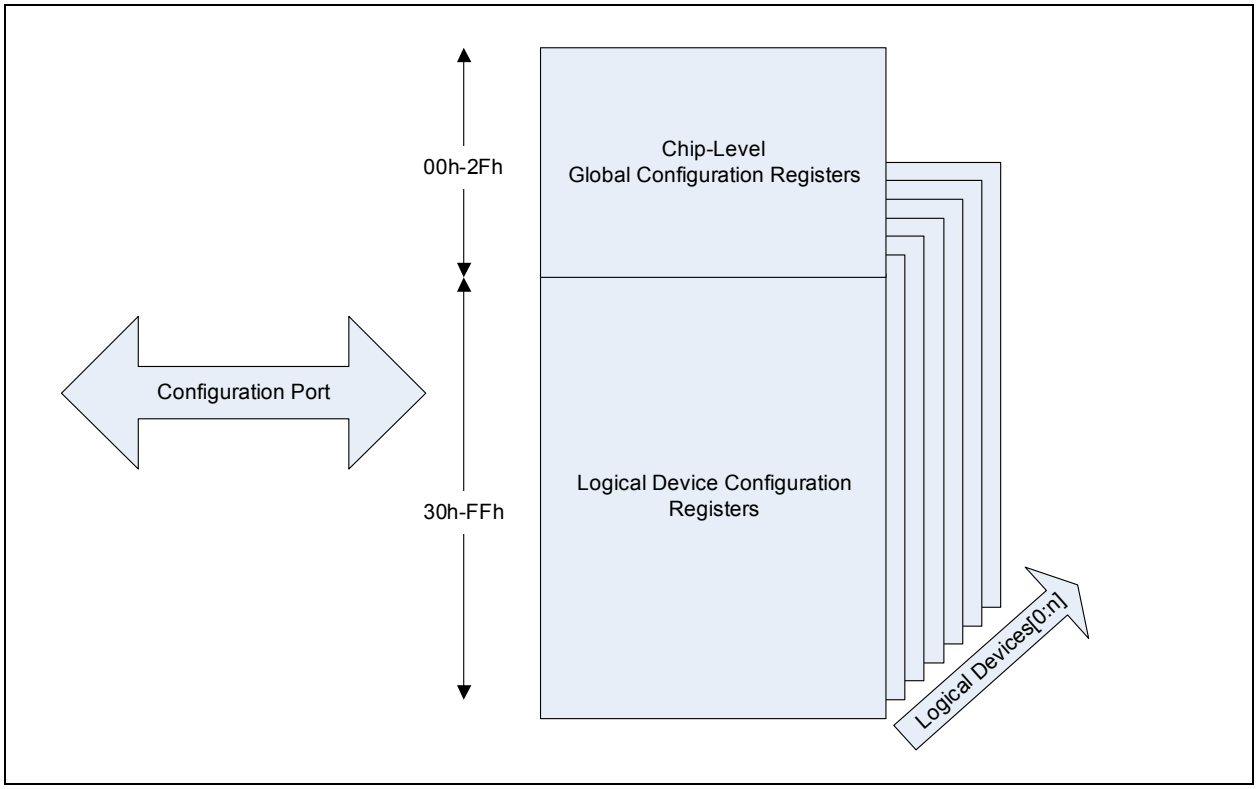
TABLE 11-1: TERMINOLOGY

Term	Definition
Global Configuration Registers	Registers used to configure the chip that are always accessible via the Configuration Port
Logical Device Configuration Registers	Registers used to configure a logical device in the chip. These registers are only accessible via the Configuration Port when enabled via the Global Configuration registers.

11.3 Interface

This block is designed to be accessed via the Host accessible Configuration Port.

FIGURE 11-1: BLOCK DIAGRAM OF CONFIGURATION PORT



Note: Each logical device has a bank of Configuration registers that are accessible at offsets 30h to FFh via the Configuration Port. The Logical Device number programmed in offset 07h determines which bank of configuration registers is currently accessible.

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11.3.1 HOST INTERFACE

The registers defined for the Chip Configuration are accessible by the Configuration Port when the device is in CONFIG MODE. For a description of the Configuration Port and CONFIG MODE see the description of the LPC Interface.

11.4 Power, Clocks and Reset

This section defines the Power, Clock, and Reset input parameters to this block.

11.4.1 POWER DOMAINS

TABLE 11-2: POWER SOURCES

Name	Description
VTR	The logic and registers implemented in this block reside on this single power well.

11.4.2 CLOCK INPUTS

This block does not require any special clock inputs.

11.4.3 RESETS

TABLE 11-3: RESET SIGNALS

Name	Description
RESET_SYS	Power on Reset to the entire device. This signal resets all the register and logic in this block to its default state.
RESET_HOST	A reset that occurs when VCC is turned off or when the system host resets the Host Interface.
RESET_eSPI	For systems with eSPI, a general reset signal for the eSPI block.

11.5 Interrupts

This block does not generate any interrupts.

11.6 Low Power Modes

This block always automatically adjusts to operate in the lowest power mode.

11.7 Description

The Chip Configuration Registers are divided into two groups: Global Configuration Registers and Logical Device Configuration registers. The following descriptions assume that the LPC interface has already been configured to operate in CONFIG MODE.

- Global Configuration Registers are always accessible via the LPC Configuration Port.
- The Logical Device Configuration registers are only accessible via the LPC Configuration Port when the corresponding Logical Device Number is loaded in the Logical Device Number register. The Logical Device Number register is a Global Configuration Register.

11.7.1 CONFIGURATION PORT

The eSPI Host can access the Chip's Configuration Registers through the Configuration Port when CONFIG MODE is enabled. The device defaults to CONFIG MODE being disabled.

Note:	The data read from the Configuration Port Data register is undefined when CONFIG MODE is not enabled.

The Configuration Port is composed of an INDEX and DATA Register. The INDEX register is used as an address pointer to an 8-bit configuration register and the DATA register is used to read or write the data value from the indexed configuration register. Once CONFIG MODE is enabled, reading the Configuration Port Data register will return the data value that is in the indexed Configuration Register.

If no value was written to the INDEX register, reading the Data Register in the Configuration Port will return the value in Configuration Address location 00h (default).

TABLE 11-4: CONFIGURATION PORT

Default I/O Address	Type	Register Name	Relative Address	Default Value	Notes
002Eh	Read / Write	INDEX	Configuration Port's Base Address + 0	00h	Note 1
002Fh	Read / Write	DATA	Configuration Port's Base Address + 1	00h	

Note 1: The default Base I/O Address of the Configuration Port can be relocated by programming the BAR register for Logical Device Ch (eSPI, I/O Configuration Port). The Relative Address shows the general case for determining the I/O address for each register.

11.7.2 ENABLE CONFIG MODE

The INDEX and DATA registers are effective only when the chip is in CONFIG MODE. CONFIG MODE is enabled when the Config Entry Key is successfully written to the I/O address of the INDEX register of the CONFIG PORT while the CONFIG MODE is disabled (see following section).

```
Config Entry Key = < 55h>
```

11.7.3 DISABLE CONFIG MODE

CONFIG MODE defaults to disabled on a RESET_SYS, RESET_HOST, and, for systems using eSPI, when RESET_HOST is asserted. CONFIG MODE is also disabled when the following Config Exit Key is successfully written to the I/O address of the INDEX PORT of the CONFIG PORT while CONFIG MODE is enabled.

```
Config Exit Key = < AAh>
```

11.7.4 CONFIGURATION SEQUENCE EXAMPLE

To program the configuration registers, the following sequence must be followed:

1. Enable Configuration State
2. Program the Configuration Registers
3. Disable Configuration State.

The following is an example of a configuration program in Intel 8086 assembly language.

```
;----------------------------.
; ENABLE CONFIGURATION STATE
;----------------------------'
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AX,055H; Config Entry Key
OUT     DX,AL
;----------------------------.
; CONFIGURE BASE ADDRESS,    |
; LOGICAL DEVICE 8           |
;----------------------------'
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AL,07H
OUT     DX,AL; Point to LD# Config Reg
MOV     DX,CONFIG_PORT_BASE_ADDRESS+1
MOV     AL, 08H
OUT DX,AL; Point to Logical Device 8
;
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AL,34H
OUT     DX,AL   ; Point to BASE ADDRESS REGISTER
MOV     DX,CONFIG_PORT_BASE_ADDRESS+1
MOV     AL,02H
OUT     DX,AL   ; Update BASE ADDRESS REGISTER
```


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```
;-----------------------------.
; DISABLE CONFIGURATION STATE
;-----------------------------'
MOV     DX,CONFIG_PORT_BASE_ADDRESS
MOV     AX,0AAH; Config Exit Key
OUT     DX,AL.
```

11.7.5 GLOBAL CONFIGURATION

There are 48 8-bit Global Configuration Registers (at offsets 00h through 2Fh), plus up to 208 8-bit registers associated with each Logical Device. The Logical Device is selected with the Logical Device Number Register (Global Configuration Register 07h).

Sequence to Access Logical Device Configuration Register:

a) Write the number of the Logical Device being accessed in the Logical Device Number Configuration Register by writing 07h into the INDEX PORT and the Logical Device Number into the DATA PORT.

b) Write the address of the desired logical device configuration register to the INDEX PORT and then write or read the value of the configuration register through the DATA PORT.

Note:	If accessing the Global Configuration Registers, step (a) is not required. Any write to an undefined or reserved Configuration register is terminated normally on the LPC bus without any modification of state in the MEC170x. Any read to an undefined or reserved Configuration register returns FFh

The following sections define the Global Configuration registers and the Logical Configuration registers.

11.7.6 GLOBAL CONTROL/CONFIGURATION REGISTERS

As with all Configuration Registers, the INDEX PORT is used to select a Global Configuration Register in the chip. The DATA PORT is then used to access the selected register. The INDEX and DATA PORTs are defined in the LPC Interface description.

11.8 Configuration Registers

Host access to Global Configuration Registers is through the Configuration Port (the INDEX PORT and the DATA PORT) using the Logical Device Number 3Fh and the Index shown in the “Offset” column of the following table. The EC can access Configuration Registers directly. The EC address for each register is formed by adding the Base Address for Global Configuration block shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the “Offset” column.

All Global Configuration registers are accessible to the Host through the Configuration Port for all Logical Devices. at offsets 00h through 2Fh.

TABLE 11-5: CHIP-LEVEL (GLOBAL) CONTROL/CONFIGURATION REGISTERS

Register	Host Offset	Description
Chip (Global) Control Registers		
Reserved	00h - 01h	Reserved - Writes are ignored, reads return 0.
TEST	02h	TEST. This register location is reserved for Microchip use. Modifying this location may cause unwanted results.
Reserved	03h - 06h	Reserved - Writes are ignored, reads return 0.
Logical Device Number	07h	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. **Note:** The Activate command operates only on the selected logical device.

TABLE 11-5: CHIP-LEVEL (GLOBAL) CONTROL/CONFIGURATION REGISTERS (CONTINUED)

Register	Host Offset	Description
Reserved	08h - 1Fh	Reserved - Writes are ignored, reads return 0.
Device ID	20h	A read-only register which provides device identification.
Device Revision Hard Wired	21h	A read-only register which provides device revision information. Bits[7:0] = current revision when read
TEST	22h - 23h	TEST. This register locations are reserved for Microchip use. Modifying these locations may cause unwanted results.
Reserved	24h	Reserved – writes are ignored, reads return “0”.
TEST	25h - 2Fh	TEST. This register locations are reserved for Microchip use. Modifying these locations may cause unwanted results.

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12.0 8042 EMULATED KEYBOARD CONTROLLER

12.1 Introduction

The MEC170x keyboard controller uses the EC to produce a superset of the features provided by the industry-standard 8042 keyboard controller. The 8042 Emulated Keyboard Controller is a Host/EC Message Interface with hardware assists to emulate 8042 behavior and provide Legacy GATEA20 support.

Note:	There is no VCC emulation in hardware for this interface.

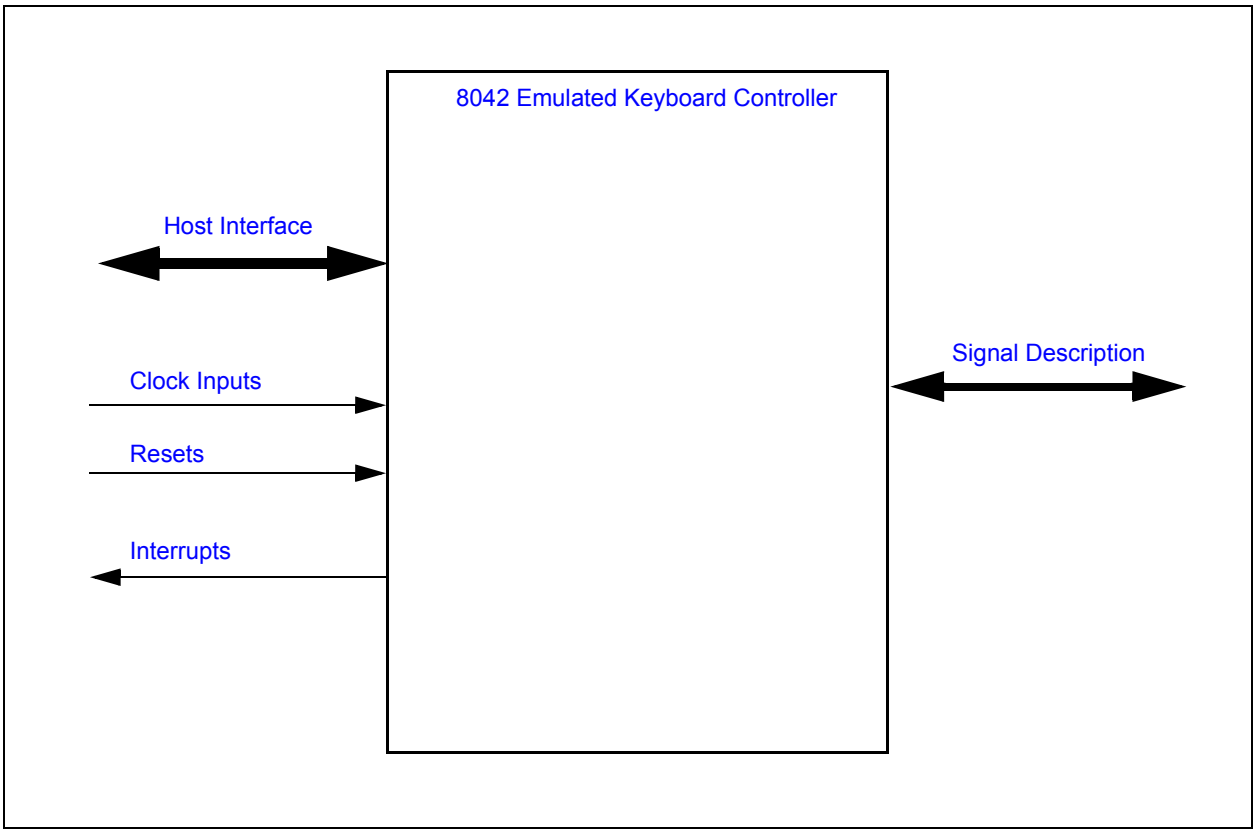
12.2 References

There are no references for this block.

12.3 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 12-1: I/O DIAGRAM OF BLOCK



12.4 Signal Description

TABLE 12-1: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
KBRST	Output	Keyboard Reset, routed to pin

12.5 Host Interface

The 8042 interface is accessed by host software via a registered interface, as defined in Section 12.13, "Configuration Registers" and Section 12.14, "Runtime Registers".

12.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

12.6.1 POWER DOMAINS

TABLE 12-2: POWER SOURCES

Name	Description
VTR	This Power Well is used to power the registers and logic in this block.

12.6.2 CLOCK INPUTS

TABLE 12-3: CLOCK INPUTS

Name	Description
1MHz	Clock used for the counter in the CPU_RESET circuitry.

12.6.3 RESETS

TABLE 12-4: RESET SIGNALS

Name	Description
RESET_SYS	This reset is asserted when VTR is applied.
RESET_VCC	This signal is asserted when the main power rail is off or held off by the PWR_INV bit in the Power Reset Control Register.
RESET_HOST	This signal is asserted when the main power rail is off or held off by the PWR_INV bit in the Power Reset Control Register, and also when the Host resets the Host-EC link via LRESET# or PLTRST#.

12.7 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 12-5: SYSTEM INTERRUPTS

Source	Description
KIRQ	This interrupt source for the SIRQ logic, representing a Keyboard interrupt, is generated when the PCOBF status bit is '1'.
MIRQ	This interrupt source for the SIRQ logic, representing a Mouse interrupt, is generated when the AUXOBF status bit is '1'.

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TABLE 12-6: EC INTERRUPTS

Source	Description
IBF	Interrupt generated by the host writing either data or command to the data register. This interrupt is asserted when the input buffer becomes not empty (i.e., when the IBF flag goes to 1).
OBE	Interrupt generated by the host reading either data or aux data from the data register. This interrupt is asserted when the output buffer becomes empty (i.e., when the OBF flag goes to 0).

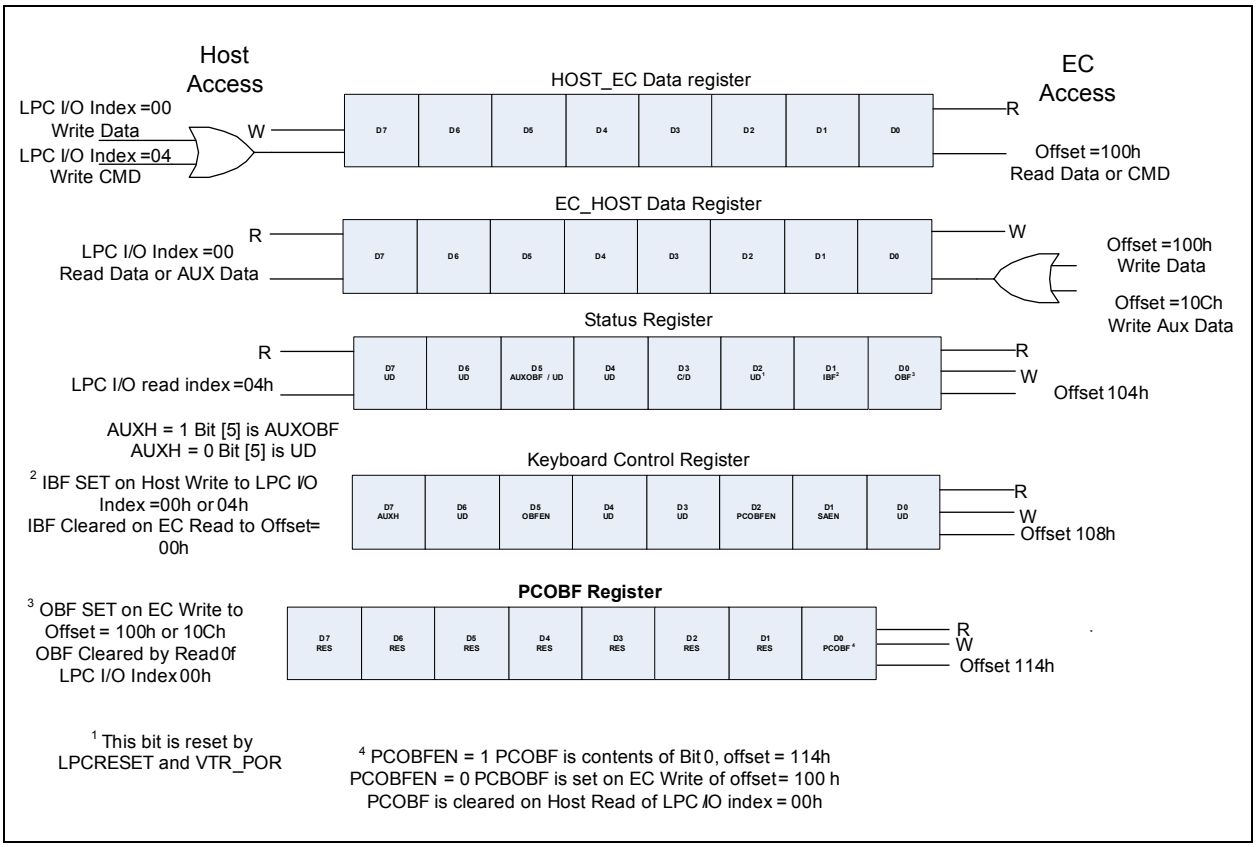
12.8 Low Power Modes

The 8042 Interface may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

12.9 Description

12.9.1 BLOCK DIAGRAM

FIGURE 12-2: BLOCK DIAGRAM OF 8042 Emulated Keyboard Controller



12.10 EC-to-Host Keyboard Communication

The EC can write to the EC_HOST Data / AUX Data Register by writing to the HOST2EC Data Register at EC-Only offset 0h or the EC AUX Data Register at EC-Only offset Ch. A write to either of these addresses automatically sets bit 0 (OBF) in the Status register. A write to the HOST2EC Data Register may also set PCOBF. A write to the EC AUX Data Register may also set AUXOBF.

12.10.1 PCOBF DESCRIPTION

If enabled by the bit OBFEN, the bit PCOBF is gated onto KIRQ. The KIRQ signal is a system interrupt which signifies that the EC has written to the HOST2EC Data Register (EC-Only offset 0h). On power-up, PCOBF is reset to 0. PCOBF will normally reflect the status of writes to HOST2EC register, if PCOBFEN is “0”. PCOBF is cleared by hardware on a HOST read of the EC_HOST Data / AUX Data Register.

KIRQ is normally selected as IRQ1 for keyboard support.

Additional flexibility has been added which allows firmware to directly control the PCOBF output signal, independent of data transfers to the host-interface data output register. This feature allows the MEC170x to be operated via the host “polled” mode. Firmware control is active when PCOBFEN is ‘1’. Firmware sets PCOBF high by writing a “1” to the PCOBF field of the PCOBF Register. Firmware must also clear PCOBF by writing a “0” to the PCOBF field.

The PCOBF register is also readable; the value read back on bit 0 of the register always reflects the present value of the PCOBF output. If PCOBFEN = 1, then this value reflects the output of the firmware latch in the PCOBF Register. If PCOBFEN = 0, then the value read back reflects the in-process status of write cycles to the HOST2EC Data Register (i.e., if the value read back is high, the host interface output data register has just been written to). If OBFEN=0, then KIRQ is driven inactive (low).

12.10.2 AUXOBF DESCRIPTION

If enabled by the bit OBFEN, the bit AUXOBF is multiplexed onto MIRQ. The AUXOBF/MIRQ signal is a system interrupt which signifies that the EC has written to the EC_HOST Data / AUX Data Register. On power-up, after RESET_SYS, AUXOBF is reset to 0. AUXOBF will normally reflects the status of writes to EC EC AUX Data Register (EC-Only offset Ch). AUXOBF is cleared by hardware on a read of the Host Data Register. If OBFEN=0, then MIRQ is driven inactive (low).

MIRQ is normally selected as IRQ12 for mouse support.

Firmware can also directly control the AUXOBF output signal, similar to the mechanism it can use to control PCOBF. Firmware control is active when AUXH is ‘0’. Firmware sets AUXOBF high by writing a “1” to the AUXOBF field of the EC Keyboard Status Register. Firmware must also clear AUXOBF by writing a “0” to the AUXOBF field.

TABLE 12-7: OBFEN AND PCOBFEN EFFECTS ON KIRQ

OBFEN	PCOBFEN	
0	X	KIRQ is inactive and driven low
1	0	KIRQ = PCOBF (status of writes to HOST2EC Data Register)
1	1	KIRQ = PCOBF (status of writes to PCOBF Register)

TABLE 12-8: OBFEN AND AUXH EFFECTS ON MIRQ

OBFEN	AUXH	
0	X	MIRQ is inactive and driven low
1	0	MIRQ = AUXOBF (status of writes to EC AUX Data Register)
1	1	MIRQ = AUXOBF (status of writes to AUXOBF in EC Keyboard Status Register)

12.11 Legacy Port92/GATEA20 Support

The MEC170x supports LPC I/O writes to port HOST I/O address 92h as a quick alternate mechanism for generating a CPU_RESET pulse or controlling the state of GATEA20. The Port92/GateA20 logic has a separate Logical Device Number and Base Address register (see Section 12.16, "Legacy Port92/GATEA20 Configuration Registers" and Section 12.17, "Legacy Port92/GATEA20 Runtime Registers". The Base Address Register for the Port92/GateA20 Logical Device has only one writable bit, the Valid Bit, since the only I/O accessible Register has a fixed address.

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The Port 92 Register resides at HOST I/O address 92h and is used to support the alternate reset (ALT_RST#) and alternate GATEA20 (ALT_A20) functions. This register defaults to 00h on assertion of RESET_VCC.

Setting the Port92 Enable bit (Port 92 Enable Register) enables the Port92h Register. When Port92 is disabled, by clearing the Port92 Enable bit, then access to this register is completely disabled (I/O writes to host 92h are ignored and I/O reads float the system data bus SD[7:0]).

12.11.1 GATE A20 SPEEDUP

The MEC170x contains on-chip logic support for the GATEA20 hardware speed-up feature. GATEA20 is part of the control required to mask address line A20 to emulate 8086 addressing.

In addition to the ability for the host to control the GATEA20 output signal directly, a configuration bit called SAEN in the Keyboard Control Register is provided; when set, SAEN allows firmware to control the GATEA20 output. When SAEN is set, a 1 bit register (GATEA20 Control Register) controls the GATEA20 output.

Host control and firmware control of GATEA20 affect two separate register elements. Read back of GATEA20 through the use of EC OFFSET 100h reflects the present state of the GATEA20 output signal: if SAEN is set, the value read back corresponds to the last firmware-initiated control of GATEA20; if SAEN is reset, the value read back corresponds to the last host-initiated control of GATEA20.

Host control of the GATEA20 output is provided by the hardware interpretation of the “GATEA20 sequence” (see Table 12-9, "GATEA20 Command/Data Sequence Examples"). The foregoing description assumes that the SAEN configuration bit is reset.

When the MEC170x receives a “D1” command followed by data (via the host interface), the on-chip hardware copies the value of data bit 1 in the received data field to the GATEA20 host latch. At no time during this host-interface transaction will PCOBF or the IBF flag (bit 1) in the EC Keyboard Status Register be activated; for example, this host control of GATEA20 is transparent to firmware, with no consequent degradation of overall system performance. Table 12-9 details the possible GATEA20 sequences and the MEC170x responses.

An additional level of control flexibility is offered via a memory-mapped synchronous set and reset capability. Any data written to the SETGA20L Register causes the GATEA20 host latch to be set; any data written to the RSTGA20L Register causes it to be reset. This control mechanism should be used with caution. It was added to augment the “normal” control flow as described above, not to replace it. Since the host and the firmware have asynchronous control capability of the host latch via this mechanism, a potential conflict could arise. Therefore, after using the SETGA20L and RSTGA20L registers, firmware should read back the GATEA20 status via the GATEA20 Control Register (with SAEN = 0) to confirm the actual GATEA20 response.

TABLE 12-9: GATEA20 COMMAND/DATA SEQUENCE EXAMPLES

Data Byte	R/W	D[0:7]	IBF Flag	GATEA20	Comments
1 0 1	W W W	D1 DF FF	0 0 0	Q 1 1	GATEA20 Turn-on Sequence
1 0 1	W W W	D1 DD FF	0 0 0	Q 0 0	GATEA20 Turn-off Sequence
1 1 0 1	W W W W	D1 D1 DF FF	0 0 0 0	Q Q 1 1	GATEA20 Turn-on Sequence(*)
1 1 0 1	W W W W	D1 D1 DD FF	0 0 0 0	Q Q 0 0	GATEA20 Turn-off Sequence(*)

TABLE 12-9: GATEA20 COMMAND/DATA SEQUENCE EXAMPLES (CONTINUED)

Data Byte	R/W	D[0:7]	IBF Flag	GATEA20	Comments
1	W	D1	0	Q	Invalid Sequence
1	W	XX**	1	Q	
1	W	FF	1	Q	

Note: The following notes apply:

- All examples assume that the SAEN configuration bit is 0.
- “Q” indicates the bit remains set at the previous state.
- *Not a standard sequence.
- **XX = Anything except D1.
- If multiple data bytes, set IBF and wait at state 0. Let the software know something unusual happened.
- For data bytes, only D[1] is used; all other bits are don't care.
- Host Commands (FF, FE, and D1) do not cause IBF. The method of blocking IBF in Figure 12-4 is the nIOW not being asserted when FF, FE, and D1 Host commands are written”.

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The hardware GATEA20 state machine returns to state S1 from state S2 when CMD = D1, as shown in the following figures:.

FIGURE 12-3: GATEA20 STATE MACHINE

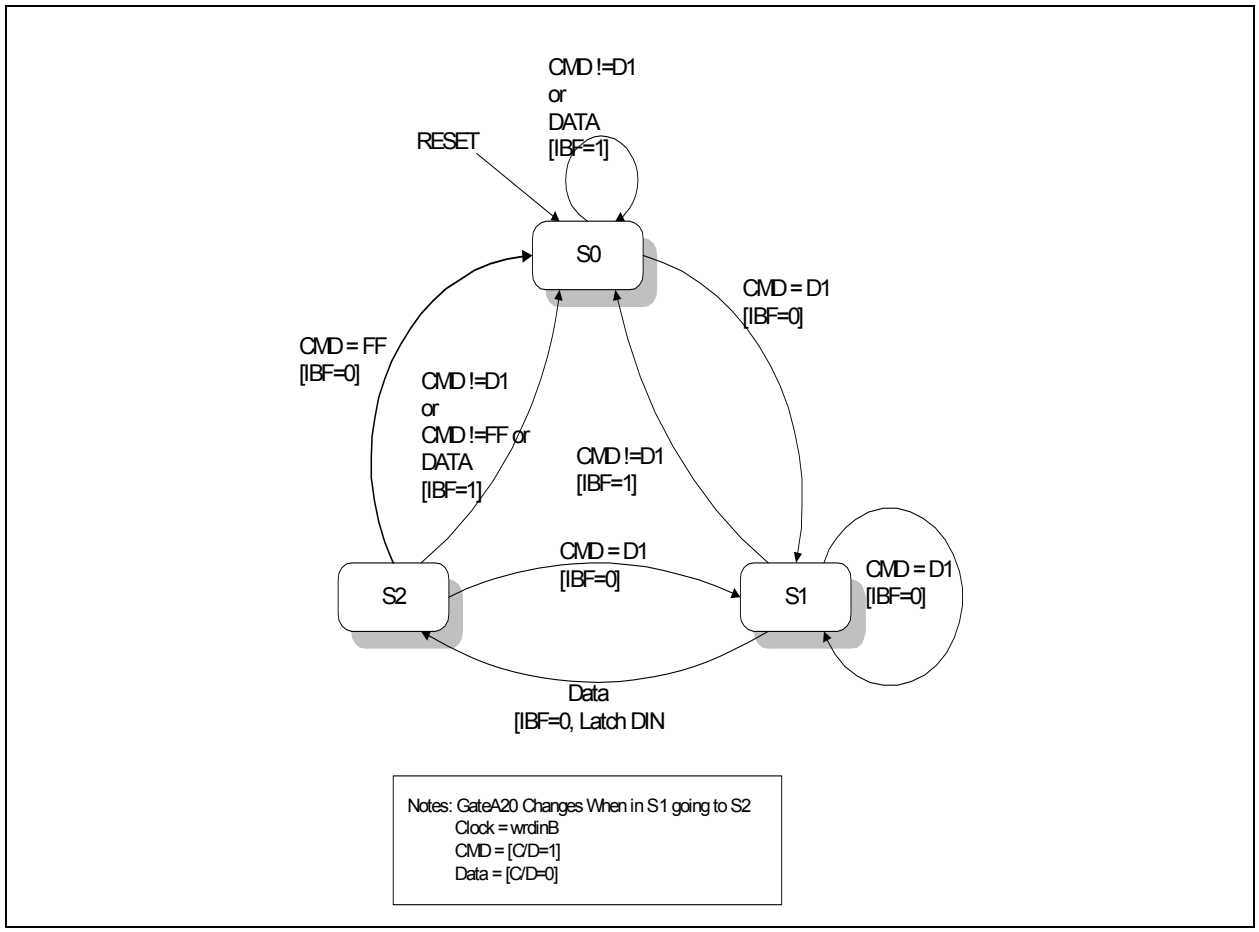
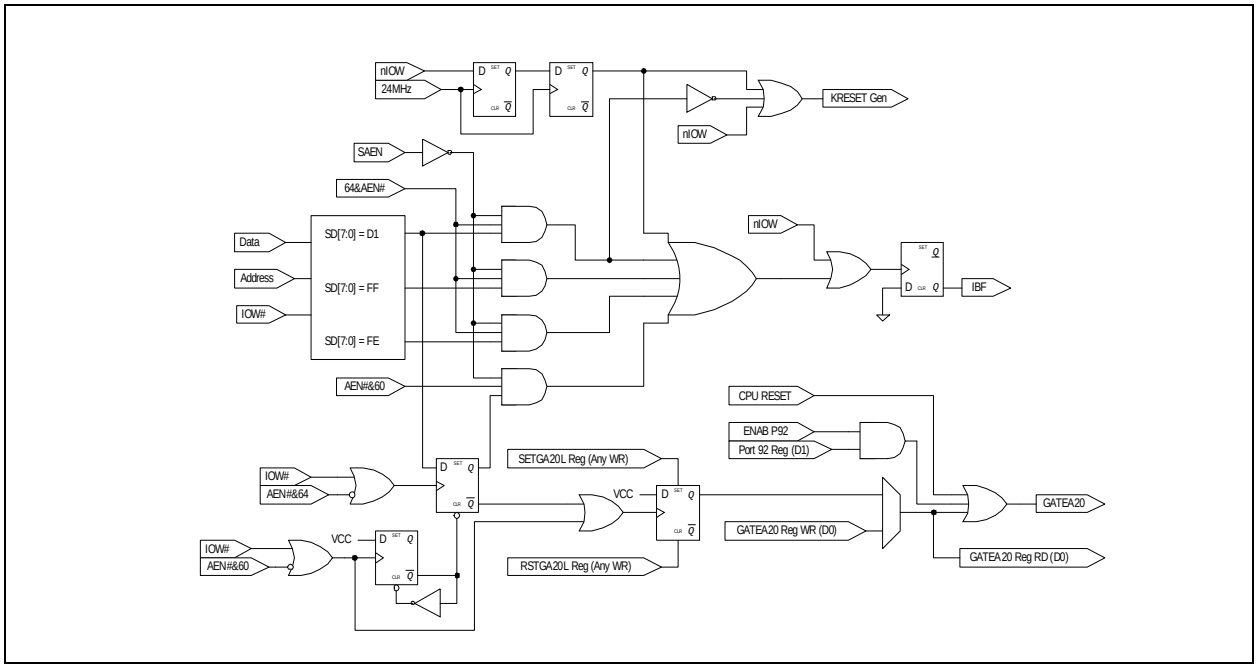


FIGURE 12-4: GATEA20 IMPLEMENTATION DIAGRAM



12.11.2 CPU_RESET HARDWARE SPEED-UP

The ALT_CPU_RESET bit generates, under program control, the ALT_RST# signal, which provides an alternate, means to drive the MEC170x CPU_RESET pin which in turn is used to reset the Host CPU. The ALT_RST# signal is internally NANDed together with the KBDRESET# pulse from the KRESET Speed up logic to provide an alternate software means of resetting the host CPU.

Before another ALT_RST# pulse can be generated, ALT_CPU_RESET must be cleared to '0' either by an RESET_VCC or by a write to the Port 92 Register with bit 0 = '0'. An ALT_RST# pulse is not generated in the event that the ALT_CPU_RESET bit is cleared and set before the prior ALT_RESET# pulse has completed.

If the 8042EM Sleep Enable is asserted, or the 8042 EM ACTIVATE bit is de-asserted, the 1MHz clocks source is disabled.

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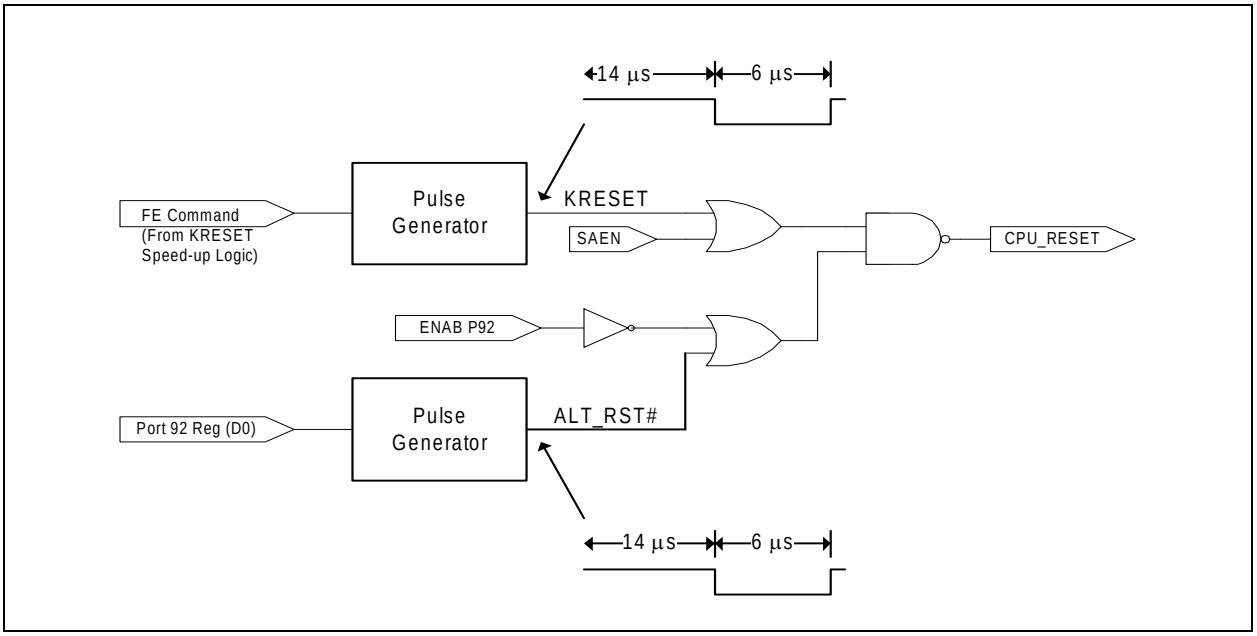
FIGURE 12-5: CPU_RESET IMPLEMENTATION DIAGRAM



12.12 Instance Description

There are two blocks defined in this chapter: Emulated 8042 Interface and the Port 92-Legacy Interface. The MEC170x has one instance of each block.

12.13 Configuration Registers

Configuration Registers for an instance of the 8042 Emulated Keyboard Controller are listed in the following table. Host access to Configuration Registers is through the Configuration Port using the Logical Device Number of the 8042 Emulated Keyboard Controller instance and the Index shown in the “Host Index” column of the table. The EC can access Configuration Registers directly. The EC address for each register is formed by adding the Base Address for each instance of the 8042 Emulated Keyboard Controller shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the “EC Offset” column.

TABLE 12-10: CONFIGURATION REGISTER SUMMARY

EC Offset	Host Index	Register Name
330h	30h	Activate Register

12.13.1 ACTIVATE REGISTER

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	ACTIVATE 1=The 8042 Interface is powered and functional. 0=The 8042 Interface is powered down and inactive.	R/W	0b	RESET_VCC

12.14 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the 8042 Emulated Keyboard Controller. Host access for each register listed in this table is defined as an offset in the Host address space to the Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for the 8042 Emulated Keyboard Controller shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

TABLE 12-11: RUNTIME REGISTER SUMMARY

Offset	Register Name
0h/04h	HOST_EC Data / CMD Register
0h	EC_HOST Data / AUX Data Register
4h	Keyboard Status Read Register

12.14.1 HOST_EC DATA / CMD REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	WRITE_DATA This 8-bit register is write-only. When written, the C/D bit in the Keyboard Status Read Register is cleared to '0', signifying data, and the IBF in the same register is set to '1'. When the Runtime Register at offset 0h is read by the Host, it functions as the EC_HOST Data / AUX Data Register.	W	0h	RESET_SYS

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	WRITE_CMD .This 8-bit register is write-only and is an alias of the register at offset 0h. When written, the C/D bit in the Keyboard Status Read Register is set to '1', signifying a command, and the IBF in the same register is set to '1'. When the Runtime Register at offset 4h is read by the Host, it functions as the Keyboard Status Read Register.	W	0h	RESET_SYS

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12.14.2 EC_HOST DATA / AUX DATA REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	READ_DATA This 8-bit register is read-only. When read by the Host, the PCOBF and/or AUXOBF interrupts are cleared and the OBF flag in the status register is cleared.	R	0h	RESET_SYS

12.14.3 KEYBOARD STATUS READ REGISTER

This register is a read-only alias of the EC Keyboard Status Register.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	UD2 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R	0h	RESET_SYS
5	AUXOBF Auxiliary Output Buffer Full. This bit is set to “1” whenever the EC writes the EC AUX Data Register. This flag is reset to “0” whenever the EC writes the EC Data Register.	R	0h	RESET_SYS
4	UD1 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R	0h	RESET_SYS
3	C/D Command Data. This bit specifies whether the input data register contains data or a command (“0” = data, “1” = command). During a Host command write operation (when the Host writes the HOST_EC Data / CMD Register at offset 04h), this bit is set to “1”. During a Host data write operation (when the Host writes the HOST_EC Data / CMD Register at offset 0h), this bit is set to “0”.	R	0h	RESET_SYS
2	UD0 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R	0h	RESET_HOST
1	IBF Input Buffer Full. This bit is set to “1” whenever the Host writes data or a command into the HOST_EC Data / CMD Registerr. When this bit is set, the EC's IBF interrupt is asserted, if enabled. When the EC reads the HOST_EC Data/CMD Register, this bit is automatically reset and the interrupt is cleared. This bit is not reset on RESET_VCC. To clear this bit, firmware must read the HOST2EC Data Register in the EC-Only address space.	R	0h	RESET_SYS

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	OBF Output Buffer Full. This bit is set when the EC writes a byte of Data or AUX Data into the EC_HOST Data / AUX Data Register. When the Host reads the HOST_EC Data / CMD Register, this bit is automatically cleared by hardware and an OBE interrupt is generated. This bit is not reset on RESET_VCC. To clear this bit, firmware must read the HOST2EC Data Register in the EC-Only address space.	R	0h	RESET_SYS

12.15 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the 8042 Emulated Keyboard Controller Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 12-12: EC-ONLY REGISTER SUMMARY

Offset	Register Name
100h	HOST2EC Data Register
100h	EC Data Register
104h	EC Keyboard Status Register
108h	Keyboard Control Register
10Ch	EC AUX Data Register
114h	PCOBF Register

12.15.1 HOST2EC DATA REGISTER

Offset	100h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOST2EC_DATA This register is an alias of the HOST_EC Data / CMD Register. When read at the EC-Only offset of 0h, it returns the data written by the Host to either Runtime Register offset 0h or Runtime Register offset 04h.	R	0h	RESET_SYS

12.15.2 EC DATA REGISTER

Offset	100h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA	W	0h	RESET_SYS

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12.15.3 EC KEYBOARD STATUS REGISTER

This register is an alias of the Keyboard Status Read Register. The fields C/D, IBF, and OBF remain read-only.

Offset	104h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	UD2 User-defined data. Readable and writable by the EC.	R/W	0h	RESET_SYS
5	AUXOBF Auxiliary Output Buffer Full. This bit is set to '1' whenever the EC writes the EC AUX Data Register. This flag is reset to '0' whenever the EC writes the EC Data Register.	R/W	0h	RESET_SYS
4	UD1 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R/W	0h	RESET_SYS
3	C/D Command Data. This bit specifies whether the input data register contains data or a command. During a Host command write operation (when the Host writes the HOST_EC Data / CMD Register at offset 04h), this bit is set to '1'. During a Host data write operation (when the Host writes the HOST_EC Data / CMD Register at offset 0h), this bit is set to '0'. 1=Command 0=Data	R	0h	RESET_SYS
2	UD0 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R/W	0h	RESET_HOST
1	IBF Input Buffer Full. This bit is set to "1" whenever the Host writes data or a command into the HOST_EC Data / CMD Registerr. When this bit is set, the EC's IBF interrupt is asserted, if enabled. When the EC reads the Data/CMD Register, this bit is automatically reset and the interrupt is cleared. This bit is not reset on RESET_VCC. To clear this bit, firmware must read the HOST2EC Data Register in the EC-Only address space.	R	0h	RESET_SYS
0	OBF Output Buffer Full. This bit is set when the EC writes a byte of Data or AUX Data into the EC_HOST Data / AUX Data Register. When the Host reads the HOST_EC Data / CMD Register, this bit is automatically cleared by hardware and a OBE interrupt is generated. This bit is not reset on RESET_VCC. To clear this bit, firmware must read the HOST2EC Data Register in the EC-Only address space.	R	0h	RESET_SYS

12.15.4 KEYBOARD CONTROL REGISTER

Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	AUXH AUX in Hardware. 1=AUXOBF of the Keyboard Status Read Register is set in hardware by a write to the EC AUX Data Register 0=AUXOBF is not modified in hardware, but can be read and written by the EC using the EC-Only alias of the EC Keyboard Status Register	R/W	0h	RESET_SYS
6	UD5 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R/W	0h	RESET_SYS
5	OBFEN When this bit is '1', the system interrupt signal KIRQ is driven by the bit PCOBF and MIRQ is driven by AUXOBF. When this bit is '0', KIRQ and MIRQ are driven low. This bit must not be changed when OBF of the status register is equal to '1'.	R/W	0h	RESET_SYS
4:3	UD4 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R/W	0h	RESET_SYS
2	PCOBFEN 1=reflects the value written to the PCOBF Register 0=PCOBF reflects the status of writes to the EC Data Register	R/W	0h	RESET_SYS
1	SAEN Software-assist enable. 1=This bit allows control of the GATEA20 signal via firmware 0=GATEA20 corresponds to either the last Host-initiated control of GATEA20 or the firmware write to the Keyboard Control Register or the EC AUX Data Register.	R/W	0h	RESET_SYS
0	UD3 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R/W	0h	RESET_SYS

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12.15.5 EC AUX DATA REGISTER

Offset	10Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_AUX_DATA This 8-bit register is write-only. When written, the C/D in the Keyboard Status Read Register is cleared to '0', signifying data, and the IBF in the same register is set to '1'. When the Runtime Register at offset 0h is read by the Host, it functions as the EC_HOST Data / AUX Data Register.	W	0h	RESET_SYS

12.15.6 PCOBF REGISTER

Offset	114h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	PCOBF For a description of this bit, see Section 12.10.1, "PCOBF Description".	R/W	0h	RESET_SYS

12.16 Legacy Port92/GATEA20 Configuration Registers

Configuration Registers for an instance of the Port92-Legacy block are listed in the following table. Host access to Configuration Registers is through the Configuration Port using the Logical Device Number of the Port 92 instance and the Index shown in the "Host Index" column of the table. The EC can access Configuration Registers directly. The EC address for each register is formed by adding the Base Address for each instance of the Port 92 block shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "EC Offset" column.

TABLE 12-13: CONFIGURATION REGISTER SUMMARY

EC Offset	Host Index	Register Name
330h	30h	Port 92 Enable Register

12.16.1 PORT 92 ENABLE REGISTER

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	P92_EN When this bit is '1', the Port92h Register is enabled. When this bit is '0', the Port92h Register is disabled, and Host writes to LPC address 92h are ignored.	R/W	0h	RESET_VCC

12.17 Legacy Port92/GATEA20 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the Legacy Port92/GATEA20 logic. The addresses of each register listed in this table are defined as a relative offset to the host "Base Address" defined in the Runtime Register Base Address Table.

TABLE 12-14: RUNTIME REGISTER BASE ADDRESS TABLE

Block Instance	Instance Number	Host	Address Space	Base Address
Port92-Legacy	0	LPC	I/O	0092h
		EC	32-bit address space	400F_2000h

The Base Address indicates where the first register can be accessed in a particular address space for a block instance.

TABLE 12-15: RUNTIME REGISTER SUMMARY

Offset	Register Namer
0h	Port 92 Register

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12.17.1 PORT 92 REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	-	-
1	ALT_GATE_A20 This bit provides an alternate means for system control of the GATEA20 pin. ALT_A20 low drives GATEA20 low, if A20 from the keyboard controller is also low. When Port 92 is enabled, writing a 1 to this bit forces ALT_A20 high. ALT_A20 high drives GATEA20 high regardless of the state of A20 from the keyboard controller. 0=ALT_A20 is driven low 1=ALT_A20 is driven high	R/W	0h	RESET_HOST
0	ALT_CPU_RESET	R/W	0h	RESET_HOST

12.18 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Port92-Legacy Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 12-16: REGISTER SUMMARY

Offset	Register Name
100h	GATEA20 Control Register
108h	SETGA20L Register
10Ch	RSTGA20L Register

12.18.1 GATEA20 CONTROL REGISTER

Offset	100h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	GATEA20 See Section 12.11.1, "GATE A20 Speedup" for information on this register. 0=The GATEA20 output is driven low 1=The GATEA20 output is driven high	R/W	1h	RESET_HOST

12.18.2 SETGA20L REGISTER

Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	SETGA20L See Section 12.11.1, "GATE A20 Speedup" for information on this register. A write to this register sets GATEA20 in the GATEA20 Control Register.	W	-	-

12.18.3 RSTGA20L REGISTER

Offset	10Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	RSTGA20L See Section 12.11.1, "GATE A20 Speedup" for information on this register. A write to this register sets GATEA20 in the GATEA20 Control Register.	W	-	-

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13.0 ACPI EMBEDDED CONTROLLER INTERFACE (ACPI-ECI)

13.1 Introduction

The ACPI Embedded Controller Interface (ACPI-ECI) is a Host/EC Message Interface. The ACPI specification defines the standard hardware and software communications interface between the OS and an embedded controller. This interface allows the OS to support a standard driver that can directly communicate with the embedded controller, allowing other drivers within the system to communicate with and use the EC resources; for example, Smart Battery and AML code.

The ACPI Embedded Controller Interface (ACPI-ECI) provides a four byte full duplex data interface which is a superset of the standard ACPI Embedded Controller Interface (ACPI-ECI) one byte data interface. The ACPI Embedded Controller Interface (ACPI-ECI) defaults to the standard one byte interface.

The MEC170x has two instances of the ACPI Embedded Controller Interface.

1. The EC host in Section 13.12, "Runtime Registers" and Section 13.13, "EC Registers" corresponds to the EC in the ACPI specification. This interface is referred to elsewhere in this chapter as ACPI_EC.
2. The LPC host in Section 13.12, "Runtime Registers" and Section 13.13, "EC Registers" corresponds to the “System Host Interface to OS” in the ACPI specification. This interface is referred to elsewhere in this chapter as ACPI_OS.

13.2 References

- Advanced Configuration and Power Interface Specification, Revision 4.0 June 16, 2009, Hewlett-Packard Corporation Intel Corporation Microsoft Corporation Phoenix Technologies Ltd. Toshiba Corporation

13.3 Terminology

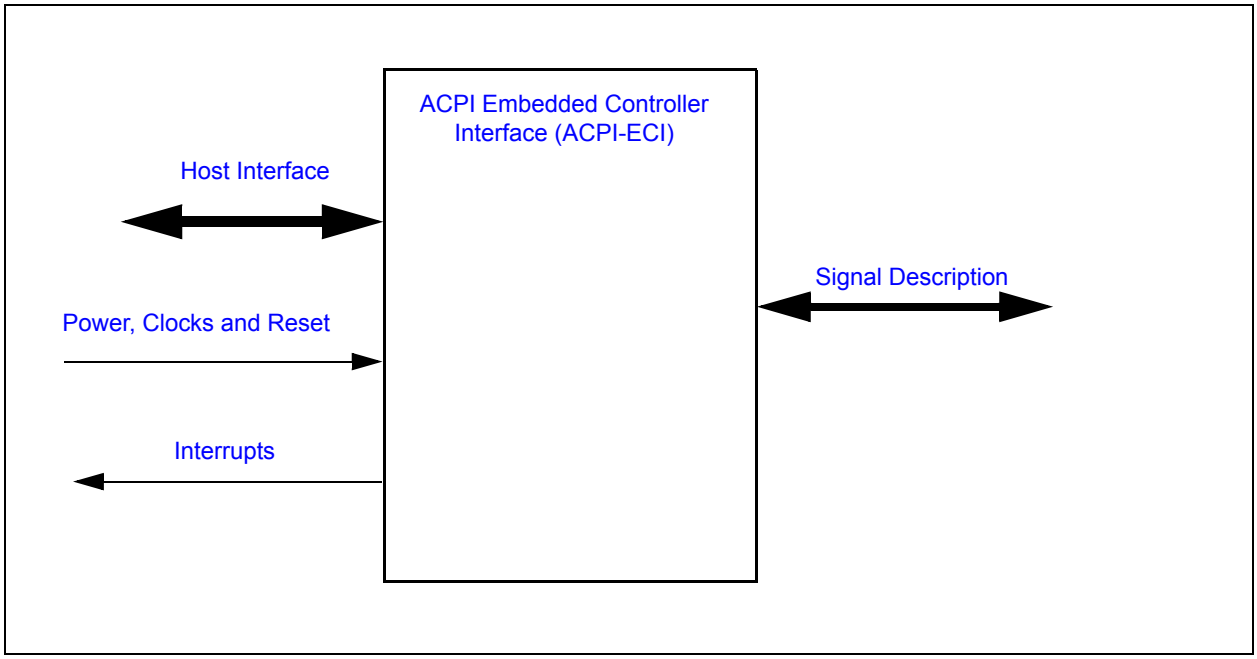
TABLE 13-1: TERMINOLOGY

Term	Definition
ACPI_EC	The EC host corresponding to the ACPI specification interface to the EC.
ACPI_OS	The LPC host corresponding to the ACPI specification interface to the “System Host Interface to OS”. ACPI_OS terminology is not meant to distinguish the ACPI System Management from Operating System but merely the hardware path upstream towards the CPU.

13.4 Interface

This block is designed to be accessed externally and internally via a register interface.

FIGURE 13-1: I/O DIAGRAM OF BLOCK



13.5 Signal Description

There are no external signals.

13.6 Host Interface

The registers defined for the ACPI Embedded Controller Interface (ACPI-ECI) are accessible by the System Host and the Embedded Controller as indicated in Section 13.12, "Runtime Registers" and Section 13.13, "EC Registers".

13.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

13.7.1 POWER DOMAINS

TABLE 13-2: POWER SOURCES

Name	Description
VTR	The logic and registers implemented in this block reside on this single power well.

13.7.2 CLOCK INPUTS

This block only requires the Host interface clocks to synchronize registers access.

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13.7.3 RESETS

TABLE 13-3: RESET SIGNALS

Name	Description
RESET_SYS	This signal resets all the logic and registers in this interface.

13.8 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 13-4: SYSTEM INTERRUPTS

Source	Description
EC_OBE	This host interrupt is asserted when the OBF bit in the EC STATUS Register is cleared to ‘0’.

TABLE 13-5: EC INTERRUPTS

Source	Description
IBF	Interrupt generated by the host writing either data or command to the data register. This interrupt is asserted when the input buffer becomes not empty (i.e., when the IBF flag goes to 1).
OBE	Interrupt generated by the host reading either data or aux data from the data register. This interrupt is asserted when the output buffer becomes empty (i.e., when the OBF flag goes to 0).

Note: The usage model from the ACPI specification requires both SMI’s and SCI’s. The ACPI_OS SMI and SCI interrupts are not implemented in the ACPI Embedded Controller Interface (ACPI-ECI). The SMI_EVT and SCI_EVT bits in the OS STATUS OS Register are software flags and this block do not initiate SMI or SCI events.

13.9 Low Power Modes

The ACPI Embedded Controller Interface (ACPI-ECI) automatically enters low power mode when no transaction targets it.

13.10 Description

The ACPI Embedded Controller Interface (ACPI-ECI) provides an APCI-EC interface that adheres to the ACPI specification. The ACPI Embedded Controller Interface (ACPI-ECI) includes two modes of operation: Legacy Mode and Four-byte Mode.

The ACPI Embedded Controller Interface (ACPI-ECI) defaults to Legacy Mode which provides single byte Full Duplex operation. Legacy Mode corresponds to the ACPI specification functionality as illustrated in Figure 13-2, "Block Diagram corresponding to the ACPI specification". The EC interrupts in Figure 13-2 are implemented as OBE and IBF. See Section 13.8, "Interrupts".

In Four-byte Mode, the ACPI Embedded Controller Interface (ACPI-ECI) provides four byte Full Duplex operation. Four-byte Mode is a superset of the ACPI specification functionality as illustrated in Figure 13-2, "Block Diagram corresponding to the ACPI specification".

Both Legacy Mode and Four-byte Mode provide Full Duplex Communications which allows data/command transfers in one direction while maintaining data from the other direction; communications can flow both ways simultaneously.

In Legacy Mode, ACPI Embedded Controller Interface (ACPI-ECI) contains three registers: ACPI OS COMMAND Register, OS STATUS OS Register, and OS2EC Data EC Byte 0 Register. The standard ACPI Embedded Controller Interface (ACPI-ECI) registers occupy two addresses in the ACPI_OS space (Table 13-8).

The OS2EC Data EC Byte 0 Register and ACPI OS COMMAND Register registers appear as a single 8-bit data register in the ACPI_EC. The CMD bit in the OS STATUS OS Register is used by the ACPI_EC to discriminate commands from data written by the ACPI_OS to the ACPI_EC. CMD bit is controlled by hardware: ACPI_OS writes to the OS2EC Data EC Byte 0 Register register clear the CMD bit; ACPI_OS writes to the ACPI OS COMMAND Register set the CMD bit.

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FIGURE 13-2: BLOCK DIAGRAM CORRESPONDING TO THE ACPI SPECIFICATION

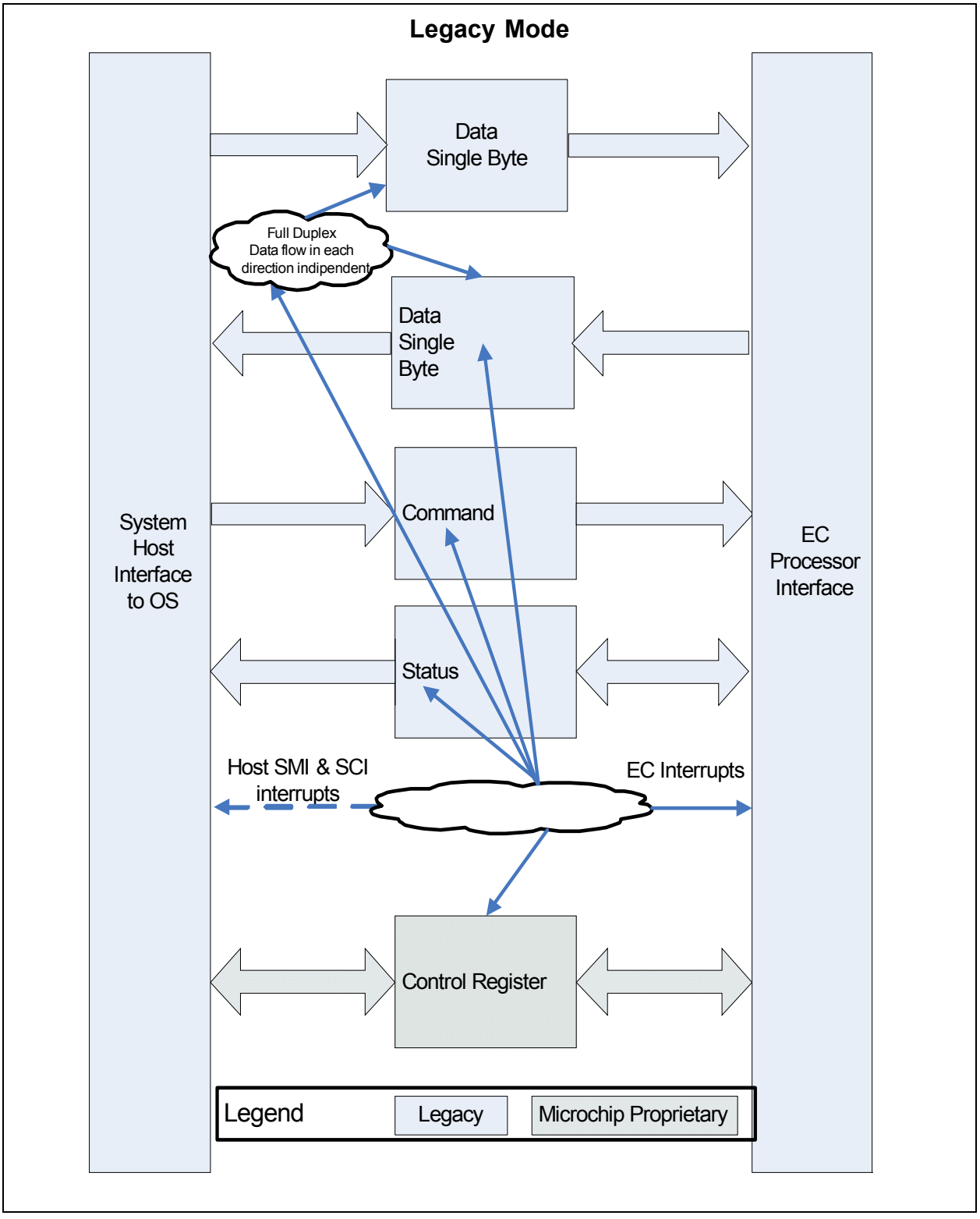
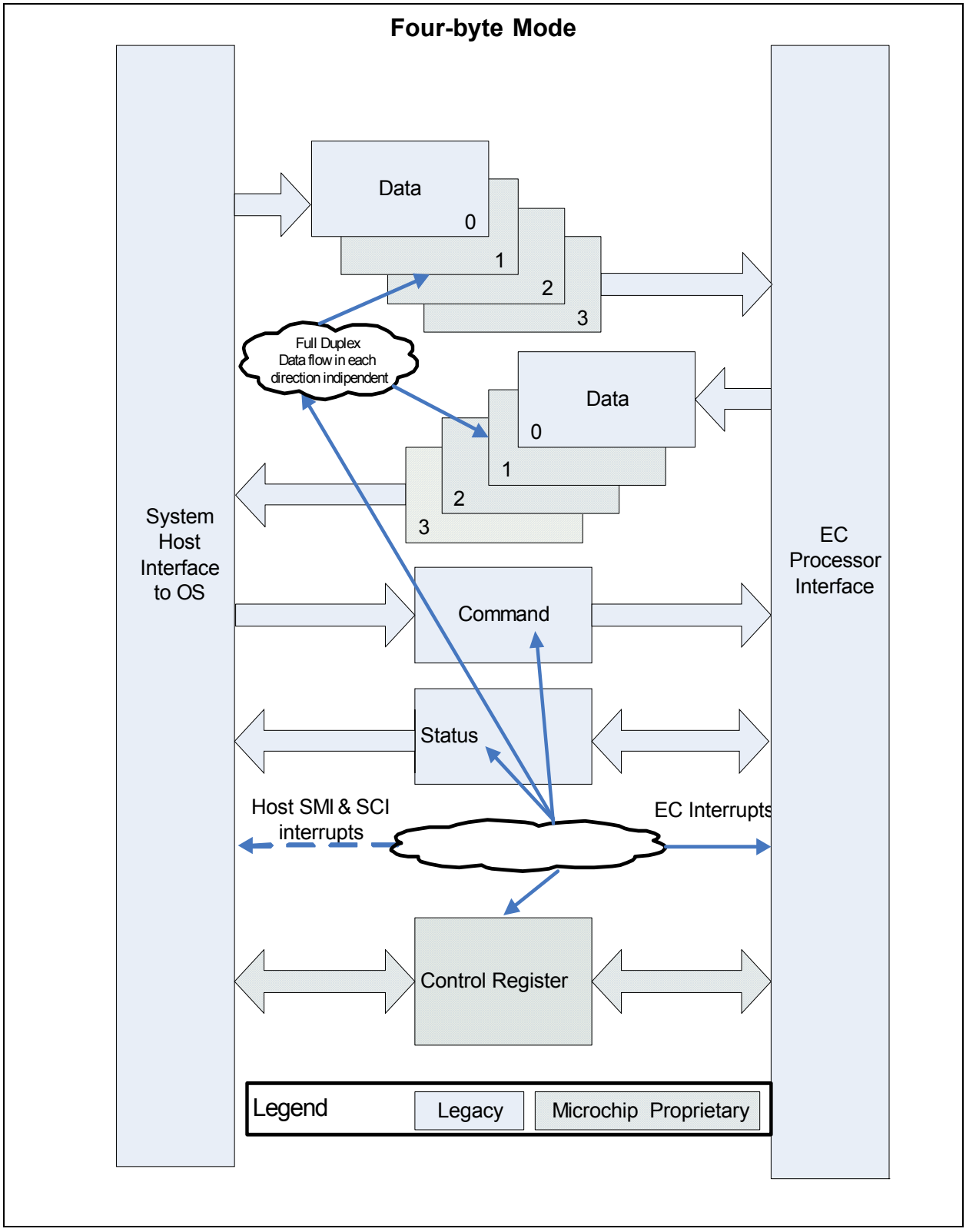


FIGURE 13-2: BLOCK DIAGRAM CORRESPONDING TO THE ACPI SPECIFICATION



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13.11 Register Aliasing between Runtime and EC-Only Registers

Table 13-6, "Runtime Register Aliasing into EC-Only Registers" indicates the aliasing from Runtime registers to EC-Only registers. The “Host/EC Access” column distinguishes the aliasing based on access type. See individual register descriptions for more details.

TABLE 13-6: RUNTIME REGISTER ALIASING INTO EC-ONLY REGISTERS

Host Offset	Runtime Register Register Name	Host Access	EC Offset	Aliased EC-Only Register Register Name	EC Access
00h	ACPI OS Data Register Byte 0 Register	W	108h	OS2EC Data EC Byte 0 Register	R
00h	ACPI OS Data Register Byte 0 Register	R	100h	EC2OS Data EC Byte 0 Register	W
01h	ACPI OS Data Register Byte 1 Register	W	109h	OS2EC Data EC Byte 1 Register	R
01h	ACPI OS Data Register Byte 1 Register	R	101h	EC2OS Data EC Byte 1 Register	W
02h	ACPI OS Data Register Byte 2 Register	W	10Ah	OS2EC Data EC Byte 2 Register	R
02h	ACPI OS Data Register Byte 2 Register	R	102h	EC2OS Data EC Byte 2 Register	W
03h	ACPI OS Data Register Byte 3 Register	W	10Bh	OS2EC Data EC Byte 3 Register	R
03h	ACPI OS Data Register Byte 3 Register	R	103h	EC2OS Data EC Byte 3 Register	W
04h	ACPI OS COMMAND Register	W	108h	OS2EC Data EC Byte 0 Register	R
04h	OS STATUS OS Register	R	104h	EC STATUS Register	W
05h	OS Byte Control Register	R	105h	EC Byte Control Register	R/W
06h	Reserved		106h	Reserved	
07h	Reserved		107h	Reserved	

Table 13-7, "EC-Only Registers Summary" indicates the aliasing from EC-Only to Runtime registers. The “Host/EC Access” column distinguishes the aliasing based on access type. See individual register descriptions for more details.

TABLE 13-7: EC-ONLY REGISTERS SUMMARY

EC Offset	EC-Only Registers Register Name	EC Access	Host Offset	Aliased Runtime Register Register Name	Host Access
108h	OS2EC Data EC Byte 0 Register	R	00h	ACPI OS Data Register Byte 0 Register	W
108h	OS2EC Data EC Byte 0 Register	R	04h	ACPI OS COMMAND Register	W
109h	OS2EC Data EC Byte 1 Register	R	01h	ACPI OS Data Register Byte 1 Register	W
10Ah	OS2EC Data EC Byte 2 Register	R	02h	ACPI OS Data Register Byte 2 Register	W
10Bh	OS2EC Data EC Byte 3 Register	R	03h	ACPI OS Data Register Byte 3 Register	W
104h	EC STATUS Register	W	04h	OS STATUS OS Register	W
105h	EC Byte Control Register	R/W	05h	OS Byte Control Register	R
106h	Reserved	R		Reserved	R
107h	Reserved	R		Reserved	R
100h	EC2OS Data EC Byte 0 Register	W	00h	ACPI OS Data Register Byte 0 Register	R
101h	EC2OS Data EC Byte 1 Register	W	01h	ACPI OS Data Register Byte 1 Register	R
102h	EC2OS Data EC Byte 2 Register	W	02h	ACPI OS Data Register Byte 2 Register	R
103h	EC2OS Data EC Byte 3 Register	W	03h	ACPI OS Data Register Byte 3 Register	R

13.12 Runtime Registers

Note: The Runtime registers may be accessed by the EC but typically the Host will access the Runtime Registers and the EC will access just the EC-Only registers.

The registers listed in the Runtime Register Summary table are for a single instance of the ACPI Embedded Controller Interface (ACPI-ECI). Host access for each register listed in this table is defined as an offset in the Host address space to the Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for each instance of the ACPI Embedded Controller Interface (ACPI-ECI) shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

TABLE 13-8: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	ACPI OS Data Register Byte 0 Register
01h	ACPI OS Data Register Byte 1 Register
02h	ACPI OS Data Register Byte 2 Register
03h	ACPI OS Data Register Byte 3 Register
04h	ACPI OS COMMAND Register

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TABLE 13-8: RUNTIME REGISTER SUMMARY (CONTINUED)

Offset	Register Name
04h	OS STATUS OS Register
05h	OS Byte Control Register
06h	Reserved
07h	Reserved

13.12.1 ACPI OS DATA REGISTER BYTE 0 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_0 This is byte 0 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.12.1.1 ACPI-OS DATA BYTES[3:0]

Writes by the ACPI_OS to the ACPI-OS DATA BYTES[3:0] are aliased to the OS2EC DATA BYTES[3:0]. Reads by the ACPI_OS from the ACPI-OS DATA BYTES[3:0] are aliased to the EC2OS DATA BYTES[3:0].

All access to the ACPI-OS DATA BYTES[3:0] registers should be orderly: Least Significant Byte to Most Significant Byte when byte access is used.

Writes to any of the four ACPI-OS DATA BYTES[3:0] registers clears the CMD bit in the OS STATUS OS Register (the state of the FOUR_BYTE_ACCESS bit in the OS Byte Control Register has no impact.)

When the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is cleared to '0', the following access rules apply:

1. Writes to the ACPI OS Data Register Byte 0 Register sets the IBF bit in the OS STATUS OS Register.
2. Reads from the ACPI OS Data Register Byte 0 Register clears the OBF bit in the OS STATUS OS Register.
3. All writes to ACPI-OS DATA BYTES[3:1] complete without error but the data are not registered.
4. All reads from ACPI-OS DATA BYTES[3:1] return 00h without error.
5. Access to ACPI-OS DATA BYTES[3:1] has no effect on the IBF and OBF bits in the OS STATUS OS Register.

When the Four Byte Access bit in the OS Byte Control Register is set to '1', the following access rules apply:

1. Writes to the ACPI OS Data Register Byte 3 Register sets the IBF bit in the OS STATUS OS Register.
2. Reads from the ACPI OS Data Register Byte 3 Register clears the OBF bit in the OS STATUS OS Register.

13.12.2 ACPI OS DATA REGISTER BYTE 1 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_1 This is byte 1 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.12.3 ACPI OS DATA REGISTER BYTE 2 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_2 This is byte 2 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.12.4 ACPI OS DATA REGISTER BYTE 3 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OS_DATA_BYTE_3 This is byte 3 of the 32-bit ACPI-OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.12.5 ACPI OS COMMAND REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ACPI_OSS_COMMAND Writes to the this register are aliased in the OS2EC Data EC Byte 0 Register. Writes to the this register also set the CMD and IBF bits in the OS STATUS OS Register	W	0h	RESET_SYS

13.12.6 OS STATUS OS REGISTER

This read-only register is aliased to the EC STATUS Register. The EC STATUS Register has read write access.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	UD0B User Defined	R	0b	RESET_SYS

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Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
6	SMI_EVT This bit is set when an SMI event is pending; i.e., the ACPI_EC is requesting an SMI query; This bit is cleared when no SMI events are pending. This bit is an ACPI_EC-maintained software flag that is set when the ACPI_EC has detected an internal event that requires system management interrupt handler attention. The ACPI_EC sets this bit before generating an SMI. **Note:** The usage model from the ACPI specification requires both SMI's and SCI's. The ACPI_OS SMI and SCI interrupts are not implemented in the ACPI Embedded Controller Interface (ACPI-ECI). The SMI_EVT and SCI_EVT bits in the OS STATUS OS Register are software flags and this block do not initiate SMI or SCI events.	R	0b	RESET_SYS
5	SCI_EVT This bit is set by software when an SCI event is pending; i.e., the ACPI_EC is requesting an SCI query; SCI Event flag is clear when no SCI events are pending. This bit is an ACPI_EC-maintained software flag that is set when the embedded controller has detected an internal event that requires operating system attention. The ACPI_EC sets this bit before generating an SCI to the OS. **Note:** The usage model from the ACPI specification requires both SMI's and SCI's. The ACPI_OS SMI and SCI interrupts are not implemented in the ACPI Embedded Controller Interface (ACPI-ECI). The SMI_EVT and SCI_EVT bits in the OS STATUS OS Register are software flags and this block do not initiate SMI or SCI events.	R	0b	RESET_SYS
4	BURST The BURST bit is set when the ACPI_EC is in Burst Mode for polled command processing; the BURST bit is cleared when the ACPI_EC is in Normal mode for interrupt-driven command processing. The BURST bit is an ACPI_EC-maintained software flag that indicates the embedded controller has received the Burst Enable command from the host, has halted normal processing, and is waiting for a series of commands to be sent from the host. Burst Mode allows the OS or system management handler to quickly read and write several bytes of data at a time without the overhead of SCIs between commands. The BURST bit is maintained by ACPI_EC software, only.	R	0b	RESET_SYS

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	CMD This bit is set when the OS2EC Data EC Byte 0 Register contains a command byte written into ACPI OS COMMAND Register; this bit is cleared when the OS2EC DATA BYTES[3:0] contains a data byte written into the ACPI-OS DATA BYTES[3:0]. This bit is hardware controlled: • ACPI_OS writes to any of the four ACPI-OS DATA BYTES[3:0] bytes clears this bit • ACPI_OS writes to the ACPI OS COMMAND Register sets this bit. **Note:** This bit allows the embedded controller to differentiate the start of a command sequence from a data byte write operation.	R	0b	RESET_SYS
2	UD1B User Defined	R	0b	RESET_SYS

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Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	IBF The Input Buffer Full bit is set to indicate that a the ACPI_OS has written a command or data to the ACPI_EC and that data is ready. This bit is automatically cleared when data has been read by the ACPI_EC. **Note:** The setting and clearing of this IBF varies depending on the setting of the following bits: CMD bit in this register and FOUR_BYTE_ACCESS bit in the OS Byte Control Register. Three scenarios follow: 1. The IBF is set when the ACPI_OS writes to the ACPI OS COMMAND Register. This same write autonomously sets the CMD bit in this register. The IBF is cleared if the CMD bit in this register is set and the ACPI_EC reads from the OS2EC Data EC Byte 0 Register. **Note:** When CMD bit in this register is set the FOUR_BYTE_ACCESS bit in the OS Byte Control Register has no impact on the IBF bit behavior. 2. A write by the to the ACPI_OS to the ACPI OS Data Register Byte 0 Register sets the IBF bit if the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is in the cleared to '0' state prior to this write. This same write autonomously clears the CMD bit in this register. A read of the OS2EC Data EC Byte 0 Register clears the IBF bit if the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is in the cleared to '0' state prior to this read. 3. A write by the to the ACPI_OS to the ACPI OS Data Register Byte 3 Register sets the IBF bit if the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is in the set to '1' state prior to this write. This same write autonomously clears the CMD bit in this register. A read of the OS2EC Data EC Byte 3 Register clears the IBF bit if the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is in the set to '1' state prior to this read. An IBF interrupt signals the ACPI_EC that there is data available. The ACPI Specification usage model is as follows: 1. The ACPI_EC reads the EC STATUS Register and sees the IBF flag set, 2. The ACPI_EC reads all the data available in the OS2EC DATA BYTES[3:0]. This causes the IBF bit to be automatically cleared by hardware. 3. The ACPI_EC must then generate a software interrupt to alert the ACPI_OS that the data has been read and that the host is free to write more data to the ACPI_EC as needed.	R	0h	RESET_SYS

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	OBF The Output Buffer Full bit is set to indicate that a the ACPI_EC has written a data to the ACPI_OS and that data is ready. This bit is automatically cleared when all the data has been read by the ACPI_OS. **Note:** The setting and clearing of this OBF varies depending on the setting FOUR_BYTE_ACCESS bit in the OS Byte Control Register. Two scenarios follow: 1. The OBF bit is set if the Four Byte Access bit in the OS Byte Control Register is '0' when the ACPI_EC writes to the EC2OS Data EC Byte 0 Register. The OBF is cleared if the Four Byte Access bit in the OS Byte Control Register is cleared to '0' when the ACPI_OS reads from the ACPI OS Data Register Byte 0 Register. 2. The OBF is set if the Four Byte Access bit in the OS Byte Control Register is set to '1' when the ACPI_EC writes to the EC2OS Data EC Byte 3 Register. The OBF is cleared if the Four Byte Access bit in the OS Byte Control Register is set to '1' when the ACPI_OS reads from the ACPI OS Data Register Byte 3 Register. The ACPI Specification usage model is as follows: 1. The ACPI_EC must generate a software interrupt (See the note in Section 13.8, "Interrupts") to alert the ACPI_OS that the data is available. 2. The ACPI_OS reads the OS STATUS OS Register and sees the OBF flag set, the ACPI_OS reads all the data available in the ACPI-OS DATA BYTES[3:0]. 3. The ACPI_OS reads all the data available in the ACPI-OS DATA BYTES[3:0]. This causes the OBF bit to be automatically cleared by hardware and the associated OBE interrupt to be asserted.	R	0h	RESET_SYS

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13.12.7 OS BYTE CONTROL REGISTER

This register is aliased to the EC Byte Control Register. No behavioral differences occur due to address aliasing.

Offset	05			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	FOUR_BYTE_ACCESS When this bit is set to '1', the ACPI Embedded Controller Interface (ACPI-ECI) accesses four bytes through the ACPI-OS DATA BYTES[3:0]. When this bit is cleared to '0', the ACPI Embedded Controller Interface (ACPI-ECI) accesses one byte through the ACPI OS Data Register Byte 0 Register. The corresponds to Legacy Mode described in Section 13.10, "Description". This bit effects the behavior of the IBF and OBF bits in the OS STATUS OS Register. See also Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed description of access rules.	R	0b	RESET_SYS

Note: The ACPI_OS access Base Address Register (BAR) should be configured to match the access width selected by the Four Byte Access bit in the OS Byte Control Register. This BAR in not described in this chapter.

13.13 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the ACPI Embedded Controller Interface (ACPI-ECI) Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 13-9: REGISTER SUMMARY

Offset	Register Name
100h	EC2OS Data EC Byte 0 Register
101h	EC2OS Data EC Byte 1 Register
102h	EC2OS Data EC Byte 2 Register
103h	EC2OS Data EC Byte 3 Register
104h	EC STATUS Register
105h	EC Byte Control Register
106h	Reserved
107h	Reserved
108h	OS2EC Data EC Byte 0 Register
109h	OS2EC Data EC Byte 1 Register
10Ah	OS2EC Data EC Byte 2 Register
10Bh	OS2EC Data EC Byte 3 Register

13.13.1 OS2EC DATA EC BYTE 0 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	OS_TO_EC_DATA_BYTE_0 This is byte 0 of the 32-bit OS2EC DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.1.1 OS2EC DATA BYTES[3:0]

When the CMD bit in the OS STATUS OS Register is cleared to '0', reads by the ACPI_EC from the OS2EC DATA BYTES[3:0] are aliased to the ACPI-OS DATA BYTES[3:0].

All access to the OS2EC DATA BYTES[3:0] registers should be orderly: Least Significant Byte to Most Significant Byte when byte access is used.

When the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is cleared to '0', the following access rules apply:

1. Writes to the OS2EC DATA BYTES[3:0] have no effect on the OBF bit in the OS STATUS OS Register.
2. Reads from the OS2EC Data EC Byte 0 Register clears the IBF bit in the OS STATUS OS Register.
3. All reads from OS2EC DATA BYTES[3:1] return 00h without error.
4. Access to OS2EC DATA BYTES[3:1 has no effect on the IBF and OBF bits in the OS STATUS OS Register.

When the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is set to '1', the following access rules apply:

1. Writes to the OS2EC DATA BYTES[3:0] have no effect on the OBF bit in the OS STATUS OS Register.
2. Reads from the OS2EC Data EC Byte 3 Register clears the IBF bit in the OS STATUS OS Register.

13.13.2 OS2EC DATA EC BYTE 1 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	109h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	OS2EC_DATA_ BYTE_1 This is byte 1 of the 32-bit OS2EC DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.3 OS2EC DATA EC BYTE 2 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

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Offset	10Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	OS2EC_DATA_BYTE_2 This is byte 2 of the 32-bit OS2EC DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.4 OS2EC DATA EC BYTE 3 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	10Bh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	OS2EC_DATA_BYTE_3 This is byte 3 of the 32-bit OS2EC DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.5 EC2OS DATA EC BYTE 0 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	100h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC2OS_DATA_BYTE_0 This is byte 0 of the 32-bit EC2OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.5.1 EC2OS DATA BYTES[3:0]

Writes by the ACPI_EC to the EC2OS DATA BYTES[3:0] are aliased to the ACPI-OS DATA BYTES[3:0]

All access to the EC2OS DATA BYTES[3:0] registers should be orderly: Least Significant Byte to Most Significant Byte when byte access is used.

When the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is cleared to ‘0’, the following access rules apply:

1. Writes to the EC2OS Data EC Byte 0 Register set the OBF bit in the OS STATUS OS Register.
2. Reads from the EC2OS DATA BYTES[3:0] have no effect on the IBF bit in the OS STATUS OS Register.
3. All reads from EC2OS DATA BYTES[3:1] return 00h without error.
4. All writes to EC2OS DATA BYTES[3:1] complete without error but the data are not registered.
5. Access to EC2OS DATA BYTES[3:1] have no effect on the IBF and OBF bits in the OS STATUS OS Register.

When the FOUR_BYTE_ACCESS bit in the OS Byte Control Register is set to ‘1’, the following access rules apply:

1. Writes to the EC2OS Data EC Byte 3 Register set the OBF bit in the OS STATUS OS Register.
2. Reads from the EC2OS DATA BYTES[3:0] have no effect on the IBF bit in the OS STATUS OS Register.

13.13.6 EC2OS DATA EC BYTE 1 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	101h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC2OS_DATA_BYTE_1 This is byte 1 of the 32-bit EC2OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.7 EC2OS DATA EC BYTE 2 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	102h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC2OS_DATA_BYTE_2 This is byte 2 of the 32-bit EC2OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

13.13.8 EC2OS DATA EC BYTE 3 REGISTER

This register is aliased; see Section 13.12.1.1, "ACPI-OS DATA BYTES[3:0]", Section 13.13.1.1, "OS2EC DATA BYTES[3:0]", and Section 13.13.5.1, "EC2OS DATA BYTES[3:0]" for detailed descriptions of access rules.

Offset	103h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC2OS_DATA_BYTE_3 This is byte 3 of the 32-bit EC2OS DATA BYTES[3:0].	R/W	0h	RESET_SYS

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13.13.9 EC STATUS REGISTER

This register is aliased to the OS STATUS OS Register. The OS STATUS OS Register is a read only version of this register.

Offset	104h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	UD0A User Defined	R/W	0b	RESET_SYS
6	SMI_EVT See the SMI_EVT bit in the OS STATUS OS Register for the bit description.	R/W	0b	RESET_SYS
5	SCI_EVT See the SMI_EVT bit in the OS STATUS OS Register for the bit description.	R/W	0b	RESET_SYS
4	BURST See the BURST bit in the OS STATUS OS Register for the bit description.	R/W	0b	RESET_SYS
3	CMD See the CMD bit in the OS STATUS OS Register for the bit description.	R	0b	RESET_SYS
2	UD1A User Defined	R/W	0b	RESET_SYS
1	IBF See the IBF bit in the OS STATUS OS Register for the bit description.	R	0h	RESET_SYS
0	OBF See the OBF bit in the OS STATUS OS Register for the bit description.	R	0h	RESET_SYS

Note: The IBF and OBF bits are not de-asserted by hardware when the host is powered off, or the LPC interface powers down; for example, following system state changes S3->S0, S5->S0, G3-> S0. For further information on how these bits are cleared, refer to IBF and OBF bit descriptions in the STATUS OS-Register definition.

13.13.10 EC BYTE CONTROL REGISTER

This register is aliased to the OS Byte Control Register. The OS Byte Control Register is a read only version of this register.

Offset	105h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	FOUR_BYTE_ACCESS See the FOUR_BYTE_ACCESS bit in the OS Byte Control Register for the bit description.	R/W	0b	RESET_SYS

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14.0 ACPI PM1 BLOCK

14.1 Introduction

The MEC170x supports ACPI as described in this section. These features comply with the ACPI Specification through a combination of hardware and EC software.

14.2 References

ACPI Specification, Revision 1.0

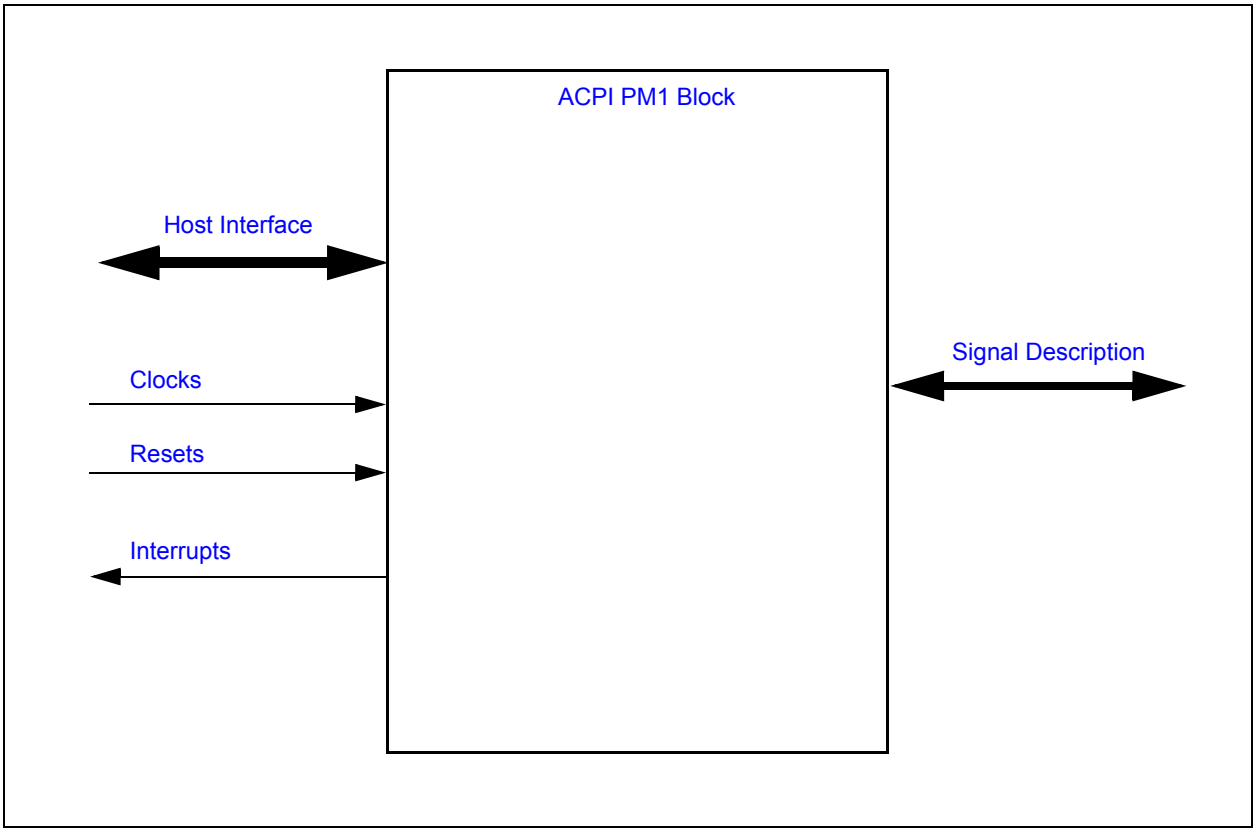
14.3 Terminology

None

14.4 Interface

This block is an IP block designed to be incorporated into a chip. It is designed to be accessed externally via the pin interface and internally via a registered host interface. The following diagram illustrates the various interfaces to the block.

FIGURE 14-1: I/O DIAGRAM OF BLOCK



14.5 Signal Description

Table 14-1, "ACPI PM1 Signal Description Table" lists the signals that are typically routed to the pin interface.

TABLE 14-1: ACPI PM1 SIGNAL DESCRIPTION TABLE

Name	Direction	Description
EC_SCI#	Output	Any or all of the PWRBTN_STS, SLPBTN_STS, and RTC_STS bits in the Power Management 1 Status 2 Register can assert the EC_SCI# pin if enabled by the associated bits in the Power Management 1 Enable 2 Register register. The EC_SCI_STS bit in the EC_PM_STS Register register can also be used to generate an SCI on the EC_SCI# pin.

14.6 Host Interface

The registers defined for the ACPI PM1 Block are accessible by the various hosts as indicated in Section 14.11, "Runtime Registers".

14.7 Power, Clocks and Resets

This section defines the Power, Clock, and Reset parameters of the block.

14.7.1 POWER DOMAINS

TABLE 14-2: POWER SOURCES

Name	Description
VTR	This power well sources the registers and logic in this block.

14.7.2 CLOCKS

This section describes all the clocks in the block, including those that are derived from the I/O Interface as well as the ones that are derived or generated internally.

TABLE 14-3: CLOCKS

Name	Description
48MHz	This clock signal drives selected logic (e.g., counters).

14.7.3 RESETS

TABLE 14-4: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in this block.

14.8 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 14-5: EC INTERRUPTS

Source	Description
ACPIPM1_CTL	This Interrupt is generated to the EC by the Host writing to the Power Management 1 Control 2 Register register
ACPIPM1_EN	This Interrupt is generated to the EC by the Host writing to the Power Management 1 Enable 2 Register register
ACPIPM1_STS	This Interrupt is generated to the EC by the Host writing to the Power Management 1 Status 2 Register register

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14.9 Low Power Modes

The ACPI PM1 Block may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

14.10 Description

This section describes the functions of the ACPI PM1 Block in more detail.

The MEC170x implements the ACPI fixed registers but includes only those bits that apply to the power button sleep button and RTC alarm events. The ACPI WAK_STS, SLP_TYP, and SLP_EN bits are also supported.

The MEC170x can generate SCI Interrupts to the Host. The functions described in the following sub-sections can generate a SCI event on the EC_SCI# pin. In the MEC170x, an SCI event is considered the same as an ACPI wakeup or runtime event.

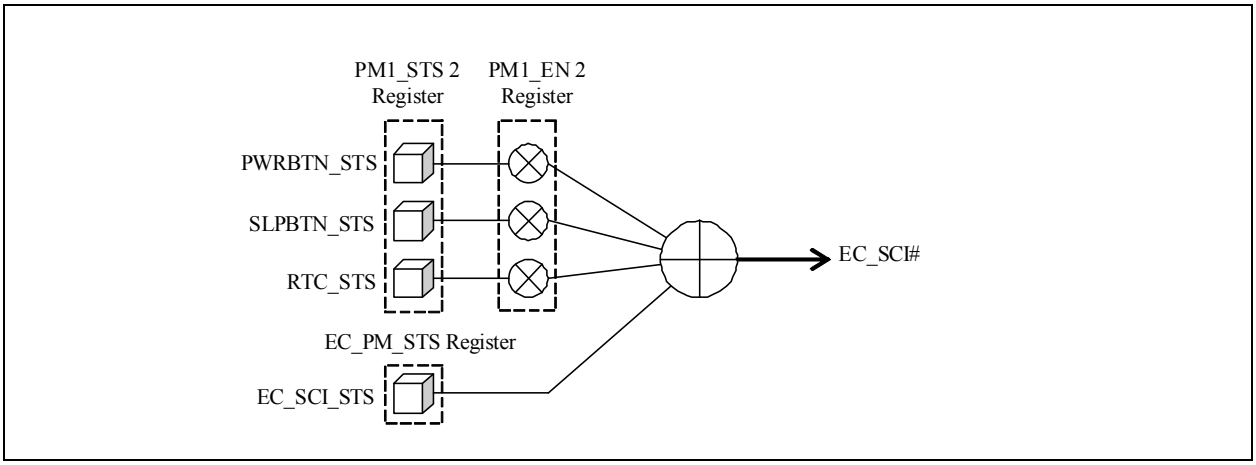
14.10.1 SCI EVENT-GENERATING FUNCTIONS

Event	Event Bit	Definition
Power Button with Override	PWRBTN_STS	The power button has a status and an enable bit in the PM1_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writable by the EC; the enable bit is Read-only by the EC. It also has a status and enable bit in the PM1_BLK of registers to indicate and control the power button override (fail-safe) event. These bits are not required by ACPI. The PWRBTN_STS bit is set by the Host to enable the generation of an SCI due to the power button event. The status bit is set by the EC when it generates a power button event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the EC generates an SCI power management event.
	PWRBTNOR_STS	The power button has a status and an enable bit in the PM1_BLK of registers to provide an SCI upon the power button override.The power button override event status bit is software Read/Writable by the EC; the enable bit is software read-only by the EC.The enable bit for the override event is located at bit 1 in the Power Management 1 Control Register 2 (PM1_CNTRL 2).The power button bit has a status and enable bit in the Runtime Registers to provide an SCI power management event on a button press The PWRBTNOR_STS bit is set by the Host to enable the generation of an SCI due to the power button override event. The status bit is set by the EC when it generates a power button event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the EC generates an SCI power management event.
Sleep Button	SLPBTN_STS	The sleep button that has a status and an enable bit in the Runtime Registers to provide an SCI power management event on a button press. The status bit is software Read/Writable by the EC; the enable bit is Read-only by the EC. The SLPBTN_STS bit is set by the Host to enable the generation of an SCI due to the sleep button event. The status bit is set by the EC when it generates a sleep button event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the EC will generate an SCI power management event.

Event	Event Bit	Definition
RTC Alarm	RTC_STS	The ACPI specification requires that the RTC alarm generate a hardware wake-up event from the sleeping state. The RTC alarm can be enabled as an SCI event and its status can be determined through bits in the Runtime Registers. The status bit is software Read/Writable by the EC; the enable bit is Read-only by the EC. The RTC_STS bit is set by the Host to enable the generation of an SCI due to the RTC alarm event. The status bit is set by the EC when the RTC generates an alarm event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the EC. If the enable bit is set, the EC will generate an SCI power management event.

Figure 14-2 describes the relationship of PM1 Status and Enable bits to the EC_SCI# pin.

FIGURE 14-2: EC_SCI# INTERFACE



14.11 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the ACPI PM1 Block. Host access for each register listed in this table is defined as an offset in the Host address space to the Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for the ACPI PM1 Block shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

TABLE 14-6: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	Power Management 1 Status 1 Register
01h	Power Management 1 Status 2 Register
02h	Power Management 1 Enable 1 Register
03h	Power Management 1 Enable 2 Register
04h	Power Management 1 Control 1 Register
05h	Power Management 1 Control 2 Register
06h	Power Management 2 Control 1 Register
07h	Power Management 2 Control 2 Register

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14.11.1 POWER MANAGEMENT 1 STATUS 1 REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	-	-

14.11.2 POWER MANAGEMENT 1 STATUS 2 REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	WAK_STS This bit can be set or cleared by the EC. The Host writing a one to this bit can also clear this bit.	R/WC (Note 1)	00h	RESET_SYS
6:4	Reserved	R	-	-
3	PWRBTNOR_STS This bit can be set or cleared by the EC to simulate a Power button override event status if the power is controlled by the EC. The Host writing a one to this bit can also clear this bit. The EC must generate the associated hardware event under software control.	R/WC (Note 1)	00h	RESET_SYS
2	RTC_STS This bit can be set or cleared by the EC to simulate a RTC status. The Host writing a one to this bit can also clear this bit. The EC must generate the associated SCI interrupt under software control.	R/WC (Note 1)	00h	RESET_SYS
1	SLPBTN_STS This bit can be set or cleared by the EC to simulate a Sleep button status if the sleep state is controlled by the EC. The Host writing a one to this bit can also clear this bit. The EC must generate the associated SCI interrupt under software control.	R/WC (Note 1)	00h	RESET_SYS
0	PWRBTN_STS This bit can be set or cleared by the EC to simulate a Power button status if the power is controlled by the EC. The Host writing a one to this bit can also clear this bit. The EC must generate the associated SCI interrupt under software control.	R/WC (Note 1)	00h	RESET_SYS
Note 1:	These bits are set/cleared by the EC directly i.e., writing '1' sets the bit and writing '0' clears it. These bits can also be cleared by the Host software writing a one to this bit position and by RESET_SYS. Writing a 0 by the Host has no effect.			

14.11.3 POWER MANAGEMENT 1 ENABLE 1 REGISTER

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	-	-

14.11.4 POWER MANAGEMENT 1 ENABLE 2 REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:3	Reserved	R	-	-
2	RTC_EN This bit can be read or written by the Host. It can be read by the EC.	R/W (Note 1)	00h	RESET_SYS
1	SLPBTN_EN This bit can be read or written by the Host. It can be read by the EC.	R/W (Note 1)	00h	RESET_SYS
0	PWRBTN_EN This bit can be read or written by the Host. It can be read by the EC.	R/W (Note 1)	00h	RESET_SYS
Note 1: These bits are read-only by the EC.				

14.11.5 POWER MANAGEMENT 1 CONTROL 1 REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	0h	RESET_SYS

14.11.6 POWER MANAGEMENT 1 CONTROL 2 REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	Reserved	R	-	-
5	SLP_EN See Table 14-7.	See Table 14-7.	00h	RESET_SYS
4:2	SLP_TYP These bits can be set or cleared by the Host, read by the EC.	R/W (Note 1)	00h	RESET_SYS
1	PWRBTNOR_EN This bit can be set or cleared by the Host, read by the EC.	R/W (Note 1)	00h	RESET_SYS
0	Reserved	R	-	-
Note 1: These bits are read-only by the EC.				

TABLE 14-7: SLP_EN DEFINITION

Host / EC	R/W	Description
Host	Read	Always reads 0
	Write	Writing a 0 has no effect, Writing a 1 sets this bit
EC	Read	Reads the value of the bit
	Write	Writing a 0 has no effect, Writing a 1 clears this bit

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14.11.7 POWER MANAGEMENT 2 CONTROL 1 REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	-	-

14.11.8 POWER MANAGEMENT 2 CONTROL 2 REGISTER

Offset	07h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Reserved	R	-	-

14.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the ACPI PM1 Block Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 14-8: REGISTER SUMMARY

Offset	Register Name
100h	Power Management 1 Status 1 Register
101h	Power Management 1 Status 2 Register
102h	Power Management 1 Enable 1 Register
103h	Power Management 1 Enable 2 Register
104h	Power Management 1 Control 1 Register
105h	Power Management 1 Control 2 Register
106h	Power Management 2 Control 1 Register
107h	Power Management 2 Control 2 Register
110h	EC_PM_STS Register

Note: The Power Management Status, Enable and Control registers in Table 14-8, "Register Summary" are described in Section 14.11, "Runtime Registers".

14.12.1 EC_PM_STS REGISTER

Offset	110h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	UD	R/W	00h	RESET_SYS
0	EC_SCI_STS If the EC_SCI_STS bit is “1”, an interrupt is generated on the EC_SCI# pin.	R/W	00h	RESET_SYS

Note: This register is only accessed by the EC. There is no host access to this register.

15.0 EMBEDDED MEMORY INTERFACE (EMI)

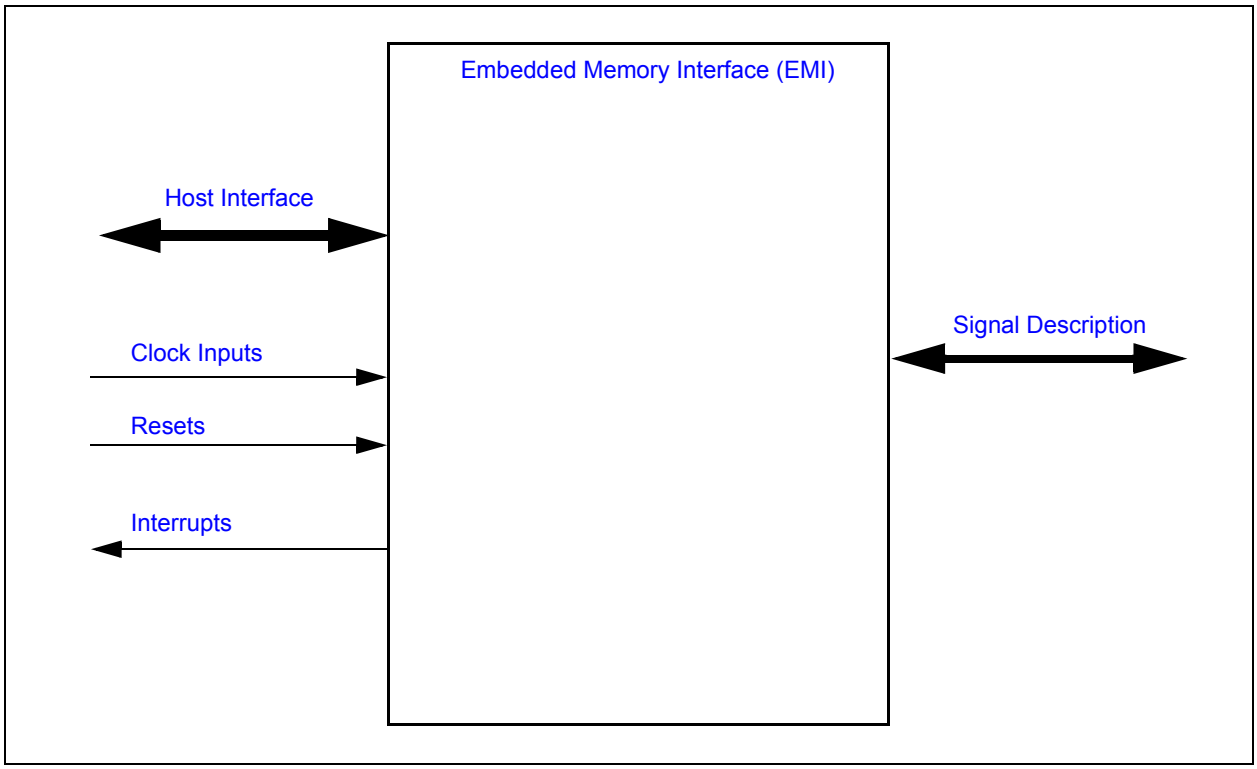
15.1 Introduction

The Embedded Memory Interface (EMI) provides a standard run-time mechanism for the system host to communicate with the Embedded Controller (EC) and other logical components. The Embedded Memory Interface includes 13 byte-addressable registers in the Host's address space, as well as 22 bytes of registers that are accessible only by the EC. The Embedded Memory Interface can be used by the Host to access bytes of memory designated by the EC without requiring any assistance from the EC. The EC may configure these regions of memory as read-only, write-only, or read/write capable.

15.2 Interface

This block is designed to be accessed externally and internally via a register interface.

FIGURE 15-1: I/O DIAGRAM OF BLOCK



15.3 Signal Description

Name	Name	Description
nEM_INT	OUTPUT	Active-low signal asserted when either the EC-to-Host or the Host_SWI_Event is asserted. This signal can be routed to nSMI and nPME inputs in the system as required.

15.4 Host Interface

The registers defined for the Embedded Memory Interface (EMI) are accessible by the System Host and the Embedded Controller (EC) as indicated in Section 15.10, "EC Registers" and Section 15.9, "Runtime Registers".

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15.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

15.5.1 POWER DOMAINS

TABLE 15-1: POWER SOURCES

Name	Description
VTR	The logic and registers implemented in this block reside on this single power well.

15.5.2 CLOCK INPUTS

This block has no special clocking requirements. Host register accesses are synchronized to the host bus clock and EC register accesses are synchronized to the EC bus clock, thereby allowing the transactions to complete in one bus clock.

15.5.3 RESETS

TABLE 15-2: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal resets all the logic and register in this block.

15.6 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 15-3: SYSTEM INTERRUPTS

Source	Description
Host_SWI_Event	This interrupt source for the SERIRQ logic is generated when any of the EC_SWI bits are asserted and the corresponding EC_SWI_EN bits are asserted as well. This event is also asserted if the embedded controller (EC) writes the EC-to-HOST Mailbox Register.
EC-to-Host	This interrupt source for the SERIRQ logic is generated by the embedded controller (EC) writing the EC-to-HOST Mailbox Register.

TABLE 15-4: EC INTERRUPTS

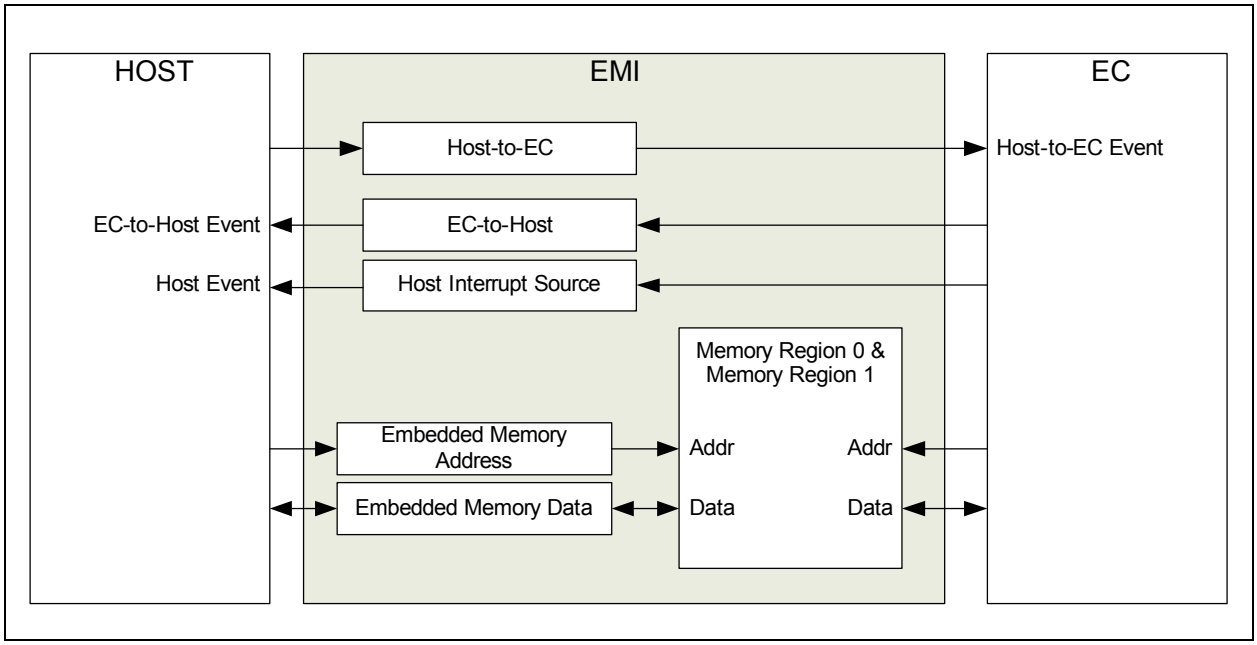
Source	Description
Host-to-EC	Interrupt source for the Interrupt Aggregator, generated by the host writing the HOST-to-EC Mailbox Register.

15.7 Low Power Modes

The Embedded Memory Interface (EMI) automatically enters low power mode when no transaction target it.

15.8 Description

FIGURE 15-2: EMBEDDED MEMORY INTERFACE BLOCK DIAGRAM



The Embedded Memory Interface (EMI) is composed of a mailbox, a direct memory interface, and an Application ID register.

The mailbox contains two registers, the HOST-to-EC Mailbox Register and the EC-to-HOST Mailbox Register, that act as a communication portal between the system host and the embedded controller. When the HOST-to-EC Mailbox Register is written an interrupt is generated to the embedded controller. Similarly, when the EC-to-HOST Mailbox Register is written an interrupt is generated to the system host. The source of the system host interrupt may be read in the Interrupt Source Register. These interrupt events may be individually prevented from generating a Host Event via the Interrupt Mask Register.

The direct memory interface, which is composed of a byte addressable 16-bit EC Address Register and a 32-bit EC Data Register, permits the Host to read or write a portion of the EC's internal address space. The embedded controller may enable up to two regions of the EC's internal address space to be exposed to the system host. The system host may access these memory locations without intervention or assistance from the EC.

The Embedded Memory Interface can be configured so that data transfers between the Embedded Memory Interface data bytes and the 32- bit internal address space may be multiple bytes, while Host I/O is always executed a byte at a time.

When the Host reads one of the four bytes in the Embedded Memory Interface data register, data from the internal 32-bit address space, at the address defined by the Embedded Memory Interface address register, is returned to the Host. This read access will load 1, 2, or 4 bytes into the Data register depending on the configuration of the ACCESS_TYPE bits. Similarly, writing one of the four bytes in the data register will write the corresponding byte(s) from the data register into the internal 32-bit address space as indicated by the ACCESS_TYPE bits. This configuration option is done to ensure that data the EC treats as 16-bit or 32-bit will be consistent in the Host, even though one byte of the data may change between two or more 8-bit accesses by the Host.

In addition, there is an auto-increment function for the Embedded Memory Interface address register. When enabled, the Host can read or write blocks of memory in the 32- bit internal address space by repeatedly accessing the Embedded Memory Interface data register, without requiring Host updates to the Embedded Memory Interface address register.

Finally, the Application ID Register may be used by the host to provide an arbitration mechanism if more than one software thread requires access through the EMI interface. See Section 15.8.4, "Embedded Memory Interface Usage" for more details.

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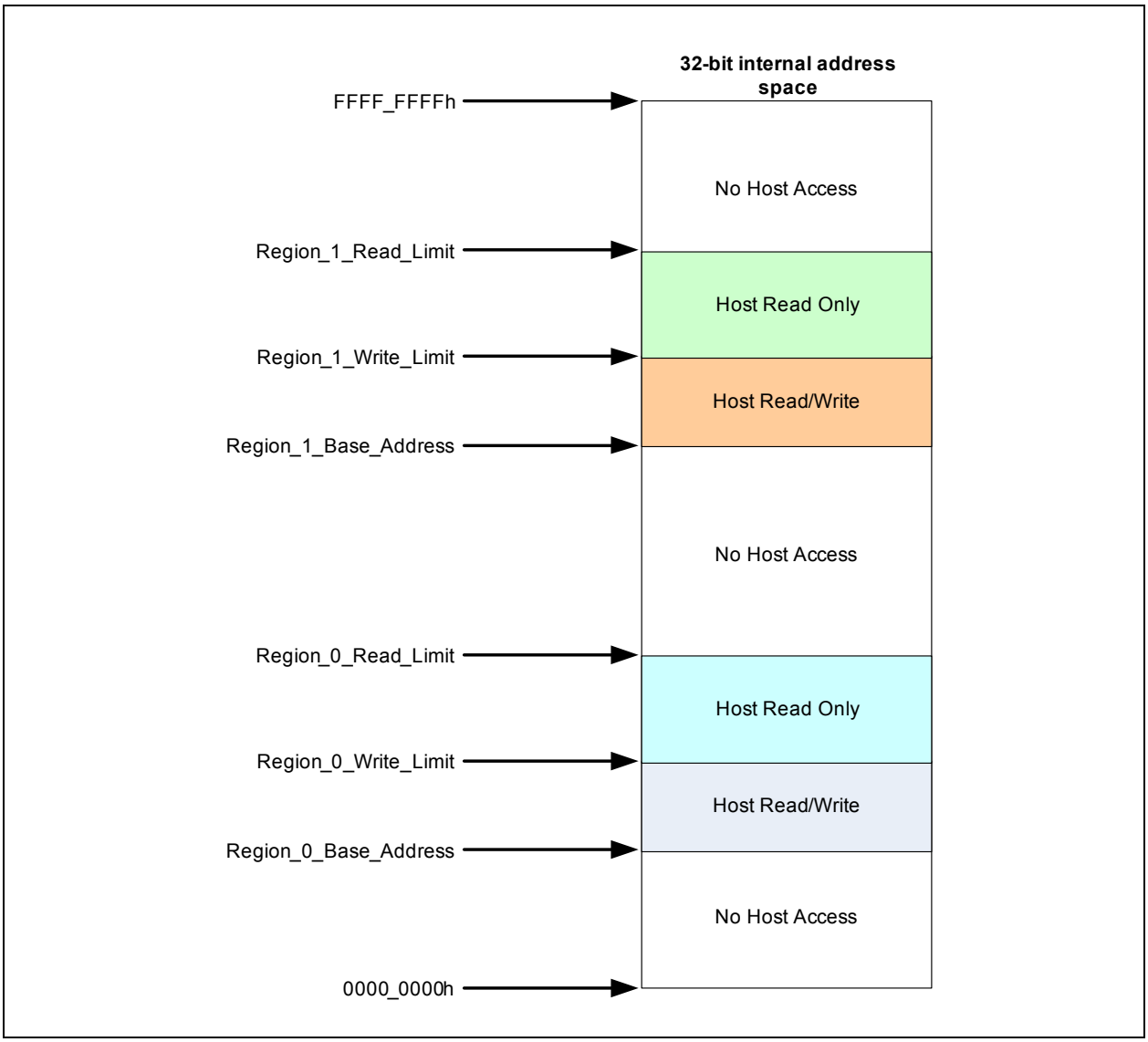
15.8.1 EMBEDDED MEMORY MAP

Each Embedded Memory interface provides direct access for the Host into two windows in the EC 32-bit internal address space. This mapping is shown in Figure 15-3, "Embedded Memory Addressing":

FIGURE 15-3: EMBEDDED MEMORY ADDRESSING



The Base addresses, the Read limits and the Write limits are defined by registers that are in the EC address space and cannot be accessed by the Host. In each region, the Read limit need not be greater than the Write limit. The regions can be contiguous or overlapping. For example, if the Region 0 Read limit is set to 0 and the Write limit is set to a positive number, then the Embedded Memory interface defines a region in the EC memory that the EC can read and write but is write-only for the host. This might be useful for storage of security data, which the Host might wish to send to the EC but should not be readable in the event a virus invades the Host.

Each window into the EC memory can be as large as 32k bytes in the 32-bit internal address space.

15.8.2 EC DATA REGISTER

The 4 1-byte EC Data Byte registers function as a 32-bit register, which creates a 4 byte window into the Memory REGION being accessed. The 4-byte window is always aligned on a 4-byte boundary. Depending on the read/write configuration of the memory region being accessed, the bytes may be extracted from or loaded into memory as a byte, word, or a DWord. The ACCESS_TYPE determines the size of the memory access. The address accessed is determined by the two EC_Address byte registers, which together function as a 15-bit EC Address Register.

- A write to the EC Data Register when the EC Address is in a read-only or a no-access region, as defined by the Memory Base and Limit registers, will update the EC Data Register but memory will not be modified.
- A read to the EC Data Register when the EC Address is in a no-access region, as defined by the Memory Base and Limit registers, will not trigger a memory read and will not modify the EC Data Register. In auto-increment mode (ACCESS_TYPE=11b), reads of Byte 3 of the EC Data Register will still trigger increments of the EC Address Register when the address is out of bounds, while writes of Byte 3 will not.

15.8.3 ACCESS TYPES

The access type field (ACCESS_TYPE in the EC Address LSB Register) defines the type of host access that occurs when the EC Data Register is read or written.

11: Auto-increment 32-bit access. This defines a 32-bit access, as in the 10 case. In addition, any read or write of Byte 3 in the EC Data Register causes the EC Data Register to be incremented by 1. That is, the EC_Address field will point to the next 32-bit double word in the 32- bit internal address space.

10: 32-bit access. A read of Byte 0 in the EC Data Register causes the 32 bits in the 32- bit internal address space at an offset of EC_Address to be loaded into the entire EC Data Register. The read then returns the contents of Byte 0. A read of Byte 1, Byte 2 or Byte 3 in the EC Data Register returns the contents of the register, without any update from the 32- bit internal address space.

A write of Byte 3 in the EC Data Register causes the EC Data Register to be written into the 32 bits in the 32- bit internal address space at an offset of EC_Address. A write of Byte 0, Byte 1 or Byte 2 in the EC Data Register updates the contents of the register, without any change to the 32- bit internal address space.

01: 16-bit access. A read of Byte 0 in the EC Data Register causes the 16 bits in the 32- bit internal address space at an offset of EC_Address to be loaded into Byte 0 and Byte 1 of the EC Data Register. The read then returns the contents of Byte 0. A read of Byte 2 in the EC Data Register causes the 16 bits in the 32- bit internal address space at an offset of EC_Address+2 to be loaded into Byte 2 and Byte 3 of the EC Data Register. The read then returns the contents of Byte 2. A read of Byte 1 or Byte 3 in the EC Data Register return the contents of the register, without any update from the 32- bit internal address space.

A write of Byte 1 in the EC Data Register causes Bytes 1 and 0 of the EC Data Register to be written into the 16 bits in the 32- bit internal address space at an offset of EC_Address. A write of Byte 3 in the EC Data Register causes Bytes 3 and 2 of the EC Data Register to be written into the 16 bits in the 32- bit internal address space at an offset of EC_Address+2. A write of Byte 0 or Byte 2 in the EC Data Register updates the contents of the register, without any change to the 32- bit internal address space.

00: 8-bit access. Any byte read of Byte 0 through Byte 3 in the EC Data Register causes the corresponding byte within the 32-bit double word addressed by EC_Address to be loaded into the byte of EC Data Register and returned by the read. Any byte write to Byte 0 through Byte 3 in the EC Data Register writes the corresponding byte within the 32-bit double word addressed by EC_Address, as well as the byte of the EC Data Register.

15.8.4 EMBEDDED MEMORY INTERFACE USAGE

The Embedded Memory Interface provides a generic facility for communication between the Host and the EC and can be used for many functions. Some examples are:

- Virtual registers. A block of memory in the 32-bit internal address space can be used to implement a set of virtual registers. The Host is given direct read-only access to this address space, referred to as peek mode. The EC may read or write this memory as needed.
- Program downloading. Because the Instruction Closely Coupled Memory is implemented in the same 32-bit internal address space, the Embedded Memory Interface can be used by the Host to download new program segments for the EC in the upper 32KB SRAM. The Read/Write window would be configured by the Host to point to the beginning of the loadable program region, which could then be loaded by the Host.
- Data exchange. The Read/Write portion of the memory window can be used to contain a communication packet. The Host, by default, “owns” the packet, and can write it at any time. When the Host wishes to communicate with the EC, it sends the EC a command, through the Host-to-EC message facility, to read the packet and perform

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some operations as a result. When it is completed processing the packet, the EC can inform the Host, either through a message in the EC-to-Host channel or by triggering an event such as an SMI directly. If return results are required, the EC can write the results into the Read/Write region, which the Host can read directly when it is informed that the EC has completed processing. Depending on the command, the operations could entail update of virtual registers in the 32-bit internal address space, reads of any register in the EC address space, or writes of any register in the EC address space. Because there are two regions that are defined by the base registers, the memory used for the communication packet does not have to be contiguous with a set of virtual registers.

Because there are two Embedded Memory Interface memory regions, the Embedded Memory Interface cannot be used for more than two of these functions at a time. The Host can request that the EC switch from one function to another through the use of the Host-to-EC mailbox register.

The Application ID Register is provided to help software applications track ownership of an Embedded Memory Interface. An application can write the register with its Application ID, then immediately read it back. If the read value is not the same as the value written, then another application has ownership of the interface.

Note: The protocol used to pass commands back and forth through the Embedded Memory Interface Registers Interface is left to the System designer. Microchip can provide an application example of working code in which the host uses the Embedded Memory Interface registers to gain access to all of the EC registers.

15.9 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the Embedded Memory Interface (EMI). Host access for each register listed in this table is defined as an offset in the Host address space to the EMI Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for each instance of the Embedded Memory Interface (EMI) shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

The Embedded Memory Interface (EMI) can be accessed from the LPC Host Interface, the ESPI Host Interface, or the internal embedded controller (EC). The following table summarizes the host access types supported for each interface.

TABLE 15-5: HOST R/W ACCESS TYPES

IP Block Register Banks	LPC	ESPI	EC
EMI - Runtime Register Bank	Byte Access: R/W Word Access: None DWord Access: None	Byte Access: R/W Word Access: R/W DWord Access: Read Only	Byte Access: R/W Word Access: R/W DWord Access: R/W

TABLE 15-6: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	HOST-to-EC Mailbox Register
01h	EC-to-HOST Mailbox Register
02h	EC Address LSB Register
03h	EC Address MSB Register
04h	EC Data Byte 0 Register
05h	EC Data Byte 1 Register
06h	EC Data Byte 2 Register
07h	EC Data Byte 3 Register
08h	Interrupt Source LSB Register
09h	Interrupt Source MSB Register
0Ah	Interrupt Mask LSB Register
0Bh	Interrupt Mask MSB Register
0Ch	Application ID Register

15.9.1 HOST-TO-EC MAILBOX REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOST_EC_MBOX 8-bit mailbox used communicate information from the system host to the embedded controller. Writing this register generates an event to notify the embedded controller. The embedded controller has the option of clearing some or all of the bits in this register. This is dependent on the protocol layer implemented using the EMI Mailbox. The host must know this protocol to determine the meaning of the value that will be reported on a read. This bit field is aliased to the HOST_EC_MBOX bit field in the HOST-to-EC Mailbox Register	R/W	0h	RESET_SYS

15.9.2 EC-TO-HOST MAILBOX REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_HOST_MBOX 8-bit mailbox used communicate information from the embedded controller to the system host. Writing this register generates an event to notify the system host. The system host has the option of clearing some or all of the bits in this register. This is dependent on the protocol layer implemented using the EMI Mailbox. The embedded controller must know this protocol to determine the meaning of the value that will be reported on a read. This bit field is aliased to the EC_HOST_MBOX bit field in the EC-to-HOST Mailbox Register	R/WC	0h	RESET_SYS

15.9.3 EC ADDRESS LSB REGISTER

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	EC_ADDRESS_LSB This field defines bits[7:2] of EC_Address [15:0]. Bits[1:0] of the EC_Address are always forced to 00b. The EC_Address is aligned on a DWord boundary. It is the address of the memory being accessed by EC Data Byte 0 Register, which is an offset from the programmed base address of the selected REGION.	R/W	0h	RESET_SYS

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Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1:0	ACCESS_TYPE This field defines the type of access that occurs when the EC Data Register is read or written. 11b=Auto-increment 32-bit access. 10b=32-bit access. 01b=16-bit access. 00b=8-bit access. Each of these access types are defined in detail in Section 15.8.3, "Access Types".	R/W	0h	RESET_SYS

15.9.4 EC ADDRESS MSB REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	REGION The field specifies which of two segments in the 32-bit internal address space is to be accessed by the EC_Address[14:2] to generate accesses to the memory. 1=The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 1 Register. 0=The address defined by EC_Address[14:2] is relative to the base address specified by the Memory Base Address 0 Register.	R/W	0h	RESET_SYS
6:0	EC_ADDRESS_MSB This field defines bits[14:8] of EC_Address. Bits[1:0] of the EC_Address are always forced to 00b. The EC_Address is aligned on a DWord boundary. It is the address of the memory being accessed by EC Data Byte 0 Register, which is an offset from the programmed base address of the selected REGION.	R/W	0h	RESET_SYS

15.9.5 EC DATA BYTE 0 REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_0 This is byte 0 (Least Significant Byte) of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 15.8.2, "EC Data Register".	R/W	0h	RESET_SYS

15.9.6 EC DATA BYTE 1 REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_1 This is byte 1 of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 15.8.2, "EC Data Register".	R/W	0h	RESET_SYS

15.9.7 EC DATA BYTE 2 REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_2 This is byte 2 of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 15.8.2, "EC Data Register".	R/W	0h	RESET_SYS

15.9.8 EC DATA BYTE 3 REGISTER

Offset	07h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_DATA_BYTE_3 This is byte 3 (Most Significant Byte) of the 32-bit EC Data Register. Use of the Data Byte registers to access EC memory is defined in detail in Section 15.8.2, "EC Data Register".	R/W	0h	RESET_SYS

15.9.9 INTERRUPT SOURCE LSB REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	EC_SWI_LSB EC Software Interrupt Least Significant Bits. These bits are software interrupt bits that may be set by the EC to notify the host of an event. The meaning of these bits is dependent on the firmware implementation. Each bit in this field is cleared when written with a '1b'. The ability to clear the bit can be disabled by the EC if the corresponding bit in the Host Clear Enable Register is set to '0b'. This may be used by firmware for events that cannot be cleared while the event is still active.	R/WC	0h	RESET_SYS

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Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	EC_WR EC Mailbox Write. This bit is set when the EC-to-HOST Mailbox Register has been written by the EC at offset 01h of the EC-Only registers. Note: there is no corresponding mask bit in the Interrupt Mask LSB Register.	R	0h	RESET_SYS

15.9.10 INTERRUPT SOURCE MSB REGISTER

Offset	09h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_SWI_MSB EC Software Interrupt Most Significant Bits. These bits are software interrupt bits that may be set by the EC to notify the host of an event. The meaning of these bits is dependent on the firmware implementation. Each bit in this field is cleared when written with a '1b'. The ability to clear the bit can be disabled by the EC. if the corresponding bit in the Host Clear Enable Register is set to '0b'. This may be used by firmware for events that cannot be cleared while the event is still active.	R/WC	0h	RESET_SYS

15.9.11 INTERRUPT MASK LSB REGISTER

Offset	0Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	EC_SWI_EN_LSB EC Software Interrupt Enable Least Significant Bits. Each bit that is set to '1b' in this field enables the generation of a Host Event interrupt by the corresponding bit in the EC_SWI field in the Interrupt Source LSB Register.	R/W	0h	RESET_SYS
0	TEST	R/W	0h	RESET_SYS

15.9.12 INTERRUPT MASK MSB REGISTER

Offset	0Bh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_SWI_EN_MSB EC Software Interrupt Enable Most Significant Bits. Each bit that is set to '1b' in this field enables the generation of a Host Event interrupt by the corresponding bit in the EC_SWI field in the Interrupt Source MSB Register.	R/W	0h	RESET_SYS

15.9.13 APPLICATION ID REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	APPLICATION_ID When this field is 00h it can be written with any value. When set to a non-zero value, writing that value will clear this register to 00h. When set to a non-zero value, writing any value other than the current contents will have no effect.	R/W	0h	RESET_SYS

15.10 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Embedded Memory Interface (EMI) Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 15-7: EC-ONLY REGISTER SUMMARY

Offset	Register Name
100h	HOST-to-EC Mailbox Register
101h	EC-to-HOST Mailbox Register
104h	Memory Base Address 0 Register
108h	Memory Read Limit 0 Register
10Ah	Memory Write Limit 0 Register
10Ch	Memory Base Address 1 Register
110h	Memory Read Limit 1 Register
112h	Memory Write Limit 1 Register
114h	Interrupt Set Register
116h	Host Clear Enable Register

15.10.1 HOST-TO-EC MAILBOX REGISTER

Offset	100h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOST_EC_MBOX 8-bit mailbox used communicate information from the system host to the embedded controller. Writing this register generates an event to notify the embedded controller. The embedded controller has the option of clearing some or all of the bits in this register. This is dependent on the protocol layer implemented using the EMI Mailbox. The host must know this protocol to determine the meaning of the value that will be reported on a read. This bit field is aliased to the HOST_EC_MBOX bit field in the HOST-to-EC Mailbox Register.	R/WC	0h	RESET_SYS

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15.10.2 EC-TO-HOST MAILBOX REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_HOST_MBOX 8-bit mailbox used communicate information from the embedded controller to the system host. Writing this register generates an event to notify the system host. The system host has the option of clearing some or all of the bits in this register. This is dependent on the protocol layer implemented using the EMI Mailbox. The embedded controller must know this protocol to determine the meaning of the value that will be reported on a read. This bit field is aliased to EC_HOST_MBOX bit field in the EC-to-HOST Mailbox Register.	R/W	0h	RESET_SYS

15.10.3 MEMORY BASE ADDRESS 0 REGISTER

Offset	104h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	MEMORY_BASE_ADDRESS_0 This memory base address defines the beginning of region 0 in the Embedded Controller's 32-bit internal address space. Memory allocated to region 0 is intended to be shared between the Host and the EC. The region defined by this base register is used when bit 15 of the EC Address Register is 0. The access will be to a memory location at an offset defined by the EC_Address relative to the beginning of the region defined by this register. Therefore, a read or write to the memory that is triggered by the EC Data Register will occur at Memory_Base_Address_0 + EC_Address.	R/W	0h	RESET_SYS
1:0	Reserved	R	-	-

15.10.4 MEMORY READ LIMIT 0 REGISTER

Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15	Reserved	R	-	-
14:2	MEMORY_READ_LIMIT_0 Whenever a read of any byte in the EC Data Register is attempted, and bit 15 of EC_Address is 0, the field EC_Address[14:2] in the EC_Address_Register is compared to this field. As long as EC_Address[14:2] is less than this field the EC_Data_Register will be loaded from the 32-bit internal address space.	R/W	0h	RESET_SYS
1:0	Reserved	R	-	-

15.10.5 MEMORY WRITE LIMIT 0 REGISTER

Offset	10Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15	Reserved	R	-	-
14:2	MEMORY_WRITE_LIMIT_0 Whenever a write of any byte in EC DATA Register is attempted and bit 15 of EC_Address is 0, the field EC_ADDRESS_MSB in the EC_Address Register is compared to this field. As long as EC_Address[14:2] is less than Memory_Write_Limit_0[14:2] the addressed bytes in the EC DATA Register will be written into the internal 32-bit address space. If EC_Address[14:2] is greater than or equal to the Memory_Write_Limit_0[14:2] no writes will take place.	R/W	0h	RESET_SYS
1:0	Reserved	R	-	-

15.10.6 MEMORY BASE ADDRESS 1 REGISTER

Offset	10Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	MEMORY_BASE_ADDRESS_1 This memory base address defines the beginning of region 1 in the Embedded Controller's 32-bit internal address space. Memory allocated to region 1 is intended to be shared between the Host and the EC. The region defined by this base register is used when bit 15 of the EC Address Register is 1. The access will be to a memory location at an offset defined by the EC_Address relative to the beginning of the region defined by this register. Therefore, a read or write to the memory that is triggered by the EC Data Register will occur at Memory_Base_Address_1 + EC_Address.	R/W	0h	RESET_SYS
1:0	Reserved	R	-	-

15.10.7 MEMORY READ LIMIT 1 REGISTER

Offset	110h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15	Reserved	R	-	-
14:2	MEMORY_READ_LIMIT_1 Whenever a read of any byte in the EC Data Register is attempted, and bit 15 of EC_ADDRESS is 1, the field EC_ADDRESS in the EC_Address_Register is compared to this field. As long as EC_ADDRESS is less than this value, the EC_Data_Register will be loaded from the 32-bit internal address space.	R/W	0h	RESET_SYS
1:0	Reserved	R	-	-

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15.10.8 MEMORY WRITE LIMIT 1 REGISTER

Offset	112h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15	Reserved	R	-	-
14:2	MEMORY_WRITE_LIMIT_1 Whenever a write of any byte in EC DATA Register is attempted and bit 15 of EC_Address is 1, the field EC_Address[14:2] in the EC_Address Register is compared to this field. As long as EC_Address[14:2] is less than Memory_Write_Limit_1[14:2] the addressed bytes in the EC DATA Register will be written into the internal 32-bit address space. If EC_Address[14:2] is greater than or equal to the Memory_Write_Limit_1[14:2] no writes will take place.	R/W	0h	RESET_SYS
1:0	Reserved	R	-	-

15.10.9 INTERRUPT SET REGISTER

Offset	114h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:1	EC_SWI_SET EC Software Interrupt Set. This register provides the EC with a means of updating the Interrupt Source Registers. Writing a bit in this field with a ‘1b’ sets the corresponding bit in the Interrupt Source Register to ‘1b’. Writing a bit in this field with a ‘0b’ has no effect. Reading this field returns the current contents of the Interrupt Source Register.	R/WS	0h	RESET_SYS
0	Reserved	R	-	-

15.10.10 HOST CLEAR ENABLE REGISTER

Offset	116h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:1	HOST_CLEAR_ENABLE When a bit in this field is ‘0b’, the corresponding bit in the Interrupt Source Register cannot be cleared by writes to the Interrupt Source Register. When a bit in this field is ‘1b’, the corresponding bit in the Interrupt Source Register can be cleared when that register bit is written with a ‘1b’. These bits allow the EC to control whether the status bits in the Interrupt Source Register are based on an edge or level event.	R/W	0h	RESET_SYS
0	Reserved	R	-	-

16.0 MAILBOX INTERFACE

16.1 Overview

The Mailbox provides a standard run-time mechanism for the host to communicate with the Embedded Controller (EC)

16.2 References

No references have been cited for this feature.

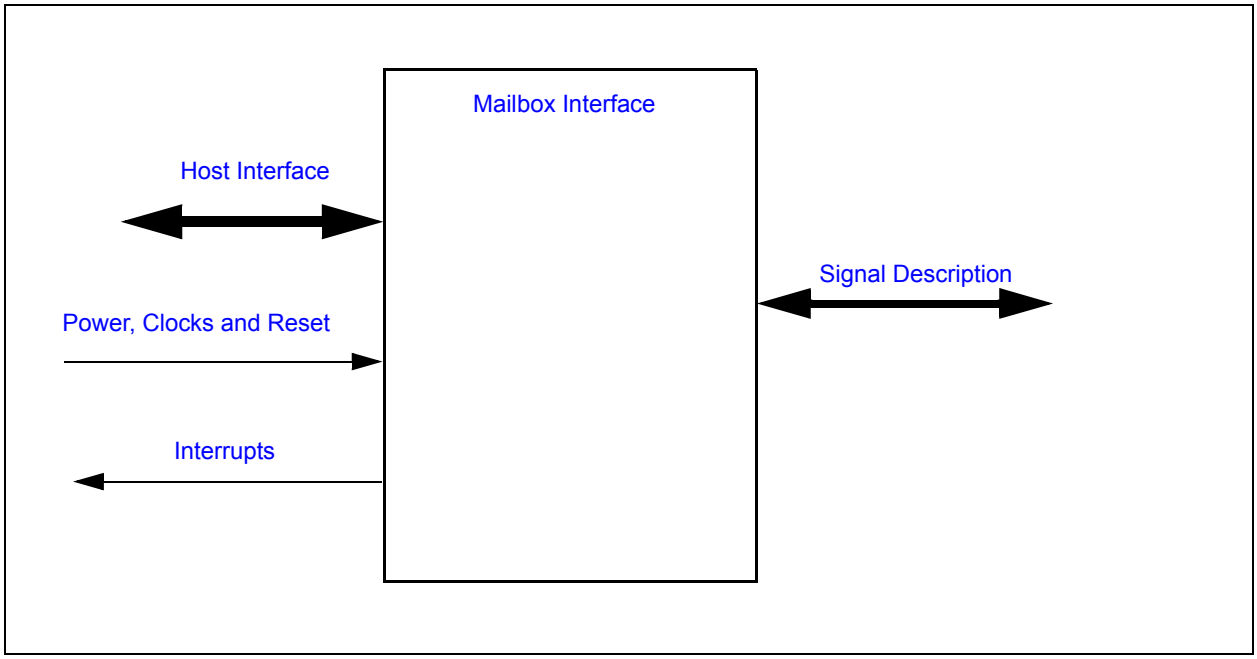
16.3 Terminology

There is no terminology defined for this section.

16.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 16-1: I/O DIAGRAM OF BLOCK



16.5 Signal Description

TABLE 16-1: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
nSMI	OUTPUT	SMI alert signal to the Host.

16.6 Host Interface

The Mailbox interface is accessed by host software via a registered interface, as defined in Section 16.11, "Runtime Registers" and Section 16.12, "EC Registers".

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16.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

16.7.1 POWER DOMAINS

TABLE 16-2: POWER SOURCES

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

16.7.2 CLOCK INPUTS

TABLE 16-3: CLOCK INPUTS

Name	Description
48MHz	This is the clock source for Mailbox logic.

16.7.3 RESETS

TABLE 16-4: RESET SIGNALS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.
RESET_VCC	This signal is asserted when the main power rail is asserted. The Host Access Port is reset when this signal is de-asserted.

16.8 Interrupts

TABLE 16-5: SYSTEM INTERRUPTS

Source	Description
MBX_Host_SERIRQ	This interrupt source for the SERIRQ logic is generated when the EC_WR bit is ‘1’ and enabled by the EC_WR_EN bit.
MBX_Host_SMI	This interrupt source for the SERIRQ logic is generated when any of the EC_SWI bits are asserted and the corresponding EC_SWI_EN bit are asserted as well. This event is also asserted if the EC_WR/EC_WR_EN event occurs as well. This bit is also routed to the nSMI pin.

TABLE 16-6: EC INTERRUPTS

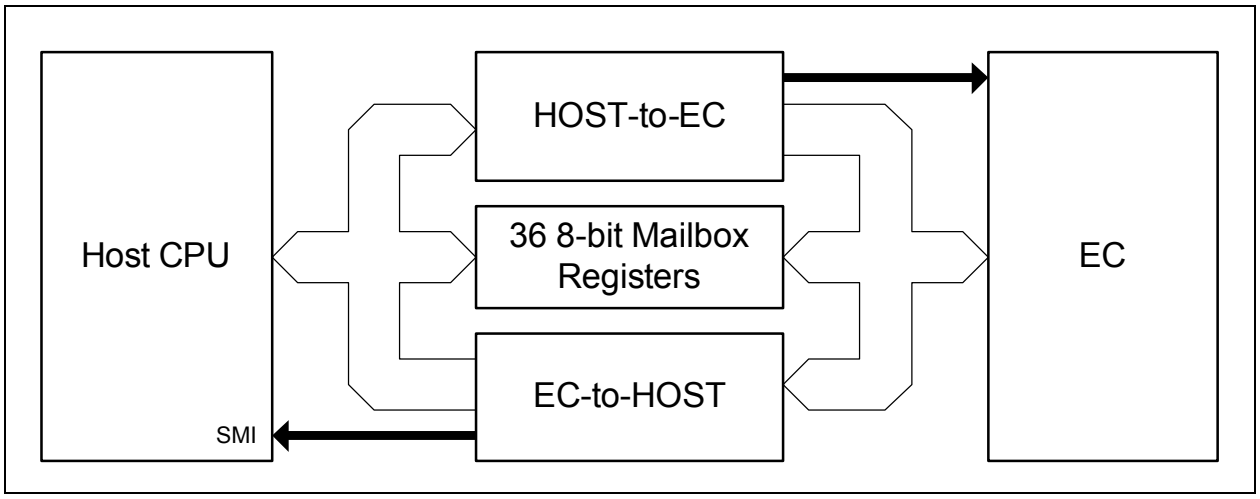
Source	Description
MBX	Interrupt generated by the host writing the HOST-to-EC Mailbox register.

16.9 Low Power Modes

The Mailbox automatically enters a low power mode whenever it is not actively.

16.10 Description

FIGURE 16-2: MAILBOX BLOCK DIAGRAM



16.10.1 HOST ACCESS PORT

The Mailbox includes a total of 36 index-addressable 8-bit Mailbox registers and a two byte Mailbox Registers Host Access Port. Thirty-two of the 36 index-addressable 8-bit registers are EC Mailbox registers, which can be read and written by both the EC and the Host. The remaining four registers are used for signaling between the Host and the EC. The Host Access Port consists of two 8-bit run-time registers that occupy two addresses in the HOST I/O space, MBX_INDEX Register and MBX_DATA Register. The Host Access Port is used by the host to access the 36 index-addressable 8-bit registers.

To access a Mailbox register once the Mailbox Registers Interface Base Address has been initialized, the Mailbox register index address is first written to the MBX Index port. After the Index port has been written, the Mailbox data byte can be read or written via the MBX data port.

The Host Access Port is intended to be accessed by the Host only, however it may be accessed by the EC at the Offset shown from its EC base address in Table 16-7, "Runtime Register Summary".

16.10.2 HOST INTERRUPT GENERATION

The Mailbox can generate a SERIRQ event for EC-to-HOST EC events, using the EC-to-Host Mailbox Register. This interrupt is routed to the SERIRQ block.

The Mailbox can also generate an SMI event, using SMI Interrupt Source Register. The SMI event can be routed to any frame in the SERIRQ stream as well as to the nSMI pin. The SMI event can be routed to nSMI pin by selecting the nSMI signal function in the associated GPIO Pin Control Register. The SMI event produces a standard active low frame on the serial IRQ stream and active low level on the open drain nSMI pin.

Routing for both the SERIRQ logic and the nSMI pin is shown in Figure 16-3.

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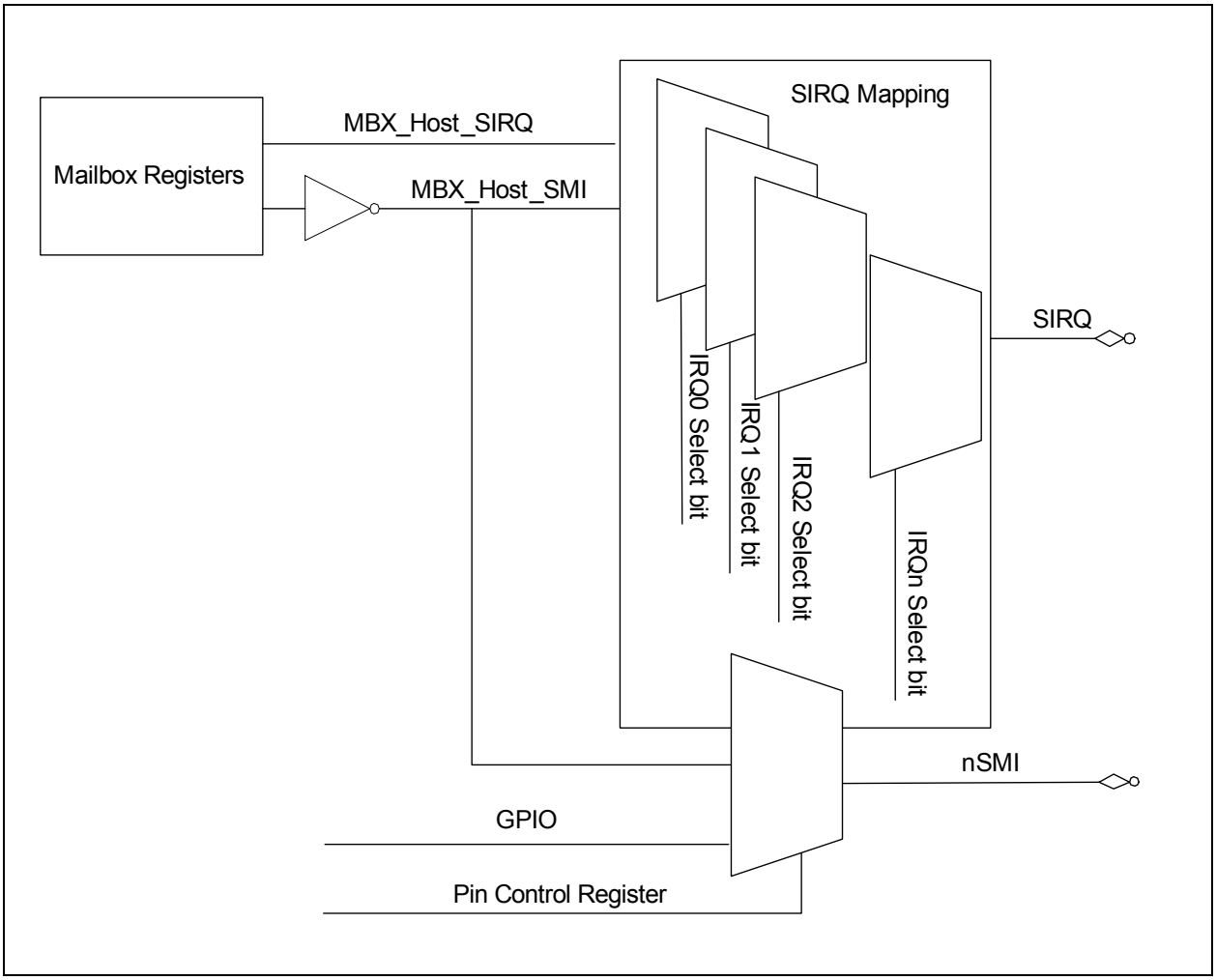
FIGURE 16-3: MAILBOX SERIRQ AND SMI ROUTING



16.10.3 EC MAILBOX CONTROL

The HOST-to-EC Mailbox Register and EC-to-Host Mailbox Register are designed to pass commands between the host and the EC. If enabled, these registers can generate interrupts to both the Host and the EC.

The two registers are not dual-ported, so the HOST BIOS and Keyboard BIOS must be designed to properly share these registers. When the host performs a write of the HOST-to-EC Mailbox Register, an interrupt will be generated and seen by the EC if unmasked. When the EC writes FFh to the Mailbox Register, the register resets to 00h, providing a simple means for the EC to inform the host that an operation has been completed.

When the EC writes the EC-to-Host Mailbox Register, an SMI may be generated and seen by the host if unmasked. When the Host CPU writes FFh to the register, the register resets to 00h, providing a simple means for the host to inform that EC that an operation has been completed.

Note:	The protocol used to pass commands back and forth through the Mailbox Registers Interface is left to the System designer. Microchip can provide an application example of working code in which the host uses the Mailbox registers to gain access to all of the EC registers.

16.11 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the Mailbox Interface. Host access for each register listed in this table is defined as an offset in the Host address space to the Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for the Mailbox Interface shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

TABLE 16-7: RUNTIME REGISTER SUMMARY

Offset	Register Name
0h	MBX_INDEX Register
1h	MBX_DATA Register

16.11.1 MBX_INDEX REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	INDEX The index into the mailbox registers listed in Table 16-8, "Register Summary".	R/W	0h	RESET_VCC

16.11.2 MBX_DATA REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DATA Data port used to access the registers listed in Table 16-8, "Register Summary".	R/W	0h	RESET_VCC

16.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset shown in the "EC Offset" column to the Base Address for each instance of the Mailbox Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory". In addition, the registers can be accessed through the Host Access Port, at the indexes listed in the following tables as "MBX_INDEX".

TABLE 16-8: REGISTER SUMMARY

EC Offset	Host I/O Index (MBX_INDEX)	Register Name
100h	00h	HOST-to-EC Mailbox Register
104h	01h	EC-to-Host Mailbox Register
108h	02h	SMI Interrupt Source Register
10Ch	03h	SMI Interrupt Mask Register
110h	10h	Mailbox register [0]
	11h	Mailbox register [1]
	12h	Mailbox register [2]
	13h	Mailbox register [3]

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TABLE 16-8: REGISTER SUMMARY (CONTINUED)

EC Offset	Host I/O Index (MBX_INDEX)	Register Name
114h	14h	Mailbox register [4]
	15h	Mailbox register [5]
	16h	Mailbox register [6]
	17h	Mailbox register [7]
118h	18h	Mailbox register [8]
	19h	Mailbox register [9]
	1Ah	Mailbox register [A]
	1Bh	Mailbox register [B]
11Ch	1Ch	Mailbox register [C]
	1Dh	Mailbox register [D]
	1Eh	Mailbox register [E]
	1Fh	Mailbox register [F]
120h	20h	Mailbox register [10]
	21h	Mailbox register [11]
	22h	Mailbox register [12]
	23h	Mailbox register [13]
124h	24h	Mailbox register [14]
	25h	Mailbox register [15]
	26h	Mailbox register [16]
	27h	Mailbox register [17]
128h	28h	Mailbox register [18]
	29h	Mailbox register [19]
	2Ah	Mailbox register [1A]
	2Bh	Mailbox register [1B]
12Ch	2Ch	Mailbox register [1C]
	2Dh	Mailbox register [1D]
	2Eh	Mailbox register [1E]
	2Fh	Mailbox register [1F]

16.12.1 HOST-TO-EC MAILBOX REGISTER

Offset	100h			
MBX_ INDEX	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOST_EC_MBOX If enabled, an interrupt to the EC marked by the MBX bit in the Interrupt Aggregator will be generated whenever the Host writes this register. The interrupt is cleared when this register is read by the EC. This register is cleared when written with FFh. This field is Read/Write when accessed through the Host Access Port. When written at the EC offset, each bit in this field is cleared when written with a '1b'. Writes of '0b' have no effect.	Host Access Port: R/W EC: R/WC	0h	RESET_SYS

16.12.2 EC-TO-HOST MAILBOX REGISTER

Offset	104h			
MBX_ INDEX	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_HOST_MBOX An EC write to this register will set bit EC_WR in the SMI Interrupt Source Register to '1b'. If enabled, this will generate a Host SMI or a Host SERIRQ. The SERIRQ is cleared when this register is read by the Host. This register is cleared when written with FFh. This field is Read/Write when accessed by the EC at the EC offset. When written through the Host Access Port, each bit in this field is cleared when written with a '1b'. Writes of '0b' have no effect.	Host Access Port: R/WC EC: R/W	0h	RESET_SYS

16.12.3 SMI INTERRUPT SOURCE REGISTER

Offset	108h			
MBX_ INDEX	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	EC_SWI EC Software Interrupt. An SERIRQ to the Host is generated when any bit in this register when this bit is set to '1b' and the corresponding bit in the SMI Interrupt Mask Register register is '1b'. This field is Read/Write when accessed by the EC at the EC offset. When written through the Host Access Port, each bit in this field is cleared when written with a '1b'. Writes of '0b' have no effect.	Host Access Port: R/WC EC: R/W	0h	RESET_SYS

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Offset	108h			
MBX_ INDEX	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	EC_WR EC Mailbox Write. This bit is set automatically when the EC-to-Host Mailbox Register has been written. An SMI or SERIRQ to the Host is generated when n this bit is ‘1b’ and the corresponding bit in the SMI Interrupt Mask Register register is ‘1b’. This bit is automatically cleared by a read of the EC-to-Host Mailbox Register through the Host Access Port. This bit is read-only when read through the Host Access Port. It is neither readable nor writable directly by the EC when accessed at the EC offset.	Host Access Port: R EC: -	0h	RESET_ SYS

16.12.4 SMI INTERRUPT MASK REGISTER

Offset	10Ch			
MBX_ INDEX	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	EC_SWI_EN EC Software Interrupt Enable. If this bit is ‘1b’, the bit EC_WR in the SMI Interrupt Source Register is enabled for the generation of SERIRQ or nSMI events.	R/W	0h	RESET_ SYS
0	EC_WR_EN EC Mailbox Write.Interrupt Enable. Each bit in this field that is ‘1b’ enables the generation of SERIRQ interrupts when the corresponding bit in the EC_SWI field in the SMI Interrupt Source Register is ‘1b’.	R/W	0h	RESET_ SYS

17.0 UART

17.1 Introduction

The 16550 UART (Universal Asynchronous Receiver/Transmitter) is a full-function Serial Port that supports the standard RS-232 Interface.

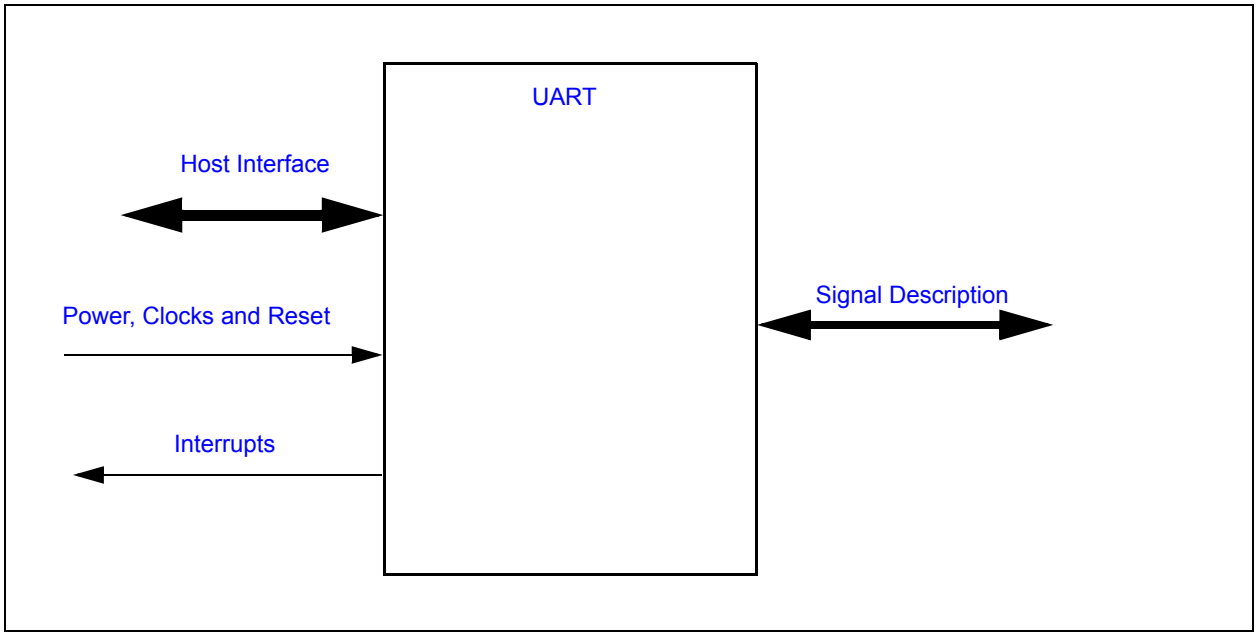
17.2 References

- EIA Standard RS-232-C specification

17.3 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 17-1: I/O DIAGRAM OF BLOCK



17.4 Signal Description

TABLE 17-1: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
DTR#	Output	Active low Data Terminal ready output for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). **Note:** Defaults to tri-state on V3_DUAL power on.
DCD#	Output	Active low Data Carrier Detect input for the serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCD# signal by reading bit 7 of Modem Status Register (MSR). A DCD# signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCD # changes state.

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TABLE 17-1: SIGNAL DESCRIPTION TABLE (CONTINUED)

Name	Direction	Description
DSR#	Input	Active low Data Set Ready input for the serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSR# signal by reading bit 5 of Modem Status Register (MSR). A DSR# signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR# changes state.
RI#	Input	Active low Ring Indicator input for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RI# signal by reading bit 6 of Modem Status Register (MSR). A RI# signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RI# changes state.
RTS#	Output	Active low Request to Send output for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). The hardware reset will reset the RTS# signal to inactive mode (high). RTS# is forced inactive during loop mode operation. Defaults to tri-state on V3_DUAL power on.
CTS#	Input	Active low Clear to Send input for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes state. The CTS# signal has no effect on the transmitter.
TXD	Output	Transmit serial data output.
RXD	Input	Receiver serial data input.

17.5 Host Interface

The UART is accessed by host software via a registered interface, as defined in Section 17.11, "Configuration Registers" and Section 17.10, "Runtime Registers".

17.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

17.6.1 POWER DOMAINS

TABLE 17-2: POWER SOURCES

Name	Description
VTR	This Power Well is used to power the registers and logic in this block.

17.6.2 CLOCKS

TABLE 17-3: CLOCK INPUTS

Name	Description
UART_CLK	An external clock that may be used as an alternative to the internally-generated 1.8432MHz and 24MHz baud clocks. Selection between internal baud clocks and an external baud clock is configured by the CLK_SRC bit in the Configuration Select Register.
48MHz	This is the main clock domain. Because the clock input must be within ± 2% in order to generate standard baud rates, the 48MHz clock must be generated by a reference clock with better than 1% accuracy (i.e., external crystal) and locked to its frequency before the UART will work with the standard rates.

TABLE 17-4: DERIVED CLOCKS

Name	Description
1.8432MHz	The UART requires a 1.8432 MHz ± 2% clock input for baud rate generation of standard baud rates up to 115,200 baud. It is derived from the system 48MHz clock domain.
24MHz	A 24MHz ± 2% clock input for baud rate generation, derived from the system 48MHz clock domain. It may be used as an alternative to the 1.8432MHz clock, generating non-standard baud rates up to 1,500,000 baud.

17.6.3 RESETS

TABLE 17-5: RESET SIGNALS

Name	Description
RESET_SYS	This reset is asserted when VTR is applied.
RESET_VCC	This is an alternate reset condition, typically asserted when the main power rail is asserted.
RESET	This reset is determined by the POWER bit signal. When the power bit signal is 1, this signal is equal to RESET_VCC, if present. When the power bit signal is 0, this signal is equal to RESET_SYS.

17.7 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 17-6: SYSTEM INTERRUPTS

Source	Description
UART	The UART interrupt event output indicates if an interrupt is pending. See Table 17-12, "Interrupt Control Table".

TABLE 17-7: EC INTERRUPTS

Source	Description
UART	The UART interrupt event output indicates if an interrupt is pending. See Table 17-12, "Interrupt Control Table".

17.8 Low Power Modes

The UART may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

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17.9 Description

The UART is compatible with the 16450, the 16450 ACE registers and the 16C550A. The UART performs serial-to-parallel conversions on received characters and parallel-to-serial conversions on transmit characters. Two sets of baud rates are provided. When the 1.8432 MHz source clock is selected, standard baud rates from 50 to 115.2K are available. When the source clock is 24 MHz, baud rates up to 1,500K are available. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock signal by 1 to 65535. The UART is also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, powering down and changing the base address of the UART. The UART interrupt is enabled by programming OUT2 of the UART to logic “1.” Because OUT2 is logic “0,” it disables the UART's interrupt. The UART is accessible by both the Host and the EC.

17.9.1 PROGRAMMABLE BAUD RATE

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal clock source by any divisor from 1 to 65535. Unless an external clock source is configured, the clock source is either the 1.8432MHz clock source or the 24MHz clock source. The output frequency of the Baud Rate Generator is 16x the Baud rate. Two eight bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers, the output divides the clock by the number 3. If a 1 is loaded, the output is the inverse of the input oscillator. If a two is loaded, the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded, the output is low for 2 bits and high for the remainder of the count.

The following tables show possible baud rates.

TABLE 17-8: UART BAUD RATES USING CLOCK SOURCE 1.8432MHz

Desired Baud Rate	BAUD_CLOCK_SEL	Divisor Used to Generate 16X Clock
50	0	2304
75	0	1536
110	0	1047
134.5	0	857
150	0	768
300	0	384
600	0	192
1200	0	96
1800	0	64
2000	0	58
2400	0	48
3600	0	32
4800	0	24
7200	0	16
9600	0	12
19200	0	6
38400	0	3
57600	0	2
115200	0	1

TABLE 17-9: UART BAUD RATES USING CLOCK SOURCE 24MHz

Desired Baud Rate	BAUD_CLOCK_SEL	Divisor Used to Generate 16X Clock
125000	1	12
136400	1	11
150000	1	10
166700	1	9
187500	1	8
214300	1	7
250000	1	6
300000	1	5
375000	1	4
500000	1	3
750000	1	2
1500000	1	1

17.10 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the UART. Host access for each register listed in this table is defined as an offset in the Host address space to the Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for each instance of the UART shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

TABLE 17-10: RUNTIME REGISTER SUMMARY

DLAB Note 1	Offset	Register Name
0	0h	Receive Buffer Register
0	0h	Transmit Buffer Register
1	0h	Programmable Baud Rate Generator LSB Register
1	1h	Programmable Baud Rate Generator MSB Register
0	1h	Interrupt Enable Register
x	02h	FIFO Control Register
x	02h	Interrupt Identification Register
x	03h	Line Control Register
x	04h	Modem Control Register
x	05h	Line Status Register
x	06h	Modem Status Register
x	07h	Scratchpad Register

Note 1: DLAB is bit 7 of the Line Control Register.

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17.10.1 RECEIVE BUFFER REGISTER

Offset	0h (DLAB=0)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	RECEIVED_DATA This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.	R	0h	RESET

17.10.2 TRANSMIT BUFFER REGISTER

Offset	0h (DLAB=0)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	TRANSMIT_DATA This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.	W	0h	RESET

17.10.3 PROGRAMMABLE BAUD RATE GENERATOR LSB REGISTER

Offset	00h (DLAB=1)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	BAUD_RATE_DIVISOR_LSB See Section 17.9.1, "Programmable Baud Rate".	R/W	0h	RESET

17.10.4 PROGRAMMABLE BAUD RATE GENERATOR MSB REGISTER

Offset	01h (DLAB=1)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	BAUD_CLK_SEL If CLK_SRC is '0': • 0=The baud clock is derived from the 1.8432MHz. • 1=IThe baud clock is derived from the 24MHz. If CLK_SRC is '1': • This bit has no effect	R/W	0h	RESET
6:0	BAUD_RATE_DIVISOR_MSB See Section 17.9.1, "Programmable Baud Rate".	R/W	0h	RESET

17.10.5 INTERRUPT ENABLE REGISTER

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the MEC170x. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Offset	01h (DLAB=0)			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	-	-
3	EMSI This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.	R/W	0h	RESET
2	ELSI This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.	R/W	0h	RESET
1	ETHREI This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".	R/W	0h	RESET
0	ERDAI This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".	R/W	0h	RESET

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17.10.6 FIFO CONTROL REGISTER

This is a write only register at the same location as the Interrupt Identification Register.

Note:	DMA is not supported.

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	RECV_FIFO_TRIGGER_LEVEL These bits are used to set the trigger level for the RCVR FIFO interrupt.	W	0h	RESET
5:4	Reserved	R	-	-
3	DMA_MODE_SELECT Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.	W	0h	RESET
2	CLEAR_XMIT_FIFO Setting this bit to a logic “1” clears all bytes in the XMIT FIFO and resets its counter logic to “0”. The shift register is not cleared. This bit is self-clearing.	W	0h	RESET
1	CLEAR_RECv_FIFO Setting this bit to a logic “1” clears all bytes in the RCVR FIFO and resets its counter logic to “0”. The shift register is not cleared. This bit is self-clearing.	W	0h	RESET
0	EXRF Enable XMIT and RECV FIFO. Setting this bit to a logic “1” enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic “0” disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.	W	0h	RESET

TABLE 17-11: RECV FIFO TRIGGER LEVELS

Bit 7	**Bit 6**	**RECV FIFO Trigger Level (BYTES)**
0	0	1
	1	4
1	0	8
	1	14

17.10.7 INTERRUPT IDENTIFICATION REGISTER

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready

3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 17-12). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	FIFO_EN These two bits are set when the FIFO CONTROL Register bit 0 equals 1.	R	0h	RESET
5:4	Reserved	R	-	-
3:1	INTID These bits identify the highest priority interrupt pending as indicated by Table 17-12, "Interrupt Control Table". In non-FIFO mode, Bit[3] is a logic “0”. In FIFO mode Bit[3] is set along with Bit[2] when a timeout interrupt is pending.	R	0h	RESET
0	IPEND This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic ‘0’ an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic ‘1’ no interrupt is pending.	R	1h	RESET

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TABLE 17-12: INTERRUPT CONTROL TABLE

FIFO Mode Only	Interrupt Identification Register			Interrupt SET and RESET Functions			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	-	None	None	-
	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
		0		Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1					Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1		Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
	0	0		Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

17.10.8 LINE CONTROL REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	DLAB Divisor Latch Access Bit (DLAB). It must be set high (logic “1”) to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic “0”) to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.	R/W	0h	RESET
6	BREAK_CONTROL Set Break Control bit. When bit 6 is a logic “1”, the transmit data output (TXD) is forced to the Spacing or logic “0” state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.	R/W	0h	RESET
5	STICK_PARITY Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled. Bit 3 is a logic “1” and bit 5 is a logic “1”, the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.	R/W	0h	RESET
4	PARITY_SELECT Even Parity Select bit. When bit 3 is a logic “1” and bit 4 is a logic “0”, an odd number of logic “1”'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic “1” and bit 4 is a logic “1” an even number of bits is transmitted and checked.	R/W	0h	RESET
3	ENABLE_PARITY Parity Enable bit. When bit 3 is a logic “1”, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).	R/W	0h	RESET
2	STOP_BITS This bit specifies the number of stop bits in each transmitted or received serial character. Table 17-13 summarizes the information. The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.	R/W	0h	RESET
1:0	WORD_LENGTH These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:	R/W	0h	RESET

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TABLE 17-13: STOP BITS

Bit 2	Word Length	Number of Stop Bits
0	--	1
1	5 bits	1.5
	6 bits	2
	7 bits	
	8 bits	

TABLE 17-14: SERIAL CHARACTER

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

17.10.9 MODEM CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:5	Reserved	R	-	-
4	LOOPBACK This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic “1”, the following occur: 1. The TXD is set to the Marking State (logic “1”). 2. The receiver Serial Input (RXD) is disconnected. 3. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input. 4. All MODEM Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. 5. The four MODEM Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (DSR#, CTS#, RI#, DCD#). 6. The Modem Control output pins are forced inactive high. 7. Data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.	R/W	0h	RESET
3	OUT2 Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic “0”, the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic “1”, the serial port interrupt outputs are enabled.	R/W	0h	RESET
2	OUT1 This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.	R/W	0h	RESET
1	RTS This bit controls the Request To Send (RTS#) output. When bit 1 is set to a logic “1”, the RTS# output is forced to a logic “0”. When bit 1 is set to a logic “0”, the RTS# output is forced to a logic “1”.	R/W	0h	RESET
0	DTR This bit controls the Data Terminal Ready (DTR#) output. When bit 0 is set to a logic “1”, the DTR# output is forced to a logic “0”. When bit 0 is a logic “0”, the DTR# output is forced to a logic “1”.	R/W	0h	RESET

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17.10.10 LINE STATUS REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	FIFO_ERROR This bit is permanently set to logic “0” in the 450 mode. In the FIFO mode, this bit is set to a logic “1” when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.	R	0h	RESET
6	TRANSMIT_ERROR Transmitter Empty. Bit 6 is set to a logic “1” whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic “0” whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,	R	0h	RESET
5	TRANSMIT_EMPTY Transmitter Holding Register Empty Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic “1” when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic “0” whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.	R	0h	RESET
4	BREAK_INTERRUPT Break Interrupt. Bit 4 is set to a logic “1” whenever the received data input is held in the Spacing state (logic “0”) for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic “1” for at least 1/2 bit time. Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt BIT 3 whenever any of the corresponding conditions are detected and the interrupt is enabled	R	0h	RESET

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	FRAME_ERROR Framing Error. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic “1” whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). This bit is reset to a logic “0” whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.	R	0h	RESET
2	PARITY ERROR Parity Error. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. This bit is set to a logic “1” upon detection of a parity error and is reset to a logic “0” whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.	R	0h	RESET
1	OVERRUN_ERROR Overrun Error. Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. This bit is set to a logic “1” immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.	R	0h	RESET
0	DATA_READY Data Ready. It is set to a logic ‘1’ whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic ‘0’ by reading all of the data in the Receive Buffer Register or the FIFO.	R	0h	RESET

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17.10.11 MODEM STATUS REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	DCD This bit is the complement of the Data Carrier Detect (DCD#) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to OUT2 in the MCR.	R	0h	RESET
6	RI This bit is the complement of the Ring Indicator (RI#) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to OUT1 in the MCR.	R	0h	RESET
5	DSR This bit is the complement of the Data Set Ready (DSR#) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to DTR# in the MCR.	R	0h	RESET
4	CTS This bit is the complement of the Clear To Send (CTS#) input. If bit 4 of the MCR is set to logic ‘1’, this bit is equivalent to RTS# in the MCR.	R	0h	RESET
3	DCD Delta Data Carrier Detect (DDCD). Bit 3 indicates that the DCD# input to the chip has changed state. NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic ‘1’, a MODEM Status Interrupt is generated.	R	0h	RESET
2	RI Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the RI# input has changed from logic ‘0’ to logic ‘1’.	R	0h	RESET
1	DSR Delta Data Set Ready (DDSR). Bit 1 indicates that the DSR# input has changed state since the last time the MSR was read.	R	0h	RESET
0	CTS Delta Clear To Send (DCTS). Bit 0 indicates that the CTS# input to the chip has changed state since the last time the MSR was read.	R	0h	RESET

17.10.12 SCRATCHPAD REGISTER

Offset	07h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	SCRATCH This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.	R/W	0h	RESET

17.11 Configuration Registers

Configuration Registers for an instance of the UART are listed in the following table. Host access to Configuration Registers is through the Configuration Port using the Logical Device Number of each instance of the UART and the Index shown in the “Host Index” column of the table. The EC can access Configuration Registers directly. The EC address for each register is formed by adding the Base Address for each instance of the UART shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the “EC Offset” column.

TABLE 17-15: CONFIGURATION REGISTER SUMMARY

EC Offset	Host Index	Register Name
330h	30h	Activate Register
3F0h	F0h	Configuration Select Register

17.11.1 ACTIVATE REGISTER

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	ACTIVATE When this bit is 1, the UART logical device is powered and functional. When this bit is 0, the UART logical device is powered down and inactive.	R/W	0b	RESET

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17.11.2 CONFIGURATION SELECT REGISTER

Offset	F0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:3	Reserved	R	-	-
2	POLARITY 1=The UART_TX and UART_RX pins functions are inverted 0=The UART_TX and UART_RX pins functions are not inverted	R/W	0b	RESET
1	POWER 1=The RESET reset signal is derived from RESET_VCC 0=The RESET reset signal is derived from RESET_SYS	R/W	1b	RESET
0	CLK_SRC 1=The UART Baud Clock is derived from an external clock source 0=The UART Baud Clock is derived from one of the two internal clock sources	R/W	0b	RESET

18.0 GPIO INTERFACE

18.1 Overview

The MEC170x GPIO interface provides general purpose input monitoring and output control, as well as managing many aspects of pin functionality; including, multi-function Pin Multiplexing Control, GPIO Direction control, Pull-up and Pull-down resistors, asynchronous wakeup and synchronous interrupt detection and Polarity control, as well as control of pin drive strength and slew rate.

Features of the GPIO interface include:

- Inputs:
  - Asynchronous rising and falling edge wakeup detection
  - Interrupt High or Low Level
- On Output:
  - Push Pull or Open Drain output
- Pull up or pull down resistor control
- Interrupt and wake capability available for all GPIOs
- Programmable pin drive strength and slew rate limiting
- Group- or individual control of GPIO data.
- Multiplexing of all multi-function pins are controlled by the GPIO interface

18.2 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

18.2.1 POWER DOMAINS

TABLE 18-1: POWER SOURCES

Name	Description
VTR	The I/O power for a subset of GPIOs is powered by this supply voltage.It may be 3.3V or 1.8V.

18.2.2 CLOCK INPUTS

TABLE 18-2: CLOCK INPUTS

Name	Description
48MHz	This clock domain is used for synchronizing GPIO inputs.

18.2.3 RESETS

TABLE 18-3: RESET SIGNALS

Name	Description
RESET_SYS	This reset is asserted when VTR is applied.
VCC_PWRGD	This signal, which if present comes directly from a pin, is asserted when the main system power rail is up.

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18.3 Interrupts

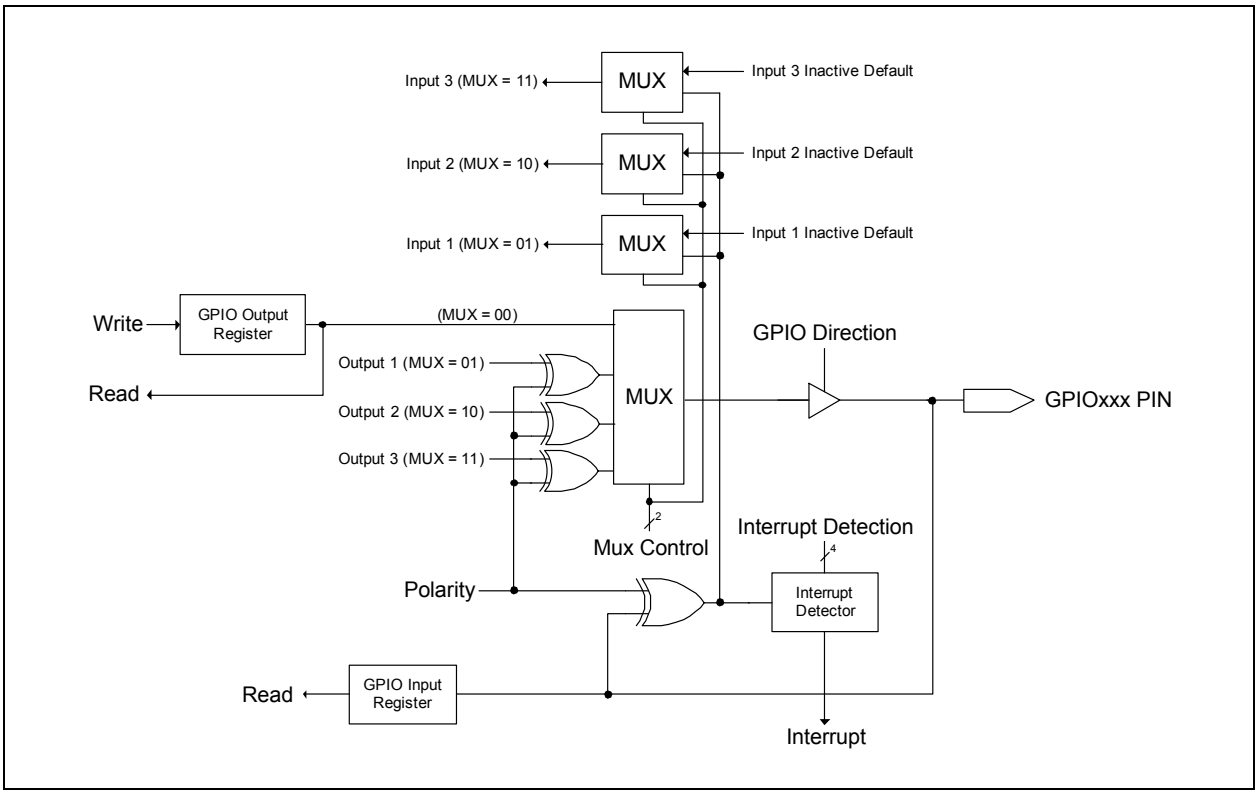
This section defines the Interrupt Sources generated from this block.

TABLE 18-4: INTERRUPTS

Source	Description
GPIO_Event	Each GPIO pin has the ability to generate an interrupt event. This event may be used as a wake event. The event can be generated on a high level, low level, rising edge, falling edge or either edge input, as configured by the INTERRUPT_DETECTION bits in the Pin Control Registers associated with the GPIO signal function. The minimum pulse width to generate in interrupt / wakeup event must be at least 5ns.

18.4 Description

FIGURE 18-1: GPIO BLOCK DIAGRAM

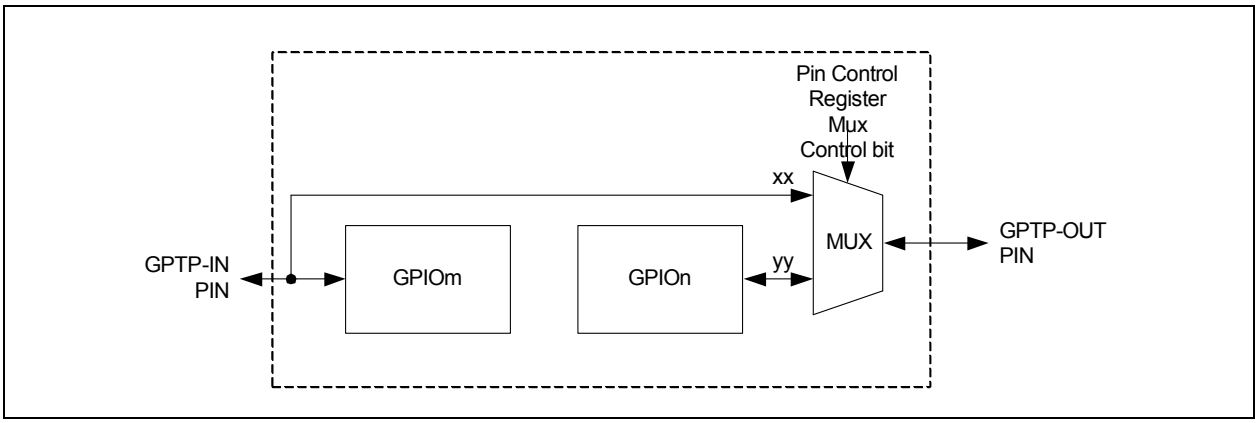


18.5 GPIO Pass-Through Ports

GPIO Pass-Through Ports (GPTP) can multiplex two general purpose I/O pins as shown in Figure 18-2. GPIO Pass-Through Ports connect the GPTP-IN pin to the GPTP-OUT pin. The GPTP are sequentially assigned values 0:7. The GPTP port assignment have no relation to the GPIO Indexing assignments. The GPTP ports are controlled by the Mux Control bits in the Pin Control Register associated with the GPTP-OUT signal function.

In order to enable the GPTP Pass-Through Mode, the GPTP-IN (GPIOm in Figure 18-2) Pin Control Register must assign the Mux Control to the GPTP_IN signal function and the GPIO Direction bit to 0 (input); the GPTP-OUT (GPIOn in Figure 18-2) Pin Control Register must assign the Mux Control to the GPTP_OUT signal function and the GPIO Direction bit to 1 (output). The GPTP-OUT signal function can differ from pin to pin.

FIGURE 18-2: GPIO PASS-THROUGH PORT EXAMPLE



The Pin Control Register Mux Control fields shown in Figure 18-2 are illustrated as ‘xx’ and ‘yy’ because this figure is an example, it does not represent the actual GPIO multiplexing configuration. The GPIO Multiplexing tables in this chapter must be used to determine the correct values to use to select between a GPIO and the pass-through.

When Pass-Through Mode is enabled, the GPIOn output is disconnected from the GPIOn pin and the GPIOm pin signal appears on GPIOn pin. Note that in this case the GPIOm input register still reflects the state of the GPIOm pin.

18.6 Accessing GPIOs

There are two ways to access GPIO output data. GPIO_OUTPUT_SELECT is used to determine which GPIO output data bit affects the GPIO output pin.

- Group Output GPIO Data
  - Outputs to individual GPIO ports are grouped into 32-bit GPIO Output Registers.
- Individual Output GPIO Data
  - Each GPIO output port may be individually accessible in the ALTERNATE_GPIO_DATA field of the port’s Pin Control Register. On reads, ALTERNATE_GPIO_DATA returns the programmed value, not the value on the pin.

There are two ways to access GPIO input data.

- Group Input GPIO Data
  - Inputs from individual GPIO ports are grouped into 32-bit GPIO Input Registers and always reflect the current state of the GPIO input from the pads, independent of the setting of the MUX_CONTROL field in the Pin Control Register.
- Group Input GPIO Data
  - Each GPIO input port is individually accessible in the GPIO_INPUT field of the port’s Pin Control Register. The GPIO_INPUT field always reflects the current state of GPIO input from the pad, independent of the setting of the MUX_CONTROL field in the Pin Control Register.

18.6.1 HOST ACCESS OF GPIOS

The GPIO Output Registers and GPIO Input Registers can be configured to be Host accessible via one of the SRAM Base Address Register, if the base of the internal address of the BAR is set to an offset of 200h from the GPIO base address, with a SIZE of 9, setting of block of 512 bytes. All of the Output and Input registers can then be accessed as offsets from the Host base address.

The GPIO Output and Input registers can also be accessed as one of the regions in an EMI block. This access is defined in the EMI Protocols chapter of the firmware specification.

18.7 GPIO Indexing

Each GPIO signal function name consists of a 4-character prefix (“GPIO”) followed by a 3-digit octal-encoded index number. In the MEC170x GPIO indexing is done sequentially starting from GPIO000.

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18.8 GPIO Multiplexing and Control Register Defaults

The default values for all GPIO Control Register and Control 2 Registers are shown in the GPIO Pin Control Registers Defaults Table in the GPIO Register Assignments Subsection of Section 3.0, "Device Inventory". The function multiplexing for each GPIO is shown in the GPIO Multiplexing Table in the same Subsection.

Note:	If a GPIO listed in the tables does not appear in the pin list of a particular device, then the Control Registers are reserved and should not be written. Similarly, if GPIO does not appear in the pin list then the bit position for the Input GPIO Register and Output GPIO Register that contains that GPIO is reserved.

18.9 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the GPIO Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 18-5: REGISTER SUMMARY

Offset	Register Name
000h - 2B3h	Pin Control Register for all GPIOs
300h	Input GPIO[000:036] Register
304h	Input GPIO[040:076] Register
308h	Input GPIO[100:136] Register
30Ch	Input GPIO[140:176] Register
310h	Input GPIO[200:236] Register
314h	Input GPIO[240:276] Register
380h	Output GPIO[000:036] Register
384h	Output GPIO[040:076] Register
388h	Output GPIO[100:136] Register
38Ch	Output GPIO[140:176] Register
390h	Output GPIO[200:236] Register
394h	Output GPIO[240:276] Register
500h - 7B3h	Pin Control 2 Register for all GPIOs

18.10 Pin Control Registers

Two Control Registers are implemented for each GPIO, the Pin Control Register and the Pin Control 2 Register.

18.10.1 PIN CONTROL REGISTER

Offset	See Section 18.8			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:25	Reserved	R	-	-
24	GPIO_INPUT Reads of this bit always return the state of GPIO input from the pad, independent of the Mux selection for the pin or the Direction, except as follows: 1. POWER_GATING = 11b - Input Disabled This bit is forced low when the input is disabled 2. POWER_GATING = 10b - Unpowered This bit is forced high when the pad is unpowered. 3. POWER_GATING = 01b - VCC Main Power Rail This bit is forced high when VCC_PWRGD is low.	R	x	RESET_SYS

Offset	See Section 18.8			
Bits	**Description**	**Type**	**Default**	**Reset Event**
23:17	Reserved	R	-	-
16	ALTERNATE_GPIO_DATA Reads of this bit always return the last data written to the GPIO output data register bit; reads do not return the current output value of the GPIO pin if it is configured as an output. If the GPIO_OUTPUT_SELECT bit in this register is '1', then this bit is Read Only and the GPIO output data register bit is only written by the GPIO Output Register. If the GPIO_OUTPUT_SELECT bit in this register is '0', then this bit is R/W, and the bit corresponding to this GPIO in the GPIO Output Register is Read Only.	R or R/W	See Section 18.8	RESET_SYS
15:14	Reserved	R	-	-
13:12	MUX_CONTROL The Mux Control field determines the active signal function for a pin. 11b=Signal Function 3 Selected 10b=Signal Function 2 Selected 01b=Signal Function 1 Selected 00b=GPIO Function Selected	R/W	See Section 18.8	RESET_SYS
11	POLARITY When the Polarity bit is set to '1' and the MUX_CONTROL bits are greater than '00,' the selected signal function outputs are inverted and Interrupt Detection sense defined in Table 18-6, "Edge Enable and Interrupt Detection Bits Definition" is inverted. When the MUX_CONTROL field selects the GPIO signal function (Mux='00'), the Polarity bit does not effect the output. Regardless of the state of the MUX_CONTROL field and the Polarity bit, the state of the pin is always reported without inversion in the GPIO input register. 1=Inverted 0=Non-inverted	R/W	See Section 18.8	RESET_SYS
10	GPIO_OUTPUT_SELECT This control bit determines which register is used to update the data register for GPIO outputs. See Section 18.4, "Description" 1=GPIO output data for this GPIO come from the bit representing this GPIO in the GPIO Output Register; writes to the ALTERNATE_GPIO_DATA field of this register do not affect the GPIO 0=GPIO output data for this GPIO come from the ALTERNATE_GPIO_DATA field of this register; writes to the bit representing this GPIO in the GPIO Output Register do not affect the GPIO	R/W	See Section 18.8	RESET_SYS
9	GPIO_DIRECTION This bit controls the buffer direction only when the MUX_CONTROL field is '00' selecting the pin signal function to be GPIO. When the MUX_CONTROL field is greater than '00' (i.e., a non-GPIO signal function is selected) this bit has no affect and the selected signal function logic directly controls the pin direction. 1=Output 0=Input	R/W	See Section 18.8	RESET_SYS

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Offset	See Section 18.8			
Bits	**Description**	**Type**	**Default**	**Reset Event**
8	OUTPUT_BUFFER_TYPE Unless explicitly stated otherwise, pins with (I/O/OD) or (O/OD) in their buffer type column in the tables in are compliant with the following Programmable OD/PP Multiplexing Design Rule: Each compliant pin has a programmable open drain/push-pull buffer controlled by the Output Buffer Type bit in the associated Pin Control Register. The state of this bit controls the mode of the interface buffer for all selected functions, including the GPIO function. 1=Open Drain 0=Push-Pull	R/W	See Section 18.8	RESET_SYS
7	EDGE_ENABLE When combined with the field INTERRUPT_DETECTION in this register, determines the interrupt capability of the GPIO input. See Table 18-6, "Edge Enable and Interrupt Detection Bits Definition" for details. 1=Edge detection enabled 0=Edge detection disabled	R/W	See Section 18.8	RESET_SYS
6:4	INTERRUPT_DETECTION When combined with the field INTERRUPT_DETECTION in this register, determines the interrupt capability of the GPIO input. See Table 18-6, "Edge Enable and Interrupt Detection Bits Definition" for details.	R/W	See Section 18.8	RESET_SYS
3:2	POWER_GATING The GPIO pin will be tristated when the selected power well is off. 11b=VTR Powered Output Only. Input pad is disabled and output will be tristated when VTR Power Rail is off. 10b=Unpowered. The GPIO pad is turned off completely. Both the input buffer and output buffer on the pad are disabled. Pull-up and pull-down resisters are disabled independent of the setting of the PU/PD field 01b=VCC Main Power Rail (as determined by the VCC_PWRGD input) 00b=VTR Power Rail **Note:** The Under Voltage Support feature requires that this bit field be set to the 11b option, VTR Powered Output Only, when pad VTR=3.3V and pin is driving out to 1.8V using Open Drain Mode.	R/W	See Section 18.8	RESET_SYS
1:0	PU/PD These bits are used to enable an internal pull-up or pull-down resistor. 11b=”Keeper Mode”. In this mode a weak latch circuit holds the last value on a pad when it becomes tri-stated and undriven 10b=Pull Down Enabled 01b=Pull Up Enabled 00b=None	R/W	See Section 18.8	RESET_SYS

TABLE 18-6: EDGE ENABLE AND INTERRUPT DETECTION BITS DEFINITION

Edge Enable	Interrupt Detection Bits			Selected Function
D7	D6	D5	D4	
0	0	0	0	Low Level Sensitive
0	0	0	1	High Level Sensitive
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Interrupt events are disabled
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	1	0	1	Rising Edge Triggered
1	1	1	0	Falling Edge Triggered
1	1	1	1	Either edge triggered

Note: Only edge triggered interrupts can wake up the main clock domain. The GPIO must be enabled for edge-triggered interrupts and the GPIO interrupt must be enabled in the interrupt aggregator in order to wake from the Heavy Sleep state.

18.10.2 PIN CONTROL 2 REGISTER

Offset	See Section 18.8			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:6	Reserved	R	-	-
5:4	DRIVE_STRENGTH These bits are used to select the drive strength on the pin. The drive strength is the same whether the pin is powered by 3.3V or 1.8V. 11b=12mA 10b=8mA 01b=4mA 00b=2mA	R/W	See Section 18.8	RESET_SYS
3:1	Reserved	R	-	-
0	SLEW_RATE This bit is used to select the slew rate on the pin. 1=fast 0=slow (half frequency)	R/W	0h	RESET_SYS

18.10.3 GPIO INPUT REGISTERS

The GPIO Input Registers can always be used to read the state of a pin, even when the pin is configured as an output, /or when the pin is configured for a signal function other than the GPIO (i.e., the MUX_CONTROL field is not equal to '00.').

Note: Bits associated with GPIOs not present in the pinout for a particular device are Reserved.

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18.10.3.1 Input GPIO[000:036] Register

Offset	300h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[036:030] Input	R	00h	RESET_SYS
23:16	GPIO[027:020] Input	R	00h	RESET_SYS
15:8	GPIO[017:010] Input	R	00h	RESET_SYS
7:0	GPIO[007:000] Input	R	00h	RESET_SYS

18.10.3.2 Input GPIO[040:076] Register

Offset	304h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[076:070] Input	R	00h	RESET_SYS
23:16	GPIO[067:060] Input	R	00h	RESET_SYS
15:8	GPIO[057:050] Input	R	00h	RESET_SYS
7:0	GPIO[047:040] Input	R	00h	RESET_SYS

18.10.3.3 Input GPIO[100:136] Register

Offset	308h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[136:130] Input	R	00h	RESET_SYS

Offset	308h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
23:16	GPIO[127:120] Input	R	00h	RESET_SYS
15:8	GPIO[117:110] Input	R	00h	RESET_SYS
7:0	GPIO[107:100] Input	R	00h	RESET_SYS

18.10.3.4 Input GPIO[140:176] Register

Offset	30Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[176:170] Input	R	00h	RESET_SYS
23:16	GPIO[167:160] Input	R	00h	RESET_SYS
15:8	GPIO[157:150] Input	R	00h	RESET_SYS
7:0	GPIO[147:140] Input	R	00h	RESET_SYS

18.10.3.5 Input GPIO[200:236] Register

Offset	310h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[236:230] Input	R/W	00h	RESET_SYS
23:16	GPIO[227:220] Input	R/W	00h	RESET_SYS
15:8	GPIO[217:210] Input	R/W	00h	RESET_SYS
7:0	GPIO[207:200] Input	R/W	00h	RESET_SYS

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18.10.3.6 Input GPIO[240:276] Register

Offset	314h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[276:270] Input	R/W	00h	RESET_SYS
23:16	GPIO[267:260] Input	R/W	00h	RESET_SYS
15:8	GPIO[257:250] Input	R/W	00h	RESET_SYS
7:0	GPIO[247:240] Input	R/W	00h	RESET_SYS

18.10.4 GPIO OUTPUT REGISTERS

If enabled by the GPIO_OUTPUT_SELECT bit, the GPIO Output bits determine the level on the GPIO pin when the pin is configured for the GPIO output function. If the GPIO Output Register bit is not enabled, its value does not affect the GPIO pin. In all cases, reads return the last programmed value in the GPIO Output Register.

Note: Bits associated with GPIOs not present in the pinout for a particular device are Reserved.

18.10.4.1 Output GPIO[000:036] Register

Offset	380h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[036:030] Output	R/W	00h	RESET_SYS
23:16	GPIO[027:020] Output	R/W	00h	RESET_SYS
15:8	GPIO[017:010] Output	R/W	00h	RESET_SYS
7:0	GPIO[007:000] Output	R/W	00h	RESET_SYS

18.10.4.2 Output GPIO[040:076] Register

Offset	384h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:24	Reserved	R	-	-
30:24	GPIO[076:070] Output	R/W	00h	RESET_SYS
23:16	GPIO[067:060] Output	R/W	00h	RESET_SYS
15:8	GPIO[057:050] Output	R/W	00h	RESET_SYS
7:0	GPIO[047:040] Output	R/W	00h	RESET_SYS

18.10.4.3 Output GPIO[100:136] Register

Offset	388h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[136:130] Output	R/W	00h	RESET_SYS
23:16	GPIO[127:120] Output	R/W	00h	RESET_SYS
15:8	GPIO[117:110] Output	R/W	00h	RESET_SYS
7:0	GPIO[107:100] Output	R/W	00h	RESET_SYS

18.10.4.4 Output GPIO[140:176] Register

Offset	38Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:22	Reserved	R	-	-
30:24	GPIO[176:170] Output	R/W	00h	RESET_SYS

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Offset	38Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
23:16	GPIO[175:160] Output	R/W	00h	RESET_SYS
15:8	GPIO[157:150] Output	R/W	00h	RESET_SYS
7:0	GPIO[147:140] Output	R/W	00h	RESET_SYS

18.10.4.5 Output GPIO[200:236] Register

Offset	390h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[236:230] Output	R/W	00h	RESET_SYS
23:16	GPIO[227:220] Output	R/W	00h	RESET_SYS
15:8	GPIO[217:210] Output	R/W	00h	RESET_SYS
7:0	GPIO[207:200] Output	R/W	00h	RESET_SYS

18.10.4.6 Output GPIO[240:276] Register

Offset	390h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[276:270] Output	R/W	00h	RESET_SYS
23:16	GPIO[267:260] Output	R/W	00h	RESET_SYS

Offset	390h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:8	GPIO[257:250] Output	R/W	00h	RESET_SYS
7:0	GPIO[247:240] Output	R/W	00h	RESET_SYS

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19.0 WATCHDOG TIMER (WDT)

19.1 Introduction

The function of the Watchdog Timer is to provide a mechanism to detect if the internal embedded controller has failed.

When enabled, the Watchdog Timer (WDT) circuit will generate a WDT Event if the user program fails to reload the WDT within a specified length of time known as the WDT Interval.

19.2 References

No references have been cited for this chapter.

19.3 Terminology

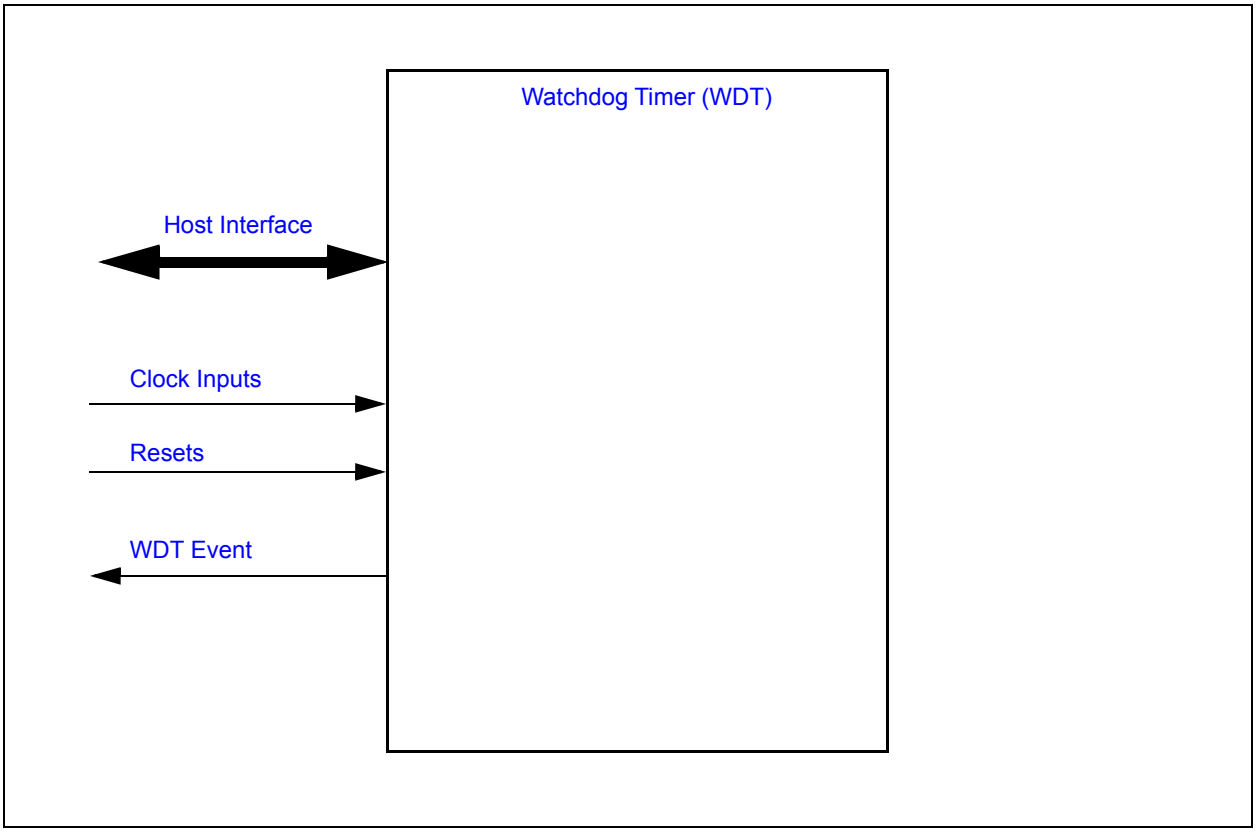
There is no terminology defined for this chapter.

19.4 Interface

This block is designed to be accessed internally via a registered host interface or externally via the signal interface.

19.5 Host Interface

FIGURE 19-1: I/O DIAGRAM OF BLOCK



The registers defined for the Watchdog Timer (WDT) are accessible by the embedded controller as indicated in Section 19.8, "EC Registers". All registers accesses are synchronized to the host clock and complete immediately. Register reads/writes are not delayed by the 32KHz.

19.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

19.6.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block reside on this single power well.

19.6.2 CLOCK INPUTS

Name	Description
32KHz	The 32KHz clock input is the clock source to the Watchdog Timer functional logic, including the counter.

19.6.3 RESETS

TABLE 19-1: RESET INPUTS

Name	Description
RESET_SYS	Power on Reset to the block. This signal resets all the register and logic in this block to its default state following a POR or a WDT Event event.
RESET_SYS_nWDT	This reset signal is used on WDT registers/bits that need to be preserved through a WDT Event.

TABLE 19-2: RESET OUTPUTS

Source	Description
WDT Event	Pulse generated when WDT expires. This signal is used to reset the embedded controller and its subsystem. The event is cleared after a RESET_SYS.

19.7 Description

19.7.1 WDT OPERATION

19.7.1.1 WDT Activation Mechanism

The WDT is activated by the following sequence of operations during normal operation:

1. Load the WDT Load Register with the count value.
2. Set the WDT_ENABLE bit in the WDT Control Register.

The WDT Activation Mechanism starts the WDT decrementing counter.

19.7.1.2 WDT Deactivation Mechanism

The WDT is deactivated by the clearing the WDT_ENABLE bit in the WDT Control Register. The WDT Deactivation Mechanism places the WDT in a low power state in which clock are gated and the counter stops decrementing.

19.7.1.3 WDT Reload Mechanism

The WDT must be reloaded within periods that are shorter than the programmed watchdog interval; otherwise, the WDT will underflow and a WDT Event will be generated and the WDT bit in Power-Fail and Reset Status Register on page 564 will be set. It is the responsibility of the user program to continually execute code which reloads the watchdog timer, causing the counter to be reloaded.

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There are three methods of reloading the WDT: a write to the WDT Load Register, a write to the WDT Kick Register, or WDT event.

19.7.1.4 WDT Interval

The WDT Interval is the time it takes for the WDT to decrements from the WDT Load Register value to 0000h. The WDT Count Register value takes 33/32KHz seconds (ex. 33/32.768 KHz = 1.007ms) to decrement by 1 count.

19.7.1.5 WDT STALL Operation

There are three STALL_ENABLE inputs to the WDT, each of which is connected to an internal signal. If enabled, and the STALL event is asserted, the WDT stops decrementing, and the WDT enters a low power state. When a WDT STALL event is de-asserted, the counter continues decrementing from the value it had when the STALL was asserted.

19.8 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Watchdog Timer (WDT) Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 19-3: REGISTER SUMMARY

Offset	Register Name
00h	WDT Load Register
04h	WDT Control Register
08h	WDT Kick Register
0Ch	WDT Count Register

19.8.1 WDT LOAD REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:0	WDT_LOAD Writing this field reloads the Watch Dog Timer counter.	R/W	FFFFh	RESET_SYS

19.8.2 WDT CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:5	Reserved	R	-	-
4	JTAG_STALL This bit enables the WDT Stall function if JTAG or SWD debug functions are active 1=The WDT is stalled while either JTAG or SWD is active 0=The WDT is not affected by the JTAG debug interface	R/W	0b	RESET_SYS
3	WEEK_TIMER_STALL This bit enables the WDT Stall function if the Week Timer is active. 1=The WDT is stalled while the Week Timer is active 0=The WDT is not affected by the Week Timer	R/W	0b	RESET_SYS
2	HIBERNATION_TIMER0_STALL This bit enables the WDT Stall function if the Hibernation Timer 0 is active. 1=The WDT is stalled while the Hibernation Timer 0 is active 0=The WDT is not affected by Hibernation Timer 0	R/W	0b	RESET_SYS
1	TEST	R	0b	RESET_SYS
0	WDT_ENABLE In WDT Operation, the WDT is activated by the sequence of operations defined in Section 19.7.1.1, "WDT Activation Mechanism" and deactivated by the sequence of operations defined in Section 19.7.1.2, "WDT Deactivation Mechanism". 1=block enabled 0=block disabled	R/W	0b	RESET_SYS

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19.8.3 WDT KICK REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	KICK The WDT Kick Register is a strobe. Reads of this register return 0. Writes to this register cause the WDT to reload the WDT Load Register value and start decrementing when the WDT_ENABLE bit in the WDT Control Register is set to '1'. When the WDT_ENABLE bit in the WDT Control Register is cleared to '0', writes to the WDT Kick Register have no effect.	W	n/a	RESET_SYS

19.8.4 WDT COUNT REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:0	WDT_COUNT This read-only register provide the current WDT count.	R	FFFFh	RESET_SYS-_nWDT

20.0 BASIC TIMER

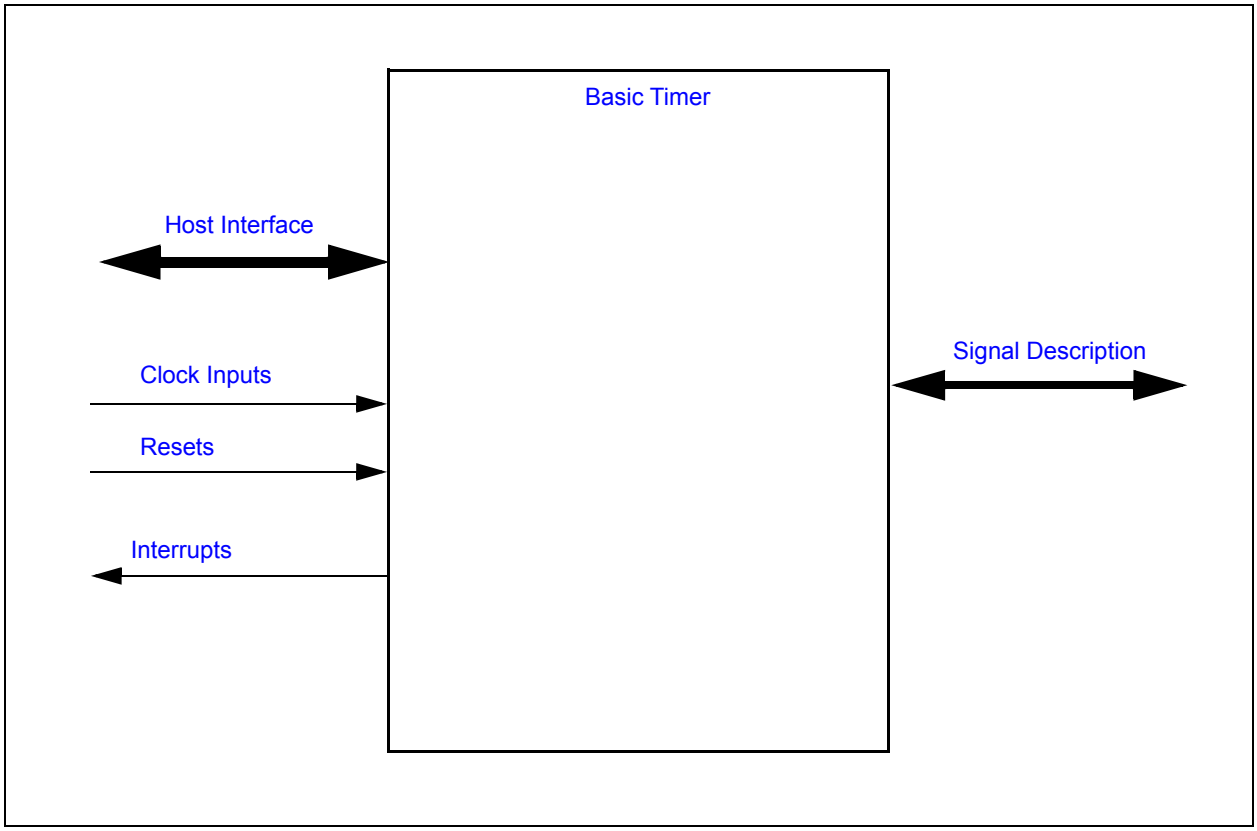
20.1 Introduction

This timer block offers a simple mechanism for firmware to maintain a time base. This timer may be instantiated as 16 bits or 32 bits. The name of the timer instance indicates the size of the timer.

20.2 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 20-1: I/O DIAGRAM OF BLOCK



20.3 Signal Description

There are no external signals for this block.

20.4 Host Interface

The embedded controller may access this block via the registers defined in Section 20.9, "EC Registers".

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20.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

20.5.1 POWER DOMAINS

TABLE 20-1: POWER SOURCES

Name	Description
VTR	The timer control logic and registers are all implemented on this single power domain.

20.5.2 CLOCK INPUTS

TABLE 20-2: CLOCK INPUTS

Name	Description
48MHz	This is the clock source to the timer logic. The Pre-scaler may be used to adjust the minimum resolution per bit of the counter.

20.5.3 RESETS

TABLE 20-3: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal, which is an input to this block, resets all the logic and registers to their initial default state.
Soft Reset	This reset signal, which is created by this block, resets all the logic and registers to their initial default state. This reset is generated by the block when the **SOFT_RESET** bit is set in the Timer Control Register register.
RESET_Timer	This reset signal, which is created by this block, is asserted when either the RESET_SYS or the Soft Reset signal is asserted. The RESET_SYS and Soft Reset signals are OR'd together to create this signal.

20.6 Interrupts

TABLE 20-4: EC INTERRUPTS

Source	Description
TIMER_16_*x*	This interrupt event fires when a 16-bit timer *x* reaches its limit. • If configured to count up, the limit is triggered when the counter wraps from FFFFh to 0h • If configured to count down, the limit is triggered when the counter wraps from 0h to FFFFh. This event is sourced by the EVENT_INTERRUPT status bit if enabled.
TIMER_32_*x*	This interrupt event fires when a 32-bit timer *x* reaches its limit. • If configured to count up, the limit is triggered when the counter wraps from FFFF_FFFFh to 0h • If configured to count down, the limit is triggered when the counter wraps from 0h to FFFF_FFFFh. This event is sourced by the EVENT_INTERRUPT status bit if enabled.

20.7 Low Power Modes

The Basic Timer may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry. This block is only be permitted to enter low power modes when the block is not active.

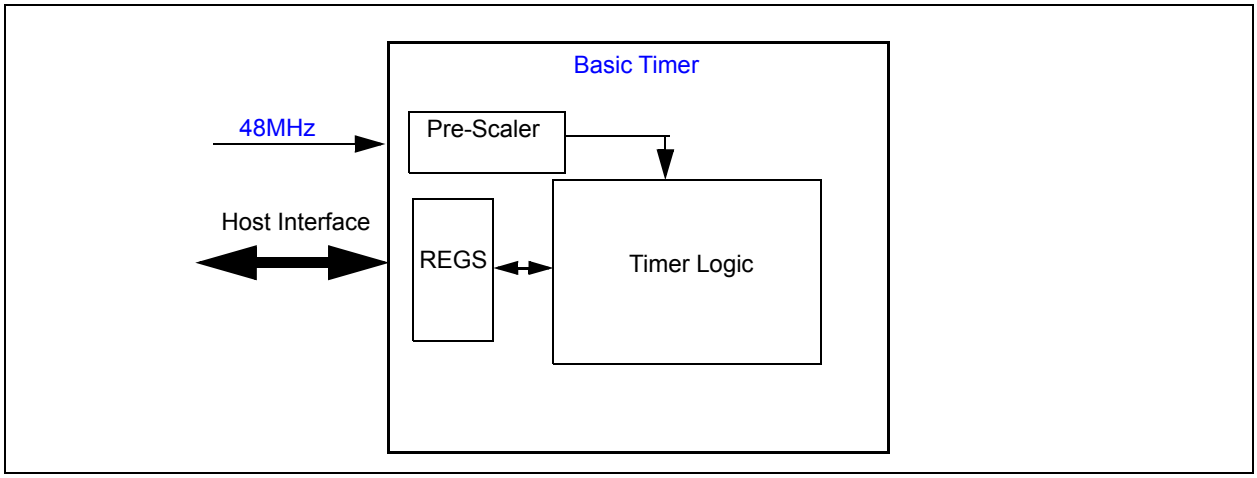
The sleep state of this timer is as follows:

- Asleep while the block is not Enabled
- Asleep while the block is not running (start inactive).
- Asleep while the block is halted (even if running).

The block is active while start is active.

20.8 Description

FIGURE 20-2: BLOCK DIAGRAM



This timer block offers a simple mechanism for firmware to maintain a time base in the design. The timer may be enabled to execute the following features:

- Programmable resolution per LSB of the counter via the Pre-scale bits in the Timer Control Register
- Programmable as either an up or down counter
- One-shot or Continuous Modes
- In one-shot mode the Auto Restart feature stops the counter when it reaches its limit and generates a level event.
- In Continuous Mode the Auto Restart feature restarts that counter from the programmed preload value and generates a pulse event.
- Counter may be reloaded, halted, or started via the Timer Control register
- Block may be reset by either a Power On Reset (POR) or via a Soft Reset.

20.9 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Basic Timer Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 20-5: REGISTER SUMMARY

Offset	Register Name
00h	Timer Count Register
04h	Timer Preload Register
08h	Timer Status Register
0Ch	Timer Int Enable Register
10h	Timer Control Register

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20.9.1 TIMER COUNT REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COUNTER This is the value of the Timer counter. This is updated by Hardware but may be set by Firmware. If it is set by firmware while the Hardware Timer is operating, functionality cannot be assured. When read, it is buffered so single byte reads will be able to catch the full 4 byte register without it changing. The size of the Counter is indicated by the instance name (e.g., 16-bit Basic Timer -> SIZE=16). Bits 0 to (SIZE-1) are r/w counter bits. Bits 31 down to SIZE are unused and should be set to zero when writing this register.	R/W	0h	RESET_Timer

20.9.2 TIMER PRELOAD REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	PRE_LOAD This is the value of the Timer pre-load for the counter. This is used by H/W when the counter is to be restarted automatically; this will become the new value of the counter upon restart. The size of the Pre-Load value is the same as the size of the counter. The size of the Counter is indicated by the instance name (e.g., 16-bit Basic Timer -> SIZE=16). Bits 0 to (SIZE-1) are r/w pre-load bits. Bits 31 down to SIZE are unused and should be set to zero when writing this register.	R/W	0h	RESET_Timer

20.9.3 TIMER STATUS REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	Reserved	R	-	-
0	EVENT_INTERRUPT This is the interrupt status that fires when the timer reaches its limit. This may be level or a self clearing signal cycle pulse, based on the AUTO_RESTART bit in the Timer Control Register. If the timer is set to automatically restart, it will provide a pulse, otherwise a level is provided.	R/WC	0h	RESET_Timer

20.9.4 TIMER INT ENABLE REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	Reserved	R	-	-
0	EVENT_INTERRUPT_ENABLE This is the interrupt enable for the status EVENT_INTERRUPT bit in the Timer Status Register	R/W	0h	RESET_Timer

20.9.5 TIMER CONTROL REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	PRE_SCALE This is used to divide down the system clock through clock enables to lower the power consumption of the block and allow slow timers. Updating this value during operation may result in erroneous clock enable pulses until the clock divider restarts. The number of clocks per clock enable pulse is (Value + 1); a setting of 0 runs at the full clock speed, while a setting of 1 runs at half speed.	R/W	0h	RESET_Timer
15:8	Reserved	R	-	-
7	HALT This is a halt bit. This will halt the timer as long as it is active. Once the halt is inactive, the timer will start from where it left off. 1=Timer is halted. It stops counting. The clock divider will also be reset. 0=Timer runs normally	R/W	0h	RESET_Timer
6	RELOAD This bit reloads the counter without interrupting it operation. This will not function if the timer has already completed (when the START bit in this register is ‘0’). This is used to periodically prevent the timer from firing when an event occurs. Usage while the timer is off may result in erroneous behavior.	R/W	0h	RESET_Timer

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Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
5	START This bit triggers the timer counter. The counter will operate until it hits its terminating condition. This will clear this bit. It should be noted that when operating in restart mode, there is no terminating condition for the counter, so this bit will never clear. Clearing this bit will halt the timer counter. Setting this bit will: • Reset the clock divider counter. • Enable the clock divider counter. • Start the timer counter. • Clear all interrupts. Clearing this bit will: • Disable the clock divider counter. • Stop the timer counter.	R/W	0h	RESET_Timer
4	SOFT_RESET This is a soft reset. This is self clearing 1 cycle after it is written. Firmware does not need to wait before reconfiguring the Basic Timer following soft reset.	WO	0h	RESET_Timer
3	AUTO_RESTART This will select the action taken upon completing a count. 1=The counter will automatically restart the count, using the contents of the Timer Preload Register to load the Timer Count Register The interrupt will be set in edge mode 0=The counter will simply enter a done state and wait for further control inputs. The interrupt will be set in level mode.	R/W	0h	RESET_Timer
2	COUNT_UP This selects the counter direction. When the counter in incrementing the counter will saturate and trigger the event when it reaches all F's. When the counter is decrementing the counter will saturate when it reaches 0h. 1=The counter will increment 0=The counter will decrement **Note:** Counter will saturate when it reaches the max count, which is dependent on the size of the counter. Examples: 16-bit timer 0=saturate and transition from 00h to FFh 1=saturate and transition from FFh to 00h 32-bit timer 0=saturate and transition from 0000h to FFFFh 1=saturate and transition from FFFFh to 0000h	R/W	0h	RESET_Timer

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	Reserved	R	-	-
0	ENABLE This enables the block for operation. 1=This block will function normally 0=This block will gate its clock and go into its lowest power state	R/W	0h	RESET_Timer

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21.0 16-BIT COUNTER-TIMER INTERFACE

21.1 Introduction

The 16-Bit Counter-Timer Interface implements four 16-bit auto-reloading timer/counters. The clock for each timer/counter is derived from the system clock and can be divided down by a prescaler. Input-Only and Input/Output timers can also use an external input pin to clock or gate the counter. To aid operation in noisy environments the external input pin also has a selectable noise filter. If large counts are required, the output of each timer/counter can be internally connected to the next timer/counter.

21.2 References

No references have been cited for this feature.

21.3 Terminology

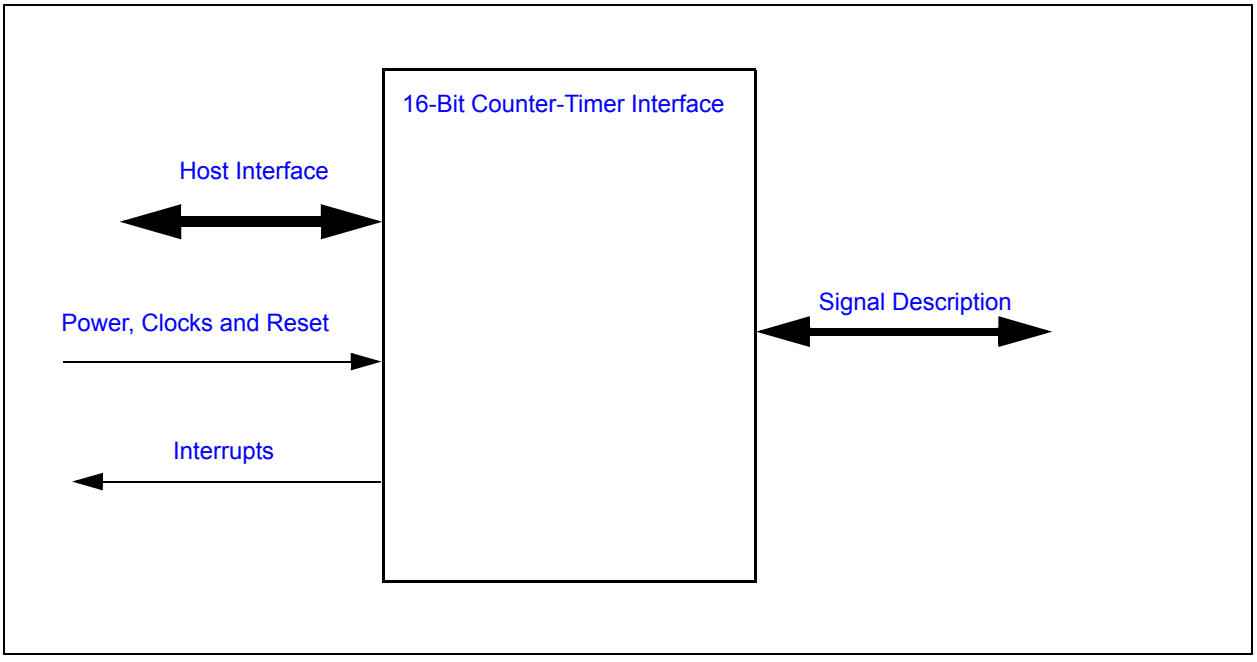
TABLE 21-1: TERMINOLOGY

Term	Definition
Overflow	When the timer counter transitions from FFFFh to 0000h
Underflow	When the timer counter transitions from 0000h to FFFFh.
Timer Tick Rate	This is the rate at which the timer is incremented or decremented.

21.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 21-1: I/O DIAGRAM OF BLOCK



21.5 Signal Description

TABLE 21-2: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
TINx	INPUT	Timer x Input signal
TOUTx	OUTPUT	Timer x Output signal

21.6 Host Interface

The registers defined for 16-bit Timers are accessible by the various hosts as indicated in Section 21.11, "EC Registers".

21.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

21.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

21.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for this block.

21.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.
Soft Reset	This reset signal, which is created by this block, resets all the logic and registers to their initial default state. This reset is generated by the block when the RESET bit is set in the Timer x Control Register.
Reset_Timer	This reset signal, which is created by this block, is asserted when either the RESET_SYS or the Soft Reset signal is asserted. The RESET_SYS and Soft Reset signals are OR'd together to create this signal.

21.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
TIMER*x*	This interrupt event fires when a 16-bit timer *x* overflows or underflows.

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21.9 Low Power Modes

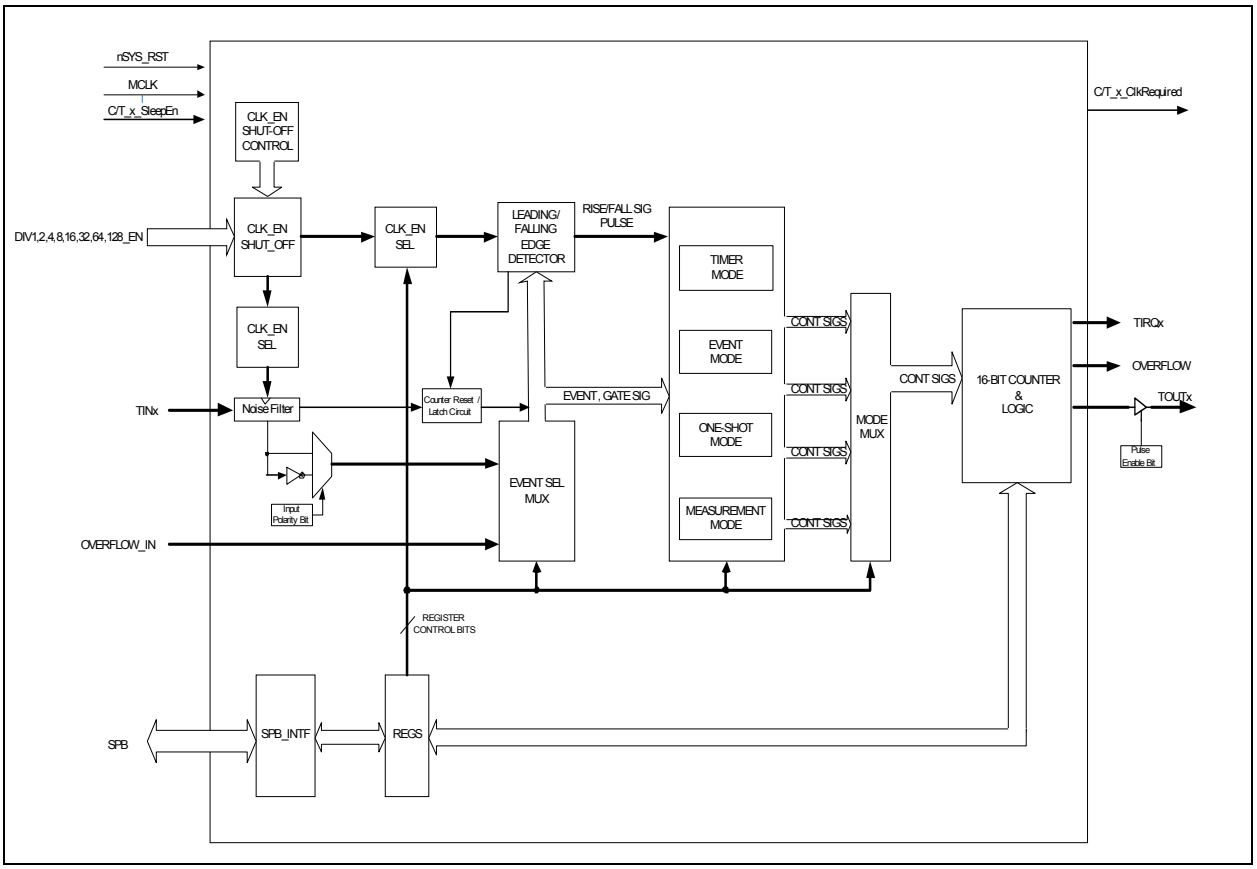
The 16-bit Timer may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry. This block is only be permitted to enter low power modes when the block is not active. The block is inactive in the following conditions:

- The block is not running (ENABLE de-asserted)
- The block is powered down (PD asserted).

The timer requires one Timer Clock period to halt after receiving a Sleep_En signal. When the block returns from sleep, if enabled, it will be restarted from the preload value.

21.10 Description

FIGURE 21-2: BLOCK DIAGRAM FOR TIMER X



The 16-bit Timer consists of a 16-bit counter, clocked by a by a configurable Timer Clock. The Timer can operate in any of 4 Modes: Timer Mode, Event Mode, One-Shot Mode, and Measurement Mode. The Timer can be used to generate an interrupt to the EC. Depending on the mode, the Timer can also generate an output signal.

21.10.1 TIMER CLOCK

Any of the frequencies listed in Table 21-3 may be used as the time base for the 16-bit counter.

TABLE 21-3: TIMER CLOCK FREQUENCIES

Timer Clock Select	Frequency Divide Select	Frequency Selected
0000b	Divide by 1	48MHz
0001b	Divide by 2	24MHz
0010b	Divide by 4	12MHz

TABLE 21-3: TIMER CLOCK FREQUENCIES (CONTINUED)

Timer Clock Select	Frequency Divide Select	Frequency Selected
0011b	Divide by 8	6MHz
0100b	Divide by 16	3MHz
0101b	Divide by 32	1.5MHz
0110b	Divide by 64	750KHz
0111b	Divide by 128	375KHz
1xxxb	Reserved	Reserved

For the Timer Clock, the **Timer Clock Select** value is defined by the TCLK field in the Timer x Clock and Event Control Register

21.10.2 FILTER CLOCK AND NOISE FILTER

The noise filter uses the Filter Clock (FCLK) to filter the signal on the TINx pins. for Event Mode and One-Shot Mode.

In Event Mode, the Event input is synchronized to FCLK and (if enabled) filtered by a three stage filter. The resulting recreated clock is used to clock the timer in Event mode. In Bypass Mode, configured by the FILTER_BYPASS bit in the Timer x Control Register, the pulse width of the external signal must be at least 2x the pulse width of the FCLK source. In Filter Mode, the pulse width of the external signal must be at least 4x the pulse width of the sync and filter clock

In One-Shot mode, the TIN duration could be smaller than a TCLK period. The filtered signal is latched until the signal is seen in the TCLK domain. This also applies in the filter bypass mode

Frequencies for the Filter Clock are the as those available for the Timer Clock, and are listed in Table 21-3. For the Filter Clock, the **Timer Clock Select** value is defined by the FCLK field in the Timer x Clock and Event Control Register. The choice of frequency is independent of the value chosen for the Timer Clock.

21.10.3 TIMER CONNECTIONS

For external inputs/outputs (TINx/TOUTx) to/from timers, please see Pin Configuration chapter for a description of the 16-bit Counter/Timer Interface.

TABLE 21-4: TIMER CASCADING DESCRIPTION

Timer Name	Timer Type	Over-Flow/ Under-flow Input's Connection
Timer 0	General Purpose	from Timer 3
Timer 1	General Purpose	from Timer 0
Timer 2	General Purpose	from Timer 1
Timer 3	General Purpose	from Timer 2

Note: The cascading connections are independent of the TINx/TOUTx connections.

21.10.4 STARTING AND STOPPING

The 16-bit timers can be started and stopped by setting and clearing the ENABLE bit in the Timer x Control Register in all modes, except one-shot.

21.10.5 TIMER MODE

Timer mode is used to generate periodic interrupts to the EC. When operating in this mode the timer always counts down based on one of the internally generated clock sources. The Timer mode is selected by setting the Timer Mode Select bits in the Timer Control Register. See Section 21.11.1, "Timer x Control Register".

The period between timer interrupts and the width of the output pulse is determined by the speed of the clock source, the clock divide ratio and the value programmed into the Timer Reload Register. The timer clock source and clock rate are selected using the Clock Source Select bits (TCLK) in the Timer x Clock and Event Control Register. See Section 21.11.2, "Timer x Clock and Event Control Register".

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TABLE 21-5: TIMER MODE OPERATIONAL SUMMARY

Item	Description
Timer Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Filter Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Count Operation	Down Counter
Reload Operation	When the timer underflows: RLOAD = 1, timer reloads from Timer Reload Reg RLOAD = 0, timer rolls over to FFFFh.
Count Start Condition	UPDN = 0 (timer only mode): ENABLE = 1 UPDN = 1 (timer gate mode): ENABLE = 1 & TIN = 1;
Count Stop Condition	UPDN = 0=ENABLE = 0; UPDN = 1: (ENABLE= 0 | TIN = 0)
Interrupt Request Generation Timing	When timer underflows from 0000h to reload value (as determined by RLOAD) an interrupt is generated.
TINx Pin Function	Provides timer gate function
TOUTx Pin Function	TOUT toggles each time the timer underflows (if enabled).
Read From Timer	Current count value can be read by reading the Timer Count Register
Write to Preload Register	After the firmware writes to the Timer Reload Register asserting the RESET loads the timer with the new value programmed in the Timer Reload Register. Note: If the firmware does not assert RESET, the timer will automatically load the Timer Reload Register value when the timer underflows. When the timer is running, values written to the Timer Reload Register are written to the timer counter when the timer underflows. The assertion of Reset also copies the Timer Reload Register into the timer counter.
Selectable Functions	• Reload timer on underflow with programmed Preload value (Basic Timer) • Reload timer with FFFFh in Free Running Mode (Free-running Timer) • Timer can be started and stopped by the TINx input pin (Gate Function) • The TOUTx pin changes polarity each time the timer underflows (Pulse Output Function)

21.10.5.1 Timer Mode Underflow

The timer operating in Timer mode can underflow in two different ways. One method, the Reload mode shown in Figure 21-3, is to reload the value programmed into the Reload register and continue counting from this value. The second method, Free Running mode Figure 21-4, is to set the timer to FFFFh and continue counting from this value. The underflow behavior is controlled by the RLOAD bit in the Timer Control Register.

FIGURE 21-3: RELOAD MODE BEHAVIOR

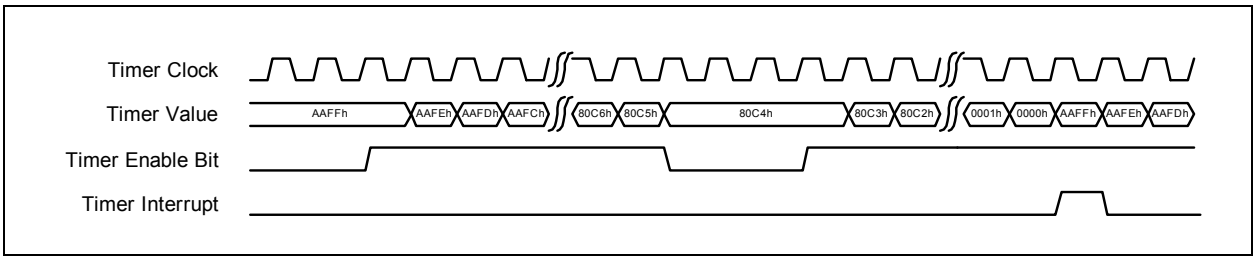
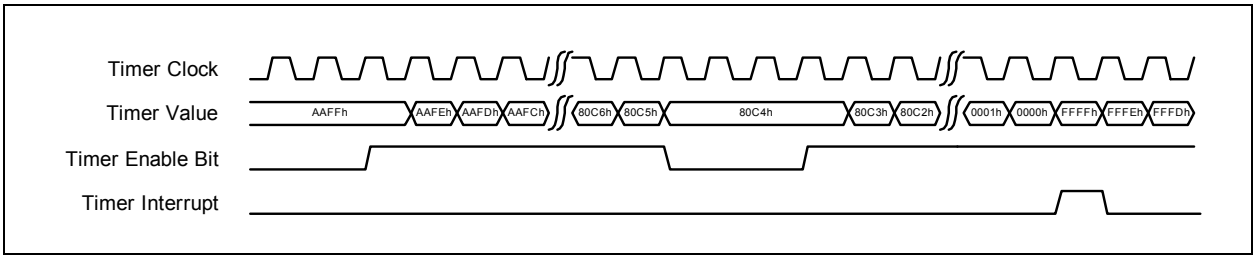


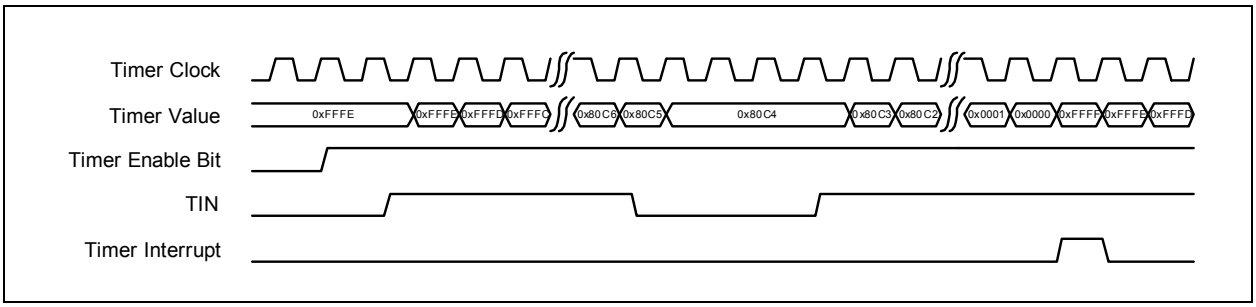
FIGURE 21-4: FREE RUNNING MODE BEHAVIOR



21.10.5.2 Timer Gate Function

The TIN pin on each timer can be used to pause the timer's operation when the timer is running. The timer will stop counting when the TIN pin is deasserted and count when the TIN pin is asserted. Figure 21-5 shows the timer behavior when the TIN pin is used to gate the timer function. The UPDN bit is used to enable and disable the Timer Gate function when in the Timer mode.

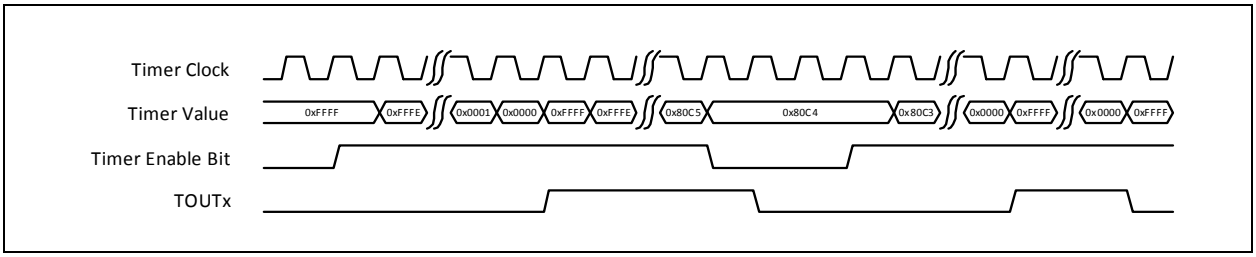
FIGURE 21-5: TIMER GATE OPERATION



21.10.5.3 Timer Mode Pulse Output

The four Timers can be used to generate a periodic output pulse. The output pulse changes state each time the timer underflows. The output is also cleared when the EN bit is cleared. Figure 21-6 shows the behavior of the TOUTx pin when it is used as a pulse output pin.

FIGURE 21-6: TIMER PULSE OUTPUT



21.10.6 EVENT MODE

Event mode is used to count events that occur external to the timer. The timer can be programmed to count the overflow output from the previous timer or an edge on the TIN pin. The direction the timer counts in Event mode is controlled by the UPDN bit in the Timer Control Register. When the timer is in Event mode, the TOUTx signal can be used to generate a periodic output pulse when the timer overflows or underflows. Figure 21-6 illustrates the pulse output behavior of the TOUTx pin in event mode when the timer underflows.

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The timer can be programmed using the Clock and Event Control register to respond to the following events using the EVENT bits and the EDGE bits: rising edge of TINx, falling edge of TINx, rising and falling edge of TINx, rising edge of overflow input, falling edge of the overflow input, and the rising and falling edges of the overflow input.

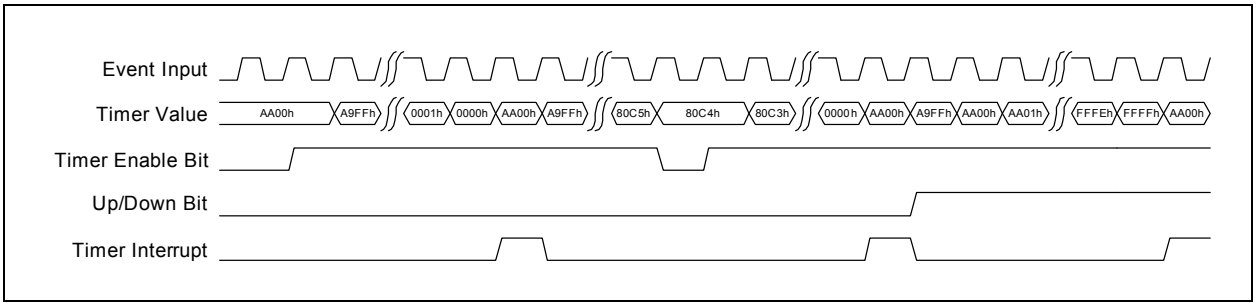
TABLE 21-6: EVENT MODE OPERATIONAL SUMMARY

Item	Description
Count Source	• External signal input to TINx pin (effective edge can be selected by software) • Timer x-1 overflow
Timer Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Filter Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Count Operation	Up/Down Counter
Reload Operation	• When the timer underflows: RLOAD = 1, timer reloads from Timer Reload Reg RLOAD = 0, timer rolls over to FFFFh. • When the timer overflows: RLOAD = 1, timer reloads from Timer Reload Reg RLOAD = 0, timer rolls over to 0000h.
Count Start Condition	Timer Enable is set (ENABLE = 1)
Count Stop Condition	Timer Enable is cleared (ENABLE = 0)
Interrupt Request Generation Timing	When timer overflows or underflows
TINx Pin Function	Event Generation
TOUTx Pin Function	TOUT toggles each time the timer underflows/overflows (if enabled).
Read From Timer	Current count value can be read by reading the Timer Count Register
Write to Preload Register	After the firmware writes to the Timer Reload Register, asserting the RESET loads the timer with the new value programmed in the Timer Reload Register. Note: If the firmware does not assert RESET, the timer will automatically load the Timer Reload Register value when the timer underflows.
Selectable Functions	• The direction of the counter is selectable via the UPDN bit. • Reload timer on underflow/overflow with programmed Preload value (Basic Timer) • Reload timer with FFFFh in Free Running Mode (Free-running Timer) • Pulse Output Function The TOUTx pin changes polarity each time the timer underflows or overflows.

21.10.6.1 Event Mode Operation

The timer starts counting events when the ENABLE bit in the Timer Control Register is set and continues to count until the ENABLE bit is cleared. When the ENABLE bit is set, the timer continues counting from the current value in the timer except after a reset event. After a reset event, the timer always starts counting from the value programmed in the Reload Register if counting down or from 0000h if counting up. Figure 21-7 shows an example of timer operation in Event mode. The RLOAD bit controls the behavior of the timer when it underflows or overflows.

FIGURE 21-7: EVENT MODE OPERATION



21.10.7 ONE-SHOT MODE

The One-Shot mode of the timer is used to generate a single interrupt to the EC after a specified amount of time. The timer can be configured to start using the ENABLE bit (Figure 21-8) or on a timer overflow event from the previous timer. See Section 21.11.2, "Timer x Clock and Event Control Register" for configuration details. The ENABLE bit must be set for an event to start the timer. The ENABLE bit is cleared one clock after the timer starts. The timer always starts from the value in the Reload Register and counts down in One-Shot mode.

TABLE 21-7: ONE SHOT MODE OPERATIONAL SUMMARY

Item	Description
Timer Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Filter Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Count Operation	Down Counter
Reload Operation	When the timer underflows the timer will stop. When the timer is enabled timer starts counting from value programmed in Timer Reload Register. (RLOAD has no effect in this mode)
Count Start Condition	Setting the ENABLE bit to 1 starts One-Shot mode. The timer clock automatically clears the enable bit one timer tick later. One-Shot mode may be enabled in Event Mode. In Event mode an overflow from the previous timer is used for timer tick rate.
Count Stop Condition	• Timer is reset (RESET = 1) • Timer underflows
Interrupt Request Generation Timing	When an underflow occurs.
TINx Pin Function	One Shot External input
TOUTx Pin Function	The TOUTx pin is asserted when the timer starts and de-asserted when the timer stops
Read From Timer	Current count value can be read by reading the Timer Count Register
Write to Preload Register	After the firmware writes to the Timer Reload Register, asserting the RESET loads the timer with the new value programmed in the Timer Reload Register. Note: If the firmware does not assert RESET, the timer will automatically load the Timer Reload Register value when the timer underflows.
Selectable Functions	• Pulse Output Function The TOUTx pin is asserted when the timer starts and de-asserted when the timer stops.

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FIGURE 21-8: TIMER START BASED ON ENABLE BIT

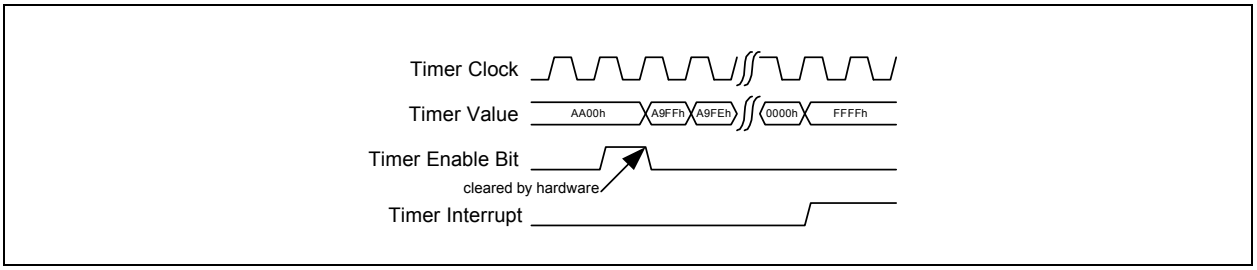


FIGURE 21-9: TIMER START BASED ON EXTERNAL EVENT

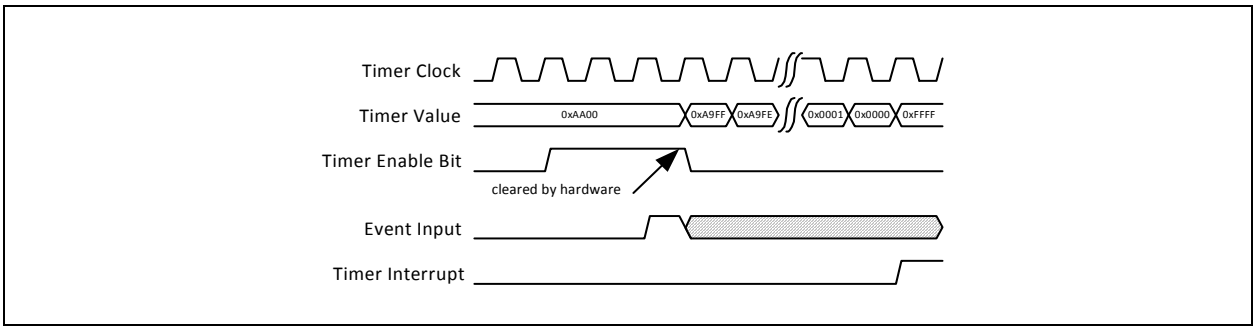
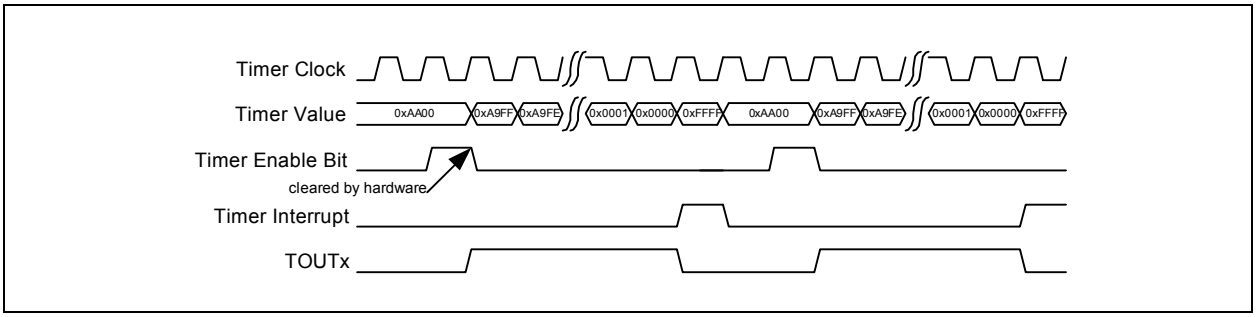


FIGURE 21-10: ONE SHOT TIMER WITH PULSE OUTPUT



21.10.8 MEASUREMENT MODE

The Measurement mode is used to measure the pulse width or period of an external signal. An interrupt to the EC is generated after each measurement or if the timer overflows and no measurement occurred. The timer measures the pulse width or period by counting the number of clock between edges on the TINx pin. The timer always stars counting at zero and counts up to 0xFFFF. The accuracy of the measurement depends on the speed of the clock being used. The speed of the clock also determines the maximum pulse width or period that can be detected.

TABLE 21-8: MEASUREMENT MODE OPERATIONAL SUMMARY

Item	Description
Timer Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"
Filter Clock Frequencies	This mode supports all the programmable frequencies listed in Table 21-3, "Timer Clock Frequencies"

TABLE 21-8: MEASUREMENT MODE OPERATIONAL SUMMARY (CONTINUED)

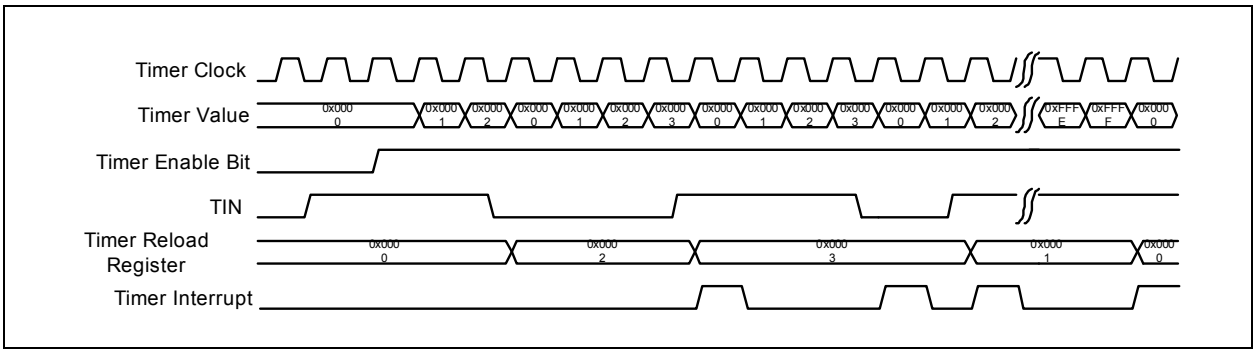
Item	Description
Count Operation	• Up Count • At measurement pulse's effective edge, the count value is transferred to the Timer Reload Register and the timer is loaded with 0000h and continues counting.
Count Start Condition	• Timer enable is set (ENABLE = 1)
Count Stop Condition	• Timer is reset (RESET = 1) • Timer overflows • Timer enable is cleared (ENABLE = 0)
Interrupt Request Generation Timing	• When timer overflows • When a measurement pulse's effective edge is input. (An interrupt is not generated on the first effective edge after the timer is started.)
TINx Pin Function	Programmable Input port or Measurement input
Read From Timer	When the Timer x Reload Register is read it indicates the measurement result from the last measurement made. The Timer x Reload Register reads 0000h if the timer overflows before a measurement is made.
Write to Timer	Timer x Reload Register is Read-Only in Measurement mode

21.10.8.1 Pulse Width Measurements

The timers measure pulse width by counting the number of timer clocks since the last rising or falling edge of the TINx input. To measure the pulse width of a signal on the TINx pin, the EDGE bits in the Clock and Event Control Register, must be set to start counting on rising and falling edges. The timer starts measuring on the next edge (rising or falling) on the TINx pin after the ENABLE bit is set. The Reload register stores the result of the last measurement taken. If the timer overflows, 0x0000 is written to the Reload register and the ENABLE bit is cleared stopping the timer. Figure 21-11 shows the timer behavior when measuring pulse widths.

The timer will not assert an interrupt in Pulse Measurement mode until the timer detects both a rising and a falling edge.

FIGURE 21-11: PULSE WIDTH MEASUREMENT



21.10.8.2 Period Measurements

The 16-bit timer measures the period of a signal by counting the number of timer clocks between either rising or falling edges of the TINx input. The measurement edge is determined by the EDGE bits in the Clock and Event Control Register. The timer starts measuring on the next edge (rising or falling) on the TINx pin after the ENABLE bit is set. The reload register stores the result of the last measurement taken. If the timer overflows, 0x0000 is written to the reload register. Figure 21-12 shows the timer behavior when measuring the period of a signal.

The timer will not signal an interrupt in period measurement mode until the timer detects either two rising edges or two falling edges.

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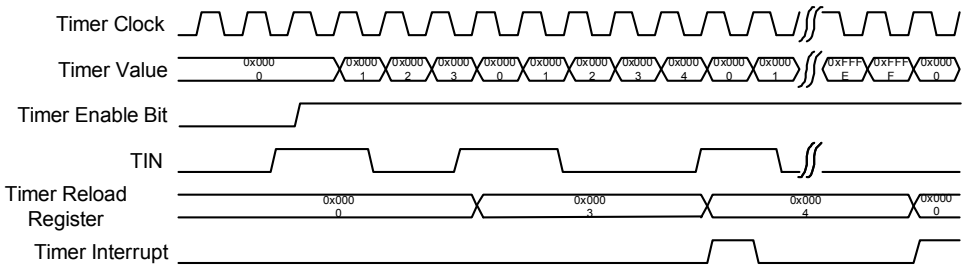
FIGURE 21-12: PULSE PERIOD MEASUREMENT



21.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the 16-Bit Counter-Timer Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 21-9: REGISTER SUMMARY

Offset	Register Name
00h	Timer x Control Register
04h	Timer x Clock and Event Control Register
08h	Timer x Reload Register
0Ch	Timer x Count Register

21.11.1 TIMER X CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:13	Reserved	R	-	-
12	TIMERX_CLK_REQ This bit reflects the current state of the timer's Clock_Required output signal. 1=The main clock is required by this block 0=The main clock is not required by this block	R	0h	Reset_Timer
11	SLEEP_ENABLE This bit reflects the current state of the timer's Sleep_Enable input signal. 1=Normal operation 0=Sleep Mode is requested	R	0h	Reset_Timer

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
10	TOUT_POLARITY This bit determines the polarity of the TOUTx output signal. In timer modes that toggle the TOUTx signal, this polarity bit will not have a perceivable difference, except to determine the inactive state. In One-Shot mode this determines if the pulsed output is active high or active low. 1=Active low 0=Active high	R/W	0h	Reset_ Timer
9	PD Power Down. 1=The timer is powered down and all clocks are gated 0=The timer is in a running state	R/W	1h	Reset_ Timer
8	FILTER_BYPASS This bit is used to enable or disable the noise filter on the TINx input signal. 1=IBypass Mode: input filter disabled. The TINx input directly affects the timer 0=Filter Mode: input filter enabled. The TINx input is filtered by the input filter	R/W	0h	Reset_ Timer
7	RLOAD Reload Control. This bit controls how the timer is reloaded on over-flow or underflow in Event and Timer modes. It has no effect in One Shot mode. 1=Reload timer from Timer Reload Register and continue counting 0=Roll timer over to FFFFh and continue counting when counting down and rolls over to 0000h and continues counting when counting up	R/W	0h	Reset_ Timer
6	TOUT_EN This bit enables the TOUTx pin 1=TOUTx pin function is enabled 0=TOUTx pin is inactive	R/W	0h	Reset_ Timer
4	UPDN In Event Mode, this bit selects the timer count direction. In Timer Mode enables timer control by the TINx input pin. Event Mode: 1=The timer counts up 0=The timer counts down Timer Mode: 1=TINx pin pauses the timer when de-asserted 0=TINx pin has no effect on the timer	R/W	0h	Reset_ Timer

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Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
4	INPOL This bit selects the polarity of the TINx input 1=TINx is active low 0=TINx is active high	R/W	0h	Reset_ Timer
3:2	MODE Timer Mode. 3=Measurement Mode 2=One Shot Mode 1=Event Mode 0=Timer Mode	R/W	0h	Reset_ Timer
1	RESET This bit stops the timer and resets the internal counter to the value in the Timer Reload Register. This bit also clears the ENABLE bit if it is set. This bit is self-clearing after the timer is reset. Firmware must poll the RESET bit in order to determine when the timer is active after reset. The polling time may be any value from 0 ms to 2^(TCLK+1))/48MHz. If it the TCLK value was set to 0111b then the polling time will be a 5.33us (typ). Worst case polling time is dependent on accuracy of 48MHz clock source. Interrupts are blocked only when RESET takes effect and the ENABLE bit is cleared. If interrupts are not desired, firmware must mask the interrupt in the interrupt block. 1=Timer reset 0=Normal timer operation	R/W	0h	Reset_ Timer
0	ENABLE This bit is used to start and stop the timer. This bit does not reset the timer count but does reset the timer pulse output. This bit will be cleared when the timer stops counting in One-Shot mode. The ENABLE bit is cleared after a RESET cycle has completed. Firmware must poll the RESET bit in order to determine when the timer is active after reset. 1=Timer is enabled 0=Timer is disabled	R/W	0h	Reset_ Timer

21.11.2 TIMER X CLOCK AND EVENT CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:12	Reserved	R	-	-
11:8	FCLK Timer Clock Select. This field determines the clock source for the TINx noise filter. See Section 21.10.2, "Filter Clock and Noise Filter" for a description of the available frequencies. The available frequencies are the same as for TCLK.	R/W	0h	Reset_Timer
7	EVENT Event Select. This bit is used to select the count source when the timer is operating in Event Mode. 1=TINx is count source 0=Timer x-1 overflow is count source	R/W	0h	Reset_Timer
6:5	EDGE This field selects which edge of the TINx input signal affects the timer in Event Mode, One-Shot Mode and Measurement Mode. Event Mode: 11b=No event selected 10b=Counts rising and falling edges 01b=Counts rising edges 00b=Counts falling edges One-Shot Mode: 11b=Start counting when the Enable bit is set 10b=Starts counting on a rising or falling edge 01b=Starts counting on a rising edge 00b=Starts counting on a falling edge Measurement Mode: 11b=No event selected 10b=Measures the time between rising edges and falling edges and the time between falling edges and rising edges 01b=Measures the time between rising edges 00b=Measures the time between falling edges	R/W	0h	Reset_Timer
4	Reserved	R	-	-
3:0	TCLK Timer Clock Select. This field determines the clock source for the 16-bit counter in the timer. See Section 21.10.1, "Timer Clock" for a description of the available frequencies.	R/W	0h	Reset_Timer

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21.11.3 TIMER X RELOAD REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	TIMER_RELOAD The Timer Reload register is used in Timer and One-Shot modes to set the lower limit of the timer. In Event mode the Timer Reload register sets either the upper or lower limit of the timer depending on if the timer is counting up or down. Valid Timer Reload values are 0001h - FFFFh. If the timer is running, the reload value will not be updated until the timer overflows or underflows. Programming a 0000h as a preload value is not a valid count value. Using a value of 0000h will cause unpredictable behavior.	R/W	FFFFh	Reset_ Timer

21.11.4 TIMER X COUNT REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	TIMER_COUNT The Timer Count register returns the current value of the timer in all modes.	R	FFFFh	Reset_ Timer

22.0 INPUT CAPTURE AND COMPARE TIMER

22.1 Introduction

The Input Capture and Compare Timers block contains a 32-bit timer running at the main system clock frequency. The timer is free-running and is associated with six 32-bit capture registers and two compare registers. Each capture register can record the value of the free-running timer based on a programmable edge of its associated input pin. An interrupt can be generated for each capture register each time it acquires a new timer value. The timer can also generate an interrupt when it automatically resets and can additionally generate two more interrupts when the timer matches the value in either of two 32-bit compare registers.

22.2 References

No references have been cited for this feature.

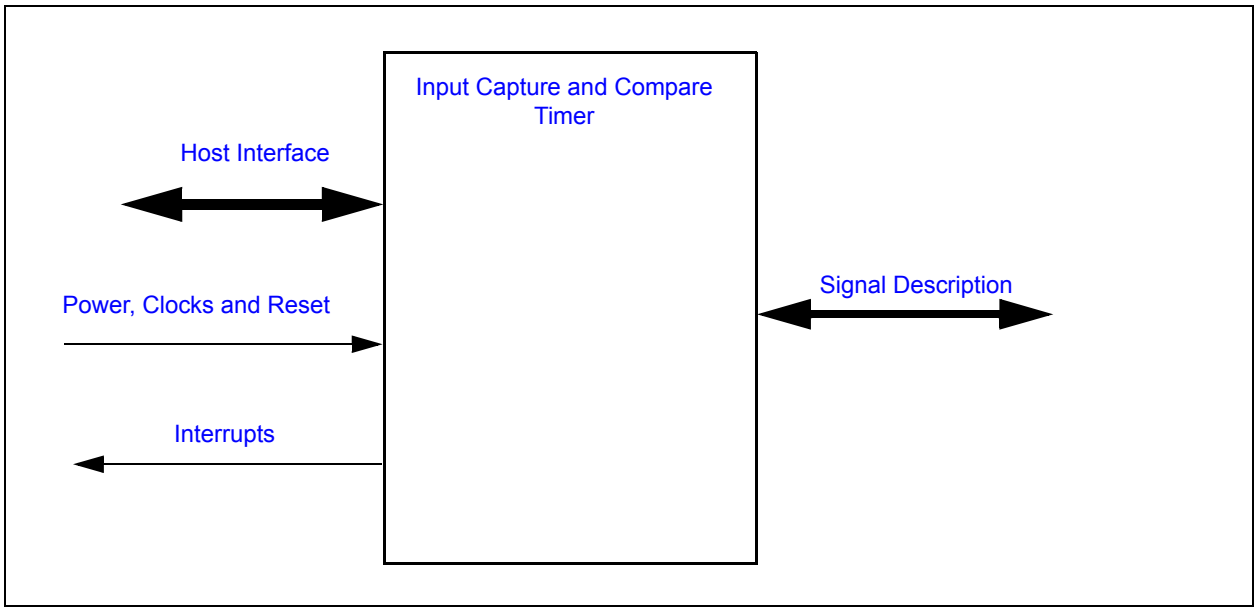
22.3 Terminology

There is no terminology for this block.

22.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 22-1: I/O DIAGRAM OF BLOCK



22.5 Signal Description

TABLE 22-1: SIGNAL DESCRIPTION

Name	Direction	Description
ICT0	INPUT	External capture trigger signal for Capture Register 0. Identical to signal FAN_TACH0.
ICT1	INPUT	External capture trigger signal for Capture Register 1. Identical to signal FAN_TACH1.

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TABLE 22-1: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
ICT2	INPUT	External capture trigger signal for Capture Register 2. Identical to signal FAN_TACH2.
ICT3	INPUT	External capture trigger signal for Capture Register 3
ICT4	INPUT	External capture trigger signal for Capture Register 4
ICT5	INPUT	External capture trigger signal for Capture Register 5
CTOUT0	OUTPUT	External compare match signal for Compare Register 0
CTOUT1	OUTPUT	External compare match signal for Compare Register 1

22.6 Host Interface

The registers defined for 16-bit Timers are accessible by the various hosts as indicated in Section 22.12, "EC Registers".

22.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

22.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

22.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for this block.

22.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

22.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
CAPTURE TIMER	This interrupt event fires when the 32-bit free running counter overflows from FFFF_FFFFh to 0000_0000h.
CAPTURE 0	This interrupt event fires when Capture Register 0 acquires a new value.
CAPTURE 1	This interrupt event fires when Capture Register 1 acquires a new value.
CAPTURE 2	This interrupt event fires when Capture Register 2 acquires a new value.
CAPTURE 3	This interrupt event fires when Capture Register 3 acquires a new value.
CAPTURE 4	This interrupt event fires when Capture Register 4 acquires a new value.
CAPTURE 5	This interrupt event fires when Capture Register 5 acquires a new value.
COMPARE 0	This interrupt event fires when the contents of Compare 0 Register match the contents of the Free Running Counter.
COMPARE 1	This interrupt event fires when the contents of Compare 1 Register match the contents of the Free Running Counter.

22.9 Low Power Modes

The Capture and Compare Timer may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry. This block is only be permitted to enter low power modes when the block is not active. The block is inactive if the ACTIVATE bit is de-asserted, and will also become inactive when the block's SLEEP_EN signal is asserted.

When the block returns from sleep, if enabled, the Free Running Timer Register value will continue counting from where it was when the block entered the Sleep state.

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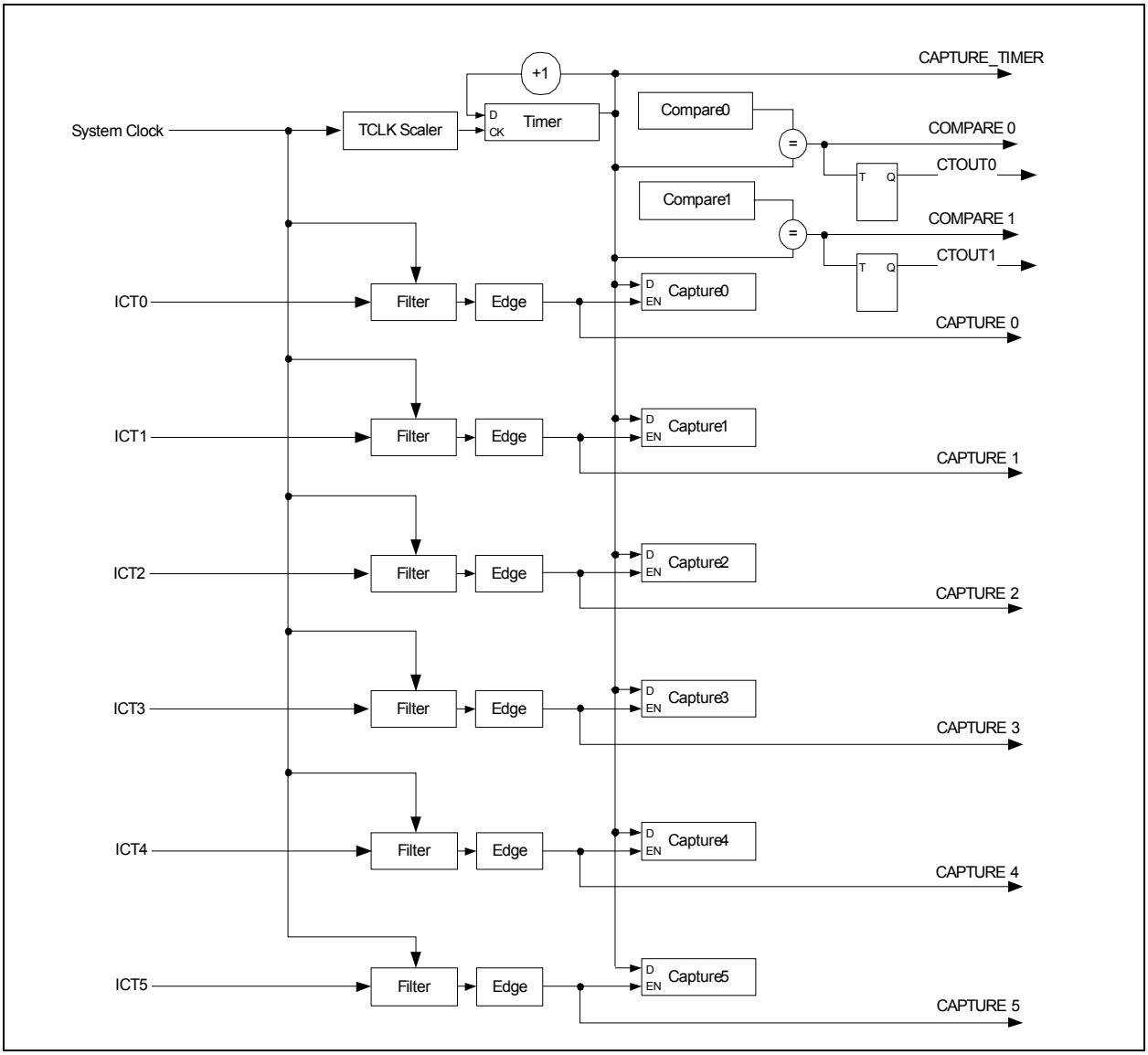
22.10 Description

FIGURE 22-2: CAPTURE AND COMPARE TIMER BLOCK DIAGRAM



22.10.1 TIMER CLOCK

Any of the frequencies listed in Table 22-2 may be used as the time base for the Free Running Counter.

TABLE 22-2: TIMER CLOCK FREQUENCIES

Timer Clock Select	Frequency Divide Select	Frequency Selected
0000b	Divide by 1	48MHz
0001b	Divide by 2	24MHz
0010b	Divide by 4	12MHz
0011b	Divide by 8	6MHz
0100b	Divide by 16	3MHz
0101b	Divide by 32	1.5MHz

TABLE 22-2: TIMER CLOCK FREQUENCIES (CONTINUED)

Timer Clock Select	Frequency Divide Select	Frequency Selected
0110b	Divide by 64	750KHz
0111b	Divide by 128	375KHz
1xxxb	Reserved	Reserved

For the Timer Clock, the **Timer Clock Select** value is defined by the TCLK field in the Capture and Compare Timer Control Register

22.10.2 FILTER CLOCK AND NOISE FILTER

The noise filter uses the Filter Clock (FCLK) to filter the signal on the Input Capture pins. An Input Capture pin must remain in the same state for three FCLK ticks before the internal state changes. The FILTER_BYPASS bit for the Input Capture pin may be used to bypass the input filter. Each Capture Register can individually bypass the filter.

When the input filter is bypassed, the minimum period of FCLK must be at least 2X the duration of an input signal pulse in order for an edge event to be captured reliably. When the input filter is enabled, the minimum period of FCLK must be at least 4X the duration of an input signal pulse in order for an edge event to be captured reliably.

22.11 Operation

22.11.1 INPUT CAPTURE

The Input Capture block consists of a free-running 32-bit timer and 2 capture registers. Each of the capture registers is associated with an input pin as well as an interrupt source bit in the Interrupt Aggregator: The Capture registers store the current value of the Free Running timer whenever the associated input signal changes, according to the programmed edge detection. An interrupt is also generated to the EC. The Capture registers are read-only. The registers are updated every time an edge is detected. If software does not read the register before the next edge, the value is lost.

22.11.2 COMPARE TIMER

There are two 32-bit Compare registers. Each of these registers can independently generate an interrupt to the EC when the 32-bit Free Running Timer matches the contents of the Compare register. The compare operation for each is enabled or disabled by a bit in the Capture and Compare Timer Control Register.

22.11.2.1 Interrupt Generation

Whenever a Compare Timer is enabled and the Compare register matches the Free Running Timer, a COMPARE event is sent to the Interrupt Aggregator. The event will trigger an EC interrupt if enabled by the appropriate Interrupt Enable register in the Aggregator.

22.11.2.2 Compare Output Generation

Each Compare Timer is associated with a toggle flip-flop. When the 32-bit Free Running Timer matches the contents of the Compare register the output off the flip-flop is complemented. Each of the toggle flip-flops can be independently set or cleared by using the COMPARE_SET or COMPARE_CLEAR fields, respectively, in the Capture and Compare Timer Control Register.

A Compare Timer should be disabled before setting or clearing the output, when updating the Compare register, or when updating the Free Running Timer, so spurious events are not generated by the matcher.

22.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Input Capture and Compare Timer Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

Note:	All registers in this block must be accessed as DWORDs.

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TABLE 22-3: REGISTER SUMMARY

Offset	Register Name
00h	Capture and Compare Timer Control Register
04h	Capture Control 0 Register
08h	Capture Control 1 Register
0Ch	Free Running Timer Register
10h	Capture 0 Register
14h	Capture 1 Register
18h	Capture 2 Register
1Ch	Capture 3 Register
20h	Capture 4 Register
24h	Capture 5 Register
28h	Compare 0 Register
2Ch	Compare 1 Register

22.12.1 CAPTURE AND COMPARE TIMER CONTROL REGISTER

Note:	It is not recommended to use Read-Modify-Write operations on this register. May inadvertently cause the COMPARE_SET and COMPARE_CLEAR bits to be written to ‘1’ in error.

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:26	Reserved	R	-	-
25	COMPARE_CLEAR0 When read, returns the current value off the Compare Timer Output 0 state. If written with a ‘1b’, the output state is cleared to ‘0’. Writes have no effect if COMPARE_SET1 in this register is written with a ‘1b’ at the same time. Writes of ‘0b’ have no effect.	R/WC	0	RESET_SYS
24	COMPARE_CLEAR1 When read, returns the current value off the Compare Timer Output 1 state. If written with a ‘1b’, the output state is cleared to ‘0’. Writes have no effect if COMPARE_SET0 in this register is written with a ‘1b’ at the same time. Writes of ‘0b’ have no effect.	R/WC	0	RESET_SYS
23:18	Reserved	R	-	-

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
17	COMPARE_SET0 When read, returns the current value off the Compare Timer Output 0 state. • If written with a ‘1b’, the output state is set to ‘1’. • Writes of ‘0b’ have no effect	R/WS	0	RESET_SYS
16	COMPARE_SET1 When read, returns the current value off the Compare Timer Output 1 state. If written with a ‘1b’, the output state is set to ‘1’. Writes of ‘0b’ have no effect	R/WS	0	RESET_SYS
15:10	Reserved	R	-	-
9	COMPARE_ENABLE1 Compare Enable for Compare 1 Register. When enabled, a match between the Compare 1 Register and the Free Running Timer Register will cause the TOUT1 output to toggle and will send a COMPARE event to the Interrupt Aggregator. 1=Enabled 0=Disabled	R/W	0b	RESET_SYS
8	COMPARE_ENABLE0 Compare Enable for Compare 0 Register. When enabled, a match between the Compare 0 Register and the Free Running Timer Register will cause the TOUT0 output to toggle and will send a COMPARE event to the Interrupt Aggregator. 1=Enabled 0=Disabled	R/W	0b	RESET_SYS
7	Reserved	R	-	-
6:4	TCLK This 3-bit field sets the clock source for the Free-Running Counter. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0b	RESET_SYS
3	Reserved	R	-	-
2	FREE_RESET Free Running Timer Reset. This bit stops the timer and resets the internal counter to 0000_0000h. This bit does not affect the FREE_ENABLE bit. This bit is self clearing after the timer is reset. 1=Timer reset 0=Normal timer operation	R/W	0h	RESET_SYS

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Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	FREE_ENABLE Free-Running Timer Enable. This bit is used to start and stop the free running timer. This bit does not reset the timer count. The timer starts counting at 0000_0000h on reset and wraps around back to 0000_0000h after it reaches FFFF_FFFFh. The FREE_ENABLE bit is cleared after the RESET cycle is done. Firmware must poll the FREE_RESET bit to determine when it is safe to re-enable the timer. 1=Timer is enabled. The Free Running Timer Register is read-only. 0=Timer is disabled. The Free Running Timer Register is writable.	R/W	0h	RESET_SYS
0	ACTIVATE 1=The timer block is in a running state 0=The timer block is powered down and all clocks are gated	R/W	0h	RESET_SYS

22.12.2 CAPTURE CONTROL 0 REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:29	FCLK_SEL3 This 3-bit field sets the clock source for the input filter for Capture Register 3. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0h	RESET_SYS
28:27	Reserved	R	-	-
26	FILTER_BYP3 This bit enables bypassing the input noise filter for Capture Register 3, so that the input signal goes directly into the timer. 1=Input filter bypassed 0=Input filter enabled	R/W	0h	RESET_SYS
25:24	CAPTURE_EDGE3 This field selects the edge type that triggers the capture of the Free Running Counter into Capture Register 3. 3=Capture event disabled 2=Both rising and falling edges 1=Rising edges 0=Falling edges	R/W	0h	RESET_SYS
23:21	FCLK_SEL2 This 3-bit field sets the clock source for the input filter for Capture Register 2. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0h	RESET_SYS

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
20:19	Reserved	R	-	-
18	FILTER_BYP2 This bit enables bypassing the input noise filter for Capture Register 2, so that the input signal goes directly into the timer. 1=Input filter bypassed 0=Input filter enabled	R/W	0h	RESET_SYS
17:16	CAPTURE_EDGE2 This field selects the edge type that triggers the capture of the Free Running Counter into Capture Register 2. 3=Capture event disabled 2=Both rising and falling edges 1=Rising edges 0=Falling edges	R/W	0h	RESET_SYS
15:13	FCLK_SEL1 This 3-bit field sets the clock source for the input filter for Capture Register 1. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0b	RESET_SYS
12:11	Reserved	R	-	-
10	FILTER_BYP1 This bit enables bypassing the input noise filter for Capture Register 1, so that the input signal goes directly into the timer. 1=Input filter bypassed 0=Input filter enabled	R/W	0h	RESET_SYS
9:8	CAPTURE_EDGE1 This field selects the edge type that triggers the capture of the Free Running Counter into Capture Register 1. 3=Capture event disabled 2=Both rising and falling edges 1=Rising edges 0=Falling edges	R/W	0h	RESET_SYS
7:5	FCLK_SEL0 This 3-bit field sets the clock source for the input filter for Capture Register 0. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0h	RESET_SYS
4:3	Reserved	R	-	-

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Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	FILTER_BYP0 This bit enables bypassing the input noise filter for Capture Register 0, so that the input signal goes directly into the timer. 1=Input filter bypassed 0=Input filter enabled	R/W	0h	RESET_SYS
1:0	CAPTURE_EDGE0 This field selects the edge type that triggers the capture of the Free Running Counter into Capture Register 0. 3=Capture event disabled 2=Both rising and falling edges 1=Rising edges 0=Falling edges	R/W	0h	RESET_SYS

22.12.3 CAPTURE CONTROL 1 REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:13	FCLK_SEL5 This 3-bit field sets the clock source for the input filter for Capture Register 5. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0b	RESET_SYS
12:11	Reserved	R	-	-
10	FILTER_BYP5 This bit enables bypassing the input noise filter for Capture Register 5, so that the input signal goes directly into the timer. 1=Input filter bypassed 0=Input filter enabled	R/W	0h	RESET_SYS
9:8	CAPTURE_EDGE5 This field selects the edge type that triggers the capture of the Free Running Counter into Capture Register 5. 3=Capture event disabled 2=Both rising and falling edges 1=Rising edges 0=Falling edges	R/W	0h	RESET_SYS
7:5	FCLK_SEL4 This 3-bit field sets the clock source for the input filter for Capture Register 4. See Table 22-2, "Timer Clock Frequencies" for a list of available frequencies.	R/W	0h	RESET_SYS

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
4:3	Reserved	R	-	-
2	FILTER_BYP4 This bit enables bypassing the input noise filter for Capture Register 4, so that the input signal goes directly into the timer. 1=Input filter bypassed 0=Input filter enabled	R/W	0h	RESET_SYS
1:0	CAPTURE_EDGE4 This field selects the edge type that triggers the capture of the Free Running Counter into Capture Register 4. 3=Capture event disabled 2=Both rising and falling edges 1=Rising edges 0=Falling edges	R/W	0h	RESET_SYS

22.12.4 FREE RUNNING TIMER REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	FREE_RUNNING_TIMER This register contains the current value of the Free Running Timer. A Capture Timer interrupt is signaled to the Interrupt Aggregator when this register transitions from FFFF_FFFFh to 0000_0000h. When FREE_ENABLE in the Capture and Compare Timer Control Register is '1', this register is read-only. When FREE_ENABLE is '0', this register may be written.	R/W	0h	RESET_SYS

22.12.5 CAPTURE 0 REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_0 This register saves the value copied from the Free Running timer on a programmed edge of ICT0.	R	0h	RESET_SYS

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22.12.6 CAPTURE 1 REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_1 This register saves the value copied from the Free Running timer on a programmed edge of ICT1.	R	0h	RESET_SYS

22.12.7 CAPTURE 2 REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_2 This register saves the value copied from the Free Running timer on a programmed edge of ICT2.	R	0h	RESET_SYS

22.12.8 CAPTURE 3 REGISTER

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_3 This register saves the value copied from the Free Running timer on a programmed edge of ICT3.	R	0h	RESET_SYS

22.12.9 CAPTURE 4 REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_4 This register saves the value copied from the Free Running timer on a programmed edge of ICT4.	R	0h	RESET_SYS

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22.12.10 CAPTURE 5 REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_5 This register saves the value copied from the Free Running timer on a programmed edge of ICT5.	R	0h	RESET_SYS

22.12.11 COMPARE 0 REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COMPARE_0 A COMPARE 0 interrupt is generated when this register matches the value in the Free Running Timer.	R/W	0h	RESET_SYS

22.12.12 COMPARE 1 REGISTER

Offset	2Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COMPARE_1 A COMPARE 1 interrupt is generated when this register matches the value in the Free Running Timer.	R/W	0h	RESET_SYS

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23.0 HIBERNATION TIMER

23.1 Introduction

The Hibernation Timer can generate a wake event to the Embedded Controller (EC) when it is in a hibernation mode. This block supports wake events up to 2 hours in duration. The timer is a 16-bit binary count-down timer that can be programmed in 30.5µs and 0.125 second increments for period ranges of 30.5µs to 2s or 0.125s to 136.5 minutes, respectively. Writing a non-zero value to this register starts the counter from that value. A wake-up interrupt is generated when the count reaches zero.

23.2 References

No references have been cited for this chapter

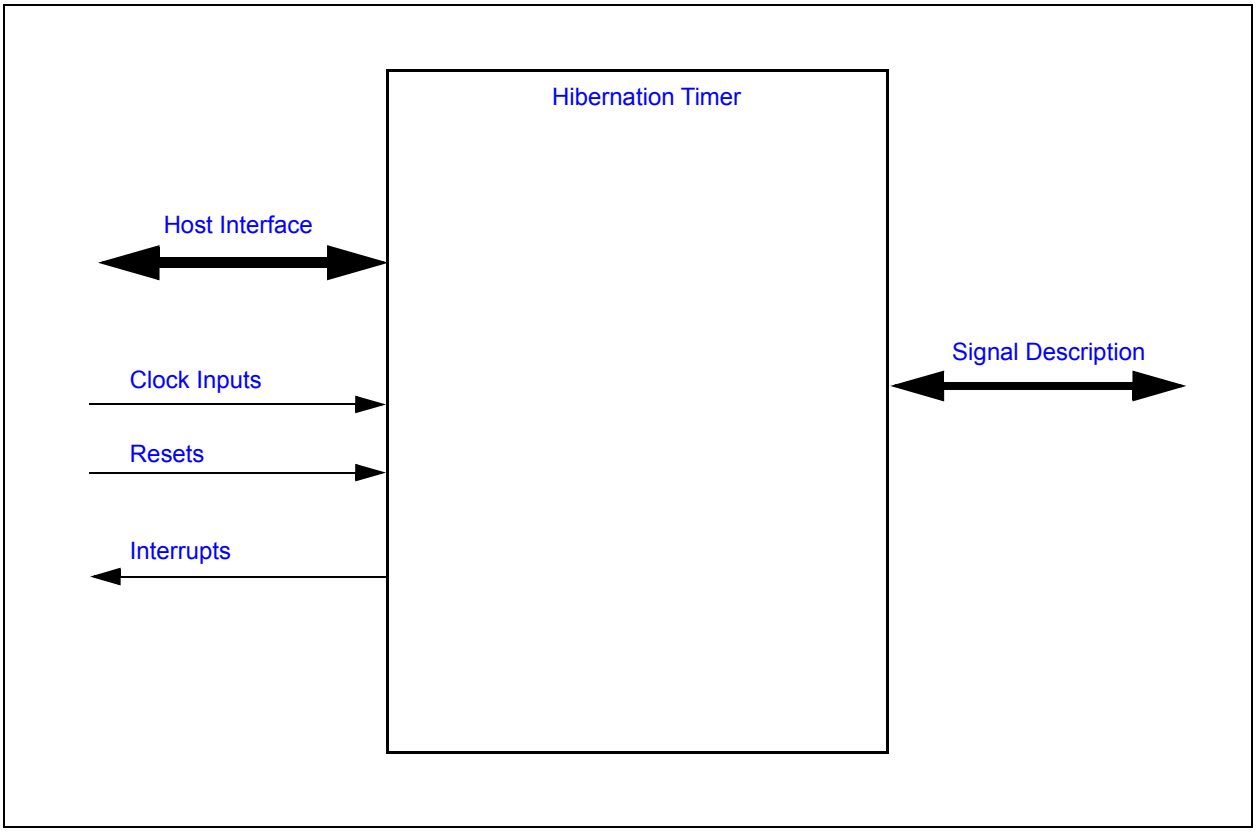
23.3 Terminology

No terms have been cited for this chapter.

23.4 Interface

This block is an IP block designed to be incorporated into a chip. It is designed to be accessed externally via the pin interface and internally via a registered host interface. The following diagram illustrates the various interfaces to the block.

FIGURE 23-1: HIBERNATION TIMER INTERFACE DIAGRAM



23.5 Signal Description

There are no external signals for this block.

23.6 Host Interface

The registers defined for the Hibernation Timer are accessible by the various hosts as indicated in Section 23.10, "EC Registers".

23.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

23.7.1 POWER DOMAINS

TABLE 23-1: POWER SOURCES

Name	Description
VTR	The timer control logic and registers are all implemented on this single power domain.

23.7.2 CLOCK INPUTS

TABLE 23-2: CLOCK INPUTS

Name	Description
32KHz	This is the clock source to the timer logic. The Pre-scaler may be used to adjust the minimum resolution per bit of the counter. if the main oscillator is stopped then an external 32.768kHz clock source must be active for the Hibernation Timer to continue to operate.

23.7.3 RESETS

TABLE 23-3: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal, which is an input to this block, resets all the logic and registers to their initial default state.

23.8 Interrupts

This section defines the interrupt Interface signals routed to the chip interrupt aggregator.

Each instance of the Hibernation Timer in the MEC170x can be used to generate interrupts and wake-up events when the timer decrements to zero.

TABLE 23-4: INTERRUPT INTERFACE SIGNAL DESCRIPTION TABLE

Name	Direction	Description
HTIMER	Output	Signal indicating that the timer is enabled and decrements to 0. This signal is used to generate an Hibernation Timer interrupt event.

23.9 Low Power Modes

The timer operates off of the 32KHz clock, and therefore will operate normally when the main oscillator is stopped.

The sleep enable inputs have no effect on the Hibernation Timer and the clock required outputs are only asserted during register read/write cycles for as long as necessary to propagate updates to the block core.

23.10 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Hibernation Timer Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

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TABLE 23-5: REGISTER SUMMARY

Offset	Register Name
00h	HTimer Preload Register
04h	HTimer Control Register
08h	HTimer Count Register

23.10.1 HTIMER PRELOAD REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:0	HT_PRELOAD This register is used to set the Hibernation Timer Preload value. Writing this register to a non-zero value resets the down counter to start counting down from this programmed value. Writing this register to 0000h disables the hibernation counter. The resolution of this timer is determined by the CTRL bit in the HTimer Control Register. Writes to the HTimer Control Register are completed with an EC bus cycle.	R/W	000h	RESET_SYS

23.10.2 HTIMER CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:1	Reserved	R	-	-
0	CTRL 1=The Hibernation Timer has a resolution of 0.125s per LSB, which yields a maximum time in excess of 2 hours. 0=The Hibernation Timer has a resolution of 30.5µs per LSB, which yields a maximum time of ~2seconds.	R	0000h	RESET_SYS

23.10.3 HTIMER COUNT REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:0	COUNT The current state of the Hibernation Timer.	R	0000h	RESET_SYS

24.0 RTOS TIMER

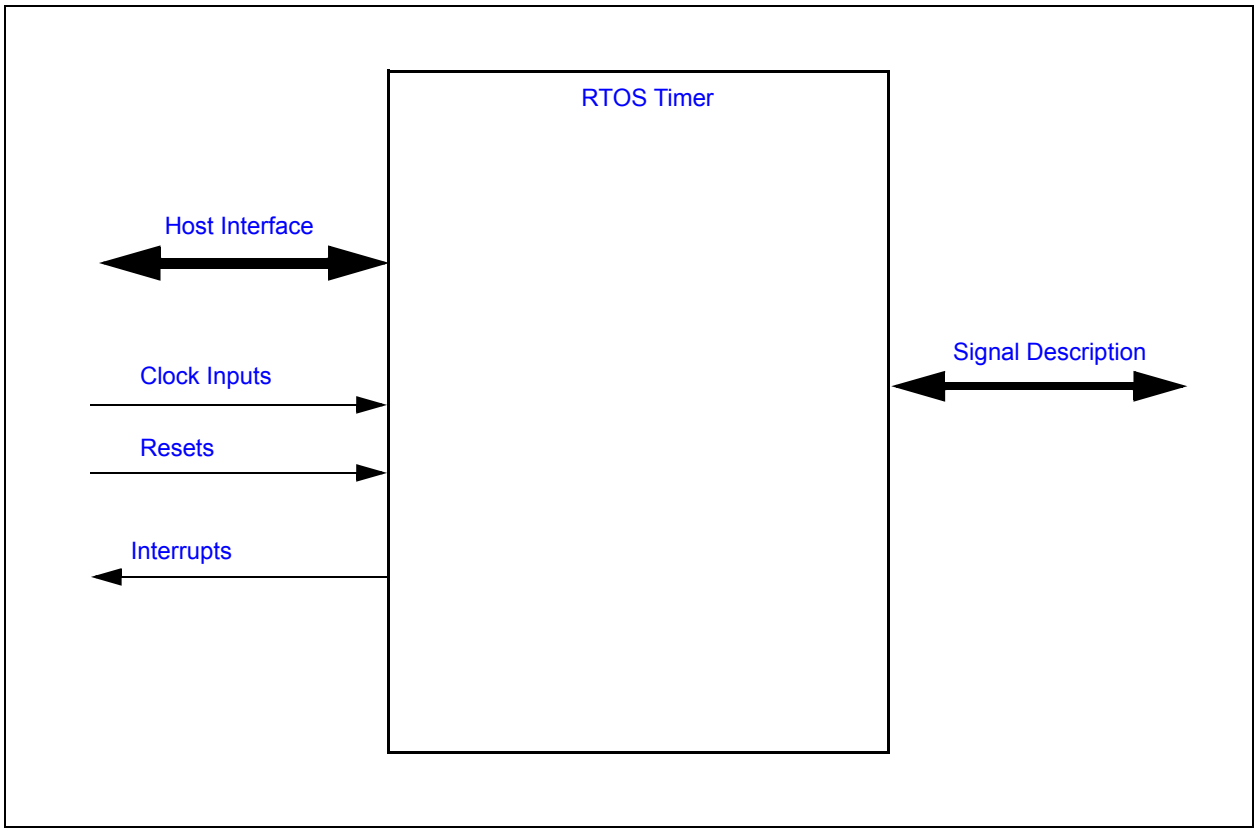
24.1 Introduction

The RTOS Timer is a low-power, 32-bit timer designed to operate on the 32kHz oscillator which is available during all chip sleep states. This allows firmware the option to sleep the processor and wake after a programmed amount of time. The timer may be used as a one-shot timer or a continuous timer. When the timer transitions to 0 it is capable of generating a wake-capable interrupt to the embedded controller. This timer may be halted during debug by hardware or via a software control bit.

24.2 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 24-1: I/O DIAGRAM OF BLOCK



24.3 Signal Description

There are no external signals for this block.

Name	Description
HALT	RTOS Timer Halt signal. This signal is connected to the same signal that halts the embedded controller during debug (e.g., JTAG Debugger is active, break points, etc.).

24.4 Host Interface

The embedded controller may access this block via the registers defined in Section 24.9, "EC Registers".

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24.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

24.5.1 POWER DOMAINS

Name	Description
VTR	The timer control logic and registers are all implemented on this single power domain.

24.5.2 CLOCK INPUTS

Name	Description
32KHz	This is the clock source to the timer logic.

24.5.3 RESETS

Name	Description
RESET_SYS	This reset signal, which is an input to this block, resets all the logic and registers to their initial default state.

24.6 Interrupts

Source	Description
RTOS_TIMER	RTOS Timer interrupt event. The interrupt is signaled when the timer counter transitions from 1 to 0 while counting.

24.7 Low Power Modes

The Basic Timer may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry. This block is only be permitted to enter low power modes when the block is not active.

24.8 Description

The RTOS Timer is a basic down counter that can operate either as a continuous timer or a one-shot timer. When it is started, the counter is loaded with a pre-load value and counts towards 0. When the counter counts down from 1 to 0, it will generate an interrupt. In one-shot mode (the AUTO_RELOAD bit is '0'), the timer will then halt; in continuous mode (the AUTO_RELOAD bit is '1'), the counter will automatically be restarted with the pre-load value.

The timer counter can be halted by firmware by setting the FIRMWARE_TIMER_HALT bit to '1'. In addition, if enabled, the timer counter can be halted by the external HALT signal.

24.9 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the RTOS Timer Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 24-1: REGISTER SUMMARY

Offset	Register Name
00h	RTOS Timer Count Register
04h	RTOS Timer Preload Register
08h	RTOS Timer Control Register
0Ch	Soft Interrupt Register

24.9.1 RTOS TIMER COUNT REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COUNTER This register contains the current value of the RTOS Timer counter. This register should be read as a DWORD. There is no latching mechanism of the upper bytes implemented if the register is accessed as a byte or word. Reading the register with byte or word operations may give incorrect results.	R/W	0h	RESET_SYS

24.9.2 RTOS TIMER PRELOAD REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	PRE_LOAD The this register is loaded into the RTOS Timer counter either when the TIMER_START bit is written with a ‘1’, or when the timer counter counts down to ‘0’ and the AUTO_RELOAD bit is ‘1’. This register must be programmed with a new count value before the TIMER_START bit is set to ‘1’. If this register is updated while the counter is operating, the new count value will only take effect if the counter transitions form 1 to 0 while the AUTO_RELOAD bit is set.	R/W	0h	RESET_SYS

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24.9.3 RTOS TIMER CONTROL REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:5	Reserved	R	-	-
4	FIRMWARE_TIMER_HALT 1=The timer counter is halted. If the counter was running, clearing this bit will restart the counter from the value at which it halted 0=The timer counter, if enabled, will continue to run	R/W	0h	RESET_SYS
3	EXT_HARDWARE_HALT_EN 1=The timer counter is halted when the external HALT signal is asserted. Counting is always enabled if HALT is de-asserted. 0=The HALT signal does not affect the RTOS Timer	R/W	0h	RESET_SYS
2	TIMER_START Writing a '1' to this bit will load the timer counter with the RTOS Timer Preload Register and start counting. If the Preload Register is 0, counting will not start and this bit will be cleared to '0'. Writing a '0' to this bit will halt the counter and clear its contents to 0. The RTOS timer interrupt will not be generated. This bit is automatically cleared if the AUTO_RELOAD bit is '0' and the timer counter transitions from 1 to 0.	R/W	0h	RESET_SYS
1	AUTO_RELOAD 1=The the RTOS Timer Preload Register is loaded into the timer counter and the counter is restarted when the counter transitions from 1 to 0 0=The timer counter halts when it transitions from 1 to 0 and will not restart	R/W	0h	RESET_SYS
0	BLOCK_ENABLE 1=RTOS timer counter is enabled 0=RTOS timer disabled. All register bits are reset to their default state	R/W	0h	RESET_SYS

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24.9.4 SOFT INTERRUPT REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3	SWI_3 Software Interrupt. A write of a ‘1’ to this bit will generate an SWI interrupt to the EC. Writes of a ‘0’ have no effect. Reads return ‘0’.	W	0h	RESET_SYS
2	SWI_2 Software Interrupt. A write of a ‘1’ to this bit will generate an SWI interrupt to the EC. Writes of a ‘0’ have no effect. Reads return ‘0’.	W	0h	RESET_SYS
1	SWI_1 Software Interrupt. A write of a ‘1’ to this bit will generate an SWI interrupt to the EC. Writes of a ‘0’ have no effect. Reads return ‘0’.	W	0h	RESET_SYS
0	SWI_0 Software Interrupt. A write of a ‘1’ to this bit will generate an SWI interrupt to the EC. Writes of a ‘0’ have no effect. Reads return ‘0’.	W	0h	RESET_SYS

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25.0 REAL TIME CLOCK

25.1 Introduction

This block provides the capabilities of an industry-standard 146818B Real-Time Clock module, without CMOS RAM. Enhancements to this architecture include:

- Industry standard Day of Month Alarm field, allowing for monthly alarms
- Configurable, automatic Daylight Savings adjustment
- Week Alarm for periodic interrupts and wakes based on Day of Week
- System Wake capability on interrupts.

25.2 References

1. Motorola 146818B Data Sheet, available on-line
2. Intel Lynx Point PCH EDS specification

25.3 Terminology

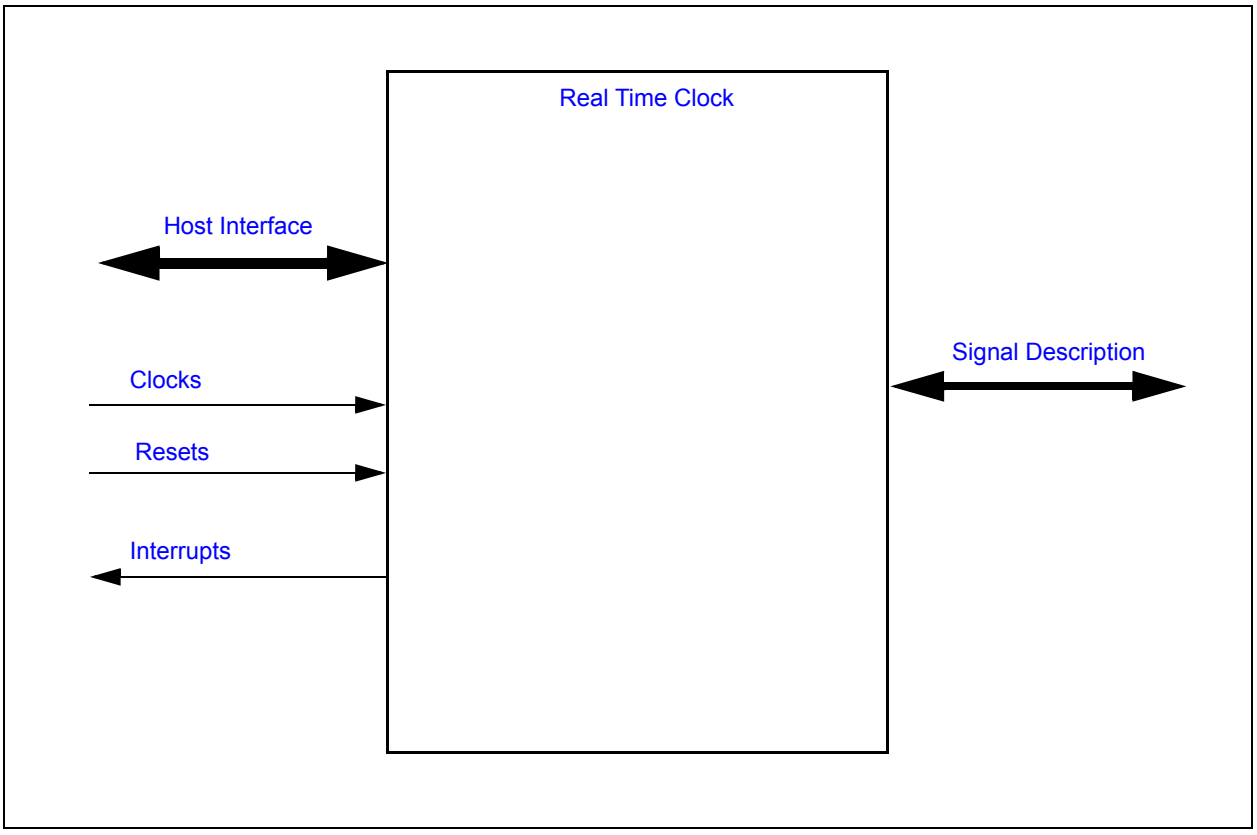
Time and Date Registers:

This is the set of registers that are automatically counted by hardware every 1 second while the block is enabled to run and to update. These registers are: **Seconds**, **Minutes**, **Hours**, **Day of Week**, **Day of Month**, **Month**, and **Year**.

25.4 Interface

This block's connections are entirely internal to the chip.

FIGURE 25-1: I/O DIAGRAM OF BLOCK



25.5 Signal Description

There are no external signals.

25.6 Host Interface

The registers defined for the Real Time Clock are accessible by the host and EC.

25.7 Power, Clocks and Resets

This section defines the Power, Clock, and Reset parameters of the block.

25.7.1 POWER DOMAINS

TABLE 25-1: POWER SOURCES

Name	Description
VBAT	This power well sources all of the internal registers and logic in this block.
VTR	This power well sources only bus communication. The block continues to operate internally while this rail is down.

25.7.2 CLOCKS

TABLE 25-2: CLOCKS

Name	Description
32KHz	This clock input drives all internal logic, and will be present at all times that the VBAT well is powered.

25.7.3 RESETS

TABLE 25-3: RESET SIGNALS

Name	Description
RESET_VBAT	This reset signal is used in the RESET_RTC signal to reset all of the registers and logic in this block. It directly resets the Soft Reset bit in the RTC Control Register.
RESET_RTC	This reset signal resets all of the registers and logic in this block, except for the Soft Reset bit in the RTC Control Register. It is triggered by RESET_VBAT, but can also be triggered by a Soft Reset from the RTC Control Register.
RESET_SYS	This reset signal is used to inhibit the bus communication logic, and isolates this block from VTR powered circuitry on-chip. Otherwise it has no effect on the internal state.

25.8 Interrupts

TABLE 25-4: SYSTEM INTERRUPTS

Source	Description
RTC	This interrupt source for the SIRQ logic is generated when any of the following events occur: • Update complete. This is triggered, at 1-second intervals, when the Time register updates have completed • Alarm. This is triggered when the alarm value matches the current time (and date, if used) • Periodic. This is triggered at the chosen programmable rate

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TABLE 25-5: EC INTERRUPTS

Source	Description
RTC	This interrupt is signaled to the Interrupt Aggregator when any of the following events occur: • Update complete. This is triggered, at 1-second intervals, when the Time register updates have completed • Alarm. This is triggered when the alarm value matches the current time (and date, if used) • Periodic. This is triggered at the chosen programmable rate
RTC ALARM	This wake interrupt is signaled to the Interrupt Aggregator when an Alarm event occurs.

25.9 Low Power Modes

The RTC has no low-power modes. It runs continuously while the VBAT well is powered.

25.10 Description

This block provides the capabilities of an industry-standard 146818B Real-Time Clock module, excluding the CMOS RAM and the SQW output. See the following registers, which represent enhancements to this architecture. These enhancements are listed below.

See the Date Alarm field of Register D for a Day of Month qualifier for alarms.

See the Week Alarm Register for a Day of Week qualifier for alarms.

See the registers Daylight Savings Forward Register and Daylight Savings Backward Register for setting up hands-off Daylight Savings adjustments.

See the RTC Control Register for enhanced control over the block's operations.

25.11 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the Real Time Clock. Host access for each register listed in this table is defined as an offset in the Host address space to the Block's Base Address, as defined by the instance's Base Address Register.

The EC address for each register is formed by adding the Base Address for each instance of the Real Time Clock shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the "Offset" column.

TABLE 25-6: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	Seconds Register
01h	Seconds Alarm Register
02h	Minutes Register
03h	Minutes Alarm Register
04h	Hours Register
05h	Hours Alarm Register
06h	Day of Week Register
07h	Day of Month Register
08h	Month Register
09h	Year Register
0Ah	Register A
0Bh	Register B
0Ch	Register C

TABLE 25-6: RUNTIME REGISTER SUMMARY (CONTINUED)

Offset	Register Name
0Dh	Register D
0Eh	Reserved
0Fh	Reserved
10h	RTC Control Register
14h	Week Alarm Register
18h	Daylight Savings Forward Register
1Ch	Daylight Savings Backward Register
20h	TEST

Note: This extended register set occupies offsets that have historically been used as CMOS RAM. Code ported to use this block should be examined to ensure that it does not assume that RAM exists in this block.

25.11.1 SECONDS REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	SECONDS Displays the number of seconds past the current minute, in the range 0--59. Presentation may be selected as binary or BCD, depending on the DM bit in Register B. Values written must also use the format defined by the current setting of the DM bit.	R/W	00h	RESET_RTC

25.11.2 SECONDS ALARM REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	SECONDS_ALARM Holds a match value, compared against the Seconds Register to trigger the Alarm event. Values written to this register must use the format defined by the current setting of the DM bit in Register B. A value of 11xxxxxxb written to this register makes it don't-care (always matching).	R/W	00h	RESET_RTC

25.11.3 MINUTES REGISTER

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	MINUTES Displays the number of minutes past the current hour, in the range 0--59. Presentation may be selected as binary or BCD, depending on the DM bit in Register B. Values written must also use the format defined by the current setting of the DM bit.	R/W	00h	RESET_RTC

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25.11.4 MINUTES ALARM REGISTER

Offset	03h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	MINUTES_ALARM Holds a match value, compared against the Minutes Register to trigger the Alarm event. Values written to this register must use the format defined by the current setting of the DM bit in Register B. A value of 11xxxxxxb written to this register makes it don't-care (always matching).	R/W	00h	RESET_RTC

25.11.5 HOURS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	HOURS_AM_PM In 12-hour mode (see bit "24/12" in register B), this bit indicates AM or PM. 1=PM 0=AM	R/W	0b	RESET_RTC
6:0	HOURS Displays the number of the hour, in the range 1--12 for 12-hour mode (see bit "24/12" in register B), or in the range 0--23 for 24-hour mode. Presentation may be selected as binary or BCD, depending on the DM bit in Register B. Values written must also use the format defined by the current setting of the DM bit.	R/W	00h	RESET_RTC

25.11.6 HOURS ALARM REGISTER

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	HOURS_ALARM Holds a match value, compared against the Hours Register to trigger the Alarm event. Values written to this register must use the format defined by the current settings of the DM bit and the 24/12 bit in Register B. A value of 11xxxxxxb written to this register makes it don't-care (always matching).	R/W	00h	RESET_RTC

25.11.7 DAY OF WEEK REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DAY_OF_WEEK Displays the day of the week, in the range 1 (Sunday) through 7 (Saturday). Numbers in this range are identical in both binary and BCD notation, so this register's format is unaffected by the DM bit.	R/W	00h	RESET_RTC

25.11.8 DAY OF MONTH REGISTER

Offset	07h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DAY_OF_MONTH Displays the day of the current month, in the range 1--31. Presentation may be selected as binary or BCD, depending on the DM bit in Register B. Values written must also use the format defined by the current setting of the DM bit.	R/W	00h	RESET_RTC

25.11.9 MONTH REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	MONTH Displays the month, in the range 1--12. Presentation may be selected as binary or BCD, depending on the DM bit in Register B. Values written must also use the format defined by the current setting of the DM bit.	R/W	00h	RESET_RTC

25.11.10 YEAR REGISTER

Offset	09h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	YEAR Displays the number of the year in the current century, in the range 0 (year 2000) through 99 (year 2099). Presentation may be selected as binary or BCD, depending on the DM bit in Register B. Values written must also use the format defined by the current setting of the DM bit.	R/W	00h	RESET_RTC

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25.11.11 REGISTER A

Offset	0Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	UPDATE_IN_PROGRESS '0' indicates that the Time and Date registers are stable and will not be altered by hardware soon. '1' indicates that a hardware update of the Time and Date registers may be in progress, and those registers should not be accessed by the host program. This bit is set to '1' at a point 488us (16 cycles of the 32K clock) before the update occurs, and is cleared immediately after the update. See also the Update-Ended Interrupt, which provides more useful status.	R	0b	RESET_RTC
6:4	DIVISION_CHAIN_SELECT This field provides general control for the Time and Date register updating logic. 11xb=Halt counting. The next time that 010b is written, updates will begin 500ms later. 010b=Required setting for normal operation. It is also necessary to set the Block Enable bit in the RTC Control Register to '1' for counting to begin 000b=Reserved. This field should be initialized to another value before Enabling the block in the RTC Control Register Other values Reserved	R/W	000b	RESET_RTC
3:0	RATE_SELECT This field selects the rate of the Periodic Interrupt source. See Table 25-7	R/W	0h	RESET_RTC

TABLE 25-7: REGISTER A FIELD RS: PERIODIC INTERRUPT SETTINGS

RS (hex)	Interrupt Period
0	Never Triggered
1	3.90625 ms
2	7.8125 ms
3	122.070 us
4	244.141 us
5	488.281 us
6	976.5625 us
7	1.953125 ms
8	3.90625 ms
9	7.8125 ms
A	15.625 ms
B	31.25 ms
C	62.5 ms
D	125 ms
E	250 ms
F	500 ms

25.11.12 REGISTER B

Offset	0Bh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	UPDATE_CYCLE_INHIBIT In its default state '0', this bit allows hardware updates to the Time and Date registers, which occur at 1-second intervals. A '1' written to this field inhibits updates, allowing these registers to be cleanly written to different values. Writing '0' to this bit allows updates to continue.	R/W	0b	RESET_RTC
6	PERIODIC_INTERRUPT_ENABLE 1=Alows the Periodic Interrupt events to be propagated as interrupts 0=Periodic events are not propagates as interrupts	R/W	0b	RESET_RTC
5	ALARM_INTERRUPT_ENABLE 1=Alows the Alarm Interrupt events to be propagated as interrupts 0=Alarm events are not propagates as interrupts	R/W	0b	RESET_RTC
4	UPDATE_ENDED_INTERRUPT_ENABLE 1=Alows the Update Ended Interrupt events to be propagated as interrupts 0=Update Ended events are not propagates as interrupts	R/W	0b	RESET_RTC
3	Reserved	R	-	-
2	DATA_MODE 1=Binary Mode for Dates and Times 0=BCD Mode for Dates and Times	R/W	0b	RESET_RTC
1	HOUR_FORMAT_24_12 1=24-Hour Format for Hours and Hours Alarm registers. 24-Hour format keeps the AM/PM bit off, with value range 0--23 0=12-Hour Format for Hours and Hours Alarm registers. 12-Hour format has an AM/PM bit, and value range 1--12	R/W	0b	RESET_RTC
0	DAYLIGHT_SAVINGS_ENABLE 1=Enables automatic hardware updating of the hour, using the registers Daylight Savings Forward and Daylight Savings Backward to select the yearly date and hour for each update 0=Automatic Daylight Savings updates disabled	R/W	0b	RESET_RTC

Note: The DATA_MODE and HOUR_FORMAT_24_12 bits affect only how values are presented as they are being read and how they are interpreted as they are being written. They do not affect the internal contents or interpretations of registers that have already been written, nor do they affect how those registers are represented or counted internally. This mode bits may be set and cleared dynamically, for whatever I/O data representation is desired by the host program.

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25.11.13 REGISTER C

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	INTERRUPT_REQUEST_FLAG 1=Any of bits[6:4] below is active after masking by their respective Enable bits in Register B. 0=No bits in this register are active This bit is automatically cleared by every Read access to this register.	RC	0b	RESET_RTC
6	PERIODIC_INTERRUPT_FLAG 1=A Periodic Interrupt event has occurred since the last time this register was read. This bit displays status regardless of the Periodic Interrupt Enable bit in Register B 0=A Periodic Interrupt event has not occurred This bit is automatically cleared by every Read access to this register.	RC	0b	RESET_RTC
5	ALARM_FLAG 1=An Alarm event has occurred since the last time this register was read. This bit displays status regardless of the Alarm Interrupt Enable bit in Register B. 0=An Alarm event has not occurred This bit is automatically cleared by every Read access to this register.	RC	0b	RESET_RTC
4	UPDATE_ENDED_INTERRUPT_FLAG 1=A Time and Date update has completed since the last time this register was read. This bit displays status regardless of the Update-Ended Interrupt Enable bit in Register B. Presentation of this status indicates that the Time and Date registers will be valid and stable for over 999ms 0=A Time and Data update has not completed since the last time this register was read This bit is automatically cleared by every Read access to this register.	RC	0b	RESET_RTC
3:0	Reserved	R	-	-

25.11.14 REGISTER D

Offset	0Dh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	Reserved	R	-	-
5:0	DATE_ALARM This field, if set to a non-zero value, will inhibit the Alarm interrupt unless this field matches the contents of the Month register also. If this field contains 00h (default), it represents a don't-care, allowing more frequent alarms.	R/W	00h	RESET_RTC

25.11.15 RTC CONTROL REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	-	-
3	ALARM_ENABLE 1=Enables the Alarm features 0=Disables the Alarm features	R/W	0b	RESET_RTC
2	Microchip Reserved	R/W	0b	RESET_RTC
1	SOFT_RESET A '1' written to this bit position will trigger the RESET_RTC reset, resetting the block and all registers except this one and the Test Register. This bit is self-clearing at the end of the reset, one cycle of LPC Bus Clock later, and so requires no waiting.	R/W	0b	RESET_VBAT
0	BLOCK_ENABLE This bit must be '1' in order for the block to function internally. Registers may be initialized first, before setting this bit to '1' to start operation.	R/W	0b	RESET_RTC

25.11.16 WEEK ALARM REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	ALARM_DAY_OF_WEEK This register, if written to a value in the range 1--7, will inhibit the Alarm interrupt unless this field matches the contents of the Day of Week Register also. If this field is written to any value 11xxxxxxb (like the default FFh), it represents a don't-care, allowing more frequent alarms, and will read back as FFh until another value is written.	R/W	FFh	RESET_RTC

25.11.17 DAYLIGHT SAVINGS FORWARD REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	DST_FORWARD_AM_PM This bit selects AM vs. PM, to match bit[7] of the Hours Register if 12-Hour mode is selected in Register B at the time of writing.	R/W	0b	RESET_RTC
30:24	DST_FORWARD_HOUR This field holds the matching value for bits[6:0] of the Hours register. The written value will be interpreted according to the 24/12 Hour mode and DM mode settings at the time of writing.	R/W	00h	RESET_RTC
23:19	Reserved	R	-	-

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Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
18:16	DST_FORWARD_WEEK This value matches an internally-maintained week number within the current month. Valid values for this field are: 5=Last week of month 4 =Fourth week of month 3=Third week of month 2=Second week of month 1=First week of month	R/W	0h	RESET_RTC
15:11	Reserved	R	-	-
10:8	DST_FORWARD_DAY_OF_WEEK This field matches the Day of Week Register bits[2:0].	R/W	0h	RESET_RTC
7:0	DST_FORWARD_MONTH This field matches the Month Register.	R/W	00h	RESET_RTC

This is a 32-bit register, accessible also as individual bytes. When writing as individual bytes, ensure that the DSE bit (in Register B) is off first, or that the block is disabled or stopped (SET bit), to prevent a time update while this register may have incompletely-updated contents.

When enabled by the DSE bit in Register B, this register defines an hour and day of the year at which the Hours register will be automatically incremented by 1 additional hour.

There are no don't-care fields recognized. All fields must be already initialized to valid settings whenever the DSE bit is '1'.

Fields other than Week and Day of Week use the current setting of the DM bit (binary vs. BCD) to interpret the information as it is written to them. Their values, as held internally, are not changed by later changes to the DM bit, without subsequently writing to this register as well.

Note: An Alarm that is set inside the hour after the time specified in this register will not be triggered, because that one-hour period is skipped. This period includes the exact time (0 minutes: 0 seconds) given by this register, through the 59 minutes: 59 seconds point afterward.

25.11.18 DAYLIGHT SAVINGS BACKWARD REGISTER

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	DST_BACKWARD_AM_PM This bit selects AM vs. PM, to match bit[7] of the Hours register if 12-Hour mode is selected in Register B at the time of writing.	R/W	0b	RESET_RTC
30:24	DST_BACKWARD_HOUR This field holds the matching value for bits[6:0] of the Hours register. The written value will be interpreted according to the 24/12 Hour mode and DM mode settings at the time of writing.	R/W	00h	RESET_RTC
23:19	Reserved	R	-	-

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
18:16	DST_BACKWARD_WEEK This value matches an internally-maintained week number within the current month. Valid values for this field are: 5=Last week of month 4 =Fourth week of month 3=Third week of month 2=Second week of month 1=First week of month	R/W	0h	RESET_RTC
15:11	Reserved	R	-	-
10:8	DST_BACKWARD_DAY_OF_WEEK This field matches the Day of Week Register bits[2:0].	R/W	0h	RESET_RTC
7:0	DST_BACKWARD_MONTH This field matches the Month Register.	R/W	00h	RESET_RTC

This is a 32-bit register, accessible also as individual bytes. When writing as individual bytes, ensure that the DSE bit (in Register B) is off first, or that the block is disabled or stopped (SET bit), to prevent a time update while this register may have incompletely-updated contents.

When enabled by the DSE bit in Register B, this register defines an hour and day of the year at which the Hours register increment will be inhibited from occurring. After triggering, this feature is automatically disabled for long enough to ensure that it will not retrigger the second time this Hours value appears, and then this feature is re-enabled automatically.

There are no don’t-care fields recognized. All fields must be already initialized to valid settings whenever the DSE bit is ‘1’.

Fields other than Week and Day of Week use the current setting of the DM bit (binary vs. BCD) to interpret the information as it is written to them. Their values, as held internally, are not changed by later changes to the DM bit, without subsequently writing to this register as well.

Note: An Alarm that is set inside the hour before the time specified in this register will be triggered twice, because that one-hour period is repeated. This period will include the exact time (0 minutes: 0 seconds) given by this register, through the 59 minutes: 59 seconds point afterward.

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26.0 WEEK TIMER

26.1 Introduction

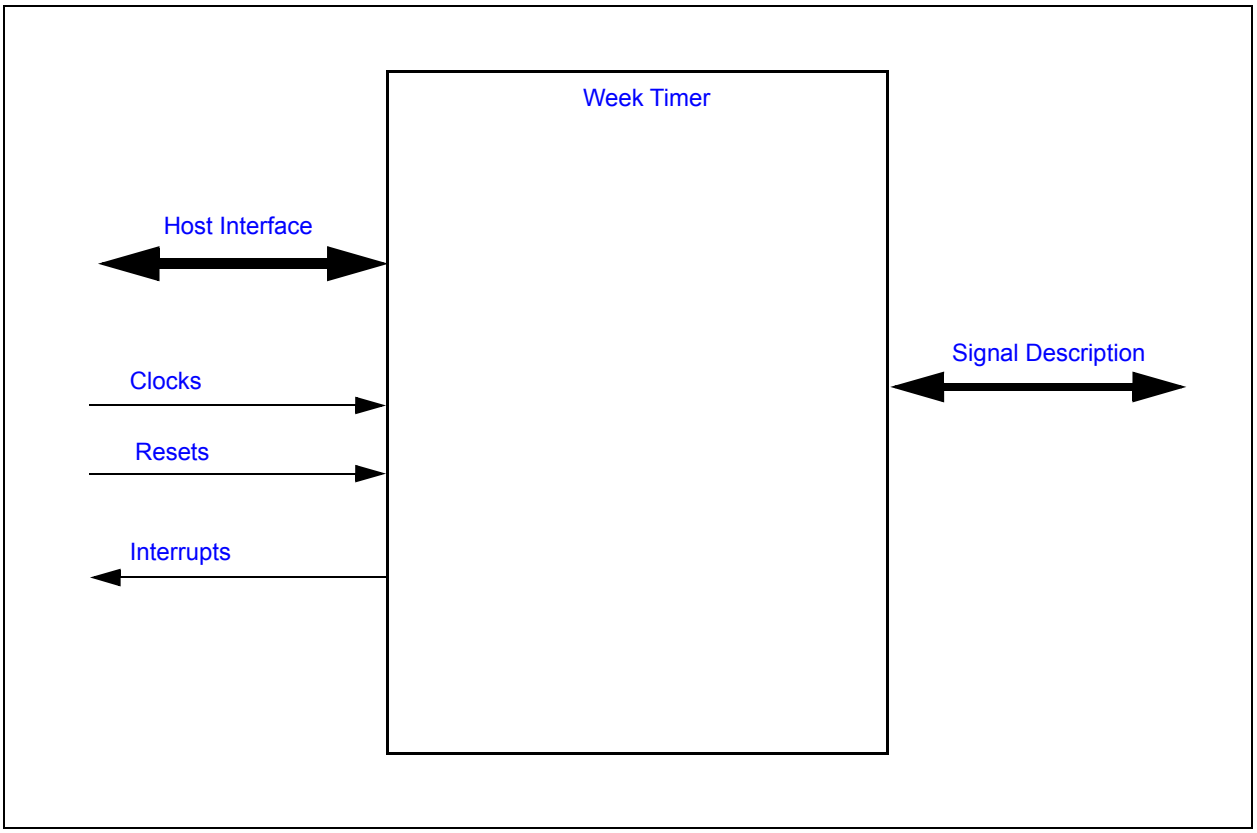
The Week Alarm Interface provides two timekeeping functions: a Week Timer and a Sub-Week Timer. Both the Week Timer and the Sub-Week Timer assert the Power-Up Event Output which automatically powers-up the system from the G3 state. Features include:

- EC interrupts based on matching a counter value
- Repeating interrupts at 1 second and sub-1 second intervals
- System Wake capability on interrupts, including Wake from Heavy Sleep

26.2 Interface

This block's connections are entirely internal to the chip.

FIGURE 26-1: I/O DIAGRAM OF BLOCK



26.3 Signal Description

TABLE 26-1: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
BGPO[9:0]	OUTPUT	Battery-powered general purpose outputs

TABLE 26-2: INTERNAL SIGNAL DESCRIPTION TABLE

Name	Direction	Description
POWER_UP_EVENT	OUTPUT	Signal to the VBAT-Powered Control Interface. When this signal is asserted, the VCI output signal asserts. See Section 26.8, "Power-Up Events".

26.4 Host Interface

The registers defined for the Week Timer are accessible only by the EC.

26.5 Power, Clocks and Resets

This section defines the Power, Clock, and Reset parameters of the block.

26.5.1 POWER DOMAINS

TABLE 26-3: POWER SOURCES

Name	Description
VBAT	This power well sources all of the internal registers and logic in this block.
VTR	This power well sources only bus communication. The block continues to operate internally while this rail is down.

26.5.2 CLOCKS

TABLE 26-4: CLOCKS

Name	Description
48MHz	Clock used for host register access
32KHz	This 32KHz clock input drives all internal logic, and will be present at all times that the VBAT well is powered.

26.5.3 RESETS

TABLE 26-5: RESET SIGNALS

Name	Description
RESET_VBAT	This reset signal is used reset all of the registers and logic in this block.
RESET_SYS	This reset signal is used to inhibit the bus communication logic, and isolates this block from VTR powered circuitry on-chip. Otherwise it has no effect on the internal state.

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26.6 Interrupts

TABLE 26-6: EC INTERRUPTS

Source	Description
WEEK_ALARM_INT	This interrupt is signaled to the Interrupt Aggregator when the Week Alarm Counter Register is greater than or equal to the Week Timer Compare Register. The interrupt signal is always generated by the Week Timer if the block is enabled; the interrupt is enabled or disabled in the Interrupt Aggregator.
SUB_WEEK_ALARM_INT	This interrupt is signaled to the Interrupt Aggregator when the Sub-Week Alarm Counter Register decrements from '1' to '0'. The interrupt signal is always generated by the Week Timer if the block is enabled; the interrupt is enabled or disabled in the Interrupt Aggregator.
ONE_SECOND	This interrupt is signaled to the Interrupt Aggregator at an isochronous rate of once per second. The interrupt signal is always generated by the Week Timer if the block is enabled; the interrupt is enabled or disabled in the Interrupt Aggregator.
SUB_SECOND	This interrupt is signaled to the Interrupt Aggregator at an isochronous rate programmable between 0.5Hz and 32.768KHz. The rate interrupts are signaled is determined by the SPISR field in the Sub-Second Programmable Interrupt Select Register. See Table 26-9, "SPISR Encoding". The interrupt signal is always generated by the Week Timer if the block is enabled; the interrupt is enabled or disabled in the Interrupt Aggregator.

26.7 Low Power Modes

The Week Alarm has no low-power modes. It runs continuously while the VBAT well is powered.

26.8 Power-Up Events

The Week Timer POWER_UP_EVENT can be used to power up the system after a timed interval. The POWER_UP_EVENT is routed to the VBAT-Powered Control Interface (VCI). The VCI_OUT pin that is part of the VCI is asserted if the POWER_UP_EVENT is asserted.

The POWER_UP_EVENT can be asserted under the following two conditions:

1. The Week Alarm Counter Register is greater than or equal to the Week Timer Compare Register
2. The Sub-Week Alarm Counter Register decrements from '1' to '0'

The assertion of the POWER_UP_EVENT is inhibited if the POWERUP_EN field in the Control Register is '0'

Once a POWER_UP_EVENT is asserted the POWERUP_EN bit must be cleared to reset the output. Clearing POWERUP_EN is necessary to avoid unintended power-up cycles.

26.9 Description

The Week Alarm block provides battery-powered timekeeping functions, derived from a low-power 32KHz clock, that operate even when the device's main power is off. The block contains a set of counters that can be used to generate one-shot and periodic interrupts to the EC for periods ranging from about 30 microseconds to over 8 years. The Week Alarm can be used in conjunction with the VBAT-Powered Control Interface to power up a sleeping system after a configurable period.

In addition to basic timekeeping, the Week Alarm block can be used to control the battery-powered general purpose BGPO outputs.

26.9.1 INTERNAL COUNTERS

The Week Timer includes 3 counters:

26.9.1.1 28-bit Week Alarm Counter

This counter is 28 bits wide. The clock for this counter is the overflow of the Clock Divider, and as long as the Week Timer is enabled, it is incremented at a 1 Hz rate.

Both an interrupt and a power-up event can be generated when the contents of this counter matches the contents of the Week Timer Compare Register.

26.9.1.2 9-bit Sub-Week Alarm Counter

This counter is 9 bits wide. It is decremented by 1 at each tick of its selected clock. It can be configured either as a one-shot or repeating event generator.

Both an interrupt and a power-up event can be generated when this counter decrements from 1 to 0.

The Sub-Week Alarm Counter can be configured with a number of different clock sources for its time base, derived from either the Week Alarm Counter or the Clock Divider, by setting the SUBWEEK_TICK field of the Sub-Week Control Register.

TABLE 26-7: SUB-WEEK ALARM COUNTER CLOCK

SUBWEEK_ TICK	Source	SPISR	Frequency	Minimum Duration	Maximum Duration
0	Counter Disabled				
1	Sub-Second	0	Counter Disabled		
		1	2 Hz	500 ms	255.5 sec
		2	4 Hz	250 ms	127.8 sec
		3	8 Hz	125 ms	63.9 sec
		4	16 Hz	62.5	31.9 sec
		5	32 Hz	31.25 ms	16.0 sec
		6	64 Hz	15.6 ms	8 sec
		7	128 Hz	7.8 ms	4 sec
		8	256 Hz	3.9 ms	2 sec
		9	512 Hz	1.95 ms	1 sec
		10	1024 Hz	977 µS	499 ms
		11	2048 Hz	488 µS	249.5 ms
		12	4096 Hz	244 µS	124.8 ms
		13	8192 Hz	122 µS	62.4 ms
		14	16.384 KHz	61.1 µS	31.2 ms
		15	32.768 KHz	30.5 µS	15.6 ms
2	Second	n/a	1 Hz	1 sec	511 sec
3	Reserved				
4	Week Counter bit 3	n/a	125 Hz	8 sec	68.1 min
5	Week Counter bit 5	n/a	31.25 Hz	32 sec	272.5 min
6	Week Counter bit 7	n/a	7.8125 Hz	128 sec	18.17 hour
7	Week Counter bit 9	n/a	1.95 Hz	512 sec	72.68 hour

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Note 1: The Week Alarm Counter **must not** be modified by firmware if Sub-Week Alarm Counter is using the Week Alarm Counter as its clock source (i.e., the SUBWEEK_TICK field is set to any of the values 4, 5, 6 or 7). The Sub-Week Alarm Counter must be disabled before changing the Week Alarm Counter. For example, the following sequence may be used:

1.Write 0h to the Sub-Week Alarm Counter Register (disabling the Sub-Week Counter)

2.Write the Week Alarm Counter Register

3.Write a new value to the Sub-Week Alarm Counter Register, restarting the Sub-Week Counter

26.9.1.3 15-bit Clock Divider

This counter is 15 bits wide. The clock for this counter is 32KHz, and as long as the Week Timer is enabled, it is incremented at 32.768KHz rate. The Clock Divider automatically The Clock Divider generates a clock out of 1 Hz when the counter wraps from 7FFFh to 0h.

By selecting one of the 15 bits of the counter, using the Sub-Second Programmable Interrupt Select Register, the Clock Divider can be used either to generate a time base for the Sub-Week Alarm Counter or as an isochronous interrupt to the EC, the SUB_SECOND interrupt. See Table 26-9, "SPISR Encoding" for a list of available frequencies.

26.9.2 TIMER VALID STATUS

If power on reset occurs on the VBAT power rail while the main device power is off, the counters in the Week Alarm are invalid. If firmware detects a POR on the VBAT power rail after a system boot, by checking the status bits in the Power, Clocks and Resets registers, the Week Alarm block must be reinitialized.

26.9.3 APPLICATION NOTE: REGISTER TIMING

Register writes in the Week Alarm complete within two cycles of the 32KHz clock.The write completes even if the main system clock is stopped before the two cycles of the 32K clock complete. Register reads complete in one cycle of the internal bus clock.

All Week Alarm interrupts that are asserted within the same cycle of the 32KHz clock are synchronously asserted to the EC.

26.9.4 APPLICATION NOTE: USE OF THE WEEK TIMER AS A 43-BIT COUNTER

The Week Timer cannot be directly used as a 42-bit counter that is incremented directly by the 32.768KHz clock domain. The upper 28 bits (28-bit Week Alarm Counter) are incremented at a 1Hz rate and the lower 16 bits (15-bit Clock Divider) are incremented at a 32.768KHz rate, but the increments are not performed in parallel. In particular, the upper 28 bits are incremented when the lower 15 bits increment from 0 to 1, so as long as the Clock Divider Register is 0 the two registers together, treated as a single value, have a smaller value then before the lower register rolled over from 7FFFh to 0h.

The following code can be used to treat the two registers as a single large counter. This example extracts a 32-bit value from the middle of the 43-bit counter:

```
dword TIME_STAMP(void)
{
    AHB_dword wct_value;
    AHB_dword cd_value1;
    AHB_dword cd_value2;
    dword irqEnableSave;

    //Disable interrupts
    irqEnableSave = IRQ_ENABLE;
    IRQ_ENABLE = 0;

    //Read 15-bit clk divider reading register, save result in A
    cd_value1 = WTIMER->CLOCK_DIVIDER;
    //Read 28 bit up-counter timer register, save result in B
    wct_value = WTIMER->WEEK_COUNTER_TIMER;
    //Read 15-bit clk divider reading register, save result in C
    cd_value2 = WTIMER->CLOCK_DIVIDER;

    if (0 == cd_value2)
```

```
    {
        wct_value = wct_value + 1;
    }
    else if ( (cd_value2 < cd_value1) || (0 == cd_value1))
    {
        wct_value = WTIMER->WEEK_COUNTER_TIMER;
    }

    //Enable interrupts
    IRQ_ENABLE = irqEnableSave;

    return (WTIMER_BASE + ((wct_value << 10) | (cd_value2>>5)));
}
```

26.10 Battery-Powered General Purpose Outputs

The Week Timer contains the control logic for Battery-Powered General Purposes Outputs (BGPOs). These are output-only pins whose state can be controlled by firmware and preserved when the device is operating on VBAT power alone.

When a BGPO function is selected on a pin that can also serve as a GPIO, using the BGPO Power Register, the GPIO input register is readable but always returns a '1b'.

26.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Week Timer Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 26-8: REGISTER SUMMARY

Offset	Register Name
00h	Control Register
04h	Week Alarm Counter Register
08h	Week Timer Compare Register
0Ch	Clock Divider Register
10h	Sub-Second Programmable Interrupt Select Register
14h	Sub-Week Control Register
18h	Sub-Week Alarm Counter Register
1Ch	BGPO Data Register
20h	BGPO Power Register
24h	BGPO Reset Register

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26.11.1 CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6	POWERUP_EN This bit controls the state of the Power-Up Event Output and enables Week POWER-UP Event decoding in the VBAT-Powered Control Interface. See Section 26.8, "Power-Up Events" for a functional description of the POWER-UP_EN bit. 1=Power-Up Event Output Enabled 0=Power-Up Event Output Disabled and Reset	R/W	00h	RESET_VBAT
5:1	Reserved	R	-	-
0	WT_ENABLE The WT_ENABLE bit is used to start and stop the Week Alarm Counter Register and the Clock Divider Register. The value in the Counter Register is held when the WT_ENABLE bit is not asserted (‘0’) and the count is resumed from the last value when the bit is asserted (‘1’). The 15-Bit Clock Divider is reset to 00h and the Week Alarm Interface is in its lowest power consumption state when the WT_ENABLE bit is not asserted.	R/W	1h	RESET_VBAT

26.11.2 WEEK ALARM COUNTER REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	Reserved	R	-	-
27:0	WEEK_COUNTER While the WT_ENABLE bit is ‘1’, this register is incremented at a 1 Hz rate. Writes of this register may require one second to take effect. Reads return the current state of the register. Reads and writes complete independently of the state of WT_ENABLE.	R/W	00h	RESET_VBAT

26.11.3 WEEK TIMER COMPARE REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	Reserved	R	-	-
27:0	WEEK_COMPARE A Week Alarm Interrupt and a Week Alarm Power-Up Event are asserted when the Week Alarm Counter Register is greater than or equal to the contents of this register. Reads and writes complete independently of the state of WT_ENABLE.	R/W	FFFFFFFh	RESET_VBAT

26.11.4 CLOCK DIVIDER REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:15	Reserved	R	-	-
14:0	CLOCK_DIVIDER Reads of this register return the current state of the Week Timer 15-bit clock divider.	R	-	RESET_VBAT

26.11.5 SUB-SECOND PROGRAMMABLE INTERRUPT SELECT REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3:0	SPISR This field determines the rate at which Sub-Second interrupt events are generated. Table 26-9, "SPISR Encoding" shows the relation between the SPISR encoding and Sub-Second interrupt rate.	R/W	00h	RESET_VBAT

TABLE 26-9: SPISR ENCODING

SPISR Value	Sub-Second Interrupt Rate, Hz	Interrupt Period
0	Interrupts disabled	
1	2	500 ms
2	4	250 ms
3	8	125 ms

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TABLE 26-9: SPISR ENCODING (CONTINUED)

SPISR Value	Sub-Second Interrupt Rate, Hz	Interrupt Period
4	16	62.5 ms
5	32	31.25 ms
6	64	15.63 ms
7	128	7.813 ms
8	256	3.906 ms
9	512	1.953 ms
10	1024	977 µS
11	2048	488 µS
12	4096	244 µS
13	8192	122 µS
14	16384	61 µS
15	32768	30.5 µS

26.11.6 SUB-WEEK CONTROL REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:7	SUBWEEK_TICK This field selects the clock source for the Sub-Week Counter. See Table 26-7, "Sub-Week Alarm Counter Clock" for the description of the options for this field. See also Note 1.	R/W	0	RESET_VBAT
6	AUTO_RELOAD 1= No reload occurs when the Sub-Week Counter expires 0= Reloads the SUBWEEK_COUNTER_LOAD field into the Sub-Week Counter when the counter expires.	R/W	0	RESET_VBAT
5	TEST Must always be written with 0.	R/W	0	-
4:2	Reserved	R	-	-

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	WEEK_TIMER_POWERUP_EVENT_STATUS This bit is set to '1' when the Week Alarm Counter Register is greater than or equal the contents of the Week Timer Compare Register and the POWERUP_EN is '1'. Writes of '1' clear this bit. Writes of '0' have no effect. **Note:** This bit does not have to be cleared to remove a Week Timer Power-Up Event.	R/WC	0	RESET_VBAT
0	SUBWEEK_TIMER_POWERUP_EVENT_STATUS This bit is set to '1' when the Sub-Week Alarm Counter Register decrements from '1' to '0' and the POWERUP_EN is '1'. Writes of '1' clear this bit. Writes of '0' have no effect. **Note:** This bit MUST be cleared to remove a Sub-Week Timer Power-Up Event.	R/WC	0	RESET_VBAT

26.11.7 SUB-WEEK ALARM COUNTER REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:25	Reserved	R	-	-
24:16	SUBWEEK_COUNTER_STATUS Reads of this register return the current state of the 9-bit Sub-Week Alarm counter.	R	00h	RESET_VBAT
15:9	Reserved	R	-	-
8:0	SUBWEEK_COUNTER_LOAD Writes with a non-zero value to this field reload the 9-bit Sub-Week Alarm counter. Writes of 0 disable the counter. If the Sub-Week Alarm counter decrements to 0 and the AUTO_RELOAD bit is set, the value in this field is automatically loaded into the Sub-Week Alarm counter.	R/W	00h	RESET_VBAT

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26.11.8 BGPO DATA REGISTER

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:0	BGPO Battery powered General Purpose Output. Each output pin may be individually configured to be either a VBAT-power BGPO or a VTR-powered GPIO, based on the corresponding settings in the BGPO Power Register. Additionally, each output pin may be individually configured to reset to 0 on either RESET_VBAT or RESET_SYS, based on the corresponding settings in the BGPO Reset Register. For each bit [*i*] in the field: 1=BGPO[*i*] output is high 0=BGPO[*i*] output is low If a BGPO[*i*] does not appear in a package, the corresponding bit **must** be written with a 0 or undesirable results will occur.	R/W	0h	RESET_VBAT or RESET_SYS

26.11.9 BGPO POWER REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:6	Reserved	R	-	-
5:1	BGPO_POWER Battery powered General Purpose Output power source. For each bit [*i*] in the field: 1=BGPO[*i*] is powered by VBAT. The BGPO[*i*] pin is always determined by the corresponding bit in the BGPO Data Register. The GPIO Input register for the GPIO that is multiplexed with the BGPO always returns a '1b'. 0=The pin for BGPO[*i*] functions as a GPIO. When VTR is powered, the pin associated with BGPO[*i*] is determined by the GPIO associated with the pin. When VTR is unpowered, the pin is tri-stated	R/W	1Fh	RESET_VBAT
0	Reserved	R	-	-

Note: Because BGPO[9:6] and BGPO0 are not multiplexed with GPIOs, bits 9:6 and 0 are reserved.

26.11.10 BGPO RESET REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:0	BGPO_RESET Battery powered General Purpose Output reset event. For each bit [*i*] in the field: 1=BGPO[*i*] is reset to 0 on RESET_VBAT 0=BGPO[*i*] is reset to 0 on RESET_SYS	R/W	0h	RESET_VBAT

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27.0 TACH

27.1 Introduction

This block monitors TACH output signals (or locked rotor signals) from various types of fans, and determines their speed.

27.2 References

No references have been cited for this feature.

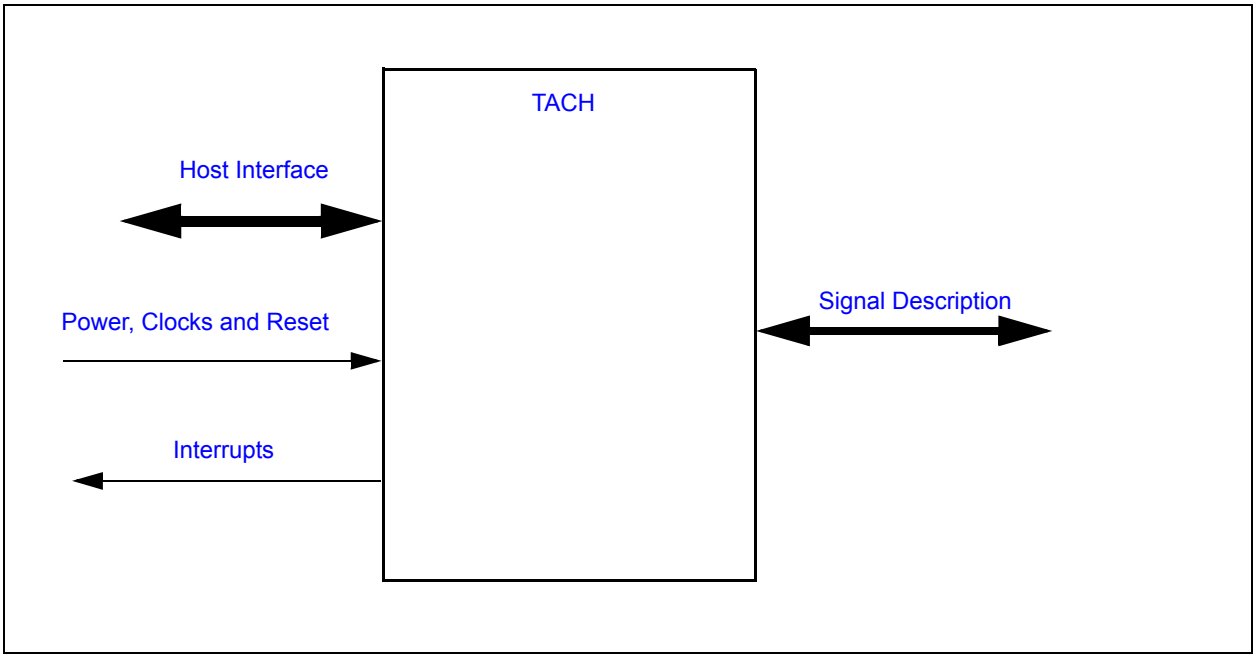
27.3 Terminology

There is no terminology defined for this section.

27.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 27-1: I/O DIAGRAM OF BLOCK



27.5 Signal Description

TABLE 27-1: SIGNAL DESCRIPTION

Name	Direction	Description
TACH INPUT	Input	Tachometer signal from TACHx Pin.

27.6 Host Interface

The registers defined for the TACH are accessible by the various hosts as indicated in Section 27.11, "EC Registers".

27.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

27.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

27.7.2 CLOCK INPUTS

Name	Description
100KHz	This is the clock input to the tachometer monitor logic. In Mode 1, the TACH is measured in the number of these clocks. This clock is derived from the main clock domain.

27.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

27.8 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 27-2: EC INTERRUPTS

Source	Description
TACH	This internal signal is generated from the OR'd result of the status events, as defined in the TACHx Status Register.

27.9 Low Power Modes

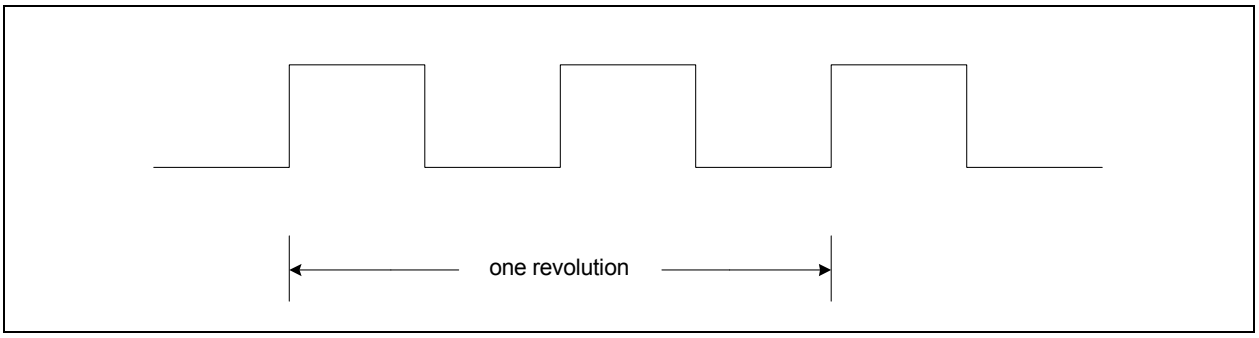
The TACH may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

27.10 Description

The TACH block monitors Tach output signals or locked rotor signals generated by various types of fans. These signals can be used to determine the speed of the attached fan. This block is designed to monitor fans at fan speeds from 100 RPMs to 30,000 RPMs.

Typically, these are DC brushless fans that generate (with each revolution) a 50% duty cycle, two-period square wave, as shown in Figure 27-2 below.

FIGURE 27-2: FAN GENERATED 50%DUTY CYCLE WAVEFORM



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In typical systems, the fans are powered by the main power supply. Firmware may disable this block when it detects that the main power rail has been turned off by either clearing the <enable> TACH_ENABLE bit or putting the block to sleep via the supported Low Power Mode interface (see Low Power Modes).

27.10.1 MODES OF OPERATION

The Tachometer block supports two modes of operation. The mode of operation is selected via the TACH_READING_-MODE_SELECT bit.

27.10.1.1 Free Running Counter

In Mode 0, the Tachometer block uses the TACH input as the clock source for the internal TACH pulse counter (see TACHX_COUNTER). The counter is incremented when it detects a rising edge on the TACH input. In this mode, the firmware may periodically poll the TACHX_COUNTER field to determine the average speed over a period of time. The firmware must store the previous reading and the current reading to compute the number of pulses detected over a period of time. In this mode, the counter continuously increments until it reaches FFFFh. It then wraps back to 0000h and continues counting. The firmware must ensure that the sample rate is greater than the time it takes for the counter to wrap back to the starting point.

Note:	Tach interrupts should be disabled in Mode 0.

27.10.1.2 Mode 1 -- Number of Clock Pulses per Revolution

In Mode 1, the Tachometer block uses its 100KHz clock input to measure the programmable number of TACH pulses. In this mode, the internal TACH pulse counter (TACHX_COUNTER) returns the value in number of 100KHz pulses per programmed number of TACH_EDGES. For fans that generate two square waves per revolution, these bits should be configured to five edges.

When the number of edges is detected, the counter is latched and the COUNT_READY_STATUS bit is asserted. If the COUNT_READY_INT_EN bit is set a TACH interrupt event will be generated.

27.10.2 OUT-OF-LIMIT EVENTS

The TACH Block has a pair of limit registers that may be configured to generate an event if the Tach indicates that the fan is operating too slow or too fast. If the <TACH reading> exceeds one of the programmed limits, the TACHx High Limit Register and the TACHx Low Limit Register, the bit TACH_OUT_OF_LIMIT_STATUS will be set. If the TACH_OUT_OF_LIMIT_STATUS bit is set, the Tachometer block will generate an interrupt event.

27.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the TACH Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 27-3: REGISTER SUMMARY

Offset	Register Name
00h	TACHx Control Register
04h	TACHx Status Register
08h	TACHx High Limit Register
0Ch	TACHx Low Limit Register

27.11.1 TACHX CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	TACHX_COUNTER This 16-bit field contains the latched value of the internal Tach pulse counter, which may be configured by the Tach Reading Mode Select field to operate as a free-running counter or to be gated by the Tach input signal. If the counter is free-running (Mode 0), the internal Tach counter increments (if enabled) on transitions of the raw Tach input signal and is latched into this field every time it is incremented. The act of reading this field will not reset the counter, which rolls over to 0000h after FFFFh. The firmware will compute the delta between the current count reading and the previous count reading, to determine the number of pulses detected over a programmed period. If the counter is gated by the Tach input and clocked by 100KHz (Mode 1), the internal counter will be latched into the reading register when the programmed number of edges is detected or when the counter reaches FFFFh. The internal counter is reset to zero after it is copied into this register. **Note:** In Mode 1, a counter value of FFFFh means that the Tach did not detect the programmed number of edges in 655ms. A stuck fan can be detected by setting the TACHx High Limit Register to a number less than FFFFh. If the internal counter then reaches FFFFh, the reading register will be set to FFFFh and an out-of-limit interrupt can be sent to the EC.	R	00h	RESET_SYS
15	TACH_INPUT_INT_EN 1=Enable Tach Input toggle interrupt from Tach block 0=Disable Tach Input toggle interrupt from Tach block	R/W	0b	RESET_SYS
14	COUNT_READY_INT_EN 1=Enable Count Ready interrupt from Tach block 0=Disable Count Ready interrupt from Tach block	R/W	0b	RESET_SYS
13	Reserved	R	-	-
12:11	TACH_EDGES A Tach signal is a square wave with a 50% duty cycle. Typically, two Tach periods represents one revolution of the fan. A Tach period consists of three Tach edges. This programmed value represents the number of Tach edges that will be used to determine the interval for which the number of 100KHz pulses will be counted 11b=9 Tach edges (4 Tach periods) 10b=5 Tach edges (2 Tach periods) 01b=3 Tach edges (1 Tach period) 00b=2 Tach edges (1/2 Tach period)	R/W	00b	RESET_SYS

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Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
10	TACH_READING_MODE_SELECT 1=Counter is incremented on the rising edge of the 100KHz input. The counter is latched into the TACHX_COUNTER field and reset when the programmed number of edges is detected. 0=Counter is incremented when Tach Input transitions from low-to-high state (default)	R/W	0b	RESET_SYS
9	Reserved	R	-	-
8	FILTER_ENABLE This filter is used to remove high frequency glitches from Tach Input. When this filter is enabled, Tach input pulses less than two 100KHz periods wide get filtered. 1=Filter enabled 0=Filter disabled (default) It is recommended that the Tach input filter always be enabled.	R/W	0b	RESET_SYS
7:2	Reserved	R	-	-
1	TACH_ENABLE This bit gates the clocks into the block. When clocks are gated, the TACHx pin is tristated. When re-enabled, the internal counters will continue from the last known state and stale status events may still be pending. Firmware should discard any status or reading values until the reading value has been updated at least one time after the enable bit is set. 1=TACH Monitoring enabled, clocks enabled. 0=TACH Idle, clocks gated	R/W	0b	RESET_SYS
0	TACH_OUT_OF_LIMIT_ENABLE This bit is used to enable the TACH_OUT_OF_LIMIT_STATUS bit in the TACHx Status Register to generate an interrupt event. 1=Enable interrupt output from Tach block 0=Disable interrupt output from Tach block (default)	R/W	0b	RESET_SYS

27.11.2 TACHX STATUS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3	COUNT_READY_STATUS This status bit is asserted when the Tach input changes state and when the counter value is latched. This bit remains cleared to '0' when the TACH_READING_MODE_SELECT bit in the TACHx Control Register is '0'. When the TACH_READING_MODE_SELECT bit in the TACHx Control Register is set to '1', this bit is set to '1' when the counter value is latched by the hardware. It is cleared when written with a '1'. If COUNT_READY_INT_EN in the TACHx Control Register is set to 1, this status bit will assert the Tach Interrupt signal. 1=Reading ready 0=Reading not ready	R/WC	0b	RESET_SYS
2	TOGGLE_STATUS This bit is set when Tach Input changes state. It is cleared when written with a '1b'. If TACH_INPUT_INT_EN in the TACHx Control Register is set to '1b', this status bit will assert the Tach Interrupt signal. 1=Tach Input changed state (this bit is set on a low-to-high or high-to-low transition) 0=Tach stable	R/WC	0b	RESET_SYS
1	TACH_PIN_STATUS This bit reflects the state of Tach Input. This bit is a read only bit that may be polled by the embedded controller. 1=Tach Input is high 0=Tach Input is low	R	0b	RESET_SYS
0	TACH_OUT_OF_LIMIT_STATUS This bit is set when the Tach Count value is greater than the high limit or less than the low limit. It is cleared when written with a '1b'. To disable this status event set the limits to their extreme values. If TACH_OUT_OF_LIMIT_ENABLE in the TACHx Control Register is set to 1', this status bit will assert the Tach Interrupt signal. 1=Tach is outside of limits 0=Tach is within limits	R/WC	0b	RESET_SYS

Note:

- Some fans offer a Locked Rotor output pin that generates a level event if a locked rotor is detected. This bit may be used in combination with the Tach pin status bit to detect a locked rotor signal event from a fan.
- Tach Input may come up as active for Locked Rotor events. This would not cause an interrupt event because the pin would not toggle. Firmware must read the status events as part of the initialization process, if polling is not implemented.

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27.11.3 TACHX HIGH LIMIT REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	-	-	-
15:0	TACH_HIGH_LIMIT This value is compared with the value in the TACHX_COUNTER field. If the value in the counter is greater than the value programmed in this register, the TACH_OUT_OF_LIMIT_STATUS bit will be set. The TACH_OUT_OF_LIMIT_STATUS status event may be enabled to generate an interrupt to the embedded controller via the TACH_OUT_OF_LIMIT_ENABLE bit in the TACHx Control Register.	R/W	FFFFh	RESET_SYS

27.11.4 TACHX LOW LIMIT REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	TACHX_LOW_LIMIT This value is compared with the value in the TACHX_COUNTER field of the TACHx Control Register. If the value in the counter is less than the value programmed in this register, the TACH_OUT_OF_LIMIT_STATUS bit will be set. The TACH_OUT_OF_LIMIT_STATUS status event may be enabled to generate an interrupt to the embedded controller via the TACH_OUT_OF_LIMIT_ENABLE bit in the TACHx Control Register To disable the TACH_OUT_OF_LIMIT_STATUS low event, program 0000h into this register.	R/W	0000h	RESET_SYS

28.0 PWM

28.1 Introduction

This block generates a PWM output that can be used to control 4-wire fans, blinking LEDs, and other similar devices. Each PWM can generate an arbitrary duty cycle output at frequencies from less than 0.1 Hz to 24 MHz.

The PWMx Counter ON Time registers and PWMx Counter OFF Time registers determine the operation of the PWM_OUTPUT signals. See Section 28.11.1, "PWMx Counter ON Time Register" and Section 28.11.2, "PWMx Counter OFF Time Register" for a description of the PWM_OUTPUT signals.

28.2 References

There are no standards referenced in this chapter.

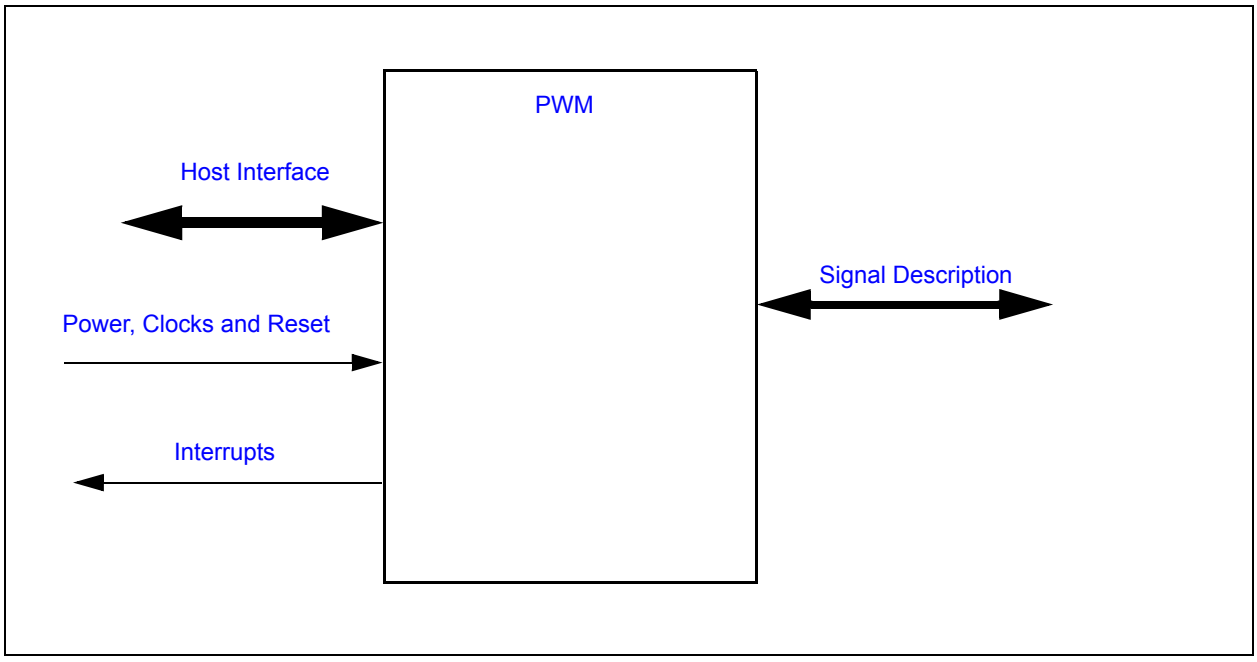
28.3 Terminology

There is no terminology defined for this section.

28.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 28-1: I/O DIAGRAM OF BLOCK



There are no external signals for this block.

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28.5 Signal Description

TABLE 28-1: SIGNAL DESCRIPTION

Name	Direction	Description
PWM_OUTPUT	OUTPUT	Pulse Width Modulated signal to PWMx pin.

28.6 Host Interface

The registers defined for the PWM Interface are accessible by the various hosts as indicated in Section 28.11, "EC Registers".

28.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

28.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

28.7.2 CLOCK INPUTS

Name	Description
48MHz	Clock input for generating high PWM frequencies, such as 15 kHz to 30 kHz.
100KHz	This is the clock input for generating low PWM frequencies, such as 10 Hz to 100 Hz.

28.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

28.8 Interrupts

The PWM block does not generate any interrupt events.

28.9 Low Power Modes

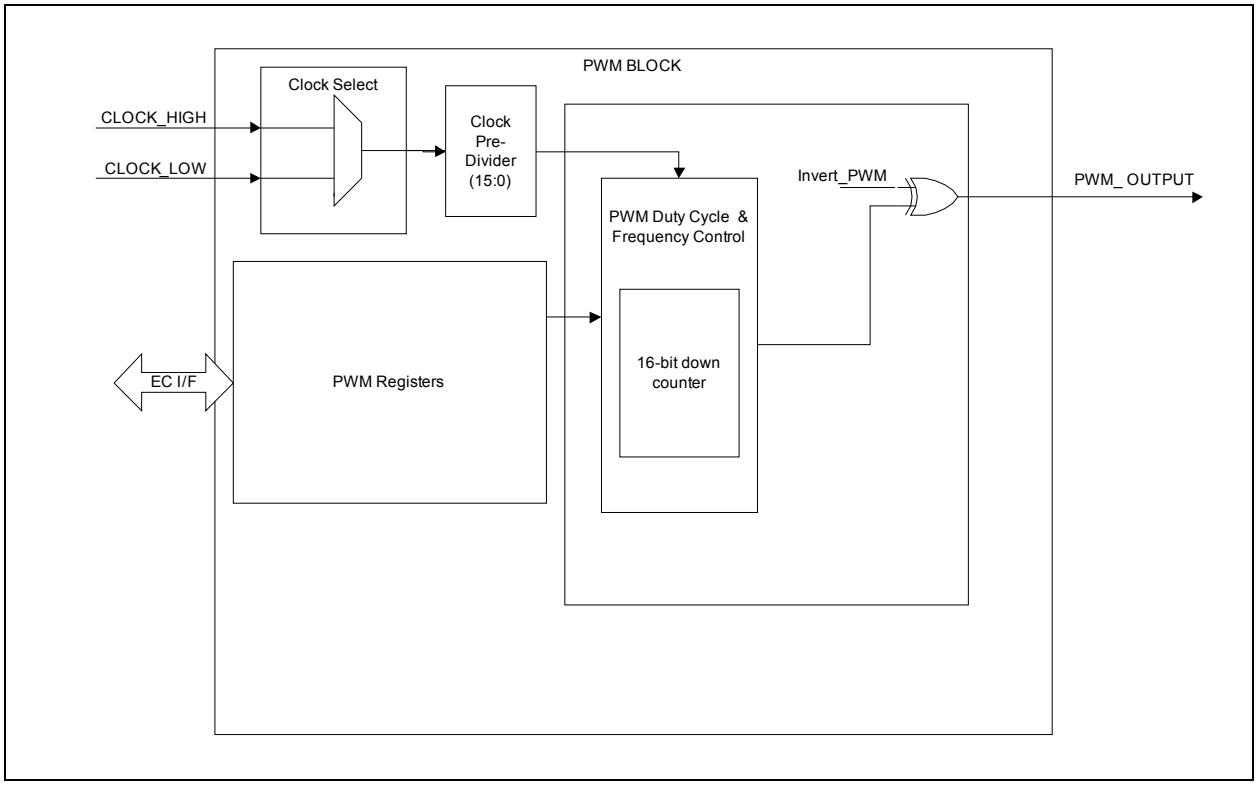
The PWM may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry. When the PWM is in the sleep state, the internal counters reset to 0 and the internal state of the PWM and the PWM_OUTPUT signal set to the OFF state.

28.10 Description

The PWM_OUTPUT signal is used to generate a duty cycle of specified frequency. This block can be programmed so that the PWM signal toggles the PWM_OUTPUT, holds it high, or holds it low. When the PWM is configured to toggle, the PWM_OUTPUT alternates from high to low at the rate specified in the PWMx Counter ON Time Register and PWMx Counter OFF Time Register.

The following diagram illustrates how the clock inputs and registers are routed to the PWM Duty Cycle & Frequency Control logic to generate the PWM output.

FIGURE 28-2: BLOCK DIAGRAM OF PWM CONTROLLER



Note: In Figure 28-2, the 48MHz clock is represented as CLOCK_HIGH and the 100KHz clock is represented as CLOCK_LOW.

The PWM clock source to the PWM Down Counter, used to generate a duty cycle and frequency on the PWM, is determined through the Clock select[1] and Clock Pre-Divider[6:3] bits in the PWMx Configuration Register register.

The PWMx Counter ON/OFF Time registers determine both the frequency and duty cycle of the signal generated on PWM_OUTPUT as described below.

The PWM frequency is determined by the selected clock source and the total on and off time programmed in the PWMx Counter ON Time Register and PWMx Counter OFF Time Register registers. The frequency is the time it takes (at that clock rate) to count down to 0 from the total on and off time.

The PWM duty cycle is determined by the relative values programmed in the PWMx Counter ON Time Register and PWMx Counter OFF Time Register registers.

The PWM Frequency Equation and PWM Duty Cycle Equation are shown below.

EQUATION 28-1: PWM FREQUENCY EQUATION

$$\text{PWM Frequency} = \frac{1}{(PreDivisor + 1)} \times \frac{(ClockSourceFrequency)}{((PWMCounterOnTime + 1) + (PWMCounterOffTime + 1))}$$

In this equation, the ClockSourceFrequency variable is the frequency of the clock source selected by the Clock Select bit in the PWMx Configuration Register, and PreDivisor is a field in the PWMx Configuration Register. The PWMCounterOnTime, PWMCounterOffTime are registers that are defined in Section 28.11, "EC Registers".

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EQUATION 28-2: PWM DUTY CYCLE EQUATION

$$\text{PWM Duty Cycle} = \frac{(PWMCounterOnTime + 1)}{((PWMCounterOnTime + 1) + (PWMCounterOffTime + 1))}$$

The PWMx Counter ON Time Register and PWMx Counter OFF Time Register registers should be accessed as 16-bit values.

28.10.1 PWM REGISTER UPDATES

The PWMx Counter ON Time Register and PWMx Counter OFF Time Register may be updated at any time. Values written into the two registers are kept in holding registers. The holding registers are transferred into the two user-visible registers when all four bytes have been written with new values and the internal counter completes the OFF time count. If the PWM is in the Full On state then the two user-visible registers are updated from the holding registers as soon as all four bytes have been written. Once the two registers have been updated the holding registers are marked empty. and all four bytes must again be written before the holding registers will be reloaded into the On Time Register and the Off Time Register. Reads of both registers return the current contents of the registers that are used to load the counter and not the holding registers.

28.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the PWM Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 28-2: REGISTER SUMMARY

Offset	Register Name
00h	PWMx Counter ON Time Register
04h	PWMx Counter OFF Time Register
08h	PWMx Configuration Register

28.11.1 PWMX COUNTER ON TIME REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	PWMX_COUNTER_ON_TIME This field determine both the frequency and duty cycle of the PWM signal. Setting this field to a value of *n* will cause the On time of the PWM to be *n*+1 cycles of the PWM Clock Source. When this field is set to zero and the PWMX_COUNTER_OFF_-TIME is not set to zero, the PWM_OUTPUT is held low (Full Off).	R/W	0000h	RESET_SYS

28.11.2 PWMX COUNTER OFF TIME REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	PWMX_COUNTER_OFF_TIME This field determine both the frequency and duty cycle of the PWM signal. Setting this field to a value of *n* will cause the Off time of the PWM to be *n*+1 cycles of the PWM Clock Source. When this field is set to zero, the PWM_OUTPUT is held high (Full On).	R/W	FFFFh	RESET_SYS

28.11.3 PWMX CONFIGURATION REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6:3	CLOCK_PRE_DIVIDER The Clock source for the 16-bit down counter (see PWMx Counter ON Time Register and PWMx Counter OFF Time Register) is determined by bit D1 of this register. The Clock source is then divided by the value of Pre-Divider+1 and the resulting signal determines the rate at which the down counter will be decremented. For example, a Pre-Divider value of 1 divides the input clock by 2 and a value of 2 divides the input clock by 3. A Pre-Divider of 0 will disable the Pre-Divider option.	R/W	0000b	RESET_SYS
2	INVERT 1=PWM_OUTPUT ON State is active low 0=PWM_OUTPUT ON State is active high	R/W	0b	RESET_SYS
1	CLOCK_SELECT This bit determines the clock source used by the PWM duty cycle and frequency control logic. 1=CLOCK_LOW 0=CLOCK_HIGH	R/W	0b	RESET_SYS
0	PWM_ENABLE When the PWM_ENABLE is set to 0 the internal counters are reset and the internal state machine is set to the OFF state. In addition, the PWM_OUTPUT signal is set to the inactive state as determined by the Invert bit. The PWMx Counter ON Time Register and PWMx Counter OFF Time Register are not affected by the PWM_ENABLE bit and may be read and written while the PWM enable bit is 0. 1=Enabled (default) 0=Disabled (gates clocks to save power)	R/W	0b	RESET_SYS

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29.0 PECI INTERFACE

29.1 Overview

The MEC170x includes a PECI Interface to allow the EC to retrieve temperature readings from PECI-compliant devices. The PECI Interface implements the PHY and Link Layer of a PECI host controller as defined in References[1] and includes hardware support for the PECI 2.0 command set.

This chapter focuses on MEC170x-specific PECI Interface configuration information such as Power Domains, Clock Inputs, Resets, Interrupts, and other chip specific information. For a functional description of the MEC170x PECI Interface refer to References [1].

29.2 References

1. PECI Interface Core, Rev. 1.31, Core-Level Architecture Specification, Microchip Confidential, 4/15/11

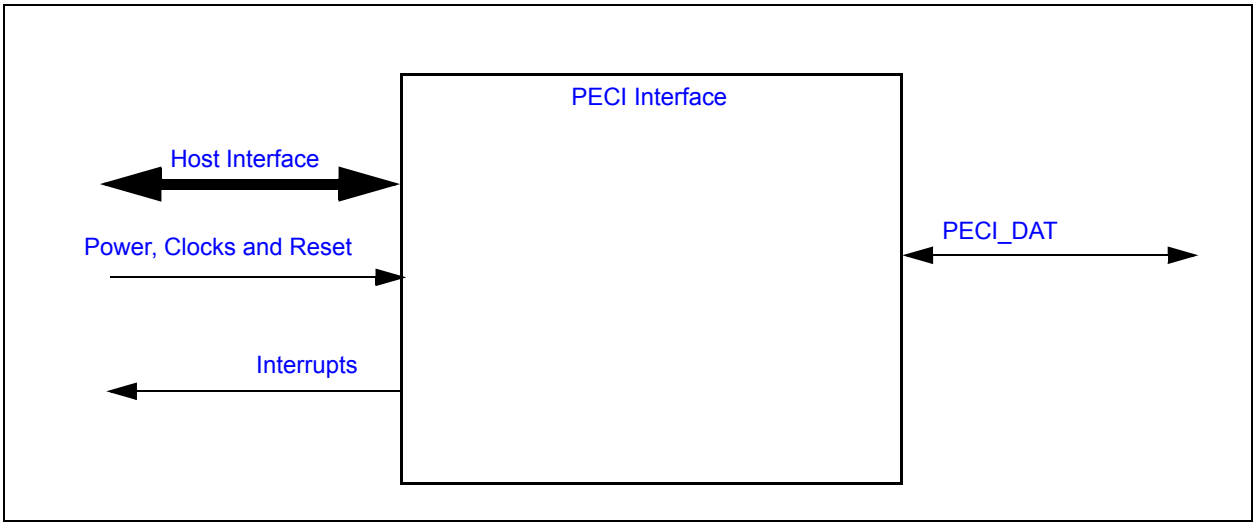
29.3 Terminology

No terminology has been defined for this chapter.

29.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 29-1: PECI INTERFACE I/O DIAGRAM



29.5 Signal Description

The Signal Description Table lists the signals that are typically routed to the pin interface.

TABLE 29-1: SIGNAL DESCRIPTION

Name	Direction	Description
PECI_DAT	Input/Output	PECI Data signal pin

Note: Routing guidelines for the PECI_DAT pin is provided in Intel Platform design guides. Refer to the appropriate Intel document for current information. See Table 29-2.

TABLE 29-2: PECI ROUTING GUIDELINES

Trace Impedance	50 Ohms +/- 15%
Spacing	10 mils
Routing Layer	Microstrip
Trace Width	Calculate to match impedance
Length	1” - 15”

29.6 Host Interface

The registers defined for the PECI Interface are accessible by the various hosts as indicated in Section 29.11, "EC Registers".

29.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

29.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

29.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the main system clock. (note)

Note: PECI Module Input Clock is an 8MHz clock derived from the 48MHz clock input. An 8MHz clock supports a maximum Optimal Bit Time of 500 kbps. The Optimal Bit Time is determined by the value programmed into the Optimal Bit Time registers at offset 20h and 24h.

29.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

29.8 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 29-3: EC INTERRUPTS

Source	Description
PECIHOST	PECI Host

29.9 Low Power Modes

The PECI Interface may be put into a low power state by the chip’s Power, Clocks, and Reset (PCR) circuitry.

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29.10 Instance Description

There is one instance of the PECI Core implemented in the PECI Interface in the MEC170x. See Reference [1], PECI Interface Core, Rev. 1.31, Core-Level Architecture Specification, Microchip Confidential, 4/15/11, for a description of the PECI Core.

Note:	If the PECI interface is not in use, the PECI_DISABLE bit in the PECI Disable Register must be set to ‘1b’ in order to minimize leakage current.

29.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the PECI Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 29-4: REGISTER SUMMARY

Offset	Register Name
00h	Write Data Register
04h	Read Data Register
08h	Control Register
0Ch	Status Register 1
10h	Status Register 2
14h	Error Register
18h	Interrupt Enable 1 Register
1Ch	Interrupt Enable 2 Register
20h	Optimal Bit Time Register (Low Byte)
24h	Optimal Bit Time Register (High Byte)
28h	TEST
2Ch	TEST
40h	Block ID Register
44h	Revision Register
48h - 7Ch	Test

For register details see References [1].

30.0 ANALOG TO DIGITAL CONVERTER

30.1 Introduction

This block is designed to convert external analog voltage readings into digital values. It consists of a single successive-approximation Analog-Digital Converter that can be shared among multiple inputs.

30.2 References

No references have been cited for this chapter

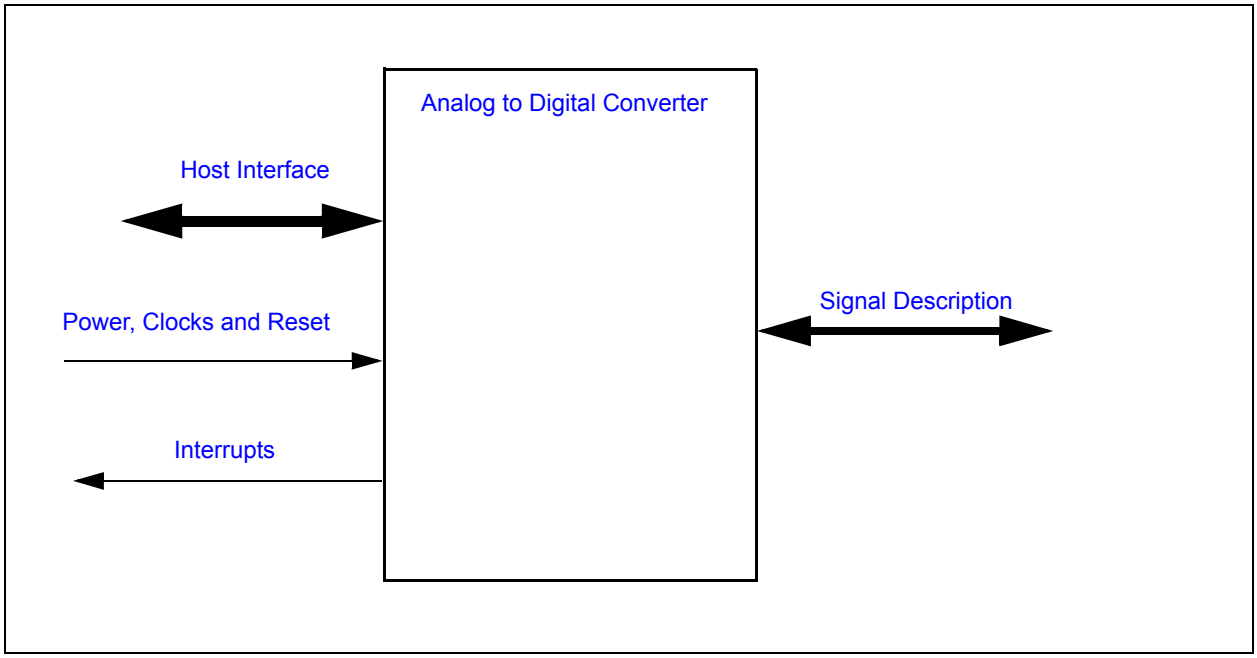
30.3 Terminology

No terminology is defined for this chapter

30.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 30-1: I/O DIAGRAM OF BLOCK



30.5 Signal Description

The Signal Description Table lists the signals that are typically routed to the pin interface.

TABLE 30-1: SIGNAL DESCRIPTION

Name	Direction	Description
ADC [15:0]	Input	ADC Analog Voltage Input from pins. **Note:** The ADC IP supports up to 16 channels. The number of channels implemented is package dependent. Refer to the Pin Chapter for the number of channels implemented in a package.

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30.6 Host Interface

The registers defined for the ADC are accessible by the various hosts as indicated in Section 30.11, "EC Registers".

30.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

30.7.1 POWER DOMAINS

TABLE 30-2: POWER SOURCES

Name	Description
VTR	This power well supplies power for the registers tn this block.
VTR_ANALOG	This power well supplies power for the analog circuitry in this block.

30.7.2 CLOCK INPUTS

TABLE 30-3: CLOCK INPUTS

Name	Description
16MHz	This derived clock signal drives controls the conversion rate of the ADC. At 16MHz, the ADC does one channel conversion in 1.125µS.

30.7.3 RESETS

TABLE 30-4: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in this block.

30.8 Interrupts

TABLE 30-5: EC INTERRUPTS

Source	Description
ADC_Single_Int	Interrupt signal from ADC controller to EC for Single-Sample ADC conversion.
ADC_Repeat_Int	Interrupt signal from ADC controller to EC for Repeated ADC conversion.

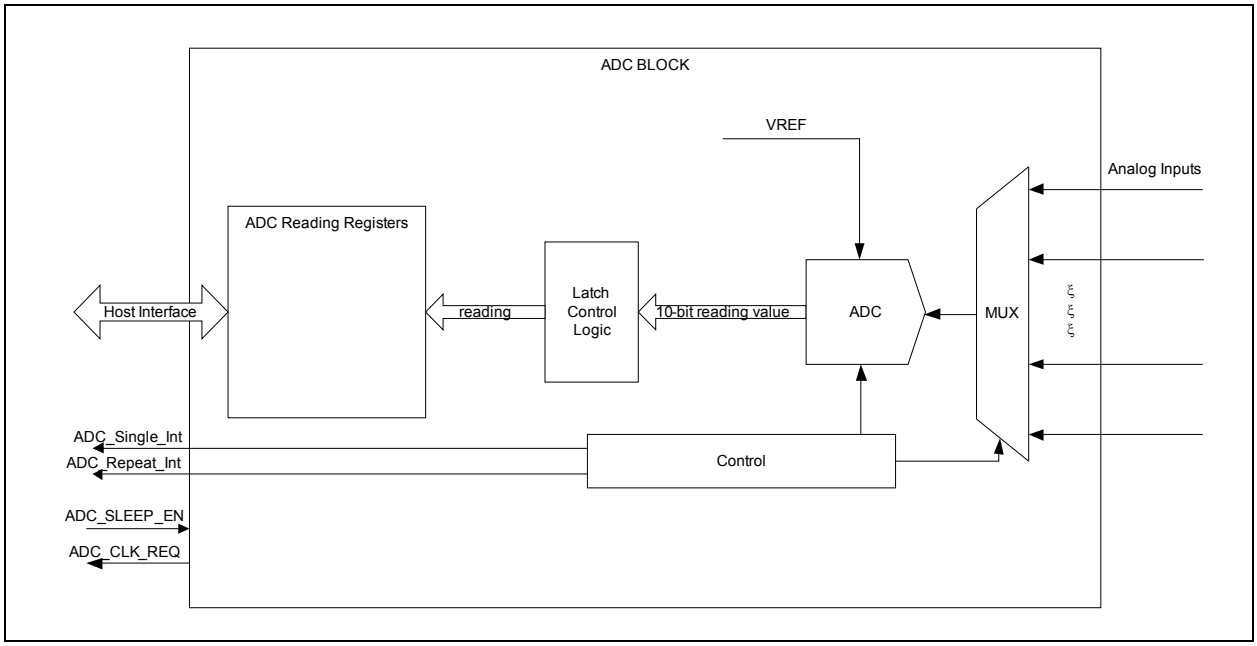
30.9 Low Power Modes

The ADC may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

The ADC is designed to conserve power when it is either sleeping or disabled. It is disabled via the ACTIVATE Bit and sleeps when the ADC_SLEEP_EN signal is asserted. The sleeping state only controls clocking in the ADC and does not power down the analog circuitry. For lowest power consumption, the ADC ACTIVATE bit must be set to '0.'

30.10 Description

FIGURE 30-2: ADC BLOCK DIAGRAM



The MEC170x features a sixteen channel successive approximation Analog to Digital Converter. The ADC architecture features excellent linearity and converts analog signals to 10 bit words. Conversion takes less than 1.125 microseconds per 10-bit word. The sixteen channels are implemented with a single high speed ADC fed by a sixteen input analog multiplexer. The multiplexer cycles through the sixteen voltage channels, starting with the lowest-numbered channel and proceeding to the highest-number channel, selecting only those channels that are programmed to be active.

The input range on the voltage channels spans from 0V to the voltage reference. With an voltage reference of 3.3V, this provides resolutions of 3.2mV. The range can easily be extended with the aid of resistor dividers. The accuracy of any voltage reading depends on the accuracy and stability of the voltage reference input.

Note:	The ADC pins are 3.3V tolerant.

The ADC conversion cycle starts either when the START_SINGLE bit in the ADC to set to 1 or when the ADC Repeat Timer counts down to 0. When the START_SINGLE is set to 1 the conversion cycle converts channels enabled by configuration bits in the ADC Single Register. When the Repeat Timer counts down to 0 the conversion cycle converts channels enabled by configuration bits in the ADC Repeat Register. When both the START_SINGLE bit and the Repeat Timer request conversions the START_SINGLE conversion is completed first.

Conversions always start with the lowest-numbered enabled channel and proceed to the highest-numbered enabled channel.

Note:	If software repeatedly sets Start_Single to 1 at a rate faster than the Repeat Timer count down interval, the conversion cycle defined by the ADC Repeat Register will not be executed.

30.10.1 REPEAT MODE

- Repeat Mode will start a conversion cycle of all ADC channels enabled by bits RPT_EN in the ADC Repeat Register. The conversion cycle will begin after a delay determined by START_DELAY in the ADC Delay Register.
- After all channels enabled by RPT_EN are complete, REPEAT_DONE_STATUS will be set to 1. This status bit is cleared when the next repeating conversion cycle begins to give a reflection of when the conversion is in progress.

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- As long as START_REPEAT is 1 the ADC will repeatedly begin conversion cycles with a period defined by REPEAT_DELAY.
- If the delay period expires and a conversion cycle is already in progress because START_SINGLE was written with a 1, the cycle in progress will complete, followed immediately by a conversion cycle using RPT_EN to control the channel conversions.

30.10.2 SINGLE MODE

- The Single Mode conversion cycle will begin without a delay. After all channels enabled by SINGLE_EN are complete, SINGLE_DONE_STATUS will be set to 1. When the next conversion cycle begins the bit is cleared.
- If START_SINGLE is written with a 1 while a conversion cycle is in progress because START_REPEAT is set, the conversion cycle will complete, followed immediately by a conversion cycle using SINGLE_EN to control the channel conversions.

30.10.3 APPLICATION NOTES

Transitions on ADC GPIOs are not permitted when Analog to Digital Converter readings are being taken.

Note:	ADC inputs require at least a 0.1 uF capacitor to filter glitches. See the MEC170x PCB Layout Guide for ADC filtering recommendations.

30.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Analog to Digital Converter Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 30-6: REGISTER SUMMARY

Offset	Register Name
00h	ADC Control Register
04h	ADC Delay Register
08h	ADC Status Register
0Ch	ADC Single Register
10h	ADC Repeat Register
14h	ADC Channel 0 Reading Register
18h	ADC Channel 1 Reading Register
1Ch	ADC Channel 2 Reading Register
20h	ADC Channel 3 Reading Register
24h	ADC Channel 4 Reading Register
28h	ADC Channel 5 Reading Register
2Ch	ADC Channel 6 Reading Register
30h	ADC Channel 7 Reading Register
34h	ADC Channel 8 Reading Register
38h	ADC Channel 9 Reading Register
3Ch	ADC Channel 10 Reading Register
40h	ADC Channel 11 Reading Register
44h	ADC Channel 12 Reading Register
48h	ADC Channel 13 Reading Register
4Ch	ADC Channel 14 Reading Register
50h	ADC Channel 15 Reading Register

30.11.1 ADC CONTROL REGISTER

The ADC Control Register is used to control the behavior of the Analog to Digital Converter.

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7	SINGLE_DONE_STATUS This bit is cleared when it is written with a 1. Writing a 0 to this bit has no effect. This bit can be used to generate an EC interrupt. 1=ADC single-sample conversion is completed. This bit is set to 1 when all enabled channels in the single conversion cycle 0=ADC single-sample conversion is not complete. This bit is cleared whenever an ADC conversion cycle begins for a single conversion cycle	R/WC	0h	RESET_SYS
6	REPEAT_DONE_STATUS This bit is cleared when it is written with a 1. Writing a 0 to this bit has no effect. This bit can be used to generate an EC interrupt. 1=ADC repeat-sample conversion is completed. This bit is set to 1 when all enabled channels in a repeating conversion cycle complete 0=ADC repeat-sample conversion is not complete. This bit is cleared whenever an ADC conversion cycle begins for a repeating conversion cycle	R/WC	0h	RESET_SYS
5	Reserved	R	-	-
4	SOFT_RESET 1=writing one causes a reset of the ADC block hardware (not the registers) 0=writing zero takes the ADC block out of reset	R/W	0h	RESET_SYS
3	POWER_SAVER_DIS 1=Power saving feature is disabled 0=Power saving feature is enabled. The Analog to Digital Converter controller powers down the ADC between conversion sequences.	R/W	0h	RESET_SYS
2	START_REPEAT 1=The ADC Repeat Mode is enabled. This setting will start a conversion cycle of all ADC channels enabled by bits RPT_EN in the ADC Repeat Register. 0=The ADC Repeat Mode is disabled. Note: This setting will not terminate any conversion cycle in process, but will clear the Repeat Timer and inhibit any further periodic conversions.	R/W	0h	RESET_SYS

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Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	START_SINGLE 1=The ADC Single Mode is enabled. This setting starts a single conversion cycle of all ADC channels enabled by bits SINGLE_EN in the ADC Single Register. 0=The ADC Single Mode is disabled. This bit is self-clearing	R/W	0h	RESET_SYS
0	ACTIVATE 1=ADC block is enabled for operation. START_SINGLE or START_REPEAT can begin data conversions by the ADC. Note: A reset pulse is sent to the ADC core when this bit changes from 0 to 1. 0=The ADC is disabled and placed in its lowest power state. Note: Any conversion cycle in process will complete before the block is shut down, so that the reading registers will contain valid data but no new conversion cycles will begin.	R/W	0h	RESET_SYS

30.11.2 ADC DELAY REGISTER

The ADC Delay register determines the delay from setting START_REPEAT in the ADC Control Register and the start of a conversion cycle. This register also controls the interval between conversion cycles in repeat mode.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	REPEAT_DELAY This field determines the interval between conversion cycles when START_REPEAT is 1. The delay is in units of 40µs. A value of 0 means no delay between conversion cycles, and a value of 0xFFFF means a delay of 2.6 seconds. This field has no effect when START_SINGLE is written with a 1.	R/W	0000h	RESET_SYS
15:0	START_DELAY This field determines the starting delay before a conversion cycle is begun when START_REPEAT is written with a 1. The delay is in units of 40µs. A value of 0 means no delay before the start of a conversion cycle, and a value of 0xFFFF means a delay of 2.6 seconds. This field has no effect when START_SINGLE is written with a 1.	R/W	0000h	RESET_SYS

30.11.3 ADC STATUS REGISTER

The ADC Status Register indicates whether the ADC has completed a conversion cycle.

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	ADC_CH_STATUS All bits are cleared by being written with a '1'. 1=conversion of the corresponding ADC channel is complete 0=conversion of the corresponding ADC channel is not complete For enabled single cycles, the SINGLE_DONE_STATUS bit in the ADC Control Register is also set after all enabled channel conversion are done; for enabled repeat cycles, the REPEAT_DONE_STATUS in the ADC Control Register is also set after all enabled channel conversion are done.	R/WC	00h	RESET_SYS

30.11.4 ADC SINGLE REGISTER

The ADC Single Register is used to control which ADC channel is captured during a Single-Sample conversion cycle initiated by the START_SINGLE bit in the ADC Control Register.

Note:	Do not change the bits in this register in the middle of a conversion cycle to insure proper operation.

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	SINGLE_EN Each bit in this field enables the corresponding ADC channel when a single cycle of conversions is started when the START_SINGLE bit in the ADC Control Register is written with a 1. 1=single cycle conversions for this channel are enabled 0=single cycle conversions for this channel are disabled	R/W	0h	RESET_SYS

30.11.5 ADC REPEAT REGISTER

The ADC Repeat Register is used to control which ADC channels are captured during a repeat conversion cycle initiated by the START_REPEAT bit in the ADC Control Register.

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	RPT_EN Each bit in this field enables the corresponding ADC channel for each pass of the Repeated ADC Conversion that is controlled by bit START_REPEAT in the ADC Control Register. 1=repeat conversions for this channel are enabled 0=repeat conversions for this channel are disabled	R/W	00h	RESET_SYS

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30.11.6 ADC CHANNEL READING REGISTERS

All 16 ADC channels return their results into a 32-bit reading register. In each case the low 10 bits of the reading register return the result of the Analog to Digital conversion and the upper 22 bits return 0. Table 30-6, "Register Summary" shows the addresses of all the reading registers.

Note: The ADC Channel Reading Registers access require single 16, or 32 bit reads; i.e., two 8 bit reads will not provide data coherency.

31.0 RPM-PWM INTERFACE

31.1 Introduction

The RPM-PWM Interface is a closed-loop RPM based Fan Control Algorithm that monitors a fan's speed and automatically adjusts the drive to the fan in order to maintain the desired fan speed.

The RPM-PWM Interface functionality consists of a closed-loop "set-and-forget" RPM-based fan controller.

31.2 References

No references have been cited for this chapter

31.3 Terminology

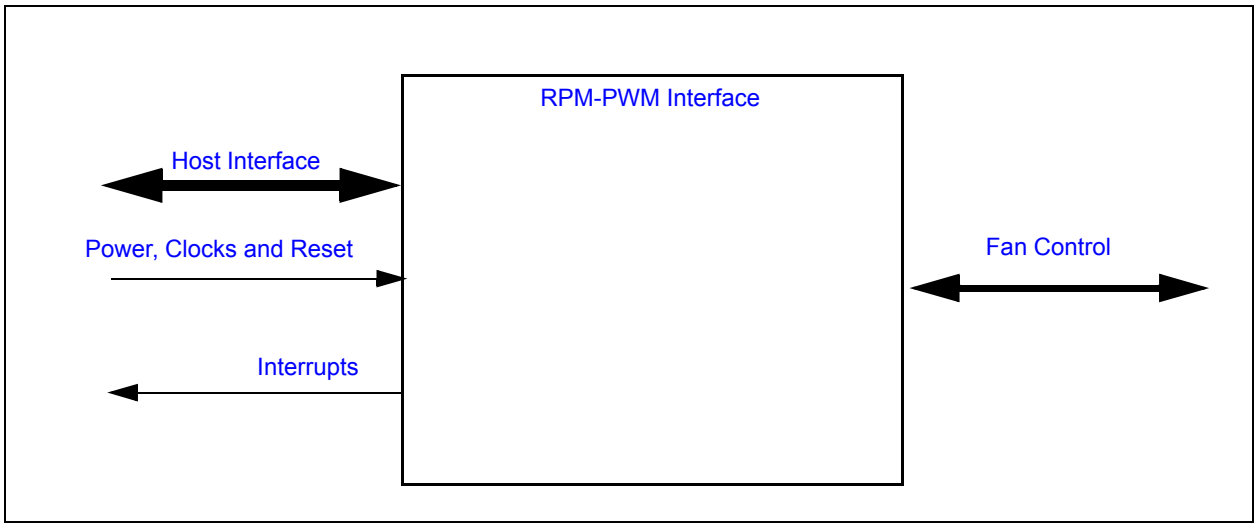
There is no terminology defined for this chapter.

31.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

The registers in the block are accessed by embedded controller code at the addresses shown in Section 31.9, "EC Registers".

FIGURE 31-1: RPM-PWM INTERFACE I/O DIAGRAM



31.4.1 FAN CONTROL

The Fan Control Signal Description Table lists the signals that are routed to/from the block.

Name	Direction	Description
GTACH	Input	Tachometer input from fan
GPWM	Output	PWM fan drive output

31.4.2 HOST INTERFACE

The registers defined for the RPM-PWM Interface are accessible by the various hosts as indicated in Section 31.9, "EC Registers".

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31.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

31.5.1 POWER DOMAINS

Name	Description
VTR	This power well sources the registers and logic in this block.

31.5.2 CLOCK INPUTS

Name	Description
48MHz	This clock signal drives selected logic (e.g., counters).
32KHz	This clock signal drives selected logic (e.g., counters).

31.5.3 RESETS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in this block.

31.6 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
FAN_FAIL	The DRIVE_FAIL & FAN_SPIN bits in the Fan Status Register are logically ORed and routed to the FAIL_SPIN Interrupt
FAN_STALL	The FAN_STALL bit in the Fan Status Register is routed to the FAN_STALL Interrupt

31.7 Low Power Modes

The RPM-PWM Interface may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

31.8 Description

This section defines the functionality of the block.

31.8.1 GENERAL OPERATION

The RPM-PWM Interface is an RPM based Fan Control Algorithm that monitors the fan's speed and automatically adjusts the drive to maintain the desired fan speed. This RPM based Fan Control Algorithm controls a PWM output based on a tachometer input.

31.8.2 FAN CONTROL MODES OF OPERATION

The RPM-PWM Interface has two modes of operation for the PWM Fan Driver. They are:

1. Manual Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 31.9.1, "Fan Setting Register") will update the fan drive based on the programmed ramp rate (default disabled).

- The Manual Mode is enabled by clearing the EN_ALGO bit in the Fan Configuration Register (see Section 31.9.2, "Fan Configuration Register").
- Whenever the Manual Mode is enabled the current drive settings will be changed to what was last used by the RPM control algorithm.
- Setting the drive value to 00h will disable the PWM Fan Driver.
- Changing the drive value from 00h will invoke the Spin Up Routine.

2. Using RPM based Fan Control Algorithm - in this mode of operation, the user determines a target tachometer reading and the drive setting is automatically updated to achieve this target speed.

Manual Mode	Algorithm
Fan Driver Setting (read / write)	Fan Driver Setting (read only)
EDGES[1:0] (Fan Configuration)	EDGES[1:0] (Fan Configuration)
UPDATE[2:0] (Fan configuration)	UPDATE[2:0] (Fan configuration)
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Step	Fan Step
-	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
-	TACH Target
TACH Reading	TACH Reading
RANGE[2:0] (Fan Configuration 2)	RANGE[2:0] (Fan Configuration 2)
-	DRIVE_FAIL_CNT[2:0] (Spin Up Config) and Drive Fail Band

31.8.3 RPM BASED FAN CONTROL ALGORITHM

The RPM-PWM Interface includes an RPM based Fan Control Algorithm.

The fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source. Figure 31-2, "RPM based Fan Control Algorithm" shows a simple flow diagram of the RPM based Fan Control Algorithm operation.

The desired tachometer count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPMs, the user would input the hexadecimal equivalent of 1312d (52_00h in the TACH Target Registers). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs (see Section 31.9.10, "TACH Target Register" and Section 31.9.11, "TACH Reading Register").

The RPM-PWM Interface's RPM based Fan Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the interrupt signal. The RPM-PWM Interface works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal.

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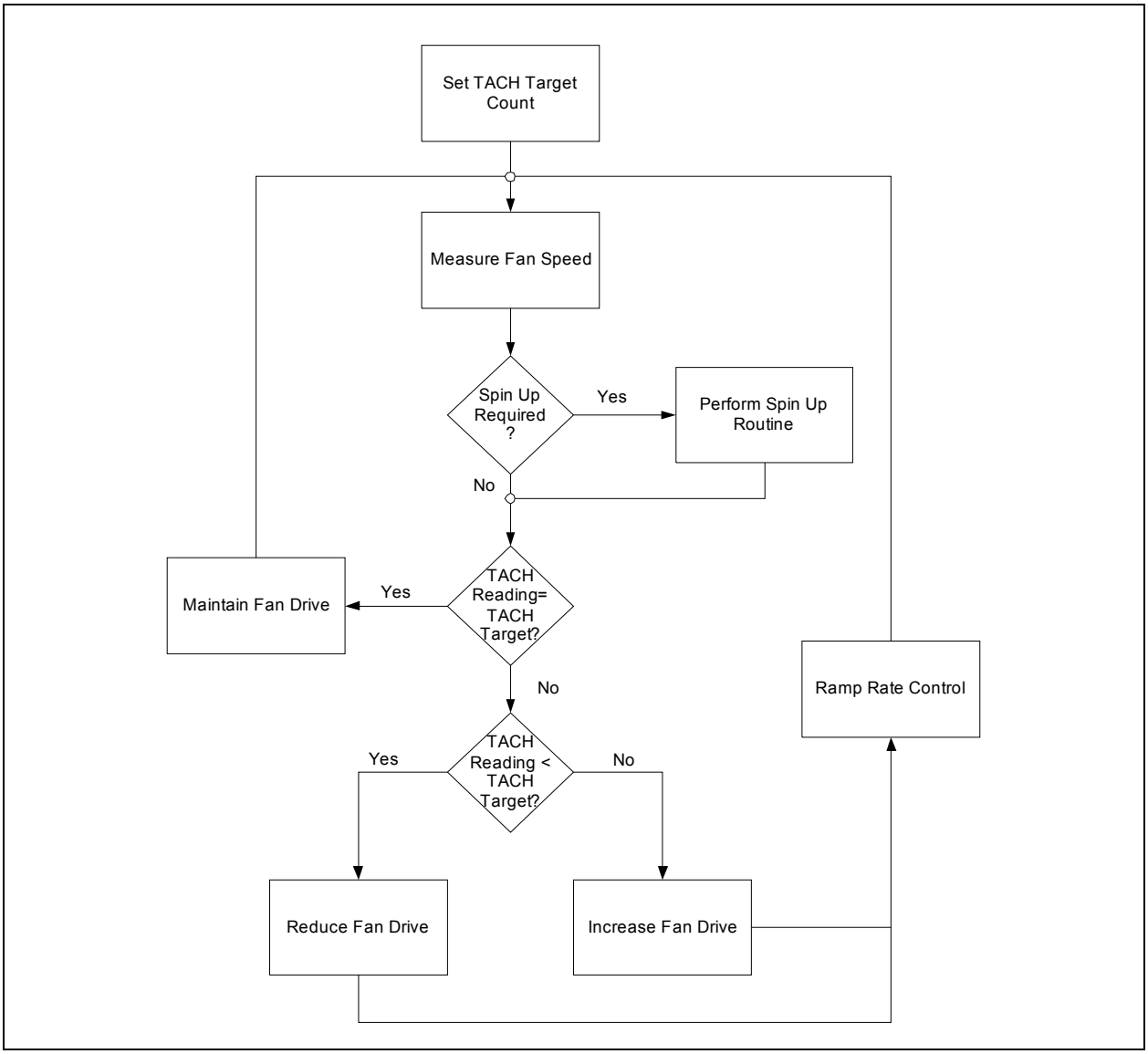
FIGURE 31-2: RPM BASED FAN CONTROL ALGORITHM



31.8.3.1 Programming the RPM Based Fan Control Algorithm

The RPM based Fan Control Algorithm powers-up disabled. The following registers control the algorithm. The RPM-PWM Interface fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

1. Set the Valid TACH Count Register to the minimum tachometer count that indicates the fan is spinning.
2. Set the Spin Up Configuration Register to the spin up level and Spin Time desired.
3. Set the Fan Step Register to the desired step size.
4. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
5. Set the Update Time, and Edges options in the Fan Configuration Register.
6. Set the TACH Target Register to the desired tachometer count.
7. Enable the RPM based Fan Control Algorithm by setting the EN_ALGO bit.

31.8.3.2 Tachometer Measurement

In both modes of operation, the tachometer measurement operates independently of the mode of operation of the fan driver and RPM based Fan Speed Control algorithm. Any tachometer reading that is higher than the Valid TACH Count (see Section 31.9.8, "Valid TACH Count Register") will flag a stalled fan and trigger an interrupt.

When measuring the tachometer, the fan must provide a valid tachometer signal at all times to ensure proper operation. The tachometer measurement circuitry is programmable to detect the fan speed of a variety of fan configurations and architectures including 1-pole, 2-pole (default), 3-pole, and 4-pole fans.

Note:	The tachometer measurement works independently of the drive settings. If the device is put into manual mode and the fan drive is set at a level that is lower than the fan can operate (including zero drive), the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

STALLED FAN

If the TACH Reading Register exceeds the user-programmable Valid TACH Count setting, it will flag the fan as stalled and trigger an interrupt. If the RPM based Fan Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Manual Mode is enabled or whenever the drive value is changed from 00h, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Section 31.9.5, "Fan Spin Up Configuration Register") to allow the fan an opportunity to reach a valid speed without generating unnecessary interrupts.
- In Manual Mode, whenever the TACH Reading Register exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When the RPM based Fan Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

31.8.3.3 Spin Up Routine

The RPM-PWM Interface also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation. The Spin Up Routine is initiated under the following conditions:

- The TACH Target High Byte Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 31.9.8, "Valid TACH Count Register").
- The RPM based Fan Control Algorithm's measured tachometer reading is greater than the Valid TACH Count.
- When in Manual Mode, the Drive Setting changes from a value of 00h.

When the Spin Up Routine is operating, the fan driver is set to full scale for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (30% to 65% drive).

After the Spin Up Routine has finished, the RPM-PWM Interface measures the tachometer. If the measured tachometer reading is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Note:	When the device is operating in manual mode, the FAN_SPIN status bit may be set if the fan drive is set at a level that is lower than the fan can operate (excluding zero drive which disables the fan driver). If the FAN_SPIN interrupt is unmasked, this condition will trigger an errant interrupt.

Figure 31-3, "Spin Up Routine" shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

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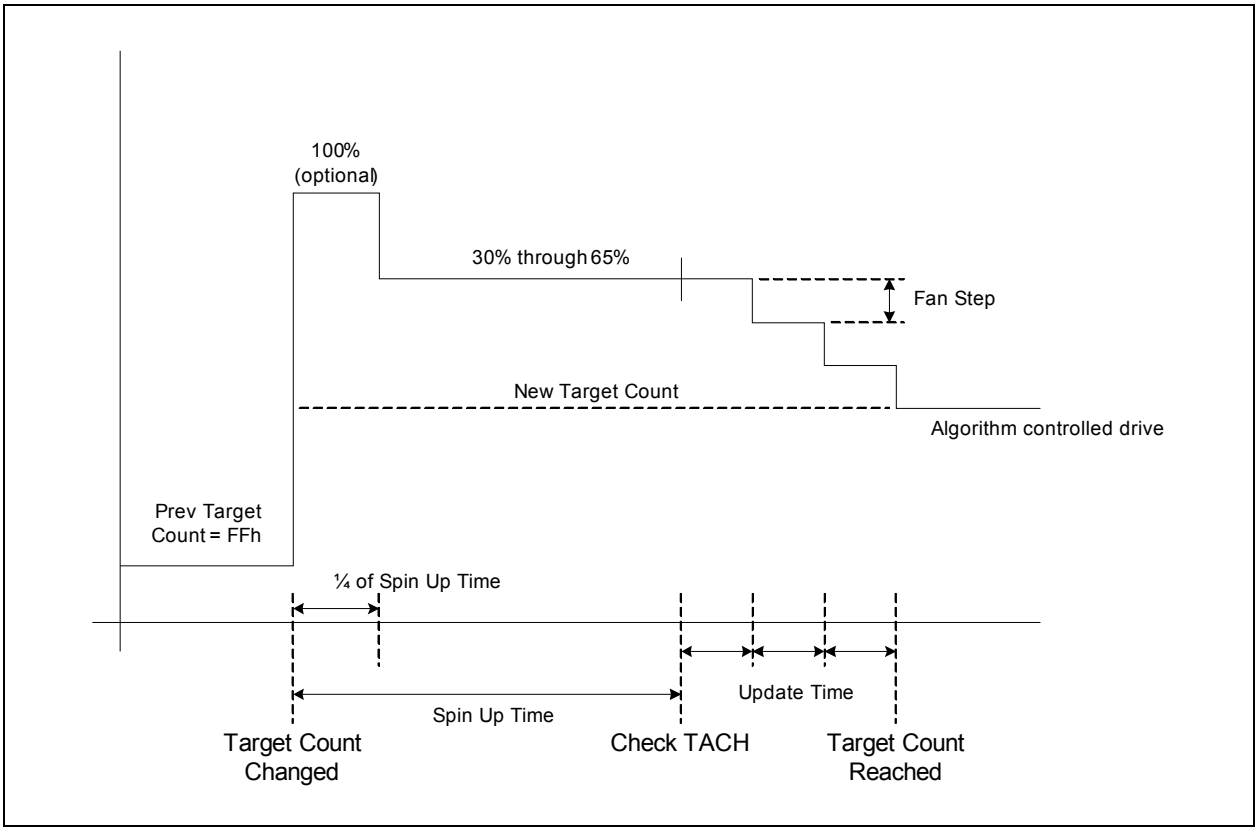
FIGURE 31-3: SPIN UP ROUTINE



31.8.4 PWM DRIVER

The RPM-PWM Interface contains an optional, programmable 10-bit PWM driver which can serve as part of the RPM based Fan Speed Control Algorithm or in Manual Mode.

When enabled, the PWM driver can operate in four programmable frequency bands. The lower frequency bands offer frequencies in the range of 9.5Hz to 4.8kHz while the higher frequency options offer frequencies of 21Hz or 25.2kHz.

The highest frequency available, 25.2KHz, operates in 8-bit resolution. All other PWM frequencies operate in 10-bit resolution.

31.8.5 FAN SETTING

The Fan Setting Registers are used to control the output of the Fan Driver. The driver setting operates independently of the Polarity bit for the PWM output. That is, a setting of 0000h will mean that the fan drive is at minimum drive while a value of FFC0h will mean that the fan drive is at maximum drive.

If the Spin Up Routine is invoked, reading from the registers will return the current fan drive setting that is being used by the Spin Up Routine instead of what was previously written into these registers.

The Fan Driver Setting Registers, when the RPM based Fan Control Algorithm is enabled, are read only. Writing to the register will have no effect and the data will not be stored. Reading from the register will always return the current fan drive setting.

If the INT_PWRGD pin is de-asserted, the Fan Driver Setting Register will be made read only. Writing to the register will have no effect and reading from the register will return 0000h.

When the RPM based Fan Control Algorithm is disabled, the current fan drive setting that was last used by the algorithm is retained and will be used.

If the Fan Driver Setting Register is set to a value of 0000h, all tachometer related status bits will be masked until the setting is changed. Likewise, the FAN_SHORT bit will be cleared and masked until the setting is changed.

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The contents of the register represent the weighting of each bit in determining the final duty cycle. The output drive for a PWM output is given by the following equation:

- Drive = (FAN_SETTING VALUE/1023) x 100%.

The PWM Divide Register determines the final PWM frequency. The base frequency set by the PWM_BASE[1:0] bits is divided by the decimal equivalent of the register settings.

The final PWM frequency is derived as the base frequency divided by the value of this register as shown in the equation below:

- PWM_Frequency = base_clk / PWM_D

Where:

- base_clk = The base frequency set by the PWMx_CFG[1:0] bits
- PWM_D = the divide setting set by the PWM Divide Register.

31.8.6 ALERTS AND LIMITS

Figure 31-4, "Interrupt Flow" shows the interactions of the interrupts for fan events.

If the Fan Driver detects a drive fail, spin-up or stall event, the interrupt signal will be asserted (if enabled).

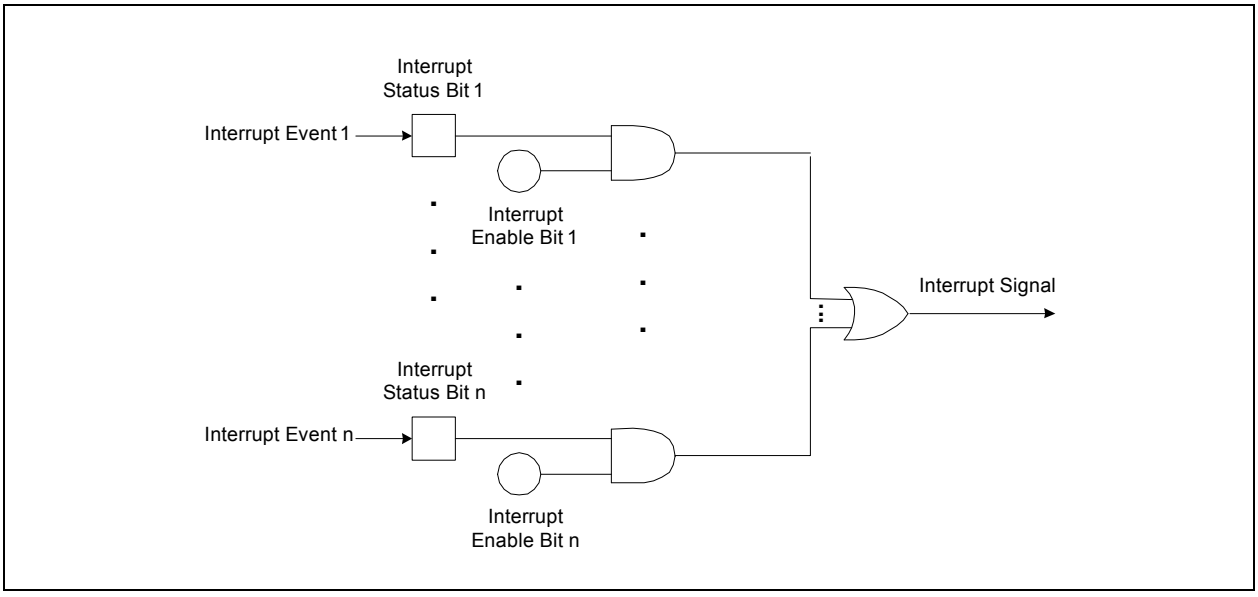
All of these interrupts can be masked from asserting the interrupt signal individually. If any bit of either Status register is set, the interrupt signal will be asserted provided that the corresponding interrupt enable bit is set accordingly.

The Status register will be updated due to an active event, regardless of the setting of the individual enable bits. Once a status bit has been set, it will remain set until the Status register bit is written to 1 (and the error condition has been removed).

If the interrupt signal is asserted, it will be cleared immediately if either the status or enable bit is cleared.

See Section 31.6, "Interrupts".

FIGURE 31-4: INTERRUPT FLOW



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31.9 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the RPM-PWM Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 31-1: REGISTER SUMMARY

Offset	Register Name
00h	Fan Setting
02h	Fan Configuration Register
04h	PWM Divide Register
05h	Gain Register
06h	Fan Spin Up Configuration Register
07h	Fan Step Register
08h	Fan Minimum Drive Register
09h	Valid TACH Count Register
0Ah	Fan Drive Fail Band Register
0Ch	TACH Target Register
0Eh	TACH Reading Register
10h	PWM Driver Base Frequency Register
11h	Fan Status Register

31.9.1 FAN SETTING REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:6	FAN_SETTING The Fan Driver Setting used to control the output of the Fan Driver.	R/W	00h	RESET_SYS
5:0	Reserved	R	-	-

31.9.2 FAN CONFIGURATION REGISTER

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15	EN_RRC Enables the ramp rate control circuitry during the Manual Mode of operation. 1=The ramp rate control circuitry for the Manual Mode of operation is enabled. The PWM setting will follow the ramp rate controls as determined by the Fan Step and Update Time settings. The maximum PWM step is capped at the Fan Step setting and is updated based on the Update Time as given by the field UPDATE. 0=The ramp rate control circuitry for the Manual Mode of operation is disabled. When the Fan Drive Setting values are changed and the RPM based Fan Control Algorithm is disabled, the fan driver will be set to the new setting immediately.	R/W	0b	RESET_SYS
14	DIS_GLITCH Disables the low pass glitch filter that removes high frequency noise injected on the TACH pin. 1=The glitch filter is disabled 0=The glitch filter is enabled	R/W	0b	RESET_SYS
13:12	DER_OPT Control some of the advanced options that affect the derivative portion of the RPM based fan control algorithm as shown in Table 31-3, "Derivative Options". These bits only apply if the Fan Speed Control Algorithm is used.	R/W	3h	RESET_SYS
11:10	ERR_RNG Control some of the advanced options that affect the error window. When the measured fan speed is within the programmed error window around the target speed, the fan drive setting is not updated. These bits only apply if the Fan Speed Control Algorithm is used. 3=200 RPM 2=100 RPM 1=50 RPM 0=0 RPM	R/W	1h	RESET_SYS
9	POLARITY Determines the polarity of the PWM driver. This does NOT affect the drive setting registers. A setting of 0% drive will still correspond to 0% drive independent of the polarity. 1=The Polarity of the PWM driver is inverted. A drive setting of 00h will cause the output to be set at 100% duty cycle and a drive setting of FFh will cause the output to be set at 0% duty cycle. 0=The Polarity of the PWM driver is normal. A drive setting of 00h will cause the output to be set at 0% duty cycle and a drive setting of FFh will cause the output to be set at 100% duty cycle.	R/W	0h	RESET_SYS

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Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
8	Reserved	R	-	-
7	EN_ALGO Enables the RPM based Fan Control Algorithm. 1=The control circuitry is enabled and the Fan Driver output will be automatically updated to maintain the programmed fan speed as indicated by the TACH Target Register. 0=The control circuitry is disabled and the fan driver output is determined by the Fan Driver Setting Register.	R/W	0b	RESET_SYS
6:5	RANGE Adjusts the range of reported and programmed tachometer reading values. The RANGE bits determine the weighting of all TACH values (including the Valid TACH Count, TACH Target, and TACH reading). 3=Reported Minimum RPM: 4000. Tach Count Multiplier: 8 2=Reported Minimum RPM: 2000. Tach Count Multiplier: 4 1=Reported Minimum RPM: 1000. Tach Count Multiplier: 2 0=Reported Minimum RPM: 500. Tach Count Multiplier: 1	R/W	1h	RESET_SYS

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
4:3	EDGES Determines the minimum number of edges that must be detected on the TACH signal to determine a single rotation. A typical fan measured 5 edges (for a 2-pole fan). Increasing the number of edges measured with respect to the number of poles of the fan will cause the TACH Reading registers to indicate a fan speed that is higher or lower than the actual speed. In order for the FSC Algorithm to operate correctly, the TACH Target must be updated by the user to accommodate this shift. The Effective Tach Multiplier shown in Table 31-2, "Minimum Edges for Fan Rotation" is used as a direct multiplier term that is applied to the Actual RPM to achieve the Reported RPM. It should only be applied if the number of edges measured does not match the number of edges expected based on the number of poles of the fan (which is fixed for any given fan). Contact Microchip for recommended settings when using fans with more or less than 2 poles.	R/W	1h	RESET_SYS
2:0	UPDATE Determines the base time between fan driver updates. The Update Time, along with the Fan Step Register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes. 7=1600ms 6=1200ms 5=800ms 4=500ms 3=400ms 2=300ms 1=200ms 0=100ms **Note:** This ramp rate control applies for all changes to the active PWM output including when the RPM based Fan Speed Control Algorithm is disabled.	R/W	3h	RESET_SYS

TABLE 31-2: MINIMUM EDGES FOR FAN ROTATION

Edges	Minimum TACH Edges	Number of Fan Poles	Effective TACH Multiplier (Based on 2 Pole Fans) If Edges Changed
0h	3	1	0.5
1h	5	2 (default)	1
2h	7	3	1.5
3h	9	4	2

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TABLE 31-3: DERIVATIVE OPTIONS

DER_OPT	Operation	Note (see Section 31.9.6, "Fan Step Register")
0	No derivative options used	PWM steps are limited to the maximum PWM drive step value in Fan Step Register
1	Basic derivative. The derivative of the error from the current drive setting and the target is added to the iterative PWM drive setting (in addition to proportional and integral terms)	PWM steps are limited to the maximum PWM drive step value in Fan Step Register
2	Step derivative. The derivative of the error from the current drive setting and the target is added to the iterative PWM drive setting and is not capped by the maximum PWM drive step. This allows for very fast response times	PWM steps are not limited to the maximum PWM drive step value in Fan Step Register (i.e., maximum fan step setting is ignored)
3	Both the basic derivative and the step derivative are used effectively causing the derivative term to have double the effect of the derivative term (default).	PWM steps are not limited to the maximum PWM drive step value in Fan Step Register (i.e., maximum fan step setting is ignored)

31.9.3 PWM DIVIDE REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	PWM_DIVIDE The PWM Divide value determines the final frequency of the PWM driver. The driver base frequency is divided by the PWM Divide value to determine the final frequency.	R/W	01h	RESET_SYS

31.9.4 GAIN REGISTER

The Gain Register stores the gain terms used by the proportional and integral portions of the RPM based Fan Control Algorithm. These terms will affect the FSC closed loop acquisition, overshoot, and settling as would be expected in a classic PID system.

This register only applies if the Fan Speed Control Algorithm is used.

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	Reserved	R	-	-
5:4	GAIND The derivative gain term. Gain Factor: 3=8x 2=4x 1=2x 0=1x	R/W	2h	RESET_SYS

Offset	05h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3:2	GAINI The integral gain term. Gain Factor: 3=8x 2=4x 1=2x 0=1x	R/W	2h	RESET_SYS
1:0	GAINP The proportional gain term. Gain Factor: 3=8x 2=4x 1=2x 0=1x	R/W	2h	RESET_SYS

31.9.5 FAN SPIN UP CONFIGURATION REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	DRIVE_FAIL_CNT Determines how many update cycles are used for the Drive Fail detection function. This circuitry determines whether the fan can be driven to the desired Tach target. These settings only apply if the Fan Speed Control Algorithm is enabled. 3=Drive Fail detection circuitry will count for 64 update periods 2=Drive Fail detection circuitry will count for 32 update periods 1=Drive Fail detection circuitry will count for 16 update periods 0=Drive Fail detection circuitry is disabled	R/W	00b	RESET_SYS
5	NOKICK Determines if the Spin Up Routine will drive the fan to 100% duty cycle for 1/4 of the programmed spin up time before driving it at the programmed level. 1=The Spin Up Routine will not drive the PWM to 100%. It will set the drive at the programmed spin level for the entire duration of the programmed spin up time 0=The Spin Up Routine will drive the PWM to 100% for 1/4 of the programmed spin up time before reverting to the programmed spin level	R/W	0b	RESET_SYS

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Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
4:2	SPIN_LVL Determines the final drive level that is used by the Spin Up Routine. 7=65% 6=60% 5=55% 4=50% 3=45% 2=40% 1=35% 0=30%	R/W	6h	RESET_SYS
1:0	SPINUP_TIME Determines the maximum Spin Time that the Spin Up Routine will run for. If a valid tachometer measurement is not detected before the Spin Time has elapsed, an interrupt will be generated. When the RPM based Fan Control Algorithm is active, the fan driver will attempt to re-start the fan immediately after the end of the last spin up attempt. 3=2 seconds 2=1 second 1=500 ms 0=250 ms	R/W	1h	RESET_SYS

31.9.6 FAN STEP REGISTER

The Fan Step Register, along with the Update Time, controls the ramp rate of the fan driver response calculated by the RPM based Fan Control Algorithm for the Derivative Options field values of “00” and “01” in the Fan Configuration Register.

The value of the register represents the maximum step size the fan driver will take for each update.

When the maximum step size limitation is applied, if the necessary fan driver delta is larger than the Fan Step, it will be capped at the Fan Step setting and updated every Update Time ms.

The maximum step size is ignored for the Derivative Options field values of “10” and “11”.

Offset	07h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	FAN_STEP The Fan Step value represents the maximum step size the fan driver will take between update times. When the PWM_BASE frequency range field in the PWM Driver Base Frequency Register is set to the value 1, 2 or 3, this 8-bit field is added to the 10-bit PWM duty cycle, for a maximum step size of 25%. When the PWM_BASE field is set to 0, the PWM operates in an 8-bit mode. In 8-bit mode, this 8-bit field is added to the 8-bit duty cycle, for a maximum step size of 100%.	R/W	10h	RESET_SYS

31.9.7 FAN MINIMUM DRIVE REGISTER

the Fan Minimum Drive Register stores the minimum drive setting for the RPM based Fan Control Algorithm. The RPM based Fan Control Algorithm will not drive the fan at a level lower than the minimum drive unless the target Fan Speed is set at FFh (see "TACH Target Registers").

During normal operation, if the fan stops for any reason (including low drive), the RPM based Fan Control Algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Registers to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

These registers only apply if the Fan Speed Control Algorithm is used.

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	MIN_DRIVE The minimum drive setting.	R/W	66h	RESET_SYS

Note:	To ensure proper operation, the Fan Minimum Drive register must be set prior to setting the Tach Target High and Low Byte registers, and then the Tach Target registers can be subsequently updated. At a later time, if the Fan Minimum Drive register is changed to a value higher than current Fan value, the Tach Target registers must also be updated.

31.9.8 VALID TACH COUNT REGISTER

The Valid TACH Count Register stores the maximum TACH Reading Register value to indicate that the fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry. See the equation in the TACH Reading Registers section for translating the RPM to a count.

If the TACH Reading Register value exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count), a stalled fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

Note:	The automatic invoking of the Spin Up Routine only applies if the Fan Speed Control Algorithm is used. If the FSC is disabled, then the device will only invoke the Spin Up Routine when the PWM setting changes from 00h.

If a TACH Target setting is set above the Valid TACH Count setting, that setting will be ignored and the algorithm will use the current fan drive setting.

These registers only apply if the Fan Speed Control Algorithm is used.

Offset	09h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	VALID_TACH_CNT The maximum TACH Reading Register value to indicate that the fan is spinning properly.	R/W	F5h	RESET_SYS

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31.9.9 FAN DRIVE FAIL BAND REGISTER

The Fan Drive Fail Band Registers store the number of Tach counts used by the Fan Drive Fail detection circuitry. This circuitry is activated when the fan drive setting high byte is at FFh. When it is enabled, the actual measured fan speed is compared against the target fan speed.

This circuitry is used to indicate that the target fan speed at full drive is higher than the fan is actually capable of reaching. If the measured fan speed does not exceed the target fan speed minus the Fan Drive Fail Band Register settings for a period of time longer than set by the DRIVE_FAIL_CNTx[1:0] bits in the Fan Spin Up Configuration Register, the DRIVE_FAIL status bit will be set and an interrupt generated.

These registers only apply if the Fan Speed Control Algorithm is used.

Offset	0Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:3	FAN_DRIVE_FAIL_BAND The number of Tach counts used by the Fan Drive Fail detection circuitry	R	0h	RESET_SYS
2:0	Reserved	R	-	-

31.9.10 TACH TARGET REGISTER

The TACH Target Registers hold the target tachometer value that is maintained for the RPM based Fan Control Algorithm.

If the algorithm is enabled, setting the TACH Target Register High Byte to FFh will disable the fan driver (or set the PWM duty cycle to 0%). Setting the TACH Target to any other value (from a setting of FFh) will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

These registers only apply if the Fan Speed Control Algorithm is used.

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:3	TACH_TARGET The target tachometer value.	R	-	RESET_SYS
2:0	Reserved	R	-	-

31.9.11 TACH READING REGISTER

The TACH Reading Registers' contents describe the current tachometer reading for the fan. By default, the data represents the fan speed as the number of 32.768kHz clock periods that occur for a single revolution of the fan.

The Equation below shows the detailed conversion from tachometer measurement (COUNT) to RPM.

$$RPM = \frac{1}{Poles} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times f_{TACH} \times 60$$

where:

- *Poles* = number of poles of the fan (typically 2)
- f_{TACH} = the frequency of the tachometer measurement clock
- *n* = number of edges measured (typically 5 for a 2 pole fan)
- *m* = the multiplier defined by the RANGE bits
- *COUNT* = TACH Reading Register value (in decimal)

The following equation shows the simplified translation of the TACH Reading Register count to RPM assuming a 2-pole fan, measuring 5 edges, with a frequency of 32.768kHz.

$$RPM = \frac{3932160 \times m}{COUNT}$$

Offset	0Eh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:3	TACH_READING The current tachometer reading value.	R	-	RESET_SYS
2:0	Reserved	R	-	-

31.9.12 PWM DRIVER BASE FREQUENCY REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	-	-
1:0	PWM_BASE Determines the frequency range of the PWM fan driver (when enabled). PWM resolution is 10-bit, except when this field is set to '0b', when it is 8-bit. 3=2.34KHz 2=4.67KHz 1=23.4KHz 0=26.8KHz	R/W	00b	RESET_SYS

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31.9.13 FAN STATUS REGISTER

Offset	11h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	Reserved	R	-	-
5	DRIVE_FAIL The bit Indicates that the RPM-based Fan Speed Control Algorithm cannot drive the Fan to the desired target setting at maximum drive. 1=The RPM-based Fan Speed Control Algorithm cannot drive Fan to the desired target setting at maximum drive. 0=The RPM-based Fan Speed Control Algorithm can drive Fan to the desired target setting.	R/WC	0b	RESET_SYS
4:2	Reserved	R	-	-
1	FAN_SPIN The bit Indicates that the Spin up Routine for the Fan could not detect a valid tachometer reading within its maximum time window. 1=The Spin up Routine for the Fan could not detect a valid tachometer reading within its maximum time window. 0=The Spin up Routine for the Fan detected a valid tachometer reading within its maximum time window.	R/WC	0b	RESET_SYS
0	FAN_STALL The bit Indicates that the tachometer measurement on the Fan detects a stalled fan. 1=Stalled fan not detected 0=Stalled fan not detected	R/WC	0b	RESET_SYS

32.0 EEPROM

32.1 Overview

The MEC170x includes a 2K x 8bit EEPROM (Electrically Erasable Programmable Read Only Memory).

32.2 References

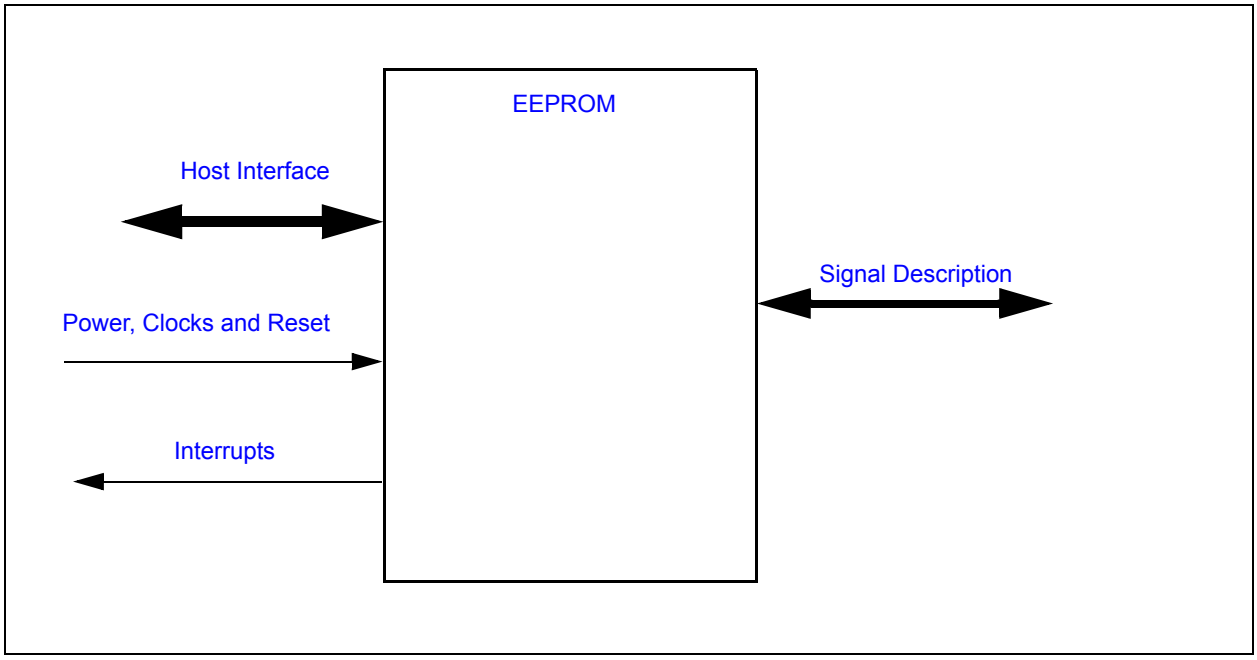
No references have been cited for this feature.

32.3 Terminology

There is no terminology defined for this section.

32.4 Interface

FIGURE 32-1: I/O DIAGRAM OF BLOCK



32.5 Signal Description

There are no external signals for this block.

32.6 Host Interface

The EEPROM interface is accessed by host software via a registered interface, as defined in Section 32.12, "EC Registers".

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32.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

32.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

32.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for EEPROM logic.

32.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.
RESET_EEPROM	This signal resets most of the registers and logic in this block to their default state. It is asserted either on a RESET_SYS is asserted, or when the SOFT_RESET bit in the EEPROM Mode Register is written with a ‘1b’.

32.8 Interrupts

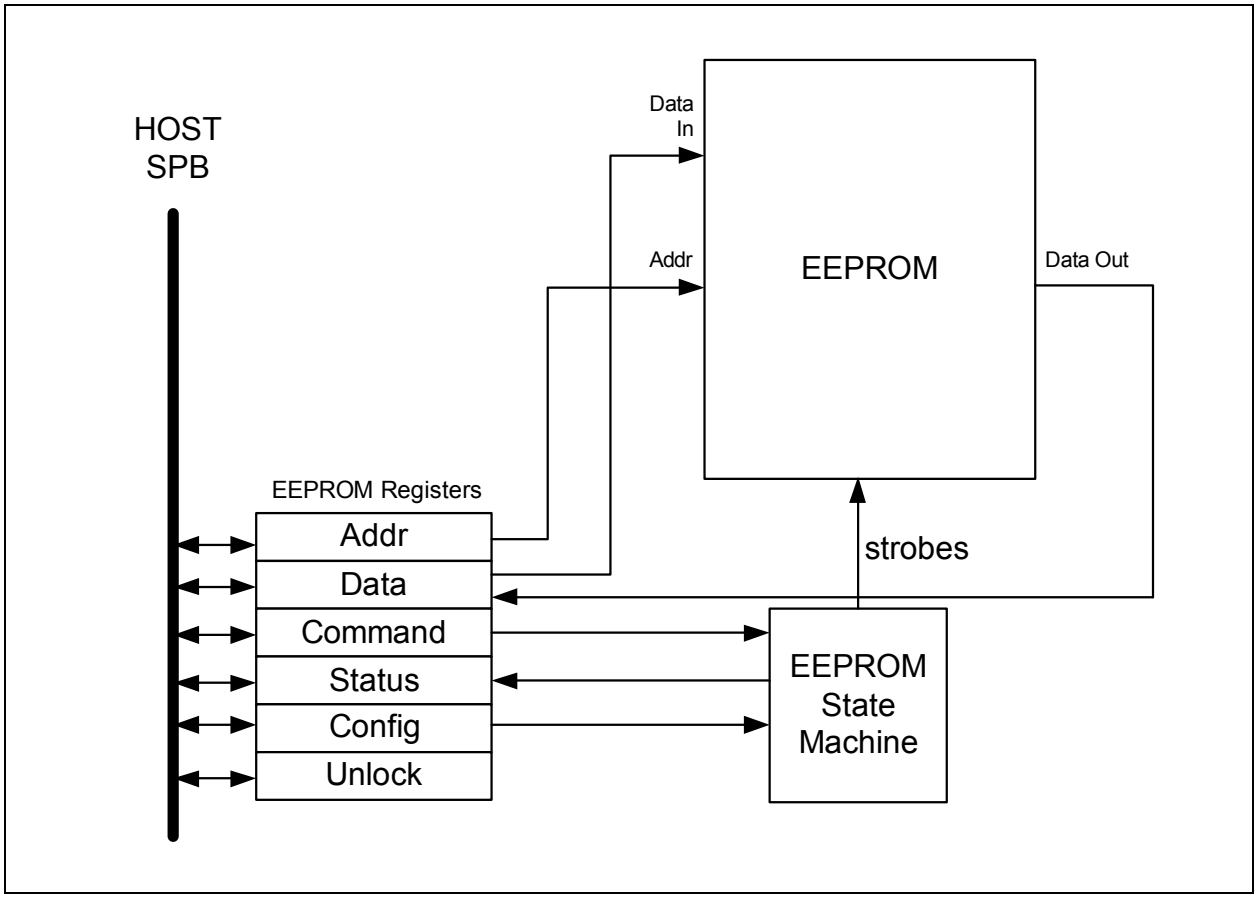
Source	Description
EEPROM	EEPROM transfer completed.

32.9 Low Power Modes

The EEPROM Controller enters its lowest power state whenever it is not busy (the TRANSFER_ACTIVE bit in the EEPROM Status Register is 0).

32.10 Description

TABLE 32-1: EEPROM BLOCK DIAGRAM



32.11 EEPROM Operation

The EEPROM consists of a 2K array of bytes, organized into 32-byte pages. Data are transfered to and from the EEPROM array to a register buffer in transfers of 1 to 32 bytes at a time. Reads can start at any byte address in the array and will transfer the quantity from the EEPROM array to the buffer. Writes can start at any byte address but cannot cross 32 byte page boundaries.

A read transfer of 1 byte from the EEPROM fabric to the buffer takes approximately 7µS. A transfer of 32 bytes takes an additional 50µS.

A write transfer of 1 byte to 32 bytes to the EEPROM fabric from the buffer takes approximately 5ms.

32.11.1 ENDURANCE

Each 32-byte page can be written up to 1,000,000 times before the page's ability to retain data is compromised.

32.11.2 EEPROM INITIALIZATION

Data in offsets 7FCh to 7FFh from the EEPROM Memory Block are examined a boot. If bit 31 is a '1,' the 31 least significant bits of the data are written to the EEPROM Unlock Register and the LOCK bit in the EEPROM Lock Register is set to '1b' and the EEPROM Memory Block becomes inaccessible.

32.11.3 PASSWORD USE

Offset 7FCh is the last 32-bit word in the EEPROM memory block. If bit 31 is a '0' in that word, then the location can be treated as EEPROM data that stores only positive integers in the range 0 to 2 billion (or so). If bit 31 is a '1' then the word contains a password that can be used to unlock the EEPROM memory block.

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To keep the EEPROM memory block secure, and to insure that the EC firmware is authorized to read its contents, EC firmware can use this password. The following code can be executed as part of the EC's initialization code:

```
int password;
#define SECRET_PASSWORD 0xXXXXXXXX
#define Unlock_register 0x40002C14 // address of key register

password = eeprom_read(0x7FC);
if( password == 0xFFFFFFFF )
{
        // EEPROM is unlocked and the key not yet installed
        // establish key and force a reboot
        eeprom_write(0x7FF, SECRET_PASSWORD);
        force_reset();
} else {
        // unlock the EEPROM
        *Unlock_register = SECRET_PASSWORD;
}
```

The subroutines force_reset() forces a system reset, using, for example, the watchdog timer. If the EC firmware knows the right password, it can unblock the EEPROM memory block; if it does not, then the block will remain inaccessible. The code can run in the Boot Block so that the SECRET_PASSWORD (a constant in the code) cannot be read via JTAG or over the LPC bus, and thus can only be known to a valid EC firmware block.

32.11.4 STATUS BYTE

The READ STATUS and WRITE STATUS commands affect the Status Byte. The Status Byte can be used to control write-protection in the EEPROM fabric, as well as providing a mechanism for reporting on status of the EEPROM fabric.The Status Byte is non-volatile and retains its value even after a RESET_SYS system reset.

The byte is defined as follows:

Bits	Description	Type
7:4	Reserved	R
3:2	WRITE_PROTECT Write protection of the EEPROM fabric. 3=The entire EEPROM fabric is write protected (read only) 2=The upper half (byte offsets 0400h to 07FFh) of the EEPROM fabric is write protected 1=The upper quarter (byte offsets 0600h to 07FFh) of the EEPROM fabric is write protected 0=The entire EEPROM fabric is writable	R/W
1	WRITE_ENABLE In normal use, this bit is always 0. Write enable of the EEPROM fabric is handled automatically.	R
0	WRITE_IN_PROGRESS 1=The EEPROM fabric is processing a write 0=The EEPROM fabric is idle	R

32.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the EEPROM Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 32-2: EC-ONLY REGISTER SUMMARY

EC Offset	Register Name
00h	EEPROM Mode Register
04h	EEPROM Execute Register
08h	EEPROM Status Register
0Ch	EEPROM Interrupt Enable Register
10h	EEPROM Password Register
14h	EEPROM Unlock Register
18h	EEPROM Lock Register
20h	EEPROM Buffer Register

32.12.1 EEPROM MODE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	SOFT_RESET This 8-bit register holds the data to be written into the EEPROM memory array during a program cycle, as well as the data returned from an EEPROM read during a read cycle. It should be set up before the EEPROM Execute Register is configured.	W	-	RESET_EEPROM
0	ACTIVATE This 8-bit register holds the data to be written into the EEPROM memory array during a program cycle, as well as the data returned from an EEPROM read during a read cycle. It should be set up before the EEPROM Execute Register is configured. 1=The EEPROM controller is enabled 0=The EEPROM controller is disabled and placed in its lowest power state	R/W	0h	RESET_EEPROM

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32.12.2 EEPROM EXECUTE REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:29	Reserved	R	-	-
28:24	TRANSFER_SIZE The number of bytes to be transfered between the EEPROM fabric and the buffer. A count of 0 is means a transfer of 32 bytes. This field is only applicable for WRITE and READ commands.	R/W	0h	RESET_EEPROM
23:19	Reserved	R	-	-
18:16	COMMAND A write to this register automatically starts an EEPROM transfer between the fabric and the buffer 3=WRITE STATUS 2=READ STATUS 1=WRITE 0=READ	R/W	0h	RESET_EEPROM
15:0	EEPROM_ADRESS This register represents a byte address in the EEPROM. Bits[15:11] should be 0, but there is error flagged if they are not. This field only applies to READ and WRITE commands. It does not apply to READ STATUS and WRITE STATUS commands.	R/W	0h	RESET_EEPROM

32.12.3 EEPROM STATUS REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:9	Reserved	R	-	-
8	TRANSFER_ACTIVE A transfer between the EEPROM fabric and the EEPROM Buffer Register is in progress	R	0h	RESET_EEPROM
6:3	Reserved	R	-	-

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	EXECUTION_ERROR This bit is set to '1b' if an illegal command has been programmed into the block. A command is illegal if: • The EEPROM Execute Register is written while a previous command has not yet completed (that is, while TRANSFER_ACTIVE is '1b') • An illegal value was written into the COMMAND field	R/WC	0h	RESET_EEPROM
0	TRANSFER_COMPLETE 1=The transfer between the EEPROM fabric and the EEPROM Buffer Register has completed 0=The transfer between the EEPROM fabric and the EEPROM Buffer Register has not yet completed	R/WC	0h	RESET_EEPROM

32.12.4 EEPROM INTERRUPT ENABLE REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	EXECUTION_ERROR_IE Assert an EEPROM interrupt when the EXECUTION_ERROR status is asserted. 1=Enable Interrupt 0=Disable Interrupt	R/W	0h	RESET_SYS
0	TRANSFER_COMPLETE_IE Assert an EEPROM interrupt when the TRANSFER_COMPLETE status is asserted. 1=Enable Interrupt 0=Disable Interrupt	R/W	0h	RESET_SYS

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32.12.5 EEPROM PASSWORD REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:0	EEPROM_PASSWORD This register stores a key that can be used to unlock the EEPROM controller if it is locked. This register is write-once only. Once written, it can be neither read nor written until the next system reset.	W	0h	RESET_SYS

32.12.6 EEPROM UNLOCK REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:0	EEPROM_UNLOCK When this 31-bit register is written, the least significant 31 bits of the write are compared to the EEPROM Password Register that stores the key. If all bits match, the LOCK bit in the EEPROM Lock Register cleared, and the EEPROM array can be read or written. This register is write only.	W	0h	RESET_SYS

32.12.7 EEPROM LOCK REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	LOCK EEPROM Access Lock. When this bit is set to ‘1b’, the EEPROM is locked from all accesses, including reads, writes and status queries. Once set to ‘1b’ it can only be cleared to ‘0b’ by a RESET_SYS or by writing the EEPROM Unlock Register with a value that matches the contents of the EEPROM Password Register. 1=EEPROM is locked and cannot be accessed 0=EEPROM is unlocked and may be accessed	R/W	0h	RESET_SYS
0	JTAG_LOCK If this bit is set to ‘1b’ the LOCK bit is set to ‘1b’ whenever the JTAG/SWD test interface is activated. This has priority over the EEPROM Unlock Register register, so that writing the EEPROM Unlock Register register with a value that matches the EEPROM Password Register if JTAG/SWD is active at the time. 1=The LOCK bit is set to ‘1b’ whenever the JTAG/SWD test interface is activated 0=The JTAG/SWD test interface has no effect on the LOCK bit	R/W	0h	RESET_SYS

32.12.8 EEPROM BUFFER REGISTER

Offset	20h to 3Fh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
	BUFFER Data buffer of 32 bytes used to transfer data to and from the EEPROM fabric. For WRITES, it must be written before the WRITE command is started. For READ STATUS and WRITE STATUS commands, only the first byte (offset 0 in this register) is used.	R/W	0h	RESET_SYS

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33.0 BLINKING/BREATHING PWM

33.1 Introduction

LEDs are used in computer applications to communicate internal state information to a user through a minimal interface. Typical applications will cause an LED to blink at different rates to convey different state information. For example, an LED could be full on, full off, blinking at a rate of once a second, or blinking at a rate of once every four seconds, in order to communicate four different states.

As an alternative to blinking, an LED can “breathe”, that is, oscillate between a bright state and a dim state in a continuous, or apparently continuous manner. The rate of breathing, or the level of brightness at the extremes of the oscillation period, can be used to convey state information to the user that may be more informative, or at least more novel, than traditional blinking.

The blinking/breathing hardware is implemented using a PWM. The PWM can be driven either by the Main system clock or by a 32.768 KHz clock input. When driven by the Main system clock, the PWM can be used as a standard 8-bit PWM in order to control a fan. When used to drive blinking or breathing LEDs, the 32.768 KHz clock source is used.

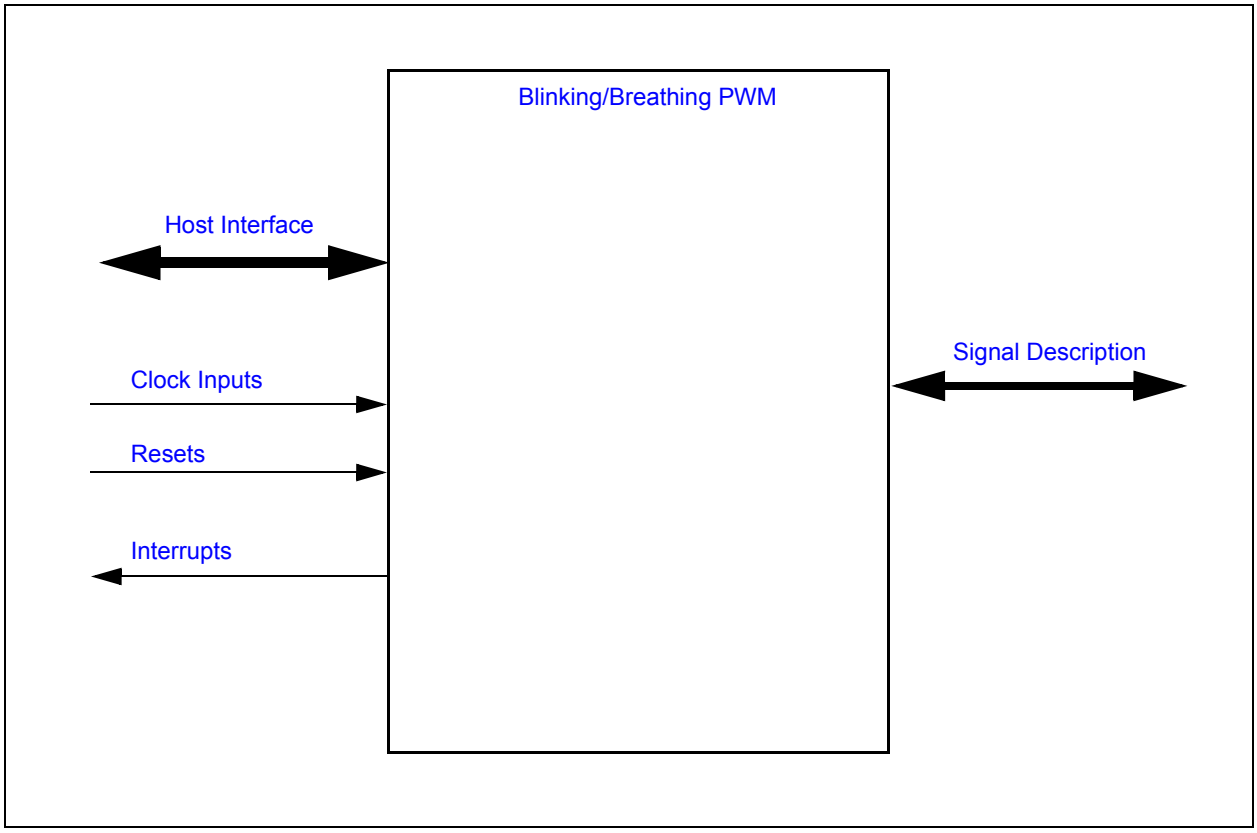
Features:

- Each PWM independently configurable
- Each PWM configurable for LED blinking and breathing output
- Highly configurable breathing rate from 60ms to 1min
- Non-linear brightness curves approximated with 8 piece wise-linear segments
- All LED PWMs can be synchronized
- Each PWM configurable for 8-bit PWM support
- Multiple clock rates
- Configurable Watchdog Timer

33.2 Interface

This block is designed to drive a pin on the pin interface and to be accessed internally via a registered host interface.

FIGURE 33-1: I/O DIAGRAM OF BLOCK



33.3 Signal Description

Name	Direction	Description
PWM Output	Output	Output of PWM By default, the PWM pin is configured to be active high: when the PWM is configured to be fully on, the pin is driving high. When the PWM is configured to be fully off, the pin is low. If firmware requires the Blinking/Breathing PWM to be active low, the Polarity bit in the GPIO Pin Control Register associated with the PWM can be set to 1, which inverts the output polarity.

33.4 Host Interface

The blinking/breathing PWM block is accessed by a controller over the standard register interface.

33.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

33.5.1 POWER DOMAINS

Name	Description
VTR	Main power. The source of main power for the device is system dependent.

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33.5.2 CLOCK INPUTS

Name	Description
32KHz	32.768 KHz clock
48MHz	Main system clock

33.5.3 RESETS

Name	Description
RESET_SYS	Block reset

33.6 Interrupts

Each PWM can generate an interrupt. The interrupt is asserted for one Main system clock period whenever the PWM WDT times out. The PWM WDT is described in Section 33.8.3.1, "PWM WDT".

Source	Description
PWM_WDT	PWM watchdog time out

33.7 Low Power Mode

The Blinking/Breathing PWM may be put into a low power mode by the chip-level power, clocks, and reset (PCR) circuitry. The low power mode is only applicable when the Blinking/Breathing PWM is operating in the General Purpose PWM mode. When the low speed clock mode is selected, the blinking/breathing function continues to operate, even when the 48MHz is stopped. Low power mode behavior is summarized in the following table:

TABLE 33-1: LOW POWER MODE BEHAVIOR

CLOCK_SOURCE	CONTROL	Mode	Low Power Mode	Description
X	‘00’b	PWM ‘OFF’	Yes	32.768 KHz clock is required.
X	‘01’b	Breathing	Yes	
1	‘10’b	General Purpose PWM	No	Main system clock is required, even when a sleep command to the block is asserted.
0	‘10’b	Blinking	Yes	32.768 KHz clock is required.
X	‘11’b	PWM ‘ON’	Yes	

Note: In order for the MEC170x to enter its.Heavy Sleep state, the SLEEP_ENABLE input for all Blinking/Breathing PWM instances must be asserted, even if the PWMs are configured to use the low speed clock.

33.8 Description

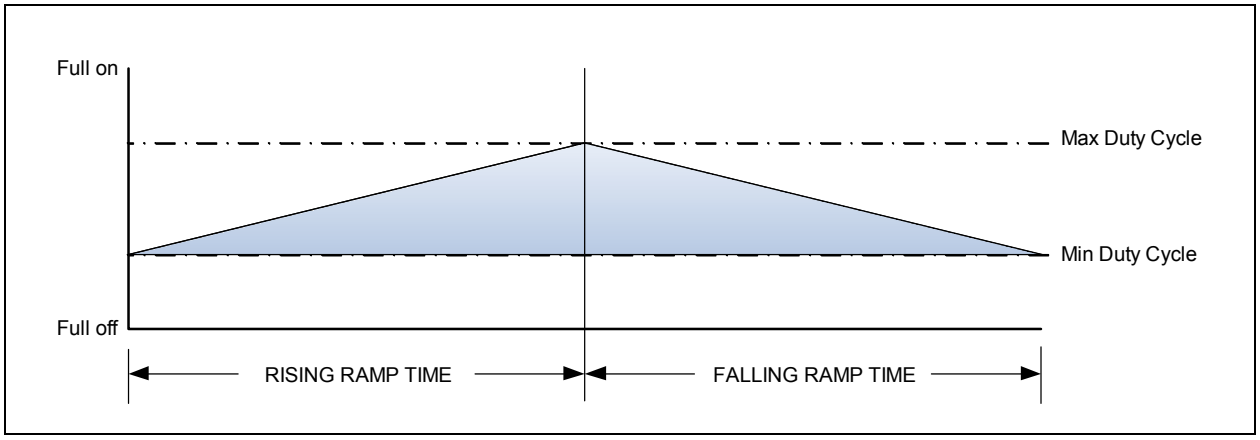
33.8.1 BREATHING

If an LED blinks rapidly enough, the eye will interpret the light as reduced brightness, rather than a blinking pattern. Therefore, if the blinking period is short enough, modifying the duty cycle will set the apparent brightness, rather than a blinking rate. At a blinking rate of 128Hz or greater, almost all people will perceive a continuous light source rather than an intermittent pattern.

Because making an LED appear to breathe is an aesthetic effect, the breathing mechanism must be adjustable or customers may find the breathing effect unattractive. There are several variables that can affect breathing appearance, as described below.

The following figure illustrates some of the variables in breathing:

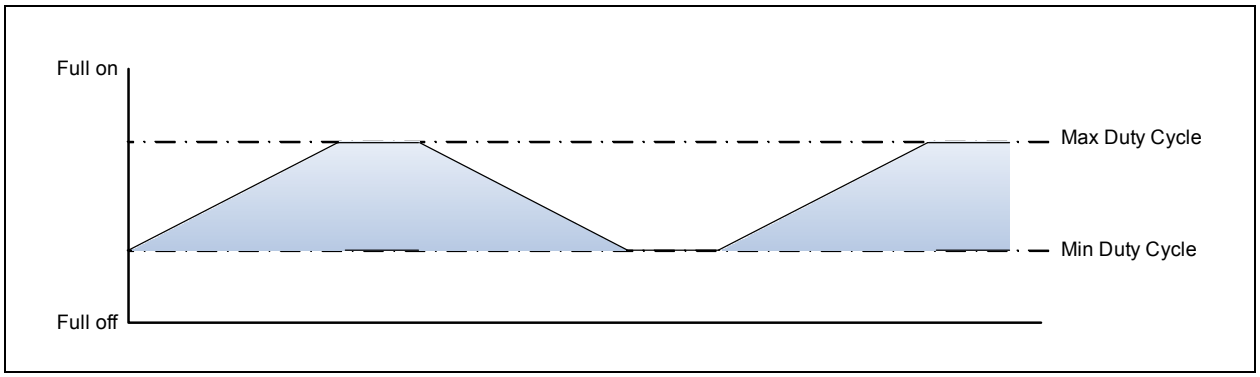
FIGURE 33-2: BREATHING LED EXAMPLE



The breathing range of and LED can range between full on and full off, or in a range that falls within the full-on/full-off range, as shown in this figure. The ramp time can be different in different applications. For example, if the ramp time was 1 second, the LED would appear to breathe quickly. A time of 2 seconds would make the LED appear to breathe more leisurely.

The breathing pattern can be clipped, as shown in the following figure, so that the breathing effect appears to pause at its maximum and minimum brightnesses:

FIGURE 33-3: CLIPPING EXAMPLE



The clipping periods at the two extremes can be adjusted independently, so that for example an LED can appear to breathe (with a short delay at maximum brightness) followed by a longer “resting” period (with a long delay at minimum brightness).

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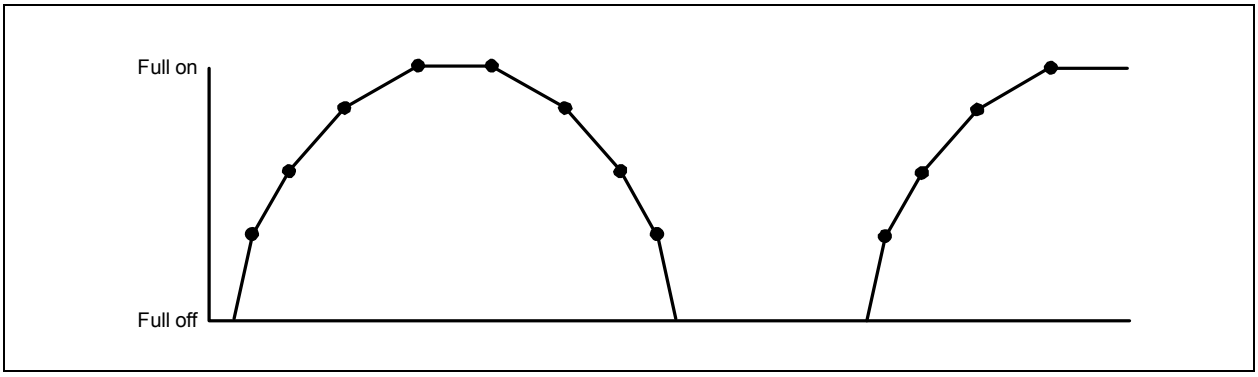
The brightness can also be changed in a non-linear fashion, as shown in the following figure:

FIGURE 33-4: EXAMPLE OF A SEGMENTED CURVE



In this figure, the rise and fall curves are implemented in 4 linear segments and are the rise and fall periods are symmetric.

The breathing mode uses the 32.768 KHz clock for its time base.

33.8.2 BLINKING

When configured for blinking, a subset of the hardware used in breathing is used to implement the blinking function. The PWM (an 8-bit accumulator plus an 8-bit duty cycle register) drives the LED directly. The Duty Cycle register is programmed directly by the user, and not modified further. The PWM accumulator is configured as a simple 8-bit up counter. The counter uses the 32.768 KHz clock, and is pre-scaled by the Delay counter, to slow the PWM down from the 128Hz provided by directly running the PWM on the 32.768 KHz clock.

With the pre-scaler, the blink rate of the LED could be as fast as 128Hz (which, because it is blinking faster than the eye can distinguish, would appear as a continuous level) to 0.03125Hz (that is, with a period of 7.8ms to 32 seconds). Any duty cycle from 0% (0h) to 100% (FFh) can be configured, with an 8-bit precision. An LED with a duty cycle value of 0h will be fully off, while an LED with a duty cycle value of FFh will be fully on.

In Blinking mode the PWM counter is always in 8-bit mode.

Table 33-2, "LED Blink Configuration Examples" shows some example blinking configurations:

TABLE 33-2: LED BLINK CONFIGURATION EXAMPLES

Prescale	Duty Cycle	Blink Frequency	Blink
000h	00h	128Hz	full off
000h	FFh	128Hz	full on
001h	40h	64Hz	3.9ms on, 11.5ms off
003h	80h	32Hz	15.5ms on, 15.5ms off
07Fh	20h	1Hz	125ms on, 0.875s off
0BFh	16h	0.66Hz	125ms on, 1.375s off
0FFh	10h	0.5Hz	125ms on, 1.875s off
180h	0Bh	0.33Hz	129ms on, 2.875s off
1FFh	40h	0.25Hz	1s on, 3s off

The Blinking and General Purpose PWM modes share the hardware used in the breathing mode. The Prescale value is derived from the LD field of the LED_DELAY register and the Duty Cycle is derived from the MIN field of the LED_LIMITS register.

TABLE 33-3: BLINKING MODE CALCULATIONS

Parameter	Unit	Equation
Frequency	Hz	(32KHz frequency) /(PRESCALE + 1)/256
'H' Width	Seconds	(1/Frequency) x (DutyCycle/256)
'L' Width	Seconds	(1/Frequency) x ((1-DutyCycle)/256)

33.8.3 GENERAL PURPOSE PWM

When used in the Blinking configuration with the 48MHz, the LED module can be used as a general-purpose programmable Pulse-Width Modulator with an 8-bit programmable pulse width. It can be used for fan speed control, sound volume, etc. With the 48MHz source, the PWM frequency can be configured in the range shown in Table 33-4.

TABLE 33-4: PWM CONFIGURATION EXAMPLES

Prescale	PWM Frequency
000h	187.5 KHz
001h	94 KHz
003h	47 KHz
006h	26.8 KHz
00Bh	15.625 KHz
07Fh	1.46 KHz
1FFh	366 Hz
FFFh	46 Hz

TABLE 33-5: GENERAL PURPOSE PWM MODE CALCULATIONS

Parameter	Unit	Equation
Frequency	Hz	(48MHz frequency) / (PRESCALE + 1) / 256
'H' Width	Seconds	(1/Frequency) x (DutyCycle/256)
'L' Width	Seconds	(1/Frequency) x (256 - DutyCycle)

33.8.3.1 PWM WDT

When the PWM is configured as a general-purpose PWM (in the Blinking configuration with the Main system clock), the PWM includes a Watch Dog Timer (WDT). The WDT consists of an internal 8-bit counter and an 8-bit reload value (the field WDTLD in LED Configuration Register register). The internal counter is loaded with the reset value of WDTLD (14h, or 4 seconds) on system RESET_SYS and loaded with the contents of WDTLD whenever either the LED Configuration Register register is written or the MIN byte in the LED Limits Register register is written (the MIN byte controls the duty cycle of the PWM).

Whenever the internal counter is non-zero, it is decremented by 1 for every tick of the 5 Hz clock. If the counter decrements from 1 to 0, a WDT Terminal Count causes an interrupt to be generated and reset sets the CONTROL bit in the LED Configuration Register to 3h, which forces the PWM to be full on. No other PWM registers or fields are affected.

If the 5 Hz clock halts, the watchdog timer stops decrementing but retains its value, provided the device continues to be powered. When the 5 Hz clock restarts, the watchdog counter will continue decrementing where it left off.

Setting the WDTLD bits to 0 disables the PWM WDT. Other sample values for WDTLD are:

01h = 200 ms

02h = 400 ms

03h = 600 ms

04h = 800 ms

...

14h = 4seconds

FFh = 51 seconds

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33.9 Implementation

In addition to the registers described in Section 33.10, "EC Registers", the PWM is implemented using a number of components that are interconnected differently when configured for breathing operation and when configured for blinking/PWM operation.

33.9.1 BREATHING CONFIGURATION

The **PSIZE** parameter can configure the PWM to one of three modes: 8-bit, 7-bit and 6-bit. The **PERIOD CTR** counts ticks of its input clock. In 8-bit mode, it counts from 0 to 255 (that is, 256 steps), then repeats continuously. In this mode, a full cycle takes 7.8ms (128Hz). In 7-bit mode it counts from 0 to 127 (128 steps), and a full cycle takes 3.9ms (256Hz). In 6-bit mode it counts from 0 to 63 (64 steps) and a full cycle takes 1.95ms (512Hz).

The output of the LED circuit is asserted whenever the **PERIOD CTR** is less than the contents of the **DUTY CYCLE** register. The appearance of breathing is created by modifying the contents of the **DUTY CYCLE** register in a continuous manner. When the LED control is off the internal counters and registers are all reset to 0 (i.e. after a write setting the RESET bit in the LED Configuration Register Register.) Once enabled, the **DUTY CYCLE** register is increased by an amount determined by the LED_STEP register and at a rate determined by the **DELAY** counter. Once the duty cycle reaches its maximum value (determined by the field MAX), the duty cycle is held constant for a period determined by the field HD. Once the hold time is complete, the **DUTY CYCLE** register is decreased, again by an amount determined by the LED_STEP register and at a rate determined by the **DELAY** counter. When the duty cycle then falls at or below the minimum value (determined by the field MIN), the duty cycle is held constant for a period determined by the field HD. Once the hold time is complete, the cycle repeats, with the duty cycle oscillating between MIN and MAX.

The rising and falling ramp times as shown in Figure 33-2, "Breathing LED Example" can be either symmetric or asymmetric depending on the setting of the SYMMETRY bit in the LED Configuration Register Register. In Symmetric mode the rising and falling ramp rates have mirror symmetry; both rising and falling ramp rates use the same (all) 8 segments fields in each of the following registers (see Table 33-6): the LED Update Stepsize Register register and the LED Update Interval Register register. In Asymmetric mode the rising ramp rate uses 4 of the 8 segments fields and the falling ramp rate uses the remaining 4 of the 8 segments fields (see Table 33-6).

The parameters MIN, MAX, HD, LD and the 8 fields in LED_STEP and LED_INT determine the brightness range of the LED and the rate at which its brightness changes. See the descriptions of the fields in Section 33.10, "EC Registers", as well as the examples in Section 33.9.3, "Breathing Examples" for information on how to set these fields.

TABLE 33-6: SYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 33-3, "Clipping Example"	Duty Cycle	Segment Index	Symmetric Mode Register Fields Utilized	
X	000xxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
X	001xxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
X	010xxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]
X	011xxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
X	100xxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
X	101xxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]
X	110xxxxxb	110b	STEP[6]/INT[6]	Bits[27:24]
X	111xxxxxb	111b	STEP[7]/INT[7]	Bits[31:28]
Note: In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]				

TABLE 33-7: ASYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 33-3, "Clipping Example"	Duty Cycle	Segment Index	Asymmetric Mode Register Fields Utilized	
Rising	00xxxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
Rising	01xxxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
Rising	10xxxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]

TABLE 33-7: ASYMMETRIC BREATHING MODE REGISTER USAGE (CONTINUED)

Rising/ Falling Ramp Times in Figure 33-3, "Clipping Example"	Duty Cycle	Segment Index	Asymmetric Mode Register Fields Utilized	
Rising	11xxxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
falling	00xxxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
falling	01xxxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]
falling	10xxxxxxb	110b	STEP[6]/INT[6]	Bits[27:24]
falling	11xxxxxxb	111b	STEP[7]/INT[7]	Bits[31:28]
Note: In Asymmetric Mode the Segment_Index[2:0] is the bit concatenation of following: Segment_Index[2] = (FALLING RAMP TIME in Figure 33-3, "Clipping Example") and Segment_Index[1:0] = Duty Cycle Bits[7:6].				

33.9.2 BLINKING CONFIGURATION

The Delay counter and the PWM counter are the same as in the breathing configuration, except in this configuration they are connected differently. The Delay counter is clocked on either the 32.768 KHz clock or the Main system clock, rather than the output of the PWM. The PWM counter is clocked by the zero output of the Delay counter, which functions as a prescalar for the input clocks to the PWM. The Delay counter is reloaded from the LD field of the LED_DELAY register. When the LD field is 0 the input clock is passed directly to the PWM counter without prescaling. In Blinking/PWM mode the PWM counter is always 8-bit, and the PSIZE parameter has no effect.

The frequency of the PWM pulse waveform is determined by the formula:

$$f_{PWM} = \frac{f_{clock}}{(256 \times (LD + 1))}$$

where f_{PWM} is the frequency of the PWM, f_{clock} is the frequency of the input clock (32.768 KHz clock or Main system clock) and LD is the contents of the LD field.

Note: At a duty cycle value of 00h (in the MIN register), the LED output is fully off. At a duty cycle value of 255h, the LED output is fully on. Alternatively, In order to force the LED to be fully on, firmware can set the CONTROL field of the Configuration register to 3 (always on).

The other registers in the block do not affect the PWM or the LED output in Blinking/PWM mode.

33.9.3 BREATHING EXAMPLES

33.9.3.1 Linear LED brightness change

In this example, the brightness of the LED increases and diminishes in a linear fashion. The entire cycle takes 5 seconds. The rise time and fall time are 1.6 seconds, with a hold time at maximum brightness of 200ms and a hold time at minimum brightness of 1.6 seconds. The LED brightness varies between full off and full on. The PWM size is set to 8-bit, so the time unit for adjusting the PWM is approximately 8ms. The registers are configured as follows:

TABLE 33-8: LINEAR EXAMPLE CONFIGURATION

Field	Value							
PSIZE	8-bit							
MAX	255							
MIN	0							
HD	25 ticks (200ms)							
LD	200 ticks (1.6s)							
Duty cycle most significant bits	000b	001b	010b	011b	100b	101b	110b	1110
LED_INT	8	8	8	8	8	8	8	8
LED_STEP	10	10	10	10	10	10	10	10

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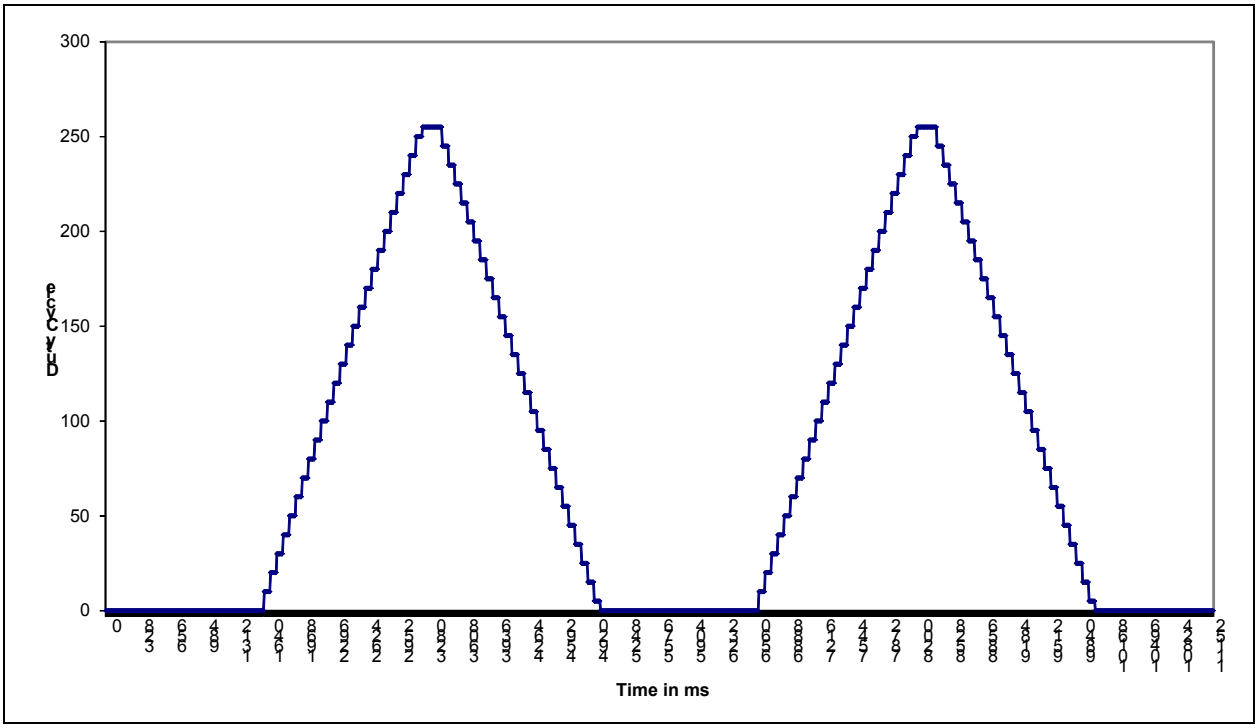
FIGURE 33-5: LINEAR BRIGHTNESS CURVE EXAMPLE



33.9.3.2 Non-linear LED brightness change

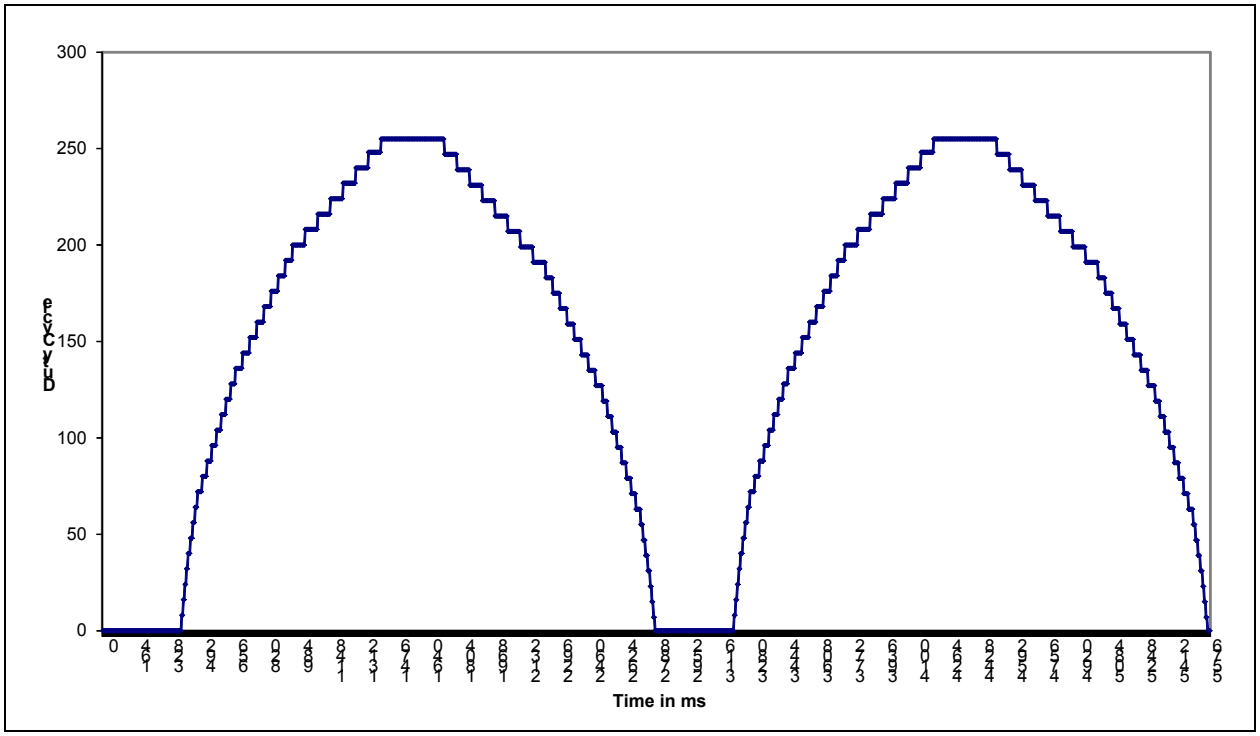
In this example, the brightness of the LED increases and diminishes in a non-linear fashion. The brightness forms a curve that is approximated by four piece wise-linear line segments. The entire cycle takes about 2.8 seconds. The rise time and fall time are about 1 second, with a hold time at maximum brightness of 320ms and a hold time at minimum brightness of 400ms. The LED brightness varies between full off and full on. The PWM size is set to 7-bit, so the time unit for adjusting the PWM is approximately 4ms. The registers are configured as follows:

TABLE 33-9: NON-LINEAR EXAMPLE CONFIGURATION

Field	Value							
PSIZE	7-bit							
MAX	255 (effectively 127)							
MIN	0							
HD	80 ticks (320ms)							
LD	100 ticks (400ms)							
Duty cycle most significant bits	000b	001b	010b	011b	100b	101b	110b	1110
LED_INT	2	3	6	6	9	9	16	16
LED_STEP	4	4	4	4	4	4	4	4

The resulting curve is shown in the following figure:

FIGURE 33-6: NON-LINEAR BRIGHTNESS CURVE EXAMPLE



33.10 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Blinking/Breathing PWM Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 33-10: REGISTER SUMMARY

Offset	Register Name
00h	LED Configuration Register
04h	LED Limits Register
08h	LED Delay Register
0Ch	LED Update Stepsize Register
10h	LED Update Interval Register
14h	LED Output Delay

In the following register definitions, a “PWM period” is defined by time the PWM counter goes from 000h to its maximum value (FFh in 8-bit mode, FEh in 7-bit mode and FCh in 6-bit mode, as defined by the PSCALE field in register LED_CFG). The end of a PWM period occurs when the PWM counter wraps from its maximum value to 0.

The registers in this block can be written 32-bits, 16-bits or 8-bits at a time. Writes to LED Configuration Register take effect immediately. Writes to LED Limits Register are held in a holding register and only take effect only at the end of a PWM period. The update takes place at the end of every period, even if only one byte of the register was updated. This means that in blink/PWM mode, software can change the duty cycle with a single 8-bit write to the MIN field in the LED_LIMIT register. Writes to LED Delay Register, LED Update Stepsize Register and LED Update Interval Register also go initially into a holding register. The holding registers are copied to the operating registers at the end of a PWM period only if the Enable Update bit in the LED Configuration Register is set to 1. If LED_CFG is 0, data in the holding registers is retained but not copied to the operating registers when the PWM period expires. To change an LED breath-

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ing configuration, software should write these three registers with the desired values and then set LED_CFG to 1. This mechanism ensures that all parameters affecting LED breathing will be updated consistently, even if the registers are only written 8 bits at a time.

33.10.1 LED CONFIGURATION REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
16	SYMMETRY 1=The rising and falling ramp times are in Asymmetric mode. Table 33-7, "Asymmetric Breathing Mode Register Usage" shows the application of the Stepsize and Interval registers to the four segments of rising duty cycles and the four segments of falling duty cycles. 0=The rising and falling ramp times (as shown in Figure 33-2, "Breathing LED Example") are in Symmetric mode. Table 33-6, "Symmetric Breathing Mode Register Usage" shows the application of the Stepsize and Interval registers to the 8 segments of both rising and falling duty cycles.	R/W	0b	RESET_SYS
15:8	WDT_RELOAD The PWM Watchdog Timer counter reload value. On system reset, it defaults to 14h, which corresponds to a 4 second Watchdog timeout value.	R/W	14h	RESET_SYS
7	RESET Writes of'1' to this bit resets the PWM registers to their default values. This bit is self clearing. Writes of '0' to this bit have no effect.	W	0b	RESET_SYS
6	ENABLE_UPDATE This bit is set to 1 when written with a '1'. Writes of '0' have no effect. Hardware clears this bit to 0 when the breathing configuration registers are updated at the end of a PWM period. The current state of the bit is readable any time. This bit is used to enable consistent configuration of LED_DELAY, LED_STEP and LED_INT. As long as this bit is 0, data written to those three registers is retained in a holding register. When this bit is 1, data in the holding register are copied to the operating registers at the end of a PWM period. When the copy completes, hardware clears this bit to 0.	R/WS	0b	RESET_SYS
5:4	PWM_SIZE This bit controls the behavior of PWM: 3=Reserved 2=PWM is configured as a 6-bit PWM 1=PWM is configured as a 7-bit PWM 0=PWM is configured as an 8-bit PWM	R/W	0b	RESET_SYS

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	SYNCHRONIZE When this bit is '1', all counters for all LEDs are reset to their initial values. When this bit is '0' in the LED Configuration Register for all LEDs, then all counters for LEDs that are configured to blink or breathe will increment or decrement, as required. To synchronize blinking or breathing, the SYNCHRONIZE bit should be set for at least one LED, the control registers for each LED should be set to their required values, then the SYNCHRONIZE bits should all be cleared. If the all LEDs are set for the same blink period, they will all be synchronized.	R/W	0b	RESET_SYS
2	CLOCK_SOURCE This bit controls the base clock for the PWM. It is only valid when CNTRL is set to blink (2). 1=Clock source is the Main system clock 0=Clock source is the 32.768 KHz clock	R/W	0b	RESET_SYS
1:0	CONTROL This bit controls the behavior of PWM: 3=PWM is always on 2=LED blinking (standard PWM) 1=LED breathing configuration 0=PWM is always off. All internal registers and counters are reset to 0. Clocks are gated	R/W	00b	RESET_SYS
			11b	WDT TC

33.10.2 LED LIMITS REGISTER

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period. The two byte fields may be written independently. Reads of this register return the current contents and not the value of the holding register.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:8	MAXIMUM In breathing mode, when the current duty cycle is greater than or equal to this value the breathing apparatus holds the current duty cycle for the period specified by the field HD in register LED_DELAY, then starts decrementing the current duty cycle	R/W	0h	RESET_SYS
7:0	MINIMUM In breathing mode, when the current duty cycle is less than or equal to this value the breathing apparatus holds the current duty cycle for the period specified by the field LD in register LED_DELAY, then starts incrementing the current duty cycle In blinking mode, this field defines the duty cycle of the blink function.	R/W	0h	RESET_SYS

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33.10.3 LED DELAY REGISTER

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period if the Enable Update bit in the LED Configuration register is set to 1. Reads of this register return the current contents and not the value of the holding register.

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:24	Reserved	R	-	-
23:12	HIGH_DELAY In breathing mode, the number of PWM periods to wait before updating the current duty cycle when the current duty cycle is greater than or equal to the value MAX in register LED_LIMIT. 4095=The current duty cycle is decremented after 4096 PWM periods … 1=The delay counter is bypassed and the current duty cycle is decremented after two PWM period 0=The delay counter is bypassed and the current duty cycle is decremented after one PWM period	R/W	000h	RESET_SYS
11:0	LOW_DELAY The number of PWM periods to wait before updating the current duty cycle when the current duty cycle is greater than or equal to the value MIN in register LED_LIMIT. 4095=The current duty cycle is incremented after 4096 PWM periods … 0=The delay counter is bypassed and the current duty cycle is incremented after one PWM period In blinking mode, this field defines the prescalar for the PWM clock	R/W	000h	RESET_SYS

33.10.4 LED UPDATE STEPSIZE REGISTER

This register has eight segment fields which provide the amount the current duty cycle is adjusted at the end of every PWM period. Segment field selection is decoded based on the segment index. The segment index equation utilized depends on the SYMMETRY bit in the LED Configuration Register Register)

- In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]
- In Asymmetric Mode the Segment_Index[2:0] is the bit concatenation of following: Segment_Index[2] = (FALLING RAMP TIME in Figure 33-3, "Clipping Example") and Segment_Index[1:0] = Duty Cycle Bits[7:6].

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period if the Enable Update bit in the LED Configuration register is set to 1. Reads of this register return the current contents and not the value of the holding register.

In 8-bit mode, each 4-bit STEPSIZE field represents 16 possible duty cycle modifications, from 1 to 16 as the duty cycle is modified between 0 and 255:

15: Modify the duty cycle by 16

...

1: Modify the duty cycle by 2

0=Modify the duty cycle by 1

In 7-bit mode, the least significant bit of the 4-bit field is ignored, so each field represents 8 possible duty cycle modifications, from 1 to 8, as the duty cycle is modified between 0 and 127:

14, 15: Modify the duty cycle by 8

...

2, 3: Modify the duty cycle by 2

0, 1: Modify the duty cycle by 1

In 6-bit mode, the two least significant bits of the 4-bit field is ignored, so each field represents 4 possible duty cycle modifications, from 1 to 4 as the duty cycle is modified between 0 and 63:

12, 13, 14, 15: Modify the duty cycle by 4

8, 9, 10, 11: Modify the duty cycle by 3

4, 5, 6, 7: Modify the duty cycle by 2

0, 1, 2, 3: Modify the duty cycle by 1

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	UPDATE_STEP7 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 111.	R/W	0h	RESET_SYS
27:24	UPDATE_STEP6 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 110.	R/W	0h	RESET_SYS
23:20	UPDATE_STEP5 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 101	R/W	0h	RESET_SYS
19:16	UPDATE_STEP4 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 100.	R/W	0h	RESET_SYS
15:12	UPDATE_STEP3 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 011.	R/W	0h	RESET_SYS
11:8	UPDATE_STEP2 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 010.	R/W	0h	RESET_SYS
7:4	UPDATE_STEP1 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 001.	R/W	0h	RESET_SYS
3:0	UPDATE_STEP0 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 000.	R/W	0h	RESET_SYS

33.10.5 LED UPDATE INTERVAL REGISTER

This register has eight segment fields which provide the number of PWM periods between updates to current duty cycle. Segment field selection is decoded based on the segment index. The segment index equation utilized depends on the SYMMETRY bit in the LED Configuration Register Register)

- In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]
- In Asymmetric Mode the Segment_Index[2:0] is the bit concatenation of following: Segment_Index[2] = (FALLING RAMP TIME in Figure 33-3, "Clipping Example") and Segment_Index[1:0] = Duty Cycle Bits[7:6].

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period if the Enable Update bit in the LED Configuration register is set to 1. Reads of this register return the current contents and not the value of the holding register.

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Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	UPDATE_INTERVAL7 The number of PWM periods between updates to current duty cycle when the segment index is equal to 111b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
27:24	UPDATE_INTERVAL6 The number of PWM periods between updates to current duty cycle when the segment index is equal to 110b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
23:20	UPDATE_INTERVAL5 The number of PWM periods between updates to current duty cycle when the segment index is equal to 101b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
19:16	UPDATE_INTERVAL4 The number of PWM periods between updates to current duty cycle when the segment index is equal to 100b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
15:12	UPDATE_INTERVAL3 The number of PWM periods between updates to current duty cycle when the segment index is equal to 011b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
11:8	UPDATE_INTERVAL2 The number of PWM periods between updates to current duty cycle when the segment index is equal to 010b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	UPDATE_INTERVAL1 The number of PWM periods between updates to current duty cycle when the segment index is equal to 001b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
3:0	UPDATE_INTERVAL0 The number of PWM periods between updates to current duty cycle when the segment index is equal to 000b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS

33.10.6 LED OUTPUT DELAY

This register permits the transitions for multiple blinking/breathing LED outputs to be skewed, so as not to present too great a current load. The register defines a count for the number of clocks the circuitry waits before turning on the output, either on initial enable, after a resume from Sleep, or when multiple outputs are synchronized through the Sync control in the LED CONFIGURATION (LED_CFG) register.

When more than one LED outputs are used simultaneously, the LED OUTPUT DELAY fields of each should be configured with different values so that the outputs are skewed. When used with the 32KHz clock domain as a clock source, the differences can be as small as 1.

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	OUTPUT_DELAY The delay, in counts of the clock defined in Clock Source (CLKSRC), in which output transitions are delayed. When this field is 0, there is no added transition delay. When the LED is programmed to be Always On or Always Off, the Output Delay field has no effect.	R/W	000h	RESET_SYS

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34.0 RC IDENTIFICATION DETECTION (RC_ID)

34.1 Introduction

The Resistor/Capacitor Identification Detection (RC_ID) interface provides a single pin interface which can discriminate a number of quantized RC constants.

34.2 References

No references have been cited for this feature.

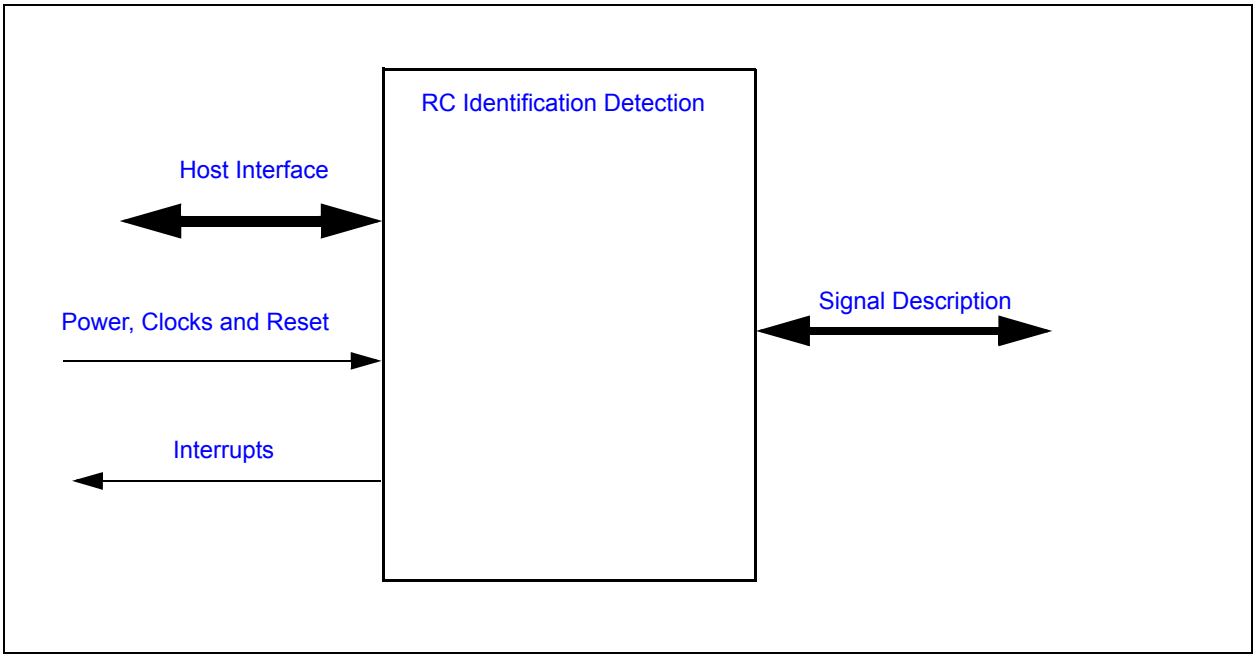
34.3 Terminology

There is no terminology defined for this section.

34.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 34-1: I/O DIAGRAM OF BLOCK



34.5 Signal Description

Name	Direction	Description
RC_ID	Input	Analog input used for measuring an external Resistor-Capacitor delay.

34.6 Host Interface

The registers defined for this block are accessible by the various hosts as indicated in Section 34.12, "EC Registers".

34.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

34.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

34.7.2 CLOCK INPUTS

Name	Description
48MHz	The main clock domain, used to generate the time base that measures the RC delay.

34.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

34.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
RCID	This internal signal is generated when the DONE bit in the RC_ID Control Register is set to ‘1’.

34.9 Low Power Modes

This block may be put into a low power state by the chip’s Power, Clocks, and Reset (PCR) circuitry. If a measurement has been started, the block will continue to assert its clock_req output until the measurement completes.

34.10 Description

Note: The RC_ID block only operates on 3.3V. The VTR pin associated with RC_ID signals must be connected to a 3.3V supply. If the VTR pin is supplied with 1.8V, the RC_ID logic will not function correctly.

The Resistor/Capacitor Identification Detection (RC_ID) interface provides a single pin interface which can discriminate a number of quantized RC constants. The judicious selection of RC values can provide a low cost means for system element configuration identification. The RC_ID I/O pin measures the charge/discharge time for an RC circuit connected to the pin as shown in Figure 34-2.

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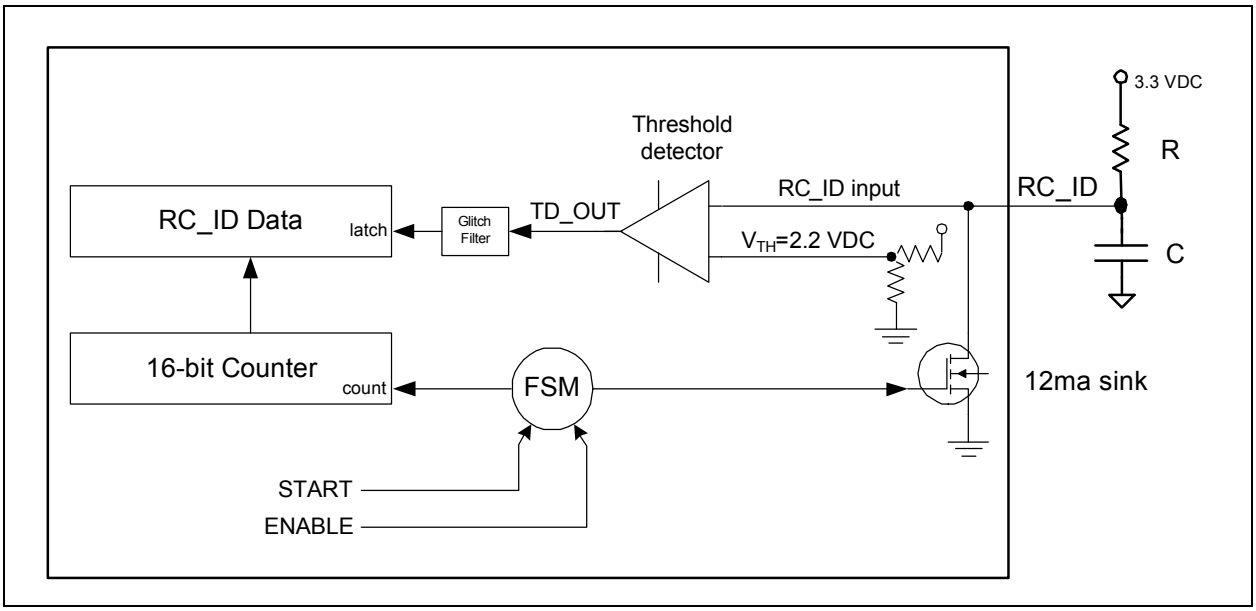
FIGURE 34-2: BLOCK DIAGRAM OF RC Identification Detection (RC_ID)



The RC_ID interface determines the selected RC delay by measuring the rise time on the RC_ID pin that is attached to the RC circuit, as shown in the above figure. The measurement is performed by first discharging the external capacitor for a fixed period of time, set by an internal 16-bit counter running at a configurable time base, and then letting the capacitor charge again, using the same counter and time base to count how many clock ticks are required until the voltage on the capacitor exceeds 2.2V. A glitch filter, consisting of three ticks of the 48MHz main oscillator, smooths the threshold detection.

By fixing the capacitor value and varying the resistor value, up to eight discrete values can be determined based on the final count. Section 34.11, "Time Constants" shows a range of possible R and C values that can be used to create eight ID values.

Measurement requires five phases:

1. Reset. The two control bits (ENABLE and START) and the three status bits (TC, DONE and CY_ER) in the RC_ID Control Register are all '0'. The RD_IC pin is tri-stated and the block is in its lowest power state. In order to enter the Reset state, firmware must write the ENABLE, START and CLOCK_SET fields to '0' simultaneously or unpredictable results may occur.
2. Armed. Firmware enables the transition to this state by setting the ENABLE bit to '1' and the CLOCK_SET field to the desired time base. The START must remain at '0'. All three fields must be set with one write to the RC_ID Control Register. In this state the RC_ID clock is enabled and the 16-bit counter is armed. Firmware must wait a minimum of 300µS in the Armed phase before starting the Discharged phase.
3. Discharged. Firmware initiates the transition to the Discharged state by setting the ENABLE bit to '1', the START bit to '1' and the CLOCK_SET field to the desired clock rate, in a single write to the RC_ID Control Register. The RC_ID pin is discharged while the 16-bit counter counts from 0000h to FFFFh at the configured time base. When the counter reaches FFFFh the TC status bit is set to '1'. If at the end of the Discharged state the RC_ID pin remains above the 2.2V threshold, the CY_ER bit is set to '1', since the measurement will not be valid.
4. Charged.The RC_ID state machine automatically transitions to this state after the 16-bit counter reaches FFFFh while in the Discharged state. The 16-bit counter starts counting up from 0000h. The counter stops counting and its value is copied into the RC_ID Data Register when the voltage on the pin exceeds 2.2V. If the counter reaches FFFFh and the pin voltage remains below 2.2V, the CY_ER bit is set to '1'.
5. Done. After the counter stops counting, either because the pin voltage exceed the 2.2V threshold or the 16-bit counter reached FFFFh, the state machine transitions to this state. The DONE bit is set to '1' and the RC_ID interface re-enters its lowest power state. The interface will remain in the Done state until firmware explicitly initiates the Reset state.

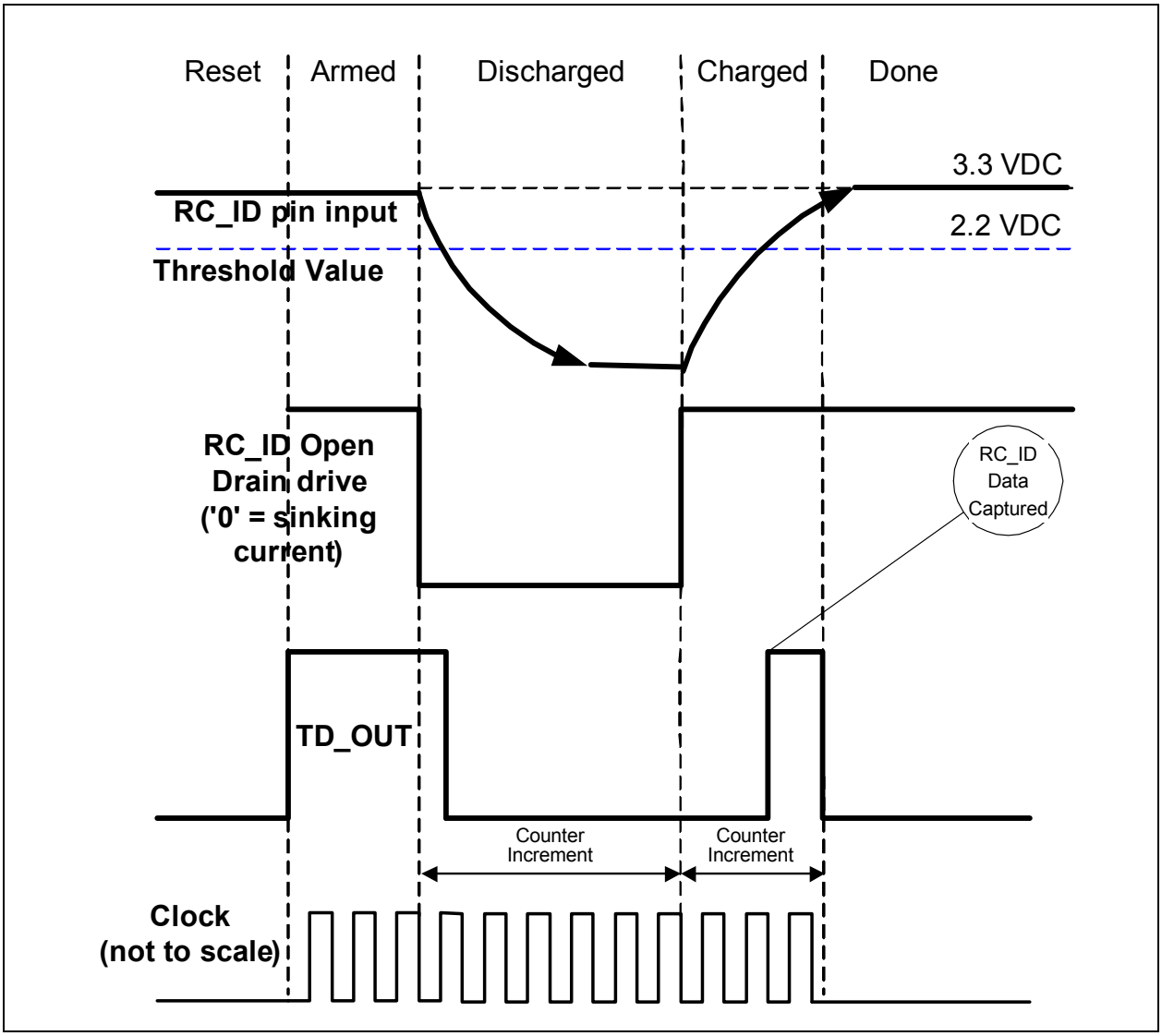
A new measurement must be started by putting the RC_ID Interface into the "Reset" state.

The five phases, along with the values of the control and status bits in the Control Register at the end of each phase, are summarized in the following table and figure:

TABLE 34-1: RC ID STATE TRANSITIONS

	State	ENABLE	START	TC	DONE
1.	Reset	0	0	0	0
2.	Armed	1	0	0	0
3.	Discharged	1	1	0	0
4.	Charged	1	1	1	0
5.	Done	1	1	1	1

FIGURE 34-3: RCID STATE TRANSITIONS



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34.11 Time Constants

This section lists a set of R and C values which can be connected to the RC_ID pin. Note that risetime generally follow RC time Tau. Firmware should use the Max and Min Counts in the tables to create quantized states.

In the following tables, the CLOCK_SET field in the RC_ID Control Register is set to '0', so the time base for measuring the rise time is 48MHz, the speed of the system clock. All capacitor values are ±10% and all resistor values are ±5%. Minimum and maximum count values are suggested ranges, calculated to provide reasonable margins around the nominal rise times. Rise times have been confirmed by laboratory measurements.

TABLE 34-2: SAMPLE RC VALUES, C=2200PF

R (KΩ)	Nominal Tau (µS)	Minimum Count	Maximum Count
1	2.2	60.00	72.00
2	4.4	115.00	140.00
4.3	9.5	241.00	294.00
8.2	18.04	456.00	557.00
33	72.6	1819.00	2224.00
62	136.4	3456.00	4224.00
130	286	7470.00	9130.00
240	528	14400.00	17600.00

TABLE 34-3: SAMPLE RC VALUES, C=3000PF

R (KΩ)	Nominal Tau (µS)	Minimum Count	Maximum Count
1	3	77.00	95.00
2	6	151.00	184.00
4.3	12.9	320.00	391.00
8.2	24.6	604.00	739.00
33	99	2439.00	2981.00
62	186	4647.00	5680.00
130	390	9990.00	12210.00
240	720	193508.00	23650.00

TABLE 34-4: SAMPLE RC VALUES, C=4700PF

R (KΩ)	Nominal Tau (µS)	Minimum Count	Maximum Count
1	4.7	116.00	142.00
2	9.4	229.00	280.00
4.3	20.2	495.00	605.00
8.2	38.5	945.00	1160.00
33	155.1	3780.00	4650.00
62	291.4	7249.00	8859.00
130	611	15480.00	18920.00
240	1128	29880.00	36520.00

34.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the RC Identification Detection (RC_ID) Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 34-5: REGISTER SUMMARY

Offset	Register Name
00h	RC_ID Control Register
04h	RC_ID Data Register

34.12.1 RC_ID CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:8	CLOCK_SET This field selects the frequency of the Counter circuit clock. This field must retain the same value as long as the ENABLE bit in this register is ‘1’. 3=6MHz 2=12MHz 1=24MHz 0=48MHz	R/W	0h	RESET_SYS
7	ENABLE Clearing the bit to ‘0’ causes the RC_ID interface to enter the Reset state, gating its clocks, clearing the status bits in this register and entering into its lowest power state. Setting this bit to ‘1’ causes the RC_ID interface to enter the Armed phase of an RC_ID measurement. When this bit is cleared to ‘0’, the CLOCK_SET and START fields in this register must also be cleared to ‘0’ in the same register write.	R/W	0h	RESET_SYS
6	START Setting this bit to ‘1’ initiates the Discharged phase of an RC_ID measurement. Writes that change this bit from ‘0’ to ‘1’ must also write the ENABLE bit to ‘1’, and must not change the CLOCK_SET field. A period of at least 300µS must elapse between setting the ENABLE bit to ‘1’ and setting this bit to ‘1’.	R/W	0h	RESET_SYS
5:3	Reserved	R	-	-

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Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	CY_ER This bit is ‘1’ if an RC_ID measurement encountered an error and the reading in the RC_ID Data Register is invalid. This bit is cleared to ‘0’ when the RC_ID interface is in the Reset phase. It is set either if during the Discharged phase the RC_ID pin did not fall below the 2.2V threshold, or if in the Charged phase the RC_ID pin did not rise above the 2.2V threshold and the 16-bit counter ended its count at FFFFh.	R	0h	RESET_SYS
1	TC This bit is cleared to ‘0’ when the RC_ID interface is in the Reset phase, and set to ‘1’ when the interface completes the Discharged phase of an RC_ID measurement.	R	0h	RESET_SYS
0	DONE This bit is cleared to ‘0’ when the RC_ID interface is in the Reset phase, and set to ‘1’ when the interface completes an RC_ID measurement.	R	0h	RESET_SYS

34.12.2 RC_ID DATA REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	DATA Reads of this register provide the result of an RC_ID measurement.	R	0h	RESET_SYS

35.0 KEYBOARD SCAN INTERFACE

35.1 Overview

The Keyboard Scan Interface block provides a register interface to the EC to directly scan an external keyboard matrix of size up to 18x8.

The maximum configuration of the Keyboard Scan Interface is 18 outputs by 8 inputs. For a smaller matrix size, firmware should configure unused KSO pins as GPIOs or another alternate function, and it should mask out unused KSIs and associated interrupts.

35.2 References

No references have been cited for this feature.

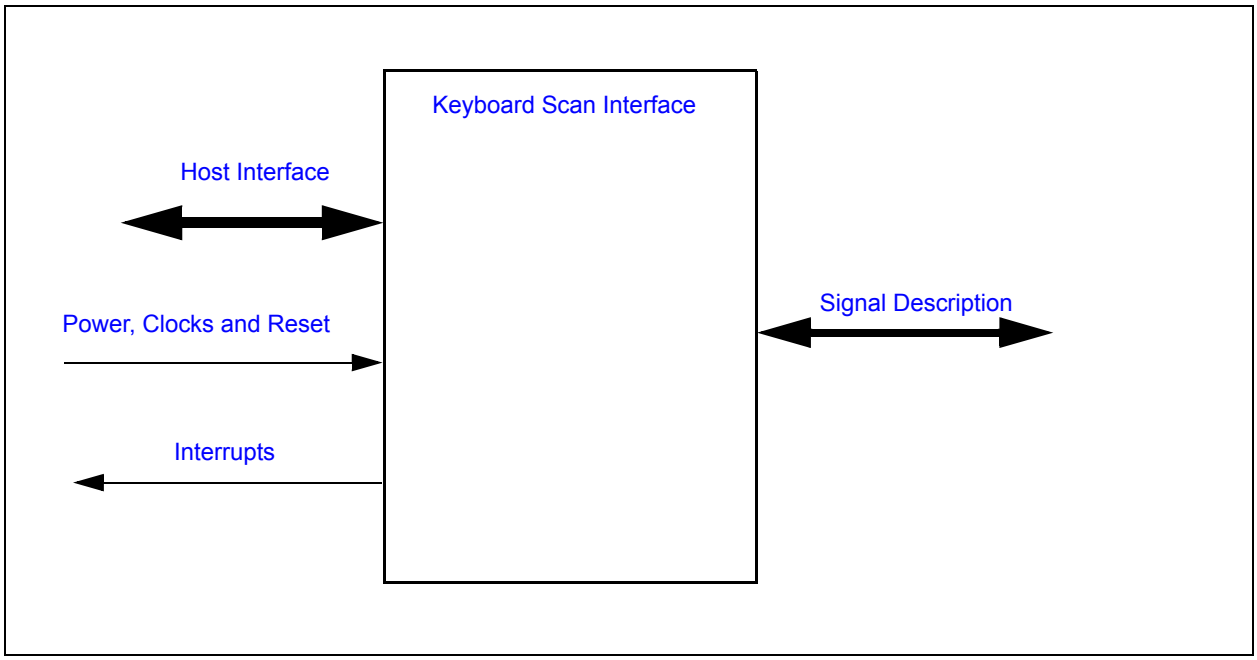
35.3 Terminology

There is no terminology defined for this section.

35.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 35-1: I/O DIAGRAM OF BLOCK



35.5 Signal Description

Name	Direction	Description
KSI[7:0]	Input	Column inputs from external keyboard matrix.
KSO[17:0]	Output	Row outputs to external keyboard matrix.

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35.6 Host Interface

The registers defined for the Keyboard Scan Interface are accessible by the various hosts as indicated in Section 35.11, "EC Registers".

35.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

35.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

35.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for Keyboard Scan Interface logic.

35.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

35.8 Interrupts

This section defines the Interrupt Sources generated from this block.

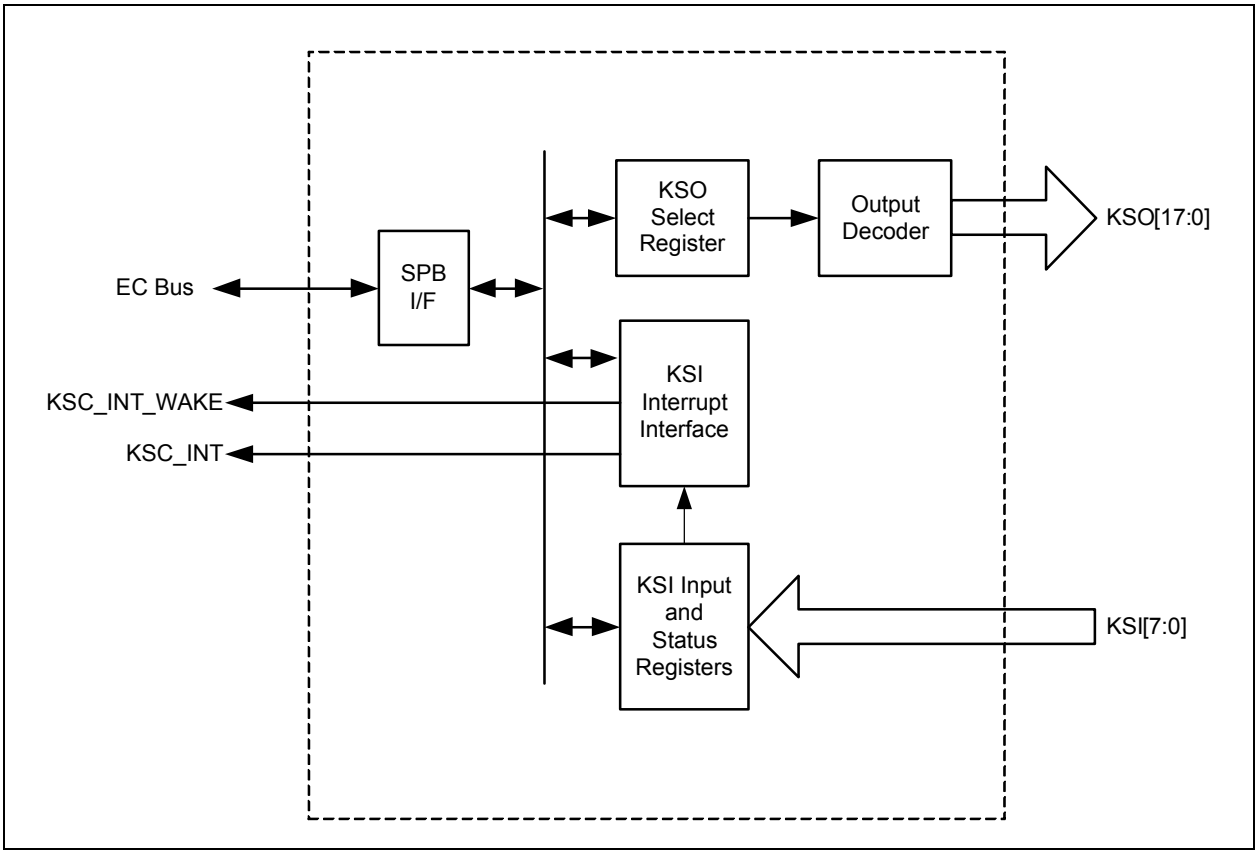
Source	Description
KSC_INT	Interrupt request to the Interrupt Aggregator.
KSC_INT_WAKE	Wake-up request to the Interrupt Aggregator’s wake-up interface.

35.9 Low Power Modes

The Keyboard Scan Interface automatically enters a low power mode whenever it is not actively scanning the keyboard matrix. The block is also placed in a low-power state when it is disabled by the KSEN bit. When the interface is in a low-power mode it will not prevent the chip from entering a sleep state. When the interface is active it will inhibit the chip sleep state until the interface has re-entered its low power mode.

35.10 Description

FIGURE 35-2: KEYBOARD SCAN INTERFACE BLOCK DIAGRAM



During scanning the firmware sequentially drives low one of the rows (KSO[17:0]) and then reads the column data line (KSI[7:0]). A key press is detected as a zero in the corresponding position in the matrix. Keys that are pressed are debounced by firmware. Once confirmed, the corresponding keycode is loaded into host data read buffer in the 8042 Host Interface module. Firmware may need to buffer keycodes in memory in case this interface is stalled or the host requests a Resend.

35.10.1 INITIALIZATION OF KSO PINS

If the Keyboard Scan Interface is not configured for PREDRIVE Mode, KSO pins should be configured as open-drain outputs. Internal or external pull-ups should be used so that the GPIO functions that share the pins do not have a floating input when the KSO pins are tri-stated.

If the Keyboard Scan Interface is configured for PREDRIVE Mode, KSO pins must be configured as push-pull outputs. Internal or external pull-ups should be used to protect the GPIO inputs associated with the KSO pins from floating inputs.

35.10.2 PREDRIVE MODE

There is an optional Predrive Mode that can be enabled to actively drive the KSO pins high before switching to open-drain operation. The PREDRIVE ENABLE bit in the Keyscan Extended Control Register is used to enable the PREDRIVE option. Timing for the Predive mode is shown in Section 51.15, Keyboard Scan Matrix Timing.

35.10.2.1 Predrive Mode Programming

The following precautions should be taken to prevent output pad damage during Predrive Mode Programming.

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35.10.2.2 Asserting PREDRIVE_ENABLE

1. Disable Key Scan Interface (KSEN = '1')
2. Enable Predrive function (PREDRIVE_ENABLE = '1')
3. Program buffer type for all KSO pins to "push-pull”
4. Enable Keyscan Interface (KSEN ='0')

35.10.2.3 De-asserting PREDRIVE_ENABLE

1. Disable Key Scan Interface (KSEN = '1')
2. Program buffer type for all KSO pins to "open-drain”
3. Disable Predrive function (PREDRIVE_ENABLE = '0')
4. Enable Keyscan Interface (KSEN ='0')

35.10.3 INTERRUPT GENERATION

To support interrupt-based processing, an interrupt can optionally be generated on the high-to-low transition on any of the KSI inputs. A running clock is not required to generate interrupts.

35.10.3.1 Runtime interrupt

KSC_INT is the block’s runtime active-high level interrupt. It is connected to the interrupt interface of the Interrupt Aggregator, which then relays interrupts to the EC.

Associated with each KSI input is a status register bit and an interrupt enable register bit. A status bit is set when the associated KSI input goes from high to low. If the interrupt enable bit for that input is set, an interrupt is generated. An Interrupt is de-asserted when the status bit and/or interrupt enable bit is clear. A status bit cleared when written to a ‘1’.

Interrupts from individual KSIs are logically ORed together to drive the KSC_INT output port. Once asserted, an interrupt is not asserted again until either all KSI[7:0] inputs have returned high or the has changed.

35.10.3.2 Wake-up interrupt

KSC_INT_WAKE is the block’s wakeup interrupt. It is routed to the Interrupt Aggregator.

During sleep mode, i.e., when the bus clock is stopped, a high-to-low transition on any KSI whose interrupt enable bit is set causes the KSC_INT_WAKE to be asserted. The block also indicates that it requires a clock to the system Power Management Interface. KSC_WAKEUP_INT remains active until the bus clock is started.

The aforementioned transition on KSI also sets the corresponding status bit in the KSI STATUS Register. If enabled, a runtime interrupt is also asserted on KSC_INT when the bus clock resumes running.

35.10.4 WAKE PROGRAMMING

Using the Keyboard Scan Interface to ‘wake’ the MEC170x can be accomplished using either the Keyboard Scan Interface wake interrupt, or using the wake capabilities of the GPIO Interface pins that are multiplexed with the Keyboard Scan Interface pins. Enabling the Keyboard Scan Interface wake interrupt requires only a single interrupt enable access and is recommended over using the GPIO Interface for this purpose.

35.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Keyboard Scan Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 35-1: EC-ONLY REGISTER SUMMARY

Offset	Register Name
0h	Reserved
4h	KSO Select Register
8h	KSI INPUT Register
Ch	KSI STATUS Register
10h	KSI INTERRUPT ENABLE Register
14h	Keyscan Extended Control Register

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35.11.1 KSO SELECT REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
7	KSO_INVERT This bit controls the output level of KSO pins when selected. 0=KSO[x] driven low when selected 1=KSO[x] driven high when selected.	R/W	0h	RESET_SYS
6	KSEN This field enables and disables keyboard scan 0=Keyboard scan enabled 1=Keyboard scan disabled. All KSO output buffers disabled.	R/W	1h	RESET_SYS
5	KSO_ALL 0=When key scan is enabled, KSO output controlled by the KSO_SELECT field. 1=KSO[x] driven high when selected.	R/W	0h	RESET_SYS
4:0	KSO_SELECT This field selects a KSO line (00000b = KSO[0] etc.) for output according to the value off KSO_INVERT in this register. See Table 35-2, "KSO Select Decode"	R/W	0h	RESET_SYS

TABLE 35-2: KSO SELECT DECODE

KSO Select [4:0]	KSO Selected
00h	KSO00
01h	KSO01
02h	KSO02
03h	KSO03
04h	KSO04
05h	KSO05
06h	KSO06
07h	KSO07
08h	KSO08
09h	KSO09
0Ah	KSO10
0Bh	KSO11
0Ch	KSO12
0Dh	KSO13
0Eh	KSO14
0Fh	KSO15

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TABLE 35-2: KSO SELECT DECODE (CONTINUED)

KSO Select [4:0]	KSO Selected
10h	KSO16
11h	KSO17

TABLE 35-3: KEYBOARD SCAN OUT CONTROL SUMMARY

KSO_INVERTt	KSEN	KSO_ALL	KSO_SELECT	Description
X	1	x	x	Keyboard Scan disabled. KSO[17:0] output buffers disabled.
0	0	0	10001b-00000b	KSO[Drive Selected] driven low. All others driven high
1	0	0	10001b-00000b	KSO[Drive Selected] driven high. All others driven low
0	0	0	11111b-10010b	All KSO's driven high
1	0	0	11111b-10010b	All KSO's driven low
0	0	1	x	All KSO's driven high
1	0	1	x	All KSO's driven low

35.11.2 KSI INPUT REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	KSI This field returns the current state of the KSI pins.	R	0h	RESET_SYS

35.11.3 KSI STATUS REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	KSI_STATUS Each bit in this field is set on the falling edge of the corresponding KSI input pin. A KSI interrupt is generated when its corresponding status bit and interrupt enable bit are both set. KSI interrupts are logically ORed together to produce KSC_INT and KSC_INT_WAKE. Writing a '1' to a bit will clear it. Writing a '0' to a bit has no effect.	R/WC	0h	RESET_SYS

35.11.4 KSI INTERRUPT ENABLE REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	KSI_INT_EN Each bit in KSI_INT_EN enables interrupt generation due to high-to-low transition on a KSI input. An interrupt is generated when the corresponding bits in KSI_STATUS and KSI_INT_EN are both set.	R/W	0h	RESET_SYS

35.11.5 KEYSCAN EXTENDED CONTROL REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
32:1	Reserved	R	-	-
0	PREDRIVE_ENABLE PREDRIVE_ENABLE enables the PREDRIVE mode to actively drive the KSO pins high for two 48 MHz PLL clocks before switching to open-drain operation. 0=Disable predrive on KSO pins 1=Enable predrive on KSO pins.	R/W	0h	RESET_SYS

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36.0 I2C/SMBUS INTERFACE

36.1 Introduction

This section describes the Power Domain, Resets, Clocks, Interrupts, Registers and the Physical Interface of the I2C/SMBus interface. For a General Description, Features, Block Diagram, Functional Description, Registers Interface and other core-specific details, *see* Ref [1] (note: in this chapter, *italicized text* typically refers to SMB-I2C Controller core interface elements as described in Ref [1]).

36.2 References

1. I2C_SMB Controller Core with Network Layer Support (SMB2) - 16MHz I2C Baud Clock“, Revision 3.6, Core-Level Architecture Specification, Microchip, date TBD

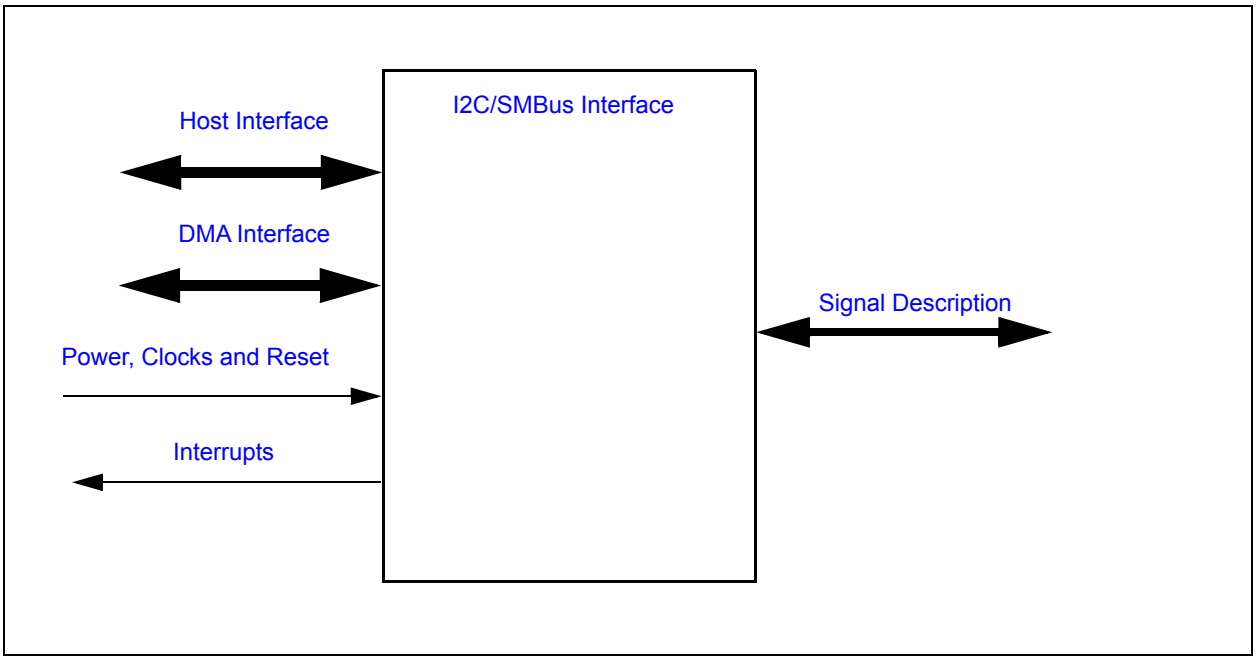
36.3 Terminology

There is no terminology defined for this chapter.

36.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface. In addition, this block is equipped with:

FIGURE 36-1: I/O DIAGRAM OF BLOCK



36.5 Signal Description

see the Pin Configuration section for a description of the SMB-I2C pin configuration.

36.6 Host Interface

The registers defined for the I2C/SMBus Interface are accessible as indicated in Section 36.12, "EC Registers".

36.7 DMA Interface

This block is designed to communicate with the Internal DMA Controller. This feature is defined in the SMB-I2C Controller Core Interface specification (*See* Ref [1]).

Note: For a description of the Internal DMA Controller implemented in this design see Section 7.0, "Internal DMA Controller".

36.8 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

36.8.1 POWER DOMAINS

Name	Description
VTR	This power well sources all of the registers and logic in this block, except where noted.

36.8.2 CLOCK INPUTS

Name	Description
16MHz	This is the clock signal drives the SMB-I2C Controller core. The core also uses this clock to generate the SMB-I2C_CLK on the pin interface. It is derived from the main system clock

36.8.3 RESETS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in the SMB-I2C Controller core.

36.9 Interrupts

Source	Description
SMB-I2C	I^2C Activity Interrupt Event
SMB-I2C_WAKE	This interrupt event is triggered when an SMB/I2C Master initiates a transaction by issuing a START bit (a high-to-low transition on the SDA line while the SCL line is high) on the bus currently connected to the SMB-I2C Controller. The EC interrupt handler for this event only needs to clear the interrupt SOURCE bit and return; if the transaction results in an action that requires EC processing, that action will trigger the SMB-I2C interrupt event.

36.10 Low Power Modes

The SMB-I2C Controller may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

36.11 Description

36.11.1 SMB-I2C CONTROLLER CORE

The SMB-I2C Controller behavior is defined in the SMB-I2C Controller Core Interface specification (*See* Ref [1]).

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36.11.2 PHYSICAL INTERFACE

The Physical Interface for the SMB-I2C Controller core is configurable for up to 15 ports. Each I2C_WAKE Controller can be connected to any of the ports defined in Table 36-1, "SMB-I2C Port Selection". The *PORT SEL [3:0]* bit field in each controller independently sets the port for the controller. The default for each field is Fh, Reserved, which means that the SMB-I2C Controller is not connected to a port.

An I^2C port should be connected to a single controller. An attempt to configure the *PORT SEL [3:0]* bits in one controller to a value already assigned to another controller may result in unexpected results.

The port signal-function names and pin numbers are defined in Pin Configuration section. The I^2C port selection is made using the *PORT SEL [3:0]* bits in the *Configuration Register* as described in Ref [1].. In the Pin section, the SDL (Data) pins are listed as SMB*i*_DATA and the SCL (Clock) pins are listed as I2C*i*_CLK, where *i* represents the port number 00 through 10. The CPU-voltage-level port SB_TSI is also listed in the pin section with the pins _DATA and _CLK.

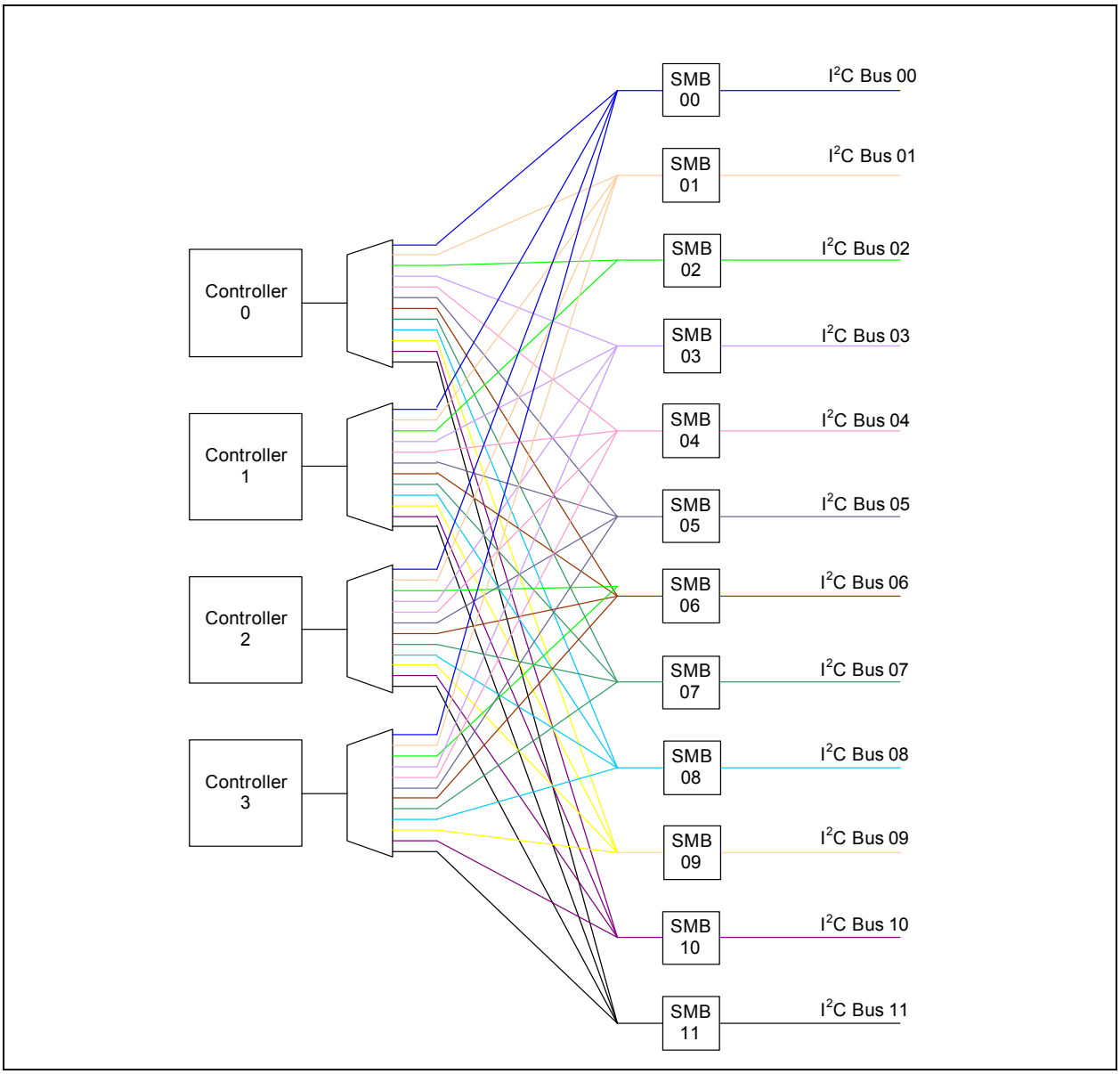
For I^2C port signal functions that are alternate functions of GPIO pins, the buffer type for these pins must be configured as open-drain outputs when the port is selected as an I^2C port.

For more information regarding the SMB-I2C Controller core see *Section 2.2,* "*Physical Interface*" in Ref[1].

TABLE 36-1: SMB-I2C PORT SELECTION

PORT_SEL[3:0]				Port
3	**2**	**1**	**0**	
0	0	0	0	SMB00 or I2C00
0	0	0	1	SMB01 or I2C01
0	0	1	0	SMB02 or I2C02
0	0	1	1	SMB03 or I2C03
0	1	0	0	SMB04 or I2C04
0	1	0	1	SMB05 or I2C05
0	1	1	0	SMB06 or I2C06
0	1	1	1	SMB07 or I2C07
1	0	0	0	SMB08 or I2C08
1	0	0	1	SMB09 or I2C09
1	0	1	0	SMB10 or I2C10
1	0	1	1	SB-TSI
1100b - 1111b				Reserved

FIGURE 36-2: SMB-I2C PORT CONNECTIVITY



36.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the SMB-I2C Controller Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

Registers for the SMB-I2C Controllers are listed in Reference[1].

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37.0 GENERAL PURPOSE SERIAL PERIPHERAL INTERFACE

37.1 Overview

The General Purpose Serial Peripheral Interface (GP-SPI) may be used to communicate with various peripheral devices, e.g., EEPROMS, DACs, ADCs, that use a standard Serial Peripheral Interface.

.Characteristics of the GP-SPI Controller include:

- 8-bit serial data transmitted and received simultaneously over two data pins in Full Duplex mode with options to transmit and receive data serially on one data pin in Half Duplex (Bidirectional) mode.
- An internal programmable clock generator and clock polarity and phase controls allowing communication with various SPI peripherals with specific clocking requirements.
- SPI cycle completion that can be determined by status polling or interrupts.
- The ability to read data in on both SPDIN and SPDOUT in parallel. This allows this SPI Interface to support dual data rate read accesses for emerging double rate SPI flashes
- Support of back-to-back reads and writes without clock stretching, provided the host can read and write the data registers within one byte transaction time.

37.2 References

No references have been cited for this feature.

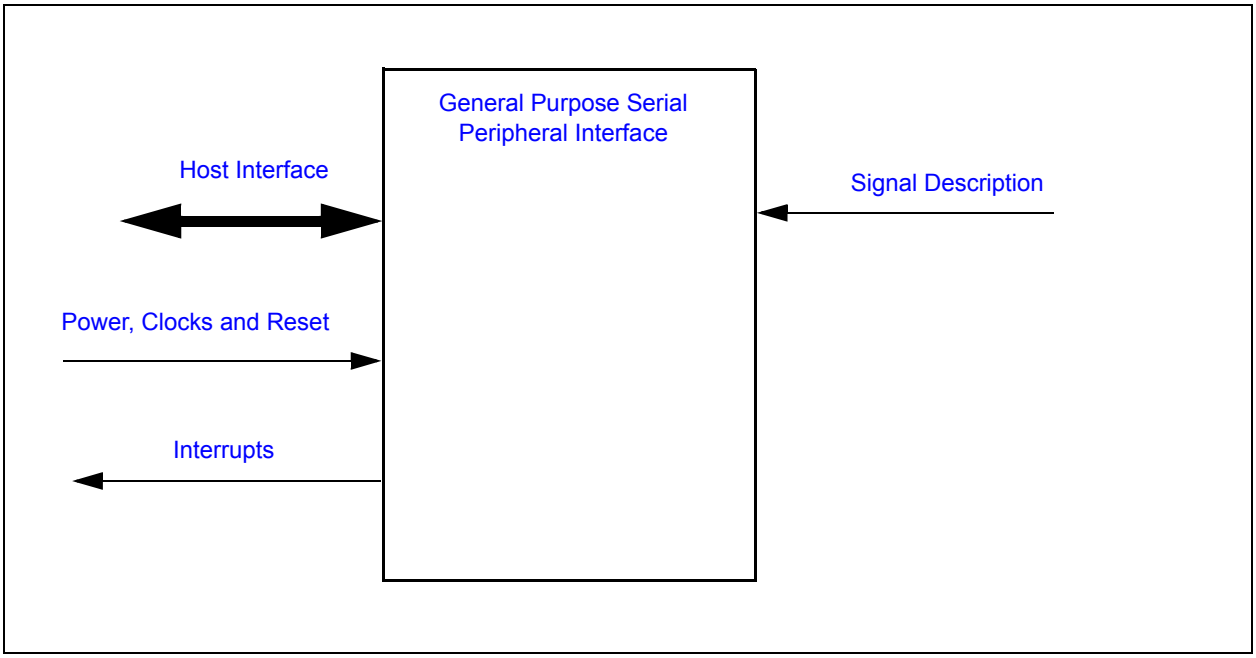
37.3 Terminology

No terminology for this block.

37.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 37-1: I/O DIAGRAM OF BLOCK



37.5 Signal Description

See the Pin Description chapter for the pins and the signal names associated with the following signals.

TABLE 37-1: EXTERNAL SIGNAL DESCRIPTION

Name	Direction	Description
SP_DIN	Input	Serial Data In pin
SP_DOUT	Input/Output	Serial Data Output pin. Switches to input when used in double-data-rate mode
SP_CLK	Output	SPI Clock output used to drive the SPCLK pin.
SP_CS#	Output	SPI chip select

TABLE 37-2: INTERNAL SIGNAL DESCRIPTION

Name	Direction	Description
SPI_TDMA_REQ	Output	DMA Request control for GP-SPI Controller Transmit Channel
SPI_RDMA_REQ	Output	DMA Request control for GP-SPI Controller Receive Channel

37.6 Host Interface

The registers defined for the General Purpose Serial Peripheral Interface are accessible by the various hosts as indicated in Section 37.12, "EC-Only/Runtime Registers".

37.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

37.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

37.7.2 CLOCK INPUTS

Name	Description
48MHz	This is a clock source for the SPI clock generator.
2MHz	This is a clock source for the SPI clock generator. It is derived from the 48MHz clock domain.

37.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

37.8 Interrupts

This section defines the Interrupt Sources generated from this block.

TABLE 37-3: EC INTERRUPTS

Source	Description
TXBE_STS	Transmit buffer empty status (TXBE), in the SPI Status Register, sent as an interrupt request to the Interrupt Aggregator.
RXBF_STS	Receive buffer full status (RXBF), in the SPI Status Register, sent as an interrupt request to the Interrupt Aggregator.

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These status bits are also connected respectively to the DMA Controller's SPI Controller TX and RX requests signals.

37.9 Low Power Modes

The GP-SPI Interface may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

37.10 Description

The Serial Peripheral Interface (SPI) block is a master SPI block used to communicate with external SPI devices. The SPI master is responsible for generating the SPI clock and is designed to operate in Full Duplex, Half Duplex, and Dual modes of operation. The clock source may be programmed to operated at various clock speeds. The data is transmitted serially via 8-bit transmit and receive shift registers. Communication with SPI peripherals that require transactions of varying lengths can be achieved with multiple 8-bit cycles.

This block has many configuration options: The data may be transmitted and received either MSbit or LSbit first; The SPI Clock Polarity may be either active high or active low; Data may be sampled or presented on either the rising of falling edge of the clock (referred to as the transmit clock phase); and the SPI_CLK SPDOUT frequency may be programmed to a range of values as illustrated in Table 37-4, "SPI_CLK Frequencies". In addition to these many programmable options, this feature has several status bits that may be enabled to notify the host that data is being transmitted or received.

37.10.1 INITIATING AN SPI TRANSACTION

All SPI transactions are initiated by a write to the TX_DATA register. No read or write operations can be initiated until the Transmit Buffer is Empty, which is indicated by a one in the TXBE status bit.

If the transaction is a write operation, the host writes the TX_DATA register with the value to be transmitted. Writing the TX_DATA register causes the TXBE status bit to be cleared, indicating that the value has been registered. If empty, the SPI Core loads this TX_DATA value into an 8-bit transmit shift register and begins shifting the data out. Loading the value into the shift register causes the TXBE status bit to be asserted, indicating to software that the next byte can be written to the TX_DATA register.

If the transaction is a read operation, the host initiates a write to the TX_DATA register in the same manner as the write operation. Unlike the transmit command, the host must clear the RXBF status bit by reading the RX_DATA register before writing the TX_DATA register. This time, the host will be required to poll the RXBF status bit to determine when the value in the RX_DATA register is valid.

Note 1: If the SPI interface is configured for Half Duplex mode, the host must still write a dummy byte to receive data.

2: Since RX and TX transactions are executed by the same sequence of transactions, data is always shifted into the RX_DATA register. Therefore, every write operation causes data to be latched into the RX_DATA register and the RXBF bit is set. This status bit should be cleared before initiating subsequent transactions. The host utilizing this SPI core to transmit SPI Data must discard the unwanted receive bytes.

3: The length and order of data sent to and received from a SPI peripheral varies between peripheral devices. The SPI must be properly configured and software-controlled to communicate with each device and determine whether SPIRD data is valid slave data.

The following diagrams show sample single byte and multi-byte SPI Transactions.

FIGURE 37-2: SINGLE BYTE SPI TX/RX TRANSACTIONS (FULL DUPLEX MODE)

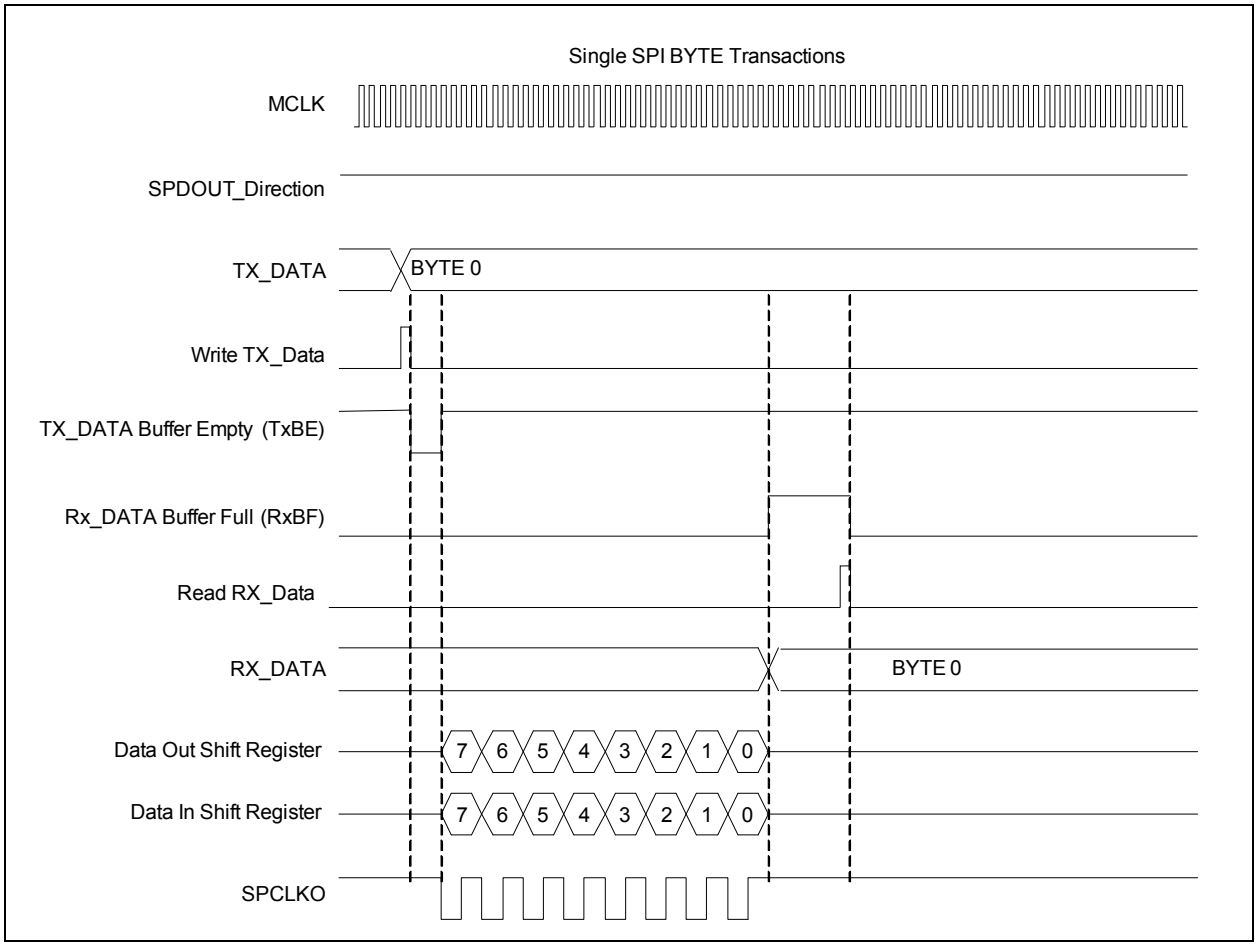

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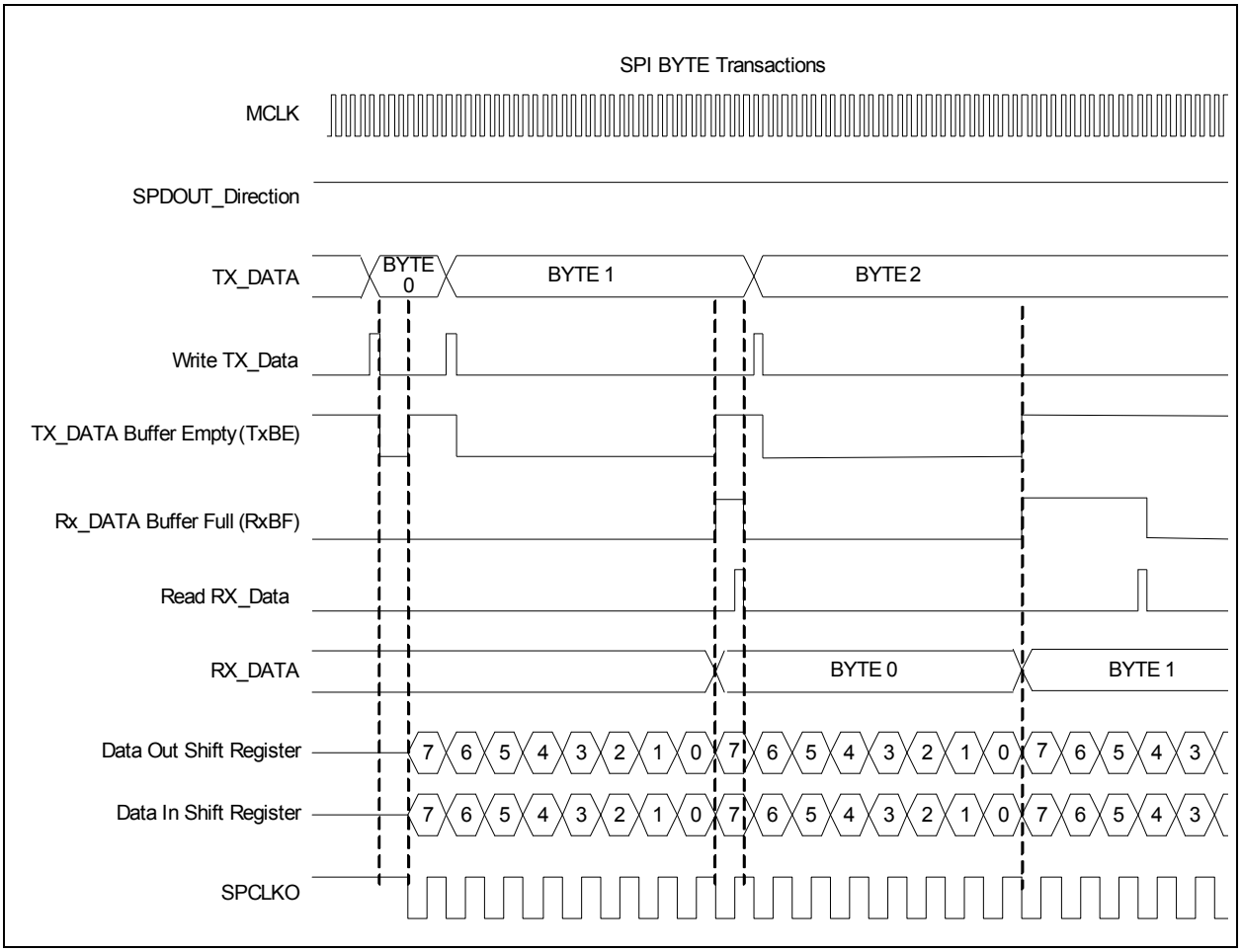
FIGURE 37-3: MULTI-BYTE SPI TX/RX TRANSACTIONS (FULL DUPLEX MODE)



The data may be configured to be transmitted MSB or LSB first. This is configured by the LSBF bit in the SPI Control Register. The transmit data is shifted out on the edge as selected by the TCLKPH bit in the SPI Clock Control Register. All received data can be sampled on a rising or falling SPI_CLK edge using the RCLKPH bit in the SPI Clock Control Register This clock setting must be identical to the clocking requirements of the current SPI slave.

Note:	Common peripheral devices require a chip select signal to be asserted during a transaction. Chip selects for SPI devices may be controlled by MEC170x GPIO pins.

There are three types of transactions that can be implemented for transmitting and receiving the SPI data. They are Full Duplex, Half Duplex, and Dual Mode. These modes are define in Section 37.10.3, "Types of SPI Transactions".

37.10.2 DMA MODE

Transmit and receive operations can use a DMA channel. Note that only one DMA channel may be enabled at a time. Setting up the DMA Controller involves specifying the device (Flash GP-SPI), direction (transmit/receive), and the start and end addresses of the DMA buffers in the closely couple memory. Please refer to the DMA Controller chapter for register programming information.

SPI transmit / DMA write: the GP-SPI block's transmit empty (TxBE) status signal is used as a write request to the DMA controller, which then fetches a byte from the DMA transmit buffer and writes it to the GP-SPI's SPI TX Data Register (SPITD). As content of the latter is transferred to the internal Tx shift register from which data is shifted out onto the SPI

bus bit by bit, the Tx Empty signal is again asserted, triggering the DMA fetch-and-write cycle. The process continues until the end of the DMA buffer is reached - the DMA controller stops responding to an active Tx Empty until the buffer's address registers are reprogrammed.

SPI receive / DMA read: the AUTO_READ bit in the SPI Control Register must be set. The driver first writes (dummy data) to the SPI TX Data Register (SPITD) to initiate the toggling of the SPI clock, enabling data to be shifted in. After one byte is received, the Rx Full (RxBF) status signal, used as a read request to the DMA controller, is asserted. The DMA controller then reads the received byte from the GP-SPI's SPI RX Data Register (SPIRD) and stores it in the DMA receive buffer. With AUTO_READ set, this read clears both the RxBF and TxBE. Clearing TxBE causes (dummy) data from the SPI TX Data Register (SPITD) to be transferred to the internal shift register, mimicking the effect of the aforementioned write to the SPI TX Data Register (SPITD) by the driver. SPI clock is toggled again to shift in the second read byte. This process continues until the end of the DMA buffer is reached - the DMA controller stops responding to an active Tx Empty until the buffer's address registers are reprogrammed.

37.10.3 TYPES OF SPI TRANSACTIONS

The GP-SPI controller can be configured to operate in three modes: Full Duplex, Half Duplex, and Dual Mode.

37.10.3.1 Full Duplex

In Full Duplex Mode, serial data is transmitted and received simultaneously by the SPI master over the SPDOUT and SPDIN pins. To enable Full Duplex Mode clear SPDIN Select.

When a transaction is completed in the full-duplex mode, the RX_DATA shift register always contains received data (valid or not) from the last transaction.

37.10.3.2 Half Duplex

In Half Duplex Mode, serial data is transmitted and received sequentially over a single data line (referred to as the SPDOUT pin). To enable Half Duplex Mode set SPDIN Select to 01b. The direction of the SPDOUT signal is determined by the BIOEN bit.

- To transmit data in half duplex mode set the BIOEN bit before writing the TX_DATA register.
- To receive data in half duplex mode clear the BIOEN bit before writing the TX_DATA register with a dummy byte.

Note:	The Software driver must properly drive the BIOEN bit and store received data depending on the transaction format of the specific slave device.

37.10.3.3 Dual Mode of Operation

In Dual Mode, serial data is transmitted sequentially from the SPDOUT pin and received in by the SPI master from the SPDOUT and SPDIN pins. This essentially doubles the received data rate and is often available in SPI Flash devices. To enable Dual Mode of operation the SPI core must be configured to receive data in path on the SPDIN1 and SPDIN2 inputs via SPDIN Select. The BIOEN bit determines if the SPI core is transmitting or receiving. The setting of this bit determines the direction of the SPDOUT signal. The SPDIN Select bits are configuration bits that remain static for the duration of a dual read command. The BIOEN bit must be toggled to indicate when the SPI core is transmitting and receiving.

- To transmit data in dual mode set the BIOEN bit before writing the TX_DATA register.
- To receive data in dual mode clear the BIOEN bit before writing the TX_DATA register with a dummy byte. The even bits (0,2,4,and 6) are received on the SPDOUT pin and the odd bits (1,3,5,and 7) are received on the SPDIN pin. The hardware assembles these received bits into a single byte and loads them into the RX_DATA register accordingly.

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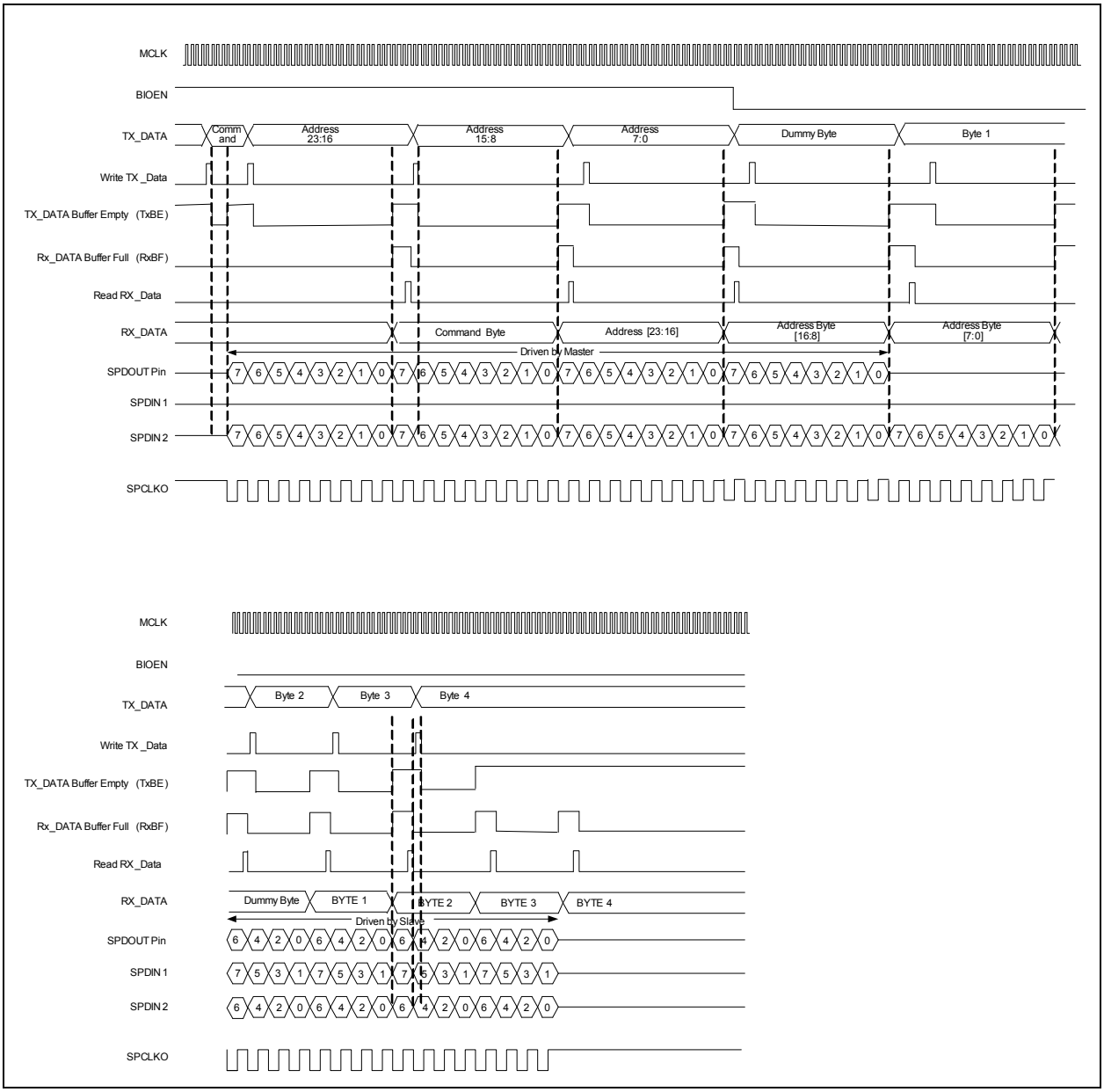
The following diagram illustrates a Dual Fast Read Command that is supported by some SPI Flash devices.

FIGURE 37-4: DUAL FAST READ FLASH COMMAND



Note:	When the SPI core is used for flash commands, like the Dual Read command, the host discards the bytes received during the command, address, and dummy byte portions of the transaction.

37.10.4 HOW BIOEN BIT CONTROLS DIRECTION OF SPDOUT BUFFER

When the SPI is configured for Half Duplex mode or Dual Mode the SPDOUT pin operates as a bi-directional signal. The BIOEN bit is used to determine the direction of the SPDOUT buffer when a byte is transmitted. Internally, the BIOEN bit is sampled to control the direction of the SPDOUT buffer when the TX_DATA value is loaded into the transmit shift register. The direction of the buffer is never changed while a byte is being transmitted.

Since the TX_DATA register may be written while a byte is being shifted out on the SPDOUT pin, the BIOEN bit does not directly control the direction of the SPDOUT buffer. An internal DIRECTION bit, which is a latched version of the BIOEN bit determines the direction of the SPDOUT buffer. The following list summarizes when the BIOEN bit is sampled.

- The DIRECTION bit is equal to the BIOEN bit when data is not being shifted out (i.e., SPI interface is idle).
- The hardware samples the BIOEN bit when it is shifting out the last bit of a byte to determine if the buffer needs to be turned around for the next byte.
- The BIOEN bit is also sampled any time the value in the TX_DATA register is loaded into the shift register to be transmitted.

If a TAR (Turn-around time) is required between transmitting and receiving bytes on the SPDOUT signal, software should allow all the bytes to be transmitted before changing the buffer to an input and then load the TX_DATA register to begin receiving bytes. If TAR greater than zero is required, software must wait for the transmission in one direction to complete before writing the TX_DATA register to start sending/receiving in the opposite direction. This allows the SPI block to operate the same as legacy Microchip SPI devices.

37.10.5 CONFIGURING THE SPI CLOCK GENERATOR

The SPI controller generates the SPI_CLK signal to the external SPI device. The frequency of the SPI_CLK signal is determined by one of two clock sources and the Preload value of the clock generator down counter. The clock generator toggles the SPI_CLK output every time the counter underflows, while data is being transmitted.

Note:	When the SPI interface is in the idle state and data is not being transmitted, the SPI_CLK signal stops in the inactive state as determined by the configuration bits.

The clock source to the down counter is determined by Bit CLKSRC. Either the main system clock or the 2MHz clock can be used to decrement the down counter in the clock generator logic.

The SPI_CLK frequency is determined by the following formula:

$$\text{SPI_CLK_FREQ} = \left(\left(\frac{1}{2} \times \text{REFERENCE_CLOCK} \right) / \text{PRELOAD} \right)$$

The REFERENCE_CLOCK frequency is selected by CLKSRC in the SPI Clock Control Register and PRELOAD is the PRELOAD field of the SPI Clock Generator Register. The frequency can be either the 48MHz clock or a 2MHz clock. When the PRELOAD value is 0, the REFERENCE_CLOCK is always the 48MHz clock and the CLKSRC bit is ignored.

Sample SPI Clock frequencies are shown in the following table:

TABLE 37-4: SPI_CLK FREQUENCIES

Clock Source	Preload	SPI_CLK Frequency
Don't Care	0	48MHz
48MHz	1	24MHz
48MHz	2	12MHz (default)
48MHz	3	6MHz
48MHz	63	381KHz
2MHz	1	1MHz
2MHz	2	500KHz
2MHz	3	333KHz
2MHz	63	15.9KHz

37.10.6 CONFIGURING SPI MODE

In practice, there are four modes of operation that define when data should be latched. These four modes are the combinations of the SPI_CLK polarity and phase.

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The output of the clock generator may be inverted to create an active high or active low clock pulse. This is used to determine the inactive state of the SPI_CLK signal and is used for determining the first edge for shifting the data. The polarity is selected by CLKPOL in the SPI Clock Control Register.

The phase of the clock is selected independently for receiving data and transmitting data. The receive phase is determine by RCLKPH and the transmit phase is determine by TCLKPH in the SPI Clock Control Register.

The following table summarizes the effect of CLKPOL, RCLKPH and TCLKPH.

TABLE 37-5: SPI DATA AND CLOCK BEHAVIOR

CLKPOL	RCLKPH	TCLKPH	Behavior
0	0	0	Inactive state is low. First edge is rising edge. Data is sampled on the rising edge. Data is transmitted on the falling edge. Data is valid before the first rising edge.
0	0	1	Inactive state is low. First edge is rising edge. Data is sampled on the rising edge. Data is transmitted on the rising edge.
0	1	0	Inactive state is low. First edge is rising edge. Data is sampled on the falling edge. Data is transmitted on the falling edge. Data is valid before the first rising edge.
0	1	1	Inactive state is low. First edge is rising edge. Data is sampled on the falling edge. Data is transmitted on the rising edge.
1	0	0	Inactive state is high. First edge is falling edge. Data is sampled on the falling edge. Data is transmitted on the rising edge. Data is valid before the first falling edge.
1	0	1	Inactive state is high. First edge is falling edge. Data is sampled on the falling edge. Data is transmitted on the falling edge.
1	1	0	Inactive state is high. First edge is falling edge. Data is sampled on the rising edge. Data is transmitted on the rising edge. Data is valid before the first falling edge.
1	1	1	Inactive state is high. First edge is falling edge. Data is sampled on the rising edge. Data is transmitted on the falling edge.

37.11 SPI Examples

37.11.1 FULL DUPLEX MODE TRANSFER EXAMPLES

37.11.1.1 Read Only

The slave device used in this example is a MAXIM MAX1080 10 bit, 8 channel ADC:

- The SPI block is activated by setting the enable bit in SPIAR - SPI Enable Register
- The SPIMODE bit is de-asserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL and TCLKPH bits are de-asserted '0', and RCLKPH is asserted '1' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- Assert CS# using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the SPITD - SPI TX_Data Register with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX_DATA byte is loaded into the shift register and the SPI master reasserts the

TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- A dummy 8 bit data value (any value) is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the first transmit bytes:
  - The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device drives '0' on the SPDIN pin to the master while it is accepting command data. This SPIRD data is ignored.
  - Once the first SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- The final SPI cycle is initiated when another dummy 8 bit data value (any value) is written to the TX_DATA register. Note that this value may be another dummy value or it can be a new 8 bit command to be sent to the ADC. The new command will be transmitted while the final data from the last command is received simultaneously. This overlap allows ADC data to be read every 16 SPCLK cycles after the initial 24 clock cycle.The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses, the second SPI cycle is complete:
  - The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is the first half of a valid 16 bit ADC value. SPIRD is read and stored.
  - Once the second SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- After 8 SPI_CLK pulses, the final SPI cycle is complete, TXBF is asserted '1', and the SPINT interrupt is asserted (if enabled). The data now contained in SPIRD - SPI RX_Data Register is the second half of a valid 16 bit ADC value. SPIRD is read and stored.
- If a command was overlapped with the received data in the final cycle, #CS should remain asserted and the SPI master will initiate another SPI cycle. If no new command was sent, #CS is released and the SPI is idle.

37.11.1.2 Read/Write

The slave device used in this example is a Fairchild NS25C640 FM25C640 64K Bit Serial EEPROM. The following subsections describe the read and write sequences.

Read

- The SPI block is activated by setting the enable bit in SPIAR - SPI Enable Register
- The SPIMODE bit is de-asserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are de-asserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- Assert CS# low using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the SPITD - SPI TX_Data Register with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.

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- Next, EEPROM address A15-A8 is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the first transmit byte (Command Byte transmitted):
  - The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIRD data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

  - Once the first SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (EEPROM address A15-A8) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock. Note: The particular slave device ignores address A15-A13.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, EEPROM address A7-A0 is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the second transmit byte (Address Byte (MSB) transmitted):
  - EEPROM address A15-A8 has been transmitted to the slave completing the second SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit address data to the slave.
  - Once the second SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (EEPROM address A7-A0) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, a dummy byte is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses, the third SPI cycle is complete (Address Byte (LSB) transmitted):
  - EEPROM address A7-A0 has been transmitted to the slave completing the third SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit address data to the slave.
  - Once the third SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (dummy byte) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- If only one receive byte is required, the host would not write any more value to the TX_DATA register until this transaction completes. If more than one byte of data is to be received, another dummy byte would be written to the TX_DATA register (one dummy byte per receive byte is required). The SPI master automatically clears the TXFE bit when the TX_DATA register is written, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses, the fourth SPI cycle is complete (First Data Byte received):
  - The dummy byte has been transmitted to the slave completing the fourth SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. Unlike the command and address phases, the data now contained in SPIRD - SPI RX_Data Register is the 8-bit EEPROM data since the last cycle was initiated to receive data from the slave.

- Once the fourth SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (if any) and loads it into the TX shift register. This process will be repeated until all the desired data is received.

- The host software will read and store the EEPROM data value in SPIRD - SPI RX_Data Register.
- If no more data needs to be received by the master, CS# is released and the SPI is idle. Otherwise, master continues reading the data by writing a dummy value to the TX_DATA register after every 8 SPI_CLK cycles.

Write

- The SPI block is activated by setting the enable bit in SPIAR - SPI Enable Register
- The SPIMODE bit is de-asserted '0' to enable the SPI interface in Full Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are de-asserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- Assert WR# high using a GPIO pin.
- Assert CS# low using a GPIO pin.
- Write a valid command word (as specified by the slave device) to the SPITD - SPI TX_Data Register with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, EEPROM address A15-A8 is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the first transmit byte (Command Byte transmitted):
  - The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit command data to the slave. This particular slave device tri-states the SPDIN pin to the master while it is accepting command data. This SPIRD data is ignored.

USER'S NOTE: External pull-up or pull-down is required on the SPDIN pin if it is tri-stated by the slave device.

  - Once the first SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (EEPROM address A15-A8) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock. Note: The particular slave device ignores address A15-A13.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, EEPROM address A7-A0 is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the second transmit byte (Address Byte (MSB) transmitted):
  - EEPROM address A15-A8 has been transmitted to the slave completing the second SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit address data to the slave.
  - Once the second SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (EEPROM address A7-A0) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, a data byte (D7:D0) is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.

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- After 8 SPI_CLK pulses, the third SPI cycle is complete (Address Byte (LSB) transmitted):
  - EEPROM address A7-A0 has been transmitted to the slave completing the third SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated solely to transmit address data to the slave.
  - Once the third SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (data byte D7:D0) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPCLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- If only one data byte is to be written, the host would not write any more values to the TX_DATA register until this transaction completes. If more than one byte of data is to be written, another data byte would be written to the TX_DATA register. The SPI master automatically clears the TXFE bit when the TX_DATA register is written, but does not begin shifting this data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses, the fourth SPI cycle is complete (First Data Byte transmitted):
  - The data byte has been transmitted to the slave completing the fourth SPI cycle. Once again, the RXBF bit is asserted '1' and the SPINT interrupt is asserted, if enabled. Like the command and address phases, the data now contained in SPIRD - SPI RX_Data Register is invalid since the last cycle was initiated to transmit data to the slave.
  - Once the fourth SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (if any) and loads it into the TX shift register. This process will be repeated until all the desired data is transmitted.
- If no more data needs to be transmitted by the master, CS# and WR# are released and the SPI is idle.

37.11.2 HALF DUPLEX (BIDIRECTIONAL MODE) TRANSFER EXAMPLE

The slave device used in this example is a National LM74 12 bit (plus sign) temperature sensor.

- The SPI block is activated by setting the enable bit in SPIAR - SPI Enable Register
- The SPIMODE bit is asserted '1' to enable the SPI interface in Half Duplex mode.
- The CLKPOL, TCLKPH and RCLKPH bits are de-asserted '0' to match the clocking requirements of the slave device.
- The LSBF bit is de-asserted '0' to indicate that the slave expects data in MSB-first order.
- BIOEN is asserted '0' to indicate that the first data in the transaction is to be received from the slave.
- Assert CS# using a GPIO pin.

//Receive 16-bit Temperature Reading

- Write a dummy command byte (as specified by the slave device) to the SPITD - SPI TX_Data Register with TXFE asserted '1'. The SPI master automatically clears the TXFE bit indicating the byte has been put in the TX buffer. If the shift register is empty the TX_DATA byte is loaded into the shift register and the SPI master reasserts the TXFE bit. Once the data is in the shift register the SPI master begins shifting the data value onto the SPDOUT pin and drives the SPI_CLK pin. This data is lost because the output buffer is disabled. Data on the SPDIN pin is sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, another dummy byte is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the dummy data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the first receive byte
  - The first SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is the first half of the 16 bit word containing the temperature data.
  - Once the first SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (dummy byte 2) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock.

- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.

//Transmit next reading command

- BIOEN is asserted '1' to indicate that data will now be driven by the master.
- Next, a command byte is written to the TX_DATA register. This value is the first half of a 16 bit command to be sent to temperature sensor peripheral. The SPI master automatically clears the TXFE bit, but does not begin shifting the command data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty. This data will be transmitted because the output buffer is enabled. Data on the SPDIN pin is sampled on each clock.
- After 8 SPI_CLK pulses from the second receive byte:
  - The second SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is the second half of the 16 bit word containing the temperature data.
  - Once the first SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (command byte 1) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Next, the second command byte is written to the TX_DATA register. The SPI master automatically clears the TXFE bit, but does not begin shifting the command data value onto the SPDOUT pin. This byte will remain in the TX_DATA register until the TX shift register is empty.
- After 8 SPI_CLK pulses from the first transmit byte:
  - The third SPI cycle is complete, RXBF bit is asserted '1', and the SPINT interrupt is asserted, if enabled. The data now contained in SPIRD - SPI RX_Data Register is invalid, since this command was used to transmit the first command byte to the SPI slave.
  - Once the first SPI cycle is completed, the SPI master takes the pending data in the TX_DATA register (command byte 2) and loads it into the TX shift register. Loading the shift register automatically asserts the TXFE bit, begins shifting the dummy data value onto the SPDOUT pin, and drives the SPI_CLK pin. Data on the SPDIN pin is also sampled on each clock.
- Once the TXFE bit is asserted the SPI Master is ready to transmit or receive its next byte. Before writing the next TX_DATA value, software must clear the RXBF status bit by reading the SPIRD - SPI RX_Data Register.
- Since no more data needs to be transmitted, the host software will wait for the RXBF status bit to be asserted indicating the second command byte was transmitted successfully.
- CS# is de-asserted.

37.12 EC-Only/Runtime Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the General Purpose Serial Peripheral Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 37-6: REGISTER SUMMARY

Offset	Register Name
0h	SPI Enable Register
4h	SPI Control Register
8h	SPI Status Register
Ch	SPI TX_Data Register
10h	SPI RX_Data Register
14h	SPI Clock Control Register
18h	SPI Clock Generator Register

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37.12.1 SPI ENABLE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	ENABLE 1=Enabled. The device is fully operational 0=Disabled. Clocks are gated to conserve power and the SPDOUT and SPI_CLK signals are set to their inactive state	R/W	0h	RESET_SYS

37.12.2 SPI CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6	CE SPI Chip Select Enable. 1=SPI_CS# output signal is asserted, i.e., driven to logic ‘0’ 0=SPI_CS# output signal is deasserted, i.e., driven to logic ‘1’	R/W	0h	RESET_SYS
5	AUTO_READ Auto Read Enable. 1=A read of the SPI RX_DATA Register will clear both the RXBF status bit and the TXBE status bit 0=A read of the SPI RX_DATA Register will clear the RXBF status bit. The TXBE status bit will not be modified	R/W	0h	RESET_SYS
4	SOFT_RESET Soft Reset is a self-clearing bit. Writing zero to this bit has no effect. Writing a one to this bit resets the entire SPI Interface, including all counters and registers back to their initial state.	R/W	0h	RESET_SYS
3:2	SPDIN_SELECT The SPDIN Select which SPI input signals are enabled when the BIOEN bit is configured as an input. 1xb=SPDIN1 and SPDIN2. Select this option for Dual Mode 01b=SPDIN2 only. Select this option for Half Duplex 00b=SPDIN1 only. Select this option for Full Duplex	R/W	0h	RESET_SYS

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	BIOEN Bidirectional Output Enable control. When the SPI is configured for Half Duplex mode or Dual Mode the SPDOUT pin operates as a bi-directional signal. The BIOEN bit is used by the internal DIRECTION bit to control the direction of the SPDOUT buffers. The direction of the buffer is never changed while a byte is being transmitted. 1=The SPDOUT_Direction signal configures the SPDOUT signal as an output. 0=The SPDOUT_Direction signal configures the SPDOUT signal as an input. See Section 37.10.4, "How BIOEN Bit Controls Direction of SPD-OUT Buffer" for details on the use of BIOEN.	R/W	1h	RESET_SYS
0	LSBF Least Significant Bit First 1=The data is transferred in LSB-first order. 0=The data is transferred in MSB-first order. (default)	R/W	0h	RESET_SYS

37.12.3 SPI STATUS REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	-
2	ACTIVE	R	0h	RESET_SYS
1	RXBF Receive Data Buffer Full status. When this bit is ‘1’ the Rx_Data buffer is full. Reading the SPI RX_Data Register clears this bit. This signal may be used to generate a SPI_RX interrupt to the EC. 1=RX_Data buffer is full 0=RX_Data buffer is not full	R	0h	RESET_SYS
0	TXBE Transmit Data Buffer Empty status. When this bit is ‘1’ the Tx_Data buffer is empty. Writing the SPI TX_Data Register clears this bit. This signal may be used to generate a SPI_TX interrupt to the EC. 1=TX_Data buffer is empty 0=TX_Data buffer is not empty	R	1h	RESET_SYS

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37.12.4 SPI TX_DATA REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	TX_DATA A write to this register when the Tx_Data buffer is empty (TXBE in the SPI Status Register is '1') initiates a SPI transaction. The byte written to this register will be loaded into the shift register and the TXBE flag will be asserted. This indicates that the next byte can be written into the TX_DATA register. This byte will remain in the TX_-DATA register until the SPI core has finished shifting out the previ-ous byte. Once the shift register is empty, the hardware will load the pending byte into the shift register and once again assert the TxBE bit. The TX_DATA register must not be written when the TXBE bit is zero. Writing this register may overwrite the transmit data before it is loaded into the shift register.	R/W	0h	RESET_SYS

37.12.5 SPI RX_DATA REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	RX_DATA This register is used to read the value returned by the external SPI device. At the end of a byte transfer the RX_DATA register contains serial input data (valid or not) from the last transaction and the RXBF bit is set to one. This status bit indicates that the RX_DATA register has been loaded with a the serial input data. The RX_DATA register should not be read before the RXBF bit is set. The RX_DATA register must be read, clearing the RXBF status bit before writing the TX_DATA register. The data in the receive shift register is only loaded into the RX_DATA register when this bit is cleared. If a data byte is pending in the receive shift register the value will be loaded immediately into the RX_DATA register and the RXBF status flag will be asserted. Software should read the RX_-DATA register twice before starting a new transaction to make sure the RX_DATA buffer and shift register are both empty.	R/W	0h	RESET_SYS

37.12.6 SPI CLOCK CONTROL REGISTER

This register should not be changed during an active SPI transaction.

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:5	Reserved	R	-	-
4	CLKSRC Clock Source for the SPI Clock Generator. This bit should not be changed during a SPI transaction. When the field PRELOAD in the SPI Clock Generator Register is 0, this bit is ignored and the Clock Source is always the main system clock (the equivalent of setting this bit to '0'). 1=2MHz 0=48MHz	R/W	0h	RESET_SYS
3	Reserved	R	-	-
2	CLKPOL SPI Clock Polarity. 1=The SPI_CLK signal is high when the interface is idle and the first clock edge is a falling edge 0=The SPI_CLK is low when the interface is idle and the first clock edge is a rising edge	R/W	0h	RESET_SYS
1	RCLKPH Receive Clock Phase, the SPI_CLK edge on which the master will sample data. The receive clock phase is not affected by the SPI Clock Polarity. 1=Valid data on SPDIN signal is expected after the first SPI_CLK edge. This data is sampled on the second and following even SPI_CLK edges (i.e., sample data on falling edge) 0=Valid data is expected on the SPDIN signal on the first SPI_CLK edge. This data is sampled on the first and following odd SPI_-CLK edges (i.e., sample data on rising edge)	R/W	1h	RESET_SYS
0	TCLKPH Transmit Clock Phase, the SPCLK edge on which the master will clock data out. The transmit clock phase is not affected by the SPI Clock Polarity. 1=Valid data is clocked out on the first SPI_CLK edge on SPDOUT signal. The slave device should sample this data on the second and following even SPI_CLK edges (i.e., sample data on falling edge) 0=Valid data is clocked out on the SPDOUT signal prior to the first SPI_CLK edge. The slave device should sample this data on the first and following odd SPI_CLK edges (i.e., sample data on rising edge)	R/W	0h	RESET_SYS

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37.12.7 SPI CLOCK GENERATOR REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
5:0	PRELOAD SPI Clock Generator Preload value.	R/W	2h	RESET_SYS

38.0 QUAD SPI MASTER CONTROLLER

38.1 Overview

The Quad SPI Master Controller may be used to communicate with various peripheral devices that use a Serial Peripheral Interface, such as EEPROMS, DACs and ADCs. The controller can be configured to support advanced SPI Flash devices with multi-phase access protocols. Data can be transfered in Half Duplex, Single Data Rate, Dual Data Rate and Quad Data Rate modes. In all modes and all SPI clock speeds, the controller supports back-to-back reads and writes without clock stretching if internal bandwidth permits.

38.2 References

No references have been cited for this feature.

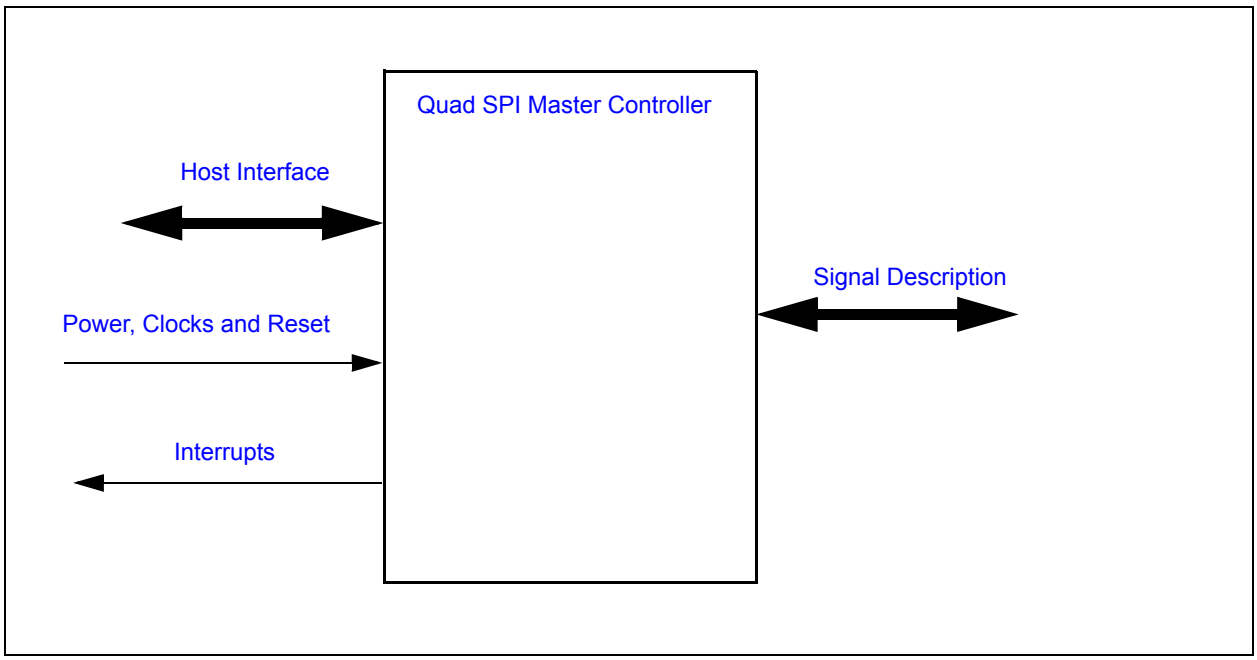
38.3 Terminology

No terminology for this block.

38.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 38-1: I/O DIAGRAM OF BLOCK



38.5 Signal Description

TABLE 38-1: EXTERNAL SIGNAL DESCRIPTION

Name	Direction	Description
SPI_CLK	Output	SPI Clock output used to drive the SPCLK pin.
SPI_CS#	Output	SPI chip select
SPI_IO0	Input/Output	SPI Data pin 0. Also used as SPI_MOSI, Master-Out/Slave-In when the interface is used in Single wire mode
SPI_IO1	Input/Output	SPI Data pin 1. Also used as SPI_MISO, Master-In/Slave-Out when the interface is used in Single wire mode

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TABLE 38-1: EXTERNAL SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
SPI_IO2	Input/Output	SPI Data pin 2 when the SPI interface is used in Quad Mode. Also can be used by firmware as WP.
SPI_IO3	Input/Output	SPI Data pin 3 when the SPI interface is used in Quad Mode. Also can be used by firmware as HOLD.

38.6 Host Interface

The registers defined for the General Purpose Serial Peripheral Interface are accessible by the various hosts as indicated in Section 38.11, "EC Registers".

38.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

38.7.1 POWER

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

38.7.2 CLOCKS

Name	Description
48MHz	This is a clock source for the SPI clock generator.

38.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.QMSPI Status Register
RESET	This reset is generated if either the RESET_SYS is asserted or the SOFT_RESET is asserted.

38.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
QMSPI_INT	Interrupt generated by the Quad SPI Master Controller. Events that may cause the interrupt to be asserted are stored in the QMSPI Status Register.

38.9 Low Power Modes

The Quad SPI Master Controller is always in its lowest power state unless a transaction is in process. A transaction is in process between the time the START bit is written with a ‘1’ and the TRANSFER_DONE bit is set by hardware to ‘1’.

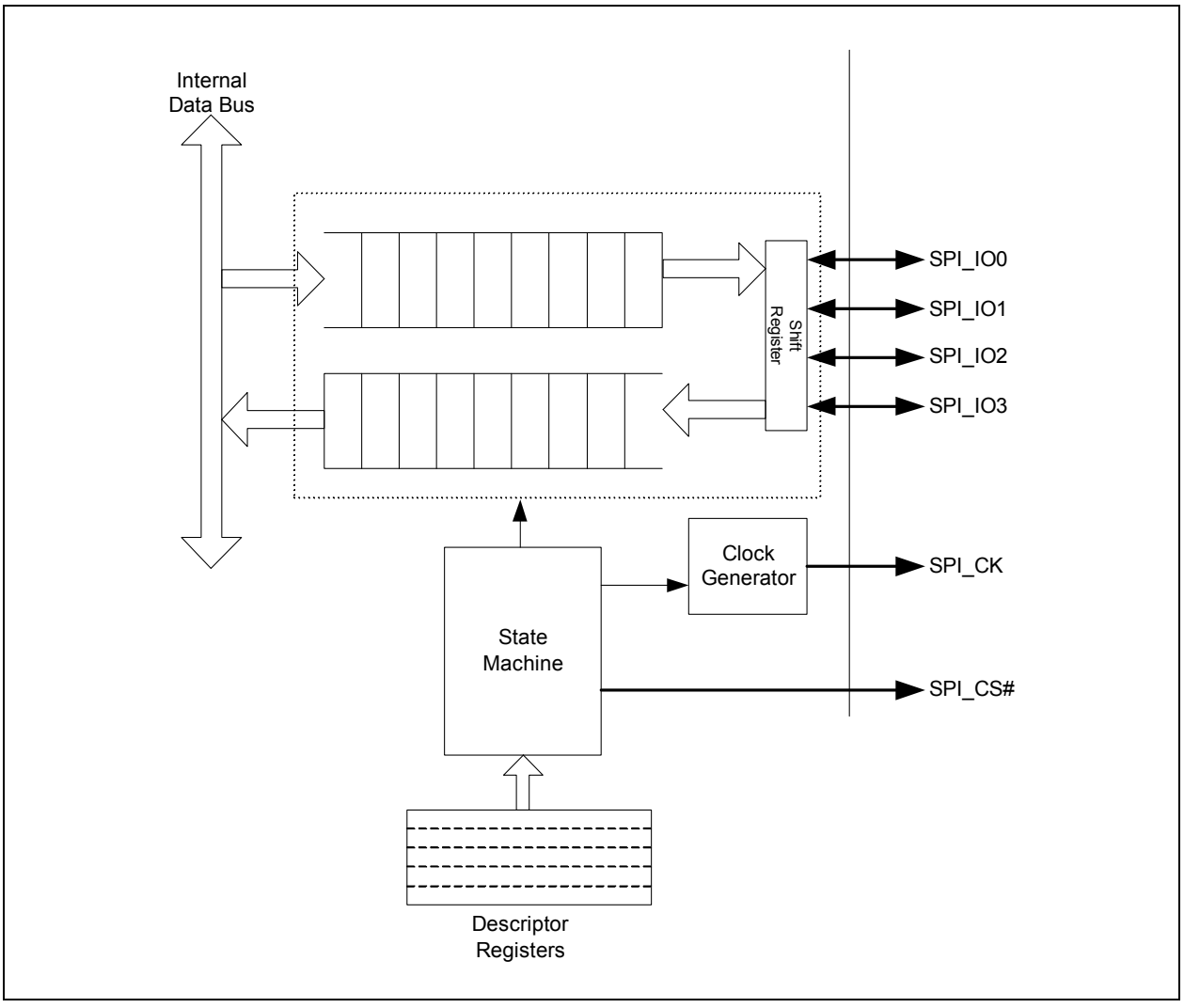
If the QMSPI SLEEP_ENABLE input is asserted, writes to the START bit are ignored and the Quad SPI Master Controller will remain in its lowest power state.

38.10 Description

- Support for multiple SPI pin configurations
  - Single wire half duplex
  - Two wire full duplex

  - Two wire double data rate
  - Four wire quad data rate
- Separate FIFO buffers for Receive and Transmit
  - 8 byte FIFO depth in each FIFO
  - Each FIFO can be 1 byte, 2 bytes or 4 bytes wide
- Support for all four SPI clock formats
- Programmable SPI Clock generator, with clock polarity and phase controls
- Separate DMA support for Receive and Transmit data transfers
- Configurable interrupts, for errors, individual bytes, or entire transactions
- Descriptor Mode, in which a set of five descriptor registers can configure the controller to autonomously perform multi-phase SPI data transfers
- Capable of wire speed transfers in all SPI modes and all configurable SPI clock rates (internal bus contention may cause clock stretching)

FIGURE 38-2: QUAD MASTER SPI BLOCK DIAGRAM



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38.10.1 SPI CONFIGURATIONS MODES

- Half Duplex. All SPI data transfers take place on a single wire, SPI_IO0
- Full Duplex. This is the legacy SPI configuration, where all SPI data is transfered one bit at a time and data from the SPI Master to the SPI Slave takes place on SPI_MOSI (SPI_IO0) and at the same time data from the SPI Slave to the SPI Master takes place on SPI_MISO (SPI_IO1)
- Dual Data Rate. Data transfers between the SPI Master and the SPI Slave take place two bits at a time, using SPI_IO0 and SPI_IO1
- Quad Data Rate. Data transfers between the SPI Master and the SPI Slave take place four bits at a time, using all four SPI data wires, SPI_IO0, SPI_IO1, SPI_IO2 and SPI_IO3

38.10.2 SPI CONTROLLER MODES

- Manual. In this mode, firmware control all SPI data transfers byte at a time
- DMA. Firmware configures the SPI Master controller for characteristics like data width but the transfer of data between the FIFO buffers in the SPI controller and memory is controlled by the DMA controller. DMA transfers can take place from the Slave to the Master, from the Master to the Slave, or in both directions simultaneously
- Descriptor. Descriptor Mode extends the SPI Controller so that firmware can configure a multi-phase SPI transfer, in which each phase may have a different SPI bus width, a different direction, and a different length. For example, firmware can configure the controller so that a read from an advanced SPI Flash, which consists of a command phase, an address phase, a dummy cycle phase and the read phase, can take place as a single operation, with a single interrupt to firmware when the entire transfer is completed

38.10.3 SPI CLOCK

The SPI output clock is derived from the 48MHz, divided by a value programmed in the CLOCK_DIVIDE field of the QMSPI Mode Register. Sample frequencies are shown in the following table:

TABLE 38-2: EXAMPLE SPI FREQUENCIES

CLOCK_DIVIDE	SPI Clock Frequency
0	187.5 KHz
1	48 MHz
2	24 MHz
3	16 MHz
6	8 MHz
48	1 MHz
128	375 KHz
255	188.25 KHz

38.10.4 ERROR CONDITIONS

The Quad SPI Master Controller can detect some illegal configurations. When these errors are detected, an error is signaled via the PROGRAMMING_ERROR status bit. This bit is asserted when any of the following errors are detected:

- Both Receive and the Transmit transfers are enabled when the SPI Master Controller is configured for Dual Data Rate or Quad Data Rate
- Both Pull-up and Pull-down resistors are enabled on either the Receive data pins or the Transmit data pins
- The transfer length is programmed in bit mode, but the total number of bits is not a multiple of 2 (when the controller is configured for Dual Data Rate) or 4 (when the controller is configured for Quad Data Rate)
- Both the STOP bit and the START bits in the QMSPI Execute Register are set to ‘1’ simultaneously

38.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Quad SPI Master Controller Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 38-3: REGISTER SUMMARY

Offset	Register Name
0h	QMSPI Mode Register
4h	QMSPI Control Register
8h	QMSPI Execute Register
Ch	QMSPI Interface Control Register
10h	QMSPI Status Register
14h	QMSPI Buffer Count Status Register
18h	QMSPI Interrupt Enable Register
1Ch	QMSPI Buffer Count Trigger Register
20h	QMSPI Transmit Buffer Register
24h	QMSPI Receive Buffer Register
30h	QMSPI Description Buffer 0 Register
34h	QMSPI Description Buffer 1 Register
38h	QMSPI Description Buffer 2 Register
3Ch	QMSPI Description Buffer 3 Register
40h	QMSPI Description Buffer 4 Register

38.11.1 QMSPI MODE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:24	Reserved	R	-	-
24:16	CLOCK_DIVIDE The SPI clock divide in number of system clocks. A value of 1 divides the master clock by 1, a value of 255 divides the master clock by 255. A value of 0 divides the master clock by 256. See Table 38-2, "Example SPI Frequencies" for examples.	R/W	0h	RESET
15:11	Reserved	R	-	-

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Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
10	CHPA_MISO If CPOL=1: 1=Data are captured on the rising edge of the SPI clock 0=Data are captured on the falling edge of the SPI clock If CPOL=0: 1=Data are captured on the falling edge of the SPI clock 0=Data are captured on the rising edge of the SPI clock Application Notes: Common SPI Mode configurations: Common SPI Modes require the CHPA_MISO and CHPA_MOSI programmed to the same value. E.g., - Mode 0: CPOL=0; CHPA_MISO=0; CHPA_MOSI=0 - Mode 3: CPOL=1; CHPA_MISO=1; CHPA_MOSI=1 Alternative SPI Mode configurations When configured for quad mode, applications operating at 48MHz may find it difficult to meet the minimum setup timing using the default Mode 0. It is recommended to configure the Master to sample and change data on the same edge when operating at 48MHz as shown in these examples. E.g, - Mode 0: CPOL=0; CHPA_MISO=1; CHPA_MOSI=0 - Mode 3: CPOL=1; CHPA_MISO=0; CHPA_MOSI=1	R/W	0h	RESET
9	CHPA_MOSI If CPOL=1: 1=Data changes on the falling edge of the SPI clock 0=Data changes on the rising edge of the SPI clock If CPOL=0: 1=Data changes on the rising edge of the SPI clock 0=Data changes on the falling edge of the SPI clock	R/W	0h	RESET
8	CPOL Polarity of the SPI clock line when there are no transactions in process. 1=SPI Clock starts High 0=SPI Clock starts Low	R/W	0h	RESET
7:2	Reserved	R	-	-
1	SOFT_RESET Writing this bit with a ‘1’ will reset the Quad SPI block. It is self-clearing.	W	0h	RESET_SYS
0	ACTIVATE 1=Enabled. The block is fully operational 0=Disabled. Clocks are gated to conserve power and the output signals are set to their inactive state	R/W	0h	RESET

38.11.2 QMSPI CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:17	TRANSFER_LENGTH The length of the SPI transfer. The count is in bytes or bits, depending on the value of TRANSFER_LENGTH_BITS. A value of '0' means an infinite length transfer.	R/W	0h	RESET
16	DESCRIPTION_BUFFER_ENABLE This enables the Description Buffers to be used. 1=Description Buffers in use. The first buffer is defined in DESCRIPTION_BUFFER_POINTER 0=Description Buffers disabled	R/W	0h	RESET
15:12	DESCRIPTION_BUFFER_POINTER This field selects the first buffer used if Description Buffers are enabled.	R/W	0h	RESET
11:10	TRANSFER_UNITS 3=TRANSFER_LENGTH defined in units of 16-byte segments 2=TRANSFER_LENGTH defined in units of 4-byte segments 1=TRANSFER_LENGTH defined in units of bytes 0=TRANSFER_LENGTH defined in units of bits	R/W	0h	RESET
9	CLOSE_TRANSFER_ENABLE This selects what action is taken at the end of a transfer. When the transaction closes, the Chip Select de-asserts, the SPI interface returns to IDLE and the DMA interface terminates When Description Buffers are in use this bit must be set only on the Last Buffer. 1=The transaction is terminated 0=The transaction is not terminated	R/W	1h	RESET
8:7	RX_DMA_ENABLE This bit enables DMA support for Receive Transfer. If enabled, DMA will be requested to empty the FIFO until either the interface reaches TRANSFER_LENGTH or the DMA sends a termination request. The size defined here must match DMA programmed access size. 1=DMA is enabled.and set to 1 Byte 2=DMA is enabled and set to 2 Bytes 3=DMA is enabled and set to 4 Bytes 0=DMA is disabled. All data in the Receive Buffer must be emptied by firmware	R/W	0h	RESET
6	RX_TRANSFER_ENABLE This bit enables the receive function of the SPI interface. 1=Receive is enabled. Data received from the SPI Slave is stored in the Receive Buffer 0=Receive is disabled	R/W	0h	RESET

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Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
5:4	TX_DMA_ENABLE This bit enables DMA support for Transmit Transfer. If enabled, DMA will be requested to fill the FIFO until either the interface reaches TRANSFER_LENGTH or the DMA sends a termination request. The size defined here must match DMA programmed access size. 1=DMA is enabled.and set to 1 Byte 2=DMA is enabled and set to 2 Bytes 3=DMA is enabled and set to 4 Bytes 0=DMA is disabled. All data in the Transmit Buffer must be emptied by firmware	R/W	0h	RESET
3:2	TX_TRANSFER_ENABLE This field bit selects the transmit function of the SPI interface. 3=Transmit Enabled in 1 Mode. The MOSI or IO Bus will send out only 1's. The Transmit Buffer will not be used 2=Transmit Enabled in 0 Mode. The MOSI or IO Bus will send out only 0's. The Transmit Buffer will not be used. 1=Transmit Enabled. Data will be fetched from the Transmit Buffer and sent out on the MOSI or IO Bus. 0=Transmit is Disabled. Not data is sent. This will cause the MOSI be to be undriven, or the IO bus to be undriven if Receive is also disabled.	R/W	0h	RESET
1:0	INTERFACE_MODE This field sets the transmission mode. If this field is set for Dual Mode or Quad Mode then either TX_TRANSFER_ENABLE or RX_TRANSFER_ENABLE **must** be 0. 3=Reserved 2=Quad Mode 1=Dual Mode 0=Single/Duplex Mode	R/W	0h	RESET

38.11.3 QMSPI EXECUTE REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	-
2	CLEAR_DATA_BUFFER Writing a ‘1’ to this bit will clear out the Transmit and Receive FIFOs. Any data stored in the FIFOs is discarded and all count fields are reset. Writing a ‘0’ to this bit has no effect. This bit is self-clearing.	W	0h	RESET
1	STOP Writing a ‘1’ to this bit will stop any transfer in progress at the next byte boundary. Writing a ‘0’ to this bit has no effect. This bit is self-clearing. This bit must not be set to ‘1’ if the field START in this register is set to ‘1’.	W	0h	RESET

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	START Writing a '1' to this bit will start the SPI transfer. Writing a '0' to this bit has no effect. This bit is self-clearing. This bit must not be set to '1' if the field STOP in this register is set to '1'.	W	1h	RESET

38.11.4 QMSPI INTERFACE CONTROL REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7	PULLUP_ON_NOT_DRIVEN 1=Enable pull-up resistors on Transmit pins while the pins are not driven 0=No pull-up resistors enabled ion Transmit pins	R/W	0h	RESET
6	PULLDOWN_ON_NOT_DRIVEN 1=Enable pull-down resistors on Transmit pins while the pins are not driven 0=No pull-down resistors enabled ion Transmit pins	R/W	0h	RESET
5	PULLUP_ON_NOT_SELECTED 1=Enable pull-up resistors on Receive pins while the SPI Chip Select signal is not asserted 0=No pull-up resistors enabled on Receive pins	R/W	1h	RESET
4	PULLDOWN_ON_NOT_SELECTED 1=Enable pull-down resistors on Receive pins while the SPI Chip Select signal is not asserted 0=No pull-down resistors enabled on Receive pins	R/W	0h	RESET
3	HOLD_OUT_ENABLE 1=HOLD SPI Output Port is driven 0=HOLD SPI Output Port is not driven	R/W	0h	RESET
2	HOLD_OUT_VALUE This bit sets the value on the HOLD SPI Output Port if it is driven. 1=HOLD is driven to 1 0=HOLD is driven to 0	R/W	1h	RESET
1	WRITE_PROTECT_OUT_ENABLE 1=WRITE PROTECT SPI Output Port is driven 0=WRITE PROTECT SPI Output Port is not driven	R/W	0h	RESET

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Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	WRITE_PROTECT_OUT_VALUE This bit sets the value on the WRITE PROTECT SPI Output Port if it is driven. 1=WRITE PROTECT is driven to 1 0=WRITE PROTECT is driven to 0	R/W	1h	RESET

38.11.5 QMSPI STATUS REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	Reserved	R	-	-
27:24	CURRENT_DESCRIPTION_BUFFER This field shows the Description Buffer currently active. This field has no meaning if Description Buffers are not enabled.	R	0h	RESET
23:17	Reserved	R	-	-
16	TRANSFER_ACTIVE 1=A transfer is currently executing 0=No transfer currently in progress	R	0h	RESET
15	RECEIVE_BUFFER_STALL 1=The SPI interface had been stalled due to a flow issue (an attempt by the interface to write to a full Receive Buffer) 0=No stalls occurred	R/WC	0h	RESET
14	RECEIVE_BUFFER_REQUEST This status is asserted if the Receive Buffer reaches a high water mark established by the RECEIVE_BUFFER_TRIGGER field. 1=RECEIVE_BUFFER_COUNT is greater than or equal to RECEIVE_BUFFER_TRIGGER 0=RECEIVE_BUFFER_COUNT is less than RECEIVE_BUFFER_TRIGGER	R/WC	0h	RESET
13	RECEIVE_BUFFER_EMPTY 1=The Receive Buffer is empty 0=The Receive Buffer is not empty	R	1h	RESET
12	RECEIVE_BUFFER_FULL 1=The Receive Buffer is full 0=The Receive Buffer is not full	R	0h	RESET
11	TRANSMIT_BUFFER_STALL 1=The SPI interface had been stalled due to a flow issue (an attempt by the interface to read from an empty Transmit Buffer) 0=No stalls occurred	R/WC	0h	RESET

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
10	TRANSMIT_BUFFER_REQUEST This status is asserted if the Transmit Buffer reaches a high water mark established by the TRANSMIT_BUFFER_TRIGGER field. 1=TRANSMIT_BUFFER_COUNT is less than or equal to TRANSMIT_BUFFER_TRIGGER 0=TRANSMIT_BUFFER_COUNT is greater than TRANSMIT_BUFFER_TRIGGER	R/WC	0h	RESET
9	TRANSMIT_BUFFER_EMPTY 1=The Transmit Buffer is empty 0=The Transmit Buffer is not empty	R	0h	RESET
8	TRANSMIT_BUFFER_FULL 1=The Transmit Buffer is full 0=The Transmit Buffer is not full	R	0h	RESET
7:5	Reserved	R	-	-
4	PROGRAMMING_ERROR This bit if a programming error is detected. Programming errors are listed in Section 38.10.4, "Error Conditions". 1=Programming Error detected 0=No programming error detected	R/WC	0h	RESET
3	RECEIVE_BUFFER_ERROR 1=Underflow error occurred (attempt to read from an empty Receive Buffer) 0=No underflow occurred	R/WC	0h	RESET
2	TRANSMIT_BUFFER_ERROR 1=Overflow error occurred (attempt to write to a full Transmit Buffer) 0=No overflow occurred	R/WC	0h	RESET
1	DMA_COMPLETE This field has no meaning if DMA is not enabled. This bit will be set to '1' when the DMA controller asserts the DONE signal to the SPI controller. This occurs either when the SPI controller has closed the DMA transfer, or the DMA channel has completed its count. If both Transmit and Receive DMA transfers are active, then this bit will only assert after both have completed. If CLOSE_TRANSFER_ENABLE is enabled, DMA_COMPLETE and TRANSFER_COMPLETE will be asserted simultaneously. This status is not inhibited by the description buffers, so it can fire on all valid description buffers while operating in that mode. 1=DMA completed 0=DMA not completed	R/WC	0h	RESET

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Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
0	TRANSFER_COMPLETE In Manual Mode (neither DMA nor Description Buffers are enabled), this bit will be set to '1' when the transfer matches TRANSFER_LENGTH. If DMA Mode is enabled, this bit will be set to '1' when DMA_COMPLETE is set to '1'. In Description Buffer Mode, this bit will be set to '1' only when the Last Buffer completes its transfer. In all cases, this bit will be set to '1' if the STOP bit is set to '1' and the controller has completed the current 8 bits being copied. 1=Transfer completed 0=Transfer not complete	R/WC	0h	RESET

38.11.6 QMSPI BUFFER COUNT STATUS REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	RECEIVE_BUFFER_COUNT This is a count of the number of bytes currently valid in the Receive Buffer.	R	0h	RESET
15:0	TRANSMIT_BUFFER_COUNT This is a count of the number of bytes currently valid in the Transmit Buffer.	R	0h	RESET

38.11.7 QMSPI INTERRUPT ENABLE REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:15	Reserved	R	-	-
14	RECEIVE_BUFFER_REQUEST_ENABLE 1=Enable an interrupt if RECEIVE_BUFFER_REQUEST is asserted 0=Disable the interrupt	R/W	0h	RESET
13	RECEIVE_BUFFER_EMPTY_ENABLE 1=Enable an interrupt if RECEIVE_BUFFER_EMPTY is asserted 0=Disable the interrupt	R/W	1h	RESET
12	RECEIVE_BUFFER_FULL_ENABLE 1=Enable an interrupt if RECEIVE_BUFFER_FULL is asserted 0=Disable the interrupt	R/W	0h	RESET
11	Reserved	R	-	-

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
10	TRANSMIT_BUFFER_REQUEST_ENABLE 1=Enable an interrupt if TRANSMIT_BUFFER_REQUEST is asserted 0=Disable the interrupt	R/W	0h	RESET
9	TRANSMIT_BUFFER_EMPTY_ENABLE 1=Enable an interrupt if TRANSMIT_BUFFER_EMPTY is asserted 0=Disable the interrupt	R/W	0h	RESET
8	TRANSMIT_BUFFER_FULL_ENABLE 1=Enable an interrupt if TRANSMIT_BUFFER_FULL is asserted 0=Disable the interrupt	R/W	0h	RESET
7:5	Reserved	R	-	-
4	PROGRAMMING_ERROR_ENABLE 1=Enable an interrupt if PROGRAMMING_ERROR is asserted 0=Disable the interrupt	R/W	0h	RESET
3	RECEIVE_BUFFER_ERROR_ENABLE 1=Enable an interrupt if RECEIVE_BUFFER_ERROR is asserted 0=Disable the interrupt	R/W	0h	RESET
2	TRANSMIT_BUFFER_ERROR_ENABLE 1=Enable an interrupt if TRANSMIT_BUFFER_ERROR is asserted 0=Disable the interrupt	R/W	0h	RESET
1	DMA_COMPLETE_ENABLE 1=Enable an interrupt if DMA_COMPLETE is asserted 0=Disable the interrupt	R/W	0h	RESET
0	TRANSFER_COMPLETE_ENABLE 1=Enable an interrupt if TRANSFER_COMPLETE is asserted 0=Disable the interrupt	R/W	0h	RESET

38.11.8 QMSPI BUFFER COUNT TRIGGER REGISTER

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	RECEIVE_BUFFER_TRIGGER An interrupt is triggered if the RECEIVE_BUFFER_COUNT field is greater than or equal to this value. A value of ‘0’ disables the interrupt.	R/W	0h	RESET
15:0	TRANSMIT_BUFFER_TRIGGER An interrupt is triggered if the TRANSMIT_BUFFER_COUNT field is less than or equal to this value. A value of ‘0’ disables the interrupt.	R/W	0h	RESET

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38.11.9 QMSPI TRANSMIT BUFFER REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	TRANSMIT_BUFFER Writes to this register store data to be transmitted from the SPI Master to the external SPI Slave. Writes to this block will be written to the Transmit FIFO. A 1 Byte write fills 1 byte of the FIFO. A Word write fills 2 Bytes and a Doubleword write fills 4 bytes. The data must always be aligned to the bottom most byte (so 1 byte write is on bits [7:0] and Word write is on [15:0]). An overflow condition,TRANSMIT_BUFFER_ERROR, if a write to a full FIFO occurs. Write accesses to this register increment the TRANSMIT_BUFFER_COUNT field.	W	0h	RESET

38.11.10 QMSPI RECEIVE BUFFER REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	RECEIVE_BUFFER Buffer that stores data from the external SPI Slave device to the SPI Master (this block), which is received over MISO or IO. Reads from this register will empty the Rx FIFO. A 1 Byte read will have valid data on bits [7:0] and a Word read will have data on bits [15:0]. It is possible to request more data than the FIFO has (underflow condition), but this will cause an error (Rx Buffer Error). Read accesses to this register decrement the RECEIVE_BUFFER_COUNT field.	R	0h	RESET

38.11.11 QMSPI DESCRIPTION BUFFER 0 REGISTER

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:17	TRANSFER_LENGTH The length of the SPI transfer. The count is in bytes or bits, depending on the value of TRANSFER_LENGTH_BITS. A value of ‘0’ means an infinite length transfer.	R/W	0h	RESET
16	DESCRIPTION_BUFFER_LAST If this bit is ‘1’ then this is the last Description Buffer in the chain. When the transfer described by this buffer completes the TRANSFER_COMPLETE status will be set to ‘1’. If this bit is ‘0’, then this is not the last buffer in use. When the transfer completes the next buffer will be activated, and no additional status will be asserted.	R/W	0h	RESET

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:12	DESCRIPTION_BUFFER_NEXT_POINTER This defines the next buffer to be used if Description Buffers are enabled and this is not the last buffer. This can point to the current buffer, creating an infinite loop.	R/W	0h	RESET
11:10	TRANSFER_UNITS 3=TRANSFER_LENGTH defined in units of 16-byte segments 2=TRANSFER_LENGTH defined in units of 4-byte segments 1=TRANSFER_LENGTH defined in units of bytes 0=TRANSFER_LENGTH defined in units of bits	R/W	0h	RESET
9	CLOSE_TRANFSER_ENABLE This selects what action is taken at the end of a transfer. This bit must be set only on the Last Buffer. 1=The transfer is terminated. The Chip Select de-asserts, the SPI interface returns to IDLE and the DMA interface completes the transfer. 0=The transfer is not closed. Chip Select remains asserted and the DMA interface and the SPI interface remain active	R/W	1h	RESET
8:7	RX_DMA_ENABLE This bit enables DMA support for Receive Transfer. If enabled, DMA will be requested to empty the FIFO until either the interface reaches TRANSFER_LENGTH or the DMA sends a termination request. The size defined here must match DMA programmed access size. 1=DMA is enabled.and set to 1 Byte 2=DMA is enabled and set to 2 Bytes 3=DMA is enabled and set to 4 Bytes 0=DMA is disabled. All data in the Receive Buffer must be emptied by firmware	R/W	0h	RESET
6	RX_TRANSFER_ENABLE This bit enables the receive function of the SPI interface. 1=Receive is enabled. Data received from the SPI Slave is stored in the Receive Buffer 0=Receive is disabled	R/W	0h	RESET
5:4	TX_DMA_ENABLE This bit enables DMA support for Transmit Transfer. If enabled, DMA will be requested to fill the FIFO until either the interface reaches TRANSFER_LENGTH or the DMA sends a termination request. The size defined here must match DMA programmed access size. 1=DMA is enabled.and set to 1 Byte 2=DMA is enabled and set to 2 Bytes 3=DMA is enabled and set to 4 Bytes 0=DMA is disabled. All data in the Transmit Buffer must be emptied by firmware	R/W	0h	RESET

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Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3:2	TX_TRANSFER_ENABLE This field bit selects the transmit function of the SPI interface. 3=Transmit Enabled in 1 Mode. The MOSI or IO Bus will send out only 1's. The Transmit Buffer will not be used 2=Transmit Enabled in 0 Mode. The MOSI or IO Bus will send out only 0's. The Transmit Buffer will not be used. 1=Transmit Enabled. Data will be fetched from the Transmit Buffer and sent out on the MOSI or IO Bus. 0=Transmit is Disabled. No data is sent. This will cause the MOSI be to be undriven, or the IO bus to be undriven if Receive is also disabled.	R/W	0h	RESET
1:0	INTERFACE_MODE This field sets the transmission mode. If this field is set for Dual Mode or Quad Mode then either TX_TRANSFER_ENABLE or RX_TRANSFER_ENABLE **must** be 0. 3=Reserved 2=Quad Mode 1=Dual Mode 0=Single/Duplex Mode	R/W	0h	RESET

38.11.12 QMSPI DESCRIPTION BUFFER 1 REGISTER

The format for this register is the same as the format o the QMSPI Description Buffer 0 Register.

38.11.13 QMSPI DESCRIPTION BUFFER 2 REGISTER

The format for this register is the same as the format o the QMSPI Description Buffer 0 Register.

38.11.14 QMSPI DESCRIPTION BUFFER 3 REGISTER

The format for this register is the same as the format o the QMSPI Description Buffer 0 Register.

38.11.15 QMSPI DESCRIPTION BUFFER 4 REGISTER

The format for this register is the same as the format o the QMSPI Description Buffer 0 Register.

39.0 PS/2 INTERFACE

39.1 Introduction

PS/2 controllers are directly controlled by the EC. The hardware implementation eliminates the need to bit bang I/O ports to generate PS/2 traffic, however bit banging is available via the associated GPIO pins.

39.2 References

No references have been cited for this feature.

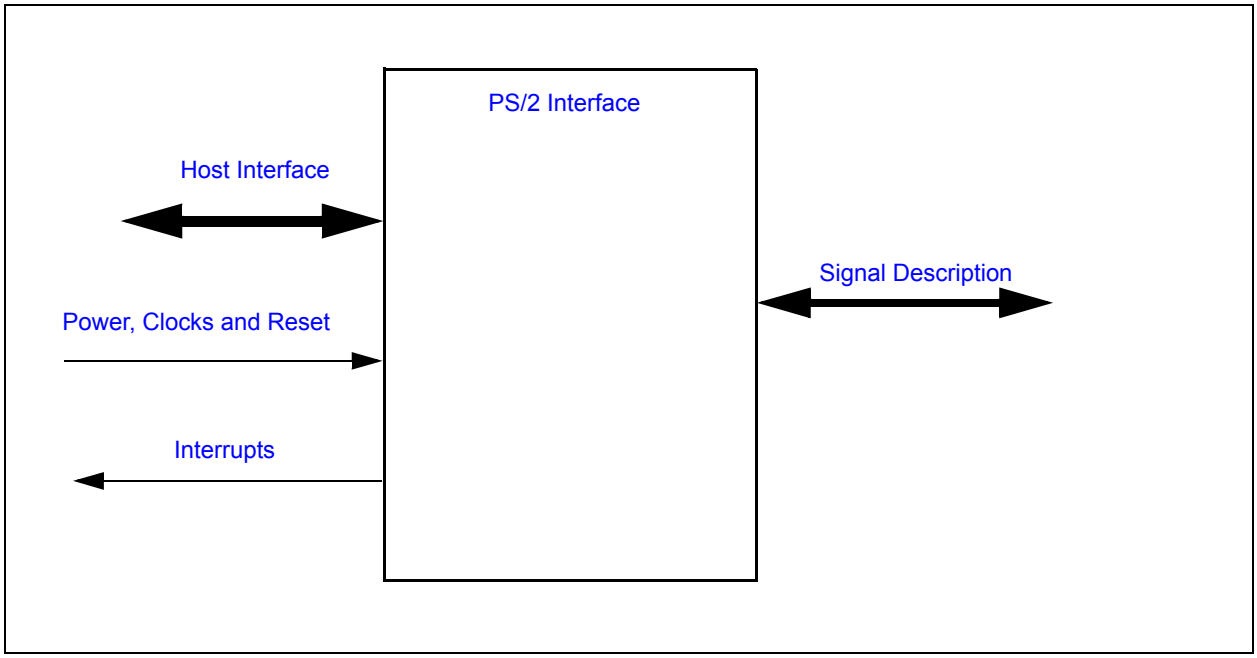
39.3 Terminology

There is no terminology defined for this section.

39.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 39-1: I/O DIAGRAM OF BLOCK



39.5 Signal Description

TABLE 39-1: SIGNAL DESCRIPTION TABLE

Name	Direction	Description
PS2DAT	INPUT/ OUTPUT	Data from the PS/2 device
PS2CLK	INPUT/ OUTPUT	Clock from the PS/2 device

Note: PS2 ports that are multiplexed onto pins that can be powered by 1.8V are not 5V tolerant, even when the pins are powered by 3.3V.

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39.6 Host Interface

The registers defined for the PS/2 Interface are accessible by the various hosts as indicated in Section 39.14, "EC Registers".

39.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

39.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

39.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for PS/2 Interface logic.
2 MHz Clock	The PS/2 state machine is clocked using the 2 MHz clock.

39.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

39.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
PS2_x	Interrupt request to the Interrupt Aggregator for PS2 controller instance *x*, based on PS2 controller activity. Section 39.14.4, "PS2 Status Register" defines the sources for the interrupt request.
PS2_*x*_WK	Wake-up request to the Interrupt Aggregator's wake-up interface for PS2 port *x*. In order to enable PS2 wakeup interrupts, the pin control registers for the PS2DAT pin must be programmed to Input, Falling Edge Triggered, non-inverted polarity detection.

39.9 Low Power Modes

The PS/2 Interface may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

The PS2 interface will only sleep while the PS2 is disabled or in Rx mode with no traffic on the bus.

39.10 Description

Each EC PS/2 serial channels use a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has Clock and Data signal lines. The signal lines are bi-directional and employ open drain outputs capable of sinking 12m, as required by the PS/2 specification. A pull-up resistor, typically 10K, is connected to both lines. This allows either the EC PS/2 logic or the auxiliary device to drive the lines. Regardless of the drive source, the auxiliary device always provides the clock for transmit and receive operations. The serial packet is made up of eleven bits, listed in the order they appear on the data line: start bit, eight data bits (least significant bit first), odd parity, and stop bit. Each bit cell is from 60µS to 100µS long.

All PS/2 Serial Channel signals (PS2CLK and PS2DAT) are driven by open drain drivers which can be pulled to VTR or the main power rail (+3.3V nominal) through 10K-ohm resistors.

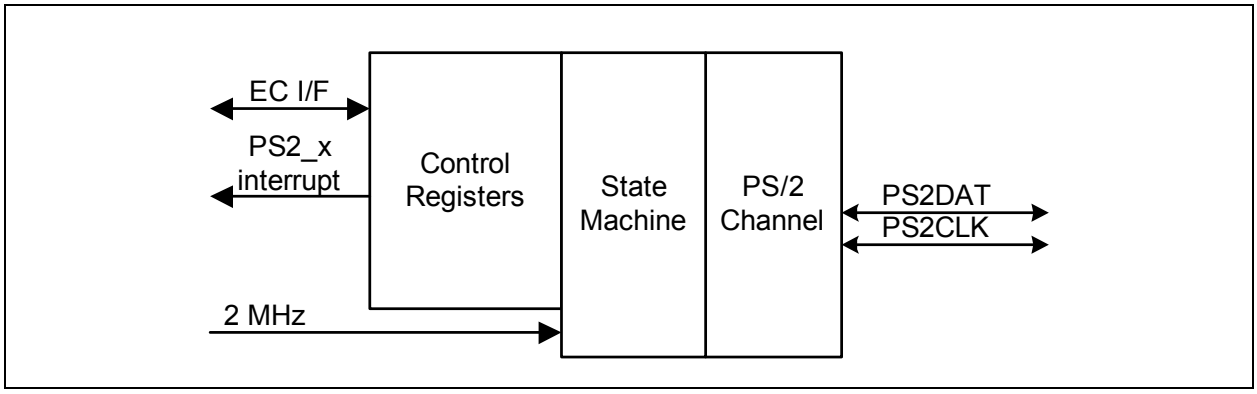
The PS/2 controller supports a PS/2 Wake Interface that can wake the EC from the IDLE or SLEEP states. The Wake Interface can generate wake interrupts without a clock. The PS/2 Wake Interface is only active when the peripheral device and external pull-up resisters are powered by the VTR supply.

There are no special precautions to be taken to prevent back drive of a PS/2 peripheral powered by the main power well when the power well is off, as long as the external 10K pull-up resistor is tied to the same power source as the peripheral.

PS/2 controllers may have one or two ports. Only one port may be active at a time. See the pin chapter for a definition of the PS/2 ports.

39.11 Block Diagram

FIGURE 39-2: PORT PS/2 BLOCK DIAGRAM



39.12 PS/2 Port Physical Layer Byte Transmission Protocol

The PS/2 physical layer transfers a byte of data via an eleven bit serial stream as shown in Table 39-2. A logic 1 is sent at an active high level. Data sent from a Keyboard or mouse device to the host is read on the falling edge of the clock signal. The Keyboard or mouse device always generates the clock signal. The Host may inhibit communication by pulling the Clock line low. The Clock line must be continuously high for at least 50 microseconds before the Keyboard or mouse device can begin to transmit its data. See Table 39-3, "PS/2 Port Physical Layer Bus States".

TABLE 39-2: PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

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FIGURE 39-3: PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

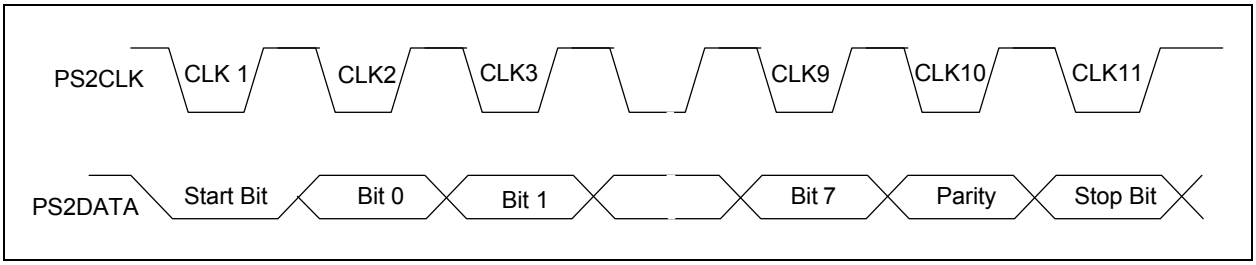

TABLE 39-3: PS/2 PORT PHYSICAL LAYER BUS STATES

Data	Clock	State
high	high	Idle
high	low	Communication Inhibited
low	low	Request to Send

39.13 Controlling PS/2 Transactions

PS/2 transfers are controlled by fields in the PS2 Control Register.

The interface is enabled by the PS2_EN bit. Transfers are enabled when PS2_EN is '1' and disabled when PS2_EN is '0'. If the PS2_EN bit is cleared to '0' while a transfer is in progress but prior to the leading edge (falling edge) of the 10th (parity bit) clock edge, the receive data is discarded (RDATA_RDY remains low). If the PS2_EN bit is cleared following the leading edge of the 10th clock signal, then the receive data is saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

The direction of a PS/2 transfer is controlled by the PS2_T/R bit.

39.13.1 RECEIVE

If PS2_T/R is '0' while the PS2 Interface is enabled, the interface is configured to receive data. If while PS2_T/R is '0' RDATA_RDY is '0', the channel's PS2CLK and PS2DAT will float waiting for the external PS/2 device to signal the start of a transmission. If RDATA_RDY is '1', the channel's PS2DAT line will float but its PS2CLK line will be held low, holding off the peripheral, until the Receive Register is read.

The peripheral initiates a reception by sending a start bit followed by the data bits). After a successful reception, data are placed in the PS2 Receive Buffer Register, the RDATA_RDY bit in the PS2 Status Register is set and the PS2CLK line is forced low. Further receive transfers are inhibited until the EC reads the data in the PS2 Receive Buffer Register. RDATA_RDY is cleared and the PS2CLK line is tri-stated following a read of the PS2 Receive Buffer Register.

The Receive Buffer Register is initialized to FFh after a read or after a Time-out has occurred.

39.13.2 TRANSMIT

If PS2_T/R is '1' while the PS2 Interface is enabled, the interface is configured to transmit data. When the PS2_T/R bit is written to '1' while the state machine is idle, the channel prepares for a transmission: the interface will drive the PS2-CLK line low and then float the PS2DAT line, holding this state until a write occurs to the Transmit Register or until the PS2_T/R bit is cleared. A transmission is started by writing the PS2 Transmit Buffer Register. Writes to the Transmit Buffer Register are blocked when PS2_EN is '0', PS2_T/R is '0' or when the transmit state machine is active (the XMIT_IDLE bit in the PS/2 Status Register is '0'). The transmission of data will not start if there is valid data in the Receive Data Register (when the status bit RDATA_RDY is '1'). When a transmission is started, the transmission state machine becomes active (the XMIT_IDLE bit is set to '1' by hardware), the PS2DAT line is driven low and within 80ns the PS2CLK line floats (externally pulled high by the pull-up resistor).

The transmission terminates either on the 11th clock edge of the transmission or if a Transmit Time-Out error condition occurs. When the transmission terminates, the PS2_T/R bit is cleared to '0'and the state machine becomes idle, setting XMIT_IDLE to '1'.

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The PS2_T/R bit must be written to a ‘1’ before initiating another transmission to the remote device. If the PS2_T/R bit is set to ‘1’ while the channel is actively receiving data (that is, while the status bit RDATA_RDYis ‘1’) prior to the leading edge of the 10th (parity bit) clock edge, the receive data is discarded. If the bit is set after the 10th edge, the receive data is saved in the Receive Register.

39.14 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the PS/2 Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 39-4: REGISTER SUMMARY

Offset	Register Name
0h	PS2 Transmit Buffer Register
0h	PS2 Receive Buffer Register
4h	PS2 Control Register
8h	PS2 Status Register

39.14.1 PS2 TRANSMIT BUFFER REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	TRANSMIT_DATA Writes to this register start a transmission of the data in this register to the peripheral.	W	0h	RESET_SYS

39.14.2 PS2 RECEIVE BUFFER REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	RECEIVE_DATA Data received from a peripheral are recorded in this register. A transmission initiated by writing the PS2 Transmit Buffer Register will not start until valid data in this register have been read and RDATA_RDY has been cleared by hardware. The Receive Buffer Register is initialized to FFh after a read or after a Time-out has occurred.	R	FFh	RESET_SYS

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39.14.3 PS2 CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:6	Reserved	R	-	-
5:4	STOP These bits are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN is set. 00b=Receiver expects an active high stop bit. 01b=Receiver expects an active low stop bit. 10b=Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit). 11b=Reserved.	R/W	0h	RESET_SYS
3:2	PARITY These bits are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN is set. 00b=Receiver expects Odd Parity (default). 01b=Receiver expects Even Parity. 10b=Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit). 11b=Reserved	R/W	0h	RESET_SYS
1	PS2_EN PS/2 Enable. 0=The PS/2 state machine is disabled. The CLK pin is driven low and the DATA pin is tri-stated. 1=The PS/2 state machine is enabled, allowing the channel to perform automatic reception or transmission, depending on the state of PS2_T/R.	R/W	0h	RESET_SYS
0	PS2_T/R PS/2 Transmit/Receive 0=The P2/2 channel is enabled to receive data. 1=The PS2 channel is enabled to transmit data.	R/W	0h	RESET_SYS

Changing values in the PS2 CONTROL REGISTER at a rate faster than 2 MHz, may result in unpredictable behavior.

39.14.4 PS2 STATUS REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7	XMIT_START_TIMEOUT Transmit Start Timeout. 0=No transmit start timeout detected 1=A start bit was not received within 25 ms following the transmit start event. The transmit start bit time-out condition is also indicated by the XMIT_TIMEOUT bit.	R/WC	0h	RESET_SYS
6	RX_BUSY Receive Channel Busy. 0=The channel is actively receiving PS/2 data 1=The channel is idle	R	0h	RESET_SYS
5	XMIT_TIME_OUT Transmitter Idle. When the XMIT_TIMEOUT bit is set, the PS2_T/R bit is held clear, the PS/2 channel's CLK line is pulled low for a minimum of 300µs until the PS/2 Status register is read. The XMIT_TIMEOUT bit is set on one of three transmit conditions: when the transmitter bit time (the time between falling edges) exceeds 300µs, when the transmitter start bit is not received within 25ms from signaling a transmit start event or if the time from the first bit (start) to the 10th bit (parity) exceeds 2ms	R/WC	0h	RESET_SYS
4	XMIT_IDLE Transmitter Idle. 0=The channel is actively transmitting PS/2 data. Writing the PS2 Transmit Buffer Register will cause the XMIT_IDLE bit to clear 1=The channel is not transmitting. This bit transitions from '0' to '1' in the following cases: • The falling edge of the 11th CLK • XMIT_TIMEOUT is set • The PS2_T/R bit is cleared • The PS2_EN bit is cleared. A low to high transition on this bit generates a PS2 Activity interrupt.	R	0h	RESET_SYS
3	FE Framing Error When receiving data, the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel is configured to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an interrupt is generated.	R/WC	0h	RESET_SYS

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Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	PE Parity Error When receiving data, the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel is configured to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an interrupt is generated.	R/WC	0h	RESET_SYS
1	REC_TIMEOUT Receive Timeout Following assertion of the REC_TIMEOUT bit, the channel's CLK line is automatically pulled low for a minimum of 300µs until the PS/2 status register is read. Under PS2 automatic operation, PS2_EN is set, this bit is set on one of three receive error conditions: • When the receiver bit time (the time between falling edges) exceeds 300µs. • If the time from the first bit (start) to the 10th bit (parity) exceeds 2ms. • On a receive parity error along with the Parity Error (PE) bit. • On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit. A low to high transition on this bit generates a PS2 Activity interrupt.	R/WC	0h	RESET_SYS
0	RDATA_RDY Receive Data Ready Under normal operating conditions, this bit is set following the falling edge of the 11th clock given successful reception of a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive timeout errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS2_EN bit is cleared following the 10th CLK edge. Reading the Receive Register clears this bit. A low to high transition on this bit generates a PS2 Activity interrupt.	R	0h	RESET_SYS

40.0 BC-LINK MASTER

40.1 Overview

This block provides BC-Link™ connectivity to a slave device. The BC-Link™ protocol includes a start bit to signal the beginning of a message and a turnaround (TAR) period for bus transfer between the Master and Companion devices.

40.2 References

No references have been cited for this feature.

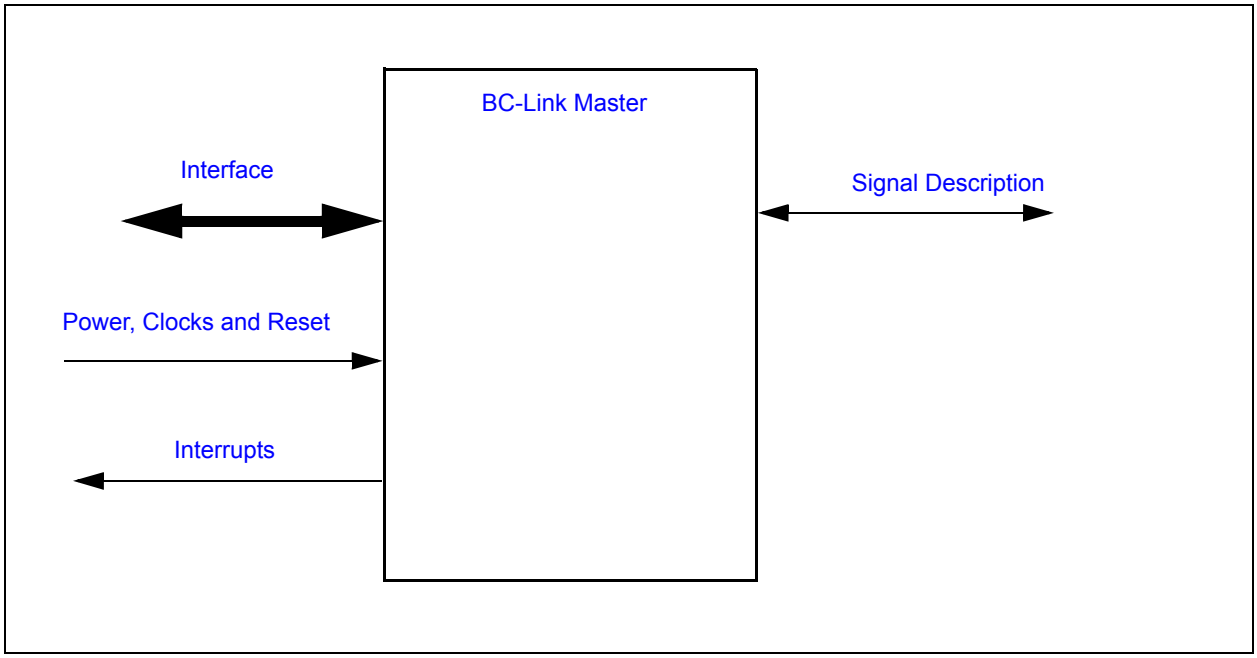
40.3 Terminology

There is no terminology defined for this section.

40.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 40-1: I/O DIAGRAM OF BLOCK



40.5 Signal Description

TABLE 40-1: SIGNAL DESCRIPTION

Name	Direction	Description
BCM_CLK	Output	BC-Link output clock
BCM_DAT	Input/Output	Bidirectional data line

Note: A weak pull-up resistor is recommended on the data line (100KW).

The maximum speed at which the BC-Link Master Interface can operate reliably depends on the drive strength of the BC-Link BCM_CLK and BCM_DAT pins, as well as the nature of the connection to the Companion device (over ribbon cable or on a PC board). The following table shows the recommended maximum speeds over a PC board as well as a 12 inch ribbon cable for selected drive strengths. The frequency is set with the BC-Link Clock Select Register.

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There is no explicit BC-Link INT# input signal. Any GPIO input can be used to generate an interrupt from a BC-Link companion's INT# output.

TABLE 40-2: BC-LINK MASTER PIN DRIVE STRENGTH VS. FREQUENCY

Pin Drive Strength	Max Freq on PC Board	Min Value in BC-Link Clock Select Register	Max Freq over Ribbon cable	Min Value in BC-Link Clock Select Register
12mA	24Mhz	1	16Mhz	2
8mA	3MHz	15	3MHz	15

40.6 Host Interface

The registers defined for the BC-Link Master Interface are accessible by the various hosts as indicated in Section 40.11, "EC Registers".

40.7 Power, Clocks and Reset

40.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

40.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for this block.

40.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

40.8 Interrupts

This section defines the Interrupt Sources generated from this block.

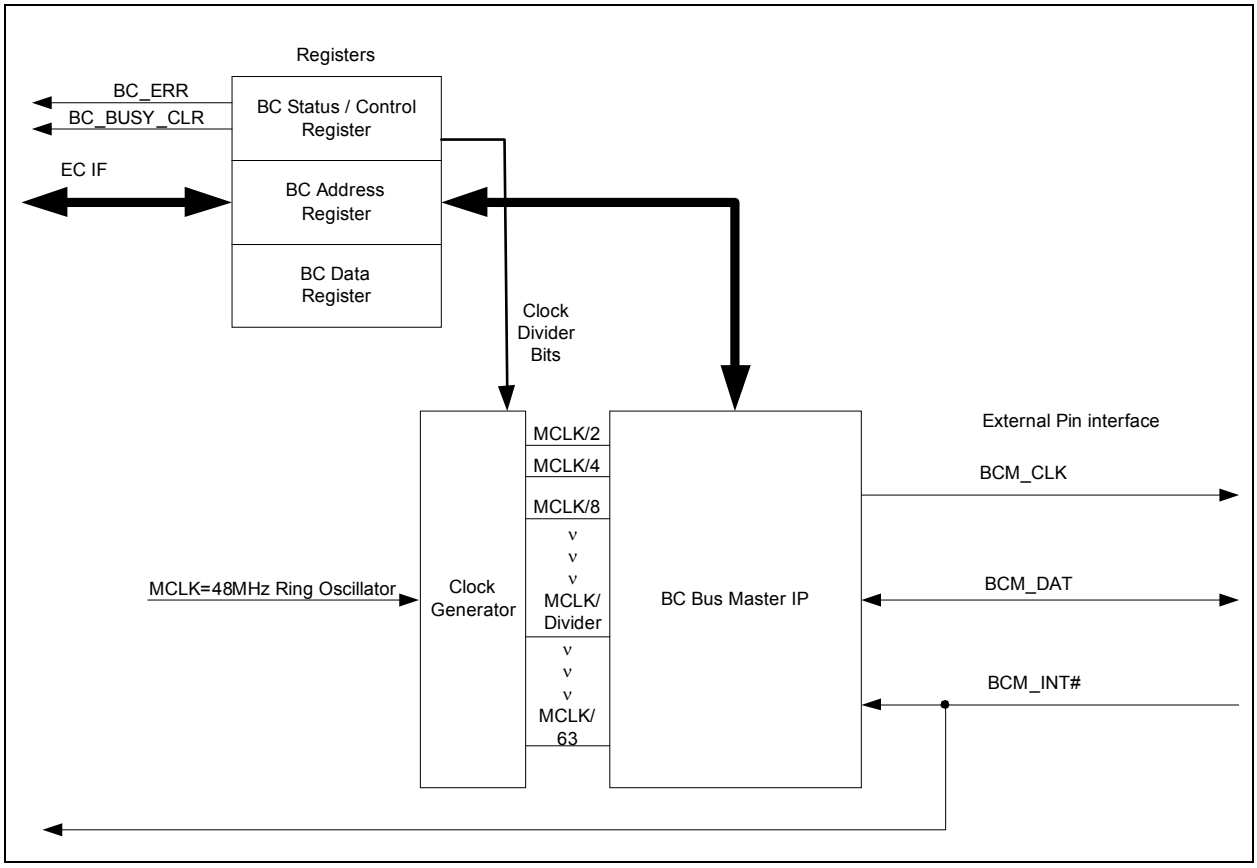
Source	Description
BCM_INT Busy	Interrupt request to the Interrupt Aggregator, generated from the status event BUSYdefined in the BC-Link Status Register.
BCM_INT Err	Interrupt request to the Interrupt Aggregator, generated from the status event defined in the BC-Link Status Register.

40.9 Low Power Modes

The BC-Link Master Interface automatically enters a low power mode whenever it is not active (that is, whenever the BUSY bit in the BC-Link Status Register is '0'). When the interface is in a low-power mode it will not prevent the chip from entering a sleep state. When the interface is active it will inhibit the chip sleep state until the interface has re-entered its low power mode.

40.10 Description

FIGURE 40-2: BC-LINK MASTER BLOCK DIAGRAM



40.10.1 BC-LINK MASTER READ OPERATION

The BC-Link Read protocol requires two reads of the BC-Link Data Register. The two reads drive a two state-state machine: the two states are Read#1 and Read#2. The Read#1 of the Data Register starts the read protocol on the BC-Link pins and sets the BUSY bit in the BC-Link Status Register. The contents of the data read during Read#1 by the EC is stale and is not to be used. After the BUSY bit in the BC-Link Status Register autonomously clears to '0', the Read#2 of the Data Register transfers the data read from the peripheral/BC-Link companion chip to the EC.

1. Software starts by checking the status of the BUSY bit in the Status Register. If the BUSY bit is '0', proceed. If BUSY is '1', firmware must wait until it is '0'.
2. Software writes the address of the register to be read into the BC-Link Address Register.
3. Software then reads the Data Register. This read returns random data. The read activates the BC-Link Master state machine to transmit the read request packet to the BC-Link companion. When the transfer initiates, the hardware sets the BUSY bit to a '1'.
4. The BC-Link Companion reads the selected register and transmits the read response packet to the BC-Link Master. The Companion will ignore the read request if there is a CRC error; this will cause the Master state machine to time-out and issue a BC_ERR Interrupt.
5. The Master state machine loads the Data Register, issues a BUSY Bit Clear interrupt and clears the BUSY bit to '0'.
6. Software, after either receiving the Bit Clear interrupt, or polling the BUSY bit until it is '0', checks the BC_ERR bit in the Status Register.
7. Software can now read the Data Register which contains the valid data if there was no BC Bus error.
8. If a Bus Error occurs, firmware must issue a soft reset by setting the RESET bit in the Status Register to '1'.
9. The read can re-tried once BUSY is cleared.

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Note:	Steps 3 thorough 7 should be completed as a contiguous sequence. If not the interface could be presenting incorrect data when software thinks it is accessing a valid register read.

40.10.2 BC-LINK MASTER WRITE OPERATION

1. Software starts by checking the status of the BUSY bit in the BC-Link Status Register. If the BUSY bit is ‘0’, proceed. If BUSY is ‘1’, firmware must wait until it is ‘0’.
2. Software writes the address of the register to be written into the BC-Link Address Register.
3. Software writes the data to be written into the addressed register in to the BC-Link Data Register.
4. The write to the Data Register starts the BC_Link write operation. The Master state machine sets the BUSY bit.
5. The BC-Link Master Interface transmits the write request packet.
6. When the write request packet is received by the BC-Link companion, the CRC is checked and data is written to the addressed companion register.
7. The companion sends an ACK if the write is completed. A time-out will occur approximately 16 BC-Link clocks after the packet is sent by the Master state machine. If a time-out occurs, the state machine will set the BC_ERR bit in the Status Register to ‘1’ approximately 48 clocks later and then clear the BUSY bit.
8. The Master state machine issues the Bit Clear interrupt and clears the BUSY bit after receiving the ACK from the Companion
9. If a Bus Error occurs, firmware must issue a soft reset by setting the RESET bit in the Status Register to ‘1’.
10. The write can re-tried once BUSY is cleared.\

40.11 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the BC-Link Master Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 40-3: REGISTER SUMMARY

EC Offset	Register Name
00h	BC-Link Status Register
04h	BC-Link Address Register
08h	BC-Link Data Register
0Ch	BC-Link Clock Select Register

40.11.1 BC-LINK STATUS REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7	RESET When this bit is ‘1’the BC_Link Master Interface will be placed in reset and be held in reset until this bit is cleared to ‘0’. Setting RESET to ‘1’ causes the BUSY bit to be set to ‘1’. The BUSY remains set to ‘1’ until the reset operation of the BC Interface is completed, which takes approximately 48 BC clocks. The de-assertion of the BUSY bit on reset will not generate an interrupt, even if the BC_BUSY_CLR_INT_EN bit is ‘1’. The BUSY bit must be polled in order to determine when the reset operation has completed.	R/W	1h	RESET_SYS
6	BC_ERR This bit indicates that a BC Bus Error has occurred. If an error occurs this bit is set by hardware when the BUSY bit is cleared. This bit is cleared when written with a ’1b’. An interrupt is generated If this bit is ‘1’ and BC_ERR_INT_EN bit is ‘1b’. Errors that cause this interrupt are: • Bad Data received by the BASE (CRC Error) • Time-out caused by the COMPANION not responding. All COMPANION errors cause the COMPANION to abort the operation and the BASE to time-out.Figure 40.11.2	R/WC	0h	RESET_SYS
5	BC_ERR_INT_EN This bit is an enable for generating an interrupt when the BC_ERR bit is set by hardware. When this bit is ‘1’, the interrupt signal is enabled. When this bit is ‘0’, the interrupt is disabled.	R/W	0h	RESET_SYS
4	BC_BUSY_CLR_INT_EN This bit is an enable for generating an interrupt when the BUSY bit in this register is cleared by hardware. When this bit is set to ‘1’, the interrupt signal is enabled. When the this bit is cleared to ‘0’, the interrupt is disabled. When enabled, the interrupt occurs after a BC Bus read or write.	R/W	0h	RESET_SYS
3:1	Reserved	R	-	-
0	BUSY This bit is asserted to ‘1’ when the BC interface is transferring data and on reset. Otherwise it is cleared to ‘0’. When this bit is cleared by hardware, an interrupt is generated if the BC_BUSY_CLR_INT_EN bit is set to ‘1’.	R	1h	RESET_SYS

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40.11.2 BC-LINK ADDRESS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	ADDRESS Address in the Companion for the BC-Link transaction.	R/W	0h	RESET_SYS

40.11.3 BC-LINK DATA REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	DATA As described in Section 40.10.1, "BC-Link Master READ Operation" and Section 40.10.2, "BC-Link Master WRITE Operation", this register hold data used in a BC-Link transaction.	R/W	0h	RESET_SYS

40.11.4 BC-LINK CLOCK SELECT REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	DIVIDER The BC Clock is set to the Master Clock divided by this field, or 48MHz/ (Divider +1). The clock divider bits can only can be changed when the BC Bus is in soft RESET (when either the Reset bit is set by software or when the BUSY bit is set by the interface). Example settings for DIVIDER are shown in Table 40-4, "Example Frequency Settings".	R/W	4h	RESET_SYS

TABLE 40-4: EXAMPLE FREQUENCY SETTINGS

Divider	Frequency
0	48MHz
1	24MHz
2	16MHz
3	12MHz
4	9.6MHz
6	6.9MHz
15	3MHz
47	1MHz

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41.0 TRACE FIFO DEBUG PORT (TFDP)

41.1 Introduction

The TFDP serially transmits Embedded Controller (EC)-originated diagnostic vectors to an external debug trace system.

41.2 References

No references have been cited for this chapter.

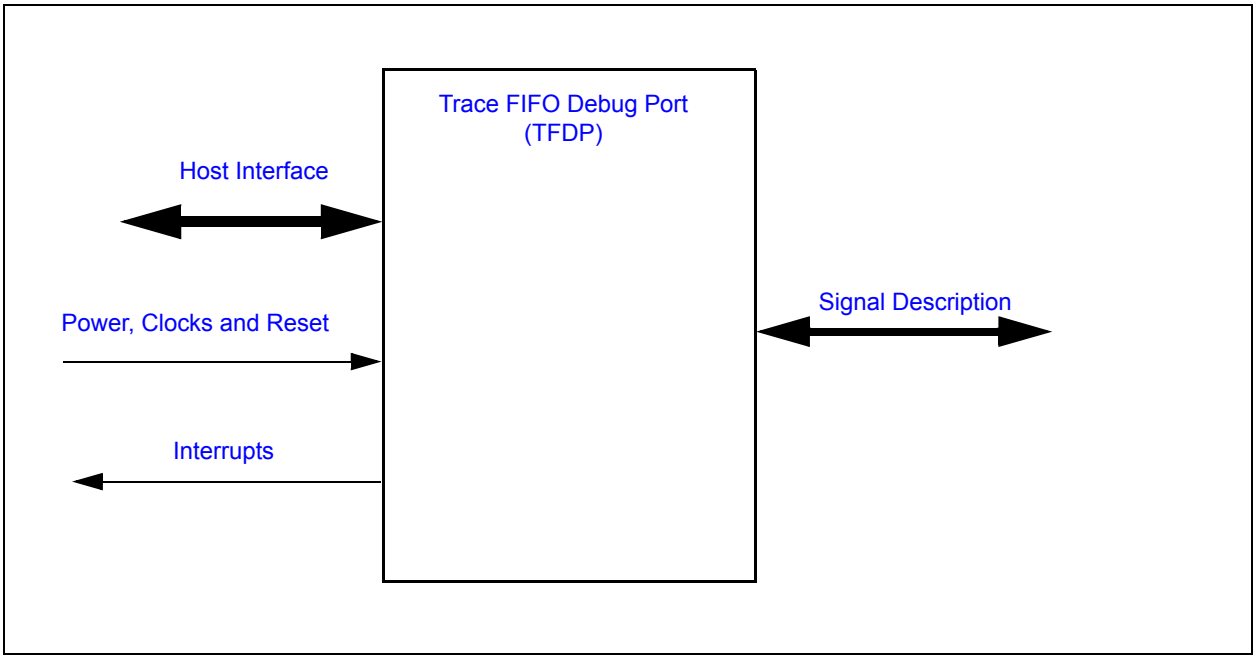
41.3 Terminology

There is no terminology defined for this chapter.

41.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 41-1: I/O DIAGRAM OF BLOCK



41.5 Signal Description

The Signal Description Table lists the signals that are typically routed to the pin interface.

TABLE 41-1: SIGNAL DESCRIPTION

Name	Direction	Description
TFDP Clk	Output	Derived from EC Bus Clock.
TFDP Data	Output	Serialized data shifted out by TFDP Clk.

41.6 Host Interface

The registers defined for the Trace FIFO Debug Port (TFDP) are accessible by the various hosts as indicated in Section 41.11, "EC-Only Registers".

41.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

41.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

41.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the main system clock.

41.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

41.8 Interrupts

There are no interrupts generated from this block.

41.9 Low Power Modes

The Trace FIFO Debug Port (TFDP) may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

41.10 Description

The TFDP is a unidirectional (from processor to external world) two-wire serial, byte-oriented debug interface for use by processor firmware to transmit diagnostic information.

The TFDP consists of the Debug Data Register, Debug Control Register, a Parallel-to-Serial Converter, a Clock/Control Interface and a two-pin external interface (TFDP Clk, TFDP Data). See Figure 41-2.

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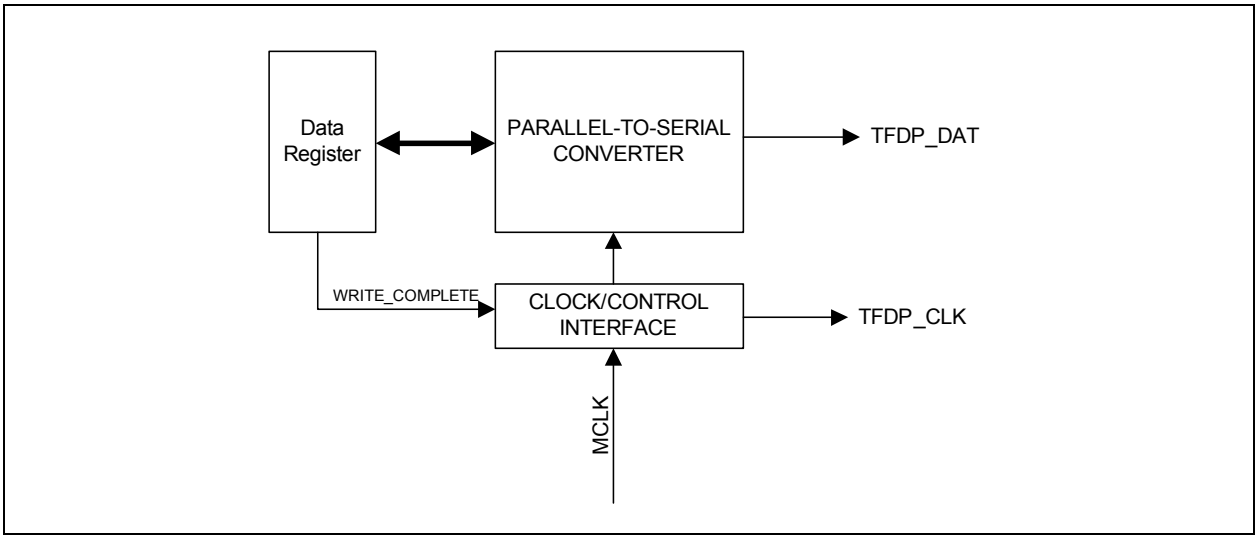
FIGURE 41-2: BLOCK DIAGRAM OF TFDP DEBUG PORT

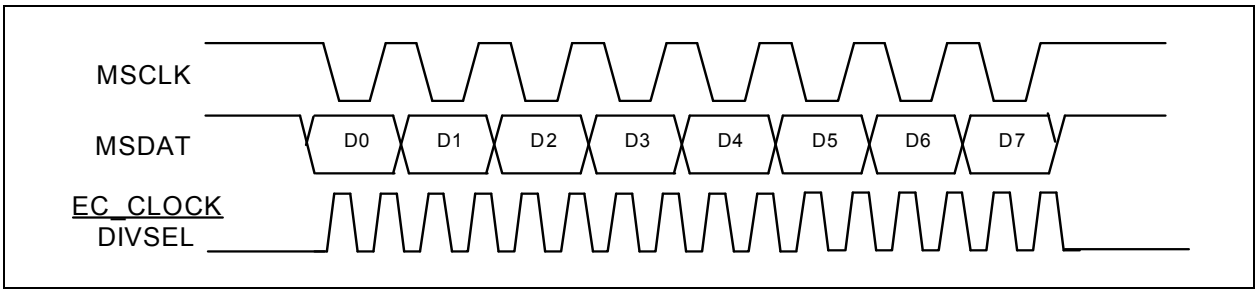


The firmware executing on the embedded controller writes to the Debug Data Register to initiate a transfer cycle (Figure 41.11). At first, data from the Debug Data Register is shifted into the LSB. Afterwards, it is transmitted at the rate of one byte per transfer cycle.

Data is transferred in one direction only from the Debug Data Register to the external interface. The data is shifted out at the clock edge. The clock edge is selected by the EDGE_SEL bit in the Debug Control Register. After being shifted out, valid data will be presented at the opposite edge of the TFDP_CLK. For example, when the EDGE_SEL bit is '0' (default), valid data will be presented on the falling edge of the TFDP_CLK. The Setup Time (to the falling edge of TFDP_CLK) is 10 ns, minimum. The Hold Time is 1 ns, minimum.

When the Serial Debug Port is inactive, the TFDP_CLK and TFDP_DAT outputs are '1.' The EC Bus Clock clock input is the transfer clock.

FIGURE 41-3: DATA TRANSFER



41.11 EC-Only Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the Trace FIFO Debug Port (TFDP) Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 41-2: REGISTER SUMMARY

Offset	Register Name
00h	Debug Data Register
04h	Debug Control Register

41.11.1 DEBUG DATA REGISTER

The Debut Data Register is Read/Write. It always returns the last data written by the TFDP or the power-on default ‘00h’.

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DATA Debug data to be shifted out on the TFDP Debug port. While data is being shifted out, the Host Interface will ‘hold-off’ additional writes to the data register until the transfer is complete.	R/W	00h	RESET_SYS

41.11.2 DEBUG CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	Reserved	R	-	-
6:4	IP_DELAY Inter-packet Delay. The delay is in terms of TFDP Debug output clocks. A value of 0 provides a 1 clock inter-packet period, while a value of 7 provides 8 clocks between packets:	R/W	000b	RESET_SYS
3:2	DIVSEL Clock Divider Select. The TFDP Debug output clock is determined by this field, according to Table 41-3, "TFDP Debug Clocking":	R/W	00b	RESET_SYS
1	EDGE_SEL 1=Data is shifted out on the falling edge of the debug clock 0=Data is shifted out on the rising edge of the debug clock (Default)	R/W	0b	RESET_SYS
0	EN Enable. 1=Clock enabled 0=Clock is disabled (Default)	R/W	0b	RESET_SYS

TABLE 41-3: TFDP DEBUG CLOCKING

divsel	TFDP Debug Clock
00	24 MHz
01	12 MHz
10	6 MHz
11	Reserved

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42.0 PORT 80 BIOS DEBUG PORT

42.1 Overview

The Port 80 BIOS Debug Port emulates the functionality of a “Port 80” ISA plug-in card. In addition, a timestamp for the debug data can be optionally added.

Diagnostic data is written by the Host Interface to the Port 80 BIOS Debug Port, which is located in the Host I/O address space. The Port 80 BIOS Debug Port generates an interrupt to the EC when host data is available. The EC reads this data along with the timestamp, if enabled.

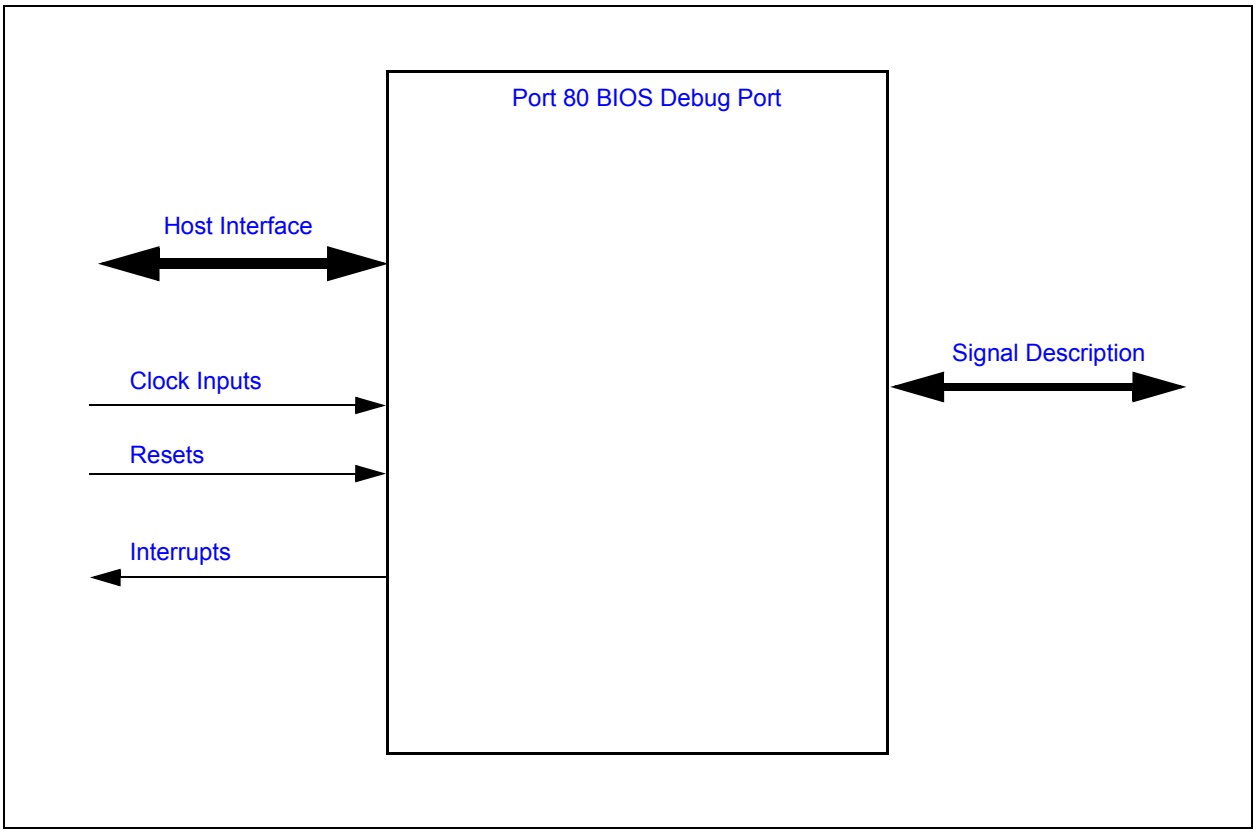
42.2 References

There are no references for this block.

42.3 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 42-1: I/O DIAGRAM OF BLOCK



42.4 Signal Description

There are no external signals for this block.

42.5 Host Interface

The Port 80 block is accessed by host software via a registered interface, as defined in Section 42.11, "Runtime Registers". In addition, there is a set of registers accessible to the EC, defined in Section 42.12, "EC Registers".

42.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

42.6.1 POWER DOMAINS

Name	Description
VTR	This Power Well is used to power the registers and logic in this block.

42.6.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for Port 80 block logic.

42.6.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

42.7 Interrupts

This section defines the Interrupt Sources generated from this block.

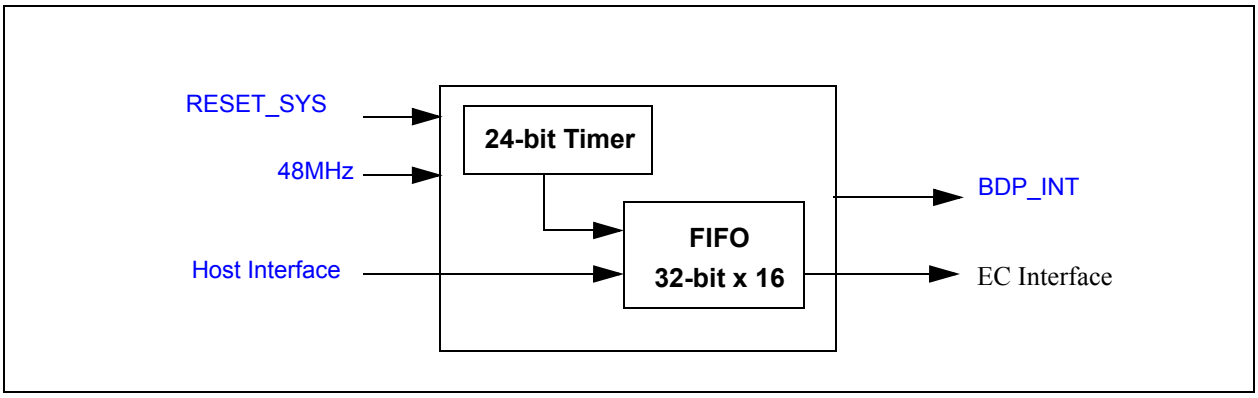
Source	Description
BDP_INT	The Port 80 BIOS Debug Port generates an EC interrupt when the amount of data in the Port 80 FIFO equals or exceeds the FIFO Threshold defined in the Configuration Register. The interrupt signal is always generated by the Port 80 block if the block is enabled; the interrupt is enabled or disabled in the Interrupt Aggregator.

42.8 Low Power Modes

The Port 80 block may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

42.9 Description

FIGURE 42-2: PORT 80 BLOCK DIAGRAM



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The Port 80 BIOS Debug Port consists of a 32-bit wide x 16 deep FIFO and a 24-bit free running timer. Host and EC access to the Port 80 device is through a set of registers. The Host can write the FIFO via the Runtime Registers and the EC can read the FIFO can control the device via the EC Registers.

Writes to the Host Data Register are concatenated with the 24-bit timestamp and written to the FIFO. Reads of the Host Data Register return zero. If writes to the Host Data Register overrun the FIFO, the oldest data are discarded and the OVERRUN status bit in the Status Register is asserted.

Only the EC can read data from the FIFO, using the EC Data Register. The use of this data is determined by EC Firmware alone.

42.10 Configuration Registers

Configuration Registers for an instance of the Port 80 BIOS Debug Port are listed in the following table. Host access to Configuration Registers is through the Configuration Port using the Logical Device Number of each instance of the Port 80 BIOS Debug Port and the Index shown in the “Host Index” column of the table. The EC can access Configuration Registers directly. The EC address for each register is formed by adding the Base Address for each instance of the Port 80 BIOS Debug Port shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the “EC Offset” column.

TABLE 42-1: CONFIGURATION REGISTER SUMMARY

EC Offset	Host Index	Register Name
330h	30h	Activate Register

42.10.1 ACTIVATE REGISTER

Offset	330h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	ACTIVATE When this bit is asserted ‘1’, the block is enabled. When this bit is ‘0’, writes by the Host interface to the Host Data Register are not claimed, the FIFO is flushed, the 24-bit Timer is reset, and the timer clock is stopped. Control bits in the Configuration Register are not affected by the state of ACTIVATE.	R/W	0h	RESET_SYS

42.11 Runtime Registers

The registers listed in the Runtime Register Summary table are for a single instance of the Port 80 BIOS Debug Port. Host access for each register listed in this table is defined as an offset in the Host address space to the Block’s Base Address, as defined by the instance’s Base Address Register.

The EC address for each register is formed by adding the Base Address for each instance of the Port 80 BIOS Debug Port shown in the Block Overview and Base Address Table in Section 3.0, "Device Inventory" to the offset shown in the “Offset” column.

TABLE 42-2: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	Host Data Register

42.11.1 HOST DATA REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	HOST_DATA	W	0h	RESET_SYS

42.12 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for each instance of the Port 80 BIOS Debug Port Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 42-3: EC REGISTER SUMMARY

Offset	Register Name
100h	EC Data Register
104h	Configuration Register
108h	Status Register
10Ch	Count Register

42.12.1 EC DATA REGISTER

Offset	100h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	TIME_STAMP	R	0h	RESET_SYS
7:0	EC_DATA	R	0h	RESET_SYS

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42.12.2 CONFIGURATION REGISTER

Offset	104h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:6	FIFO_THRESHOLD This field determines the threshold for the Port 80 BIOS Debug Port Interrupts. 3=14 entry threshold 2=8 entry threshold 1=4 entry threshold 0=1 entry threshold	R/W	0h	RESET_SYS
5	TIMER_ENABLE When the TIMER_ENABLE bit is '1', the 24-bit Timer is actively counting at a rate determined by the TIMEBASE_SELECT bits. When the TIMER ENABLE bit is '0', counting is stopped.	R/W	0h	RESET_SYS
4:3	TIMEBASE_SELECT The TIMEBASE SELECT bits determine the clock for the 24-bit Timer. 3=48MHz/64 2=48MHz/32 1=48MHz/16 0=48MHz/8	R/W	0h	RESET_SYS
2	RESET_TIMESTAMP When this field is written with a '1', the 24-bit Timer is reset to '0'. Writing zero to the Count Register has the same effect. Writes of a '0' to this field have no effect. Reads always return '0'.	W	-	RESET_SYS
1	FLUSH When this field is written with a '1', the FIFO is flushed. Writes of a '0' to this field have no effect. Reads always return '0'.	W	-	RESET_SYS
0	Reserved	R	-	-

42.12.3 STATUS REGISTER

Offset	108h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	OVERRUN The OVERRUN bit is ‘1’ when the host writes the Host Data Register when the FIFO is full.	R	0h	RESET_SYS
0	NOT_EMPTY The NOT EMPTY bit is ‘1’ when there is data in the FIFO. The NOT EMPTY bit is ‘0’ when the FIFO is empty.	R	0h	RESET_SYS

42.12.4 COUNT REGISTER

Offset	10Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
32:8	COUNT Writes load data into the 24-bit Timer. Reads return the 24-bit Timer current value.	R/W	0h	–
7:0	Reserved	R	-	-

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43.0 VBAT-POWERED CONTROL INTERFACE

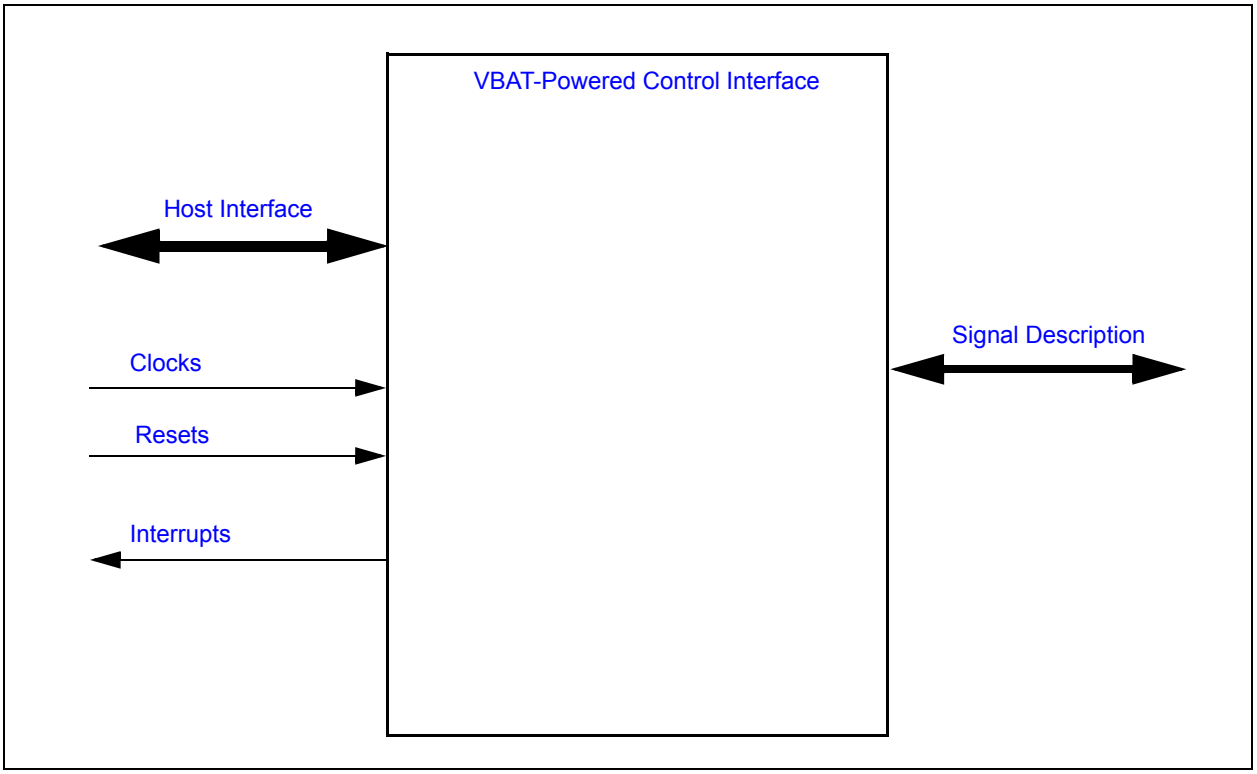
43.1 General Description

The VBAT-Powered Control Interface has VBAT-powered combinational logic and input and output signal pins. The block interfaces with the Real Time Clock as well as the Week Alarm.

43.2 Interface

This block's connections are entirely internal to the chip.

FIGURE 43-1: I/O DIAGRAM OF BLOCK



43.3 Signal Description

TABLE 43-1: EXTERNAL SIGNAL DESCRIPTION

Name	Direction	Description
VCI_OUT	OUTPUT	Output status driven by this block.

TABLE 43-2: INTERNAL SIGNAL DESCRIPTION

Name	Direction	Description
Week_Alarm	INPUT	Signal from the Week Timer block. The alarm is asserted by the timer when the Week_Alarm Power-Up Output is asserted
RTC_Alarm	INPUT	Signal from the Real Time Clock block. The alarm is asserted by the RTC when the RTC_ALRM signal is asserted.
VTR_PWRGD	INPUT	Status signal for the state of the VTR power rail. This signal is high if the power rail is on, and low if the power rail is off.

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43.4 Host Interface

The registers defined for the VBAT-Powered Control Interface are accessible only by the EC.

43.5 Power, Clocks and Resets

This section defines the Power, Clock, and Reset parameters of the block.

43.5.1 POWER DOMAINS

Name	Description
VBAT	This power well sources all of the internal registers and logic in this block.
VTR	This power well sources only bus communication. The block continues to operate internally while this rail is down.

43.5.2 CLOCKS

This block does not require clocks.

43.5.3 RESETS

Name	Description
RESET_VBAT	This reset signal is used reset all of the registers and logic in this block.
RESET_SYS	This reset signal is used to inhibit the bus communication logic, and isolates this block from VTR powered circuitry on-chip. Otherwise it has no effect on the internal state.

43.6 Interrupts

Source	Description
VCI_IN[4:0]	These interrupts are routed to the Interrupt Controller They are only asserted when both VBAT and VTR are powered. Edge detection and assertion level for the interrupt are configured in the GPIO Pin Control Registers for the GPIOs that shares pins with VCI_IN# inputs. The interrupts are equivalent to the GPIO interrupts for the GPIOs that share the pins, but appear on different registers in the Interrupt Aggregator.

43.7 Low Power Modes

The VBAT-powered Control Interface has no low-power modes. It runs continuously while the VBAT well is powered.

43.8 General Description

The VBAT-Powered Control Interface (VCI) is used to drive the VCI_OUT pin. The output pin can be controlled either by VBAT-powered inputs, or by firmware when the VTR is active and the EC is powered and running. When the VCI_OUT pin is controlled by hardware, either because VTR is inactive or because the VCI block is configured for hardware control, the VCI_OUT pin can be asserted by a number of inputs:

- When one or more of the VCI_INx# pins are asserted. By default, the VCI_IN# pins are active low, but firmware can switch each input individually to an active-high input. See Section 43.8.1, "Input Polarity".
- When the Week Alarm from the Week Alarm Interface is asserted
- When the RTC Alarm from the Real Time Clock is asserted

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Firmware can configure which of the hardware pin inputs contribute to the VCI_OUT output by setting the enable bits in the VCI Input Enable Register. Even if the input pins are not configured to affect VCI_OUT, firmware can monitor their current state through the status bits in the VCI Register. Firmware can also enable EC interrupts from the state of the input pins.

Each of the VCI_IN# pins can be configured for additional properties.

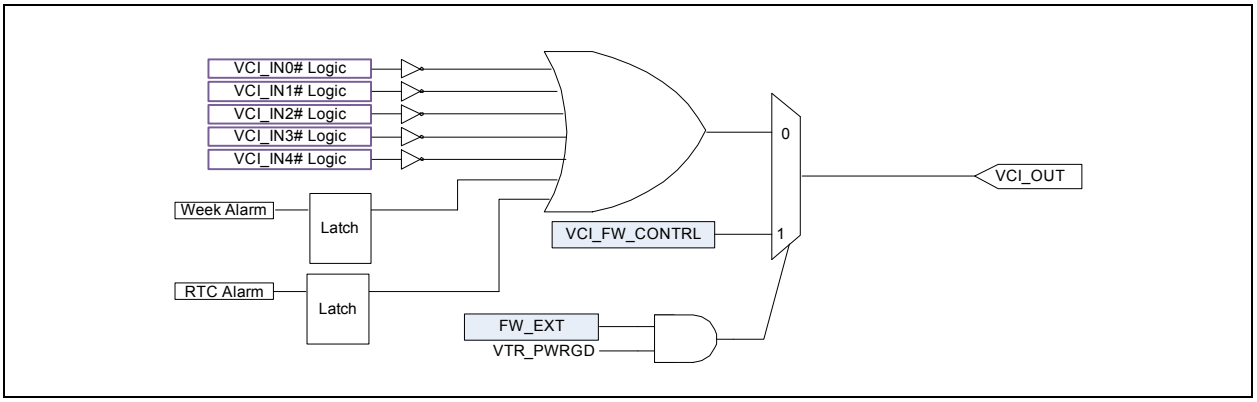
- By default, each of the VCI_IN# pins have an input glitch filter. All glitch filters can be disabled by the FILTERS_BYPASS bit in the VCI Register
- Assertions of each of the VCI_IN# pins can optionally be latched, so hardware can maintain the assertion of a VCI_IN# even after the physical pin is de-asserted, or so that firmware can determine which of the VCI_IN# inputs contributed to VCI_OUT assertion. See the Latch Enable Register and the Latch Resets Register.
- Rising edges and falling edges on the VCI_IN# pins are latched, so firmware can detect transitions on the VCI_IN# pins even if the transitions occurred while EC power was not available. See Section 43.8.2, "Edge Event Status".

If none of the additional properties are required, firmware can disable a VCI_IN# pin completely, by clearing both the corresponding bit in the VCI Input Enable Register and the corresponding bit in the VCI Buffer Enable Register. When both bits are '0', the input is disabled and will not be a drain on the VBAT power rail.

When VTR power is present and the EC is operating, firmware can configure the VCI_OUT pin to operate as a general-purpose output pin. The VCI_OUT pin is firmware-controlled when the FW_EXT bit in the VCI Register is '1'. When firmware is controlling the output, the state of VCI_OUT is defined by the VCI_FW_CNTRL bit in the same register. When VTR is not present (the VTR_PWRGD input is low), the VCI_OUT pin is also determined by the hardware circuit.

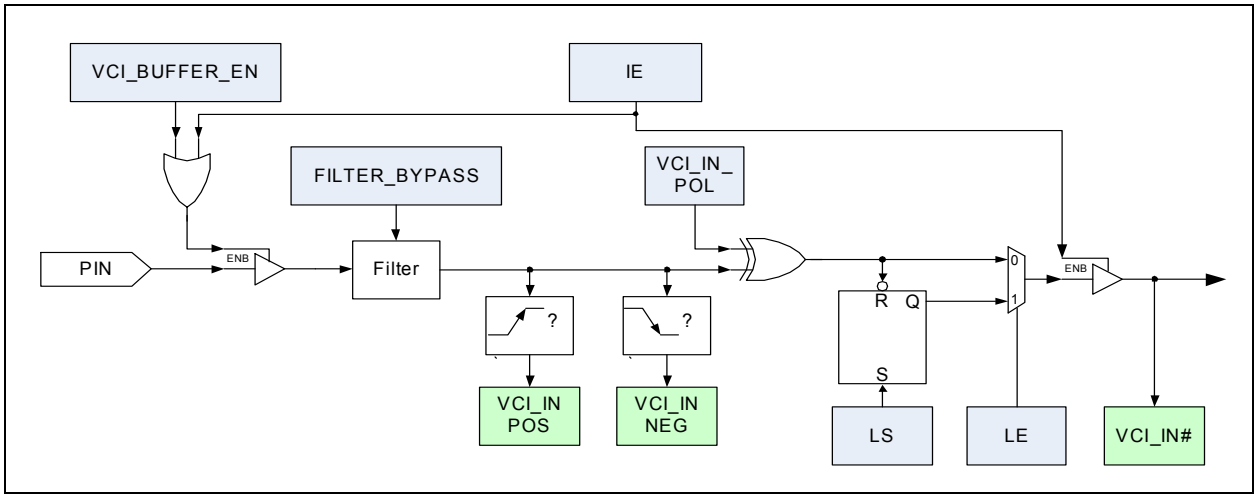
The following figures illustrate the VBAT-Power Control Interface logic:

FIGURE 43-2: VBAT-POWERED CONTROL INTERFACE BLOCK DIAGRAM



The VCI_INx# Logic in the block diagram is illustrated in the following figure:

FIGURE 43-3: VBAT-POWERED CONTROL INTERFACE BLOCK DIAGRAM



43.8.1 INPUT POLARITY

The VCI_IN# pins have an optional polarity inversion. The inversion takes place after any input filtering and before the VCI_IN signals are latched in the VCI_IN# status bits in the VCI Register. Edge detection occurs before the polarity inversion. The inversion is controlled by battery-backed configuration bits in the VCI Polarity Register.

43.8.2 EDGE EVENT STATUS

Each VCI_IN# input pin is associated with two register bits used to record edge transitions on the pins. The edge detection takes place after any input filtering, before polarity control and occurs even if the VCI_IN# input is not enabled as part of the VCI_OUT logic (the corresponding control bit in the VCI Input Enable Register is '0') or if the state of the VCI_IN# input is not latched (the corresponding control bit in the Latch Enable Register is '0'). One bit is set whenever there is a high-to-low transition on the VCI_IN# pin (the VCI Negedge Detect Register) and the other bit is set whenever there is a low-to-high transition on the VCI_IN# pin (the VCI Posedge Detect Register).

In order to minimize power drain on the VBAT circuit, the edge detection logic operates only when the input buffer for a VCI_IN# pin is enabled. The input buffer is enabled either when the VCI_IN# pin is configured to determine the VCI_OUT pin, as controlled by the VCI_IN[1:0]# field of the VCI Register, or when the input buffer is explicitly enabled in the VCI Input Enable Register. When the pins are not enabled transitions on the pins are ignored.

43.8.3 VCI PIN MULTIPLEXING

Each of the VCI inputs, as well as VCI_OUT, are multiplexed with standard VTR-powered GPIOs. When VTR power is off, the mux control is disabled and the pin always reverts to the VCI function. The VCI_IN# function should be disabled in the VCI Input Enable Register VCI Buffer Enable Register and for any pin that is intended to be used as a GPIO rather than a VCI_IN#, so that VCI_OUT is not affected by the state of the pin.

43.8.4 APPLICATION EXAMPLE

For this example, a mobile platform configures the VBAT-Powered Control Interface (VCI) as follows:

- VCI_IN0# is wired to a power button on the mobile platform
- VCI_IN1# is wired to a power button on a dock
- The VCI_OUT pin is connected to the regulator that sources the VTR power rail, the rail which powers the EC

The VCI can be used in a system as follows:

1. In the initial condition, there is no power on either the VTR or VBAT power rails. All registers in the VCI are in an indeterminate state
2. A coin cell battery is installed, causing a RESET_VBAT. All registers in the interface are forced to their default conditions. The VCI_OUT pin is driven by hardware, input filters on the VCI_IN# pins are enabled, the VCI_IN# pins are all active low, all VCI inputs are enabled and all edge and status latches are in their non-asserted state

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3. The power button on VCI_IN0# is pushed. This causes VCI_OUT to be asserted, powering the VTR rail. This causes the EC to boot and start executing EC firmware
4. The EC changes the VCI configuration so that firmware controls the VCI_OUT pin, and sets the output control so that VCI_OUT is driven high. With this change, the power button can be released without removing the EC power rail.
5. EC firmware re-configures the VCI logic so that the VCI_IN# input latches are enabled. This means that subsequent presses of the power button do not have to be held until EC firmware switches the VCI logic to firmware control
6. During this phase the VCI_OUT pin is driven by the firmware-controlled state bit and the VCI input pins are ignored. However, the EC can monitor the state of the pins, or generate inputs when their state changes
7. At some later point, EC firmware must enter a long-term power-down state.
   - Firmware configures the Week Timer for a Week Alarm once every 8 hours. This will turn on the EC power rail three times a day and enable the EC to perform low frequency housekeeping tasks even in its lowest-power state
   - Firmware de-asserts VCI_OUT. This action kills power to the EC and automatically returns control of the VCI_OUT pin to hardware.
   - The EC will remain in its lowest-power state until a power pin is pushed, AC power is connected, or the Sub-Week Alarm is active

43.9 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the VBAT-Powered Control Interface Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 43-3: REGISTER SUMMARY

EC OFFSET	REGISTER NAME
00h	VCI Register
04h	Latch Enable Register
08h	Latch Resets Register
0Ch	VCI Input Enable Register
10h	Reserved
14h	VCI Polarity Register
18h	VCI Posedge Detect Register
1Ch	VCI Negedge Detect Register
20h	VCI Buffer Enable Register

43.9.1 VCI REGISTER

Offset	00h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:18	Reserved	R	-	-
17	RTC_ALRM If enabled by RTC_ALRM_LE, this bit is set to '1' if the RTC Alarm signal is asserted. It is reset by writes to RTC_ALRM_LS.	R	0	RESET_VBAT
16	WEEK_ALRM If enabled by WEEK_ALRM_LE, this bit is set to '1' if the Week Alarm signal is asserted. It is reset by writes to WEEK_ALRM_LS.	R	0	RESET_VBAT
15:13	Reserved	R	-	-
Note 1:	The VCI_IN[6:0]# bits default to the state of their respective input pins. The VCI_OUT bit is determined by the VCI hardware circuit			

Offset	00h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
12	FILTERS_BYPASS The Filters Bypass bit is used to enable and disable the input filters on the VCI_IN# pins. See Section 47.17, "VBAT-Powered Control Interface Timing". 1=Filters disabled 0=Filters enabled (default)	R/W	0	RESET_VBAT
11	FW_EXT This bit controls selecting between the external VBAT-Powered Control Interface inputs, or the VCI_FW_CNTRL bit output to control the VCI_OUT pin. 1=VCI_OUT is determined by the VCI_FW_CNTRL field, when VTR is active **Note:** 0=VCI_OUT is determined by the external inputs.	R/W	0	RESET_SYS and RESET_VBAT
10	VCI_FW_CNTRL This bit can allow EC firmware to control the state of the VCI_OUT pin. For example, when VTR_PWRGD is asserted and the FW_EXT bit is '1', clearing the VCI_FW_CNTRL bit de-asserts the active high VCI_OUT pin. BIOS must set this bit to '1' prior to setting the FW_EXT bit to '1' on power up, in order to avoid glitches on the VCI_OUT pin.	R/W	0	RESET_SYS and RESET_VBAT
9	VCI_OUT This bit provides the current status of the VCI_OUT pin.	R	See Note 1	–
8:7	Reserved	R	-	-
6:0	VCI_IN# These bits provide the latched state of the associated VCI_IN# pin, if latching is enabled or the current state of the pin if latching is not enabled. In both cases, the value is determined after the action of the VCI Polarity Register.	R	See Note 1	
Note 1:	The VCI_IN[6:0]# bits default to the state of their respective input pins. The VCI_OUT bit is determined by the VCI hardware circuit			

43.9.2 LATCH ENABLE REGISTER

Offset	04h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:18	Reserved	R	-	-
17	RTC_ALRM_LE Latch enable for the RTC Power-Up signal. 1=Enabled. Assertions of the RTC Alarm are held until the latch is reset by writing the correspondingLS bit 0=Not Enabled. The RTC Alarm signal is not latched but passed directly to the VCI_OUT logic	R/W	0h	RESET_VBAT

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Offset	04h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
16	WEEK_ALRM_LE Latch enable for the Week Alarm Power-Up signal. 1=Enabled. Assertions of the Week Alarm are held until the latch is reset by writing the correspondingLS bit 0=Not Enabled. The Week Alarm signal is not latched but passed directly to the VCI_OUT logic	R/W	0h	RESET_VBAT
15:7	Reserved	R	-	-
6:0	LE Latching Enables. Latching occurs after the Polarity configuration, so a VCI_IN# pin is asserted when it is ‘0’ if VCI_IN_POL is ‘0’, and asserted when it is ‘1 ‘if VCI_IN_POL is ‘1’. For each bit in the field: 1=Enabled. Assertions of the VCI_IN# pin are held until the latch is reset by writing the corresponding LS bit 0=Not Enabled. The VCI_IN# signal is not latched but passed directly to the VCI_OUT logic	R/W	30h	RESET_VBAT

43.9.3 LATCH RESETS REGISTER

Offset	08h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:18	Reserved	R	-	-
17	RTC_ALRM_LS RTC Alarm Latch Reset. When this bit is written with a ‘1’, the RTC Alarm Event latch is reset The RTC Alarm input to the latch has priority over the Reset input Reads of this register are undefined.	W	-	–
16	WEEK_ALRM_LS Week Alarm Latch Reset. When this bit is written with a ‘1’, the Week Alarm Event latch is reset The Week Alarm input to the latch has priority over the Reset input Reads of this register are undefined.	W	-	–
15:7	Reserved	R	-	-

Offset	08h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
6:0	LS Latch Resets. When a Latch Resets bit is written with a '1', the corresponding VCI_IN# latch is de-asserted ('1'). The VCI_IN# input to the latch has priority over the Latch Reset input, so firmware cannot reset the latch while the VCI_IN# pin is asserted. Firmware should sample the state of the pin in the VCI Register before attempting to reset the latch. As noted in the Latch Enable Register, the assertion level is determined by the VCI_IN_POL bit. Reads of this register are undefined.	W	–	–

43.9.4 VCI INPUT ENABLE REGISTER

Offset	0Ch			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:7	Reserved	R	-	-
6:0	IE Input Enables for VCI_IN# signals. After changing the input enable for a VCI input, firmware should reset the input latch and clear any potential interrupt that may have been triggered by the input, as changing the enable may cause the internal status to change. For each bit in the field: 1=Enabled. The corresponding VCI_IN# input is not gated and toggling the pin will affect the VCI_OUT pin 0=Not Enabled. the corresponding VCI_IN# input does not affect the VCI_OUT pin, even if the input is '0.' Unless the corresponding bit in the VCI Buffer Enable Register is 1, latches are not asserted, even if the VCI_IN# pin is low, during a VBAT power transition	R/W	Fh	RESET_VBAT

43.9.5 VCI POLARITY REGISTER

Offset	14h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:7	Reserved	R	-	-
6:0	VCI_IN_POL These bits determine the polarity of the VCI_IN input signals: For each bit in the field: 1=Active High. The value on the pins is inverted before use 0=Active Low (default)	RW	0	RESET_VBAT

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43.9.6 VCI POSEDGE DETECT REGISTER

Offset	18h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:7	Reserved	R	-	-
6:0	VCI_IN_POS These bits record a low to high transition on the VCI_IN# pins. A “1” indicates a transition occurred. For each bit in the field: 1=Positive Edge Detected 0=No edge detected	R/WC	0	RESET_VBAT

43.9.7 VCI NEGEDGE DETECT REGISTER

Offset	1Ch			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:7	Reserved	R	-	-
6:0	VCI_IN_NEG These bits record a high to low transition on the VCI_IN# pins. A “1” indicates a transition occurred. For each bit in the field: 1=Negative Edge Detected 0=No edge detected	R/WC	0	RESET_VBAT

43.9.8 VCI BUFFER ENABLE REGISTER

Offset	20h			
Bits	**DESCRIPTION**	**TYPE**	**DEFAULT**	**RESET EVENT**
31:7	Reserved	R	-	-
6:0	VCI_BUFFER_EN Input Buffer enable. After changing the buffer enable for a VCI input, firmware should reset the input latch and clear any potential interrupt that may have been triggered by the input, as changing the buffer may cause the internal status to change. This register has no effect when VTR is powered. When VTR is on, the input buffers are enabled only by the IE bit. For each bit in the field: 1=VCI_IN# input buffer enabled independent of the IE bit. The edge detection latches for this input are always enabled 0=VCI_IN# input buffer enabled by the IE bit. The edge detection latches are only enabled when the IE bit is '1' (default)	RW	0	RESET_VBAT

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44.0 VBAT-POWERED RAM

44.1 Overview

The VBAT Powered RAM provides a 128 Byte Random Accessed Memory that is operational while the main power rail is operational, and will retain its values powered by battery power while the main rail is unpowered.

44.2 References

No references have been cited for this feature.

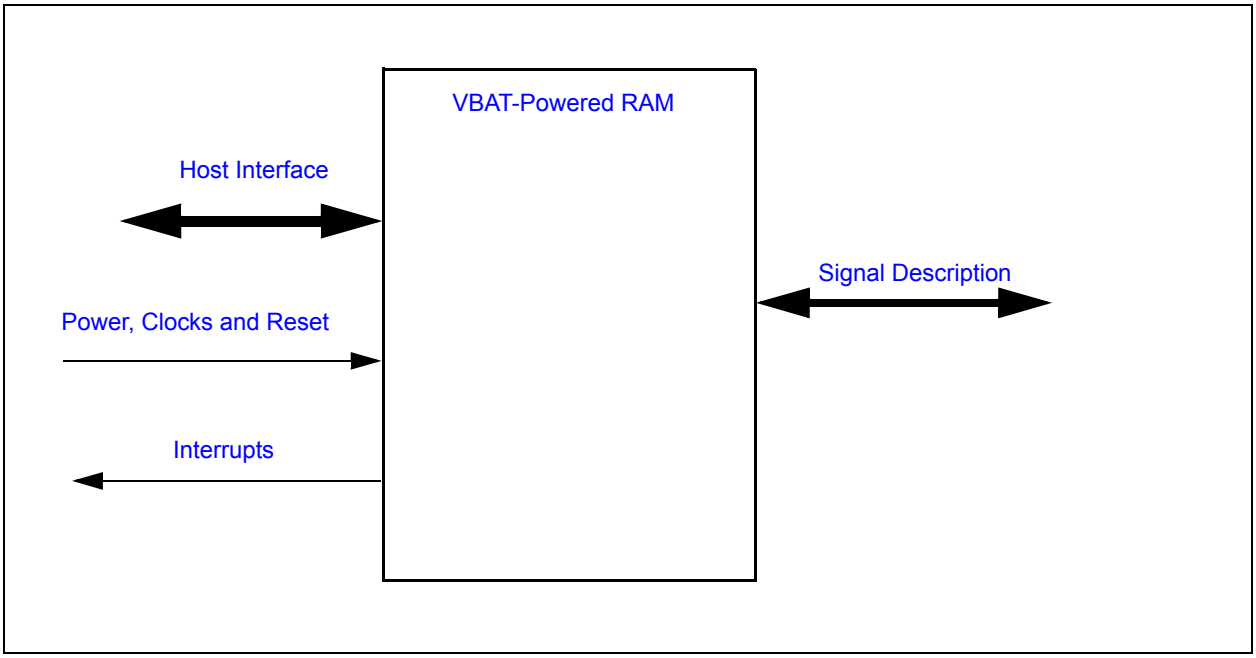
44.3 Terminology

There is no terminology defined for this section.

44.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 44-1: I/O DIAGRAM OF BLOCK



44.5 Signal Description

There are no external signals for this block.

44.6 Host Interface

The contents of the VBAT RAM are accessible to the EC over the Host Interface.

44.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

44.7.1 POWER DOMAINS

Name	Description
VTR	The main power well used when the VBAT RAM is accessed by the EC.
VBAT	The power well used to retain memory state while the main power rail is unpowered.

44.7.2 CLOCK INPUTS

No special clocks are required for this block.

44.7.3 RESETS

Name	Description
RESET_VBAT	This signal resets all the registers and logic in this block to their default state.

44.8 Interrupts

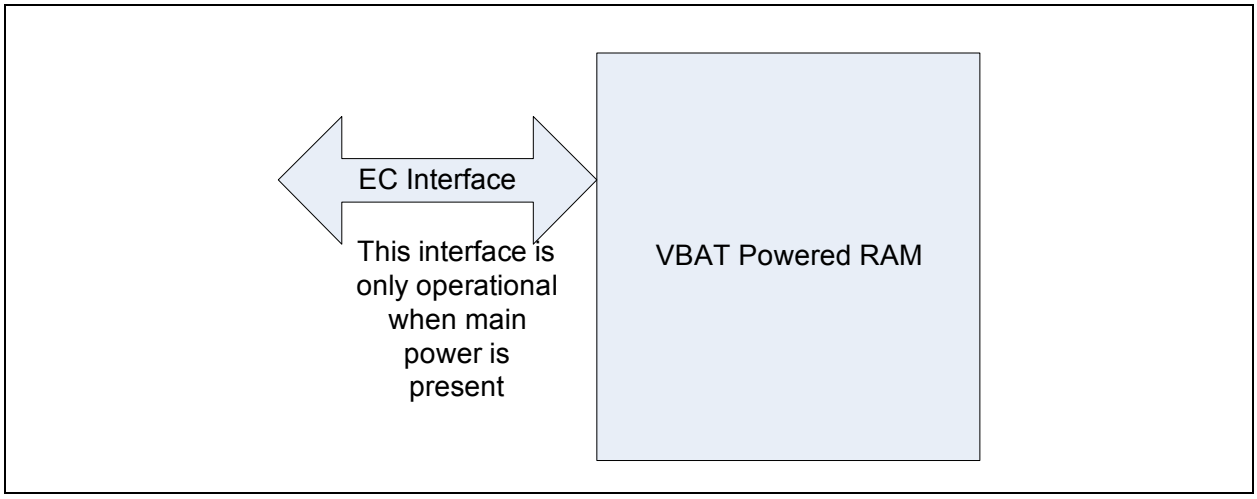
This block does not generate any interrupts.

44.9 Low Power Modes

The VBAT-Powered RAM automatically enters a low power mode whenever it is not being accessed by the EC. There is no chip-level Sleep Enable input.

44.10 Description

FIGURE 44-2: VBAT RAM BLOCK DIAGRAM



The VBAT Powered RAM provides a 128 Byte Random Accessed Memory that is operational while VTR is powered, and will retain its values powered by VBAT while VTR is unpowered. The RAM is organized as a 32 words x 32-bit wide for a total of 128 bytes.

The contents of the VBAT RAM is indeterminate after a RESET_VBAT.

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45.0 VBAT REGISTER BANK

45.1 Introduction

This chapter defines a bank of registers powered by VBAT.

45.2 Interface

This block is designed to be accessed internally by the EC via the register interface.

45.3 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

45.3.1 POWER DOMAINS

Name	Description
VBAT	The VBAT Register Bank are all implemented on this single power domain.

45.3.2 CLOCK INPUTS

This block does not require any special clock inputs. All register accesses are synchronized to the host clock.

45.3.3 RESETS

Name	Description
RESET_VBAT	This reset signal, which is an input to this block, resets all the logic and registers to their initial default state.

45.4 Interrupts

This block does not generate any interrupt events.

45.5 Low Power Modes

The VBAT Register Bank is designed to always operate in the lowest power consumption state.

45.6 Description

The VBAT Register Bank block is a block implemented for aggregating miscellaneous battery-backed registers required the host and by the Embedded Controller (EC) Subsystem that are not unique to a block implemented in the EC subsystem.

45.7 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the VBAT Register Bank Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 45-1: REGISTER SUMMARY

Offset	Register Name
00h	Power-Fail and Reset Status Register
04h	TEST
08h	Clock Enable Register
0Ch	TEST
10h	TEST
14h	TEST

TABLE 45-1: REGISTER SUMMARY (CONTINUED)

Offset	Register Name
1Ch	TEST
20h	Monotonic Counter Register
24h	Counter HiWord Register
28h	VWire Backup Register
2Ch	TEST

45.7.1 POWER-FAIL AND RESET STATUS REGISTER

The Power-Fail and Reset Status Register collects and retains the VBAT RST and WDT event status when VTR is unpowered.

Address	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	VBAT_RST The VBAT_RST bit is set to '1' by hardware when a RESET_VBAT is detected. This is the register default value. To clear VBAT RST EC firmware must write a '1' to this bit; writing a '0' to VBAT RST has no affect.	R/WC	1	RESET_VBAT
6	SYSRESETREQ This bit is set to '1b' if a RESET_SYS was triggered by an ARM SYSRESETREQ event. This bit is cleared to '0b' when written with a '1b'; writes of a '0b' have no effect.	R/WC	-	-
5	WDT This bit is set to '1b' if a RESET_SYS was triggered by a Watchdog Timer event. This bit is cleared to '0b' when written with a '1b'; writes of a '0b' have no effect.	R/WC	0	RESET_VBAT
4	RESETI This bit is set to '1b' if a RESET_SYS was triggered by a low signal on the RESETI# input pin. This bit is cleared to '0b' when written with a '1b'; writes of a '0b' have no effect.	R/WC	0	RESET_VBAT
3	TEST	R/WC	0	RESET_VBAT
2	SOFT_SYS_RESET Status This bit is set to '1b' if a was triggered by an assertion of the SOFT-_SYS_RESET bit in the System Reset Register. This bit is cleared to '0b' when written with a '1b'; writes of a '0b' have no effect.	R/WC	0	RESET_VBAT
1	Reserved	R	0	RESET_VBAT
0	Reserved	R	-	-

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45.7.2 CLOCK ENABLE REGISTER

Address	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	-
3	XOSEL This bit selects between a single-ended clock source for the crystal oscillator or an external parallel crystal. 1=The crystal oscillator is driven by a single-ended 32KHz clock source connected to the XTAL2 pin 0=The crystal oscillator requires a 32KHz parallel resonant crystal connected between the XTAL1 and XTAL2 pins	R/W	0b	RESET_VBAT
2	32KHZ_SOURCE This field determines the source for the always-on 32KHz internal clock source. If set to '1b', this bit will only take effect if an active clock has been detected on the crystal pins. Once the 32KHz source has been switched, activity detection on the crystal no longer functions. Therefore, if the crystal oscillator uses a single-ended input, once started that input must not stop while this bit is '1b'. 1=Crystal Oscillator. The selection between a singled-ended input or a resonant crystal is determined by XOSEL in this register 0=Silicon Oscillator	R/W	0b	RESET_VBAT
1	EXT_32K This bit selects the source for the 32KHz clock domain. 1=The 32KHZ_IN VTR-powered pin is used as a source for the 32KHz clock domain. If an activity detector does not detect a clock on the selected source, the always-on 32KHz internal clock source is automatically selected 0=The always-on32Khz clock source is used as the source for the 32KHz clock domain	R/W	0b	RESET_VBAT
0	32K_SUPPRESS 1=32KHz clock domain is off while VTR is off (i.e., while on VBAT only). The 32KHz domain is always on while VTR is on, so the PLL always has a reference 0=32KHz clock domain is enabled while VTR is off (i.e., while on VBAT only). The clock source for the 32KHz domain is determined by the other bits in this register	R/W	0b	RESET_VBAT

45.7.3 MONOTONIC COUNTER REGISTER

Address	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	MONOTTONIC_COUNTER Read-only register that increments by 1 every time it is read. It is reset to 0 on a VBAT Power On Reset.	R	0b	RESET_VBAT

45.7.4 COUNTER HIWORD REGISTER

Address	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COUNTER_HIWORD Thirty-two bit read/write register. If software sets this register to an incrementing value, based on an external non-volatile store, this register may be combined with the Monotonic Counter Register to form a 64-bit monotonic counter.	R/W	0b	RESET_VBAT

45.7.5 VWIRE BACKUP REGISTER

Address	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:4	M2S_42H_BACKUP The Boot ROM firmware will copy this field into the SRC3 to SRC0 bits of the Master-to-Slave Virtual Wire Register that corresponds to Virtual Wire Index 42h on a RESET_SYS. If software always saves the state of the Index 42h SRC bits on the falling edge of the SUSWARN# virtual wire, the state of the four SRC bits will be synchronized to the state of the four bits in the core logic.	R/W	0b	RESET_VBAT
3:0	M2S_2H_BACKUP The Boot ROM firmware will copy this field into the SRC3 to SRC0 bits of the Master-to-Slave Virtual Wire Register that corresponds to Virtual Wire Index 2h on a RESET_SYS. If software always saves the state of the Index 2h SRC bits on the falling edge of the SUSWARN# virtual wire, the state of the four SRC bits will be synchronized to the state of the four bits in the core logic.	R/W	0b	RESET_VBAT

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46.0 EC SUBSYSTEM REGISTERS

46.1 Introduction

This chapter defines a bank of registers associated with the EC Subsystem.

46.2 References

None

46.3 Interface

This block is designed to be accessed internally by the EC via the register interface.

46.4 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

46.4.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

46.4.2 CLOCK INPUTS

This block does not require any special clock inputs. All register accesses are synchronized to the host clock.

46.4.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state, except WDT Event Count Register.
RESET_SYS_nWDT	This signal resets the WDT Event Count Register register. This reset is not asserted on a WDT Event.
RESET_VTR	This reset signal is asserted only on VTR power on.

46.5 Interrupts

This block does not generate any interrupt events.

46.6 Low Power Modes

The EC Subsystem Registers may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry. When this block is commanded to sleep it will still allow read/write access to the registers.

46.7 Description

The EC Subsystem Registers block is a block implemented for aggregating miscellaneous registers required by the Embedded Controller (EC) Subsystem that are not unique to a block implemented in the EC subsystem.

46.8 EC-Only Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the EC Subsystem Registers Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 46-1: REGISTER SUMMARY

Offset	Register Name
00h	SRAM Configuration Register
04h	AHB Error Address Register
08h	TEST
0Ch	TEST
10h	TEST
14h	AHB Error Control Register
18h	Interrupt Control Register
1Ch	ETM TRACE Enable Register
20h	Debug Enable Register
24h	OTP Lock Register
28h	WDT Event Count Register
2Ch	AES HASH Byte Swap Control Register
30h	TEST
34h	TEST
38h	Reserved
3Ch	TEST
40h	PECI Disable Register
44h	TEST
48h	TEST
5Ch	Crypto Soft Reset Register
60h	TEST
64h	GPIO Bank Power Register
68h	TEST
6Ch	TEST
70h	JTAG Master Configuration Register
74h	JTAG Master Status Register
78h	JTAG Master TDO Register
7Ch	JTAG Master TDI Register
80h	JTAG Master TMS Register
84h	JTAG Master Command Register
90h	TEST
100h	TEST

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46.8.1 SRAM CONFIGURATION REGISTER

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1:0	SRAM_SIZE 3=480KB total (Code=416KB; DATA=64KB). Code RAM starts at address B0000h and extends to 117FFFh. Data RAM starts at 118000h and extends to 127FFFh 2=320KB total (Code=288KB; DATA=32KB). Code RAM starts at address D0000h and extends to 117FFFh. Data RAM starts at 118000h and extends to 11FFFFh 1=256KB total (Code=224KB; DATA=32KB). Code RAM starts at address E0000h and extends to 117FFFh. Data RAM starts at 118000h and extends to 11FFFh 0=Reserved	R	0h	RESET_SYS

46.8.2 AHB ERROR ADDRESS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	AHB_ERR_ADDR In priority order: 1. AHB address is registered when an AHB error occurs on the processors AHB master port and the register value was already 0. This way only the first address to generate an exception is captured. 2. The processor can clear this register by writing any 32-bit value to this register.	R/WZC	0h	RESET_SYS

46.8.3 AHB ERROR CONTROL REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	-	-
1	TEST	R/W	0h	RESET_SYS
0	AHB_ERROR_DISABLE 1=EC memory exceptions are disabled 0=EC memory exceptions are enabled	R/W	0h	RESET_SYS

46.8.4 INTERRUPT CONTROL REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	NVIC_EN This bit enables Alternate NVIC IRQ's Vectors. The Alternate NVIC Vectors provides each interrupt event with a dedicated (direct) NVIC vector. 1=Alternate NVIC vectors enabled 0=Alternate NVIC vectors disabled	R/W	1b	RESET_SYS

46.8.5 ETM TRACE ENABLE REGISTER

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	TRACE_EN This bit enables the ARM TRACE debug port (ETM/ITM). The Trace Debug pins are forced to the TRACE functions. 1=ARM TRACE port enabled 0=ARM TRACE port disabled	R/W	0b	RESET_SYS

46.8.6 DEBUG ENABLE REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3	DEBUG_PU_EN If this bit is set to '1b' internal pull-up resistors are automatically enabled on the appropriate debugging port wires whenever the debug port is enabled (the DEBUG_EN bit in this register is '1b' and the JTAG_RST# pin is high). The setting of DEBUG_PIN_CFG determines which pins have pull-ups enabled when the debug port is enabled.	R/W	0h	RESET_SYS

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Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2:1	DEBUG_PIN_CFG This field determines which pins are affected by the TRST# debug enable pin. 3=Reserved 2=The pins associated with the JTAG TCK and TMS switch to the debug interface when TRST# is de-asserted high. The pins associated with TDI and TDO remain controlled by the associated GPIO. This setting should be used when the ARM Serial Wire Debug (SWD) is required for debugging and the Serial Wire Viewer is not required 1=The pins associated with the JTAG TCK, TMS and TDO switch to the debug interface when TRST# is de-asserted high. The pin associated with TDI remains controlled by the associated GPIO. This setting should be used when the ARM Serial Wire Debug (SWD) and Serial Wire Viewer (SWV) are both required for debugging 0=All four pins associated with JTAG (TCK, TMS, TDI and TDO) switch to the debug interface when TRST# is de-asserted high. This setting should be used when the JTAG TAP controller is required for debugging	R/W	0h	RESET_SYS
0	DEBUG_EN This bit enables the JTAG/SWD debug port. 1=JTAG/SWD port enabled. A high on TRST# enables JTAG or SWD, as determined by SWD_EN 0=JTAG/SWD port disabled. JTAG/SWD cannot be enabled (the TRST# pin is ignored and the JTAG signals remain in their non-JTAG state)	R/W	0b	RESET_SYS

46.8.7 OTP LOCK REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:5	Reserved	R	-	-
4	PUBLIC_KEY_LOCK This bit controls access to the Public Key region of the eFuse memory, bytes 128 to 191. Once written, this bit becomes Read Only. If the JTAG_EN bit is 1 (enabled), the Public Key is inaccessible, independent of the state of this bit. 1=The Public Key is inaccessible (i.e, always returns 0 or 1 for every bit) 0=The Public Key is accessible	R/W / R	0b	RESET_SYS

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
3	USER_OTP_LOCK This bit controls access to the User region of the eFuse memory, bytes 192 to 511. Once written, this bit becomes Read Only. If the JTAG_EN bit is 1 (enabled), the User region is inaccessible, independent of the state of this bit. 1=The User region is inaccessible (i.e, always returns 0 or 1 for every bit) 0=The User region is accessible	R/W / R	0b	RESET_SYS
2	PRIVATE_KEY_LOCK This bit controls access to Private Key region of the eFuse memory, bytes 0 to 31. Once written, this bit becomes Read Only. If the JTAG_EN bit is 1 (enabled), the Private Key is inaccessible, independent of the state of this bit. 1=The Private Key is inaccessible (i.e, always returns 0 or 1 for every bit) 0=The Private Key is accessible	R/W / R	0b	RESET_SYS
1	MCHIP_LOCK This bit controls access to Microchip region of the eFuse memory, bytes 32 to 127. Once written, this bit becomes Read Only. If the JTAG_EN bit is 1 (enabled), the Private Key is inaccessible, independent of the state of this bit. 1=The Microchip region is inaccessible (i.e, always returns 0 or 1 for every bit) 0=The Microchip region is accessible	R/W / R	0b	RESET_SYS
0	TEST	R	0b	RESET_SYS

46.8.8 WDT EVENT COUNT REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
3:0	WDT_COUNT This field is cleared to 0 on a reset triggered by the main power on reset, but not on a reset triggered by the Watchdog Timer. This field is written by Boot ROM firmware to indicate the number of times a WDT fired before loading a good EC code image was obtained.	R/W	0b	RESET_SYS_n-WDT

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46.8.9 AES HASH BYTE SWAP CONTROL REGISTER

Offset	2Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:5	OUTPUT_BLOCK_SWAP_ENABLE Used to enable word swap on a DWORD during AHB write from AES / HASH block 4=Swap 32-bit doublewords in 128-byte blocks 3=Swap doublewords in 64-byte blocks. Useful for SHA-256. Bus references issued in the order 0x3C, 0x38, 0x34, 0x30, 0x2C, 0x28, 0x24, 0x20, 0x1C, 0x18, 0x14, 0x10, 0xC, 0x8, 0x4, 0x0, … 2=Swap doublewords in 16-byte blocks. Useful for AES. Bus references issued in the order 0xC, 0x8, 0x4, 0x0, 0x1C, 0x18,… 1=Swap doublewords in 8-byte blocks. Useful for SHA-512, which works on 64-bit words. Bus references issued in the order 0x4, 0x0, 0xC, 0x8, … 0=Disable	R/W	0b	RESET_SYS
4:2	INPUT_BLOCK_SWAP_ENABLE Used to enable word swap on a DWORD during AHB read from AES / HASH block 4=Swap 32-bit doublewords in 128-byte blocks 3=Swap doublewords in 64-byte blocks. Useful for SHA-256. Bus references issued in the order 0x3C, 0x38, 0x34, 0x30, 0x2C, 0x28, 0x24, 0x20, 0x1C, 0x18, 0x14, 0x10, 0xC, 0x8, 0x4, 0x0, … 2=Swap doublewords in 16-byte blocks. Useful for AES. Bus references issued in the order 0xC, 0x8, 0x4, 0x0, 0x1C, 0x18,… 1=Swap doublewords in 8-byte blocks. Useful for SHA-512, which works on 64-bit words. Bus references issued in the order 0x4, 0x0, 0xC, 0x8, … 0=Disable	R/W	0b	RESET_SYS
1	OUTPUT_BYTE_SWAP_ENABLE Used to enable byte swap on a DWORD during AHB write from AES / HASH block 1=Enable 0=Disable	R/W	0b	RESET_SYS
0	INPUT_BYTE_SWAP_ENABLE Used to enable byte swap on a DWORD during AHB read from AES / HASH block 1=Enable 0=Disable	R/W	0b	RESET_SYS

46.8.10 PECI DISABLE REGISTER

Offset	40h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	PECI_DISABLE This bit reduces leakage current through the CPU voltage reference pin if PECI or SB-TSI are not used. 1=The VREF_VTT function is disabled, independent of the mux setting of the GPIO that shares the pin. The GPIO that shares the pin is not disabled 0=The VREF_VTT pin is enabled	R/W	0b	RESET_SYS

46.8.11 CRYPTO SOFT RESET REGISTER

Offset	5Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:3	Reserved	R	-	–
2	AES_HASH_SOFT_RESET When this bit is asserted (‘1’), the AES and Hash blocks are reset.	W	0	RESET_VTR
1	PUBLIC_KEY_SOFT_RESET When this bit is asserted (‘1’), the Public Key block is reset.	W	0	RESET_VTR
0	RNG_SOFT_RESET When this bit is asserted (‘1’), the Random Number Generator block is reset.	W	0	RESET_VTR

46.8.12 GPIO BANK POWER REGISTER

Offset	64h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	–
7	GPIO Bank Power Lock 0 = VTR_LEVEL bits[2:0] and GPIO Bank Power Lock bit are R/W 1 = VTR_LEVEL bits[2:0] and GPIO Bank Power Lock bit are Read Only This bit cannot be cleared once it is set to ‘1’. Writing zero has no effect.	Bit[7]=0 R/W Bit[7]=1 RO	0h	RESET_SYS
6:3	Reserved	R	-	–

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Offset	64h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
2	VTR_LEVEL3 Voltage value on VTR3. This bit is set by hardware after a VTR Power On Reset, but may be overridden by software. It must be set by software if the VTR power rail is not active when RESET_SYS is de-asserted. 1=VTR3 is powered by 1.8V 0=VTR3 is powered by 3.3V	see Bit[7]	0h	RESET_SYS
1	VTR_LEVEL2 Voltage value on VTR2. This bit is set by hardware after a VTR Power On Reset, but may be overridden by software. It must be set by software if the VTR power rail is not active when RESET_SYS is de-asserted. 1=VTR2 is powered by 1.8V 0=VTR2 is powered by 3.3V	see Bit[7]	0h	RESET_SYS
0	VTR_LEVEL1 Voltage value on VTR1. This bit is set by hardware after a VTR Power On Reset, but may be overridden by software. It must be set by software if the VTR power rail is not active when RESET_SYS is de-asserted. 1=VTR1 is powered by 1.8V 0=VTR1 is powered by 3.3V	see Bit[7]	0h	RESET_SYS

Note: The Boot ROM reads the VTR_LEVEL1, VTR_LEVEL2, VTR_LEVEL3 values from the SPI Flash Header and writes the VTR_LEVEL1, VTR_LEVEL2, VTR_LEVEL3 bits. If the SPI Flash load fails, the Boot ROM clears all VTR_LEVEL1, VTR_LEVEL2, VTR_LEVEL3 bits.

46.8.13 JTAG MASTER CONFIGURATION REGISTER

Offset	70h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	–
3	MASTER_SLAVE This bit controls the direction of the JTAG port. 1=The JTAG Port is configured as a Master 0=The JTAG Port is configures as a Slave	R/W	0h	RESET_SYS
2:0	JTM_CLK This field determines the JTAG Master clock rate, derived from the 48MHz master clock. 7=375KHz 6=750KHz 5=1.5Mhz 4=3Mhz 3=6Mhz 2=12Mhz 1=24MHz 0=Reserved.	R/W	3h	RESET_SYS

46.8.14 JTAG MASTER STATUS REGISTER

Offset	74h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	–
0	JTM_DONE This bit is set to ‘1b’ when the JTAG Master Command Register is written. It becomes ‘0b’ when shifting has completed. Software can poll this bit to determine when a command has completed and it is therefore safe to remove the data in the JTAG Master TDO Register and load new data into the JTAG Master TMS Register and the JTAG Master TDI Register.	R	-	RESET_SYS

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46.8.15 JTAG MASTER TDO REGISTER

Offset	78h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	JTM_TDO When the JTAG Master Command Register is written, from 1 to 32 bits are shifted into this register, starting with bit 0, from the JTAG_TDO pin. Shifting is at the rate determined by the JTM_CLK field in the JTAG Master Configuration Register	R/W	0h	RESET_SYS

46.8.16 JTAG MASTER TDI REGISTER

Offset	7Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	JTM_TDI When the JTAG Master Command Register is written, from 1 to 32 bits are shifted out of this register, starting with bit 0, onto the JTAG_TDI pin. Shifting is at the rate determined by the JTM_CLK field in the JTAG Master Configuration Register	R/W	0h	RESET_SYS

46.8.17 JTAG MASTER TMS REGISTER

Offset	80h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	JTM_TMS When the JTAG Master Command Register is written, from 1 to 32 bits are shifted out of this register, starting with bit 0, onto the JTAG_TMS pin. Shifting is at the rate determined by the JTM_CLK field in the JTAG Master Configuration Register	R/W	0h	RESET_SYS

46.8.18 JTAG MASTER COMMAND REGISTER

Offset	84h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:5	Reserved	R	-	–
4:0	JTM_COUNT If the JTAG Port is configured as a Master, writing this register starts clocking and shifting on the JTAG port. The JTAG Master port will shift JTM_COUNT+1 times, so writing a '0h' will shift 1 bit, and writing '31h' will shift 32 bits. The signal JTAG_CLK will cycle JTM_COUNT+1 times. The contents of the JTAG Master TMS Register and the JTAG Master TDI Register will be shifted out on the falling edge of JTAG_CLK and the.JTAG Master TDO Register will get shifted in on the rising edge of JTAG_CLK. If the JTAG Port is configured as a Slave, writing this register has no effect.	W	–	RESET_SYS

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47.0 SECURITY FEATURES

47.1 Overview

This device includes a set of components that can support a high level of system security. Hardware support is provided for:

- Authentication, using public key algorithms
- Integrity, using Secure Hash Algorithms (SHA)
- Privacy, using symmetric encryption (Advanced Encryption Standard, AES)
- Entropy, using a true Random Number Generator

47.2 References

- American National Standards Institute, “Public Key Cryptography for the Financial Services Industry: Key Agreement and Key Transport Using Elliptic Curve Cryptography”, X9.63-2011, December 2011
- American National Standards Institute, “Public Key Cryptography for the Financial Servic3es Industry: The Elliptic Curve Digital Signature Algorithm (ECDSA)”, X9.62-2005, November 2005
- International Standards Organization, “Information Technology - Security techniques - Cryptographic techniques based on elliptic curves -- Part 2: Digital Signatures”, ISO/IEC 15946-2, December 2002
- National Institute of Standards and Technology, “Secure Hash Standard (SHS)”, FIPS Pub 180-4, March 2012
- National Institute of Standards and Technology, “Digital Signature Standard (DSS)”, FIPS Pub 186-3, June 2009
- National Institute of Standards and Technology, “Advanced Encryption Standard (AES)”, FIPS Pub 197, November 2001
- National Institute of Standards and Technology, “Recommendation for Block Cipher Modes of Operation”, FIPS SP 800-38A, 2001
- RSA Laboratories, “PKCS#1 v2.2: RSA Cryptography Standard”, October 2012

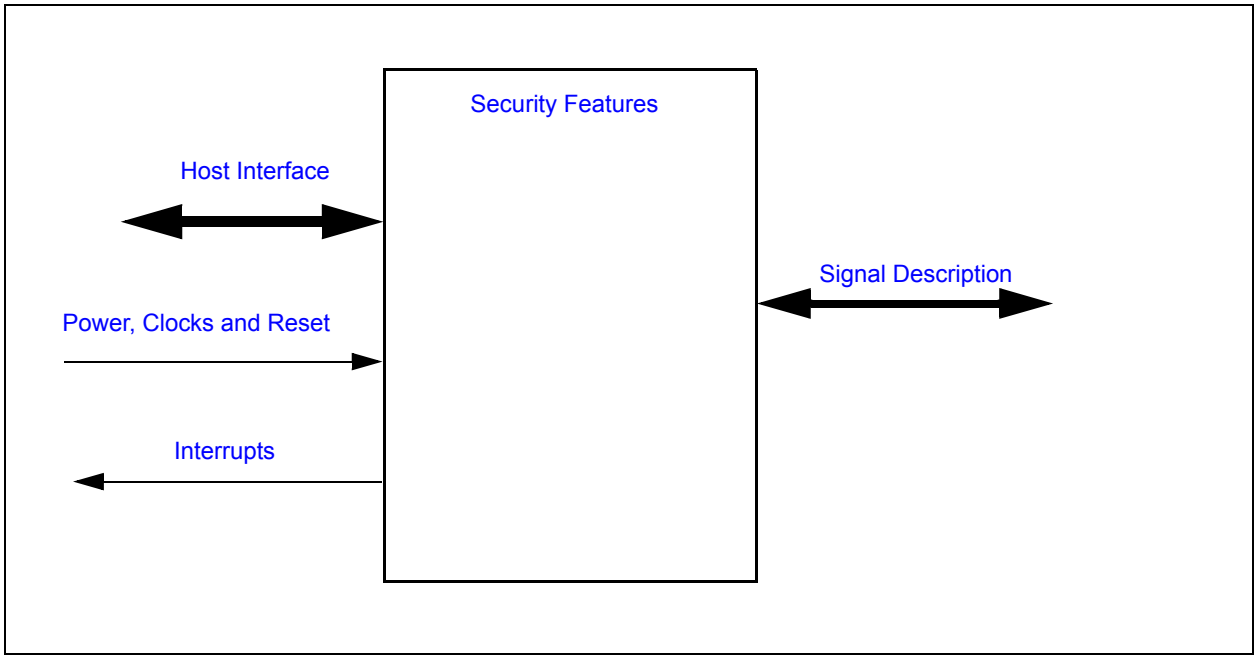
47.3 Terminology

There is no terminology defined for this section.

47.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 47-1: I/O DIAGRAM OF BLOCK



47.5 Signal Description

There are no external signals for this block.

47.6 Host Interface

Registers for the cryptographic hardware are accessible by the EC.

47.7 Power, Clocks and Reset

47.7.1 POWER DOMAINS

Name	Description
VTR	The main power well used when the VBAT RAM is accessed by the EC.

47.7.2 CLOCK INPUTS

No special clocks are required for this block.

47.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

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47.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
Public Key Engine	
PKE_ERROR	Public Key Engine core error detected
PKE END	Public Key Engine completed processing
Symmetric Encryption	
AES	Symmetric Encryption block completed processing
Cryptographic Hashing	
HASH	HASH
Random Number Generator	
RNG	Random Number Generator filled its FIFO

47.9 Low Power Modes

The Security Features may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

47.10 Description

The security hardware incorporates the following functions:

47.10.1 SYMMETRIC ENCRYPTION/DECRYPTION

Standard AES encryption and decryption, with key sizes of 128 bits, 192 bits and 256 bits, are supported with a hardware accelerator. AES modes that can be configured include Electronic Code Block (ECB), Cipher Block Chaining (CBC), Counter Mode (CTR), Output Feedback (OFB) and Cipher Feedback (CFB).

47.10.2 CRYPTOGRAPHIC HASHING

Standard SHA hash algorithms, including SHA-1, SHA-256, SHA-384 and SHA-512, are supported by hardware.

47.10.3 PUBLIC KEY CRYPTOGRAPHIC ENGINE

A large variety of public key algorithms are supported directly in hardware. These include:

- RSA encryption and decryption, with key sizes of 1024 bits, 2048 bits, 3072 bits and 4096 bits
- Elliptic Curve point multiply, with all standard NIST curves, using either binary fields or prime fields
- Elliptic Curve point multiply with Curve25519
- The Elliptic Curve Digital Signature Algorithm (ECDSA), using all supported NIST curves
- The Elliptic Curve Korean Certificate-based Digital Signature Algorithm (EC-KCDSA), using all supported NIST curves
- The Edwards-curve Digital Signature Algorithm (EdDSA), using Curve25519
- Miller-Rabin primality testing

The Public Key Engine includes a 24KB cryptographic SRAM, which can be accessed by the EC when the engine is not in operation. With its private SRAM memory, the Public Key Engine can process public key operations independently of the EC.

47.10.4 TRUE RANDOM NUMBER GENERATOR

A true Random Number Generator, which includes a 1K bit FIFO for pre-calculation of random bits.

47.10.5 temperature MONOTONIC COUNTER

The Monotonic Counter is defined in Section 45.7.3, "Monotonic Counter Register". The counter automatically increments every time it is accessed, as long as VBAT power is maintained. If it is necessary to maintain a monotonic counter across VBAT power cycles, the Counter HiWord Register can be combined with the Monotonic Counter Register to form a 64-bit monotonic counter. Firmware would be responsible for updating the Counter HiWord on a VBAT POR. The HiWord could be maintained in a non-volatile source, such as the EEPROM or an external SPI Flash.

47.10.6 CRYPTOGRAPHIC API

The Boot ROM includes an API for direct software access to cryptographic functions. API functions for Hashing and AES include a DMA interface, so the operations can function on large blocks of SRAM with a single call.

47.11 Registers

TABLE 47-1: CRYPTOGRAPHIC SRAM

Block Instance	Start Address	End Address	Size
Cryptographic SRAM	4010_0000h	4010_5FFF	24KB

47.11.1 REGISTERS SUMMARY

The Public Key Engine, The Random Number Generator, the Hash Engine and the Symmetric Encryption Engine are all listed in the Block Overview and Base Addresses in Section 3.0, "Device Inventory".

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48.0 TEST MECHANISMS

48.1 ARM Test Functions

Test mechanisms for the ARM are described in Section 5.0, "ARM M4F Based Embedded Controller".

48.2 JTAG Boundary Scan

Note:	Boundary Scan operates in 4-wire JTAG mode only. This is not supported by 2-wire SWD.

JTAG Boundary Scan includes registers and functionality as defined in IEEE 1149.1 and the MEC170x BSDL file. Functionality implemented beyond the standard definition is summarized in Table 48-1. The MEC170x Boundary Scan JTAG ID is shown in Table 1-1.

Note:	Must wait a minimum of 35ms after a POR to accurately read the Boundary Scan JTAG ID. Reading the JTAG ID too soon may return a Boundary Scan JTAG ID of 00000000h. This is not a valid ID value.

48.2.1 TAP CONTROLLER SELECT STRAP OPTION

The TAP Controller Select Strap Option determines the JTAG slave that is selected when JTAG_RST# is not asserted. The state of the TAP Controller Select Strap Option pin, defined in the Pin Configuration chapter, is sampled by hardware at POR according to the Slave Select Timing as defined in Section 51.26, "JTAG Interface Timing" and is registered internally to select between the debug and boundary scan TAP controllers.

If the strap is sampled low, the debug TAP controller is selected; if the strap is sampled high, the boundary scan slave is selected. An internal pull-up resistor is enabled by default on the TAP Controller Select Strap Option pin and can be disabled by firmware, if necessary.

TABLE 48-1: EXTENDED BOUNDARY SCAN FUNCTIONALITY

Bits	Function	Description
12, 14	TAP Controller Select Strap Option Override	When the Strap Option Override is ‘1,’ the strap option is overridden to select the debug TAP Controller until the next time the strap is sampled. To set Strap Override Function, write 0X1FFFFD to the TAP controller instruction register, then write 0x5000 to the TAP controller data register. Note that the instruction register is 18 bits long; the data register is 16 bits long.

48.3 JTAG Master

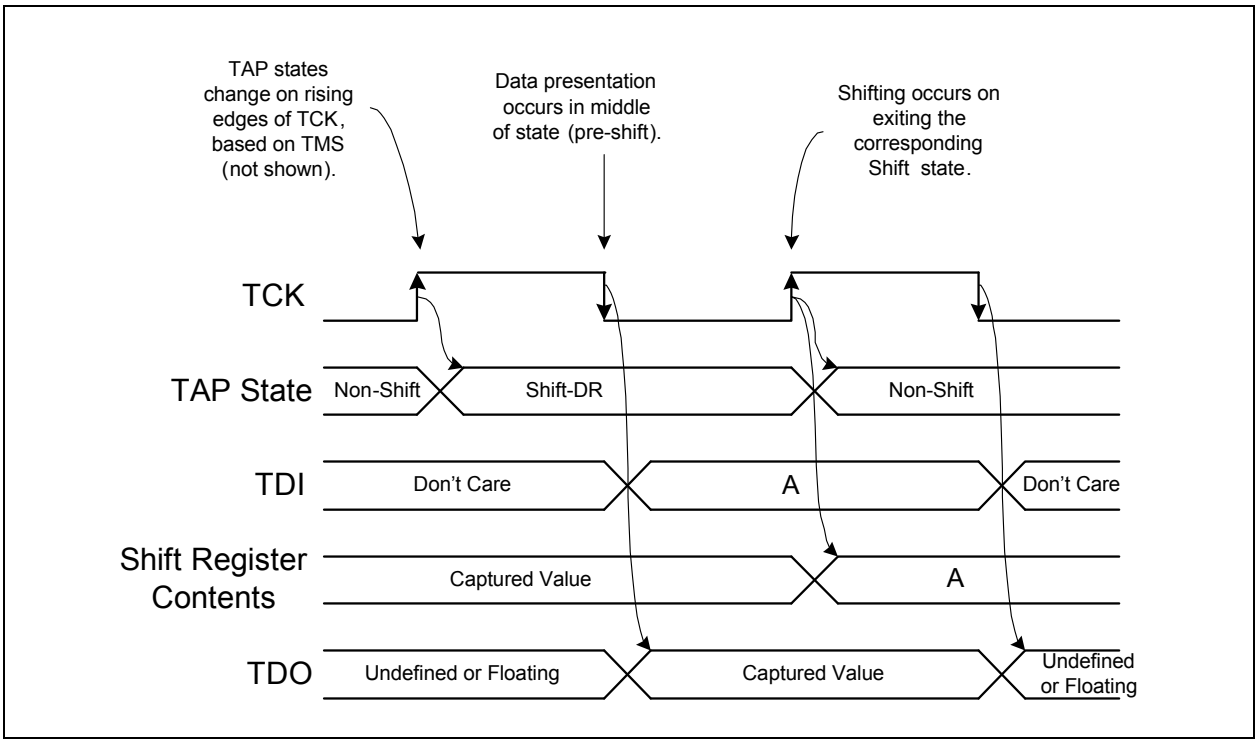
The JTAG Master controller in the MEC170x enables the embedded controller to perform full IEEE 1149.1 test functions as the master controller for test operations at assembly time or in the field.

The JTAG Master interface shares the JTAG pin interface with the JTAG Boundary Scan and Debug TAP controllers; including, JTAG_CLK, JTAG_TDI, JTAG_TDO and JTAG_TMS. When the MEC170x JTAG interface is configured as master, it is the responsibility of the master firmware to satisfy all requirements regarding JTAG port multiplexing. It is also it is the responsibility of the JTAG Master firmware to satisfy all requirements for external JTAG slave devices that require an external asynchronous reset (TRST#) input.

When JTAG slave functions are not required and the JTAG Master is enabled, the JTAG Interface pins are turned around so that the pins JTAG_CLK, JTAG_TMS and JTAG_TDI become outputs and the JTAG_TDO becomes an input.

Figure 48-1, "JTAG Signal Clocking" shows the clocking behavior of JTAG in the TAP controller in a JTAG Slave device. The rows “TAP State” and “Shift Reg. Contents” refer to the state of the JTAG Slave device and are provided for reference. When configured as a Master, the JTAG interface drives JTAG_CLK and will shift out data onto JTAG_TMS and JTAG_TDI in parallel, updating the pins on the falling edge of JTAG_CLK. The Master will sample data on JTAG_TDO on the rising edge of JTAG_CLK.

FIGURE 48-1: JTAG SIGNAL CLOCKING



48.3.1 JTAG MASTER REGISTER INTERFACE

Registers that control the JTAG Master Port are located in the EC Subsystem Registers block. These registers are listed in the following table:

TABLE 48-2: JTAG MASTER REGISTERS

Offset	Register Name
20h	Debug Enable Register
70h	JTAG Master Configuration Register
74h	JTAG Master Status Register
78h	JTAG Master TDO Register
7Ch	JTAG Master TDI Register
80h	JTAG Master TMS Register
84h	JTAG Master Command Register

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49.0 EFUSE BLOCK

49.1 Introduction

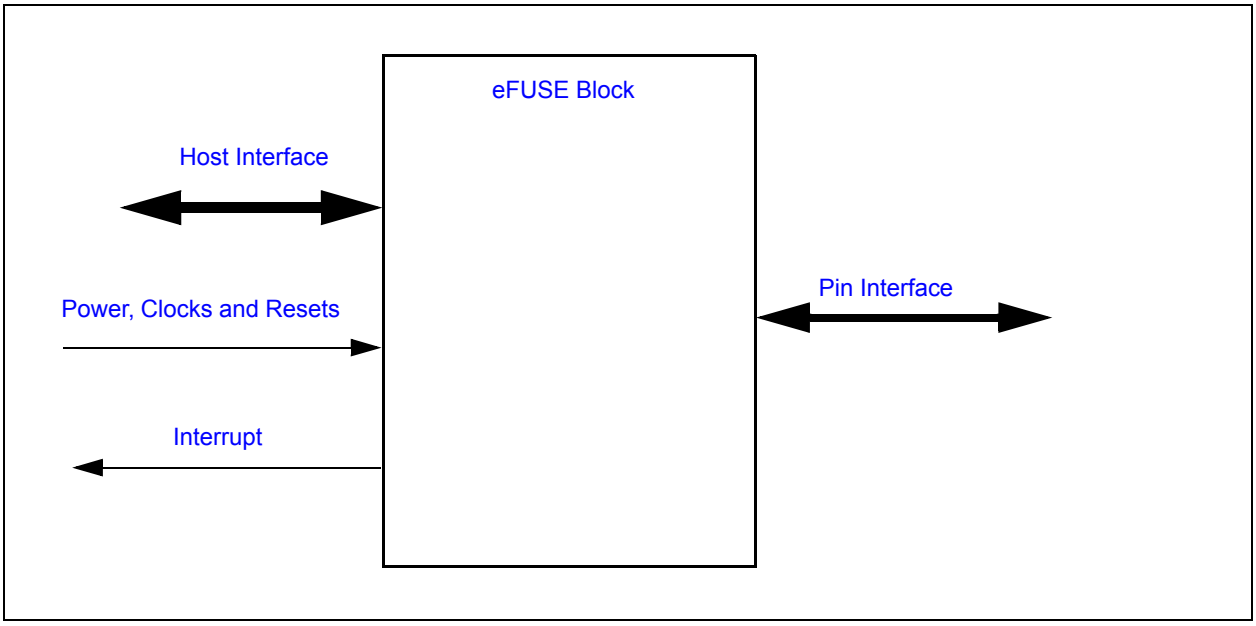
The eFUSE block provides a means of programming and accessing a block of One Time Programmable memory.

49.2 Terminology

None.

49.3 Interface

FIGURE 49-1: EFUSE BLOCK INTERFACE DIAGRAM



49.3.1 PIN INTERFACE

Table 49-1, "Signal Description" lists the signals that are routed to the pin interface.

TABLE 49-1: SIGNAL DESCRIPTION

Name	Direction	Description
VREF_ADC	Input	VPP Programming Pin

49.3.2 HOST INTERFACE

The registers defined for the eFUSE Block are accessible by the EC.

49.3.3 CLOCKING AND RESETS

This IP block has the following clocks and reset ports. For a complete list of all the clocks and resets associated with this block see Section 49.4, "Power, Clocks and Resets".

49.3.4 INTERRUPT INTERFACE

There are no interrupts from this block.

49.4 Power, Clocks and Resets

This section defines the Power, Clock, and Reset parameters of the block.

49.4.1 POWER DOMAINS

TABLE 49-2: POWER SOURCES

Name	Description
VTR	This power well sources all of the registers and logic in this block, except where noted.

49.4.2 CLOCKS

This section describes all the clocks in the block, including those that are derived from the I/O Interface as well as the ones that are derived or generated internally.

TABLE 49-3: CLOCKS

Name	Description
48MHz	This clock signal drives selected logic (e.g., counters).

49.4.3 RESETS

TABLE 49-4: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in this block.

49.5 Interrupt Generation

There are no interrupts from this block.

49.6 Low Power Modes

The eFUSE Block may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

49.7 Description

The eFuse memory consists of four blocks of 1K bits each, for a total of 4K bits. The assignment of the eFuse data is shown in Section 49.8, "eFuse Memory Map".The eFUSE bits are programmed one bit at a time through a register interface. Addressing bits for writing bits is by a 2-bit block address field and a 10-bit offset within block field. The eFUSE memory can be read through 8-bit or 16-bit reads of a block of register addresses.

Note: Only 8-bit and 16-bit access to the eFUSE memory is supported. A 32-bit access or larger will just have the 16-bit read-back value replicated in the other byte lanes.

49.7.1 EFUSE PROGRAMMING SEQUENCE

Programming of the eFuse array is one bit at a time. Programming changes a bit of '0b' to '1b'. There is no way to change the value of a bit that is already '1b'.

Sequence for programming one bit of eFuse memory:

1. Set the VREF_ADC pin to ground before powering up.
2. Power up the rest of the supplies
3. Set the MAN_ENABLE bit in the Manual Control Register to '1b'
4. Set the FSOURCE_EN_PRGM to '1b'
5. Set FSOURCE_EN_READ to '0b' - DO NOT combine with step 4; writing FSOURCE_EN_PRGM and FSOURCE_EN_READ MUST be performed with separate writes
6. Set the VREF_ADC pin to the VPP programming voltage in between1.52V to 1.60V.

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7. Set the IP_CS bit in the Manual Control Register to ‘0b’. The disables the eFuse memory array
8. Select the IP_ADDR_HI field in the Manual Mode Address Register to the block number of the block to be programmed
9. Set the IP_CS bit in the Manual Control Register to ‘1b’. The enables and powers up the selected block in the eFuse memory array
10. Select the IP_ADDR_LO field in the Manual Mode Address Register to the address of the bit within the current block to be programmed
11. Wait 100 ns (min)
12. Set PROG_EN to HIGH for 10µs (typical.
13. Set PROG_EN to LOW for 100 ns (min)
14. Repeat steps 10 to 13 for all bits within a block of 1K bits that are to be programmed to ‘1b’
15. In order to program bits in another 1K bit block, go back to Step 7 and follow the subsequent steps to programs the bits in that block

Programming one 1K bit block at a time eliminates glitches when switching between physical eFUSE blocks to prevent memory corruption.

Power down sequence after programming operation

1. Set the IP_CS bit in the Manual Control Register to ‘0b’. The disables and powers down the eFuse memory array
2. Set the VREF_ADC pin to ground
3. Set FSOURCE_EN_READ to ‘1b’
4. Set FSOURCE_EN_PRGM to ‘0b’ - DO NOT combine with step 3; writing FSOURCE_EN_PRGM and FSOURCE_EN_READ MUST be performed with separate writes

After programming is completed, the eFuse memory array may be read.

49.8 eFuse Memory Map

The eFuse memory array is organized into four regions. Each of the four regions may be locked by a control bit in the EC Register Bank. When locked, a region in eFuse memory cannot be written, and always returns 0 on reads. The lock bits are located in the OTP Lock Register. In the following table, the four regions are identified by the lock bit names in the Lock Register.

TABLE 49-5: EFUSE MEMORY MAP

Byte Number	Lock Bit	Location Name	Description
0-31	PRIVATE_KEY_LOCK	Encryption ECDH private key (aka, ECC private key)	256-bit P-256 Elliptic Curve private key, for key exchange as part of the optional decryption step in the Boot ROM Load process. Stored big-endian. • If this region is programmed by Microchip, it is encrypted with AES-256 and is always locked when the Boot ROM exits. • If this region is not programmed by Microchip, it is not encrypted, and is left unlocked when the Boot ROM exits and can be programmed by customers.
32-127	MCHIP_LOCK	Microchip	OTP data required by Microchip. This region is always locked when the Boot ROM exits.
128-159	PUBLIC_KEY_LOCK	Qx	Authentication Public Key X coordinate, NIST P-256 Elliptic Curve. 256 bits. Stored big-endian. This region is never locked after the Boot ROM exits.
160-191		Qy	Authentication Public Key Y coordinate, NIST P-256 Elliptic Curve. 256 bits. Stored big-endian. This region is never locked after the Boot ROM exits.

TABLE 49-5: EFUSE MEMORY MAP (CONTINUED)

Byte Number	Lock Bit	Location Name	Description
192-479	USER_ OTP_ LOCK	Customer use	One-time programmable memory available for customer use. 2336 bits. This region is never locked after the Boot ROM exits.
480-481		TEST	Microchip test functions. These bits should not be modified.
482		Microchip test functions	Bits[5:0] Microchip test functions. These bits should not be modified. Bit[6] Debug Select 1=Configure debug port to use SWD for debugging 0=Configure debug port to use JTAG for debugging Bit[7] Debug Disable =0 (T/Eng)/ =1 (prod) 1=JTAG and SWD disabled on ROM code exit. See bit 6 0=JTAG and SWD enabled on ROM code exit. See bit 6
483	USER_ OTP_ LOCK	Customer Flags	Bit[0]: Authenticate 1=Header and firmware authenticated with ECC public key stored in Qx and Qy 0=Header and firmware checked with SHA-256 Bit[1]: Private Key Encryption - Enable 1=Private ECC key (bytes 0-31) is AES-encrypted with ROM AES key 0=Private ECC key does not need decryption Bit[2]: Private Key Encryption - Lock 1= ECC key (bytes 0-31) is locked 0= ECC key (bytes 0-31) is not locked Bits[7:3]: Undefined
484-507	USER_ OTP_ LOCK	TEST	Microchip test functions. These bits should not be modified.
508-509	USER_ OTP_ LOCK (Bytes 192-511)	SPI Flash Tag base	Tag block address in the SPI Flash, containing pointers to EC load image. Byte 508: Bits 15:8 of the Tag Block address Byte 509: Bits 23:16 of the Tag Block address Bits 7:0 of the Tag Block address are always 0
510-511	USER_ OTP_ LOCK	OTP Version	Version Identifier

49.9 EC Registers

Registers for this block are shown in the following summary table. Addresses for each register are determined by adding the offset to the Base Address for the eFUSE Block Block in the Block Overview and Base Address Table in Section 3.0, "Device Inventory".

TABLE 49-6: REGISTER SUMMARY

Offset	Register Name
00h	Control Register
04h	Manual Control Register
06h	Manual Mode Address Register

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TABLE 49-6: REGISTER SUMMARY

Offset	Register Name
0Ch	Manual Mode Data Register
10h	eFUSE Memory

49.9.1 CONTROL REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:5	Reserved	R	-	-
4	FSOURCE_EN_READ FSOURCE pin enable for reading: 1=FSOURCE switch logic connects eFUSE FSOURCE pin to a power pad for read mode. Only set this bit when FSOURCE_EN_PRGM bit is already 0 to avoid shorting the power pad to ground 0=FSOURCE switch logic isolates eFUSE FSOURCE pin from ground	R/W	1b	RESET_SYS
3	FSOURCE_EN_PRGM FSOURCE pin enable for programming: 1=FSOURCE switch logic connects eFUSE FSOURCE pin to a power pad for PROGRAM mode. Only set this bit when FSOURCE_EN_READ bit is already 0 to avoid shorting the power pad to ground 0=FSOURCE switch logic isolates eFUSE FSOURCE pin from power pad	R/W	0b	RESET_SYS
2	EXT_PGM External programming enable: 1=eFUSE programming is done via external pin interface 0=Manual/Normal mode. eFUSE programming is done via this block's register set	R/W	0b	RESET_SYS
1	RESET Block reset: 1=Block is reset 0=Normal operation This bit self-clears and always reads back 0.	R/W	0b	RESET_SYS
0	ENABLE Block enable: 1=block is enabled for operation 0=block is disabled and in lowest power state	W	0b	RESET_SYS

49.9.2 MANUAL CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
15:6	Reserved	R	-	-
5	IP_OE eFUSE output enable. The IP might tri-state at various times, so this bit isolates the outputs to avoid potential crowbar. 1=eFUSE outputs enabled for read 0=eFUSE outputs isolated	R/W	0b	RESET_SYS
4	IP_SENSE_PULSE eFUSE sense, outputs are valid on falling edge of this bit.	R/W	0b	RESET_SYS
3	IP_PRCHG eFUSE precharge: 1=Outputs are being precharged 0=Outputs are not precharged	R/W	0b	RESET_SYS
2	IP_PRGM_EN) eFUSE program enable. Can also be considered the write signal: 1=eFUSE is programming 0=eFUSE is in read mode	R/W	0b	RESET_SYS
1	IP_CS eFUSE chip select (CS) pin: 1=eFUSE is enabled for PROGRAM/READ modes 0=eFUSE is disabled and in low power state	R/W	0b	RESET_SYS
0	MAN_ENABLE Manual mode enable bit: 1=Manual mode is enabled and this register interfaces to the eFUSE 0=Normal mode, internal controller interfaces to eFUSE IP This bit only takes affect when the REG_CTRL.EXT_PRGM bit is 0.	W	0b	RESET_SYS

49.9.3 MANUAL MODE ADDRESS REGISTER

Offset	06h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:12	Reserved	R	-	-
11:10	IP_ADDR_HI Manual mode address, selecting a 1K bit block of eFuse data.	R/W	0b	RESET_SYS
9:0	IP_ADDR_LO Manual mode address, selecting the bit address within a 1K bit block.	R/W	0b	RESET_SYS

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49.9.4 MANUAL MODE DATA REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:16	Reserved	R	-	-
15:0	IP_DATA Manual mode data: This field connects to the eFUSE data output pins.	R/W	0b	RESET_SYS

49.9.5 EFUSE MEMORY

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
4095:0	IP_MEM eFUSE memory read-back data, used to read eFuse data. Although these registers can be written, writes only change the read-back data and do not update the eFuse memory itself.	R/W	0	RESET_SYS

50.0 ELECTRICAL SPECIFICATIONS

50.1 Maximum Ratings*

*Stresses exceeding those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note:	When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

50.1.1 ABSOLUTE MAXIMUM THERMAL RATINGS

Parameter	Maximum Limits
Operating Temperature Range	0°C to +70°C Commercial -40°C to +85°C Industrial[a]
Storage Temperature Range	-55° to +150°C
Lead Temperature Range	Refer to JEDEC Spec J-STD-020B

a. For MEC1705 and MEC1704 only

50.1.2 ABSOLUTE MAXIMUM SUPPLY VOLTAGE RATINGS

Symbol	Parameter	Maximum Limits
VBAT	3.0V Battery Backup Power Supply with respect to ground	-0.3V to +3.63V
VTR_REG	Main Regulator Power Supply with respect to ground	-0.3V to +3.63V
VTR_ANALOG	3.3V Analog Power Supply with respect to ground	-0.3V to +3.63V
VTR1	3.3V or 1.8V Power Supply with respect to ground	-0.3V to +3.63V
VTR2	3.3V or 1.8V Power Supply with respect to ground	-0.3V to +3.63V
VTR3	3.3V or 1.8V Power Supply with respect to ground	-0.3V to +3.63V
VCC	3.3V Main Power Supply with respect to ground (Connected to VCC_PWRGD pin)	-0.3V to +3.63V

50.1.3 ABSOLUTE MAXIMUM I/O VOLTAGE RATINGS

Parameter	Maximum Limits
Voltage on any Digital Pin with respect to ground	Determined by Power Supply of I/O Buffer and Pad Type

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50.2 Operational Specifications

50.2.1 POWER SUPPLY OPERATIONAL CHARACTERISTICS

TABLE 50-1: POWER SUPPLY OPERATING CONDITIONS

Symbol	Parameter	MIN	TYP	MAX	Units
VBAT	Battery Backup Power Supply	2.0	3.0	3.465	V
VTR_REG	Main Regulator Power Supply	1.71	3.0	3.465	V
VTR_ANALOG	Analog Power Supply	3.135	3.3	3.465	V
VTRx	3.3V Power Supply	3.135	3.3	3.465	V
	1.8V Power Supply	1.71	1.80	1.89	V

Note: The specification for the VTRx supplies are +/- 5%.

50.2.2 AC ELECTRICAL SPECIFICATIONS

The AC Electrical Specifications for the clock input time are defined in Section 51.5, "Clocking AC Timing Characteristics". The clock rise and fall times use the standard input thresholds of 0.8V and 2.0V unless otherwise specified and the capacitive values listed in this section.

50.2.3 CAPACITIVE LOADING SPECIFICATIONS

The following table defines the maximum capacitive load validated for the buffer characteristics listed in Table 50-3, "DC Electrical Characteristics".

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{TR} = 3.3 VDC

Note: All output pins, except pin under test, tied to AC ground.

TABLE 50-2: MAXIMUM CAPACITIVE LOADING

Parameter	Symbol	Limits			Unit	Notes
		MIN	TYP	MAX		
Input Capacitance of PCI_I and PCI_IO pins	C_{IN}			Note 3	pF	
Input Capacitance of PCI_CLK pin	C_{IN}			Note 3	pF	
Output Load Capacitance supported by PCI_IO, PCI_O, and PCI_OD	C_{OUT}			Note 3	pF	
SUSCLK Input Capacitance	C_{IN}			10	pF	
Input Capacitance of PECI_I and PECI_IO	C_{IN}			10	pF	

Note 1: All input buffers can be characterized by this capacitance unless otherwise specified.

2: All output buffers can be characterized by this capacitance unless otherwise specified.

3: The PCI buffers are designed to meet the defined PCI Local Bus Specification, Rev. 2.1, electrical requirements.

TABLE 50-2: MAXIMUM CAPACITIVE LOADING (CONTINUED)

Parameter	Symbol	Limits			Unit	Notes
		MIN	TYP	MAX		
Output Load Capacitance supported by PECI_IO and OD_PH	C_{OUT}			10	pF	
Input Capacitance (all other input pins)	C_{IN}			10	pF	Note 1
Output Capacitance (all other output pins)	C_{OUT}			20	pF	Note 2

Note 1: All input buffers can be characterized by this capacitance unless otherwise specified.

2: All output buffers can be characterized by this capacitance unless otherwise specified.

3: The PCI buffers are designed to meet the defined PCI Local Bus Specification, Rev. 2.1, electrical requirements.

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50.2.4 DC ELECTRICAL CHARACTERISTICS FOR I/O BUFFERS

TABLE 50-3: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
PIO Type Buffer						
All PIO Buffers						Internal PU/PD selected via the GPIO Pin Control Register.
Pull-up current	I_{PU}	39	84	162	KΩ	
Pull-down current	I_{PD}	39	65	105	KΩ	
PIO						The drive strength is determined by programming bits[5:4] of the Pin Control 2 Register
DRIVE_STRENGTH = 00b	_	_	_	_	_	Same characteristics as an IO-2 mA.
DRIVE_STRENGTH = 01b	_	_	_	_	_	Same characteristics as an IO-4 mA.
DRIVE_STRENGTH = 10b	_	_	_	_	_	Same characteristics as an IO-8 mA.
DRIVE_STRENGTH = 11b	_	_	_	_	_	Same characteristics as an IO-12 mA.
I Type Input Buffer						TTL Compatible Schmitt Trigger Input
Low Input Level	V_{ILI}			0.3x VTR	V	
High Input Level	V_{IHI}	0.7x VTR			V	
Schmitt Trigger Hysteresis	V_{HYS}		400		mV	
O-2 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2 mA (min)
High Output Level	V_{OH}	VTR-0.4			V	I_{OH} = -2 mA (min)
IO-2 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-2mA.
OD-2 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2 mA (min)
IOD-2 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-2mA.

TABLE 50-3: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
O-4 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA (min)
High Output Level	V_{OH}	VTR-0.4			V	I_{OH} = -4 mA (min)
IO-4 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-4mA.
OD-4 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA (min)
IOD-4 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-4mA.
O-8 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA (min)
High Output Level	V_{OH}	VTR-0.4			V	I_{OH} = -8 mA (min)
						Unless the pin chapter explicitly indicates specific pin has “Over-voltage protection” feature.
IO-8 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-8mA.
OD-8 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA (min)
IOD-8 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-8mA.
O-12 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA (min)
High Output Level	V_{OH}	VTR-0.4			V	I_{OH} = -12mA (min)
IO-12 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an O-12mA.
OD-12 mA Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA (min)
IOD-12 mA Type Buffer	_	_	_	_	_	Same characteristics as an I and an OD-12mA.

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TABLE 50-3: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I_AN Type Buffer						
I_AN Type Buffer (Analog Input Buffer)	I_AN					Voltage range on pins: -0.3V to +3.63V These buffers are not 5V tolerant buffers and they are not back-drive protected
PCI Type Buffer (3.3V)						
PCI Buffers (PCI_ICLK, PCI_IO, PCI_I, PCI_O, PCI_OD)	V_{IH}	$0.5V_{TR}$		V_{TR} + 0.5	V	See *PCI Local Bus Specification Rev. 2.2*
	V_{IL}	-0.5		$0.3V_{TR}$	V	
	V_{TR}	3.0		3.6	V	LPC Supply Voltage
	I_{IL}	-10		+10	µA	$0 < V_{IN} < V_{CC}$
	V_{OH}	$0.9V_{TR}$			V	I_{OUT} = -500 µA
	V_{OL}			$0.1V_{TR}$	V	I_{OUT} = 1500 µA
	C_{IN}			10	pF	
PCI Type Buffer (1.8V)						
PCI Buffers (PCI_ICLK, PCI_IO, PCI_I, PCI_O, PCI_OD)	V_{IH}	1.5		V_{TR} + 0.5	V	See *PCI Local Bus Specification Rev. 2.2*
	V_{IL}	-0.5		0.8	V	
	V_{OH}	$0.9 \times V_{TR}$			V	I_{OUT} = -500 µA
	V_{OL}			$0.1 \times V_{TR}$	V	I_{OUT} = -1500 µA
PECI Type Buffer						
VREF_VTT						Connects to CPU Voltage pin (Processor dependent)
PECI Bus Voltage	V_{BUS}	0.95		1.26	V	
SBTSI Bus Voltage	V_{BUS}	1.28		1.9	V	
Input current	IDC			100	µA	
Input Low Current	ILEAK	-10		+10	µA	This buffer is not 5V tolerant This buffer is not backdrive protected.

TABLE 50-3: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
PECI_I Buffer						All input and output voltages are a function of Vref, which is connected to CPU_VREF input.
Input voltage range	VIn	-0.3		+Vref 0.3	V	
Low Input Level	VIL			0.275 ×Vref	V	
High Input Level	VIH	0.725 ×Vref			V	This buffer is not 5V tolerant This buffer is not backdrive protected.
PECI_IO						All input and output voltages are a function of Vref, which is connected to CPU_VREF input.
Input voltage range	VIn	-0.3		+Vref 0.3	V	See PECI Specification.
Hysteresis	VHYS	0.1 ×Vref	0.2×V ref		V	
Low Input Level	VIL			0.275 ×Vref	V	
High Input Level	VIH	0.725 ×Vref			V	
Low Output Level	VOL			0.25× Vref	V	0.5mA < IOL < 1mA
High Output Level	VOH	0.75 ×Vref			V	IOH = -6mA
Tolerance				3.63	V	This buffer is not 5V tolerant This buffer is not backdrive protected.
Crystal Oscillator						
XTAL1 (OCLK)	The MEC170x crystal oscillator design requires a 32.768 KHz parallel resonant crystal with load caps in the range 4-18pF. Refer to “Application Note PCB Layout Guide for MEC170x” for more information.					
XTAL2 (ICLK)						
Low Input Level	V_{ILI}			0.4	V	
High Input Level	V_{ILH}	2.0			V	VIN = 0 to VTR

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TABLE 50-3: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
ADC Reference Pins						
ADC_VREF						
Voltage (Option A)	V		VTR		V	Connect to same power supply as VTR
Voltage (Option B)	V	2.97	3.0	3.03	V	
Input Impedance	R_{REF}	66	67	68	KΩ	
Input Low Current	ILEAK	-0.05		+0.05	µA	This buffer is not 5V tolerant This buffer is not backdrive protected.

50.2.4.1 Pin Leakage

Leakage characteristics for all digital I/O pins is shown in the following Pin Leakage table, unless otherwise specified. Two exceptions are pins with Over-voltage protection and Backdrive protection. Leakage characteristics for Over-Voltage protected pins and Backdrive protected pins are shown in the two sub-sections following the Pin Leakage table.

TABLE 50-4: PIN LEAKAGE (VTR=3.3V + 5%; VTR = 1.8V +5%)

(T_A = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Leakage Current	I_{IL}			+/- 2	µA	VIN=0V to VTR
(T_A = -40°C to +85°C)Note 4						
Leakage Current	I_{IL}			+/- 3	µA	VIN=0V to VTR

OVER-VOLTAGE PROTECTION TOLERANCE

All the I/O buffers that do not have “Over-voltage Protection” are can only tolerate up to +/-10% I/O operation (or +1.98V when powered by 1.8V, or 3.63V when powered by 3.3V).

Functional pins that have “Over-voltage Protection” can tolerate up to 3.63V when powered by 1.8V, or 5.5V when powered by 3.3V. These pins are also backdrive protected. Backdrive Protection characteristics are shown in the following table:

TABLE 50-5: 5V TOLERANT LEAKAGE CURRENTS (VTR = 3.3V-5%)

(T_A = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Three-State Input Leakage Current for 5V Tolerant Pins	I_{IL}	-	-	+/- 4	µA	VIN: 4.0V < Vin ≤ 5.5V
		-	-	+/- 66	µA	VIN: 3.6V < Vin ≤ 4.0V
		-	-	+/- 2	µA	VIN: ≤3.6V
(T_A = -40°C to +85°C)Note 4						
Three-State Input Leakage Current for 5V Tolerant Pins	I_{IL}	-	-	+/- 4	µA	VIN: 4.0V < Vin ≤ 5.5V
		-	-	+/- 70	µA	VIN: 3.6V < Vin ≤ 4.0V
		-	-	+/- 3	µA	VIN: ≤3.6V

Note: These measurements are done without an external pull-up.

TABLE 50-6: 3.6V TOLERANT LEAKAGE CURRENTS (VTR = 1.8V-5%)

(T_A = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Three-State Input Leakage Current for Under-Voltage Tolerant Pins	I_{IL}	-	-	+/- 2	µA	VIN: 2.47V < Vin <3.6V
				+/- 42	µA	VIN: 1.92V < Vin <2.47V
		-	-	+/- 2	µA	VIN: ≤1.92V
(T_A = -40°C to +85°C)Note 4						
Three-State Input Leakage Current for Under-Voltage Tolerant Pins	I_{IL}	-	-	+/- 3	µA	VIN: 2.47V < Vin <3.6V
				+/- 50	µA	VIN: 1.92V < Vin <2.47V
		-	-	+/- 3	µA	VIN: ≤1.92V

Note: This measurements are done without an external pull-up.

BACKDRIVE PROTECTION

TABLE 50-7: BACKDRIVE PROTECTION LEAKAGE CURRENTS (VTR=0V)

(T_A = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Input Leakage	I_{IL}			4	µA	3.6V < VIN ≤ 5.5V
Input Leakage	I_{IL}			2	µA	0V < VIN ≤ 3.6V

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TABLE 50-7: BACKDRIVE PROTECTION LEAKAGE CURRENTS (VTR=0V)

(T_A = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
(T_A = -40°C to +85°C)Note 4						
Input Leakage	I_{IL}			5	µA	3.6V < VIN ≤ 5.5V
Input Leakage	I_{IL}			3	µA	0V < VIN ≤ 3.6V

50.2.5 ADC ELECTRICAL CHARACTERISTICS

TABLE 50-8: ADC CHARACTERISTICS

Symbol	Parameter	MIN	TYP	MAX	Units	Comments
VTR_ ANALOG	Analog Supply Voltage (powered by VTR)	3.135	3.3	3.465	V	
V_{RNG}	Input Voltage Range	0		ADC_ VREF	V	Range of ADC_VREF input to ADC ground
RES	Resolution	–	–	10	Bits	Guaranteed Monotonic
ACC	Absolute Accuracy	–	2	4	LSB	
DNL	Differential Non Linearity, DNL	-1	–	+1	LSB	Guaranteed Monotonic
INL	Integral Non Linearity, INL	-1.5	–	+1.5	LSB	Guaranteed Monotonic
E_{GAIN}	Gain Error, E_{GAIN}	-2	–	2	LSB	
E_{OFFSET}	Offset Error, E_{OFFSET}	-2	–	2	LSB	
CONV	Conversion Time		1.125		µS/channel	
II	Input Impedance	3.5	–	–	MΩ	

50.2.6 THERMAL CHARACTERISTICS

TABLE 50-9: THERMAL OPERATING CONDITIONS

Rating	Symbol	MIN	TYP	MAX	Unit
Consumer Temperature Devices					
Operating Junction Temperature Range	T_J	0	—	125	°C
Operating Ambient Temperature Range - Commercial	T_A	0	—	+70	°C
Operating Ambient Temperature Range - Industrial	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $I/O = S\ (\{V_{DD} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	69.3 ($P_{INT} + P_{I/O}$)			mW
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 50-10: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	TYP	MAX	Unit	Part #
Package Thermal Resistance, 169-pin WFBGA	θ_{JA}	60.8	—	°C/W	**MEC1701**
	θ_{jC}	16.3	—	°C/W	
Package Thermal Resistance, 169-pin XFBGA	θ_{JA}	52.3	—	°C/W	**MEC1703**
	θ_{jC}	12.3	—	°C/W	
Package Thermal Resistance, 144-pin WFBGA	θ_{JA}	52.9	—	°C/W	**MEC1703/ MEC1705**
	θ_{jC}	13.9	—	°C/W	
Package Thermal Resistance, 144-pin WFBGA	θ_{JA}	60.3	—	°C/W	**MEC1701**
	θ_{jC}	16.4	—	°C/W	

Note: Junction to ambient thermal resistance, Theta-JA (θ_{JA}), and Junction to case thermal resistance, Theta-JC (θ_{JC}), numbers are achieved by package simulations

50.3 Power Consumption

TABLE 50-11: VTR SUPPLY CURRENT, I_VTR

VTR	VCC	System State	48 MHz PLL	EC_CLK Freq	Typical (3.3V, 25^0 C)	Max (3.45V, 70^0 C)	Max (3.45V, 85^0 C) (Note 3)	Units	Comments (Note 1)
On	On	S0	On	48MHz	13.0	15.0	16.5	mA	FULL ON, 48MHz, LPC Clock ON
On	On	S0	On	12MHz	8.5	10.0	11.5	mA	FULL ON, 12MHz, LPC Clock ON
On	On	S0	On	1MHz	5.0	7.0	8.5	mA	FULL ON, 1MHz, LPC Clock ON
On	On	S0	On	12MHz	2.0	3.0	4.5	mA	Light Sleep, LPC Clock ON (Note 2)

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TABLE 50-11: VTR SUPPLY CURRENT, I_VTR (CONTINUED)

VTR	VCC	System State	48 MHz PLL	EC_CLK Freq	Typical (3.3V, 25^0 C)	Max (3.45V, 70^0 C)	Max (3.45V, 85^0 C) (Note 3)	Units	Comments (Note 1)
On	On	S0	Off	Off	1.0	2.0	3.1	mA	Heavy Sleep, LPC Clock ON (Note 2)
On	Off	S5	On	48MHz	12.5	14.5	16.0	mA	FULL ON (48MHz), LPC Clock Off
On	Off	S5	On	12MHz	8.0	9.5	11.5	mA	FULL ON (12MHz), LPC Clock Off
On	Off	S5	On	1MHz	5.5	6.5	8.0	mA	FULL ON (1MHz), LPC Clock Off
On	Off	S5	On	12MHz	1.5	2.5	4.0	mA	Light Sleep , LPC Clock Off (Note 2)
On	Off	S5	Off	Off	0.5	1.9	3.0	mA	Heavy Sleep, LPC Clock Off (Note 2)

Note 1: FULL ON is defined as follows: The processor is not sleeping, the Core regulator and the PLL remain powered, and at least one block is not sleeping.

2: The sleep states are defined in the System Sleep Control Register in the Power, Clocks and Resets Chapter. See Table 4.9.4, "System Sleep Control Register".

3: Applicable to MEC1705 and MEC1704 only

Note: In order to achieve the lowest leakage current when the VREF_VTT power domain is not required, ground the VREF_VTT pin.

TABLE 50-12: VBAT SUPPLY CURRENT, I_VBAT (VBAT=3.0V)

VCC	VTR	System State	48 MHz PLL	Typical (3.0V, 25^0 C)	Max (3.0V, 25^0 C)	Units	Comments
Off	Off	S5	Off	11.0	20.0	uA	Internal 32kHz oscillator
Off	Off	S5	Off	5.0	9.0	uA	32kHz crystal oscillator
Off	Off	S5	Off	5.0	9.0	uA	External 32kHz clock on XTAL2 pin

TABLE 50-13: VBAT SUPPLY CURRENT, I_VBAT (VBAT=3.3V)

VCC	VTR	System State	48 MHz PLL	Typical (3.3V, 25^0 C)	Max (3.3V, 25^0 C)	Units	Comments
Off	Off	S5	Off	12.0	22.0	uA	Internal 32kHz oscillator

TABLE 50-13: VBAT SUPPLY CURRENT, I_VBAT (VBAT=3.3V)

VCC	VTR	System State	48 MHz PLL	Typical (3.3V, 25^0 C)	Max (3.3V, 25^0 C)	Units	Comments
Off	Off	S5	Off	6.0	10.0	uA	32kHz crystal oscillator
Off	Off	S5	Off	6.0	10.0	uA	External 32kHz clock on XTAL2 pin

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51.0 TIMING DIAGRAMS

51.1 Power-up and Power-down Timing

FIGURE 51-1: VTR/VBAT POWER-UP TIMING

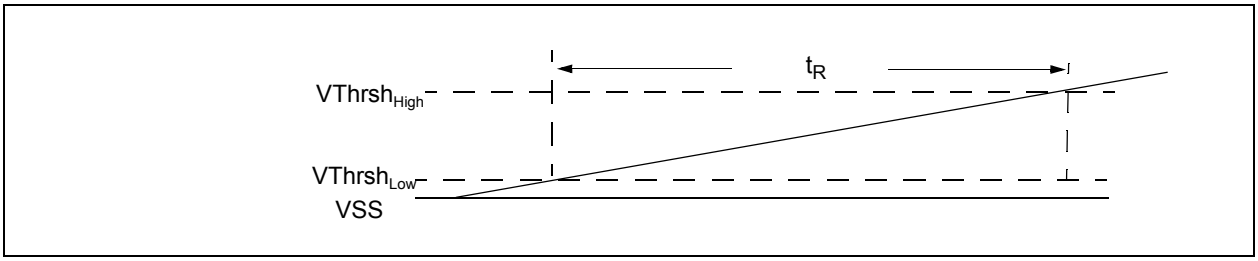

FIGURE 51-2: VTR RESET AND POWER-DOWN

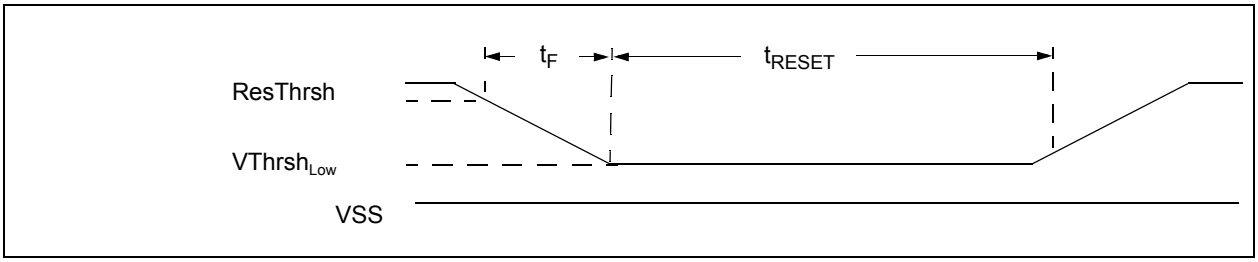

TABLE 51-1: VTR/VBAT TIMING PARAMETERS

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
t_F	VTR Fall time	30			µs	1
	VBAT Fall time	30			µs	
t_R	VTR Rise time	0.050		20	ms	1
	VBAT Rise time	0.100		20	ms	
t_{RESET}	Minimum Reset Time	1			µs	
$VThrsh_{Low}$	VTR Low Voltage Threshold	0.1 × VTR			V	1
	VBAT Low Voltage Threshold	0.1 × VBAT			V	
$VThrsh_{High}$	VTR High Voltage Threshold			0.9 × VTR	V	1
	VBAT High Voltage Threshold			0.9 × VBAT	V	
ResThrsh	VTR Reset Threshold	0.5	1.8	2.7	V	1
	VBAT Reset Threshold	0.5	1.25	1.9	V	

Note 1: VTR applies to both VTR_REG and VTR_ANALOG

51.2 Power Sequencing (Functional Rev A)

FIGURE 51-3: POWER RAIL SEQUENCING

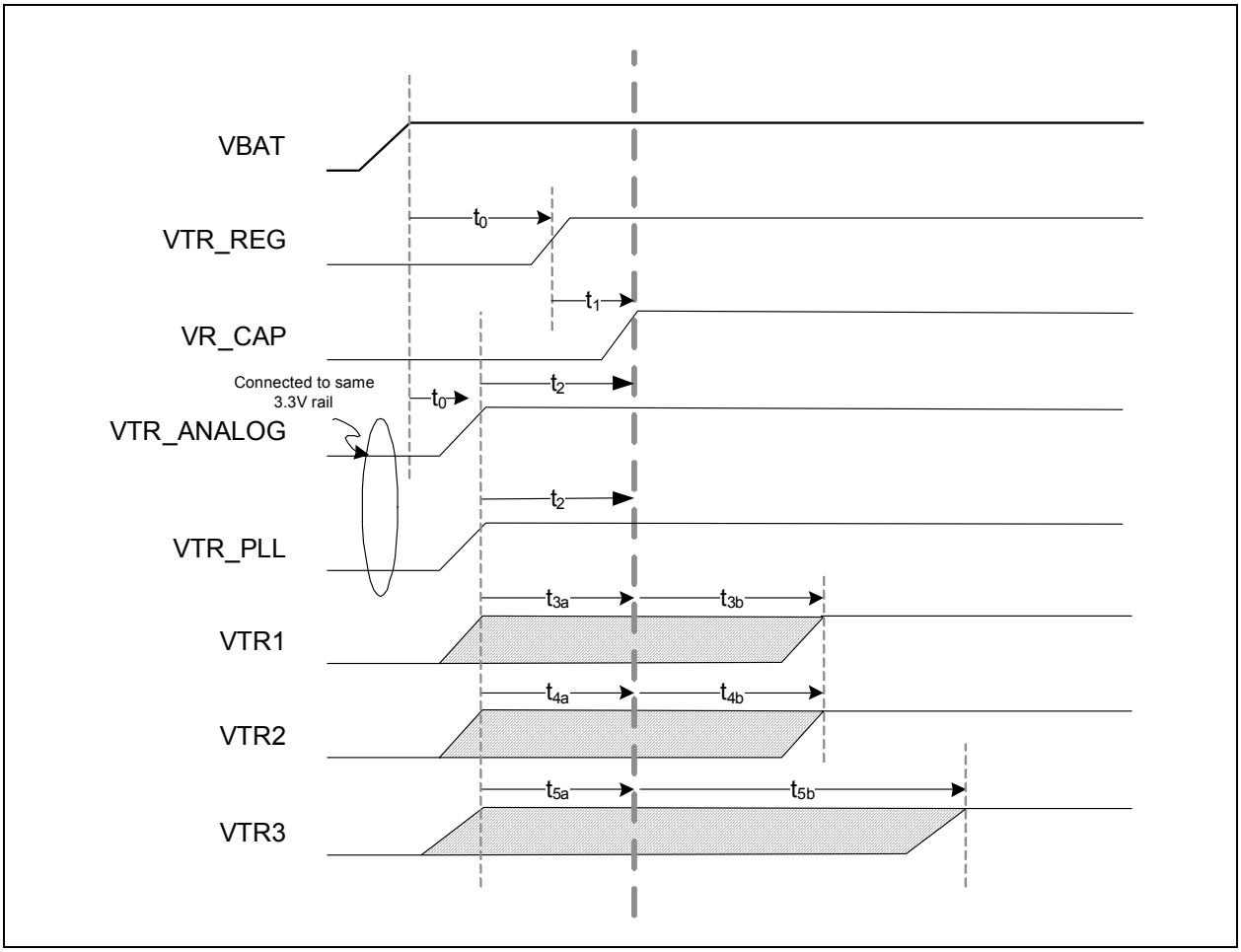

TABLE 51-2: POWER SEQUENCING PARAMETERS

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_0	VBAT above minimum operating threshold to VTR_ANALOG and VTR_REG above minimum operating thresholds	0			ms	1, 9
t_1	VTR_REG above 1.6V to VR_CAP assertion	300			µs	2
t_2	VTR_ANALOG & VTR_PLL above minimum operating threshold to VR_CAP assertion.	0		1	ms	3, 9
t_{3a}	If VTR1=3.3V or 1.8V and VTR1 rises before VR_CAP assertion then: VTR1 above minimum operating threshold to VR_CAP assertion.	0		1	ms	4 5, 9

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TABLE 51-2: POWER SEQUENCING PARAMETERS (CONTINUED)

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{3b}	If VTR1=1.8V and VTR1 rises after VR_CAP assertion then: VR_CAP assertion to VTR1 above minimum operating threshold.	0		1	ms	5, 9
t_{4a}	If VTR2=3.3V or 1.8V and VTR2 rises before VR_CAP assertion then: VTR2 above minimum operating threshold to VR_CAP assertion.	0		1	ms	4, 6, 9
t_{4b}	If VTR2=1.8V and VTR2 rises after VR_CAP assertion then: VR_CAP assertion to VTR2 above minimum operating threshold.	0		1	ms	6, 9
t_{5a}	If VTR3=3.3V or 1.8V and VTR3 rises before VR_CAP assertion then: VTR3 above minimum operating threshold to VR_CAP assertion.	0		1	ms	9
t_{5b}	FOR ESPI BOOT If VTR3=1.8V and VTR3 rises after VR_CAP assertion then: VR_CAP assertion to VTR3 above minimum operating threshold.	0		30	sec	7, 9
	FOR NON-ESPI BOOT If VTR3=1.8V and VTR3 rises after VR_CAP assertion then VR_CAP assertion to VTR3 above minimum operating threshold.	0			ms	9
	FOR NON-ESPI BOOT If VTR3=3.3V and VTR3 rises after VR_CAP assertion then: VR_CAP assertion to VTR3 above minimum operating threshold.	0			ms	8, 9

Note 1: VBAT must rise no later than VTR_ANALOG and VTR_REG. This relationship is ensured by the recommended battery circuit.

2: VR_CAP output is asserted by the regulator when VR_REG is on and stable for at least the minimum defined time. All other signal timing requirements are relative to VR_CAP assertion.

3: VTR_PLL Must be connected to 3.3V VTR_ANALOG power supply.

4: VTR1 and VTR2 cannot be connected to VTR_REG for 3.3V operation. If VTR1 or VTR2 is powered by 3.3V, they must be connected to the 3.3V VTR_ANALOG supply. This is to ensure they power up before VR_CAP is asserted so that the auto voltage detection circuit that sets the bits in the GPIO Bank Power bits functions correctly.

5: The JTAG_STRAP pin is powered by VTR1 and is sampled when the RESET_EC signal goes inactive following POR event. Subsequent EC resets will not sample the JTAG_STRAP pin. VTR1 must be powered prior to RESET_EC signal going inactive.

6: The SHD_CS# pin, which is powered by VTR2, must be powered before the Boot ROM samples this pin.

7: If booting over eSPI, the EC boot ROM code monitors GPIO227/SHD_IO2, which is a VTR2 signal, to determine that VTR3 is active. The maximum time is the time after which the code abandons the boot.

8: Software must program 3.3V VTR_LEVEL3 bit in GPIO Bank Power register to 0 for 3.3V operation.

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9: Minimum operating threshold values for Power Rails are defined in Table 50-1, “Power Supply Operating Conditions,” on page 593.

51.3 Power Sequencing (Functional Rev B and later)

FIGURE 51-4: POWER RAIL SEQUENCING

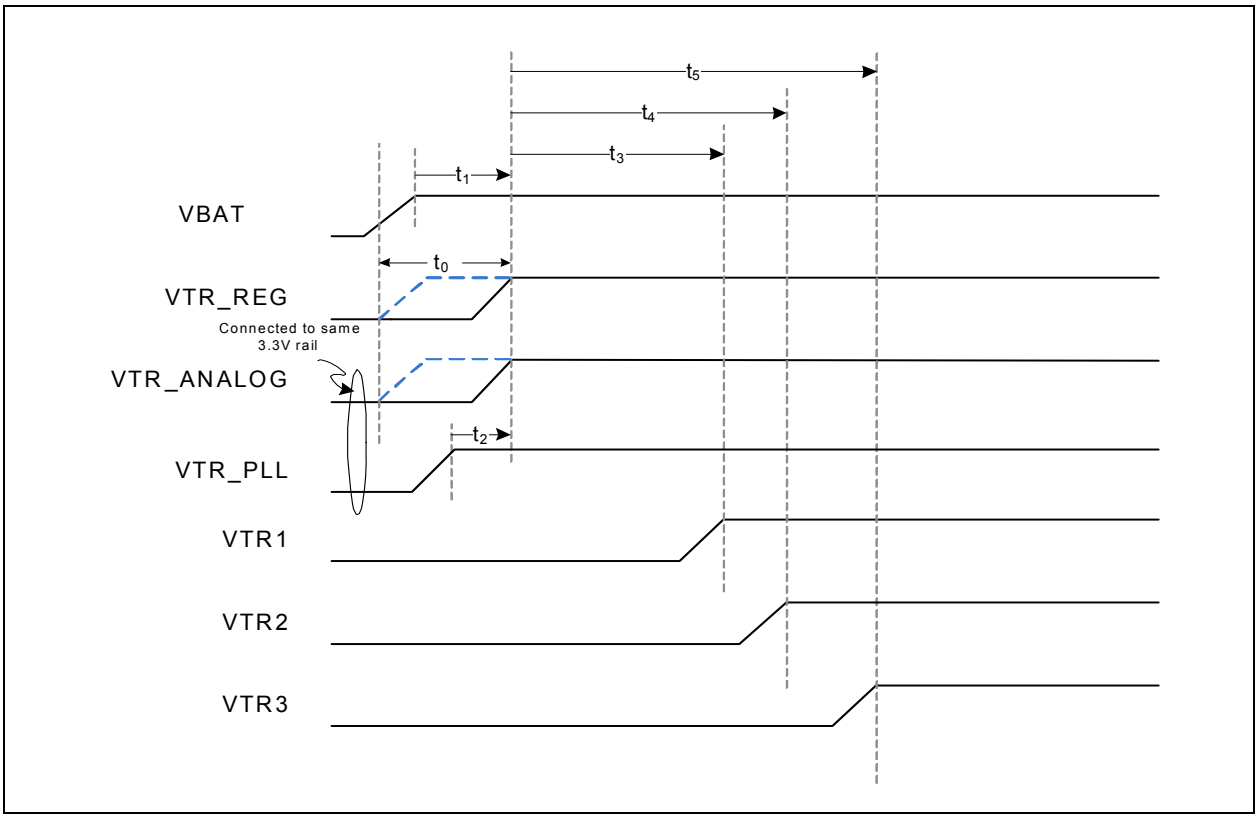

TABLE 51-3: POWER SEQUENCING PARAMETERS

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_0	VTR_ANALOG above minimum operating threshold to VTR_REG above minimum operating threshold	0		1	ms	10, 17
	VTR_REG above minimum operating threshold to VTR_ANALOG above minimum operating threshold	0		1	ms	
t_1	VBAT above minimum operating threshold to VTR_ANALOG and VTR_REG are both above minimum operating thresholds	0			ms	11, 17
t_2	VTR_PLL above minimum operating threshold to VTR_ANALOG above minimum operating threshold			0	ms	12, 17

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TABLE 51-3: POWER SEQUENCING PARAMETERS (CONTINUED)

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_3	VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR1 above minimum operating threshold. VTR1 at1.8V(nom) or 3.3V(nom)	0		1	ms	13, 17
t_4	VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR2 above minimum operating threshold. VTR2 at1.8V(nom) or 3.3V(nom)	0		1	ms	14, 17
t_{5b}	FOR ESPI BOOT (VTR3=1.8V) VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR3 above minimum operating threshold.	0		30	sec	15, 17
	FOR NON-ESPI BOOT (VTR3 = 1.8V or 3.3V) VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR3 above minimum operating threshold.	0			ms	16, 17

10: VTR_ANALOG and VTR_REG may ramp in either order. There is no limit on the time between the ramp of one rail and the ramp of the other.

11: VBAT must rise no later than VTR_ANALOG and VTR_REG. This relationship is ensured by the recommended battery circuit.

12: VTR_ANALOG and VTR_PLL must be connected to the same 3.3V power source.

13: The JTAG_STRAP pin is powered by VTR1 and is sampled on the assertion of the first RESET_EC event following a RESET_VTR. Subsequent EC resets will not sample the JTAG_STRAP pin. VTR1 must be powered prior to the deassertion of RESET_EC.

14: The SHD_CS# pin, which is powered by VTR2, must be powered before the Boot ROM samples this pin.

15: If booting over eSPI, the EC boot ROM code monitors GPIO227/SHD_IO2, which is a VTR2 signal, to determine that VTR3 is active. The maximum time is the time after which the code abandons the boot.

16: In non-eSPI applications, where VTR3 may be either 1.8V or 3.3V, software must program the GPIO Bank Power register for VTR3 pins before any of the VTR3 powered pins are used.

17: minimum operating threshold values for Power Rails are defined in Table 50-1, “Power Supply Operating Conditions,” on page 593.

51.4 RESETI# Timing

FIGURE 51-5: RESETI# TIMING

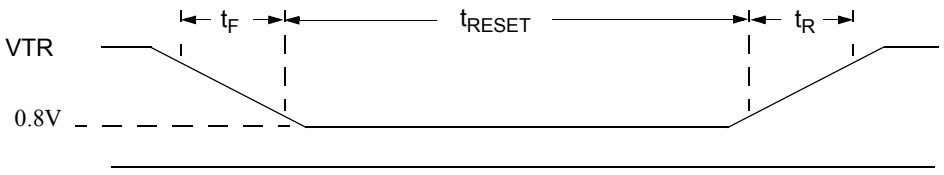

TABLE 51-4: RESETI# TIMING PARAMETERS

Symbol	Parameter	Limits		Units	Comments
		MIN	MAX		
t_F	RESETI# Fall time	0	1	ms	
t_R	RESETI# Rise time	0	1	ms	
t_{RESET}	Minimum Reset Time	1		µs	Note 1

Note 1: The RESETI# input pin can tolerate glitches of no more than 50ns.

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51.5 Clocking AC Timing Characteristics

FIGURE 51-6: CLOCK TIMING DIAGRAM

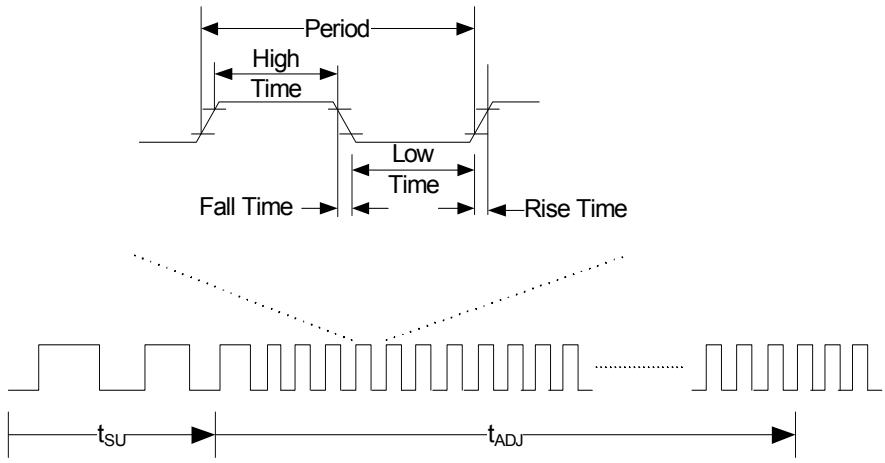

TABLE 51-5: CLOCK TIMING PARAMETERS

Clock	Symbol	Parameters	MIN	TYP	MAX	Units
48 MHz PLL	f_{SU}	Start-up accuracy	-	-	3	ms
	-	Operating Frequency (locked to 32KHz single-ended input) (Note 1)	47.5	48	48.5	MHz
	-	Operating Frequency (locked to 32KHz Silicon Oscillator) (Note 1)	46.56	48	49.44	MHz
	CCJ	Cycle to Cycle Jitter(Note 2)	-200		200	ps
	t_{DO}	Output Duty Cycle	45	-	55	%
32MHz Ring Oscillator	-	Operating Frequency	16	-	48	MHz
32.768 kHz Crystal Oscillator (Note 3)	-	Operating Frequency	-	32.768	-	kHz

Note 1: The 48MHz PLL is frequency accuracy is computed by adding +/-1% to the accuracy of the 32kHz reference clock.

2: The Cycle to Cycle Jitter of the 48MHz PLL is +/-200ps based on an ideal 32kHz clock source. The actual jitter on the 48MHz clock generated is computed by adding the clock jitter of the 32kHz reference clock to the 48MHz PLL jitter (e.g., 32kHz jitter +/- 200ps).

3: See the PCB Layout guide for design requirements and recommended 32.768 kHz Crystal Oscillators.

4: An external single-ended 32KHz clock is required to have an accuracy of +/- 100 ppm.

5: The external single-ended 32KHz clock source may be connected to either the XTAL2 pin or 32KHZ_IN pin.

TABLE 51-5: CLOCK TIMING PARAMETERS (CONTINUED)

Clock	Symbol	Parameters	MIN	TYP	MAX	Units
32KHz single-ended input (Note 5)	-	Operating Frequency	-	32.768	-	kHz
	-	Period	(Note 4)	30.52	(Note 4)	µs
	-	High Time	10			us
	-	Low Time	10			us
	-	Fall Time	-	-	1	us
	-	Rise Time	-	-	1	us
32KHz Silicon Oscillator	-	Operating Frequency	32.112	32.768	33.424	kHz
	-	Start-up delay from 0k Hz to Operating Frequency	150			us

Note 1: The 48MHz PLL is frequency accuracy is computed by adding +/-1% to the accuracy of the 32kHz reference clock.

2: The Cycle to Cycle Jitter of the 48MHz PLL is +/-200ps based on an ideal 32kHz clock source. The actual jitter on the 48MHz clock generated is computed by adding the clock jitter of the 32kHz reference clock to the 48MHz PLL jitter (e.g., 32kHz jitter +/- 200ps).

3: See the PCB Layout guide for design requirements and recommended 32.768 kHz Crystal Oscillators.

4: An external single-ended 32KHz clock is required to have an accuracy of +/- 100 ppm.

5: The external single-ended 32KHz clock source may be connected to either the XTAL2 pin or 32KHZ_IN pin.

51.6 GPIO Timings

FIGURE 51-7: GPIO TIMING

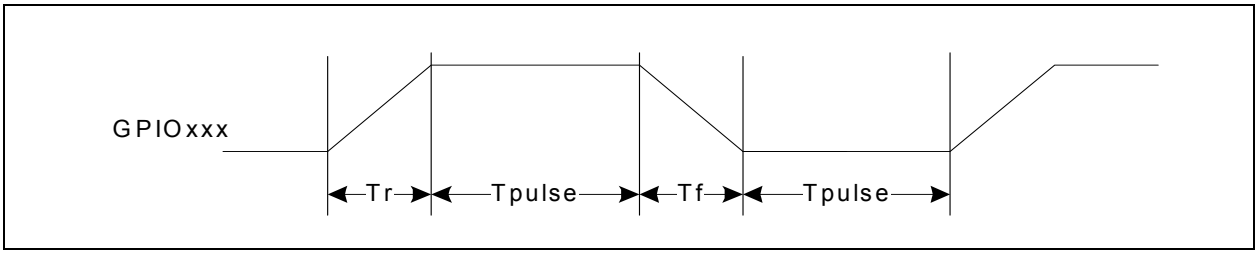

TABLE 51-6: GPIO TIMING PARAMETERS

Symbol	Parameter	MIN	TYP	MAX	Unit	Notes
t_R	GPIO Rise Time (push-pull)	0.54		1.31	ns	1
t_F	GPIO Fall Time	0.52		1.27	ns	
t_R	GPIO Rise Time (push-pull)	0.58		1.46	ns	2
t_F	GPIO Fall Time	0.62		1.48	ns	

Note 1: Pad configured for 2ma, CL=2pF

2: Pad configured for 4ma, CL=5pF

3: Pad configured for 8ma, CL=10pF

4: Pad configured for 12ma, CL=20pF

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TABLE 51-6: GPIO TIMING PARAMETERS (CONTINUED)

Symbol	Parameter	MIN	TYP	MAX	Unit	Notes
t_R	GPIO Rise Time (push-pull)	0.80		2.00	ns	3
t_F	GPIO Fall Time	0.80		1.96	ns	
t_R	GPIO Rise Time (push-pull)	1.02		2.46	ns	4
t_F	GPIO Fall Time	1.07		2.51	ns	
t_{pulse}	GPIO Pulse Width	60			ns	

Note 1: Pad configured for 2ma, CL=2pF

2: Pad configured for 4ma, CL=5pF

3: Pad configured for 8ma, CL=10pF

4: Pad configured for 12ma, CL=20pF

51.7 Boot from SPI Flash Timing

FIGURE 51-8: SPI BOOT TIMING

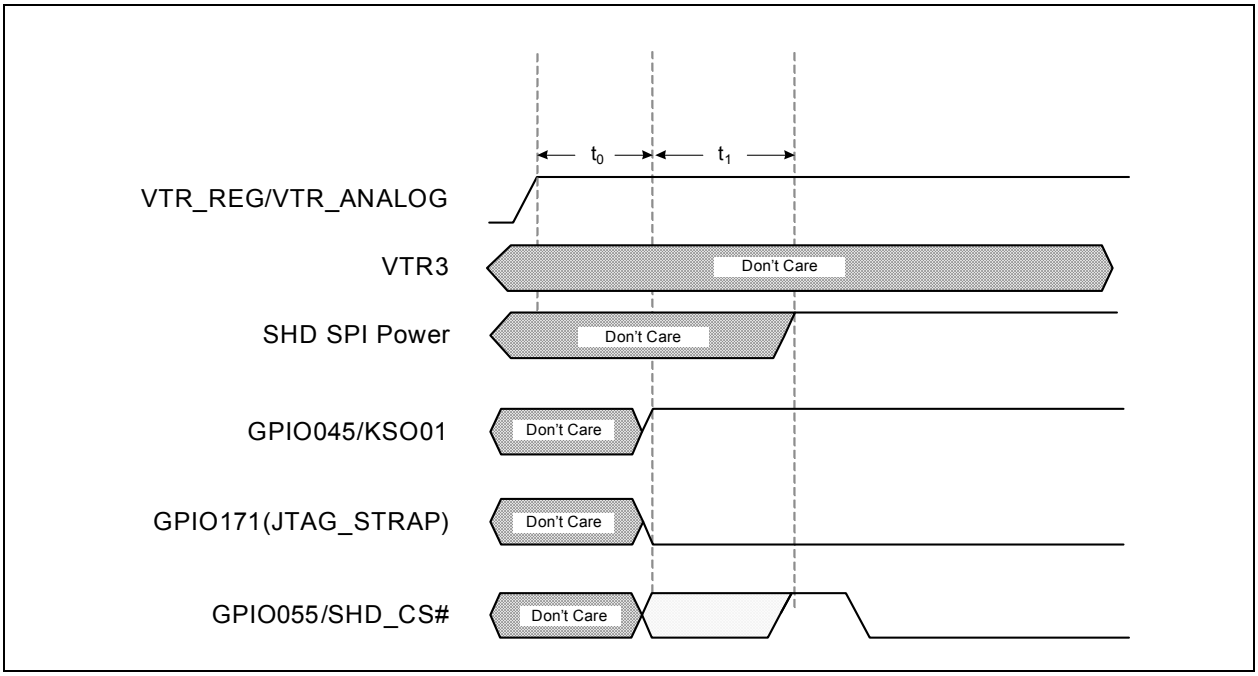

TABLE 51-7: SPI FLASH BOOT TIMING PARAMETERS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_0	Time from Power On to sample PVT_SPI Strap options	3			ms	
t_1	Time for SPI Power to be active after sampling starts			5	ms	

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51.8 Boot from eSPI Timing

FIGURE 51-9: ESPI BOOT TIMING

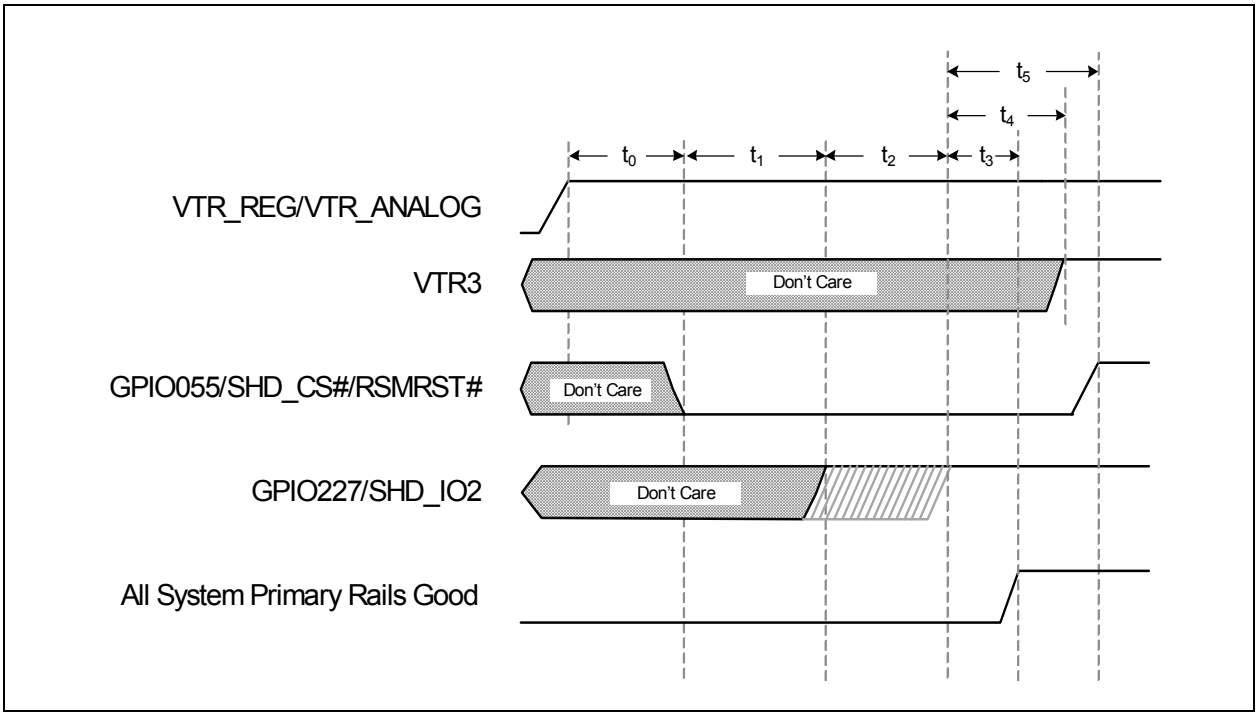

TABLE 51-8: ESPI BOOT TIMING PARAMETERS

Symbol	Parameter	MIN	TYP	MAX	Unit	Notes
t_0	Time from Power On to sample Strap options	2			ms	
t_1	Time Shared_SPI/eSPI boot strap pin must be low (i.e., GPIO055/SHD_CS#/RSMRST# pin low)	5			ms	
t_2	Time from strap detection of eSPI Flash Channel boot requirement to at least one Primary Rail active (i.e., GPIO227/SHD_IO2 is high)			30	sec	1
t_3	Time from when at least one Primary Rail is active until the time all 4 Primary Rails are active.			20	ms	2
t_4	Time from when at least one Primary Rail is active until the time VTR3 must be active. System requirement from Intel will limit this to 20ms max, but the hardware can tolerate up to 30ms max.			30	ms	
t_5	Time from the detection of an active Primary Rail until RSMRST# is de-asserted	35			ms	

Note 1: Intel Primary Rails are defined as VCC_Prim 1.8V, VCC_Prim 3.3V, VCCPRIM_CORE and VCC_Prim 1.0V

2: This is an Intel system requirement. This time is not monitored directly.

51.9 VCC_PWRGD Timing

FIGURE 51-10: VCC_PWRGD TIMING

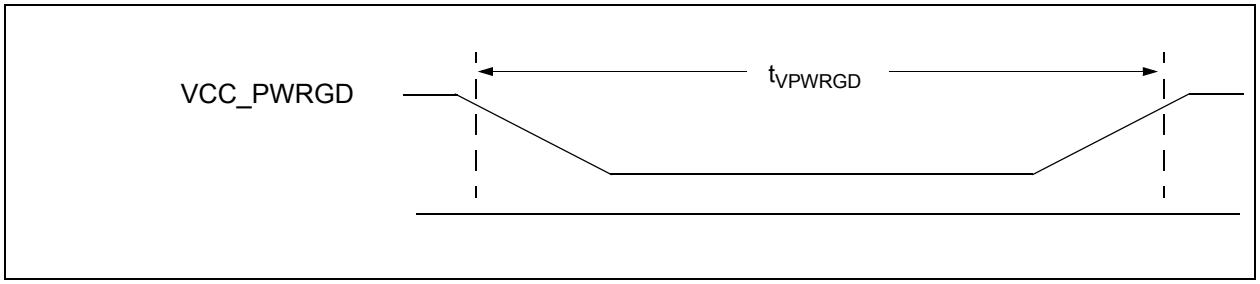

TABLE 51-9: VCC_PWRGD POWER TIMING PARAMETERS

Symbol	Parameter	Limits		Units	Notes
		MIN	MAX		
t_{VPWRGD}	VCC_PWRGD Pulse Width	31		ns	

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51.10 LPC LCLK Timing

FIGURE 51-11: LPC CLOCK TIMING

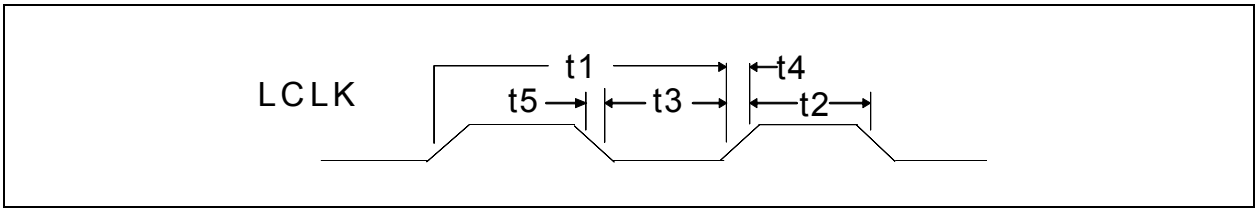

TABLE 51-10: LPC CLOCK TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	Period	30		57	nsec
t2	High Time	11			
t3	Low Time				
t4	Rise Time			3	
t5	Fall Time				

51.11 LPC RESET# Timing

FIGURE 51-12: RESET TIMING

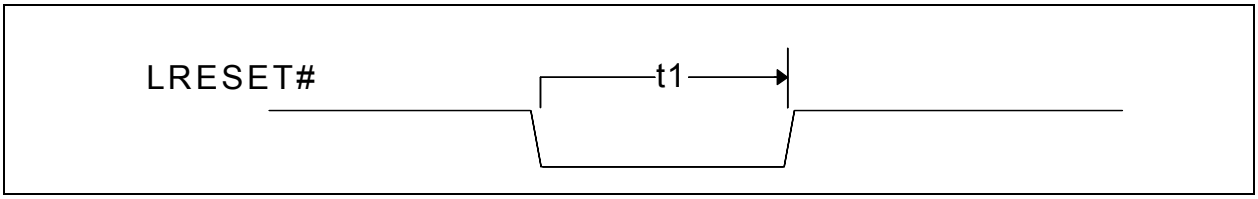

TABLE 51-11: RESET TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	LRESET# width	1			ms

51.11.1 LPC BUS TIMING

FIGURE 51-13: OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

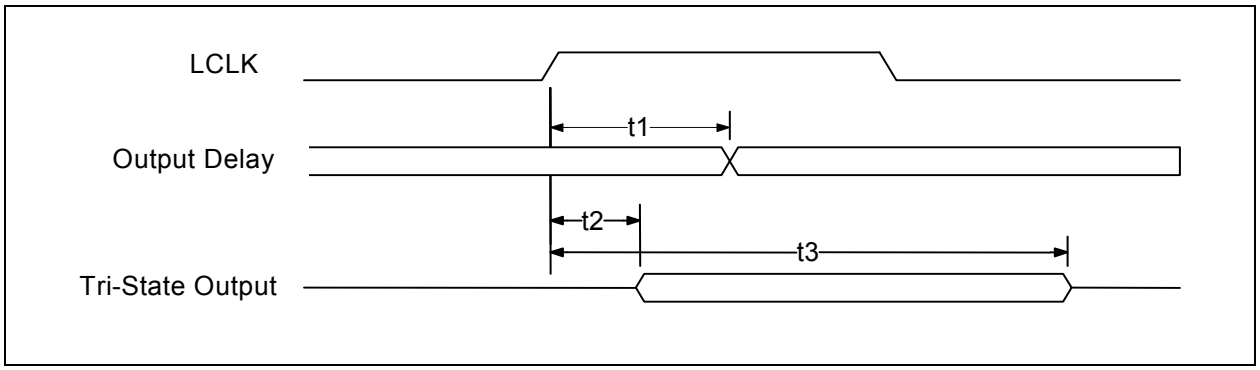

TABLE 51-12: OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	LCLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay				
t3	Active to Float Delay			28	

51.11.2 LPC INPUT TIMING

FIGURE 51-14: INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

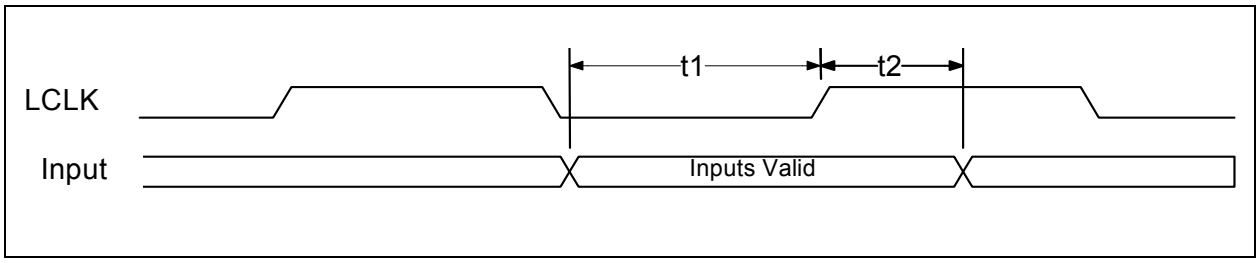

TABLE 51-13: INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	Input Set Up Time to LCLK – Bused Signals	7			ns
t2	Input Hold Time from LCLK	0			

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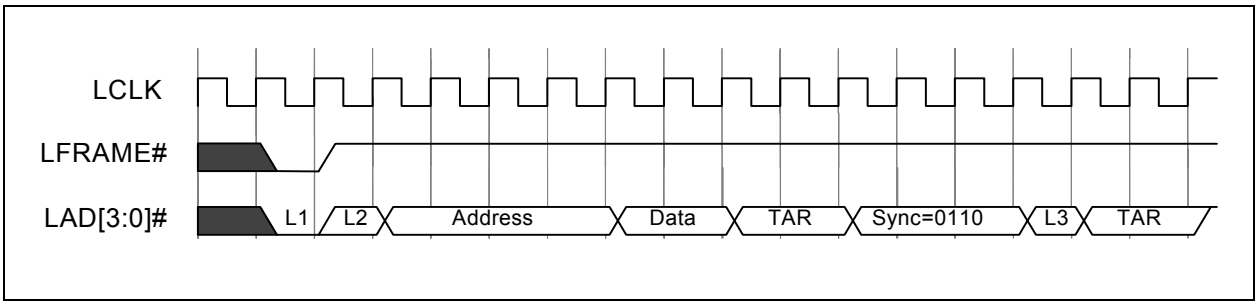
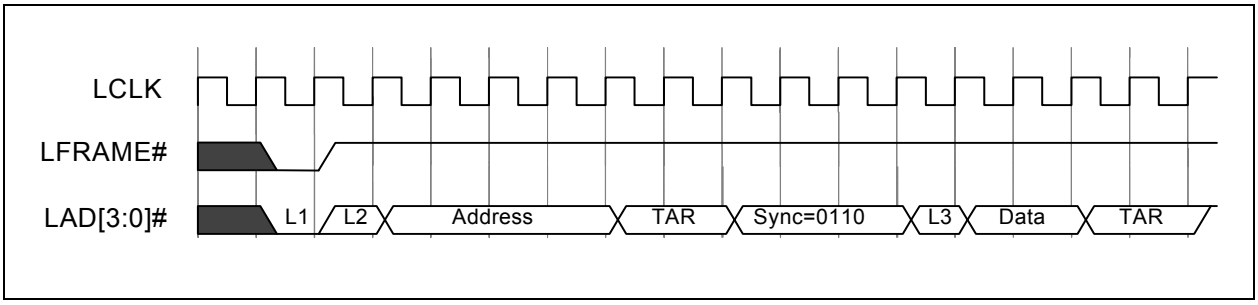
51.11.3 LPC I/O TIMING

FIGURE 51-15: I/O WRITE



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 51-16: I/O READ



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

51.11.4 SERIAL IRQ TIMING

FIGURE 51-17: SETUP AND HOLD TIME

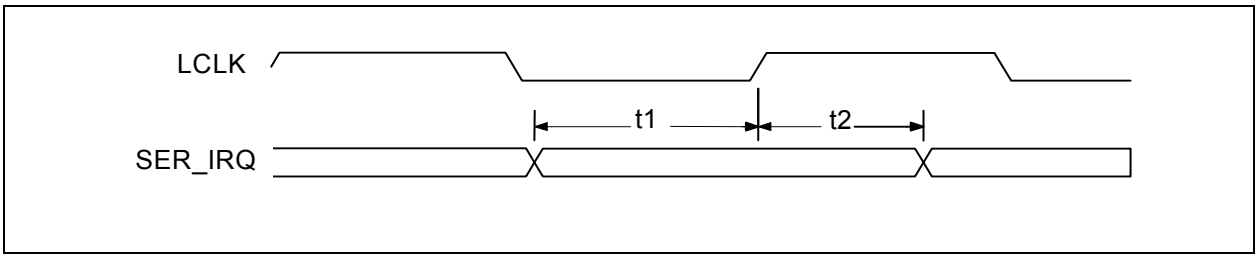


TABLE 51-14: SETUP AND HOLD TIME

Name	Description	MIN	TYP	MAX	Units
t1	SER_IRQ Setup Time to LCLK Rising	7			nsec
t2	SER_IRQ Hold Time to LCLK Rising	0			

51.12 Serial Port (UART) Data Timing

FIGURE 51-18: SERIAL PORT DATA

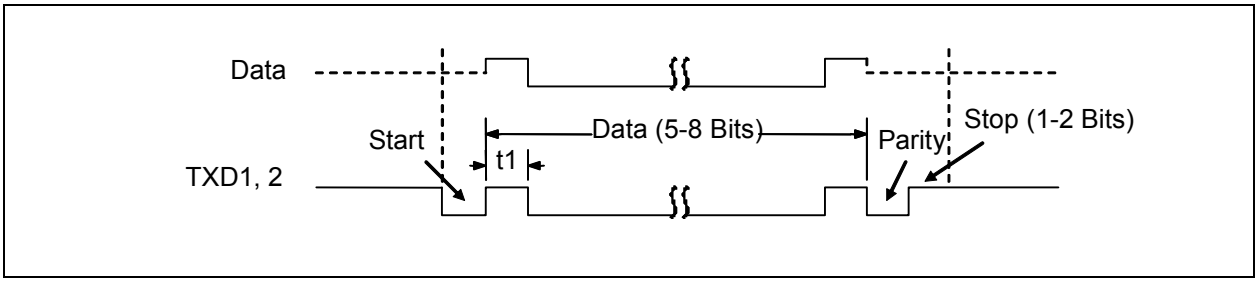


TABLE 51-15: SERIAL PORT DATA PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	Serial Port Data Bit Time		t_{BR} (Note 1)		nsec

Note 1: tBR is 1/Baud Rate. The Baud Rate is programmed through the Baud_Rate_Divisor bits located in the Programmable Baud Rate Generator registers. Some of the baud rates have some percentage of error because the clock does not divide evenly. This error can be determined from the values in these baud rate tables.

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51.13 PECI Interface

Name	Description	MIN	MAX	Units	Notes
t_{BIT}	Bit time (overall time evident on PECI pin) Bit time driven by an originator	0.495 0.495	500 250	µsec µsec	Note 1
$t_{BIT,jitter}$	Bit time jitter between adjacent bits in a PECI message header or data bytes after timing has been negotiated	-	-	%	
$t_{BIT,drift}$	Change in bit time across a PECI address or PECI message bits as driven by the originator. This limit only applies across t_{BIT-A} bit drift and t_{BIT-M} drift.	-	-	%	
t_{H1}	High level time for logic 1	0.6	0.8	t_{BIT}	Note 2
t_{H0}	High level time for logic 0	0.2	0.4	t_{BIT}	
t_{PECIR}	Rise time (measured from V_{OL} to $V_{IH,min}$, $Vtt_{(nom)}$–5%)	-	30 + (5 x #nodes)	ns	Note 3
t_{PECIF}	Fall time (measured from V_{OH} to $V_{IL,max}$, $Vtt_{(nom)}$+5%)	-	(30 x #nodes)	ns	Note 3

Note 1: The originator must drive a more restrictive time to allow for quantized sampling errors by a client yet still attain the minimum time less than 500 µsec. t_{BIT} limits apply equally to t_{BIT-A} and t_{BIT-M}. The MEC170x is designed to support 2 MHz, or a 500ns bit time. See the PECI 3.0 specification from Intel Corp. for further details.

2: The minimum and maximum bit times are relative to t_{BIT} defined in the Timing Negotiation pulse. See the PECI 3.0 specification from Intel Corp. for further details.

3: "#nodes" is the number of nodes on the PECI bus; host and client nodes are counted as one each. Extended trace lengths may appear as extra nodes. Refer also to Table 29-2, "PECI Routing Guidelines". See the PECI 3.0 specification from Intel Corp. for further details.

51.14 8042 Emulation CPU_Reset Timing

FIGURE 51-19: KBRST TIMING

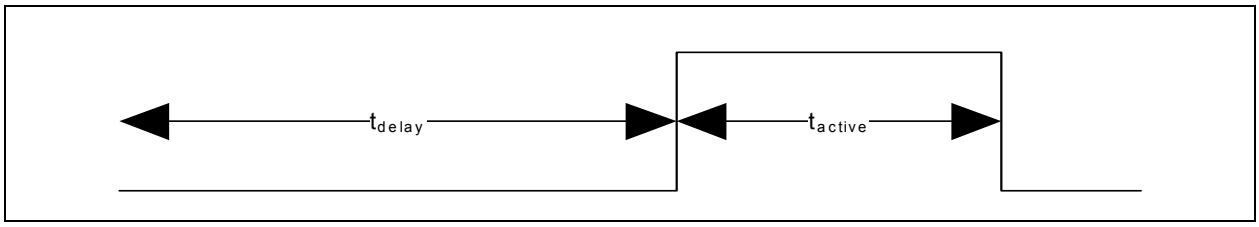

TABLE 51-16: KBRST TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t_{delay}	Delay prior to active pulse	14	15	15.5	µs
t_{active}	Active pulse width	6	8	8.5	µs

The KBRST pin is the CPU_RESET signal described in Section 12.11.2, "CPU_RESET Hardware Speed-Up"

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51.15 Keyboard Scan Matrix Timing

TABLE 51-17: ACTIVE PRE DRIVE MODE TIMING

Parameter	Symbol	Value			Units	Notes
		MIN	TYP	MAX		
Active Predrive Mode	$t_{PREDRIVE}$		41.7		ns	

Note: The TYP value is based on two 48 MHz PLL clocks. The MIN and MAX values are dependent on the accuracy of the 48 MHz PLL.

51.16 PS/2 Timing

FIGURE 51-20: PS/2 TRANSMIT TIMING

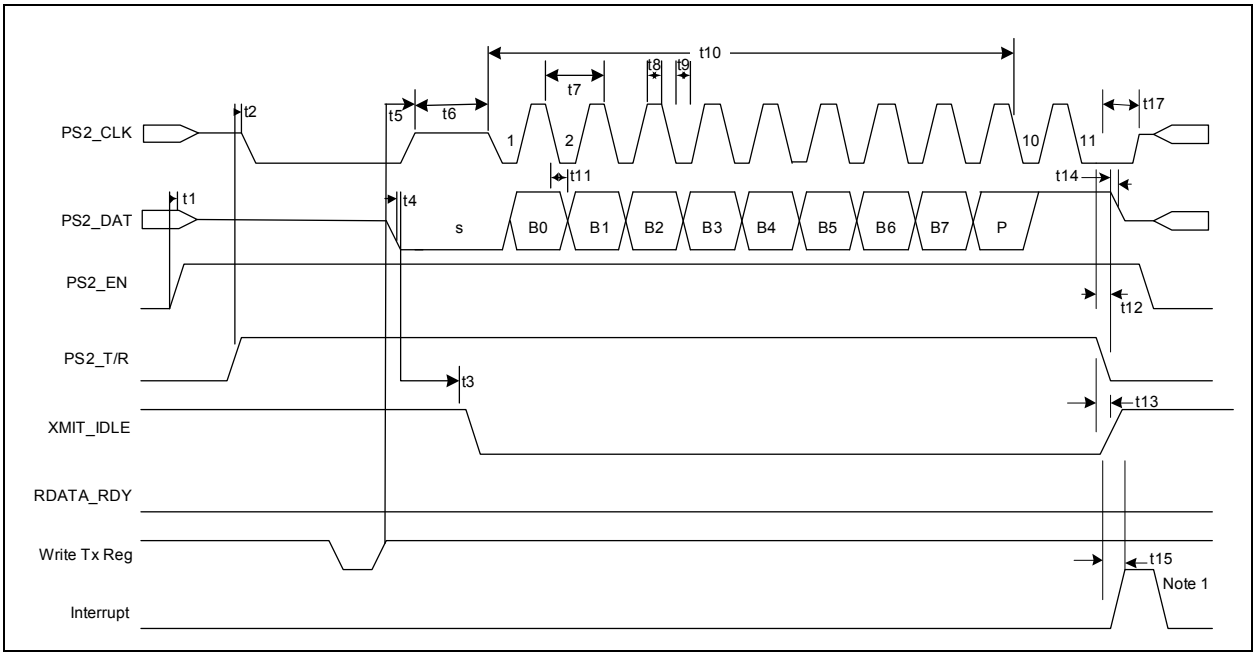

TABLE 51-18: PS/2 CHANNEL TRANSMISSION TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	The PS/2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			1000	ns
t2	PS2_T/R bit set to CLK driven low preparing the PS/2 Channel for data transmission.				
t3	CLK line floated to XMIT_IDLE bit deasserted.			1.7	
t4	Trailing edge of WR to Transmit Register to DATA line driven low.	45		90	
t5	Trailing edge of EC WR of Transmit Register to CLK line floated.	90		130	ns
t6	Initiation of Start of Transmit cycle by the PS/2 channel controller to the auxiliary peripheral's responding by latching the Start bit and driving the CLK line low.	0.002		25.003	ms
t7	Period of CLK	60		302	µs
t8	Duration of CLK high (active)	30		151	
t9	Duration of CLK low (inactive)				

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TABLE 51-18: PS/2 CHANNEL TRANSMISSION TIMING PARAMETERS (CONTINUED)

Name	Description	MIN	TYP	MAX	Units
t10	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t11	DATA output by MEC170x following the falling edge of CLK. The auxiliary peripheral device samples DATA following the rising edge of CLK.			1.0	µs
t12	Rising edge following the 11th falling clock edge to PS_T/R bit driven low.	3.5		7.1	µs
t13	Trailing edge of PS_T/R to XMIT_IDLE bit asserted.			500	ns
t14	DATA released to high-Z following the PS2_T/R bit going low.				
t15	XMIT_IDLE bit driven high to interrupt generated.				
t17	Trailing edge of CLK is held low prior to going high-Z				

FIGURE 51-21: PS/2 RECEIVE TIMING

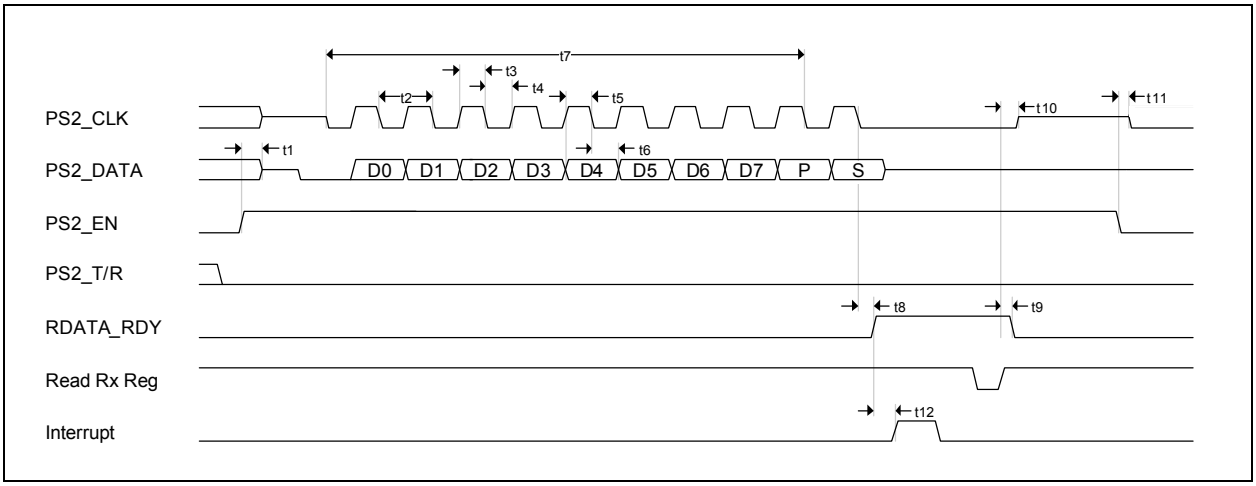

TABLE 51-19: PS/2 CHANNEL RECEIVE TIMING DIAGRAM PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	The PS/2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			1000	ns
t2	Period of CLK	60		302	µs
t3	Duration of CLK high (active)	30		151	
t4	Duration of CLK low (inactive)				
t5	DATA setup time to falling edge of CLK. MEC170x samples the data line on the falling CLK edge.	1			
t6	DATA hold time from falling edge of CLK. MEC170x samples the data line on the falling CLK edge.	2			
t7	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t8	Falling edge of 11th CLK to RDATA_RDY asserted.			1.6	µs
t9	Trailing edge of the EC's RD signal of the Receive Register to RDATA_RDY bit de-asserted.			500	ns
t10	Trailing edge of the EC's RD signal of the Receive Register to the CLK line released to high-Z.				
t11	PS2_CLK is "Low" and PS2_DATA is "Hi-Z" when PS2_EN is de-asserted.				
t12	RDATA_RDY asserted an interrupt is generated.				

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51.17 PWM Timing

FIGURE 51-22: PWM OUTPUT TIMING

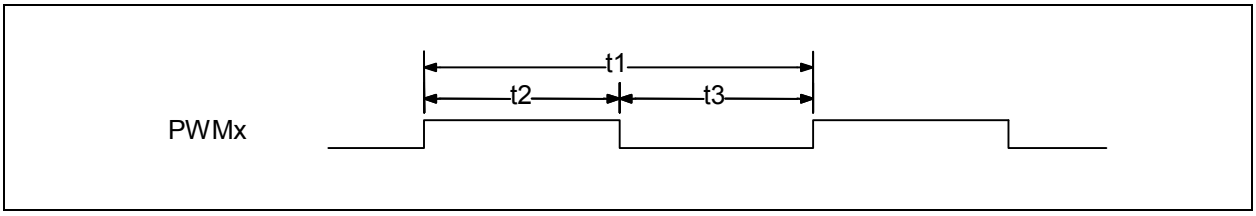

TABLE 51-20: PWM TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	Period	42ns		23.3sec	
t_f	Frequency	0.04Hz		24MHz	
t2	High Time	0		11.65	sec
t3	Low Time	0		11.65	sec
t_d	Duty cycle	0		100	%

51.18 Fan Tachometer Timing

FIGURE 51-23: FAN TACHOMETER INPUT TIMING

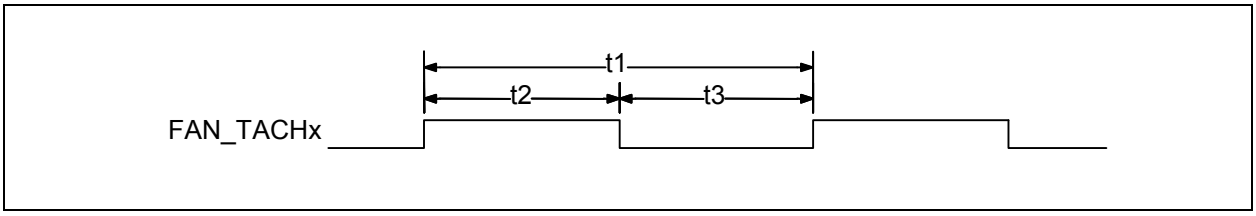

TABLE 51-21: FAN TACHOMETER INPUT TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	Pulse Time	100			µsec
t2	Pulse High Time	20			
t3	Pulse Low Time	20			
Note:	t_{TACH} is the clock used for the tachometer counter. It is 30.52 * prescaler, where the prescaler is programmed in the Fan Tachometer Timebase Prescaler register.				

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51.19 Blinking/Breathing PWM Timing

FIGURE 51-24: BLINKING/BREATHING PWM OUTPUT TIMING

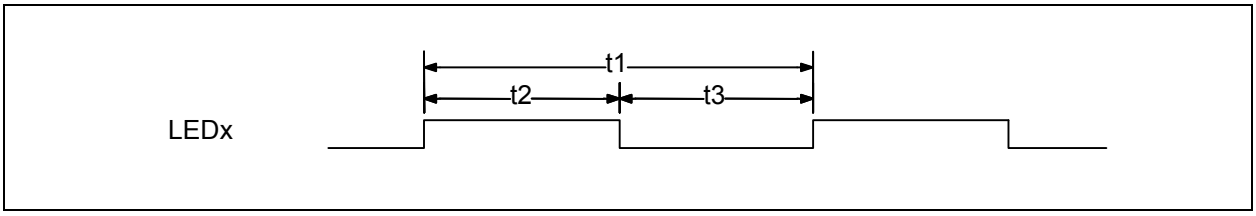

TABLE 51-22: BLINKING/BREATHING PWM TIMING PARAMETERS, BLINKING MODE

Name	Description	MIN	TYP	MAX	Units
t1	Period	7.8ms		32sec	
t_f	Frequency	0.03125		128	Hz
t2	High Time	0		16	sec
t3	Low Time	0		16	sec
t_d	Duty cycle	0		100	%

TABLE 51-23: BLINKING/BREATHING PWM TIMING PARAMETERS, GENERAL PURPOSE

Name	Description	MIN	TYP	MAX	Units
t1	Period	5.3µs		21.8ms	
t_f	Frequency	45.8Hz		187.5kHz	
t2	High Time	0		10.9	ms
t3	Low Time	0		10.9	ms
t_d	Duty cycle	0		100	%

51.20 I2C/SMBus Timing

FIGURE 51-25: I2C/SMBUS TIMING

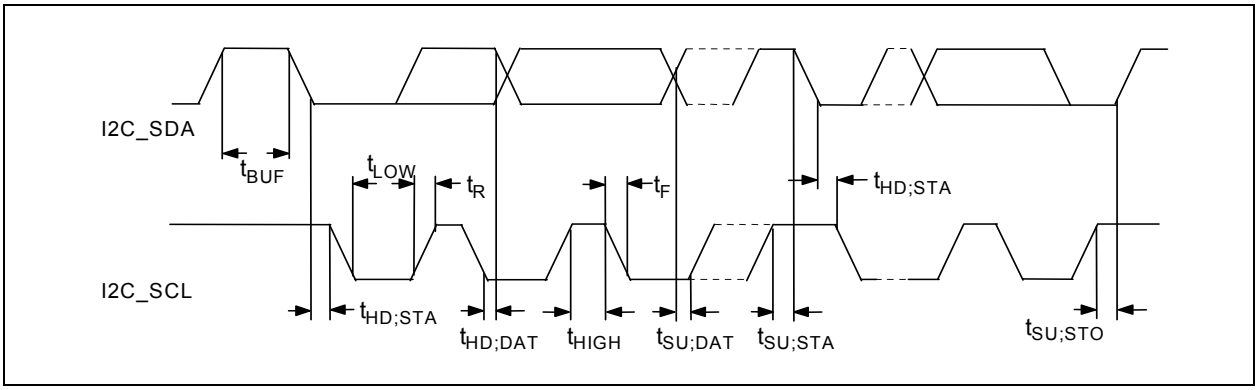

TABLE 51-24: I2C/SMBUS TIMING PARAMETERS

Symbol	Parameter	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL Clock Frequency		100		400		1000	kHz
t_{BUF}	Bus Free Time	4.7		1.3		0.5		µs
$t_{SU;STA}$	START Condition Set-Up Time	4.7		0.6		0.26		µs
$t_{HD;STA}$	START Condition Hold Time	4.0		0.6		0.26		µs
t_{LOW}	SCL LOW Time	4.7		1.3		0.5		µs
t_{HIGH}	SCL HIGH Time	4.0		0.6		0.26		µs
t_R	SCL and SDA Rise Time		1.0		0.3		0.12	µs
t_F	SCL and SDA Fall Time		0.3		0.3		0.12	µs
$t_{SU;DAT}$	Data Set-Up Time	0.25		0.1		0.05		µs
$t_{HD;DAT}$	Data Hold Time	0		0		0		µs
$t_{SU;STO}$	STOP Condition Set-Up Time	4.0		0.6		0.26		µs

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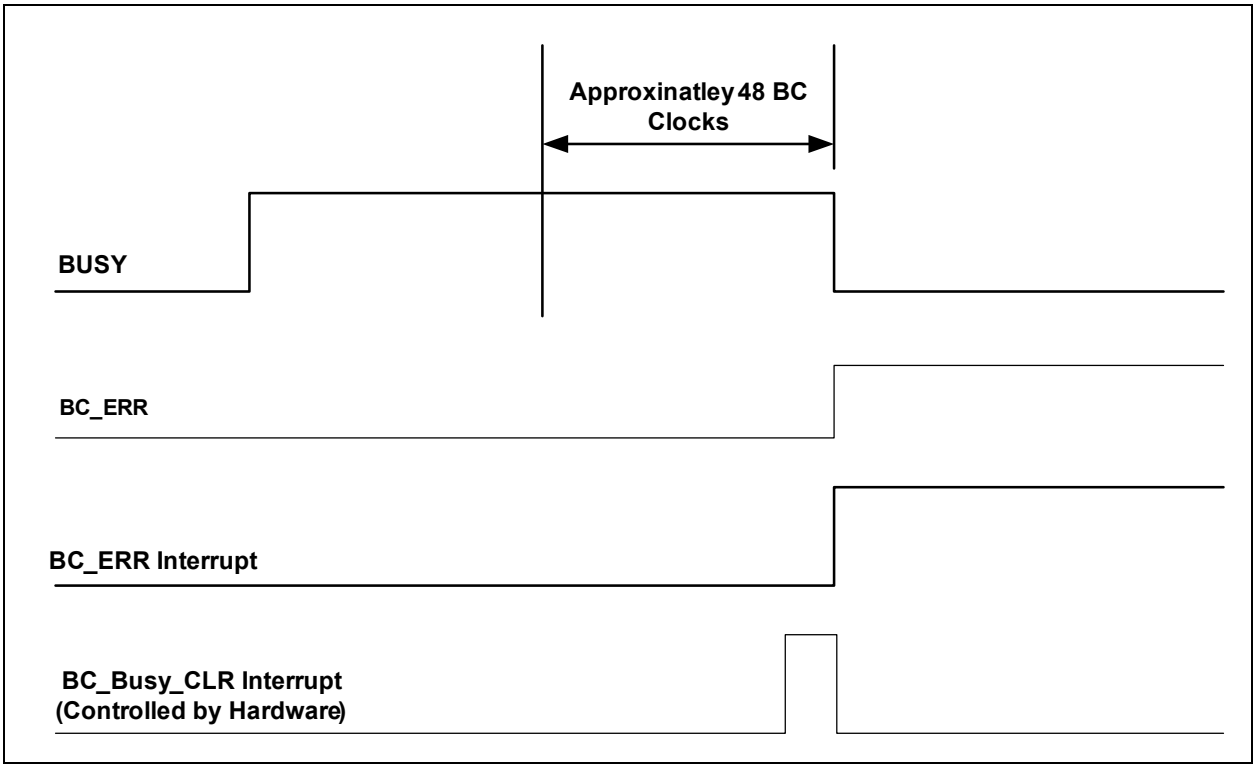
51.21 BC-Link Master Interrupt Timing

FIGURE 51-26: BC-LINK ERR INTERRUPT TIMING



51.22 BC-Link Master Timing

FIGURE 51-27: BC-LINK READ TIMING

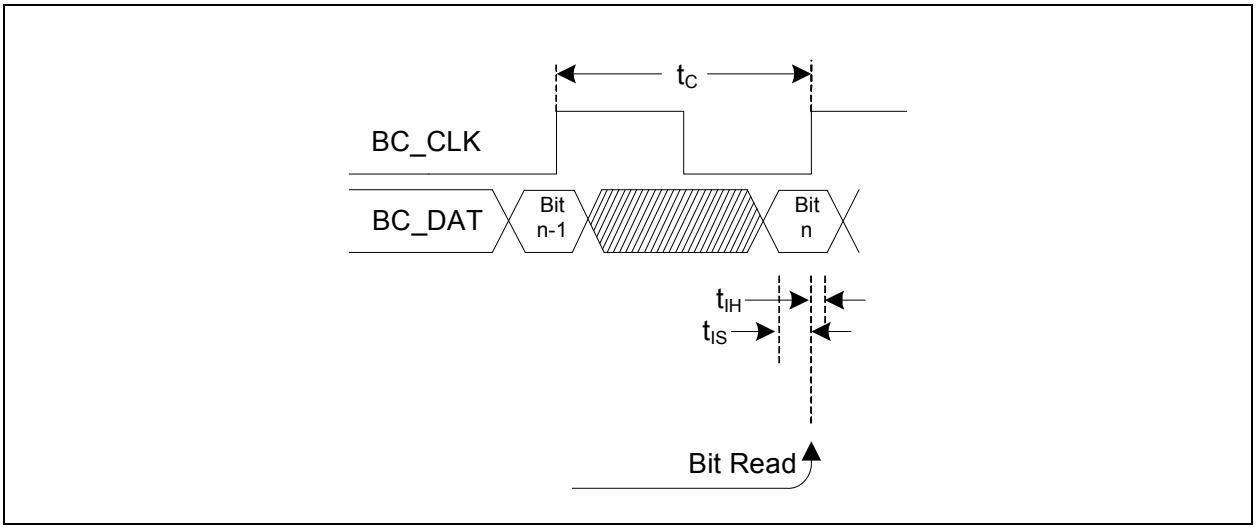


FIGURE 51-28: BC-LINK WRITE TIMING

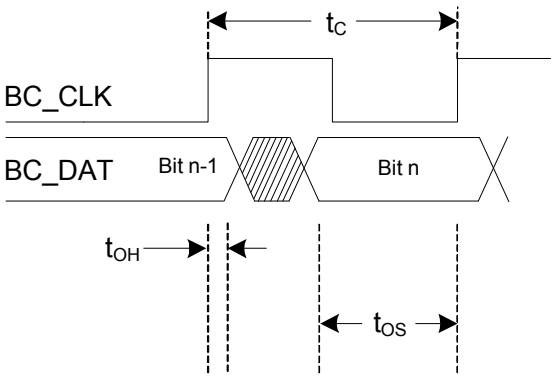


TABLE 51-25: BC-LINK MASTER TIMING DIAGRAM PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t_C	BC Clock Frequency			24	MHz
t_f	BC Clock Period	42			ns
t_{OS}	BC-Link Master DATA output setup time before rising edge of CLK.			t_c-t_{OH-MAX}	nsec
t_{OH}	BC-Link Master Data hold time after falling edge of CLK			10	nsec
t_{IS}	BC-Link Master DATA input setup time before rising edge of CLK.	15			nsec
t_{IH}	BC-Link Master DATA input hold time after rising edge of CLK.	0			nsec

Note 1: The (t_{IH} in Table 51-25) BC-Link Master DATA input must be stable before next rising edge of CLK.

2: The BC-Link Clock frequency is limited by the application usage model (see BC-Link Master Section 40.5, "Signal Description"). The BC-Link Clock frequency is controlled by the BC-Link Clock Select Register. The timing budget equation is as follows for data from BC-Link slave to master:

Tc > TOD(master-clk) + Tprop(clk) +TOD(slave) + Tprop(slave data) + TIS(master).

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51.23 Quad SPI Master Controller - Serial Peripheral Interface (QMSPI) Timings

FIGURE 51-29: SPI CLOCK TIMING

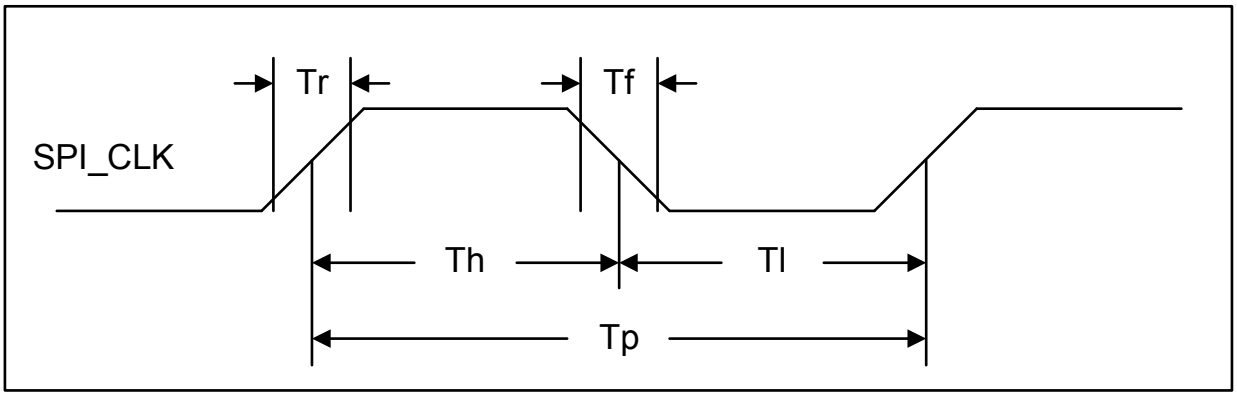
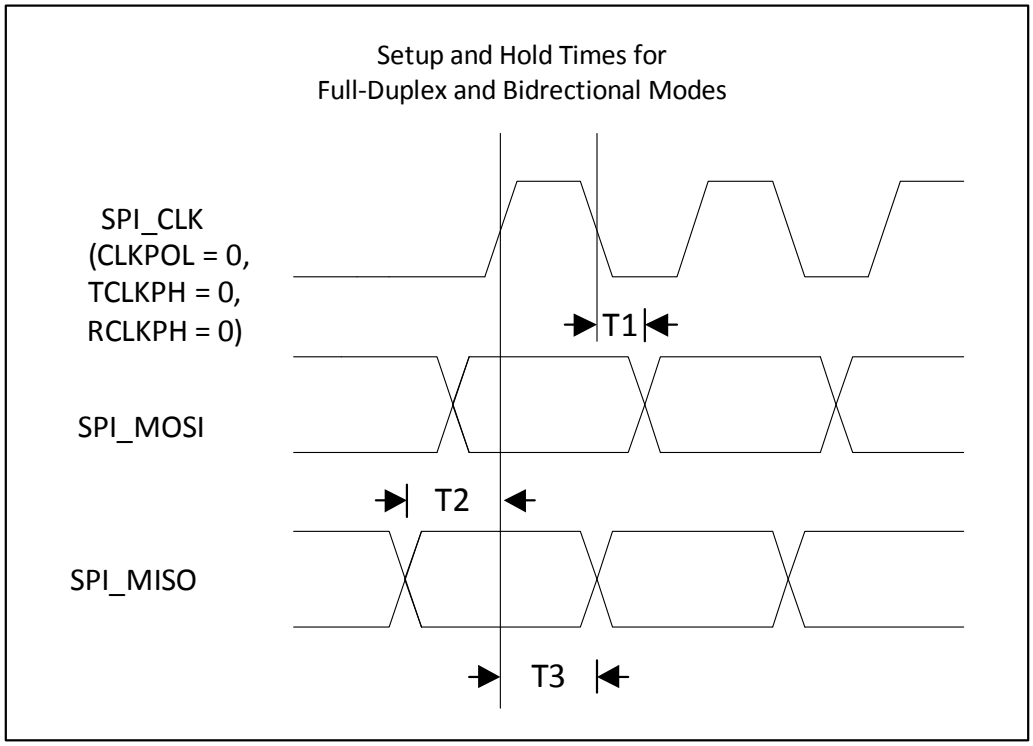


TABLE 51-26: SPI CLOCK TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
Tr	SPI Clock Rise Time. Measured from 10% to 90%.			3	ns
Tf	SPI Clock Fall Time. Measured from 90% to 10%.			3	ns
Th/Tl	SPI Clock High Time/SPI Clock Low Time	40% of SPCLK Period	50% of SPCLK Period	60% of SPCLK Period	ns
Tp	SPI Clock Period – As selected by SPI Clock Generator Register	20.8		5,333	ns
Note:	Test conditions are as follows: output load is C_L=30pF, pin drive strength setting is 4mA and slew rate setting is slow.				

FIGURE 51-30: SPI SETUP AND HOLD TIMES



Note:	SPI_IO[3:0] obey the SPI_MOSI and SPI_MISO timing. In the 2-pin SPI Interface implementation, SPI_IO0 pin is the SPI Master-Out/Slave-In (MOSI) pin and the SPI_IO1 pin is the Master-In/Slave-out (MISO) pin.

TABLE 51-27: SPI SETUP AND HOLD TIMES PARAMETERS

Name	Description	MIN	TYP	MAX	Units
T1	Data Output Delay			2	ns
T2	Data IN Setup Time	5.5			ns
T3	Data IN Hold Time	0			ns
Note:	Test conditions are as follows: output load is C_L=30pF, pin drive strength setting is 4mA and slew rate setting is slow				

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51.24 General Purpose Serial Peripheral Interface (GP-SPI) Timings

Note that the following timing applies to all of the MEC170x Serial Peripheral Interface functions.

FIGURE 51-31: SPI CLOCK TIMING

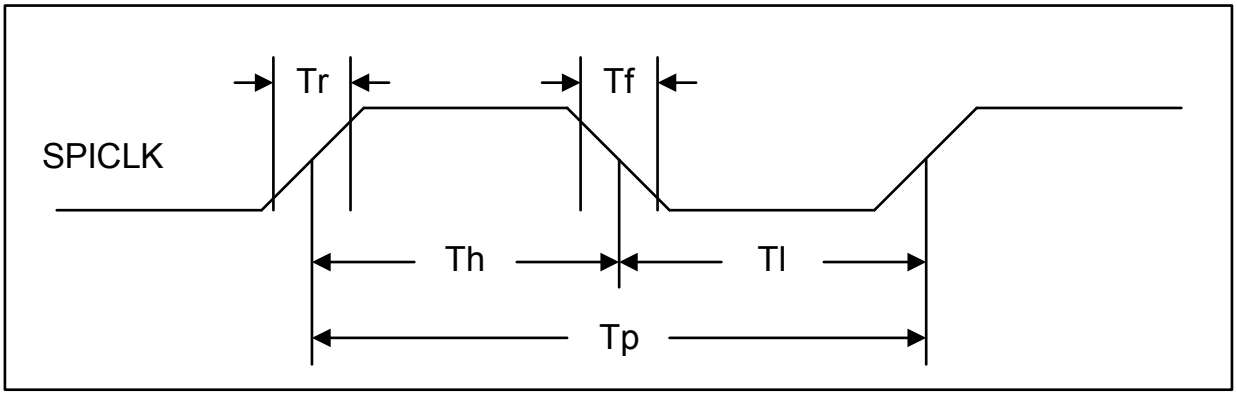
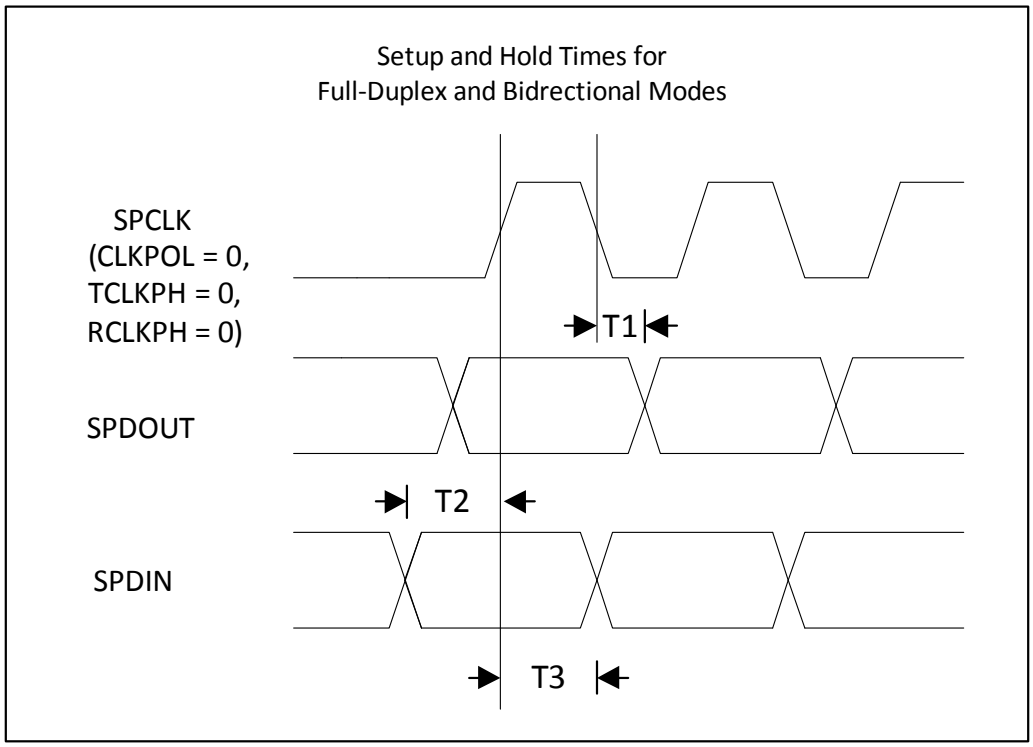


TABLE 51-28: SPI CLOCK TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
Tr	SPI Clock Rise Time. Measured from 10% to 90%.			3	ns
Tf	SPI Clock Fall Time. Measured from 90% to 10%.			3	ns
Th/Tl	SPI Clock High Time/SPI Clock Low Time	40% of SPCLK Period	50% of SPCLK Period	60% of SPCLK Period	ns
Tp	SPI Clock Period – As selected by SPI Clock Generator Register	20.8		62500	ns
Note:	Test conditions are as follows: output load is C_L=30pF, pin drive strength setting is 4mA and slew rate setting is slow.				

FIGURE 51-32: SPI SETUP AND HOLD TIMES



Note:	SPI IO[3:0] obey the SPI_MOSI and SPI_MISO timing. In the 2-pin SPI Interface implementation, SPI_IO0 pin is the SPI Master-Out/Slave-In (MOSI) pin and the SPI_IO1 pin is the Master-In/Slave-out (MISO) pin.

TABLE 51-29: SPI SETUP AND HOLD TIMES PARAMETERS

Name	Description	MIN	TYP	MAX	Units
T1	Data Output Delay			2	ns
T2	Data IN Setup Time	5.5			ns
T3	Data IN Hold Time	0			ns
Note:	Test conditions are as follows: output load is C_L=30pF, pin drive strength setting is 4mA and slew rate setting is slow				

51.24.1 SPI INTERFACE TIMINGS

The following timing diagrams represent a single-byte transfer over the SPI interface using different SPCLK phase settings. Data bits are transmitted in bit order starting with the MSB (LSBF='0') or the LSB (LSBF='1'). See the SPI Control Register for information on the LSBF bit. The CS signal in each diagram is a generic bit-controlled chip select signal required by most peripheral devices. This signal and additional chip selects can be GPIO controlled. Note that these timings for Full Duplex Mode are also applicable to Half Duplex (or Bi-directional) mode.

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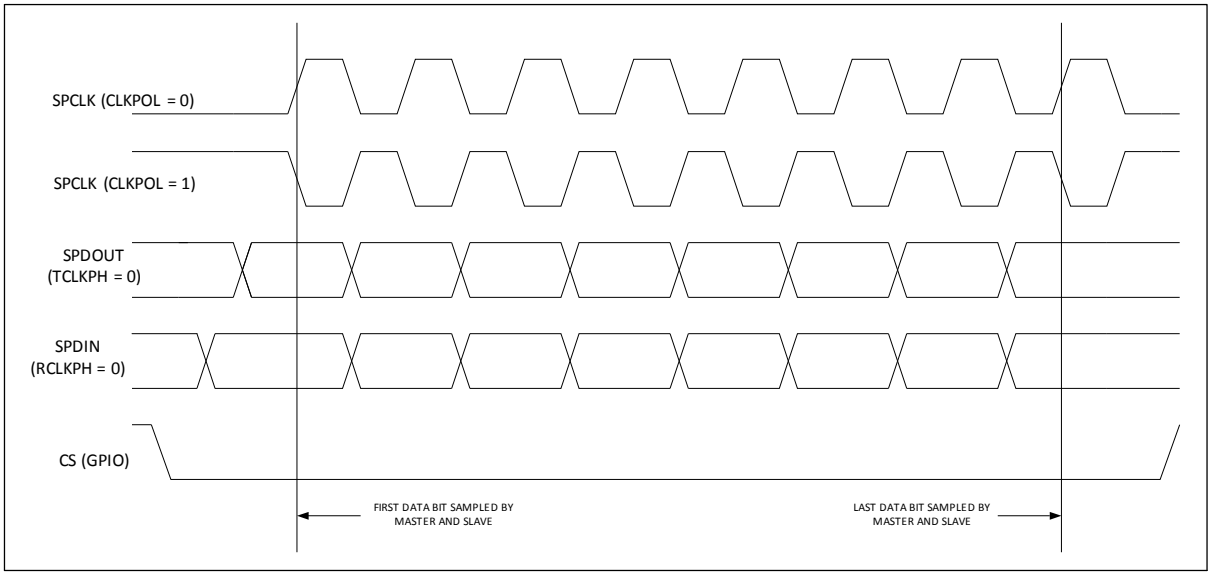
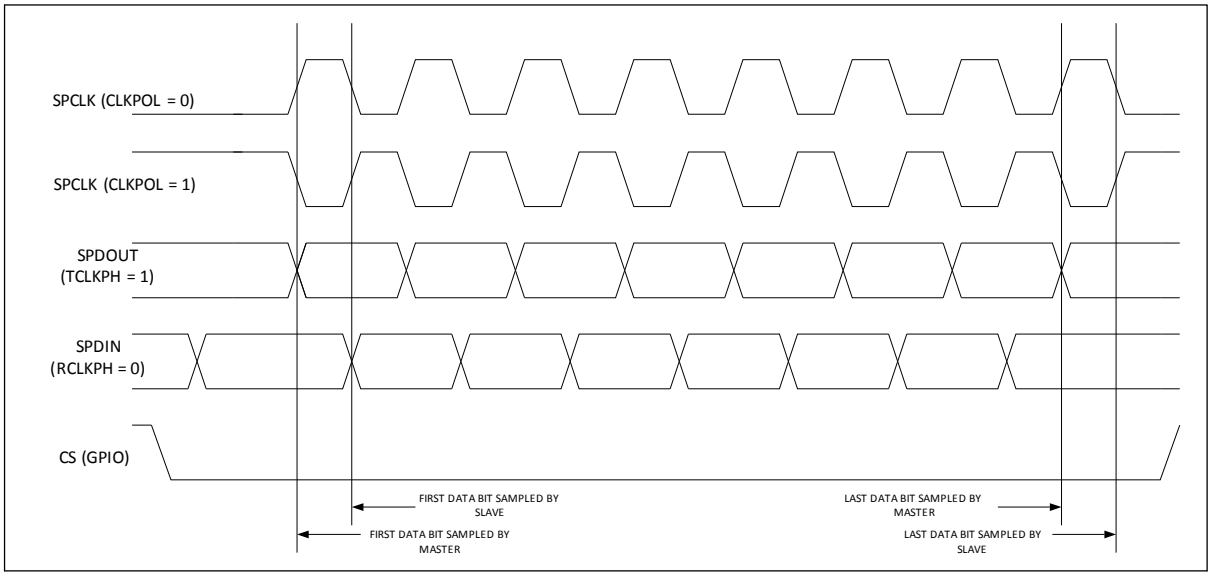
FIGURE 51-33: INTERFACE TIMING, FULL DUPLEX MODE (TCLKPH = 0, RCLKPH = 0)



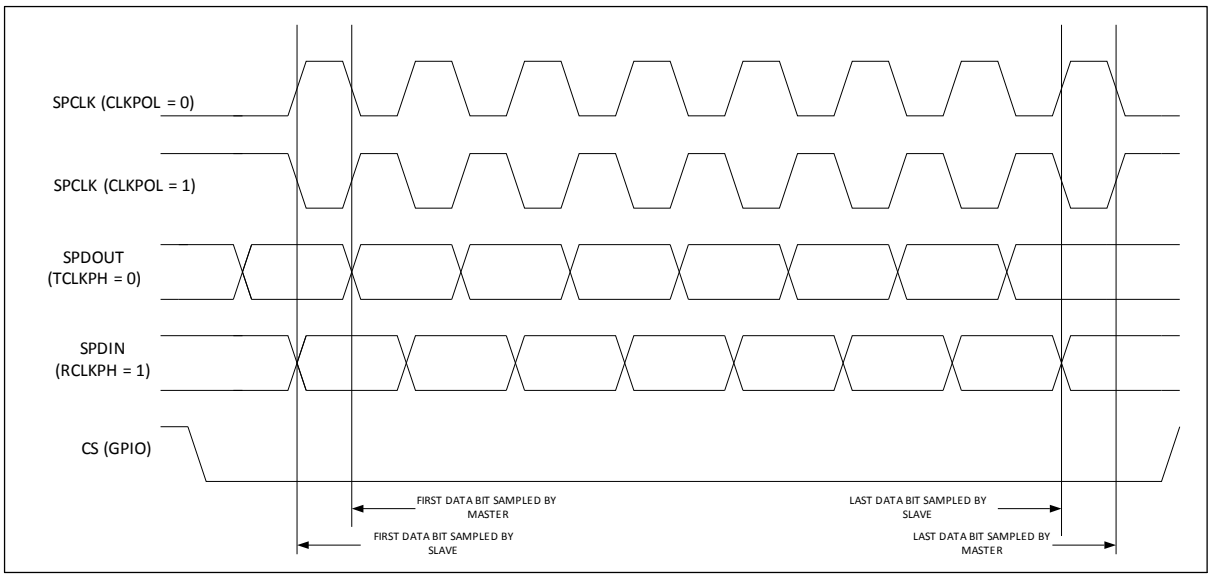
In this mode, data is available immediately when a device is selected and is sampled on the first and following odd SPCLK edges by the master and slave.

FIGURE 51-34: SPI INTERFACE TIMING, FULL DUPLEX MODE (TCLKPH = 1, RCLKPH = 0)



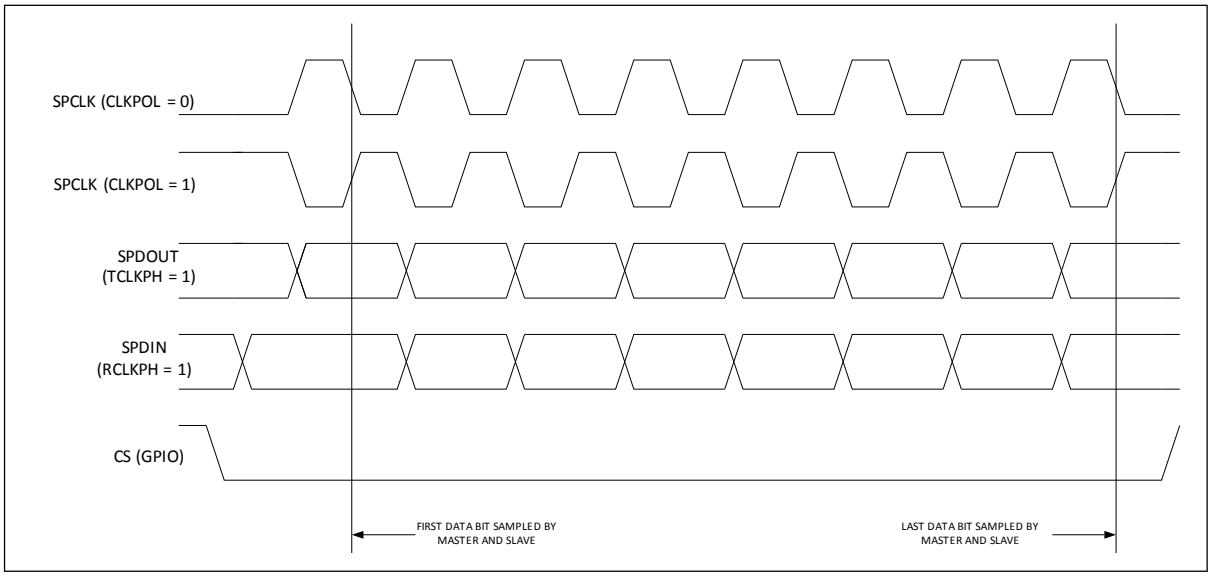
In this mode, the master requires an initial SPCLK edge before data is available. The data from slave is available immediately when the slave device is selected. The.data is sampled on the first and following odd edges by the master. The data is sampled on the second and following even SPCLK edges by the slave.

FIGURE 51-35: SPI INTERFACE TIMING, FULL DUPLEX MODE (TCLKPH = 0, RCLKPH = 1)



In this mode, the data from slave is available immediately when the slave device is selected. The slave device requires an initial SPCLK edge before data is available. The data is sampled on the second and following even SPCLK edges by the master. The data is sampled on the first and following odd edges by the slave.

FIGURE 51-36: SPI INTERFACE TIMING - FULL DUPLEX MODE (TCLKPH = 1, RCLKPH = 1)



In this mode, the master and slave require an initial SPCLK edge before data is available. Data is sampled on the second and following even SPCLK edges by the master and slave.

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51.25 Serial Debug Port Timing

FIGURE 51-37: SERIAL DEBUG PORT TIMING PARAMETERS

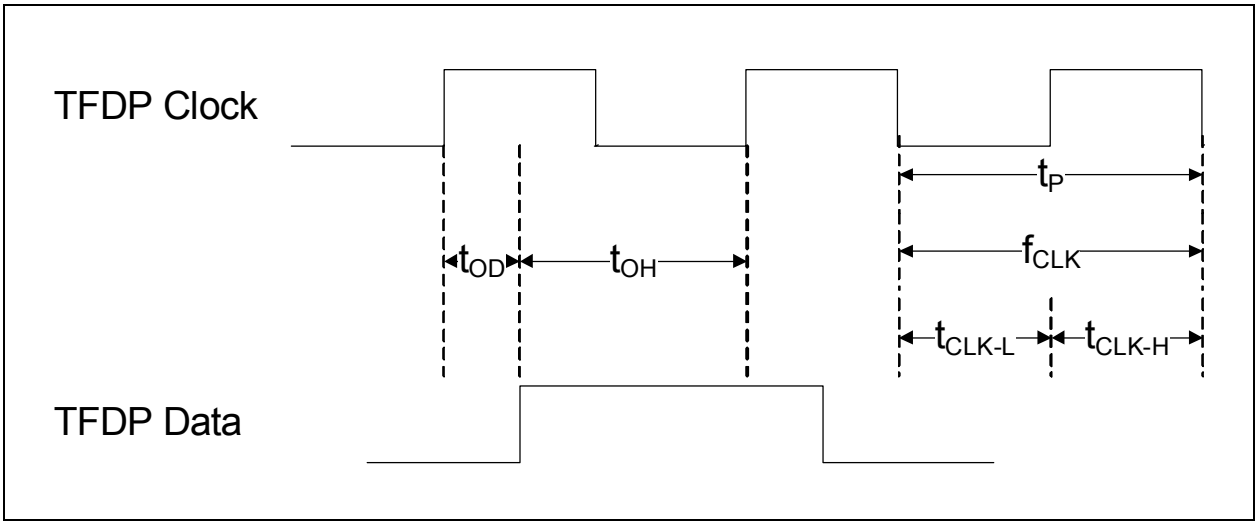

TABLE 51-30: SERIAL DEBUG PORT INTERFACE TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
f_{clk}	TFDP Clock frequency (see note)	2.5	-	24	MHz
t_P	TFDP Clock Period.	1/fclk			µs
t_{OD}	TFDP Data output delay after falling edge of TFDP_CLK.			5	nsec
t_{OH}	TFDP Data hold time after falling edge of TFDP Clock	$t_P - t_{OD}$			nsec
t_{CLK-L}	TFDP Clock Low Time	$t_P/2 - 3$		$t_P/2 + 3$	nsec
t_{CLK-H}	TFDP Clock high Time (see Note 1)	$t_P/2 - 3$		$t_P/2 + 3$	nsec

Note 1: When the clock divider for the embedded controller is an odd number value greater than 2h, then $t_{CLK-L} = t_{CLK-H} + 15$ ns. When the clock divider for the embedded controller is 0h, 1h, or an even number value greater than 2h, then $t_{CLK-L} = t_{CLK-H}$.

51.26 JTAG Interface Timing

FIGURE 51-38: JTAG POWER-UP & ASYNCHRONOUS RESET TIMING

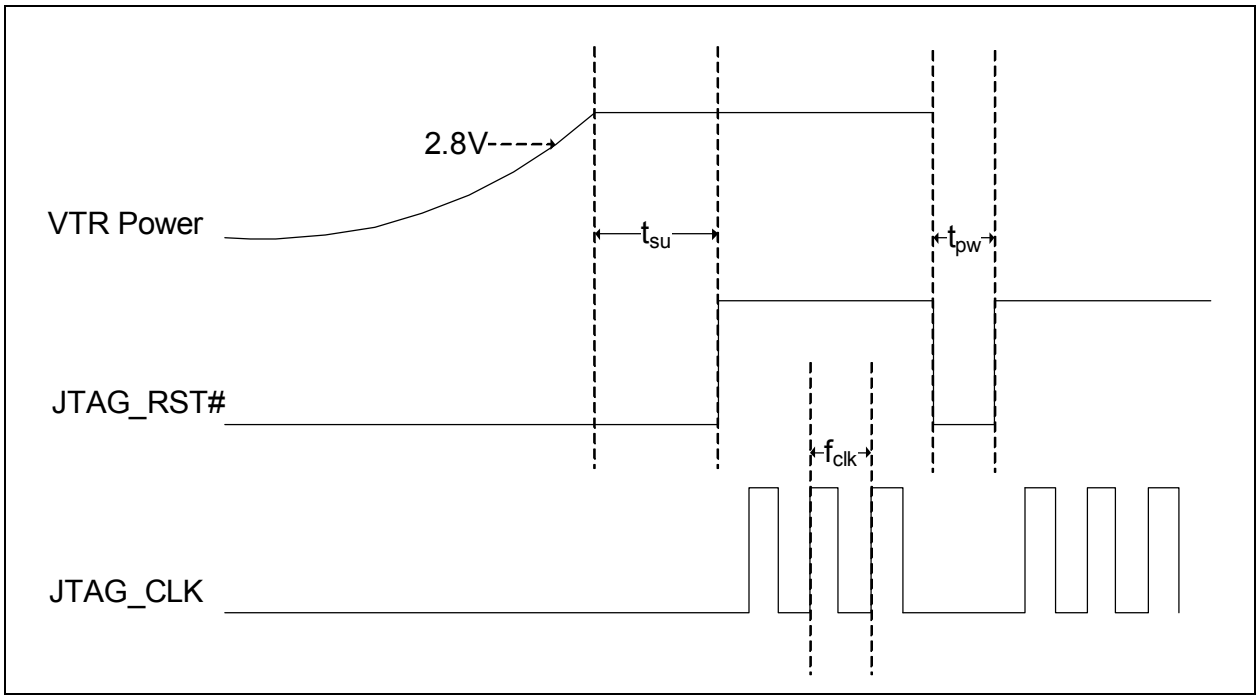

FIGURE 51-39: JTAG SETUP & HOLD PARAMETERS

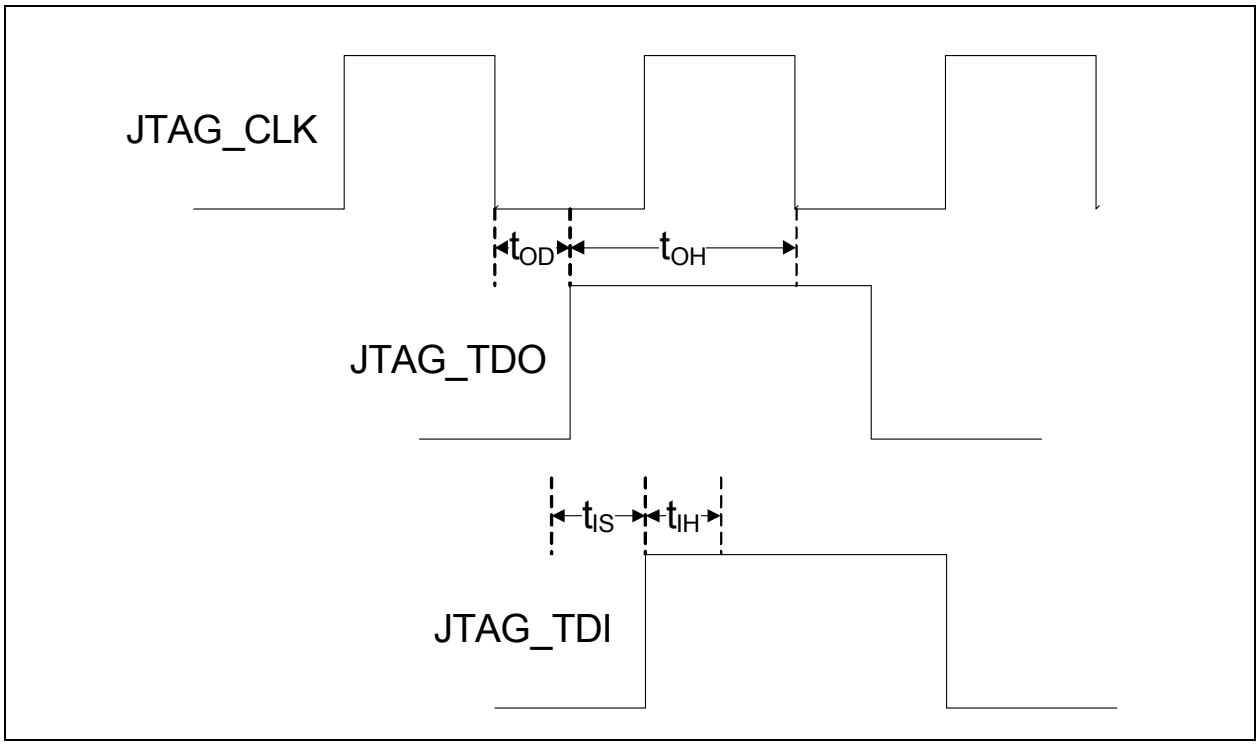

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TABLE 51-31: JTAG INTERFACE TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t_{su}	JTAG_RST# de-assertion after VTR power is applied	5			ms
t_{pw}	JTAG_RST# assertion pulse width	500			nsec
f_{clk}	JTAG_CLK frequency (see note)			48	MHz
t_{OD}	TDO output delay after falling edge of TCLK.	5		10	nsec
t_{OH}	TDO hold time after falling edge of TCLK	1 TCLK - t_{OD}			nsec
t_{IS}	TDI setup time before rising edge of TCLK.	5			nsec
t_{IH}	TDI hold time after rising edge of TCLK.	5			nsec

Note: f_{clk} is the maximum frequency to access a JTAG Register.

APPENDIX A: DATA SHEET REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002206C (10-31-17)	Document Features and Section 47.10.2, "Cryptographic Hashing," on page 581	Added SHA-384.
	Table 1-1, “MEC170x Feature List by Package,” on page 6	Added UPD Dead Battery Support in 169-pin package of MEC1701 and MEC1703.
	Section 2.8, "UPD Dead Battery Interface Pins," on page 60	Added pin information for UPD Dead Battery Interface.
	Section 2.9, "Strapping Options," on page 61	Added UPD Strap Options.
	Product Identification System on page 645	Changed MEC1704 Product Identification to “Industrial Embedded Controller” and MEC1705 Product Identification to “Industrial Embedded Controller with EEPROM Integration”.
	Section 50.2.3, "Capacitive Loading Specifications," on page 593	Changed “VCC” to “VTR”.
	Section 49.7.1, "eFUSE Programming Sequence," on page 586	Programming voltage corrected to be in the range of 1.52V to 1.60.
	Section 4.4.2, "Battery Circuit Requirements," on page 136	“Ground” changed to “Discharge”.
	Removed “BGND” signal from data sheet.	
	Section 2.4.1, "Default State," on page 12	Changed default of GPIO064 to “LRESET#”.
	Section 49.8, "eFuse Memory Map," on page 587	Modified eFuse block.
	Section 46.8.12, "GPIO Bank Power Register," on page 574	Added note below section.
	Table 50-3, “DC Electrical Characteristics,” on page 595	Updated I0L and I0H values.
	Section 2.3, "Notes for Tables in this Chapter," on page 11	Added Note 16.
	Table 17-5, “Reset Signals,” on page 306 and Section 17.11.2, "Configuration Select Register," on page 321	Removed “RESET_VCC” from table; Changed bit1 to reserved and added note to customer to change this register to “0”.
	Table 50-4, Table 50-5, Table 50-6, Table 50-7 and Table 50-11	Added characterization information for Industrial part.
	Section 2.4.1, "Default State," on page 12Section 2.5.8, "MEC1705/MEC1704/MEC1701/MEC1703 144 wFBGA," on page 20	Added MEC1704 144 WFBGA pinout details.
	Section 50.1.1, "Absolute Maximum Thermal Ratings," on page 592	Added MEC1704 to the list of supported devices for industrial temperature rating.

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Revision	Section/Figure/Entry	Correction
	Table 1-1, “MEC170x Feature List by Package,” on page 6	Modified MEC1701 144 pin WFBGA UART to have 2 pin UART.
DS00002206B (03-03-17)	Updated to reflect Functional Rev C.	
DS00002206A (07-19-16)	Document Release	

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PART NO.[1]	-	X	-	XX	-	X[4]/XXX[2]	-	[X][3]
Device		Total SRAM		Version/ Revision		Temp Range/ Package		Tape and Reel Option

Device:	MEC1701[1]	Embedded Controller
	MEC1703[1]	Embedded Controller with EEPROM Integration
	MEC1705[1]	Industrial Embedded Controller with EEPROM Integration
	MEC1704[1]	Industrial Embedded Controller
Total SRAM	H	256KB
	K	320KB
	Q	480KB
Version/ Revision:	C#	C = Standard Version, # = Version Revision Number
Temperature Range	Blank	= 0°C to +70°C (Commercial)
	I/	= -40°C to +85°C (Industrial)
Package:	SZ	144 pin WFBGA[2], 9mm x 9mm body, 0.65mm pitch
	TN	169 pin WFBGA[2)], 11mm x 11mm body, 0.8mm pitch
	9S	169 pin XFBGA[2], 8mm x 8mm body, 0.5mm pitch
Tape and Reel Option:	Blank	= Tray packaging
	TR	= Tape and Reel[3]

Examples:

a) MEC1701H-C1-SZ = MEC1701, 256KB total SRAM, Standard ROM, ROM Version 1, 144-WFBGA, Tray packaging

b) MEC1701K-C1-TN-TR = MEC1701, 320KB total SRAM, Standard ROM, ROM Version 1, 169-WFBGA, Tape and Reel packaging

c) MEC1705Q-C1-I/SZ-TR = MEC1705,480KB total SRAM, Standard ROM,ROM Version 1, Industrial Temp,144-WFBGA, Tape and Reel Packaging

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html

3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option

4: Industrial Temperature is supported only by CEC1702, MEC1705 and MEC1704

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