*Click **here** to ask about the production status of specific part numbers.*

MAX14914, MAX14914A, MAX14914B

High-Side Switch with Settable Current-Limiting, Push-Pull Driver Option and Digital Input Configuration

General Description

The MAX14914, MAX14914A and MAX14914B are the family of high-side/push-pull drivers that operate as both an industrial digital output (DO) and an industrial digital input (DI). The MAX14914 family features full IEC 61131-2 compliance in both their DO and DI modes of operation. The high-side switch current is resistor settable from 135mA (min) to 1.3A (min). The high-side driver's on-resistance is 120mΩ (typ) at 125°C ambient temperature. Optional push-pull operation allows driving of cables and fast discharge of load capacitance. The output voltage is monitored and indicated through the $\overline{DOI\_LVL}$ pin for safety applications.

The MAX14914 family complies with Type 1, Type 2, or Type 3 input characteristics when configured for DI operation.

The MAX14914A is a low-DOI-leakage version of MAX14914, designed to work together with the MAX22000 Industrial Configurable Analog IO device. The MAX14914B features a high-side switch overcurrent indication.

Applications

- Industrial Digital Outputs and Inputs Modules
- Configurable Digital Input/Output
- Motor Control
- Safety Systems

Benefits and Features

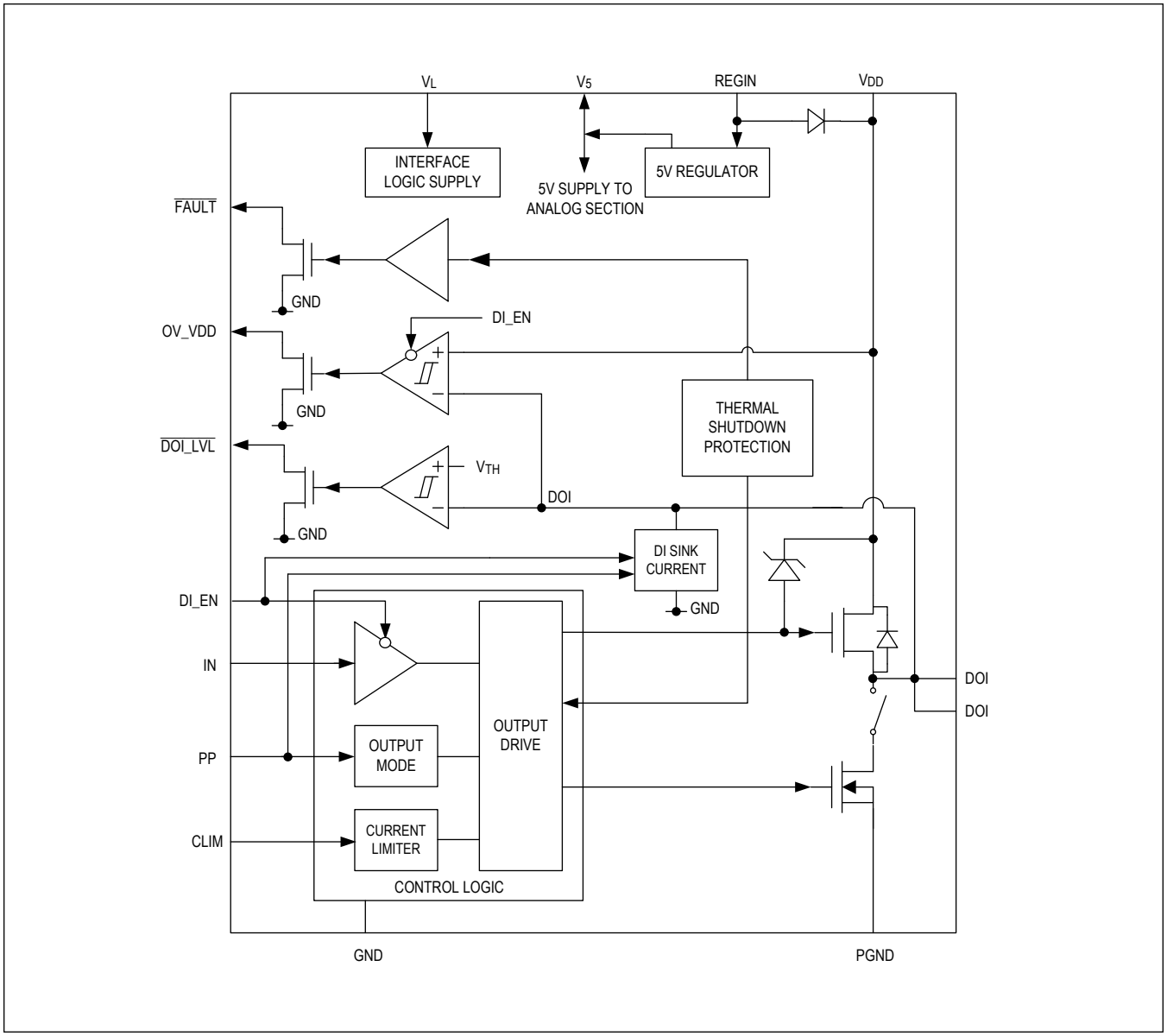
- Reduces Power and Heat Dissipation
  - 240mΩ (max) HS R_{ON} at T_A = 125°C
  - 0.9mA (typ) High-Side DO-Mode Supply Current
  - Accurate Internal Current Limiter for Type 1, Type 2, and Type 3 Digital Inputs
- Enhances System Robustness
  - SafeDemag™ for Safe Turn-Off of Unlimited Inductance
  - 60V Supply Tolerance
  - Accurate Short-Circuit DO Mode Current Limiting
  - ±2kV IEC 61000-4-5 Surge Protection
  - ±20kV IEC 61000-4-2 Air-Gap ESD Protection
  - ±7kV IEC 61000-4-2 Contact ESD Protection
  - -40°C to +125°C Ambient Operating Temperature
- Reduces BOM Count and PCB Space
  - Small 4mm x 4mm TQFN Package
  - Internal Clamp for Fast Inductive Load Turn-Off
  - On-Chip 5V Regulator
- Provides Flexibility
  - Configurable as a Digital Input, or a High-Side or Push-Pull Digital Output
  - Low-Leakage Mode (MAX14914A) Allows High Accuracy AIO/DIO applications
  - Resistor Settable Current Limiting for the High-Side Switch (135mA to 1.3A)
  - Pin-Selectable Type 1/3 or Type 2 DI Operation
- Improves System Speed and Throughput
  - Propagation Delay of Less Than 2µs

***Ordering Information* and *Typical Application Diagram* appears at end of data sheet.**

19-8712; Rev 4; 9/20

maxim integrated™

Block Diagram of MAX14914 and MAX14914A



Absolute Maximum Ratings

V_{DD} ..... -0.3V to +65V
REGIN ..... -0.3V to lower of +65V and (V_{DD} + 0.3V)
PGND ..... -0.3V to +0.3V
DOI (V_{DD} < V_{DD_OVLOTH}) ..... (V_{DD} - 49V) to (V_{DD} + 0.3V)
DOI (V_{DD} > V_{DD_OVLOTH}) ..... -1V to (V_{DD} + 0.3V)
V_5 ..... -0.3V to lower of +6V and (REGIN + 0.3V)
V_L ..... -0.3V to +6V
IN, PP, DIN_EN, /FAULT, CLIM ..... -0.3V to +6V
$\overline{DOI\_LVL}$ ..... -0.3V to (V_L + 0.3V)
OV_VDD, $\overline{OV\_CURR}$ ... -0.3V to lower of +65V and (V_{DD} + 0.3V)
DOI Load Current ..... Internally Limited
Continuous Current (any other terminal) ..... -100mA to +100mA
Continuous Power Dissipation (T_A = +70°C, derate 28,6mW/°C above +70°C) 2280mW
Inductive Demagnetization Energy (I_{LOAD} < 0.6A) ..... Unlimited
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... Internally Limited
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN

Package Code	T1644+4A
Outline Number	21-0139
Land Pattern Number	90-0070
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	35°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = +10V to +40V, V_5 = +4.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = +25ºC , V_{DD} = +24V, V_L= +3.3V and V_5 = +5V, R_{LIM} = 50kΩ.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} SUPPLY						
Supply Voltage	V_{DD}	Operting Conditions	10		40	V
		Tolerant	0		60	
Supply Current	$I_{DD\_ON\_HS}$	HS mode, PP = low, IN = V_L, DOI high (no switching), no load, V_5 = V_L = REGIN = 5V, V_{DD} = 40V.		0.6	0.95	mA
	$I_{DD\_ON\_PP}$	PP mode, PP = high, 10kHz switching, V_5 = V_L = REGIN = 5V, V_{DD} = 40V, no load		0.85	1.4	
	$I_{DD\_ON\_DI}$	DI mode, DI_EN = V_L, REGIN = V_{DD} = 40V		0.13	0.3	mA

Electrical Characteristics (continued)

(V_{DD} = +10V to +40V, V_5 = +4.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = +25ºC , V_{DD} = +24V, V_L= +3.3V and V_5 = +5V, R_{LIM} = 50kΩ.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage-Lockout Threshold	V_{DD_UVLO}	V_{DD} rising, $V_5 = V_L$	8.5	9.1	9.7	V
	V_{DD_UVLO}	V_{DD} falling, $V_5 = V_L$	8	8.6	9	V
Undervoltage-Lockout Hysteresis	V_{DD_UVHYST}	$V_5 = V_L$		0.5		V
V_{DD} Overvoltage-Lockout Threshold	V_{DD_OVLO}	V_{DD} rising, $V_5 = V_L$	41.5	43.5	45	V
	V_{DD_OVLO}	V_{DD} falling, $V_5 = V_L$	40.5	42.2	44	V
V_{DD} Overvoltage-Lockout Hysteresis	V_{DD_OVHYST}	$V_5 = V_L$		1		V
V_L LOGIC INTERFACE SUPPLY						
V_L Supply Voltage	V_L		2.5		5.5	V
V_L Supply Current	I_L	All logic inputs high or low, all outputs unloaded		10	25	uA
V_L POR Threshold	V_{L_POR}	V_L falling	1.12	1.27	1.52	V
5V SUPPLY / LINEAR REGULATOR						
REGIN Current HS Mode	$I_{REGIN\_ON\_HS}$	HS mode, REGIN = 40V, IN = V_L, no load on DOI, no load on V_5		0.3	0.5	mA
REGIN Current PP Mode	$I_{REGIN\_ON\_PP}$	PP = high, REGIN = 40V, 10kHz switching, no load on DOI, no load on V_5		0.35	0.6	mA
REGIN Current DI Mode	$I_{REGIN\_ON\_DI}$	DI_EN = V_L, REGIN = 40V			0.5	mA
V_5 Supply Current	I_{V5_HS}	HS mode, REGIN = V_5 = 5V, IN = V_L, no load on DOI		0.24	0.4	mA
	I_{V5_PP}	PP mode, REGIN = V_5 = 5V, 10kHz switching, no load on DOI		0.3	0.5	
	I_{V5_DI}	DI mode, DI_EN = high, REGIN = V_5 = 5V		0.22	0.4	
REGIN Undervoltage Threshold	V_{REG_UV}	REGIN rising. V_5 enabled when REGIN > V_{REG_UV}.	6.75		7.6	V
REGIN Undervoltage Hysteresis	V_{REG_UVHYST}			0.45		V
V_5 Undervoltage-Lockout Threshold	V_{5_UVLO}	V_5 rising	3.8		4.2	V
V_5 Undervoltage-Lockout Hysteresis	V_{5UV_UVHYST}			0.3		V
V_5 Output Voltage	V_5	0mA - 20mA external load	4.75	5.0	5.25	V
V_5 Current Limit	I_{V5_CL}		25			mA
DRIVER OUTPUT (DOI)						
HS On-Resistance	$R_{DOI\_ON\_HS}$	PP = X, IN = high, I_{DOI} = 500mA		120	240	mΩ
LS Output Low	V_{DOI_LOW}	PP = high, IN = low, I_{DOI} = 100mA			1.2	V

Electrical Characteristics (continued)

(V_{DD} = +10V to +40V, V_5 = +4.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = +25ºC , V_{DD} = +24V, V_L= +3.3V and V_5 = +5V, R_{LIM} = 50kΩ.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DOI Clamp Voltage	V_{DOI_CL}	Relative to V_{DD}, I_{DOI} = 500mA, V_{DD} < V_{DD_OVLO}	-63	-55	-49	V
	V_{DOI_CL}	Relative to GND, I_{DOI} = 500mA, V_{DD_OVLO} < V_{DD} < 60V	-4.5	-2.9	-1.5	V
DOI Leakage MAX14914, MAX14914A, MAX14914B	I_{DOI_LK}	V_{DD} = 40V, PP = IN = low, DI_EN = low, 0V < V_{DOI} < V_{DD}, V_L > V_{L_POR}	-60		60	µA
		VDD = 60V, PP = IN = X, DI_EN = low, 0V < V_{DOI} < V_{DD}, V_L > V_{L_POR}	-150		150	
DOI Leakage MAX14914A	I_{DOI_LK}	V_{DD} = 40V, V_L < V_{L_POR}, PP = IN = DI_EN = X, 0V < V_{DOI} < 15V	-2.4		0	µA
		V_{DD} = 40V, V_L < V_{L_POR}, PP = IN = DI_EN = X, 0V < V_{DOI} < 15V, T = -40°C to +85°C	-0.4		0	
		V_{DD} = 34V, V_L < V_{L_POR}, PP = IN = DI_EN = X, -15V < V_{DOI} < 0V		-80		
OUTPUT DRIVER CURRENT LIMITING (DOI)						
HS Current-Limit Minimum	$I_{CLIM\_HS\_MIN}$	R_{LIM} = 220kΩ	135	196	255	mA
HS Current-Limit Maximum	$I_{CLIM\_HS\_MAX}$	R_{LIM} = 27kΩ	1.3	1.6	1.9	A
HS Current-Limit Offset Error	$I_{CLIM\_HS\_OE}$	(*Note 2*)	-25		+25	mA
HS Current-Limit Gain Error	$I_{CLIM\_HS\_GE}$	(*Note 2*)	-20		+20	%
CLIM Voltage	V_{CLIM}			1.21		V
CLIM Short Resistor Threshold Value	R_{LIM_SHORT}	(*Note 3*)	10	12.9	15	kΩ
CLIM Open Resistor Threshold Value	R_{LIM_OPEN}	(*Note 4*)	440		750	kΩ
LS Current Limit	I_{CLIM_LS}		150		280	mA
DIGITAL INPUT / DOI MONITOR						
DO Monitor Threshold Voltage	V_{TH_DO}	DI_EN = low, DOI rising	1.5		2.0	V
	V_{TH_DO}	DI_EN = low, DOI falling	1.3		1.8	V
DO Monitor Hysteresis	V_{HYS_DO}	DI_EN = low		0.2		V
DI Threshold Voltage	V_{TH_DI}	DI_EN = high, DOI rising	6.7		8	V
		DI_EN = high, DOI falling	5.5		6.8	
DI Hysteresis	V_{HYS_DI}	DI_EN = high		1.2		V
DI Current Sink Type 1/ 3	I_{DOI}	DI_EN = high, PP = low, 0V < V_{DOI} < 5V			2.6	mA
		DI_EN = high, PP = low, 8V < V_{DOI} < 40V, V_{DOI} < V_{DD}	2.0	2.3	2.6	

Electrical Characteristics (continued)

(V_{DD} = +10V to +40V, V_5 = +4.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = +25ºC , V_{DD} = +24V, V_L= +3.3V and V_5 = +5V, R_{LIM} = 50kΩ.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DI Current Sink Type 2	I_{DOI}	DI_EN = high, PP = high, 0V < V_{DOI} < 5V	0		7.5	mA
		DI_EN = high, PP = high, 8V < V_{DOI} < 40V, V_{DOI} < V_{DD}	6.0	7.0	7.7	
LOGIC (I/O)						
Input Voltage High	V_{IH}		0.7xV_L			V
Input Voltage Low	V_{IL}				0.3xV_L	V
Input Threshold Hysteresis	V_{IHYST}			0.11xV_L		V
Input Pulldown Resistor	R_I	All logic input pins	140	200	275	kΩ
Output Logic Low	V_{OL}	I_{LOAD} = +5mA			0.33	V
$\overline{DOI\_LVL}$ Tristate Leakage	I_{LEAK}	GND < V_{DOI_LVL} < V_L	-1		+1	µA
$\overline{FAULT}$ Output Tristate Leakage	I_{LEAK}	GND < $V_{\overline{FAULT}}$ < V_5	-1		+1	µA
OV_VDD Leakage	I_{LEAK}	GND < V_{OV_VDD} < V_{DD}	-1		+1	µA
$\overline{OV\_CURR}$ Leakage	I_{LEAK}	GND < V_{OV_CURR} < V_{DD}	-1		+1	µA
THERMAL PROTECTION						
Driver Thermal-Shutdown Temperature	T_{JSHDN}	Junction temperature rising		170		°C
Driver Thermal-Shutdown Hysteresis	T_{JSHDN_HYST}			15		°C
Chip Thermal Shutdown	T_{CSHDN}	Temperature rising		150		°C
Chip Thermal-Shutdown Hysteresis	T_{CSHDN_HYST}			10		°C
TIMING CHARACTERISTICS / OUTPUT DRIVER (DOI)						
Output Propagation Delay LH	t_{PD_LH}	PP = low, delay from IN to DOI rising by 1V, R_L = 5kΩ, C_L = 100pF (Figure 1)		0.4	1.5	µs
Output Propagation Delay HL	t_{PD_HL}	PP = low, delay between IN switching low to DOI falling by 1V, R_L= 5kΩ, C_L = 100pF, V_{DD} = 24V (Figure 1)		0.6	1.5	µs
	t_{PD_HL}	PP = high, delay between IN switching low to DOI falling by 1V, R_L = 5kΩ, C_L = 100pF (Figure 1)		0.6	1.5	µs
DOI Output Rise Time	t_R	PP = X, 20% to 80% V_{DD}, R_L = 5kΩ, C_L = 100pF (Figure 2)		0.9	2	µs
DOI Output Fall Time	t_F	PP = low, 80% to 20% V_{DD}, V_{DD} = 24V, R_L = 5kΩ, CL = 100pF (Figure 2)		0.65	2	µs
	t_F	PP = low, 80% to 20% V_{DD}, V_{DD} = 24V, R_L = 47Ω, C_L = 100pF (Figure 2)		1		µs
TIMING CHARACTERISTICS / PROPAGATION DELAY (DOI to DOI_LVL)						
Propagation Delay LH	t_{PDL_LH}	DI_EN = low, delay from DOI rising to 5V to $\overline{DOI\_LVL}$ low (Figure 3)		2.7	5	µs

Electrical Characteristics (continued)

(V_{DD} = +10V to +40V, V_5 = +4.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = +25ºC , V_{DD} = +24V, V_L= +3.3V and V_5 = +5V, R_{LIM} = 50kΩ.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay LH DI	$t_{PDL\_HL\_DI}$	DI_EN = high, delay from DOI rising to 8V to $\overline{DOI\_LVL}$ low		1.1		µs
Propagation Delay HL	t_{PDL_HL}	DI_EN = low, delay from DOI falling to 3.5V to $\overline{DOI\_LVL}$ high		0.9	8	µs
Propagation Delay HL DI	$t_{PDL\_HL\_DI}$	DI_EN = high, delay from DOI falling to 5.5V to $\overline{DOI\_LVL}$ high		0.9		µs
TIMING CHARACTERISTICS / GLITCH REJECTION (IN)						
Pulse Length of Rejected Glitch	t_{FPL_GF}		0		80	ns
Glitch Filter Delay Time	t_{D_GF}			140	300	ns
TIMING CHARACTERISTICS / FAULT DETECTION (OV_VDD)						
OV_VDD Threshold	$V_{TH\_OV\_VDD}$	DI_EN = low, relative to V_{DD}. MAX14914 and MAX14914A		0.22		V
OVLO_VDD Debounce Time	TD_{OVLO_VDD}	DI_EN = low. MAX14914 and MAX14914A.		200		µs

Electrical Characteristics—ESD and SURGE Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD	V_{ESD}	DOI pin Contact Discharge (*Note 5*)		±7		kV
		DOI pin Air Discharge (*Note 5*)		±20		
		All other pins. Human Body Model		±2		
IEC Surge	V_{SURGE}	DOI to PGND or Earth GND per IEC 61000-4-5 (42Ω/0.5µF) (*Note 6*)		±2		kV

Note 1: All the MAX14914ATE+ and MAX14914BATE+ units are production tested at T_A = +25°C. All the MAX14914AATE+ units are production tested at T_A = +25°C and +125°C. Specifications over temperature are guaranteed by characterization and design.

Note 2: Specification is guaranteed by design; not production tested.

Note 3: Lower resistor values than CLIM_SHORT act like a CLIM pin short to GND

Note 4: Higher resistor values than CLIM_OPEN act like a CLIM open circuit.

Note 5: Bypass V_{DD} pin to PGND with 1µF capacitor as close as possible to the device for high ESD protection.

Note 6: With TVS protection on V_{DD} to PGND.

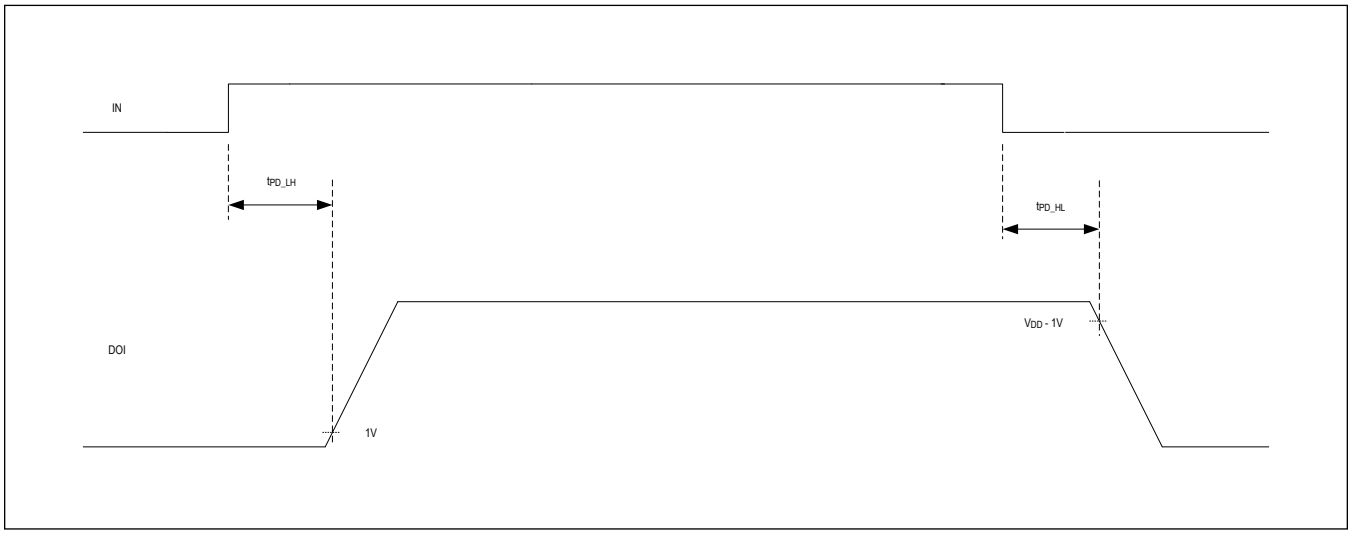


Figure 1. IN to DOI Propagation Delay

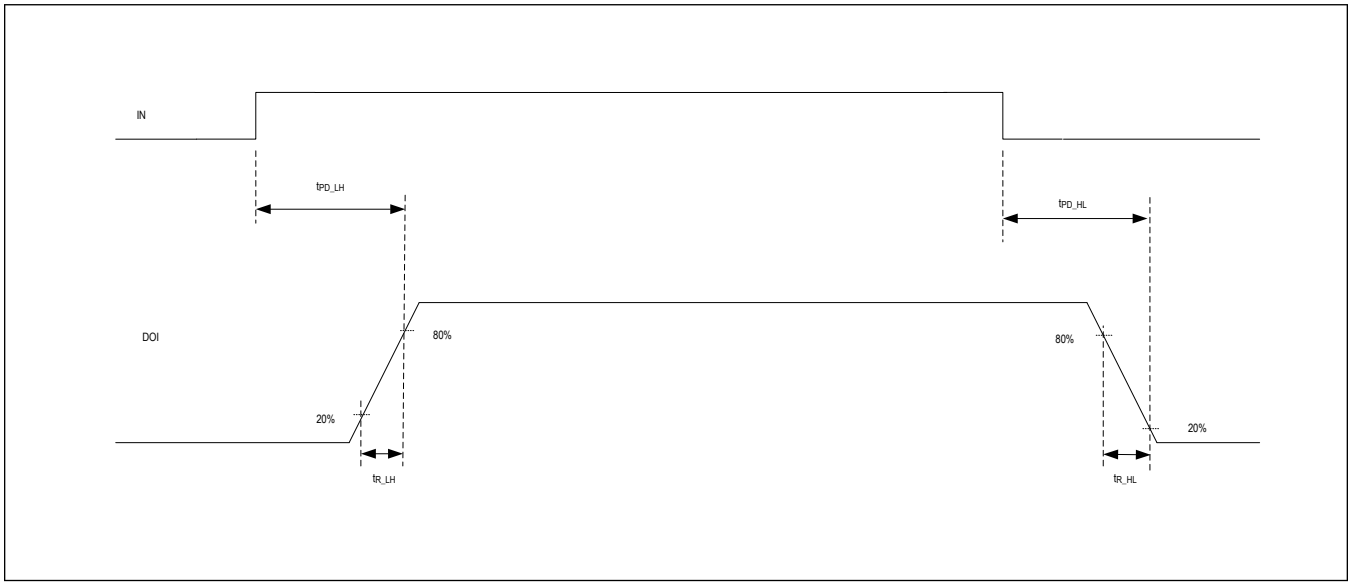


Figure 2. DOI Rise and Fall Time

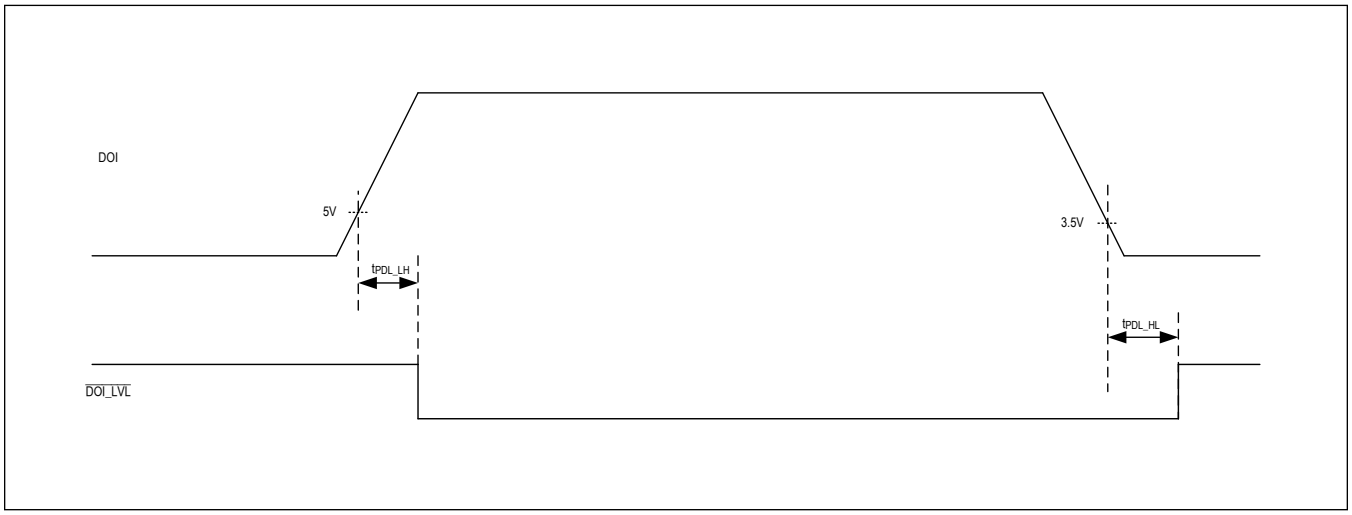
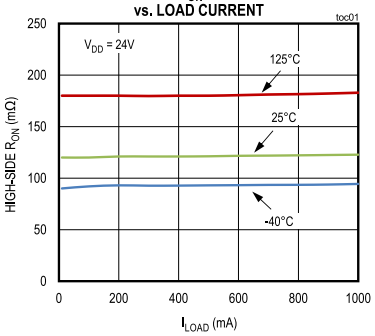


Figure 3. DOI to DOI_LVL Propagation Delay

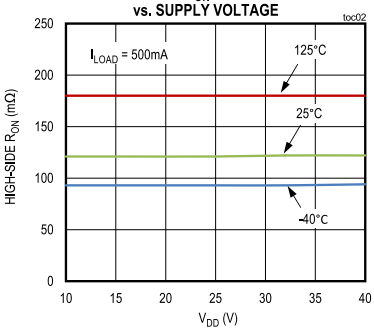
Typical Operating Characteristics

(V_{DD} = +24V, V_L = +3.3V, V_5 = +5V, T_A = +25°C, unless otherwise noted.)

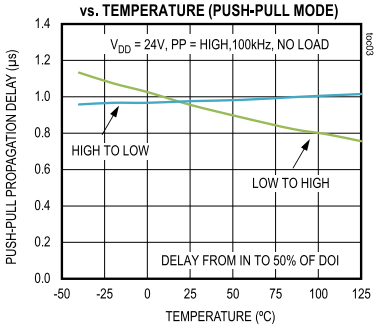
HIGH-SIDE R_{ON} RESISTANCE vs. LOAD CURRENT



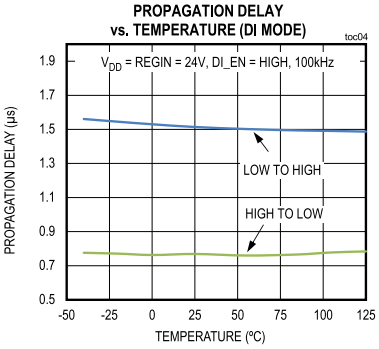
HIGH-SIDE R_{ON} RESISTANCE vs. SUPPLY VOLTAGE



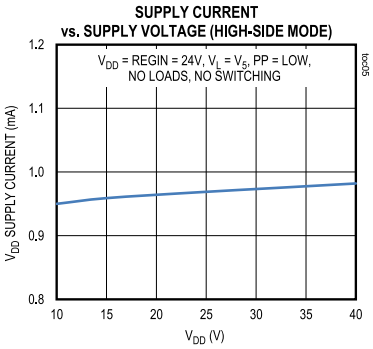
PROPAGATION DELAY vs. TEMPERATURE (PUSH-PULL MODE)



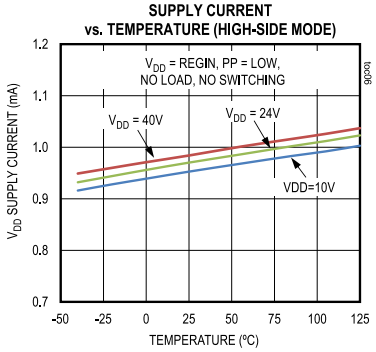
PROPAGATION DELAY vs. TEMPERATURE (DI MODE)



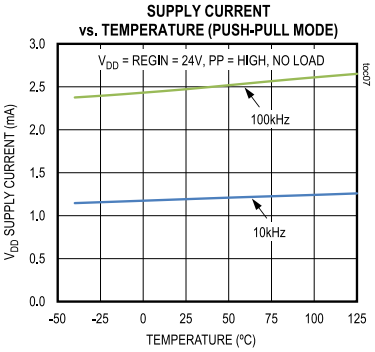
SUPPLY CURRENT vs. SUPPLY VOLTAGE (HIGH-SIDE MODE)



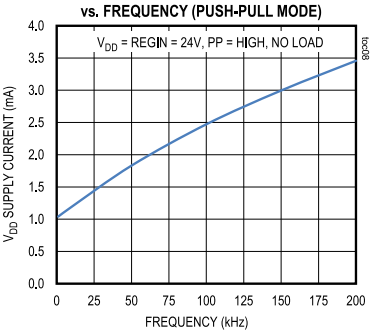
SUPPLY CURRENT vs. TEMPERATURE (HIGH-SIDE MODE)



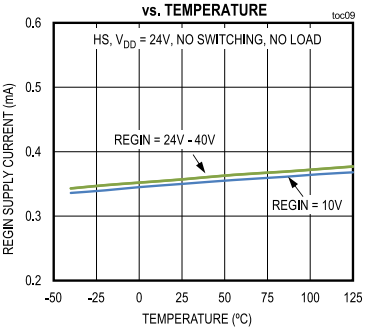
SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL MODE)



SUPPLY CURRENT vs. FREQUENCY (PUSH-PULL MODE)

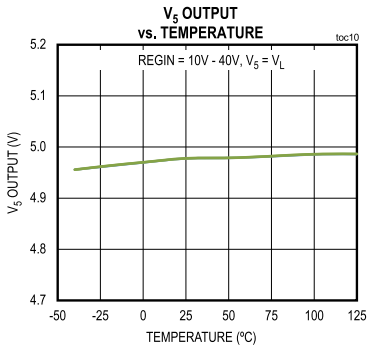


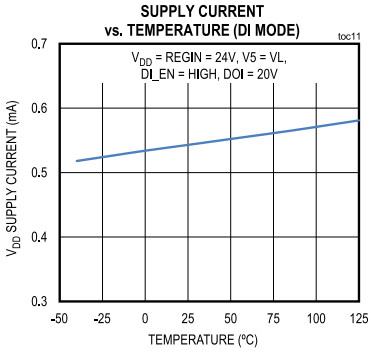
REGIN SUPPLY CURRENT vs. TEMPERATURE

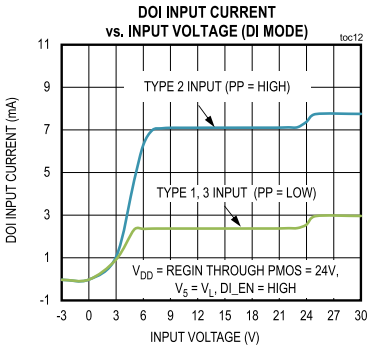


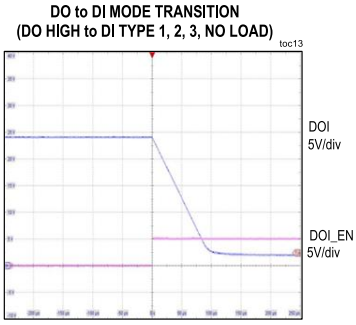
Typical Operating Characteristics (continued)

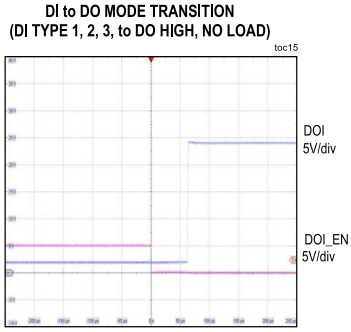
(V_{DD} = +24V, V_L = +3.3V, V_5 = +5V, T_A = +25°C, unless otherwise noted.)

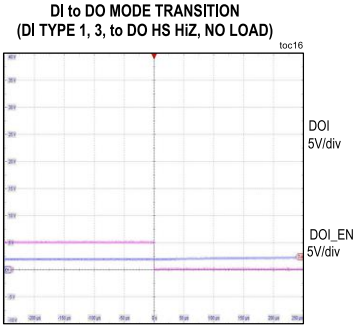


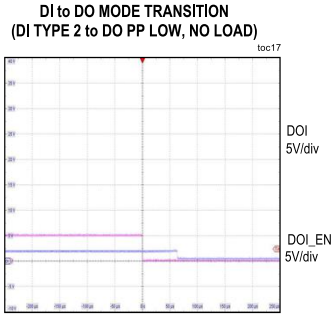


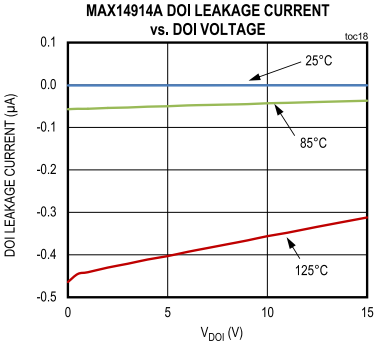






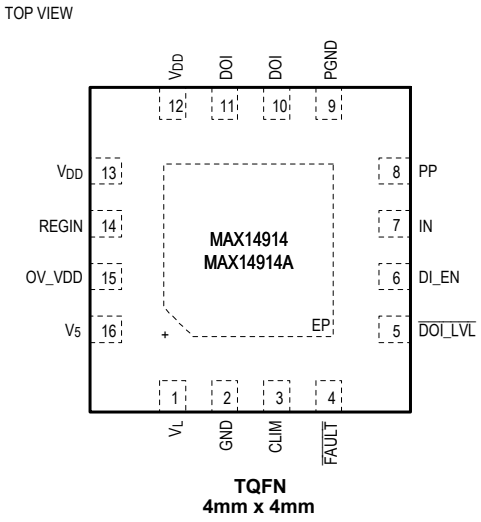






Pin Configurations

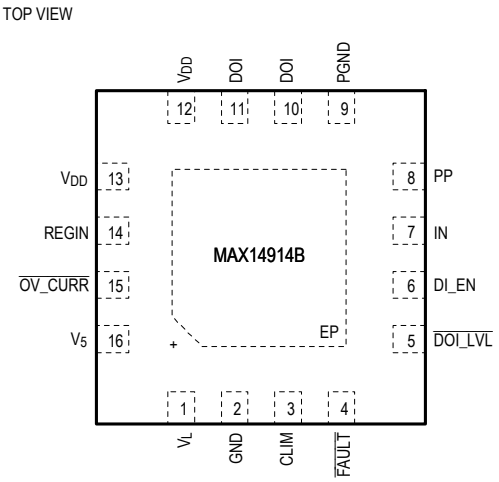
MAX14914 and MAX14914A



TQFN
4mm x 4mm

*EP = EXPOSED PAD. CONNECT EP TO GND

MAX14914B



TQFN
4mm x 4mm

*EP = EXPOSED PAD. CONNECT EP TO GND

Pin Description

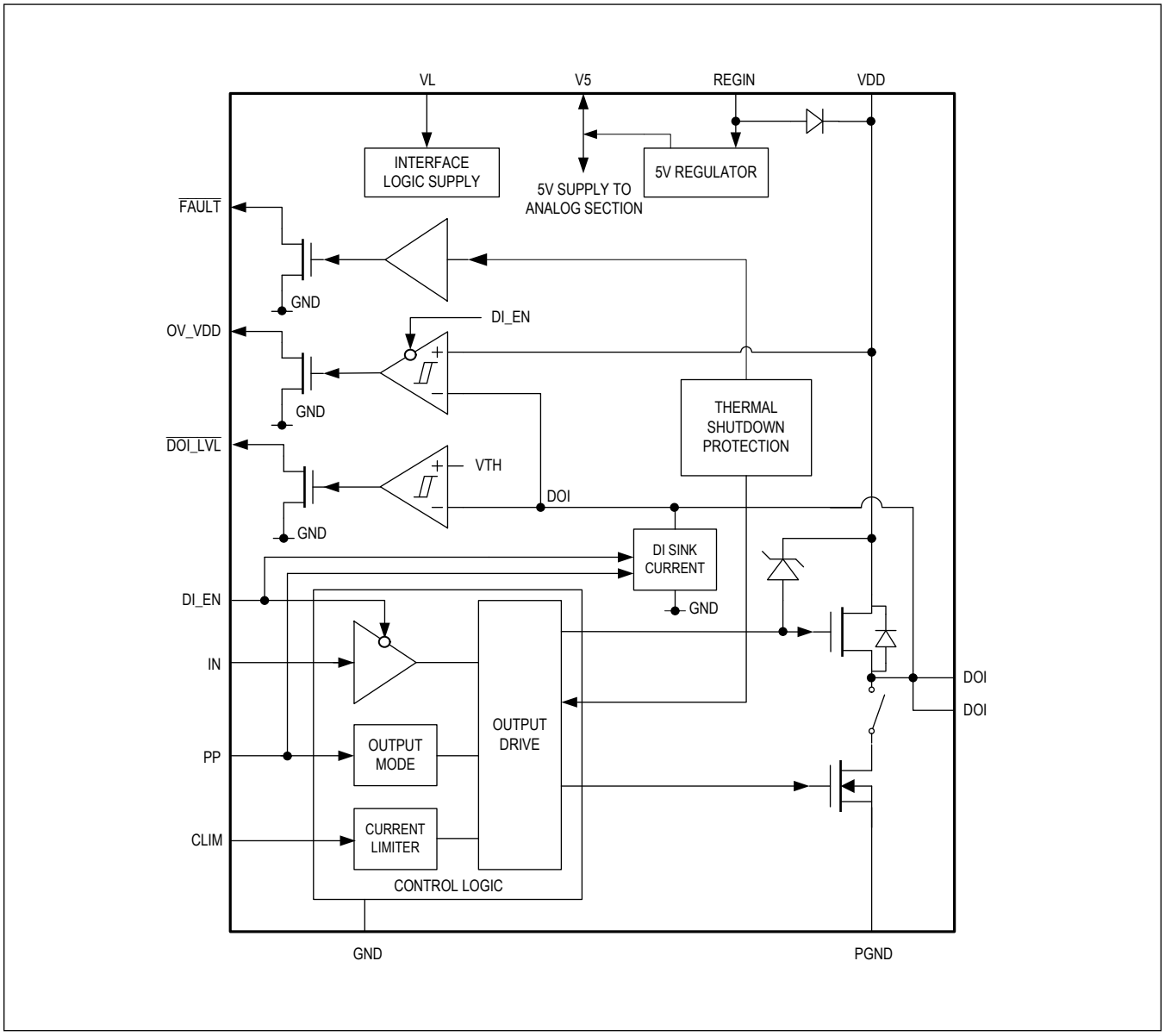
PIN		NAME	FUNCTION	TYPE
MAX14914 and MAX14914A	MAX14914B			
1	1	V_L	Logic Supply Input. V_L defines the levels on all I/O logic interface pins. Bypass V_L to GND through a 100nF ceramic capacitor.	Supply
2	2	GND	Analog Ground	Supply
3	3	CLIM	Current Limit Set Input. Connect a resistor from CLIM to GND to set the current limit. See Detailed Description for further information.	Analog Input
4	4	$\overline{FAULT}$	Open-Drain Fault Output. The $\overline{FAULT}$ transistor turns on when a fault condition (driver thermal shutdown or loss of ground) occurs. Connect a pullup to V_L or V_5.	Logic Output
5	5	$\overline{DOI\_LVL}$	Open-Drain DOI Level Output. $\overline{DOI\_LVL}$ is logic-low when DOI voltage is higher than the threshold voltage. $\overline{DOI\_LVL}$ is logic-high (using a pullup resistor) when DOI voltage is lower than the threshold voltage. The threshold voltage depends on DI_EN. Connect a pullup to V_L or V_5.	Logic Output
6	6	DI_EN	Digital Input Mode Logic Enable Input. Set DI_EN high to enable digital input operation on the DOI pin, which enables the internal current sink and sets Type 1, Type 2, or Type 3 thresholds on $\overline{DOI\_LVL}$. Select between Type 1 and 3, and Type 2 DI characteristics through the PP input.	Analog
7	7	IN	Switch Control Input. Drive IN high to close the HS switch; drive IN low to open the HS switch and close the LS switch (when PP = low).	Logic Input
8	8	PP	Push-Pull DO or DI Type Select Input. In DO mode, set PP high to enable push-pull mode operation of the DO driver. In DI mode, set PP low for IEC Type 1/3 input characteristics and set high for Type 2 input characteristics.	Logic Input
9	9	PGND	Power Ground	Supply
10, 11	10, 11	DOI	High-Side / Push-Pull Output (DI_EN = low) or Digital Input (DI_EN = high). Connect both DOI pins together externally.	Power
12, 13	12, 13	V_{DD}	Supply Voltage, Nominally 24V. Bypass V_{DD} to GND through a 1uF capacitor.	Supply
14	14	REGIN	5V Regulator Input. Connect REGIN to V_{DD} when using the internal 5V regulator. Connect REGIN to V_5 when powering V_5 from an external regulator.	Supply
15	—	OV_VDD	Open-Drain Overvoltage Output for the MAX14914 and MAX14914A. The OV_VDD transistor turns off when: 1) a device configured for DI operation; 2) DOI level is higher than V_{DD}. Connect a pullup to V_{DD}.	
—	15	$\overline{OV\_CURR}$	Open-Drain Overcurrent Output for the MAX14914B. $\overline{OV\_CURR}$ turns active low when the load current exceeds the high-side current limit. Connect a pullup resistor between $\overline{OV\_CURR}$ and V_L.	

Pin Description (continued)

PIN		NAME	FUNCTION	TYPE
MAX14914 and MAX14914A	MAX14914B			
16	16	V_5	Analog Supply Voltage/LDO Output. The MAX14914 requires a 5V supply for normal operation, which can come from the internal linear regulator (REGIN connected to V_{DD}) or from an external regulator (REGIN connected to V_5). Bypass to GND through a 1µF ceramic capacitor.	Supply
—	—	EP	Exposed Pad. Connect EP to GND.	

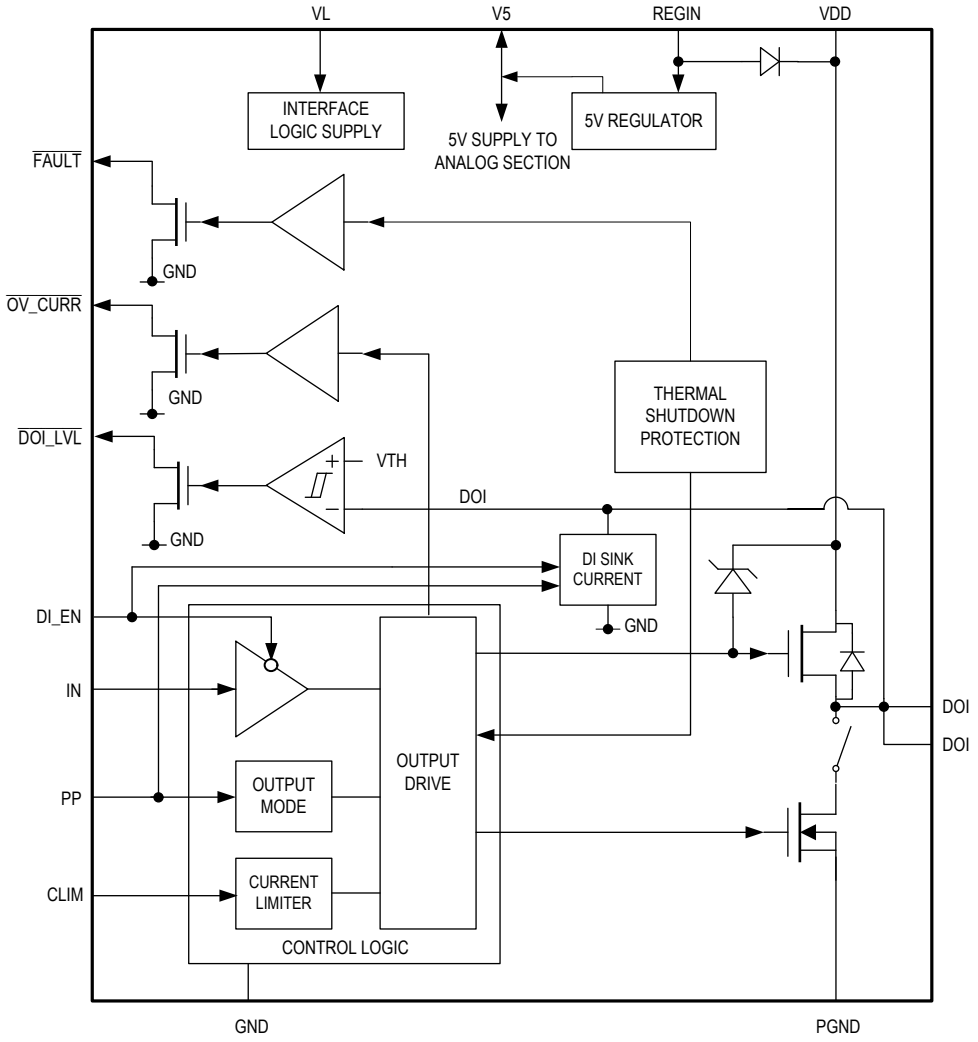
Functional Diagrams

MAX14914 and MAX14914A



Functional Diagrams (continued)

MAX14914B



Detailed Description

The MAX14914 family of parts is a high-side/push-pull driver that operates as an industrial digital output and can also operate as an industrial digital input. The MAX14914 family is specified for operation with supplies up to 40V. The high-side switch current limiting is resistor settable from 135mA (min) to 1.3A (min). The high-side driver on-resistance is 120mΩ (typ) and 240mΩ (max) at +125°C ambient temperature. Optional push-pull operation allows driving of cables and fast discharge of load capacitance. A separate digital $\overline{DOI\_LVL}$ allows supervision of the DOI voltage in DO mode for safety applications. The MAX14914 family complies with IEC Type 1, Type 2, or Type 3 input characteristics when configured for digital input operation.

The difference between the MAX14914, MAX14914A and MAX14914B versions is summarized in Table 1, and the summary of the control signals is shown in Table 2.

Table 1. Features Selection

	DOI OVERVOLTAGE (OV_VDD)	DOI OVERCURRENT ($\overline{OV\_CURR}$)	LOW DOI LEAKAGE ($V_L < V_{L\_POR}$)
MAX14914	YES	NO	NO
MAX14914A	YES	NO	YES
MAX14914B	NO	YES	NO

Table 2. Operation Truth Table

MODE	DI_EN	IN	PP	DOI	$\overline{DOI\_LVL}$
DO High-Side	low	low	low	three-state	high/low
DO High-Side	low	high	low	high	low
DO Push-Pull	low	low	high	low	high
DO Push-Pull	low	high	high	high	low
DI Type 1/3	high	x	low	high	low
DI Type 1/3	high	x	low	low	high
DI Type 2	high	x	high	high	low
DI Type 2	high	x	high	low	high

5V Supply and Regulator

The MAX14914 family requires a 5V supply on the V_5 pin for normal operation. This 5V supply can come from an external supply or from the internal 5V linear regulator. Connect REGIN pin to V_{DD} to enable the internal regulator. Connect REGIN pin to V_5 pin to disable the internal regulator, when an external 5V is used. The internal 5V regulator also can power the external loads/circuits with of up to 20mA.

Logic Interface

The logic interface features flexible logic levels, allowing interfacing to a wide range of common logic. The V_L supply input defines the logic levels and can be set in the range of 2.5V to 5.5V. Connect a 0.1µF capacitor to V_L.

Digital Output Operation

The driver can be configured for high-side (PP pin is driven low) or push-pull (PP pin is driven high) operation. In DO high-side mode, the DOI output voltage is high (V_{DD}) when the logic level on IN pin is high, and three-state (Hi-Z), when the logic level on IN pin is low. In DO Push-Pull mode, the DOI output voltage follows the logic level on IN pin. The high-side driver has 240mΩ (max) on-resistance at 500mA and T_A = 125°C. The DOI voltage can go below ground, as will occur during inductive load demagnetization. An internal clamping diode limits the negative excursion to (V_{DD} - V_{CL}). See *Driving Inductive Loads* for details. The low-side (LS) switch speeds up the discharge of RC loads in Push-Pull mode.

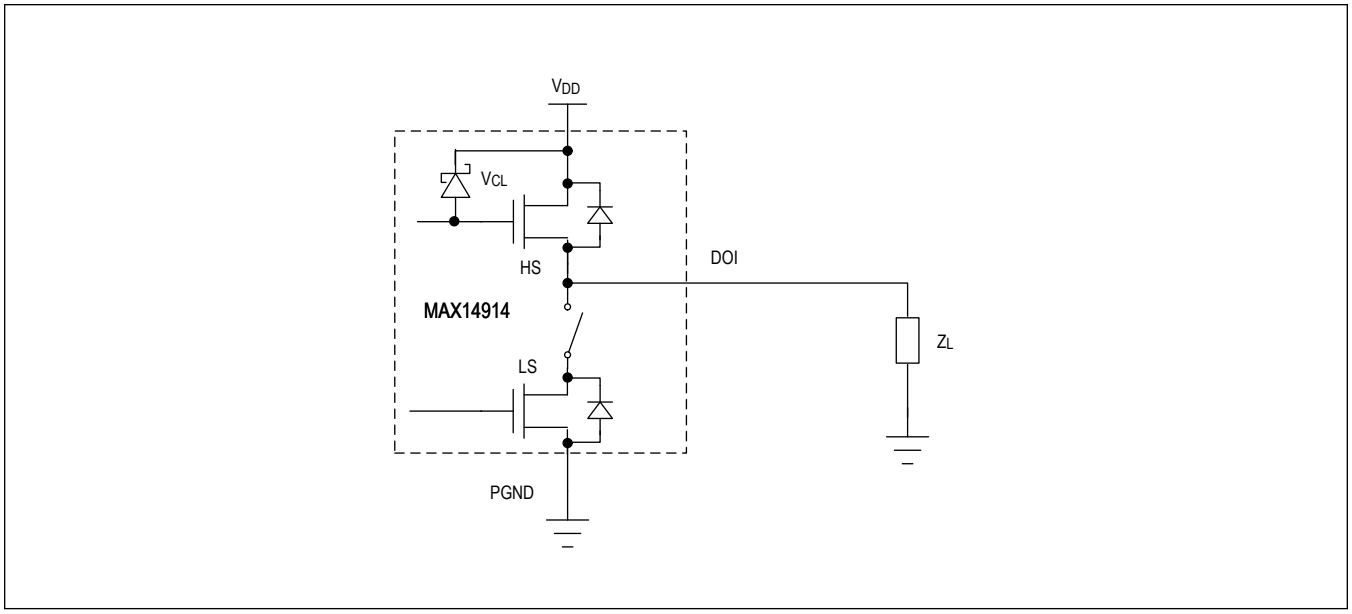


Figure 4. Digital Output Driver

Low DOI Leakage Mode

The MAX14914A features a low-leakage mode in which the DOI leakage current is less than 0.4µA with temperature up to +85°C and DOI between 0V and +15V. This is useful when the DOI pin is connected to an analog input/output (I/O) line and does not affect the performance of the analog I/O device. Low-leakage mode is enabled when the V_L voltage is held low below V_{L_POR} (min) = 1.12V. Note that the logic inputs, like IN, DI_EN and PP, can be held high or low in low-leakage mode.

Current Limit Adjustment

The MAX14914 family has a settable current limiting of the HS switch. The load current is limited to between 135mA (min) and 1.3A (min), depending on the value of the resistor used at the CLIM pin. A short-circuit or overcurrent generally creates a temperature rise in the chip; both the HS and LS FET's temperatures are continuously monitored. When any switch temperatures exceed 170°C, the DOI output is put in Hi-Z until the temperature falls by 15°C. Connect a resistor (RLIM) from CLIM to GND to set the required current limit. The current is given by:

$$I_{LIM} = K \times V_{LIM} / R_{LIM}$$

where, V_{LIM} = 1.21V and K = 35.6 x 10^3. If no resistor is connected to CLIM (i.e., CLIM is kept floating) or RLIM is more than 440k, the ILIM is internally set to 1.1A (typ). If the RLIM resistor is less than 12.9k (typ), the output is turned off. CLIM is short-circuit protected.

Use the formulas below to validate the accuracy range

$I_{LIM\_MAX} = I_{LIM} \times (1 + |I_{CLIM\_HS\_GE}|/100) + |I_{CLIM\_HS\_OE}|$

$I_{LIM\_MIN} = I_{LIM} \times (1 - |I_{CLIM\_HS\_GE}|/100) - |I_{CLIM\_HS\_OE}|$

Low-Side Current Limit

The low-side transistor has fixed-current limiting, when enabled in push-pull mode (PP driven high). The low-side driver limits current at 200mA (typ). The load current is actively controlled and the low-side switch only turns off if the driver temperature has fallen by the hysteresis value.

Overcurrent Signaling

The MAX14914B features an overcurrent output ($\overline{OV\_CURR}$), which provides a diagnostic signal as soon as the load current exceeds the high-side driver set current limit in both high-side and push-pull DO modes (DI_EN = low and PP = x). When the high-side FET detects an overcurrent for a duration longer than 8µs, the $\overline{OV\_CURR}$ open-drain signal becomes active low and remains low until the overcurrent condition disappears. The overcurrent condition also disappears every time the high-side switch turns off when a short-circuit condition exists and the FET turns off for thermal shutdown protection. Note that $\overline{OV\_CURR}$ does not signal an overcurrent on the low-side driver in push-pull mode. The typical application circuit with the overcurrent signaling is shown in Figure 5.

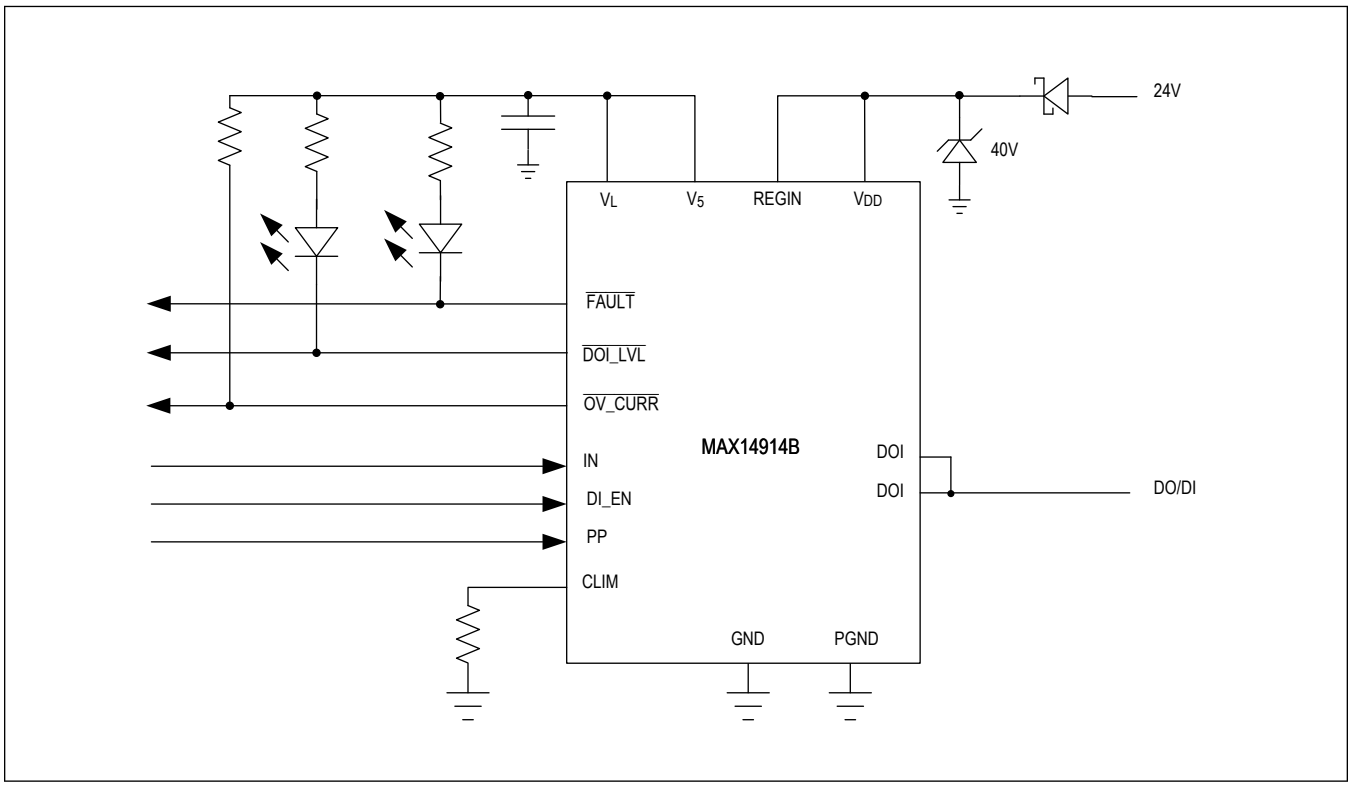


Figure 5. MAX14914B Application Diagram

Short-Circuit Protection

Short circuits at the DOI output generates high transient current until the active current limiting kicks in. In order to protect the MAX14914_ against high currents that can be seen over an extended time, especially if the output is switching at a high rate into a short circuit, the MAX14914_ enters a protect mode. When the MAX14914_ detects that the DOI current is over 3x higher than the set current limit, the driver is switched to protect mode with reduced turn-on slew rate of the rising and falling edges for a duration of 4ms. The $\overline{FAULT}$ signal does not become active and the chip operates normally, but with reduced slew rate. If the cause for the short circuit is not removed, the protect mode will remain for an additional 4ms until the short circuit is removed.

Overvoltage Lockout

When the V_{DD} supply voltage exceeds the OVLO threshold voltage of 42.2V (typ), for a time duration larger than 200µs, the high-side and low-side switches automatically turn off. They remain off until V_{DD} is reduced to below the threshold OVLO voltage minus hysteresis. When V_{DD} is above the OVLO threshold, the OV_VDD output is active.

Undervoltage Lockout

When the V_{DD}, V_5, or V_L supply voltages are under their respective UVLO thresholds the DOI driver is turned off (three-stated). DOI automatically turns back on, once V_{DD}, V_5, and V_L rise above their UVLO threshold.

Note that when $V_L \leq 1.12V$, the MAX14914ATE+ and MAX14914BATE+ force the OV_VDD pin low while the MAX14914AATE+ keeps this pin in a Hi-Z state.

Driving Capacitive Loads

When charging/discharging purely capacitive loads with a push-pull driver, the driver dissipates power that is proportional to the switching frequency. The power can be estimated by $PD \sim C \times V_{DD}^2 \times f$, where C is the load capacitance, V_{DD} is the supply voltage, and f is the switching frequency. For example, in an application with a 10nF load and 10kHz switching frequency, the driver dissipates 130mW at V_{DD} = 36V. Therefore, switching a higher capacitance can induce thermal shutdown and that limits the operational frequency.

Driving Inductive Loads

The DOI pins can be pulled below ground potential when the high-side transistor is off. The MAX14914_ has an internal clamping diode from V_{DD} to DOI that limits the negative voltage excursion to (V_{DD} - 55V) typ. Turning off the current flowing in ground-connected inductive loads results in a negative voltage at the DOI pin limited to V_{CL} below V_{DD} by the internal clamping diodes.

The MAX14914_ features SafeDemag, meaning that there are no limits for load inductance that it can demagnetize, for load currents of up to 600mA. Turn-off of large inductive loads with currents larger than 600mA requires an external clamping diode, as shown in Figure 6. The clamping (breakdown) voltage of such diode needs to be less than V_{CL}: $V_Z < V_{CL}$. Ensure that the Zener diode is able to dissipate the energy.

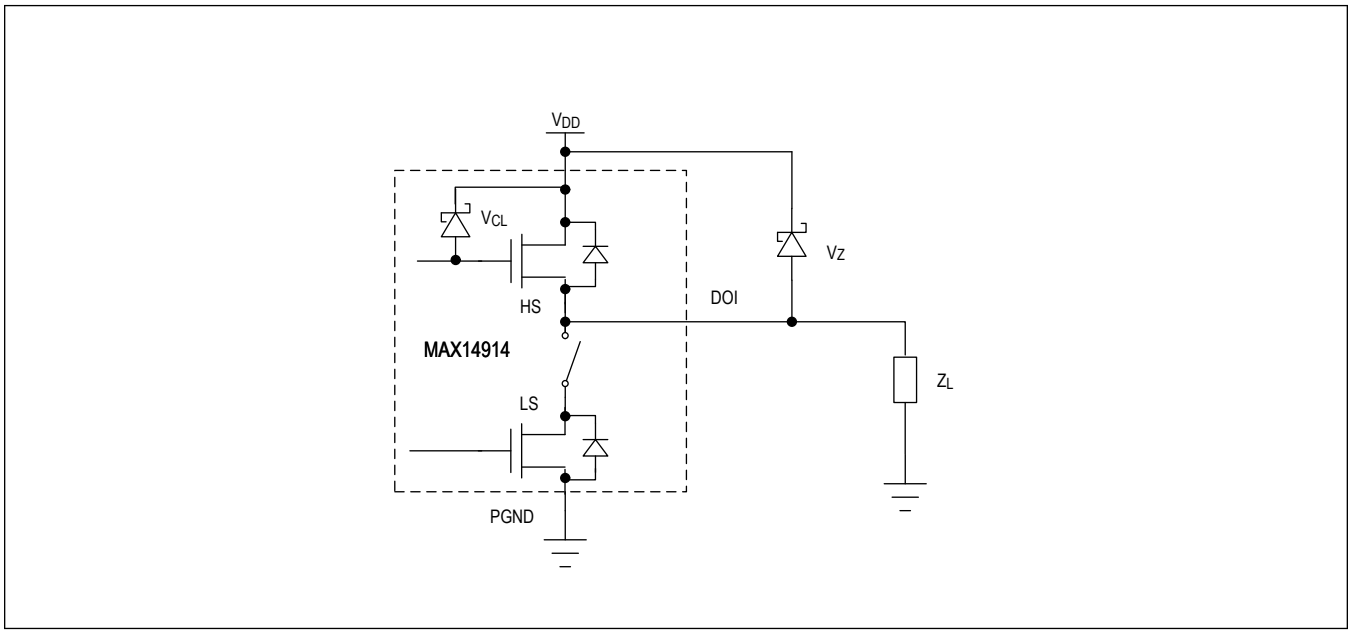


Figure 6. External Inductive Load Clamping

Monitoring of the DOI Output

The driver output (DOI) is monitored in both high-side and push-pull modes and corresponding logic level can be seen through the inversed DOI_LVL logic output. The threshold voltage for the DOI_LVL comparator is between 1.5V and 2.0V. This feature is useful for functional safety applications.

Digital Input Operation

The MAX14914_ can operate as an industrial digital input. Drive the DI_EN pin high to enable digital input operation. The 2.3mA/7mA internal current sink on DIO is then enabled and the DOI_LVL logic output presents the inverse of the DOI logic, with threshold voltages compliant with IEC61131-2 Type 1, Type 2, or Type 3 levels. IN DI mode, the PP input allows selection between IEC Type 1/3 and Type 2 input characteristics. Set PP low for Type 1/3 compatibility and set PP high for Type 2 compatibility. In order to allow the DOI input voltage to go above the V_{DD} supply voltage and preventing race condition, an external Schottky diode can be placed in series with the V_{DD} supply, as shown in Figure 7. Alternatively, an external pMOS transistor can be placed in series with the 24V supply, as shown in Figure 8, to allow the DOI voltage to exceed V_{DD}. The gate of the pMOS can be driven by the open drain OV_VDD output (MAX14914 and MAX14914A only). When DI_EN = high, the OV_V_{DD} pin turns the pMOS off permanently. Therefore, V_{DD} is one forward diode voltage (of the pMOS) below the external 24V field supply, when the DOI voltage is less than the field supply voltage. The MAX14914_ is parasitically powered by the external DOI input, when the DOI voltage is higher than the V_{DD} supply. Note that the power dissipation increases strongly when Type 2 DI mode is selected (PP = high), particularly with high DOI input voltages due to the 7mA (typ) current sink. When the V_{DOI} voltage exceeds 42.5V (typ) the sink current is automatically decreased from 7mA (typ) to 2.3mA (typ) to reduce the power dissipation.

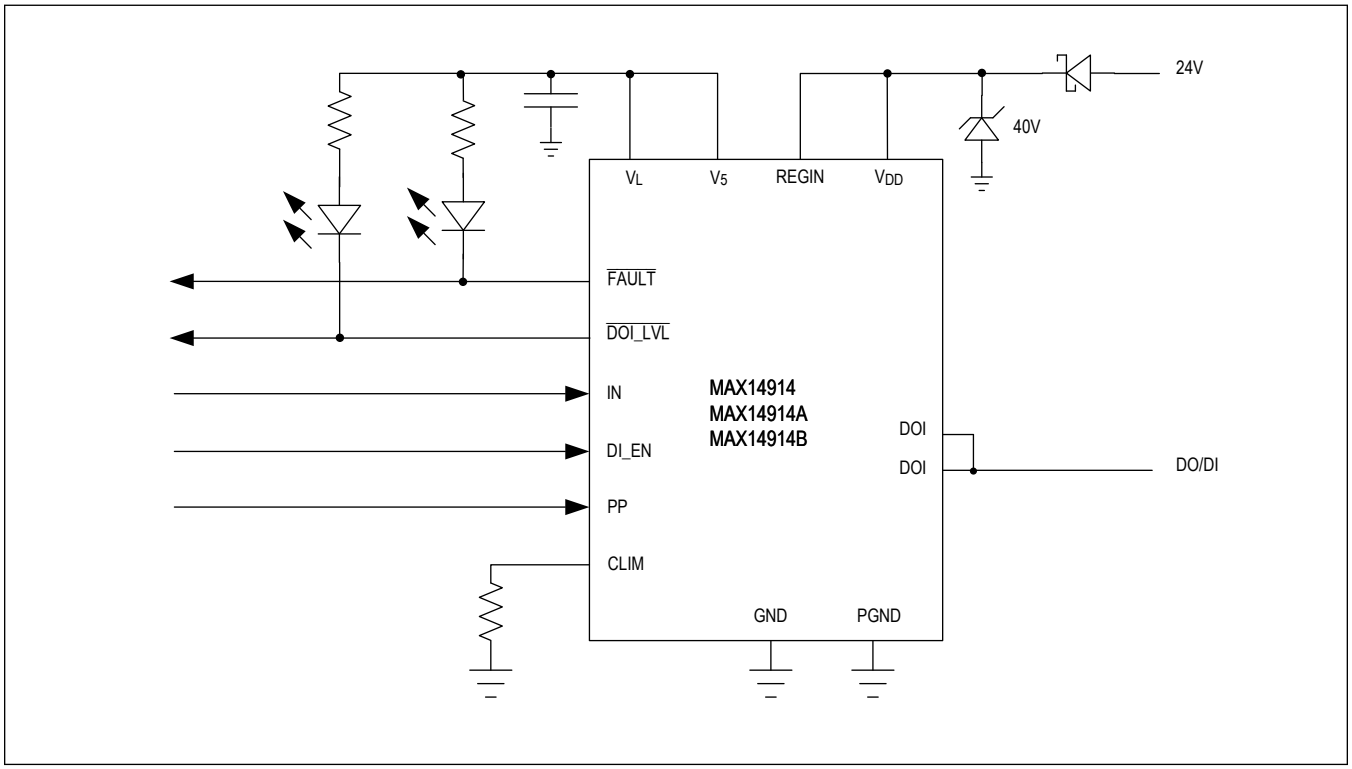


Figure 7. DO/DI Configuration with External Schottky Diode

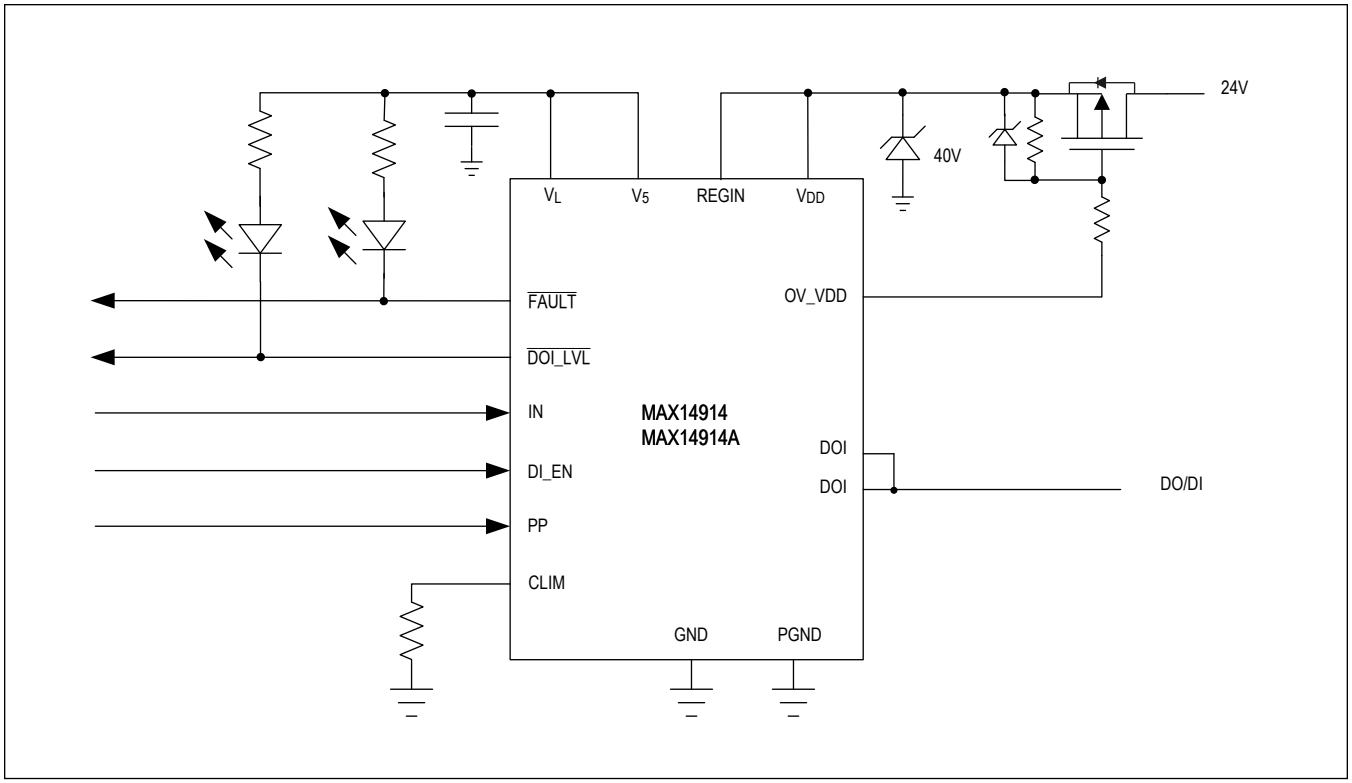


Figure 8. DO/DI Configuration with External pMOSFET

Applications Information

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

● Keep the input/output traces as short as possible. Avoid using vias to make low-inductance paths for the signals.

● Have a solid ground plane underneath the high-speed signal layer.

A suppressor/TVS diode should be used between V_{DD} and PGND to clamp positive-surge transients on the V_{DD} supply input and surges from DOI. The standoff voltage should be higher than the maximum operating voltage of the device while the breakdown voltage should be below 65V. As long field-supply cables can generate large voltage transients on the V_{DD} supply due to large dI/dt, it is recommended to add a large 10µF capacitor on V_{DD} at the point of field supply entry.

Surge Protection

DOI is protected against ±2kV/42Ω surge pulses as per IEC61000-4-5. Thus, no external surge suppression is needed on DOI. A suppressor/TVS diode (SMBJ40A, for example) should be used between V_{DD} and PGND to clamp high-surge transients on the V_{DD} supply input and surges from DOI. The breakdown voltage of TVS should be higher than the maximum operating voltage of the equipment, while the maximum clamping voltage should be below 65V.

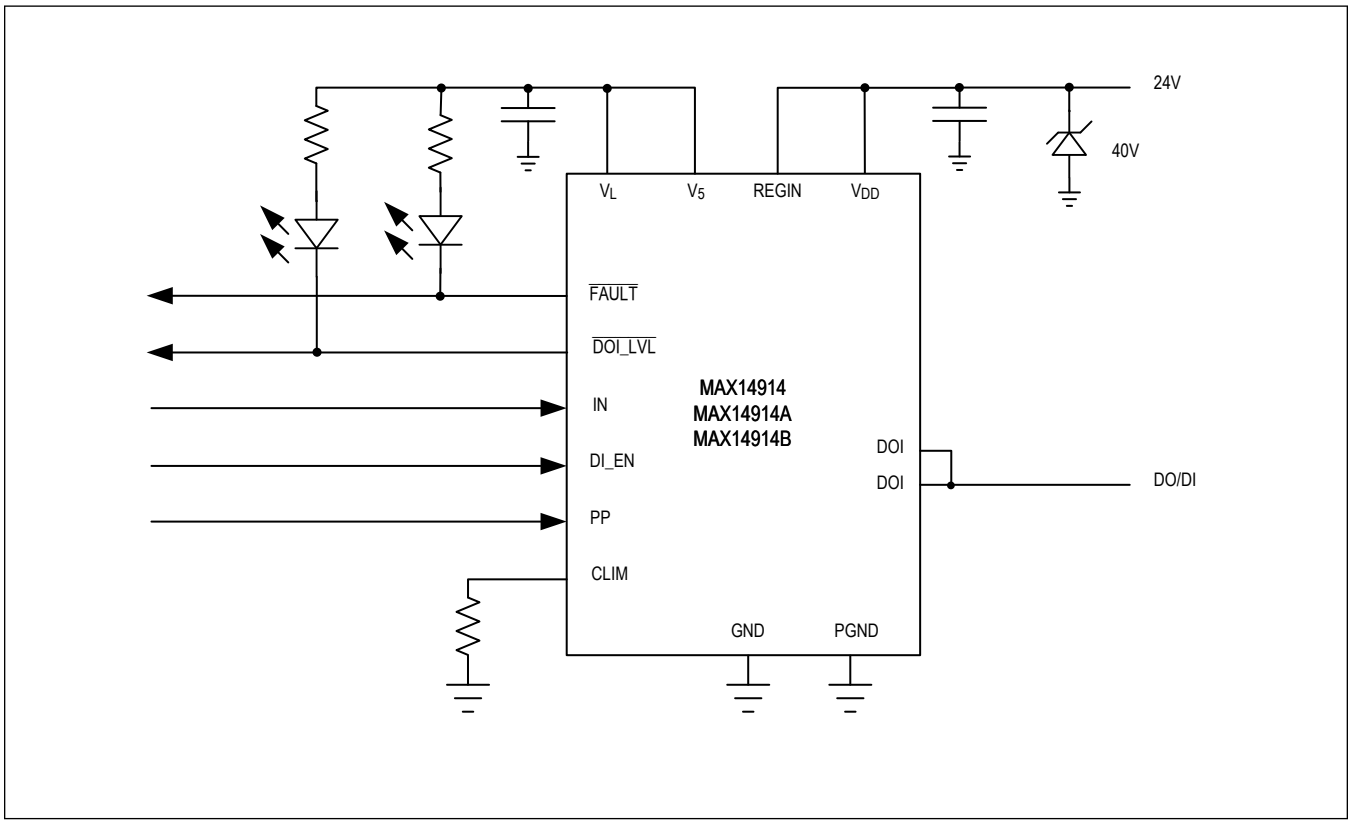
Conducted RF Immunity

To insure that the DOI driver, configured for HS mode with the switch turned off, is not turned on during IEC61000-4-6 RF immunity testing, a 10nF capacitor should be applied between the DOI output and PGND. For PP mode a capacitor on DOI is not needed.

Reverse Current into DOI

Reverse current flow into DOI pin in DO mode will heat up the device and can destroy it thermally. The allowed reverse current depends on V_{DD}, the ambient temperature and the thermal resistance. At 25°C ambient temperature the continuous reverse current into DOI pin should be limited to 250mA at V_{DD} = 40V and 400mA at V_{DD} = 24V. Using a pMOS transistor or a Schottky diode (as shown in Figure 7 and Figure 8) removes the reverse current flow path into the 24V field supply.

Typical Application Circuits



Ordering Information

PART	PACKAGE	BODY SIZE	PIN PITCH	TEMP RANGE (°C)
MAX14914ATE+	TQFN16	4mm x 4mm	0.65mm	-40 to +125
MAX14914ATE+T	TQFN16	4mm x 4mm	0.65mm	-40 to +125
MAX14914AATE+	TQFN16	4mm x 4mm	0.65mm	-40 to +125
MAX14914AATE+T	TQFN16	4mm x 4mm	0.65mm	-40 to +125
MAX14914BATE+	TQFN16	4mm x 4mm	0.65mm	-40 to +125
MAX14914BATE+T	TQFN16	4mm x 4mm	0.65mm	-40 to +125

+Denotes a lead (Pb)-free/RoHS-compliant package

T = Tape and Reel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—
1	07/17	Corrected pin number in *Pin Description* section and updated various typos	1, 10, 13
2	12/17	Updated the *Electrical Characteristics* global specifications	2-5
3	6/18	Updated the *Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Description,* and *Function Diagram* sections, and Figures 4 and 5	5, 9, 10, 12–14
4	9/20	Added MAX14914A and MAX14914B; updated the *General Description, Benefits and Features, Block Diagram, Electrical Characteristics, Pin Configuration, Pin Description, Functional Diagrams, Overvoltage Lockout, Undervoltage Lockout, Driving Inductive Loads,* and *Ordering Information* sections; updated Figures 1–2 and before renumbering, Figures 6–7; added TOC18, the *Low DOI Leakage Mode* and *Overcurrent Signaling* sections, and a new Figure 5 and renumbered subsequent figures	1–25

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX14914AATE+ MAX14914BATE+