MAX49140

30ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparator

General Description

The MAX49140 is a single high-speed comparator optimized for systems powered from a 3V or 5V supply. The MAX49140 combines high speed, low power, and rail-to-rail inputs. Propagation delay is 30ns, while supply current is only 100µA (typ).

The input common-mode range of the device extends up to both power-supply rails. The output pulls to within 0.3V of either supply rail without external pullup circuitry, making the device ideal for interfacing with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The MAX49140 is offered in tiny, 5-pin SC70 package and is fully specified over -40°C to +125°C automotive temperature range. The device is AEC-Q100 qualified.

Applications

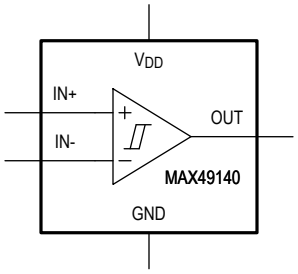
- Car Battery-Powered Systems
- Line Receivers
- Threshold Detectors/Discriminators
- 3V/5V Systems
- Zero-Crossing Detectors
- Sampling Circuits

Benefits and Features

- Fast, 30ns Propagation Delay (10mV Overdrive)
- Low-Power 100µA Supply Current (V_{DD} = 3V)
- Optimized for 3V and 5V Applications
- Rail-to-Rail Input Voltage Range
- Low, 500µV Offset Voltage
- Internal Hysteresis for Clean Switching
- Output Swing 300mV of Power Rails
- CMOS/TTL-Compatible Outputs
- Small SC70 Package
- AEC-Q100 Qualified

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



19-100740; Rev 0; 7/20

maxim integrated™

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LIST OF FIGURES

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +6V
IN+, IN- to GND ..... -0.3V to V_{DD} + 0.3V
OUT to GND ..... -0.3V to V_{DD} + 0.3V
Current into Input Pins ..... ±20mA
Input/Output Short-Circuit Duration to V_{DD} or GND ... Continuous
Continuous Power Dissipation (T_A = +70°C), 5 Pin SC70 (derate 3.1mW/°C above +70°C), Multilayer Board 246.9mW

Operating Temperature Range ..... -40°C to +125°C
Junction Temperature (T_{JMAX}) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

5 SC70

Package Code	X5+1C
Outline Number	21-0076
Land Pattern Number	90-0188
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	324°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	115°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	324°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	115°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 5V, V_{CM} = 0.1V, C_L = 15pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Voltage	V_{DD}	Guaranteed by PSRR specification		2.7		5.5	V
V_{DD} Supply Current	I_{DD}	V_{CM} = 5V, V_{DD} = 5V	T_A = -40°C to +85°C		100	180	µA
			T_A = -40°C to +125°C			200	
Common-Mode Input Voltage	V_{CM}	*Note 2*		0		V_{DD}	V
Input Offset Voltage	V_{OS}	*Note 3*			0.5	5	mV
Input Hysteresis	V_{HYS}	*Note 4*			1.2		mV

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{CM} = 0.1V, C_L = 15pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Current	I_B	*Note 5*	T_A = +25°C		200	500	nA
			T_A = -40°C to +125°C			900	
Input Offset Current	I_{OS}	T_A = +25°C			20	50	nA
		T_A = -40°C to +125°C				100	
Common-Mode Rejection Ratio	CMRR	*Note 6*			50	500	µV/V
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{DD} ≤ 5.5V			100	450	µV/V
Output-High Voltage	V_{OH}	I_{SOURCE} = 4mA		V_{DD} - 0.3			V
Output-Low Voltage	V_{OL}	I_{SINK} = 4mA				0.3	V
Propagation Delay	t_{PD+}, t_{PD-}	V_{DD} = 3V, V_{OD} = 10mV, V_{CM} = 0.1V			30		ns
Propagation Delay Skew		V_{OD} = 10mV (*Note 7*)			1		ns

Note 1: All specifications are 100% production tested at T_A = +25°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by design, not production tested.

Note 2: Inferred from CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

Note 3: V_{OS} is defined as the center of the input-referred hysteresis zone. See Figure 1.

Note 4: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. See Figure 1.

Note 5: The polarity of I_B reverses direction as V_{CM} approaches either supply rail.

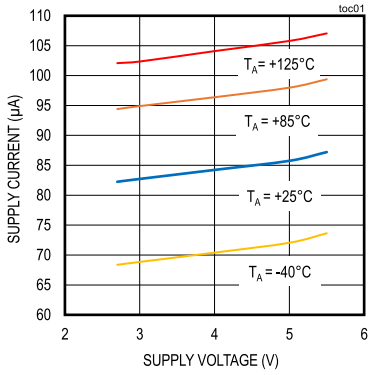
Note 6: Specified over the full common-mode voltage range (V_{CM}).

Note 7: Specified as the difference between t_{PD+} and t_{PD-}.

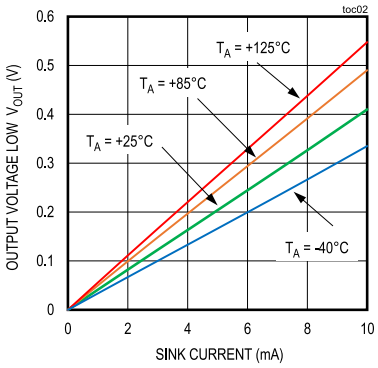
Typical Operating Characteristics

(V_{DD} = 3.0V, V_{CM} = 0.1V, C_L = 15pF, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

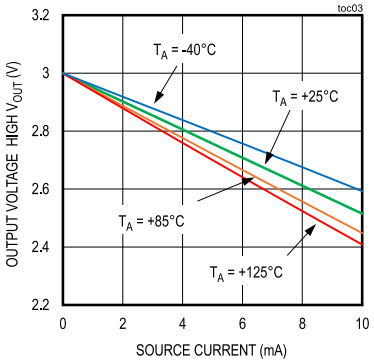
SUPPLY CURRENT vs. SUPPLY VOLTAGE



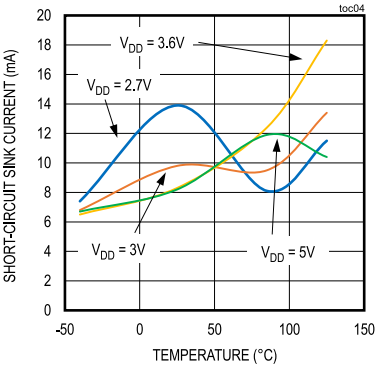
OUTPUT VOLTAGE LOW vs. SINK CURRENT



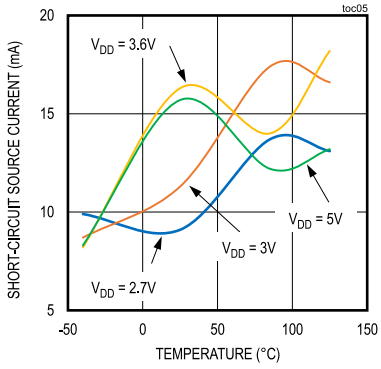
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT



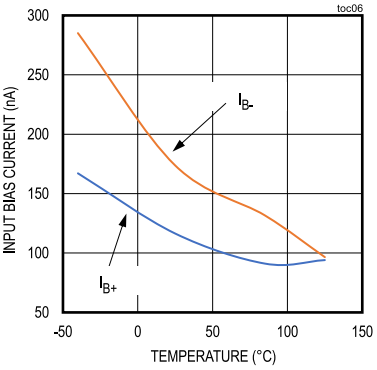
SHORT-CIRCUIT SINK CURRENT vs. TEMPERATURE



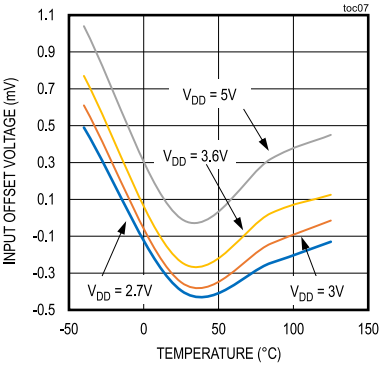
SHORT-CIRCUIT SOURCE CURRENT vs. TEMPERATURE



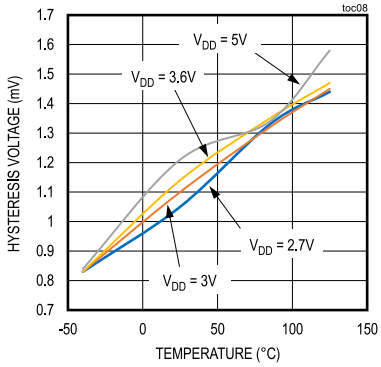
INPUT BIAS CURRENT vs. TEMPERATURE



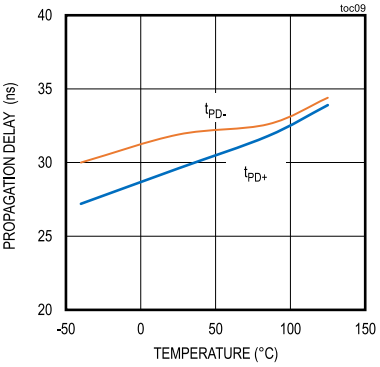
INPUT OFFSET VOLTAGE vs. TEMPERATURE



HYSTERESIS VOLTAGE vs. TEMPERATURE



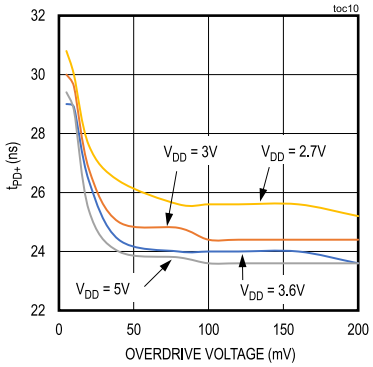
PROPAGATION DELAY vs. TEMPERATURE



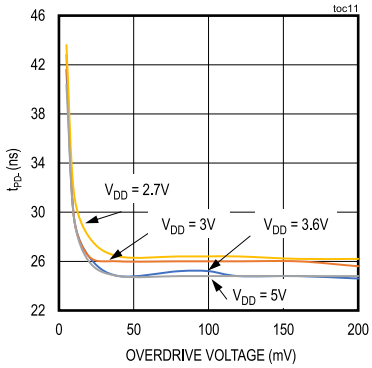
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, V_{CM} = 0.1V, C_L = 15pF, V_{OD} = 10mV, T_A = +25°C, unless otherwise noted.)

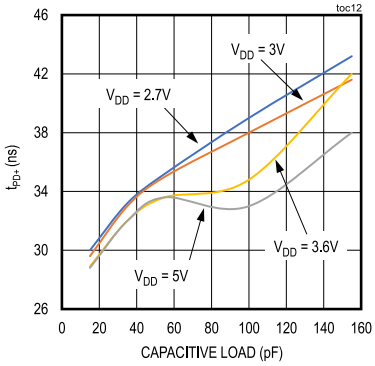
PROPAGATION DELAY (t_{PD+}) vs. INPUT OVERDRIVE



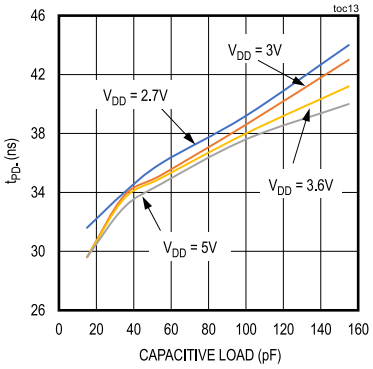
PROPAGATION DELAY (t_{PD-}) vs. INPUT OVERDRIVE



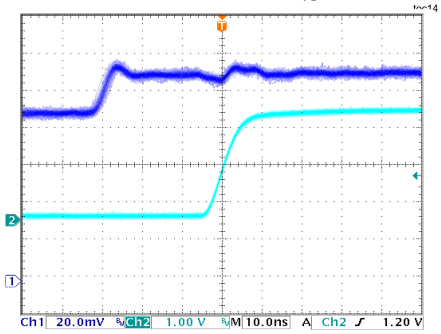
PROPAGATION DELAY (t_{PD+}) vs. CAPACITIVE LOAD



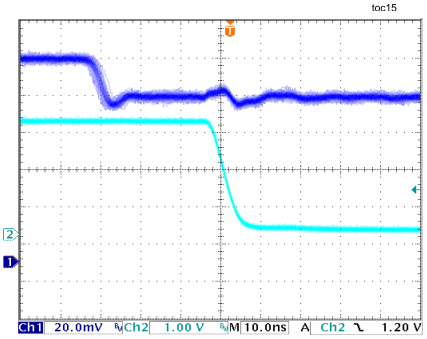
PROPAGATION DELAY (t_{PD-}) vs. CAPACITIVE LOAD



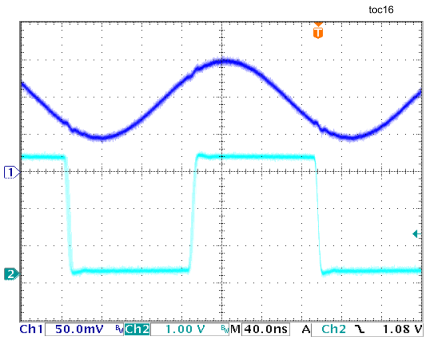
PROPAGATION DELAY t_{PD+}



PROPAGATION DELAY t_{PD-}

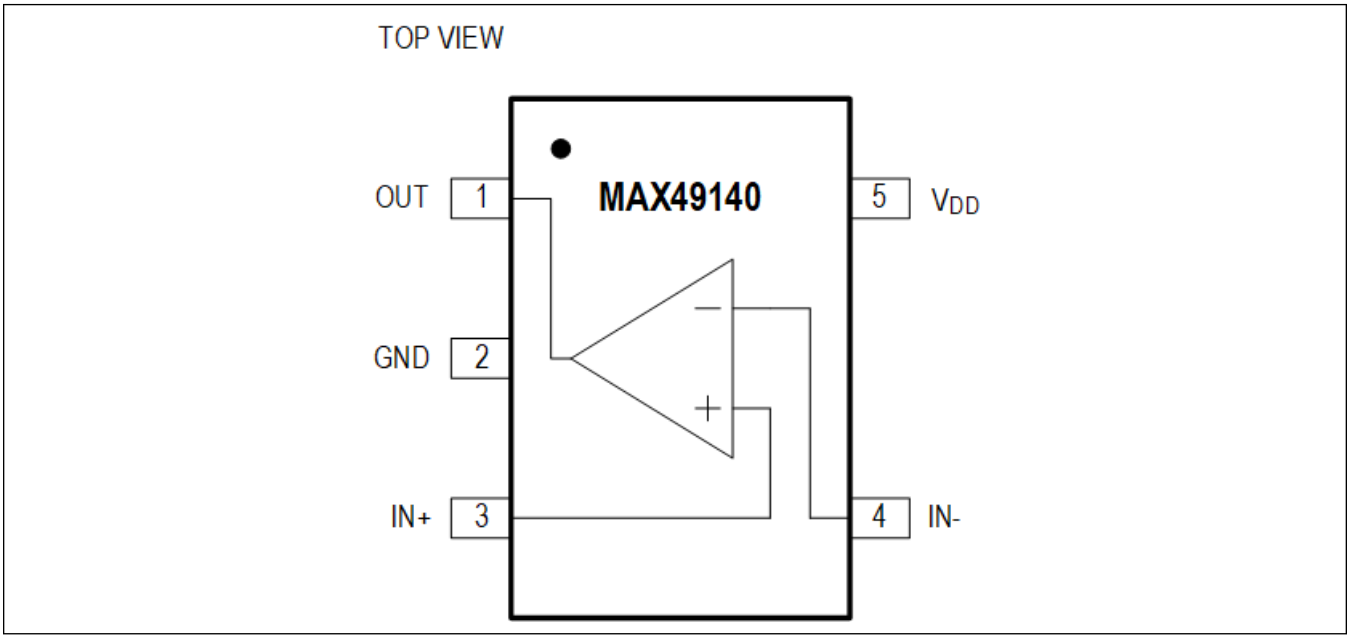


SINUSOID RESPONSE AT 4MHz



Pin Configuration

SC70



Pin Description

PIN	NAME	FUNCTION
1	OUT	Comparator Output
2	GND	Ground
3	IN+	Noninverting Input
4	IN-	Inverting Input
5	V_{DD}	Positive Supply

Detailed Description

The MAX49140 single-supply comparator features internal hysteresis, high speed, and low power. The output is pulled to within 300mV of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage, single-supply operation make the device ideal for portable equipment. The devices interface directly to CMOS and TTL logic.

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the device has an internal hysteresis of 1.2mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The device's fixed internal hysteresis eliminates these resistors. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage-divider from the output to the non-inverting input.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

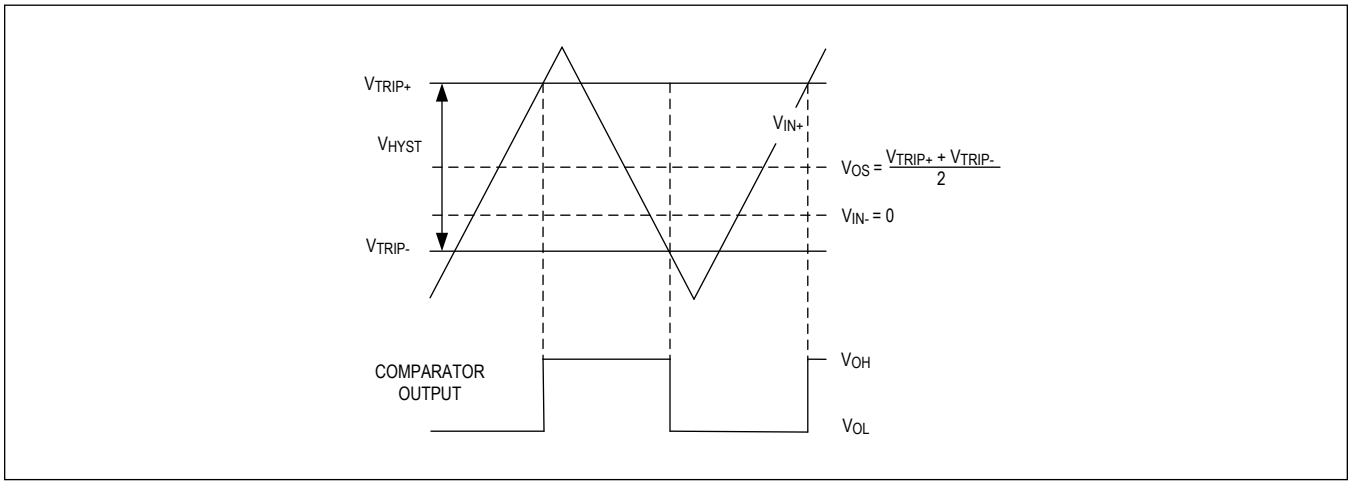


Figure 1. Input and Output Waveform, Noninverting Input Varied

Input Stage Circuitry

The device includes internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two series 1kΩ resistors (Figure 2). The diodes limit the differential voltage applied to the internal circuitry of the comparator to be no more than $2V_F$, where V_F is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{InputCurrent} = \frac{(IN+ - IN-) - 2V_F}{2x1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I_B). As long as the differential input voltage is less than $2V_F$, this input current is equal to I_B. The output is in the correct logic state if one or both inputs are within the common-mode range.

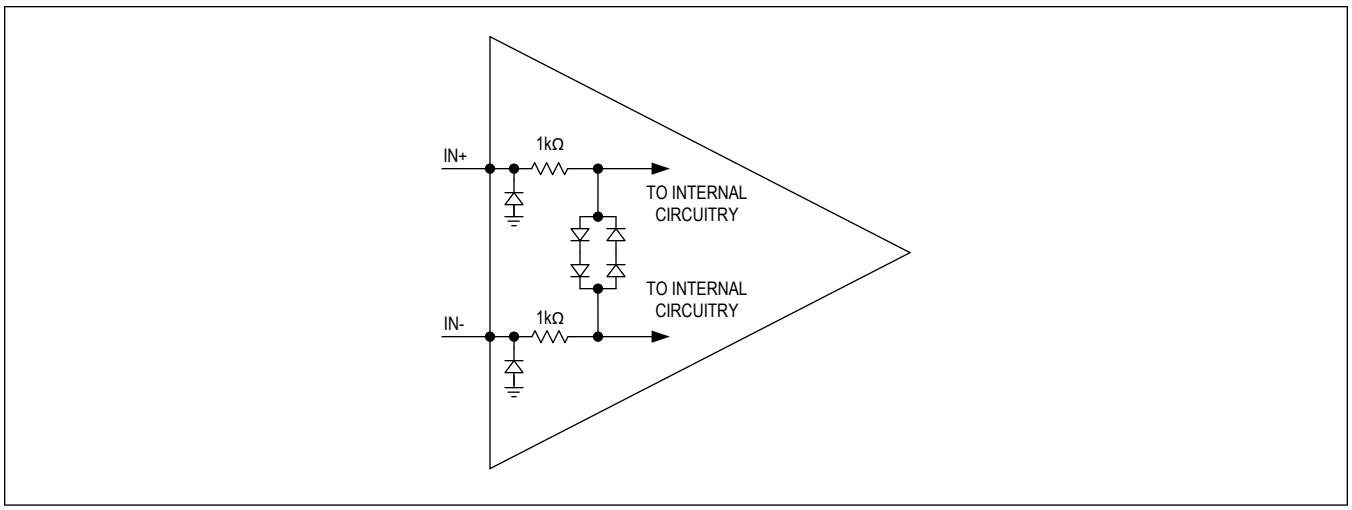


Figure 2. Input Stage Circuitry

Output Stage Circuitry

The MAX49140 contains a current-driven output stage as shown in Figure 3. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noise-sensitive applications where fast edges may cause interference.

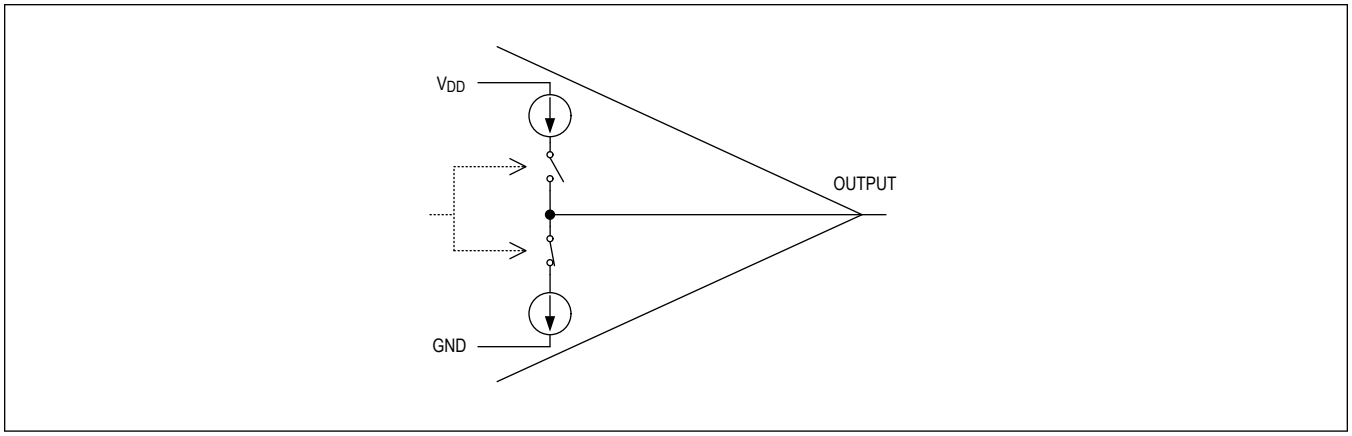


Figure 3. Output Stage Circuitry

Applications Information

Circuit Layout and Bypassing

The high-gain bandwidth of the MAX49140 requires design precautions to realize the full high-speed capabilities of this comparator. The recommended precautions are:

1) Use a PCB with a good, unbroken, low-inductance ground plane.

2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V_{DD} as possible.

3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.

4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparator.

5) Solder the device directly to the PCB instead of using a socket.

Typical Applications

Figure 4 and Figure 5 show two typical applications.

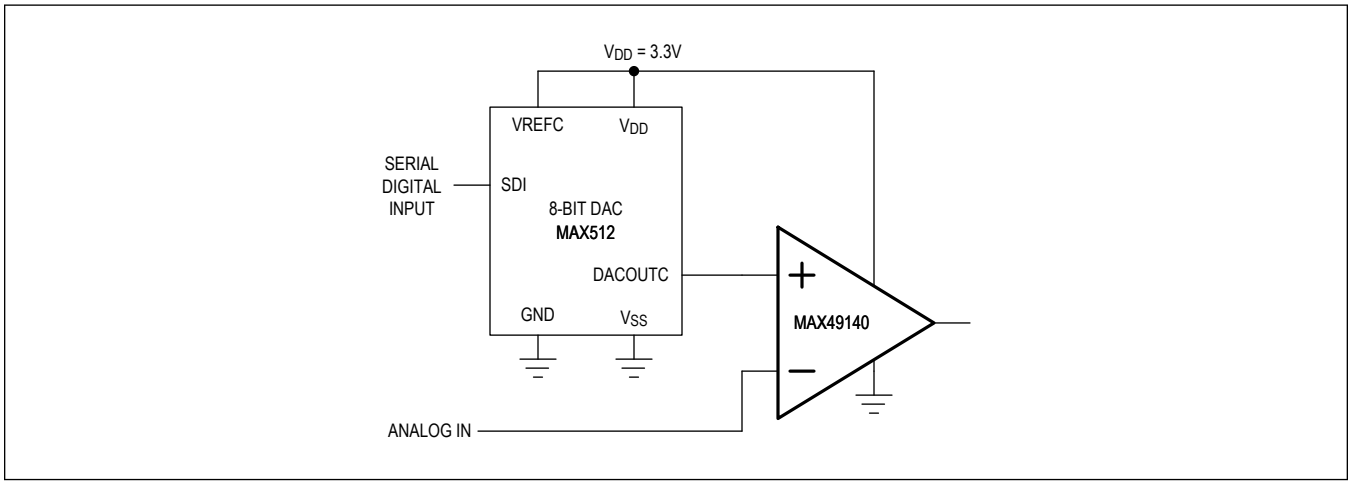


Figure 4. 3.3V Digitally Controlled Threshold Detector

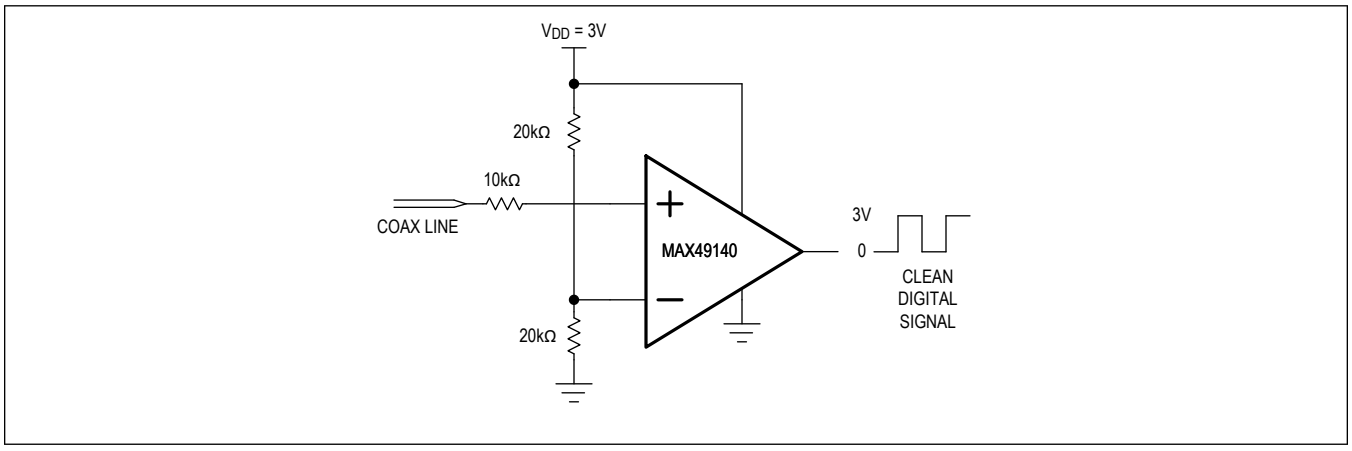


Figure 5. Line Receiver Application

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX49140AXK/V+T	-40°C to +125°C	5 SC70	+AVC

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V denotes an automotive qualified part.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/20	Release for intro	—

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