*Click here to ask an associate for production status of specific part numbers.*

# Automotive, 65V 2A/3A Mini Buck Converter

# MAX25262/MAX25263

## General Description

The MAX25262/MAX25263 are small, synchronous buck converters with integrated high-side and low-side switches. The device is designed to deliver up to 2A/3A with 3.5V to 65V input voltages while using only 3.5µA quiescent current at no load. The IC comes with a small 20ns minimum on-time capability, which enables the large step-down conversions in a single stage without skipping cycles. A max duty cycle of 98% and low high side FET ON resistance enable a low dropout operation for low input voltage applications.

The voltage quality can be monitored by observing the PGOOD signal. The device offers two fixed 5V and 3.3V output voltages. In addition, the device can be configured for 1V to 20V output voltages using an external resistor-divider. The frequency is internally fixed at 2.1MHz, which allows for small external components, reduced output ripple, and guarantees no AM interference. A 400kHz option is also offered to provide the minimum switching losses and maximum efficiency. For high light load efficiency, the IC enters skip mode at light loads when FSYNC is pulled low. A pin selectable forced pulse-width modulation (PWM) mode is also available for the EMI critical applications. The IC comes in a symmetrical flip-chip package that offers superior EMI performance. Further, the pin selectable spread spectrum helps to enhance the EMI performance.

## Applications

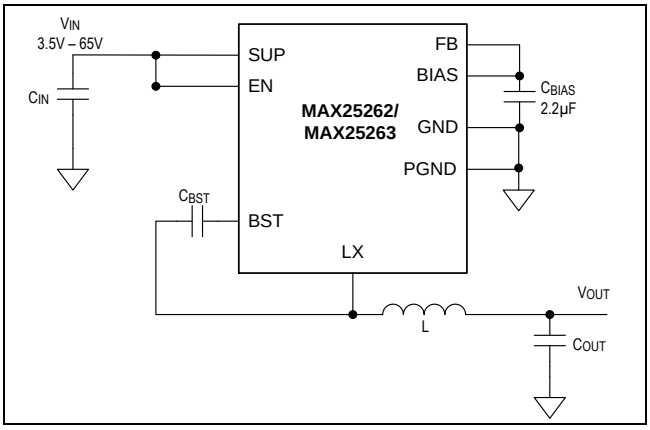
- Double Battery Automotive Systems
- Automotive Instrument Cluster
- Distributed DC Power Systems
- Navigation and Radio Head Units

***Ordering Information* appears at end of data sheet.**

## Benefits and Features

- Meets Stringent Original Equipment Manufacturer (OEM) Module Power Consumption and Performance Specifications
  - 2A/3A Output-Current Capability
  - 3.5µA Supply Current in Standby Mode
- Enables Double Battery Operation
  - Wide Input Supply Range from 3.5V to 65V
  - Programmable 1V to 20V Output Voltage
  - Fixed 5V/3.3V/12V Options Available
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 20ns (typ) Minimum On-Time Guarantees Skip-Free Operation for 3.3V Output at 2.1MHz and 24Vin
  - Spread-Spectrum Option
  - Phase-Locked Loop (PLL) Frequency Synchronization
- Protection Features Improve System Reliability
  - PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
  - Under-voltage Lockout
  - Over Temperature and Short Circuit Protection
  - AEC-Q100 Qualified

## Simplified Block Diagram




*19-101221; Rev 0; 2/22*

## Absolute Maximum Ratings

EN, SUP to PGND ..... -0.3V to 70V
LX to PGND (*Note 1*) ..... -0.3V to SUP+0.3V
SYNC, BIAS to GND ..... -0.3V to 6V
SPS, FB, EXTVCC to AGND ..... -0.3V to BIAS+0.3V
PGOOD to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
OUT to PGND ..... -0.3V to +22V
BST to LX ..... -0.3V to +6V

Continuous Power Dissipation ( ($T_A$ = +70°C, derate 35.71mW/°C above +70°C)) ..... 2857.14mW
Operating Temperature Range ..... -40°C to 125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature(soldering,10s) ..... 300°C

**Note 1:** Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITION | TYPICAL RANGE | UNIT |
|---|---|---|---|---|
| Ambient Temperature Range | | | -40 to 125 | ºC |

## Package Information

| | |
|---|---|
| Package Code | F173B3FY+1 |
| Outline Number | 21-100429 |
| Land Pattern Number | 90-100162 |
| **Thermal Resistance, Four Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 28°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 8°C/W |

## Electrical Characteristics

($V_{SUP}$ = $V_{EN}$ = 24V, $T_J$ = -40ºC to +150ºC, unless otherwise noted. Typical values are at $T_A$ = +25ºC (*Note 2* and *Note 3*))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{SUP}$ | Normal Operation | 3.5 | | 65 | V |
| Supply Current | $I_{IN}$ | $V_{EN}$ = 0V | | 1.5 | 5 | µA |
| | | $V_{EN}$ = $V_{SUP}$, Switching, EXTVCC = 3.3V | | 3.5 | | |
| Buck Fixed Output Voltage | $V_{OUT}$ | $V_{FB}$ = $V_{BIAS}$, 3.2V<$V_{OUT}$ <13V, PWM mode | -2 | | 2 | % |
| | | $V_{FB}$ = $V_{BIAS}$, 3.2V<$V_{OUT}$ <13V, Skip mode | -3 | | 3 | |
| Regulated Feedback Voltage | $V_{FB}$ | | 0.985 | 1 | 1.015 | V |

($V_{SUP}$ = $V_{EN}$ = 24V, $T_J$ = -40°C to +150°C, unless otherwise noted. Typical values are at $T_A$ = +25°C (*Note 2* and *Note 3*))

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Feedback Leakage Current | $I_{FB}$ | $T_A$ = +25°C | | | 0.01 | 1 | µA |
| Feedback Line Regulation Error | | $V_{SUP}$ = 3.5V to 65V, $V_{FB}$ = 1V | | | 0.01 | | %/V |
| Maximum Duty Cycle | | | | 96 | 97.8 | | % |
| Minimum On-Time | $T_{ON\_MIN}$ | | | | 20 | | ns |
| Switching Frequency Accuracy | $f_{SW\_400kHz}$ | | | 360 | 400 | 440 | kHz |
| | $f_{SW\_2.1MHz}$ | | | 1.9 | 2.1 | 2.32 | MHz |
| Current-Limit | $ILIM_{2A}$ | 2A version | | 2.6 | 3.6 | 5 | A |
| Current Limit | $ILIM_{3A}$ | 3A version | | 3.4 | 4.75 | 6.2 | A |
| Soft-Start Time | $t_{SS}$ | (*Note 5*) | 2.1MHz setting | 2.75 | 4 | 4.75 | ms |
| | | (*Note 5*) | 400kHz setting | 4 | 5 | 6 | ms |
| LX Leakage Current | $ILX_{LKG}$ | $V_{LX}$ = $V_{PGND}$ or $V_{IN}$, $T_A$ = +25°C | | | 0.001 | 1 | µA |
| High-Side Switch On Resistance | $RON_{HS}$ | $I_{LX}$ = 1A, $V_{BIAS}$ = 5V | | | 108 | 250 | mΩ |
| Low-Side Switch On Resistance | $RON_{LS}$ | $I_{LX}$ = 1A, $V_{BIAS}$ = 5V | | | 56 | 120 | mΩ |
| **PGOOD** | | | | | | | |
| PGOOD UV Threshold | $V_{PGOOD\_H}$ | % of VOUT, Rising | | 93 | 95 | 97 | % |
| | $V_{PGOOD\_F}$ | % of VOUT, Falling | | 91.5 | 93 | 95.5 | |
| PGOOD OV Threshold | | % of VOUT, Rising | | 106 | 108 | 110 | % |
| | | % of VOUT, Falling | | 103.5 | 105.5 | 107.5 | |
| PGOOD Output Low Voltage | | $I_{SINK}$ = 1mA | | | 0.03 | 0.2 | V |
| PGOOD Leakage Current | | $V_{PGOOD}$ = 5V, TA = +25°C | | | 0.01 | 1 | µA |
| PGOOD Debounce Time | | Fault Detection, Falling | | | 63 | | µs |
| | | Fault Detection, Rising | | | 47 | | µs |
| PGOOD Assertion Time | | PGOOD Low to High | | | 47 | | µs |
| **SYNC INPUT** | | | | | | | |
| SYNC frequency Range | | $f_{SW}$ = 2.1MHz | | 1.8 | | 2.6 | MHz |
| | | $f_{SW}$ = 400kHz | | 250 | | 550 | kHz |
| SYNC Switching Thresholds | | High Threshold | | 1.4 | | | V |
| | | Low Threshold | | | | 0.4 | |
| SYNC Pulldown | | Resistance to GND | | | 1 | | MegΩ |
| SPS INPUT | | | | | | | |
| SPS Switching Thresholds | | High Threshold | | 1.5 | | | V |
| | | Low Threshold | | | | 0.4 | |

($V_{SUP}$ = $V_{EN}$ = 24V, $T_J$ = -40°C to +150°C, unless otherwise noted. Typical values are at $T_A$ = +25°C (*Note 2* and *Note 3*))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INTERNAL LDO BIAS AND EXTVCC** | | | | | | |
| Internal BIAS Voltage | | VSUP > 6V | | 5 | | V |
| BIAS UVLO Threshold | | $V_{BIASRising}$ | | 3.1 | 3.3 | V |
| | | $V_{BIASFalling}$ | 2.4 | 2.65 | | |
| EXTVCC Operating Range | | | 3.25 | | 5.5 | V |
| EXTVCC Threshold | VTHEXTVCC | EXTVCC Rising, Hysteresis = 110mV | | 3.09 | 3.25 | V |
| **THERMAL OVERLOAD** | | | | | | |
| Thermal Shutdown Temperature | | (*Note 4*) | | 170 | | °C |
| Thermal Shutdown Hysteresis | | (*Note 4*) | | 15 | | °C |
| EN Logic Input | | | | | | |
| High Threshold | | ENHigh | 1.8 | | | V |
| Low Threshold | | ENLow | | | 0.8 | V |
| EN Input Bias Current | | EN_Logic Inputs Only, TA = +25°C | | 0.01 | 1 | µA |
| **SPREAD SPECTRUM** | | | | | | |
| Spread Spectrum | | Percentage of $f_{SW}$ | | +/- 6 | | % |

**Note 2:** Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

**Note 3:** This device is designed for continuous operation up to $T_J$ = +125°C for 95,000 hours and $T_J$ = +150°C for 5,000 hours.

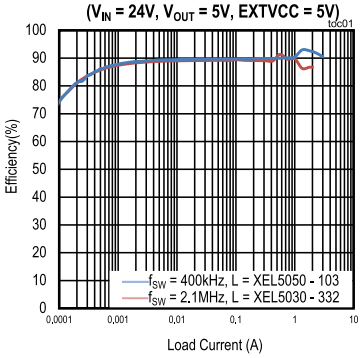
**Note 4:** Guaranteed by design, not production tested.

**Note 5:** Soft-start time is measured as the time taken from EN going high to PGOOD going high.

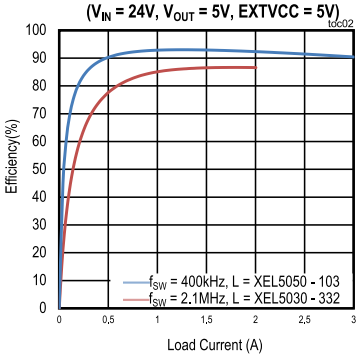
## Typical Operating Characteristics

($V_{SUP}$ = 24V, $T_A$ = +25°C, unless otherwise stated.)

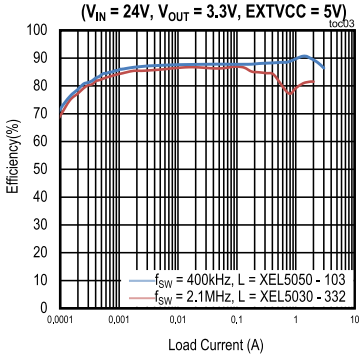
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
($V_{IN}$ = 24V, $V_{OUT}$ = 5V, EXTVCC = 5V)



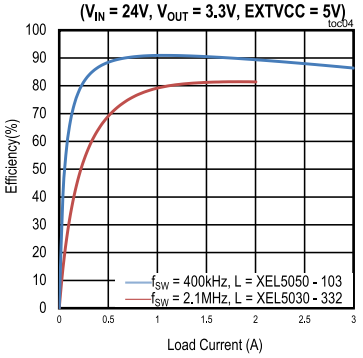

EFFICIENCY vs. LOAD CURRENT
FPWM MODE
($V_{IN}$ = 24V, $V_{OUT}$ = 5V, EXTVCC = 5V)



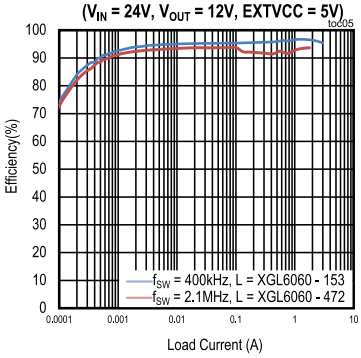

EFFICIENCY vs. LOAD CURRENT
SKIP MODE
($V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, EXTVCC = 5V)



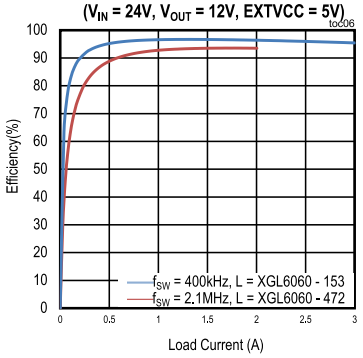

EFFICIENCY vs. LOAD CURRENT
FPWM MODE
($V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, EXTVCC = 5V)



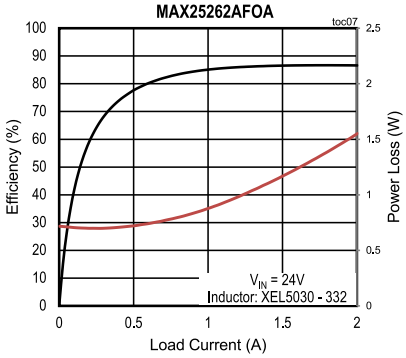

EFFICIENCY vs. LOAD CURRENT
SKIP MODE
($V_{IN}$ = 24V, $V_{OUT}$ = 12V, EXTVCC = 5V)



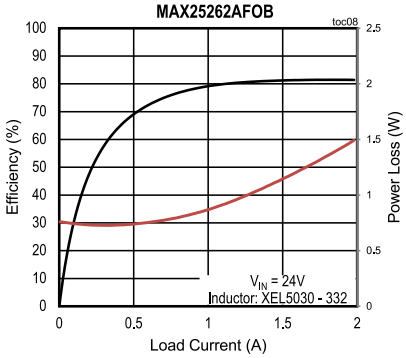

EFFICIENCY vs. LOAD CURRENT
FPWM MODE
($V_{IN}$ = 24V, $V_{OUT}$ = 12V, EXTVCC = 5V)



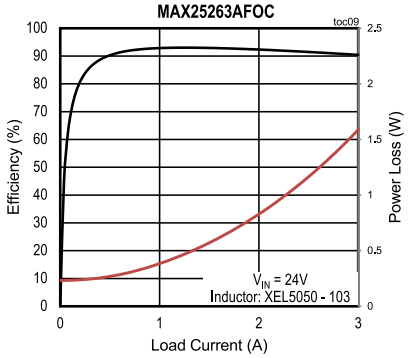

EFFICIENCY&POWER LOSS vs. LOAD CURRENT
MAX25262AFOA



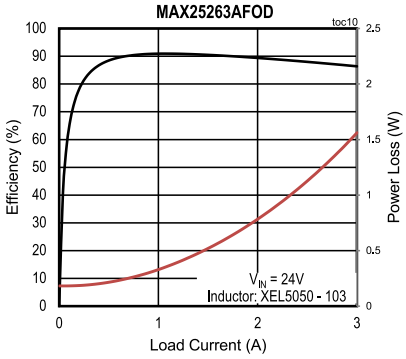

EFFICIENCY&POWER LOSS vs. LOAD CURRENT
MAX25262AFOB



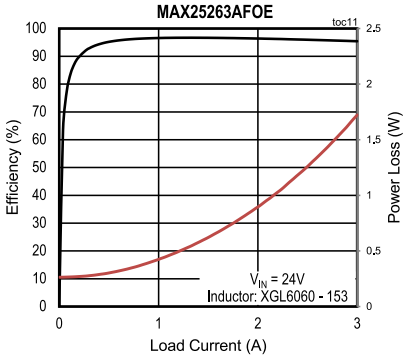

EFFICIENCY&POWER LOSS vs. LOAD CURRENT
MAX25263AFOC



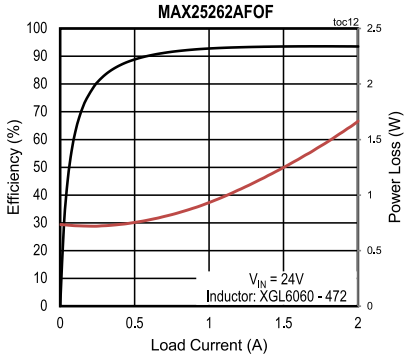
EFFICIENCY&POWER LOSS vs. LOAD CURRENT
MAX25263AFOD



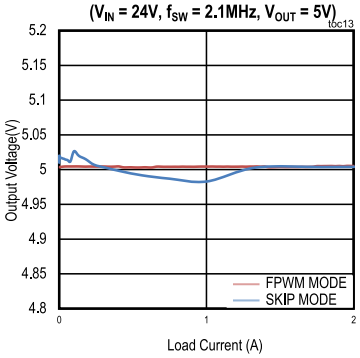

EFFICIENCY&POWER LOSS vs. LOAD CURRENT
MAX25263AFOE



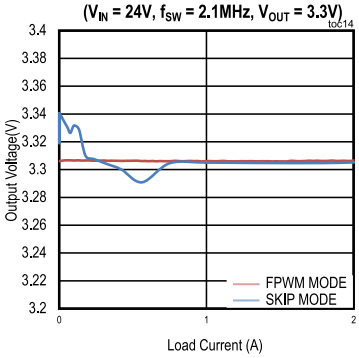

EFFICIENCY&POWER LOSS vs. LOAD CURRENT
MAX25262AFOF



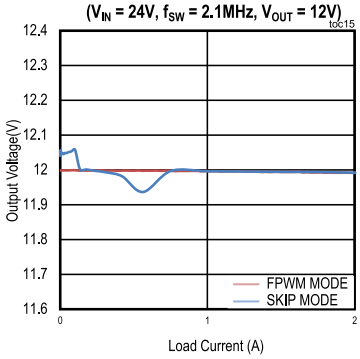

LOAD REGULATION
($V_{IN}$ = 24V, $f_{SW}$ = 2.1MHz, $V_{OUT}$ = 5V)



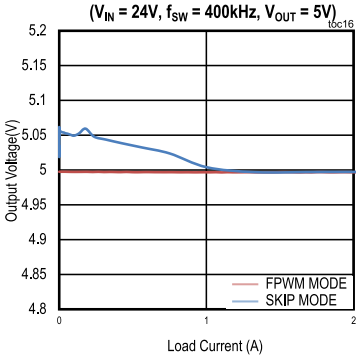

LOAD REGULATION
($V_{IN}$ = 24V, $f_{SW}$ = 2.1MHz, $V_{OUT}$ = 3.3V)



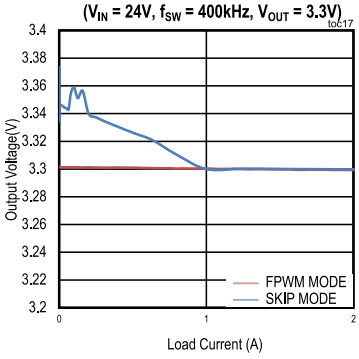

LOAD REGULATION
($V_{IN}$ = 24V, $f_{SW}$ = 2.1MHz, $V_{OUT}$ = 12V)



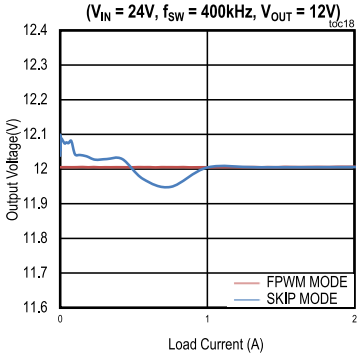

LOAD REGULATION
($V_{IN}$ = 24V, $f_{SW}$ = 400kHz, $V_{OUT}$ = 5V)



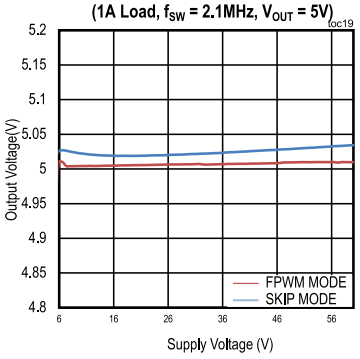

LOAD REGULATION
($V_{IN}$ = 24V, $f_{SW}$ = 400kHz, $V_{OUT}$ = 3.3V)



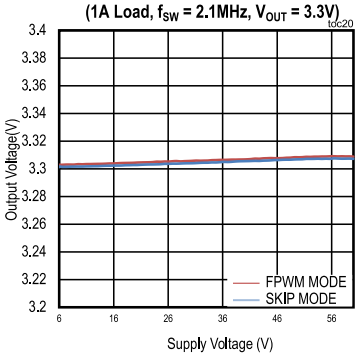

LOAD REGULATION
($V_{IN}$ = 24V, $f_{SW}$ = 400kHz, $V_{OUT}$ = 12V)



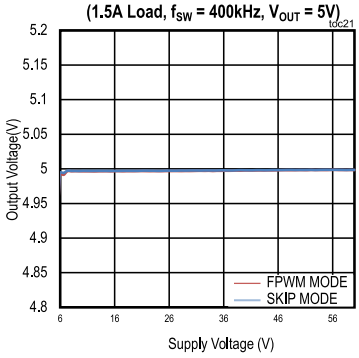
LINE REGULATION
(1A Load, $f_{SW}$ = 2.1MHz, $V_{OUT}$ = 5V)



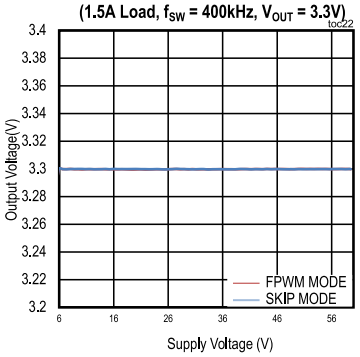

LINE REGULATION
(1A Load, $f_{SW}$ = 2.1MHz, $V_{OUT}$ = 3.3V)



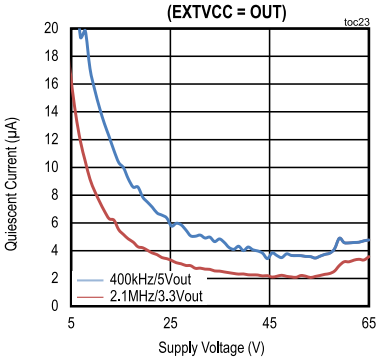

LINE REGULATION
(1.5A Load, $f_{SW}$ = 400kHz, $V_{OUT}$ = 5V)



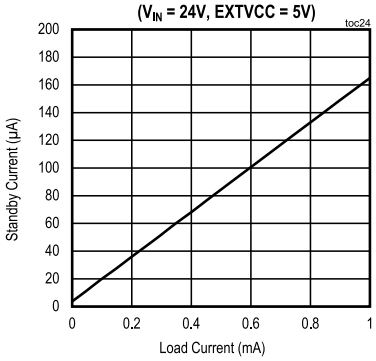

LINE REGULATION
(1.5A Load, $f_{SW}$ = 400kHz, $V_{OUT}$ = 3.3V)



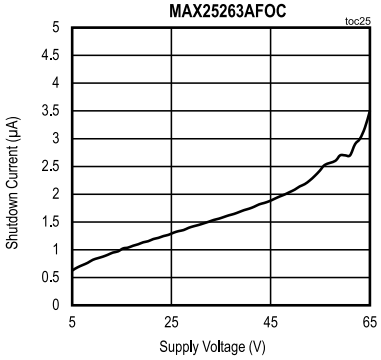

QUIESCENT CURRENT vs. SUPPLY VOLTAGE
(EXTVCC = OUT)



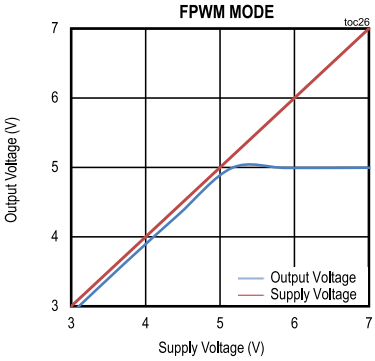

STANDBY CURRENT vs. LOAD CURRENT
MAX25262AFOB
($V_{IN}$ = 24V, EXTVCC = 5V)



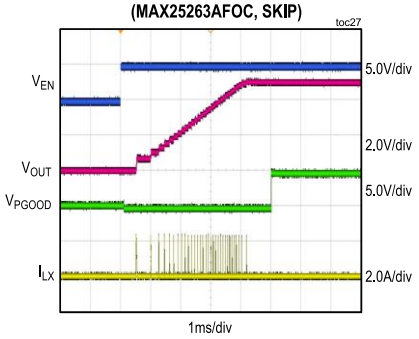

SHUTDOWN CURRENT vs. SUPPLY VOLTAGE
MAX25263AFOC



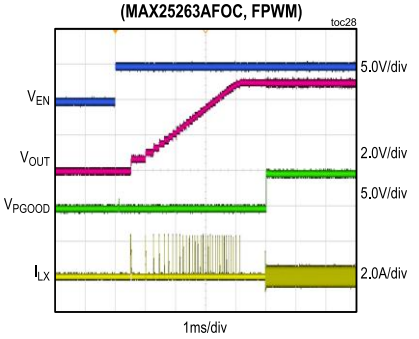

OUTPUT VOLTAGE vs. SUPPLY VOLTAGE
MAX25263AFOC
FPWM MODE



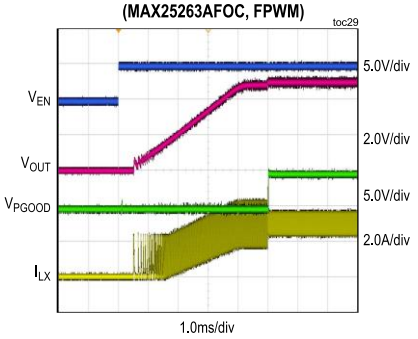

STARTUP INTO NO LOAD
(MAX25263AFOC, SKIP)



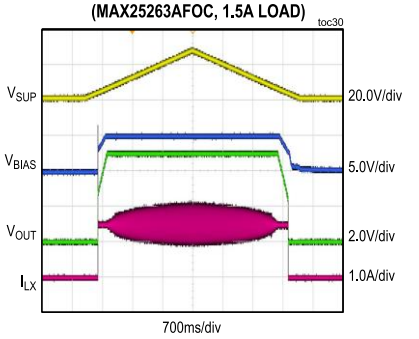
STARTUP INTO NO LOAD
(MAX25263AFOC, FPWM)



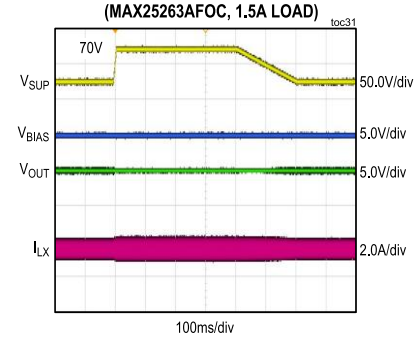

STARTUP INTO FULL LOAD
(MAX25263AFOC, FPWM)



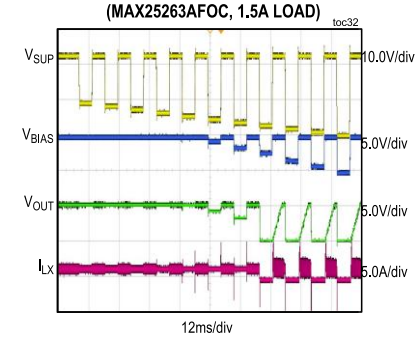

SLOW INPUT VOLTAGE RISING
(MAX25263AFOC, 1.5A LOAD)



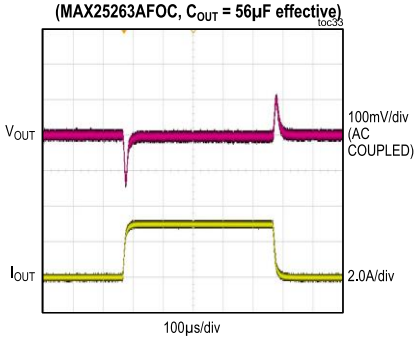

LOAD DUMP
(MAX25263AFOC, 1.5A LOAD)



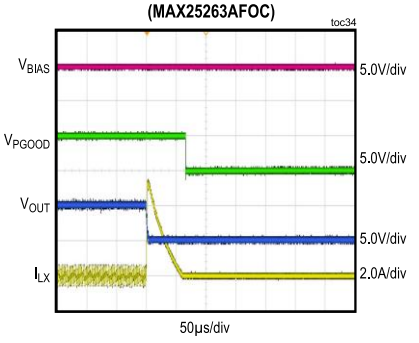

DIPS AND DROPS
(MAX25263AFOC, 1.5A LOAD)



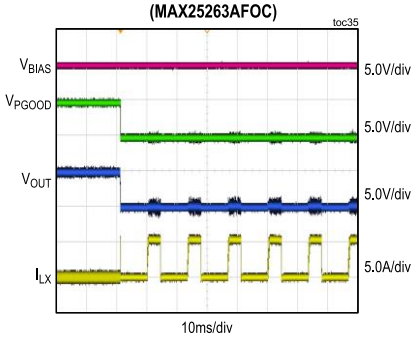

LOAD TRANSIENT
(MAX25263AFOC, $C_{OUT}$ = 56µF effective)



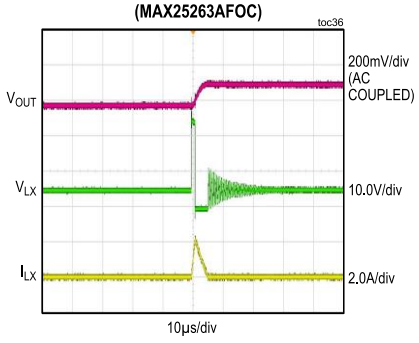

SHORT CIRCUIT RESPONSE
(MAX25263AFOC)



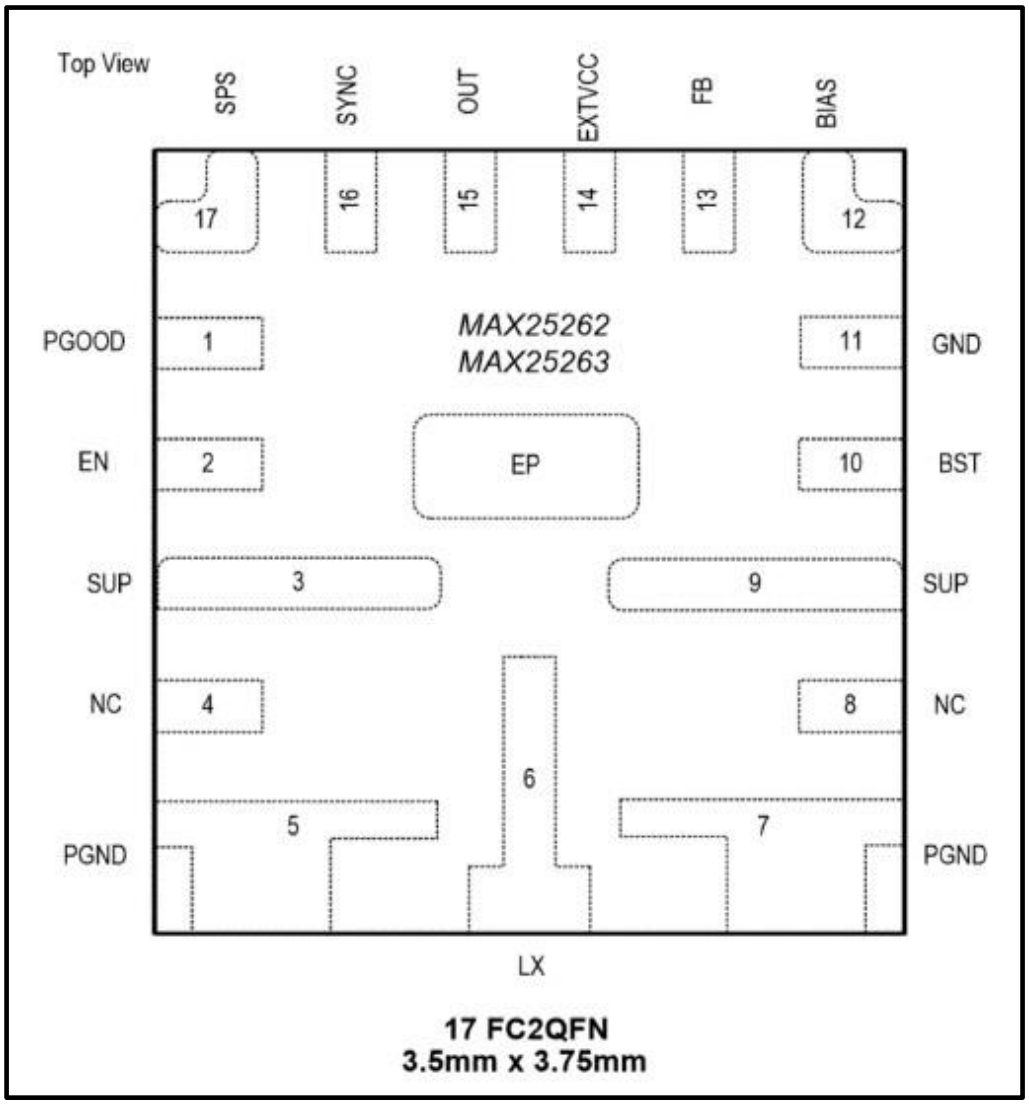

HIPCUP MODE
(MAX25263AFOC)




SKIP MODE NO LOAD OPERATION
(MAX25263AFOC)



## Pin Configurations

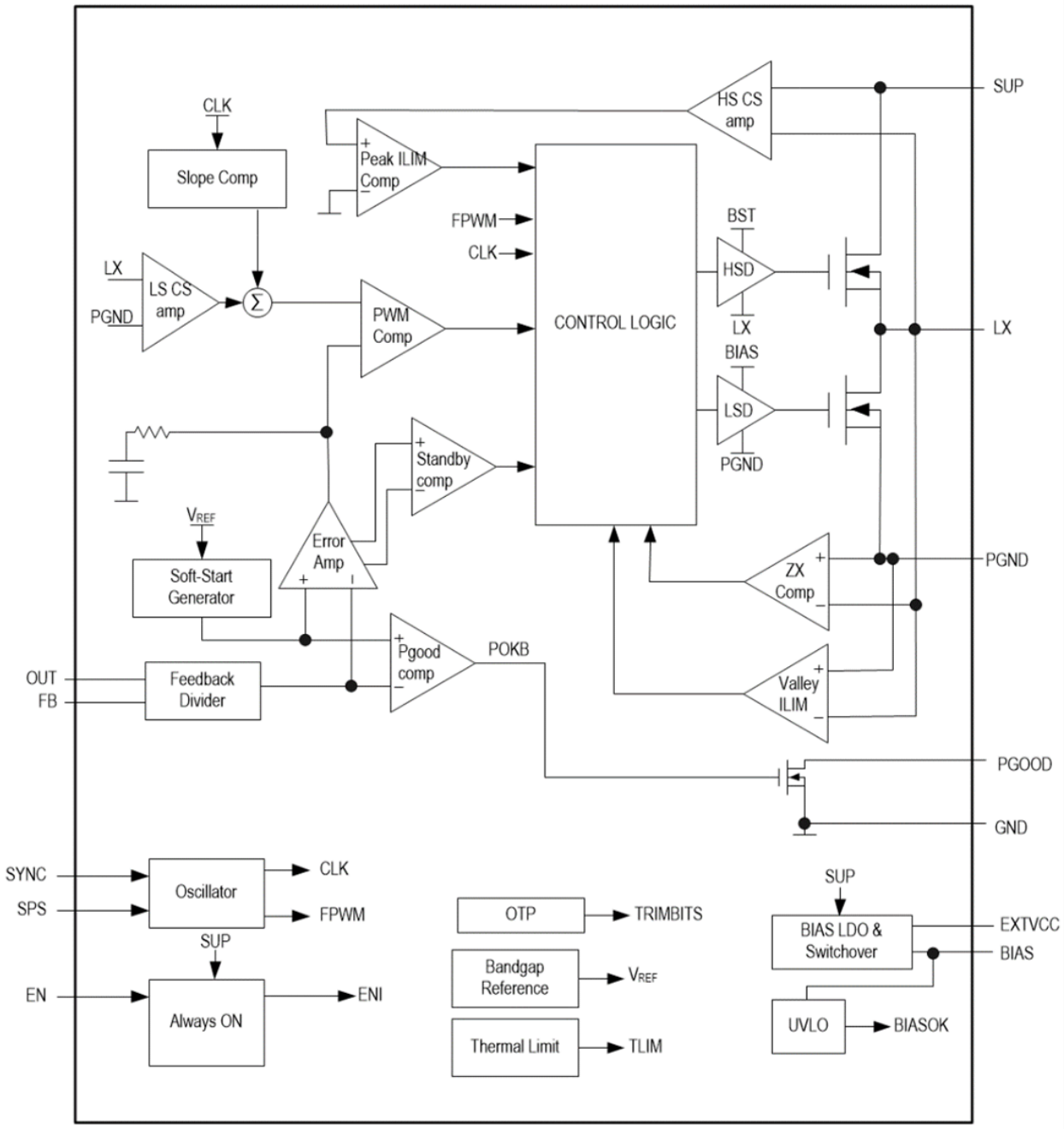



## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | PGOOD | Open drain pin, tie through pullup resistor to a 5.5V or less supply. This pin goes high when OUT is within normal range. |
| 2 | EN | SUP Voltage-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device. |
| 3 | SUP | Internal High-Side Supply Input. SUP provides power to the internal switch and LDO. Bypass each SUP to PGND with a 0.1µF and 2.2µF ceramic capacitors. Place the 0.1µF as close to the SUP and PGND pins as possible, followed by the 2.2µF capacitor. Place these caps on both sides of the part. |
| 4 | N/C | No connect. |
| 5 | PGND | Power Ground.Connect all PGND pins together. |
| 6 | LX | Inductor Connection. Connect LX to the switched side of the inductor. |
| 7 | PGND | Power Ground. |

| | | |
|---|---|---|
| 8 | N/C | No connect. |
| 9 | SUP | Internal High-Side Supply Input. SUP provides power to the internal switch and LDO. Bypass SUP to PGND with a 0.1µF and 2.2µF ceramic capacitors. Place the 0.1µF as close to the SUP and PGND pins as possible, followed by the 2.2µF capacitor. Place these caps on both sides of the part. |
| 10 | BST | High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST. |
| 11 | GND | Analog Ground. |
| 12 | BIAS | Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a minimum of 2.2µF ceramic capacitor to ground. |
| 13 | FB | Feedback Input. For external feedback, connect a resistor divider from OUT to FB to GND to set the output voltage. Connect FB to BIAS to select a fixed output voltage (P/N dependent). |
| 14 | EXTVCC | External VCC power and Switchover Comparator Input. Connect a voltage between 3.25V and 5.5V to EXTVCC to power the IC and bypass the internal bias LDO. Connect EXTVCC to ground if not used. |
| 15 | OUT | Output Sense Input. When using the internal preset feedback divider, FB is connected to BIAS, and the converter uses OUT to sense the output voltage. |
| 16 | SYNC | Synchronization Input. Connect SYNC to GND to enable skip-mode operation under light loads. Connect SYNC to BIAS or an external clock to enable fixed-frequency forced-PWM-mode operation. When driving SYNC externally do not exceed the BIAS voltage. The BIAS pin may transition from 5V to the output voltage after startup to increase efficiency. |
| 17 | SPS | Spread Spectrum Enable Input. Connect to BIAS to enable spread spectrum. Connect to GND to disable Spread Spectrum. |
| | EP | Connect to input supply voltage along with pins 3 and 9. |

## Functional Diagrams



## Detailed Description

The MAX25262/MAX25263 are 2A and 3A current-mode step-down converters, respectively, with integrated high-side and low-side MOSFETs. The devices operate with 3.5V to 65V input voltages while using only 5µA (typ) quiescent current at no load. The switching frequency is fixed internally at 400kHz or 2.1MHz and can be synchronized to an external clock. The spread spectrum is pin selectable. The devices' output voltage is available as fixed at 5V or 3.3V, or adjustable between 1V and 20V. The wide input voltage range, along with the ability to operate at a 98% duty cycle during undervoltage transients, makes these devices ideal for automotive applications. In light-load applications, a logic input (SYNC) allows the devices to operate either in skip mode for reduced current consumption, or in fixed-frequency FPWM mode to eliminate frequency variation and helps to minimize the EMI.

The IC comes in a small 3.5mmx3.75mm FCQFN package with pin out optimized to enhance the EMI performance. The protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

### Internal 5V BIAS LDO

An internal 5V BIAS LDO supplies the IC internal circuitry. The SUP supplies the internal BIAS LDO. Bypass BIAS with a minimum 2.2µF ceramic capacitor. To minimize the internal power dissipation, bypass BIAS to an external 5V rail using the EXTVCC pin.

### EXTVCC Switchover

The internal linear regulator can be bypassed by connecting an external 3.25V to 5.5V supply or the buck converter output to EXTVCC. With a valid supply applied to the EXTVCC, the BIAS is internally switched to the EXTVCC, and the internal linear regulator turns off. This configuration has two main advantages:

1. Reduces IC internal power dissipation.
2. Improves light-load efficiency as the internal supply current is scaled down proportionally to the duty cycle if connecting any buck output to EXTVCC.

If the EXTVCC drops below 3V (typ), the internal regulator is enabled, and the BIAS is switched back to 5V.

The 5V for EXTVCC is recommended for optimal efficiency since any voltage lower than 5V on EXTVCC will cause the Rdson of the FETs to increase, which increases the internal power dissipation.

**Note:** When the output voltage is set to be higher than 5V, the EXTVCC should not be connected to the output, as that would exceed the EXTVCC abs max condition and may cause permanent damage to the IC.

### Switching Frequency/External Synchronization

The MAX25262/MAX25263 provide an internal oscillator with 400kHz and 2.1MHz fixed frequency options. The 2.1MHz frequency operation optimizes the application for the smallest component size, at the cost of lower efficiency. The 400kHz frequency operation offers the best overall efficiency at the expense of component size and board space.

Apply an external clock to SYNC to enable the frequency synchronization. The MAX25262/MAX25263 use a phase-locked loop (PLL) to synchronize the internal oscillator to an external clock signal. The external SYNC signal should have a duty cycle of between 25% and 75%.

### Spread Spectrum Option

The ICs feature enhanced EMI performance with a spread spectrum option. The spread spectrum is pin selectable using an SPS pin. To enable the spread spectrum, pull the pin high. When the spread spectrum is enabled, the operating frequency is varied ±6% centered at the switching frequency. The modulation signal is a triangular wave with a period of 110µs at 2.1MHz. Therefore, switching frequency ramps down 6% and back to 2.1MHz in 110µs and also ramps up 6% and back to 2.1MHz in 110µs and the cycle repeats.

For operations at 400kHz, the modulation signal scales proportionally (the 110µs modulation period for 2.1MHz increases to 110µs x 2.1MHz/0.4MHz = 577.5µs).

The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the SYNC pin and pass any modulation (including spread spectrum) present on the driving external clock.

### SYNC Mode Selection

To enable the skip mode, drive the SYNC low. In skip mode, the high-side FET turns for a fixed adaptable on-time (depending on VOUT, VSUP, and FSW). The high-side FET then turns off and the low-side FET turns on until the inductor current falls to zero cross threshold. Once the low-side FET turns off by hitting the zero-crossing threshold, LX becomes high impedance, and the output voltage keeps decreasing. When the output voltage or FB voltage is detected below the set point, the new cycle starts by turning on the high-side FET again. In this way, the regulator switches only as needed to service load to improve system efficiency.

To enable the forced PWM (FPWM) mode, drive the SYNC high. The FPWM mode prevents the regulator from entering skip mode by disabling the zero-cross detection of the inductor current. The benefit of the FPWM mode is to keep the switching frequency constant under all load conditions. However, the FPWM operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions. The FPWM mode is useful to improve the load-transient response and eliminate unknown frequency harmonics that can interfere with AM radio bands.

### Over Current Protection

The MAX25262/MAX25263 have a cycle-by-cycle current limit and include a hiccup mode to prevent any damage from overcurrent or short-circuit on the power channel. When the inductor current continuously hits the current limit at over current, the output voltage starts decreasing. If the IC detects the output voltage drops below 70% of the programmed regulation value, it turns off that channel. After waiting for about 10ms of hiccup time, the IC restarts that channel in case overcurrent or short-circuit condition is removed.

### Soft-Start

When the IC is enabled, the soft-start circuitry gradually ramps up the reference voltage during soft-start time to reduce the input surge current during startup. Before the soft-start can be enabled, the BIAS voltage must exceed its UVLO threshold (3.1V typ).

For the parts using an external divider or fixed internal output parts that have an output voltage higher or equal to 5V, the 2.1Mhz parts have a 2.75ms ramp time, and the 400kHz parts have a 3.6ms ramp time.

For fixed output parts that have an output voltage lower than 5V, the soft-start ramp time can be calculated as follows:

$$t_{ss-ramp} = \frac{V_{out}}{5} \times 2.75 \; for \; 2.1Mhz$$

$$t_{ss-ramp} = \frac{V_{out}}{5} \times 3.6 \; for \; 400khz$$

### Internal Gate Driver Supply

The gate drive for internal MOSFETs is driven by the internal BIAS voltage. In case the EXTVCC is not supplied externally with a power supply in the given range, the IC uses an internal LDO at 5V for the MOSFET gate drive. In case of an appropriate voltage on the EXTVCC, the internal LDO is turned OFF and the gate drive voltage is equal to the voltage at the EXTVCC.

The MOSFET RdsON and gate capacitance charge depend heavily on the gate drive voltage. Thus, the efficiency and thermal performance of the IC depend on the voltage provided on the EXTVCC. An external +5V supply on the EXTVCC is recommended as that saves power dissipation in the internal LDO and enhances the MOSFETs for low RdsON.

### Thermal Overload Protection

The thermal overload protection limits total power dissipation in the ICs. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 20°C.

### Undervoltage Lockout (UVLO)

The internal 5V BIAS LDO undervoltage-lockout (UVLO) circuitry inhibits switching if the BIAS voltage drops below its 2.6V (typ) UVLO falling threshold. Once the BIAS voltage rises above its UVLO rising threshold, 3.1V (typ), and EN is pulled high, the IC starts switching and its output voltage begins to soft-start.

### Frequency Foldback

The frequency foldback is implemented in the buck converters when operating at only 2.1MHz and when the internal fixed output voltage option is selected. When the input voltage of a buck converter drops close to the output voltage, the converter runs at a maximum duty cycle of 98.6% (typ). To prevent the output voltage drifting out of regulation, frequency foldback is used to automatically reduce the switching frequency from 2.1MHz to 262.5kHz and maintain a high duty cycle of 98.6% (typ). The frequency foldback occurs when the input voltage drops below a certain threshold calculated by the formula of $V_{SUP} = 1.4 \times V_{OUT}$. Specially for 3.3V part, this threshold is calculated by $V_{SUP} = 1.56 \times V_{OUT}$.

### Power-Good Indicator (PGOOD)

The IC includes a power-good indicator to indicate the buck output voltage status. The PGOOD indicator can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn-on subsequent supplies.

The PGOOD goes from low to high impedance when the corresponding regulator output voltage rises above 95% (typ) of its nominal regulation voltage. The PGOOD goes low when the corresponding regulator output voltage drops below 93% (typ) of its nominal regulation voltage. Connect a 20kΩ (typ) pullup resistor from the PGOOD to the relevant logic rail to level-shift the signal. The PGOOD asserts low during soft-start, and when the buck converter is disabled. If the output voltage rises above 108% (typ) of its nominal regulation voltage, the PGOOD goes low after the debounce time. After the output voltage drops below 105% (typ) of its nominal regulation voltage, the PGOOD goes high again after the assertion time expires.

## Applications Information

### Setting Output Voltage

As shown in *Figure 1*, connect FB to BIAS to enable a fixed buck output voltage set by a preset internal resistive divider connected between OUT and GND. To externally adjust the output voltage between 1V and 20V, connect a resistive voltage-divider from the converter output (OUT) to FB and then to AGND. Set $R_{FB2}$ to any value between 10kΩ and 100kΩ and use the following equation to calculate the top-side ($R_{FB1}$):

$$R_{FB1} = R_{RB2} \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

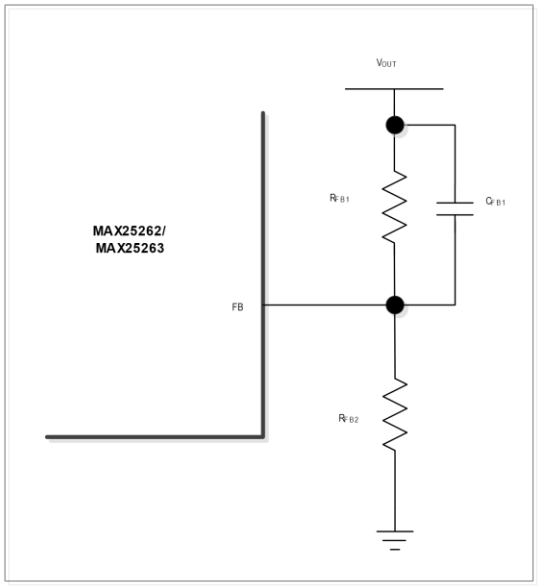



*Figure 1. Setting Output Voltage*

Where, $V_{FB} = 1V(typ)$ (For more information, see the *Electrical Characteristics* table).

**Note:** For an output voltage higher that 12V, contact the factory.

### Input Capacitor

A total of 4.7µF ceramic input capacitance is recommended for proper buck operation. This value can be adjusted based on the application's input-voltage-ripple requirements. The package comes with two symmetrical SUP pins. Connect these pins with high frequency ceramic caps (for example, 0.1µF 0603) to the ground and place them as close as possible to the IC in a symmetrical fashion for the best EMI results. For more information, see the *PCB Layout Guidelines* section.

The input capacitor RMS current requirement (IRMS) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times \left(V_{SUPSW\_} - V_{OUT}\right)}}{V_{SUPSW\_}}$$

The IRMS has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore,

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔVQ (caused by the capacitor discharge) and ΔVESR (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. The total voltage ripple is the sum of ΔVQ and ΔVESR that peaks at the end of an on-cycle. Calculate the input capacitance and equivalent series resistance (ESR) required for a specific ripple by using the following equation:

$$ESR[\Omega] = \frac{\Delta V_{ESR}}{\left(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN}[\mu F] = \frac{I_{LOAD(MAX)} \times \frac{V_{OUT}}{V_{IN}}}{\Delta V_Q \times f_{SW}}$$

Where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and,

$I_{LOAD(MAX)}$ = Maximum output current in A,

$\Delta I_{P-P}$ = Peak-to-peak inductor current in A,

$f_{SW}$ = Switching frequency in MHz,

L = Inductor value in µH.

### Inductor Selection

The MAX25262/MAX25263 operate with two switching frequency options: 2.1MHz and 400kHz. The inductor design is based on the compromise between the size, efficiency, control-loop bandwidth, and stability of the converter.

The key parameters for inductor selection are inductance value (L), inductor saturation current ($I_{SAT}$), and DC resistance ($R_{DCR}$). The nominal required inductance is calculated as:

$$L_{nom} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

Where LIR is the ratio of the inductor peak-to-peak ripple current to DC average current, and 0.35 is a typical value to use.
The inductance value also depends on the compensation design, which in this case is done internally. Hence, a value of inductance for each application is recommended to optimize the size of the solution, efficiency, and compensation design. For the recommended inductors for optimum transient response and the highest efficiency, see *Table 1*. The inductor's saturation current rating must meet or exceed the LX current limit.

A large inductor reduces the ripple, however, increases the size and cost of the solution and slows the response.

**Note:** If a smaller ripple is needed, contact the factory for the optimized design.

## Table 1. Recommended Component Selection

| SWITCHING FRQUENCY | INDUCTOR | EFFECTIVE OUTPUT CAPACITANCE (µF) |
|---|---|---|
| 2.1MHz | 3.3µH | 24µF |
| 400kHz | 10µH | 56µF |

### Output Capacitor

The actual capacitance value required relates to the physical size needed to achieve low ESR as well as the chemistry of the capacitor technology. The capacitor is usually selected by the ESR and the voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent $V_{SAG}$ and $V_{SOAR}$ from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot is no longer a problem.

The total voltage sag ($V_{SAG}$) can be calculated as follows:

$$V_{SAG} = \frac{L \times \left(\Delta I_{LOAD(MAX)}\right)^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)} \times (t - \Delta t)}{C_{OUT}}$$

The amount of overshoot ($V_{SOAR}$) during a full-load to no-load transient due to stored inductor energy can be calculated as follows:

$$V_{SOAR} = \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

For the recommended output capacitance, see *Table 1*.

### ESR Considerations

The output capacitor must have a low enough equivalent ESR to meet output ripple and load transient requirements. When using high-capacitance, low-ESR capacitors, the ESR of the filter capacitor dominates the output voltage ripple:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

### PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. For a good PCB layout, see *Figure 2* and the following guidelines:

- Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.
- Place the ceramic input bypass capacitors, $C_{BP}$ and $C_{IN}$, as close as possible to the SUP, SW, and PGND pins on both sides of the IC. Use low impedance connections (no vias or other discontinuities) between the capacitors and IC pins. $C_{BP}$ should be located closest to the IC and should have very good high frequency performance (small package size + high capacitance). Use flexible terminations or other technologies instead of series capacitors for these functions if failure modes are a concern. This provides the best EMI rejection and minimize the internal noise of the device, which can degrade performance.
- Place the inductor (L), output capacitors ($C_{OUT}$), boost capacitor ($C_{BST}$) and BIAS capacitor ($C_B$) in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors ($C_{OUT}$) near the inductor such that the ground side of COUT is near the CIN ground connection to minimize the current in the loop area. Place the BIAS capacitor ($C_B$) next to the BIAS pin.
- Use a contiguous copper GND plane on the layer next to the IC to “shield” the entire circuit. GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias on the GND pin and at the GND terminals of the IC and input/output/bypass capacitors.

**Note:** Do not separate or isolate PGND and GND connections with separate planes or areas.

- Place the feedback resistor divider (if used) near the IC and route the feedback and OUT connections away from the inductor and LX node and other noisy signals.

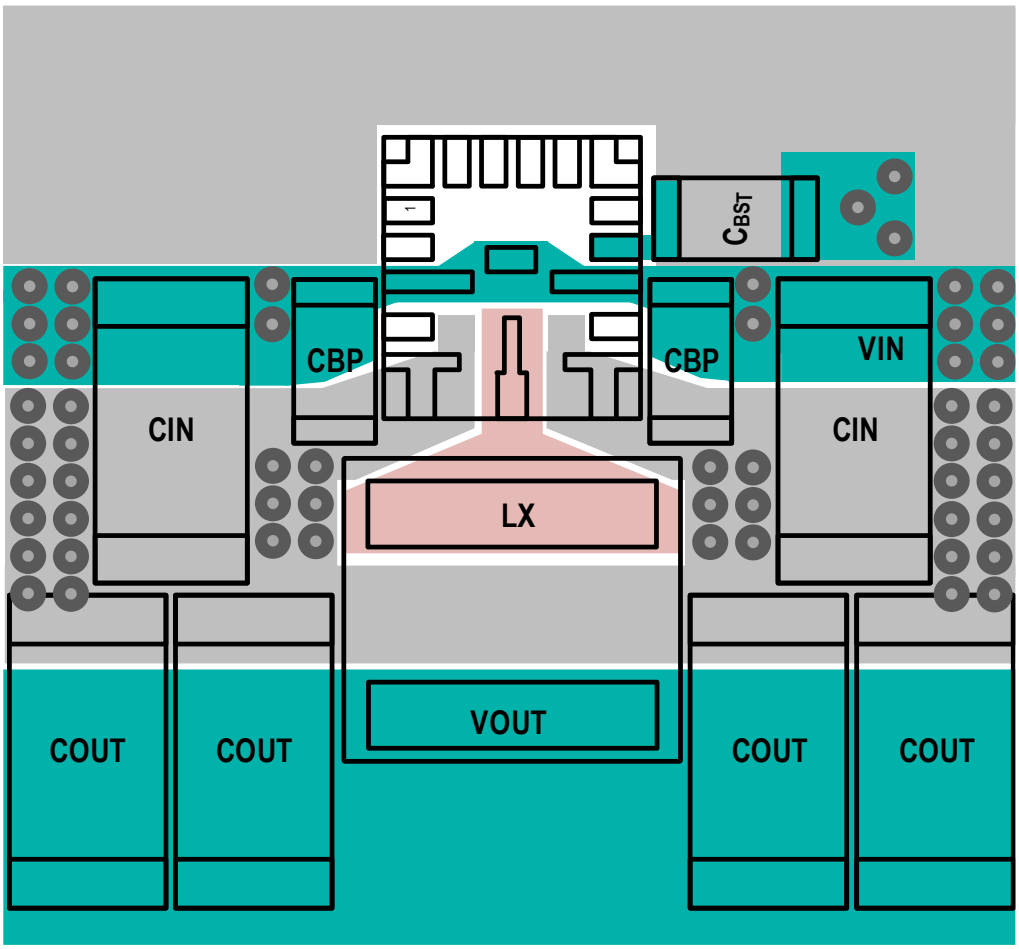
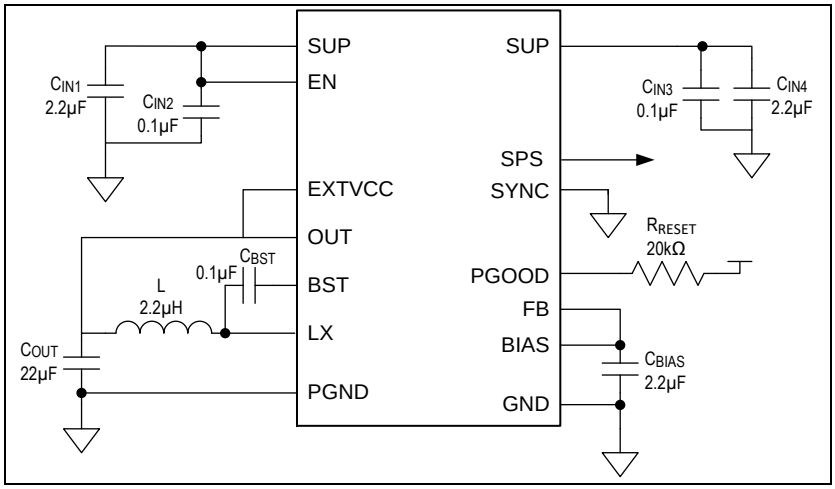



*Figure 2. Simplified Layout Example*

## Typical Application Circuits




## Ordering Information

| PART NUMBER | DESCRIPTION | IOUT (A) | FREQUENCY (kHz) |
|---|---|---|---|
| MAX25262AFOA/VY+ | Fixed 5V output or 1V to 12V external resistor divider | 2 | 2100 |
| MAX25262AFOB/VY+ | Fixed 3.3V output or 1V to 12V external resistor divider | 2 | 2100 |
| MAX25263AFOC/VY+ | Fixed 5V output or 1V to 12V external resistor divider | 3 | 400 |
| MAX25263AFOD/VY+* | Fixed 3.3V output or 1V to 12V external resistor divider | 3 | 400 |
| MAX25263AFOE/VY+* | Fixed 12V output or 1V to 12V external resistor divider | 3 | 400 |
| MAX25262AFOF/VY+ | Fixed 12V output or 1V to 12V external resistor divider | 2 | 2100 |

***For variants with different options contact factory.***

*/VY+ Denotes AEC-Q100 Automotive Qualified Parts in a Side-Wettable Package.*

*+ Indicates a lead (Pb) free/RoHS compliant package.*

** Future product - contact factory for availability.*

*1 Contact factory for output voltage higher than 12V.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 2/22 | Release for market intro | – |

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