Click here to ask about the production status of specific part numbers.

MAX22088

Home Bus System (HBS) Compatible Transceiver

General Description

The MAX22088 Home Bus transceiver complies with the Home Bus standard, where data and power are passed on one single pair of wires, while minimizing the need for external components. The MAX22088 eliminates the large external AC-blocking inductor typically required in bus powered applications and improves the signal quality to allow for longer cables. Additionally, the MAX22088 features an integrated 5V linear regulator to power system loads up to 70mA (max).

The MAX22088 supports passing power and data with speed up to, and exceeding, 200kbps. The MAX22088 features dynamic cable termination to improve the signal quality for applications with high data rates.

Additional features include adjustable receiver hysteresis, receiver thresholds and driver slew rate allow the MAX22088 to be used in a wide variety of systems.

Integrated protection (IEC 61000-4-2 ±8kV Contact and ±15kV Air-Gap ESD) ensures robust communication in harsh industrial environments. The MAX22088 is specified for operation over the -40°C to +105°C temperature range and is available in a compact 24-pin 4mm x 4mm TQFN package.

Applications

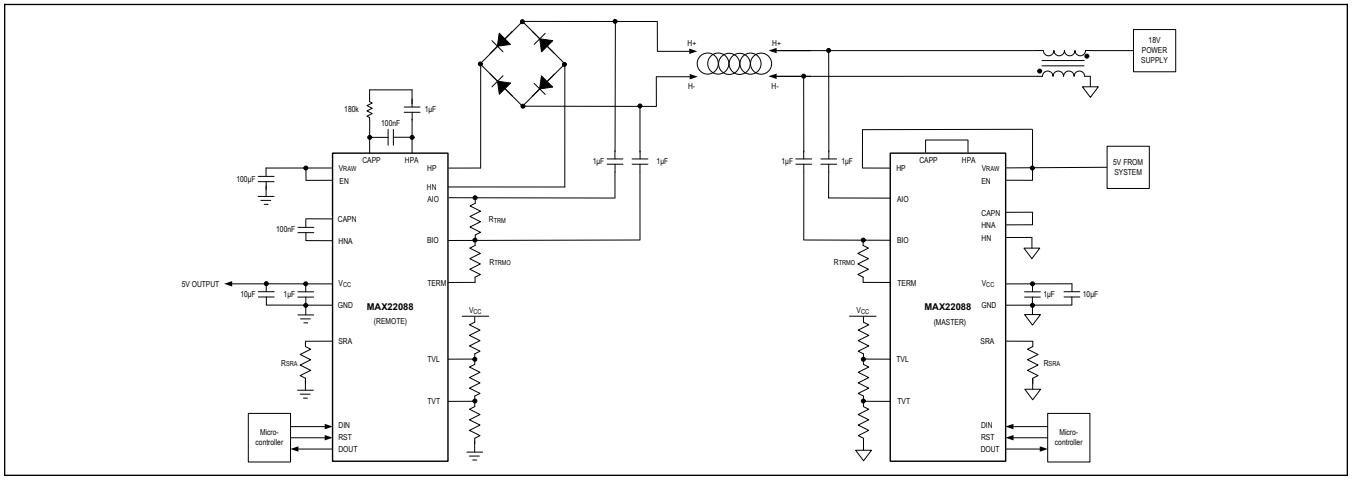
- HVAC
- Data over Power Applications
- Digital Signage
- Remote Monitoring and Sensing

Benefits and Features

- High Integration Reduces BOM and Footprint
  - Eliminates the Need for Large AC-blocking Inductor
  - Compact 4mm x 4mm TQFN Package
  - Supports External DC-DC Converter for System Loads More Than 70mA
- Configurability Enables Flexible Design
  - Adjustable Receiver Thresholds
  - Switched Cable Termination
  - Adjustable Slew Rate on Transmit Signals
  - Large Receiver Hysteresis
  - Data Rates from 9600bps to ≥200kbps
  - Dynamic Cable Termination Improves Signal Quality for High Speed Applications
- Integrated Protection for Robust Communication
  - IEC 61000-4-2 ±8kV Contact and ±15kV Air-Gap ESD Protection
  - IEC 61000-4-5 ±1kV Surge Protection with Selected External Components
  - -40°C to +105°C Operating Temperature Range
  - Thermal Shutdown Protection

***Ordering Information* appears at end of datasheet.**

Simplified Home Bus System (HBS)



19-100718; Rev 2; 2/21

Absolute Maximum Ratings

HP to HN ..... -0.3V to +28.0V
HP to GND..... -0.3V to +28.0V
HN to GND ..... -6.0V to +6.0V
HPA to CAPP ..... -0.3V to +6.0V
CAPN to HNA..... -0.3V to +6.0V
V_{RAW}, EN to GND..... -0.3V to +28.0V
V_{CC} to GND..... -0.3V to +6.0V
AIO, BIO, TERM, SRA to GND..... -0.3V to V_{CC}+0.3V
DIN, DOUT, RST, TVL, TVT, $\overline{HPEN}$ to GND..... -0.3V to +6.0V
Continuous Current Into Any Pin
HP, HN, V_{RAW}, GND..... ±250mA
V_{CC}, AIO, BIO, TERM ..... ±100mA
CAPP, CAPN..... ±10mA
All Other Pins ..... ±50mA
Continuous Power Dissipation
Single-Layer Board (T_A = +70°C, derate 20.8mW/°C above +70°C)..... 1666.70mW
Multilayer Board (T_A = +70°C, derate 27.8mW/°C above +70°C)..... 2222.20mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24-TQFN

Package Code	T2444+4C
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Global conditions: R_{SRA} = 120kΩ, V_{TVL} = 1V, V_{TVT} = 0.5V, Typical values are at V_{HP} - V_{HN} = 9V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS / POWER SUPPLY (V_{CC}, V_{RAW}, HP, HN)						
Supply Voltage	V_{HP} - V_{HN}	DC input voltage, excluding superimposed HBS data signals	9		24	V
	V_{RAWI}	External voltage applied to V_{RAW}	4.6		24	
V_{RAW} Output Voltage	V_{RAWO}	V_{HP} - V_{HN} = 9V, I_{RAW} = 0mA	7.4	7.7		V
		V_{HP} - V_{HN} = 9V, I_{RAW} = 200mA	6.9	7.3		
V_{CC} Output Voltage	V_{CC}	I_{LOAD} = 70mA, V_{RAW} ≥ 6V	4.5	5.0	5.5	V
Supply Current	I_{HP}, I_{HN}	V_{RST} = V_{CC}, I_{CC} = 0mA, V_{HP} - V_{HN} = 9V		3	5	mA
	I_{RAW}	V_{RST} = V_{CC}, HP = CAPP = V_{RAW}, HN = CAPN = GND		2.5	4.0	
		HP = CAPP = V_{RAW}, V_{RST} = HN = CAPN = GND, DIN at 57.6kbps, R_{LOAD} = 100Ω		25		
Maximum V_{CC} Load Current	I_{VCCMAX}	V_{HP} - V_{HN} ≥ 9V, including I_{RAW}			70	mA
Maximum V_{RAW} Load Current	$I_{VRAWMAX}$	V_{HP} - V_{HN} ≥ 9V, excluding superimposed HBS data signals			200	mA
DC CHARACTERISTICS / TRANSMIT CHANNEL (AIO, BIO, TERM)						
Output Voltage High	V_{TOH}	AIO, BIO to GND, V_{RAW} ≥ 4.6V, I_{LOAD} = 45mA to GND	V_{CC} - 0.6			V
Output Voltage Low	V_{TOL}	AIO, BIO to GND, V_{RAW} ≥ 4.6V, I_{LOAD} = 45mA to V_{CC}			0.6	V
Termination Switch On Resistance	R_{TERM}	TERM to AIO	2.5	5	10	Ω
AIO, BIO Transmit Input Resistance	R_{IN}	Input resistance of AIO and BIO when they are unconnected, DIN = V_{CC}	7	10	13	kΩ
Bias Voltage Ratio Matching	V_{AIO} / V_{BIO}	AIO, BIO unconnected	-1		+1	%
DC CHARACTERISTICS / RECEIVE CHANNEL (TVL, TVT)						
Receive Threshold Leading Edge	V_{LEAD}	V_{TVL} = 1.0V, $\overline{HPEN}$ = V_{CC}	0.85	1	1.15	V
Receive Threshold Trailing Edge	V_{TRAIL}	V_{TVT} = 0.5V, $\overline{HPEN}$ = V_{CC}	0.35	0.5	0.65	V
TVL and TVT Input Leakage Current	I_{THLEAK}	V_{TVT} = V_{TVL} = 2.5V	-1		+1	µA
DC CHARACTERISTICS / DIGITAL I/O						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current	I_{LEAK}		-1		+1	µA
Open-Drain Logic-Low	V_{OL}	I_{SINK} = 2mA			0.3	V
Open-Drain Leakage	I_{ODL}	V_{OUT} = 5V, output not asserted			1	µA

Electrical Characteristics (continued)

(Global conditions: R_{SRA} = 120kΩ, V_{TVL} = 1V, V_{TVT} = 0.5V, Typical values are at V_{HP} - V_{HN} = 9V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS / TRANSMIT CHANNEL (Note 3)						
Output Rise Time Leading Edge	t_{RLD}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.8	1.4	2.0	µs
Output Fall Time Leading Edge	t_{FLD}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.8	1.4	2.0	µs
Output Rise Time Trailing Edge	t_{RTR}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.8	1.4	2.0	µs
Output Fall Time Trailing Edge	t_{FTR}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.8	1.4	2.0	µs
Transmit Propagation Delay	t_{TPROP}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*			1.2	µs
Transmission Output Symmetry	t_{SYM}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	-0.4	0	+0.4	µs
Termination Switching Delay	t_{TERM}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 2*			0.5	µs
Termination On-Time	t_{TRMON}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 2*	19	34	63	µs
AC CHARACTERISTICS / RECEIVE CHANNEL (Note 3)						
Receive Propagation Delay	t_{RPROP}	$\overline{HPEN}$ = V_{CC}, *Figure 3*			1	µs
Receiver High Pass Filter Time Constant	t_{HP}	$\overline{HPEN}$ = GND		1200		µs
PROTECTION						
ESD Protection AIO, BIO, TERM, HP, HN to GND (Note 2)		IEC 61000-4-2 air-gap discharge		±15		kV
		IEC 61000-4-2 contact discharge		±8		
ESD Protection	V_{ESD}	Human Body Model		±4		kV
Thermal Shutdown	T_{SHDN}	Junction temperature rising		+150		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYST}			20		°C

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Both air-gap and contact ESD are tested with no power connected to HP, HN, V_{RAW}, or V_{CC}.

Note 3: Not production tested. Guaranteed by design.

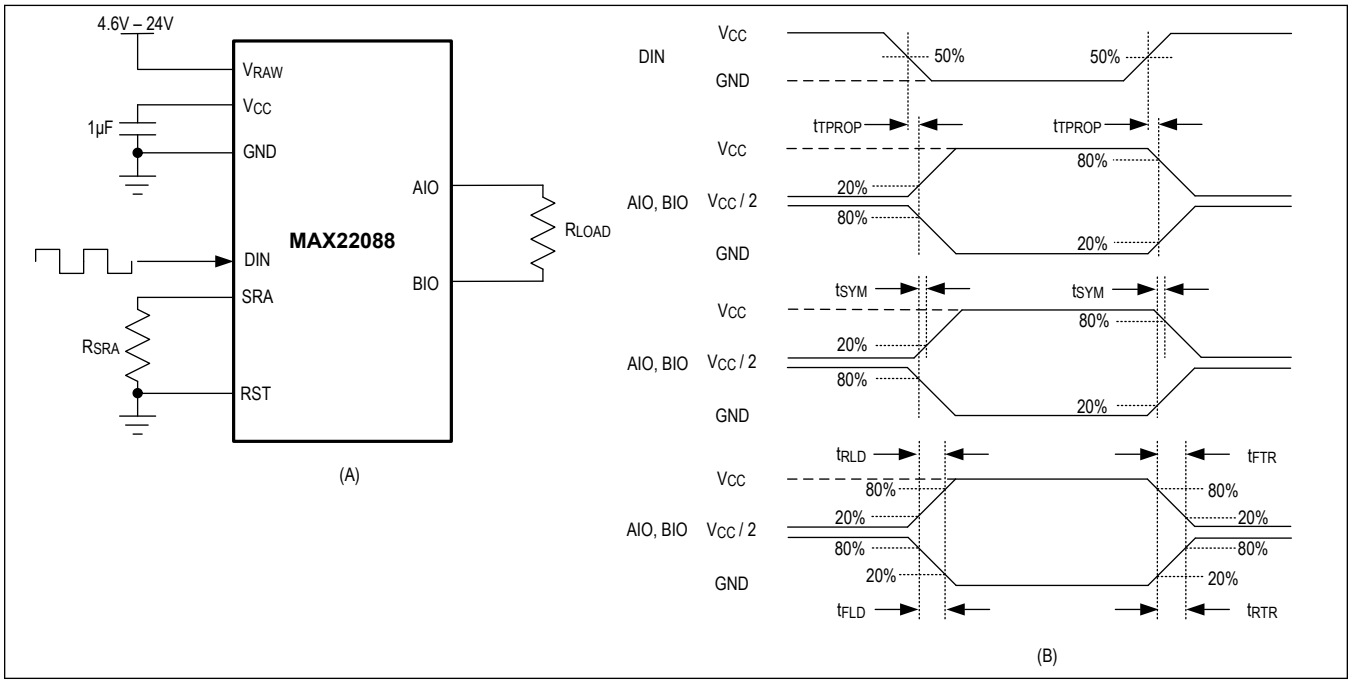


Figure 1. Transmit Channel Timing Diagram

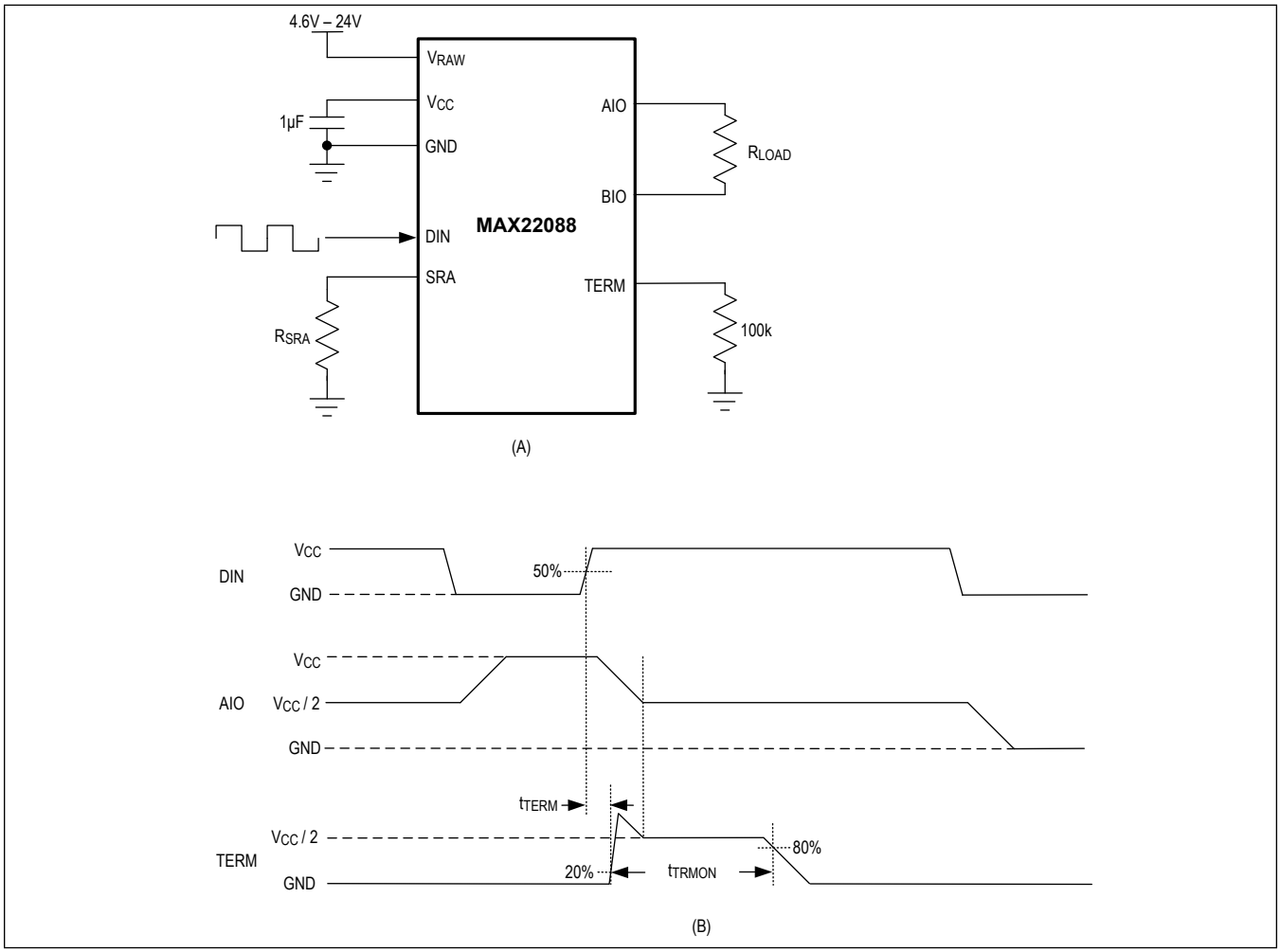


Figure 2. Transmission Switch Delay and Termination On-Time

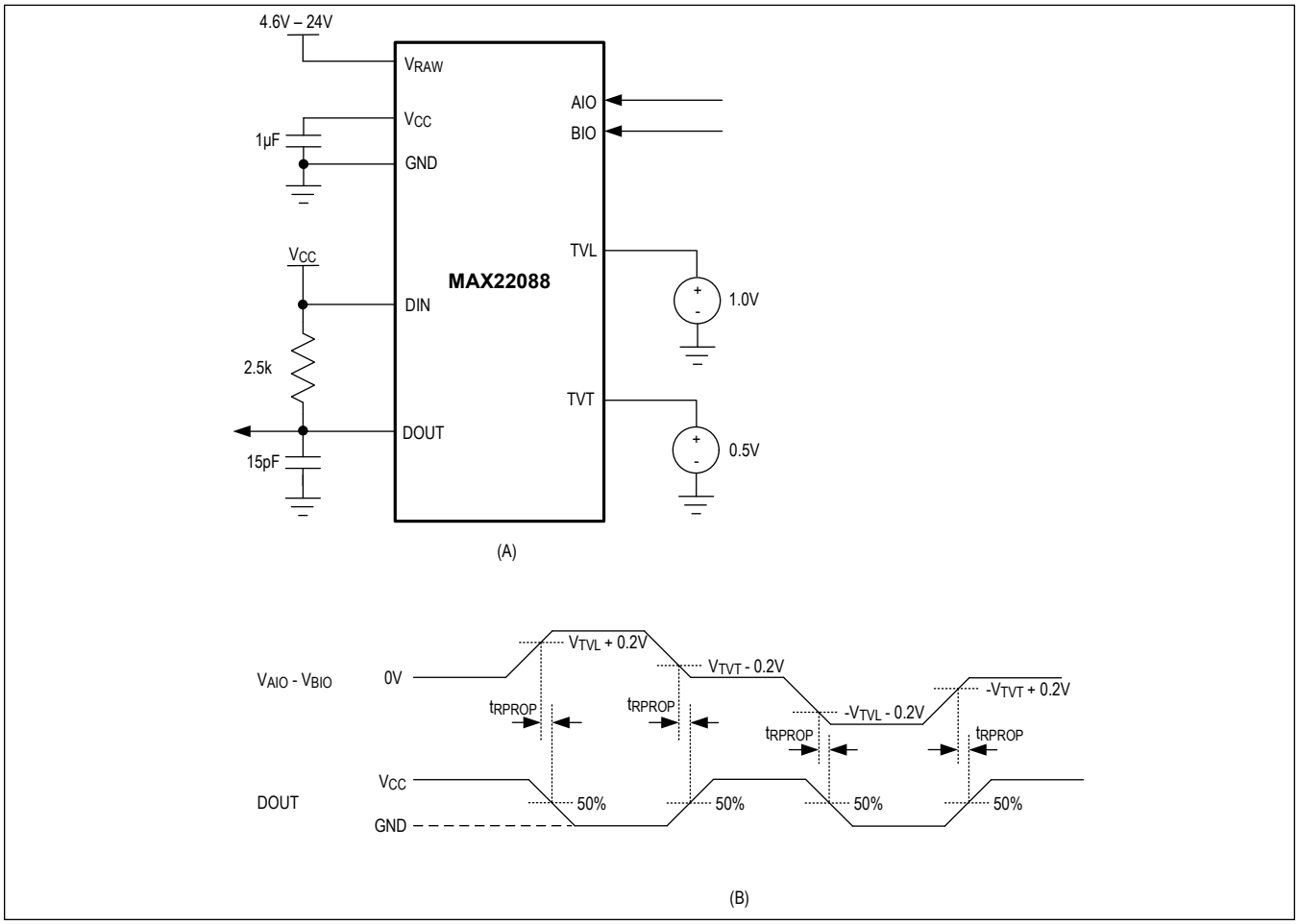
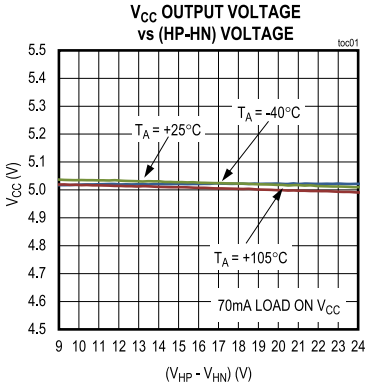
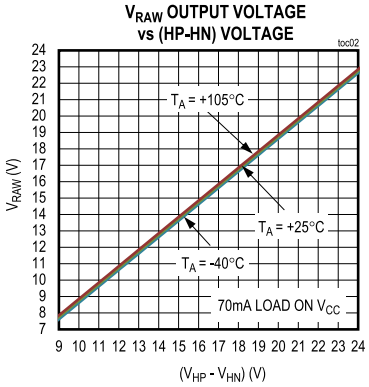


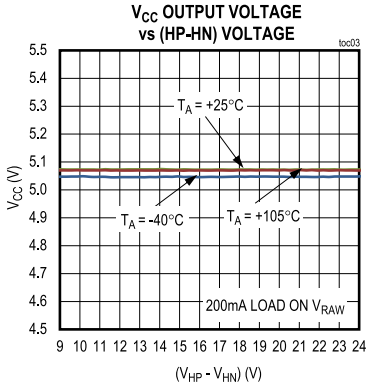
Figure 3. Receive Propagation Delay

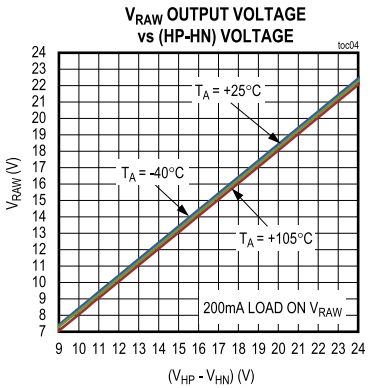
Typical Operating Characteristics

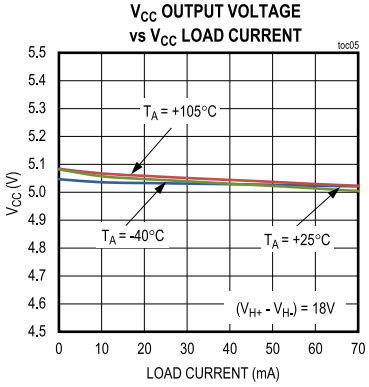
(T_A = +25°C, unless otherwise noted.)

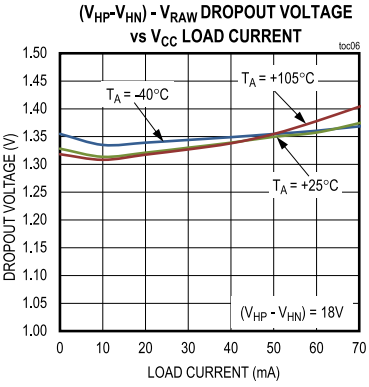


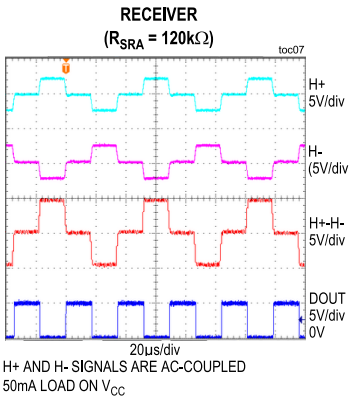


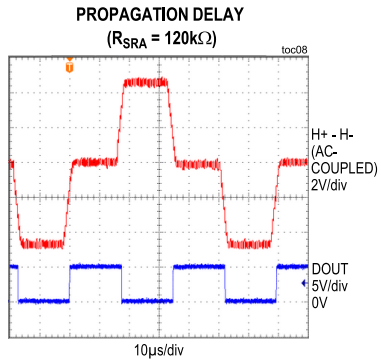


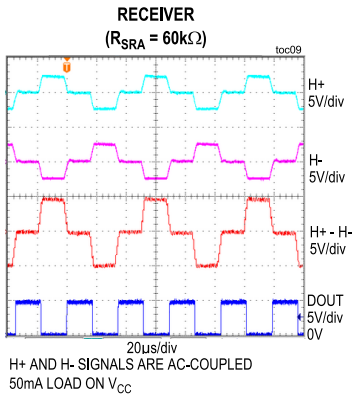








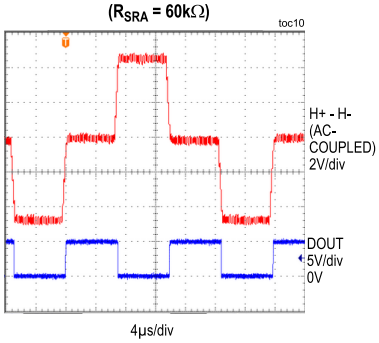




Typical Operating Characteristics (continued)

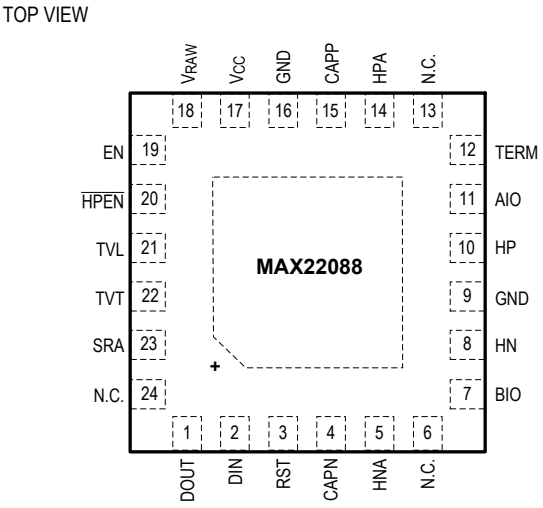
(T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY
(R_{SRA} = 60kΩ)



Pin Configuration

MAX22088



TQFN
4mm x 4mm

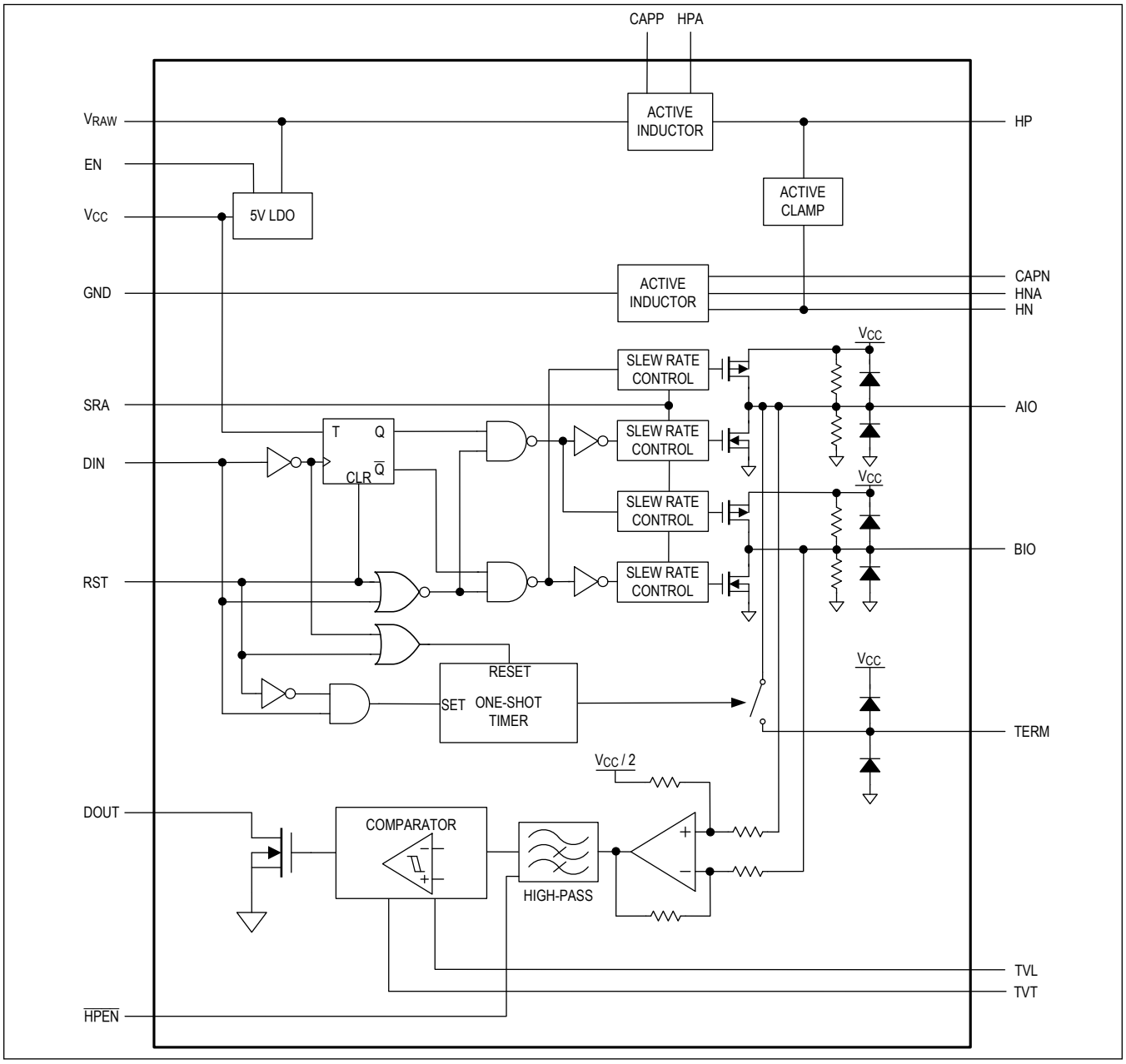
Pin Description

PIN	NAME	FUNCTION
POWER		
4	CAPN	Active Inductor Bypass Capacitor Connection. For 57.6kbps operation, connect a 100nF ceramic capacitor between CAPN and HNA. Connect CAPN to HNA when the Active Inductor is not used. See the *Active Inductor* section for more information.
5	HNA	Active Inductor Bypass Capacitor Connection. For 57.6kbps operation, connect a 100nF ceramic capacitor between CAPN and HNA. Connect HNA to CAPN when the Active Inductor is not used.
14	HPA	Active Inductor Bypass Capacitor Connection. Connect a 1µF ceramic capacitor in series with a 180kΩ resistor between CAPP and HPA. In parallel, connect an additional 100nF ceramic capacitor between CAPP and HPA for 57.6kbps operation. Connect HPA to CAPP when the Active Inductor is not used.
15	CAPP	Active Inductor Bypass Capacitor Connection. Connect a 1µF ceramic capacitor in series with a 180kΩ resistor between CAPP and HPA. In parallel, connect an additional 100nF ceramic capacitor between CAPP and HPA for 57.6kbps operation. Connect CAPP to HPA when the Active Inductor is not used. See the *Active Inductor* section for more information.
9, 16	GND	Ground Reference. See the *Layout Recommendations* section for more information.
17	V_{CC}	LDO Power Output. Bypass V_{CC} to GND with a 1µF (min) ceramic capacitor as close to the device as possible. V_{CC} is able to supply up to 70mA (max) of current to external loads. See the *Internal Voltage Regulator* section for more information.
18	V_{RAW}	Active Inductor Power Output. Bypass V_{RAW} to GND with a 100µF (min) capacitor to drive loads less than 70mA (max). Bypass V_{RAW} to GND with a 200µF (min) capacitor to drive loads more than 70mA (max). See the *V_{RAW} Voltage Output* section for more information.
EP	—	Exposed pad. Connect EP to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
HOME BUS		
7	BIO	Home Bus Data Input and Output. Connect BIO to Home Bus through an external 1µF capacitor in series with a 4.7Ω resistor for 57.6kbps operation. See the *Operation of MAX22088 Transceiver* section for more information.
8	HN	Power Supply Input from Home Bus. Connect HN to GND when the Active Inductor is not used. See the *Power Supply* section for more information.
10	HP	Power Supply Input from Home Bus. Connect HP to V_{RAW} when the Active Inductor is not used. See the *Power Supply* section for more information.
11	AIO	Home Bus Data Input and Output. Connect AIO to Home Bus through an external 1µF capacitor in series with a 4.7Ω resistor for 57.6kbps operation. See the *Operation of MAX22088 Transceiver* section for more information.
12	TERM	Switched Bus Termination. Connect a resistor between TERM and BIO to adjust Home Bus cable termination for better signal quality. See the *Dynamic Cable Termination* section for more information.
21	TVL	Leading Edge Data Threshold. See the *Receiver Thresholds* section for more information.
22	TVT	Trailing Edge Data Threshold. See the *Receiver Thresholds* section for more information.
LOGIC		
1	DOUT	Open-Drain Data Output. Connect a pullup resistor to the logic voltage supply.
2	DIN	Data Input
3	RST	Bus Reset Control Input. See the *RST (Reset) Functionality* section for more information.
19	EN	LDO Enable Input. Connect EN to V_{RAW} to enable the internal voltage regulator. Connect EN to GND to disable the internal voltage regulator.
20	$\overline{HPEN}$	High Pass Filter Enable Input. Connect $\overline{HPEN}$ to GND to enable the internal high pass filter on receiver input. Connect $\overline{HPEN}$ to V_{CC} to disable the internal high pass filter. Do not leave $\overline{HPEN}$ unconnected. See the *High Pass Filter* section for more information.
23	SRA	Slew Rate Adjustment Input. Connect SRA to GND through a resistor to adjust the slew rate of the AIO and BIO transmit edges. See the *Transmit Slew Rate Adjustment* section for more information.
6, 13, 24	N.C.	Not Connected

Functional Diagrams



Detailed Description

The MAX22088 Home Bus transceiver complies with the Home Bus standard, where power and data are carried on a single pair of wires. The MAX22088 operates with data rates up to, and exceeding, 200kbps for bus-powered applications. For applications where power is consumed, the MAX22088 features an integrated Active Inductor to eliminate the use of external AC-blocking inductor.

The MAX22088 can drive external system loads at 5V up to 70mA using the integrated voltage regulator. The MAX22088 also features dynamic cable termination, configurable receiver hysteresis and thresholds, and transmit driver slew rate adjustment for better signal quality and flexible design.

Power Supply

In the Home Bus standard, power and data are carried on a single pair of wires. For applications where power is sourced, the MAX22088 is powered by the system voltage supplied at V_{RAW}. In this configuration, an external AC-blocking inductor is required to superimpose the data on the Home Bus cable. Bypass the integrated Active Inductor by connecting CAPN to HNA, HN to GND, CAPP to HPA, and HP to V_{RAW}.

For applications where power is consumed, the MAX22088 is powered by the voltage carried on the Home Bus cable. In this configuration, the MAX22088 eliminates the need for an external AC-blocking inductor and uses the integrated Active Inductor to separate data from power. Power is passed from the Home Bus cable to V_{RAW} to supply the MAX22088 and drive external system loads.

V_{RAW} Voltage Output

V_{RAW} is the output of the integrated Active Inductor. The integrated Active Inductor can source up to 200mA (max) to V_{RAW} to power the external loads, minus internal load current. Bypass V_{RAW} to GND with a 100µF (min) capacitor to drive loads less than 70mA (max). Bypass V_{RAW} to GND with a 200µF (min) capacitor to drive loads more than 70mA (max). To drive larger loads, or for a regulated output, connect a DC-DC converter, or an LDO, to V_{RAW}. See the *Typical Application Circuits* section for more information.

Internal Voltage Regulator

The MAX22088 features an internal 5V linear regulator, powered by V_{RAW}, capable of driving external loads up to 70mA (max), minus internal load current. Connect EN to V_{RAW} to enable the 5V output at V_{CC}. Connect EN to GND to disable the linear regulator. Do not use V_{CC} to power external loads if an external LDO or DC-DC converter is connected at V_{RAW}. See the *Typical Application Circuits* section for more information.

Active Inductor

The MAX22088 features an integrated Active Inductor to eliminate the need for an external AC-blocking inductor in applications where power is consumed. The differential inputs, HP and HN, to the integrated Active Inductor maintain a balanced termination for the Home Bus cable. The equivalent value of the integrated Active Inductor (L_{ACT}) is set by the values of the two capacitors (C_{ACT}) connected between CAPP and HPA, and between CAPN and HNA. Use the following approximate formula to calculate the typical value of the integrated Active Inductor:

$$L_{ACT} = \frac{C_{ACT}}{6 \times 10^{-7}} \times \left(\frac{1}{10 \times \sqrt{I_{LOAD}}} - \frac{1}{3 + 25 \times I_{LOAD}}\right)$$

where L_{ACT} is in Henry, C_{ACT} is in Farad, I_{LOAD} is in Ampere (*Figure 4*).

For 57.6kbps operation, the recommended value for C_{ACT} is 100nF.

In parallel to C_{ACT}, connect a 180kΩ resistor and a 1µF ceramic capacitor in series between CAPP and HPA to provide dampening for the LC network formed by the integrated Active Indutor and the bypass capacitor on V_{RAW}. This LC network also limits the inrush current that charges the bypass capacitor on V_{RAW}.

The transient load current, in series with the output inductance, can cause fluctuations on output voltage at V_{RAW}. In a Home Bus system, the total inductance is the serial combination of the passive inductor on the power-sourcing side (host) and the integrated Active Inductor on the power-consuming side (device). Limit the load current and carefully select the C_{ACT} value to avoid excessive voltage fluctuations at V_{RAW}, as shown in *Table 1*.

Table 1. Capacitor Value and Maximum Transient Load Current

C_{ACT} (nF)	MAXIMUM TRANSIENT I_{LOAD} (mA)
100	200
200	160
300	120
400	100
500	90

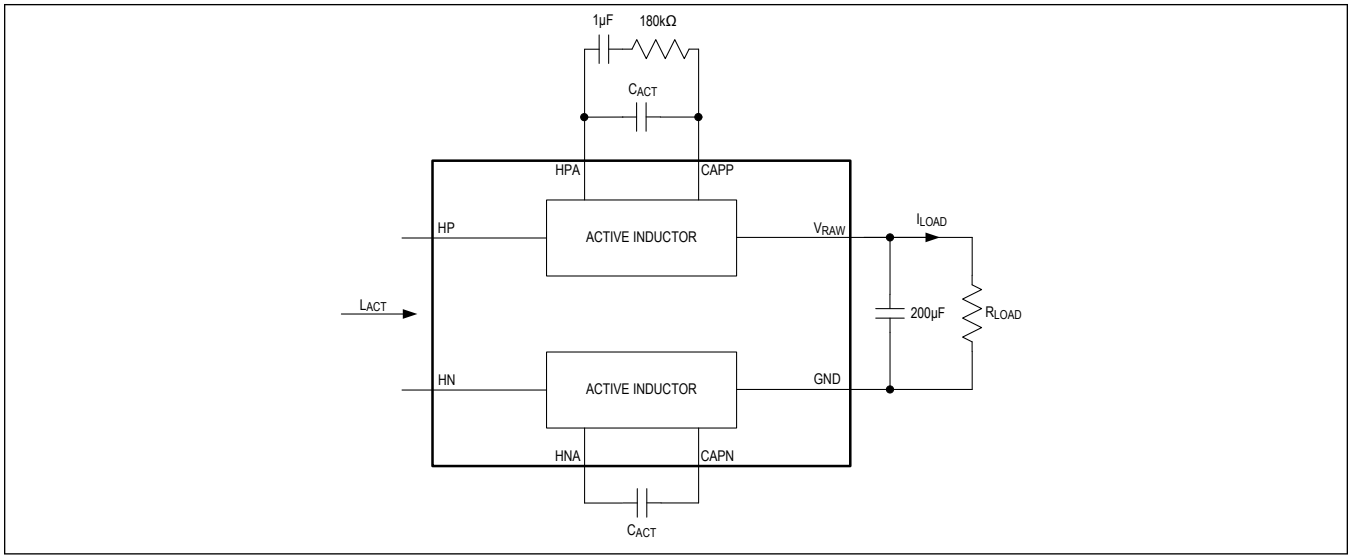


Figure 4. Integrated Active Inductor Circuit

Operation of MAX22088 Transceiver

The MAX22088 uses three pins for the logic interface: RST, DIN, and DOUT. AIO, BIO, and TERM are connected to the Home Bus network. RST is the bus reset control input. Drive RST low to enable the transmitter on AIO and BIO. Drive RST high to disable the transmitter. The MAX22088 Home Bus receiver is always enabled.

DIN is the logic input of the MAX22088. DOUT is the logic output. When DIN goes from high to low, the polarities of AIO and BIO invert. When DIN goes from low to high, AIO and BIO are set to high-impedance (*Figure 5*).

DOUT asserts low when the leading edge of V_{AIO} - V_{BIO} crosses V_{TVL} or -V_{TVL}. DOUT is high-impedance when the trailing edge of V_{AIO} - V_{BIO} crosses V_{TVT} or -V_{TVT}. See the *Receiver Threshold Adjustment* section for more information.

To improve signal quality, the MAX22088 features an internal switch that connects TERM to AIO for 34µs (typ) after the driver transitions to high-impedance. See the *Dynamic Cable Termination* section for more information.

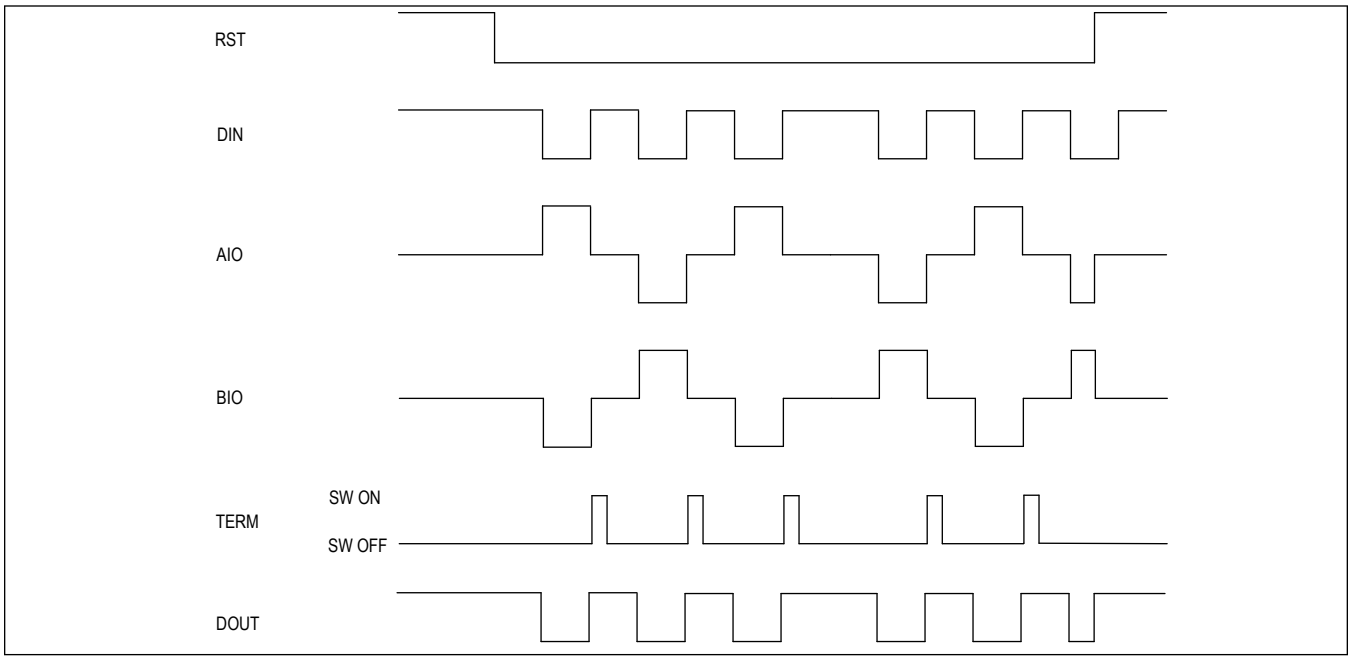


Figure 5. Operation of MAX22088 Transceiver

Dynamic Cable Termination

The MAX22088 supports Home Bus signals at data rates up to, and exceeding, 200kbps. When operating at high data rates, the mismatch between the Home Bus cable impedance and cable termination resistor can negatively affect the signal quality. The MAX22088 features dynamic cable termination to improve the signal quality with longer cables. When the driver transitions to high-impedance, an internal switch connects AIO to TERM. The external termination resistor at TERM is then connected between AIO and BIO in parallel with the static cable termination resistor. The internal switch opens after 34µs (typ), when DOUT asserts low, or when RST is driven high. The optimized value of the dynamic termination resistor depends on the application. For typical applications, the value of the dynamic termination resistor is between 50Ω and 240Ω.

Transmit Slew Rate Adjustment

Connect an external resistor, R_{SRA}, from SRA to GND to control the slew rate of the transmit signals at AIO and BIO. The transmit rise/fall time (t_{RLD}, t_{FLD}, t_{RTR}, t_{FTR}) is proportional to R_{SRA} and is calculated using the following equation:

$$t_{rise/fall} = 17pF \times R_{SRA}$$

For most applications, it is recommended to use R_{SRA} = 62kΩ resulting in 1µs (typ) output rise/fall time. Ensure that R_{SRA} is in the range from 33kΩ to 470kΩ.

Receiver Threshold Adjustment

The threshold levels for the receiving signals are set by the voltages at TVL and TVT. The voltage at TVL sets the threshold for the leading edge of the pulse on the Home Bus signal (V_{AIO} - V_{BIO}). The voltage at TVT sets the threshold for the trailing edge of the pulse. Ensure that $V_{TVL} > V_{TVT}$.

DOUT asserts low when V_{AIO} - V_{BIO} crosses V_{TVL} or -V_{TVL}. DOUT is high-impedance when V_{AIO} - V_{BIO} crosses V_{TVT} or -V_{TVT} (*Figure 6*). Connect a pullup resistor from DOUT to a logic voltage supply.

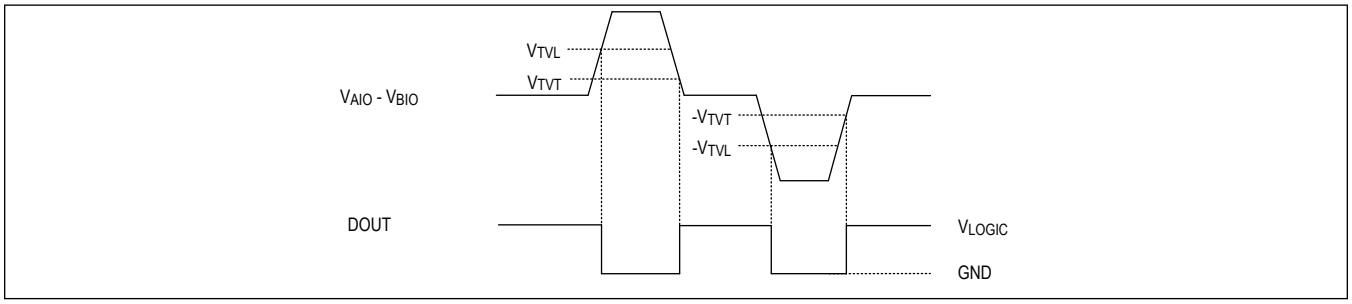


Figure 6. Receiver Thresholds

RST (Reset) Functionality

The MAX22088 features a bus reset control input. Drive RST low to enable the transmitter. Drive RST high to disable the transmitter. RST also controls the internal switch used for dynamic cable termination. Ensure that RST remains low for at least 34µs (typ) after the internal switch is closed when the driver transitions to high-impedance. The internal switch opens when RST is driven high.

High-Pass Filter

The MAX22088 features an internal high pass filter on the receiver to filter out the low frequency voltage fluctuations at AIO and BIO. Connect $\overline{HPEN}$ to GND to enable the internal high-pass filter on the receiver input. Connect $\overline{HPEN}$ to V_{CC} to disable the internal high pass filter. Ensure that $\overline{HPEN}$ is always connected.

Applications Information

Surge Protection

External components are required to protect the MAX22088 Home Bus pins (HP, HN, AIO, BIO, and TERM) from high-voltage transient events. The *Typical Application Circuits* show a typical protection scheme.

HP and HN Surge Protection

HP and HN must be protected with external components from surge transients. Connect a TVS diode between the HP and HN lines. Ensure that the maximum standoff voltage of the TVS diode does not exceed 24V (max). Connect a 1Ω current limiting resistor between the TVS diode and HP to force the current sharing between an internal Active Clamp and the external TVS diode (*Figure 7*).

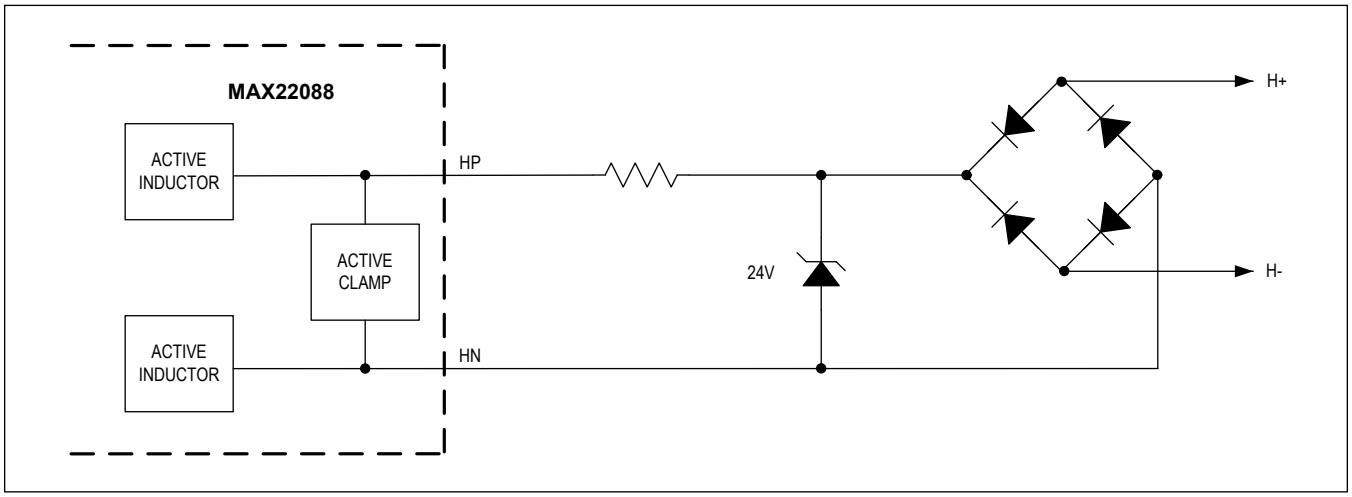


Figure 7. HP and HN Surge Protection

AIO, BIO, and TERM Surge Protection

AIO, BIO, and TERM must be protected with external components from surge transients. Connect TVS diodes with a 5.8V (max) standoff voltage from AIO and BIO to GND. Connect a 4.7Ω serial resistor between each TVS diode and AIO/BIO to limit the current flows into AIO/BIO during the surge transients. Depending on the surge transients polarities, the residual current after the 4.7Ω resistor flows from AIO/BIO through the internal ESD clamping diodes to V_{CC} or GND. Connect a 1µF (min) ceramic capacitor as close to V_{CC} as possible, and a 10µF (min) bulk capacitor on the V_{CC} bus to absorb this current and limit the voltage overshoot on V_{CC} during surge transients.

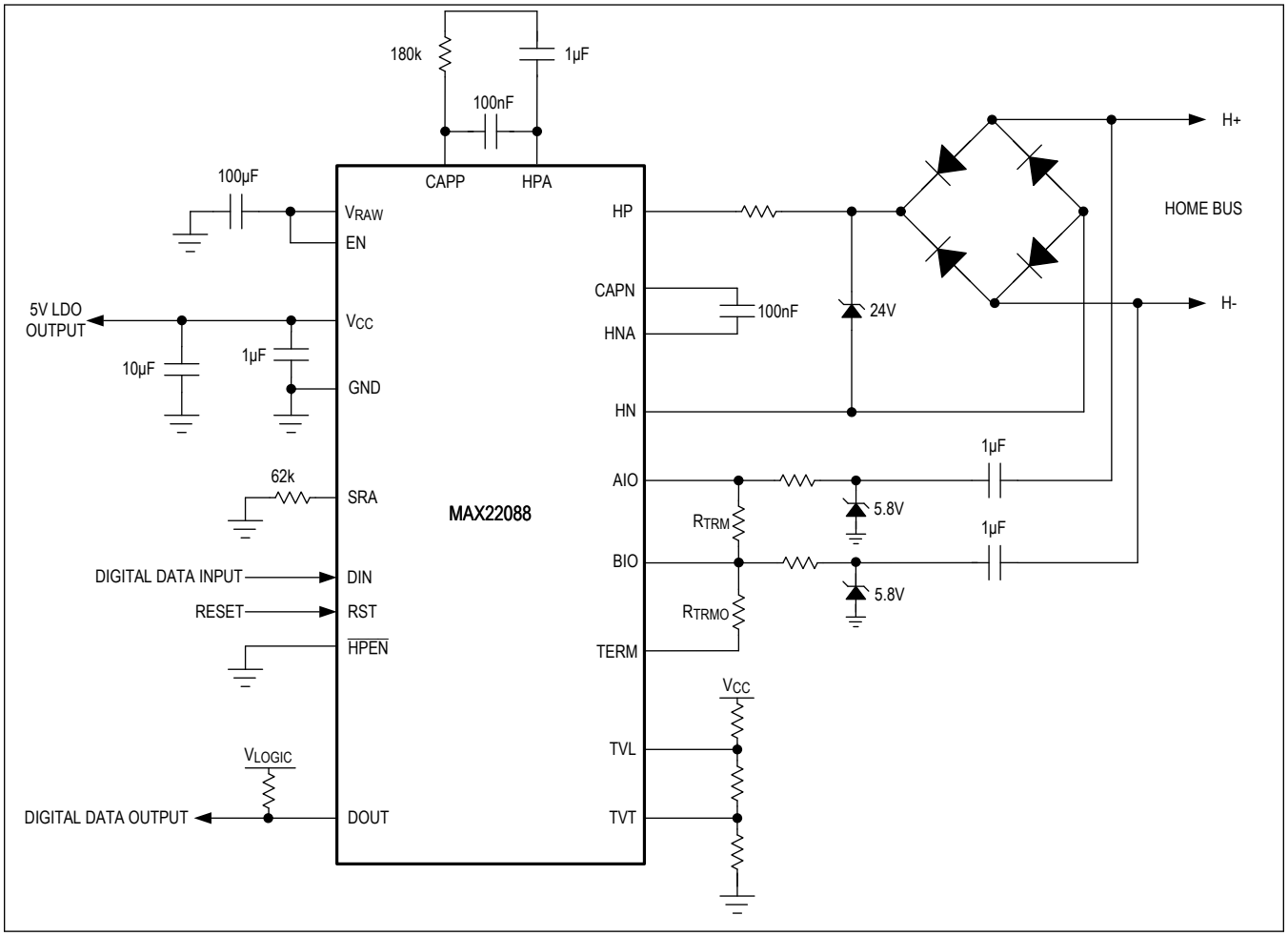
Layout Recommendations

Although impedance matching is not required on H+ and H- lines, route them together as much as possible. To reduce the parasitic capacitance on signal lines, do not route H+ and H- lines, or their connected components, over the ground planes.

To ensure proper protection, connect the ground return of the protection diodes directly to the ground plane. Use a star configuration to connect all grounds together as close to the GND (pin 9) as possible. Place the external protection TVS diodes and the diode bridge as close to the Home Bus connector as possible.

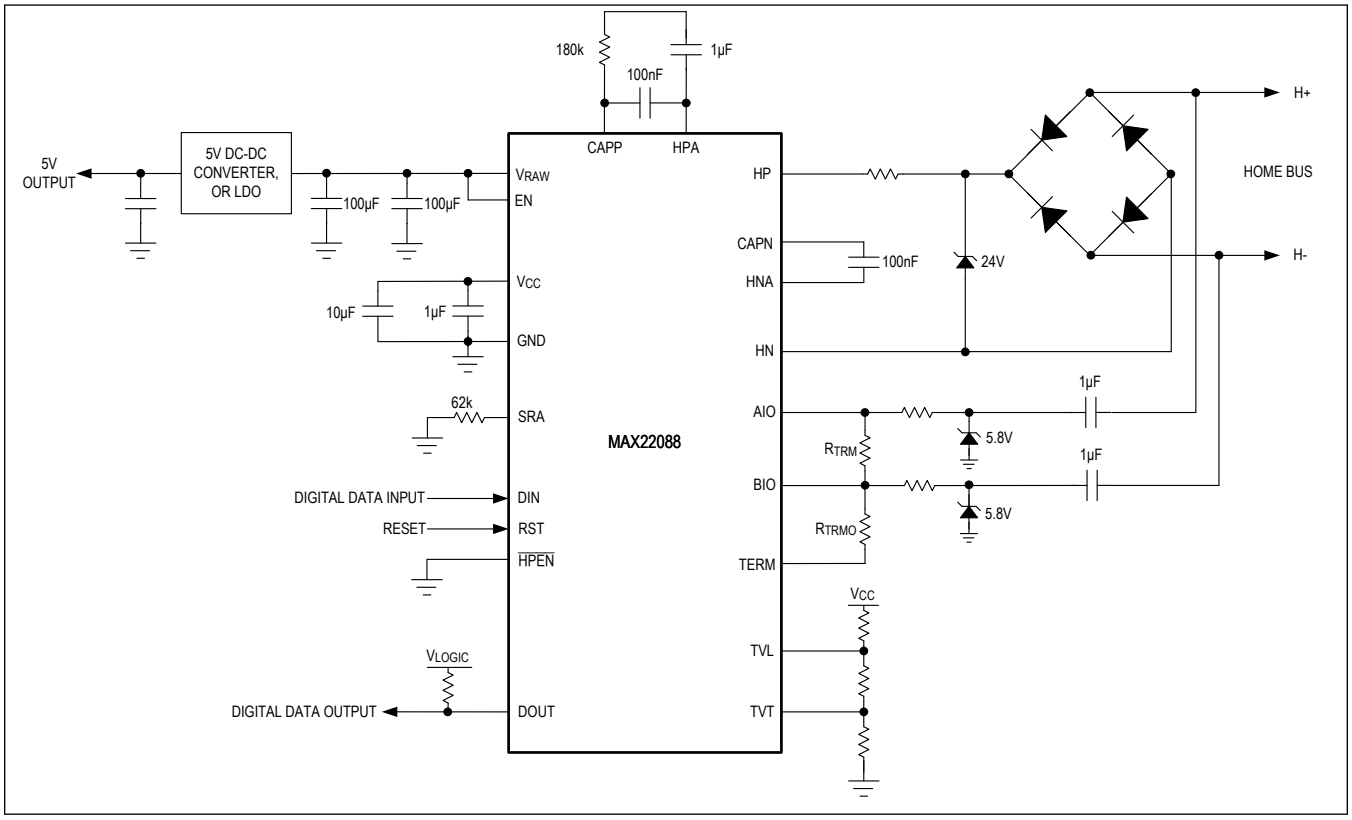
Typical Application Circuits

Low-Power Application with Internal LDO Output (57.6kbps)



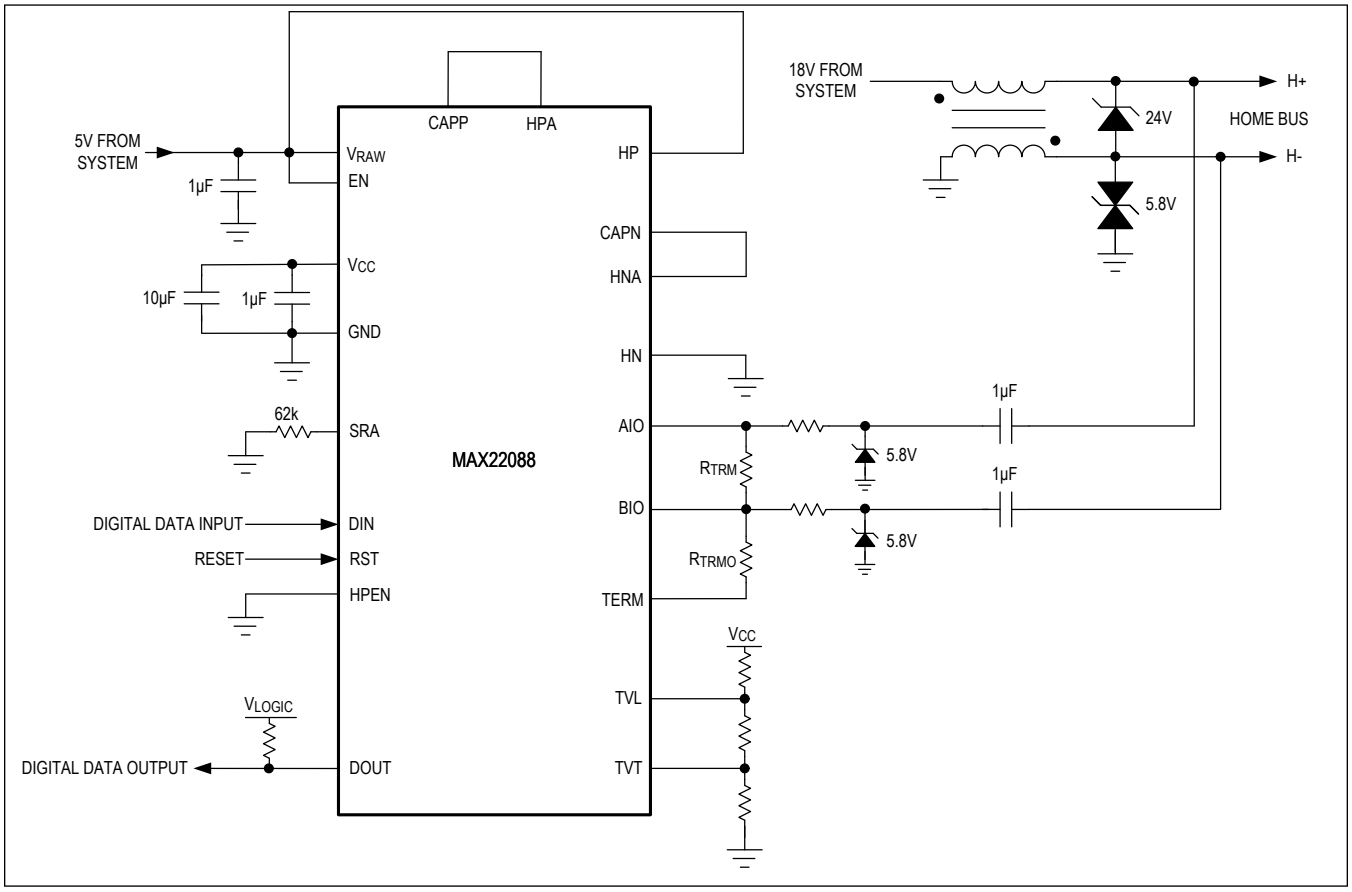
Typical Application Circuits (continued)

Medium-Power Application with External DC-DC Converter (57.6kbps)



Typical Application Circuits (continued)

Application Where Power is Sourced from Unit (57.6kbps)



Ordering Information

PART NUMBER	TEMPERATURE RANGE
MAX22088GTG+	-40°C to +105°C
MAX22088GTG+T	-40°C to +105°C

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial release	—
1	6/20	Updated Homebus to Home Bus in title and all sections	1–21
2	2/21	Updated the *Electrical Characteristics* section	3

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