*Click **here** for production status of specific part numbers.*

# MAX20342

# USB Type-C Charger Detector with Integrated OVP

## General Description

The MAX20342 is a USB Type-C® charger detector that is also capable of detecting chargers compliant with the USB Battery Charging Specification Revision 1.2. The USB Type-C charger detection circuitry functions as a UFP or DRP depending on factory configuration.

The device implements USB Type-C detection logic and enables systems to support charging based on USB Type-C ports. The device also includes charger detection capability for BC1.2 compatible chargers and detects USB standard downstream ports (SDPs), USB charging downstream ports (CDPs), dedicated charger ports (DCPs), and other proprietary chargers. GPIO outputs allow the MAX20342 to control an external lithium-ion (Li+) battery charger based on charger detection results.

The MAX20342 integrates a resistance detection block that can be used to automatically configure factory configuration states based upon attached resistors. Additionally, the resistance measurement can be configured to detect the presence of moisture in the USB Type-C connector.

The MAX20342 also features an integrated low on-resistance, low-capacitance double-pole double-throw (DPDT) USB switch that can pass Hi-Speed USB, full-speed USB, low-speed USB, and UART signals. The switch position can be automatically configured by the USB detection logic or manually controlled.

The MAX20342 features high-ESD protection up to ±15kV human-body model (HBM) on CC1, CC2, SBU1, and SBU2 pins. The CDP and CDN pins are protected against ESD up to ±6kV. The MAX20342 is specified for ±15kV Air-Gap and ±8kV Contact Discharge IEC 61000-4-2 on the CC1, CC2, SBU1, and SBU2 pins. The MAX20342 is available in a 24-bump, 0.4mm pitch, 2.62mm x 2.02mm wafer-level package (WLP) and operates over the -40ºC to +85ºC extended temperature range.

## Applications

- DSCs and Camcorders
- Tablets
- Smartphones
- e-Readers

*USB Type-C® is a registered trademark of USB Implementers Forum.*

*Apple is a registered trademark of Apple Inc.*

*Samsung is a registered trademark of Samsung Electronics Co., Ltd*

## Benefits and Features

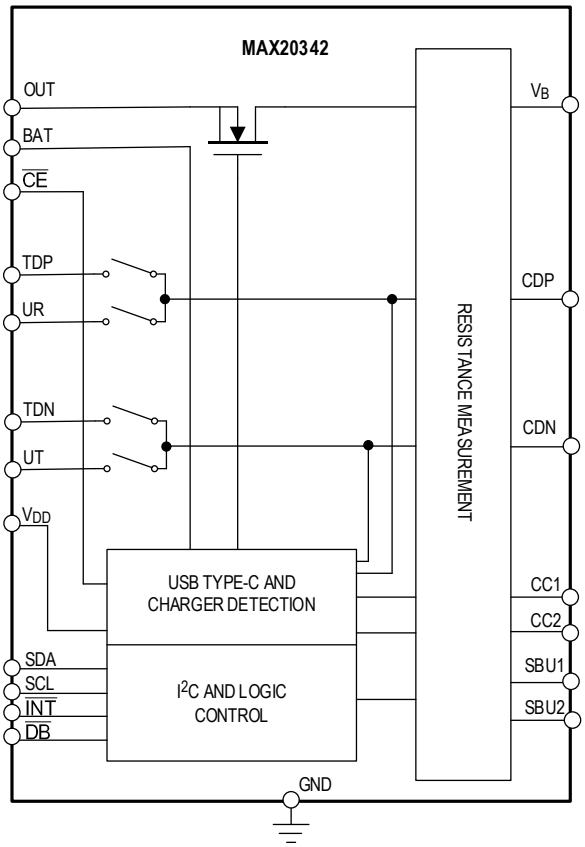
- Low Power Consumption
  - Battery Standby Current 17µA (typ)
  - Battery Shutdown Current 2.5µA (typ)
- Delivers USB Compliance and Flexibility
  - Compliant with USB Type-C Specification Revision 1.3
  - Supports USB Battery Charger Specification Revision 1.2
  - Detects Proprietary Chargers such as Apple® and Samsung®
- Simplifies Complex System Designs
  - Integrated Overvoltage Protection
  - Negative Swing Audio Capable Hi-Speed USB/UART Switches
  - Automatic Switch and Charger Interface Control
  - Full Control through I²C Interface
  - Interrupts for Device Status Changes
- Improves Quality and Reliability
  - Automatic Factory Mode Configuration
  - USB Type-C Port Moisture Detection
  - Low-Corrosion DRP Mode
- Robust Protection
  - $V_B$ Connection Withstands up to +30V
  - $V_B$ Surge Protection up to ±120V
  - ±15kV HBM ESD Protection on CC1, CC2, SBU1 and SBU2 Pins
  - ±6kV HBM ESD Protection on CDP and CDN Pins
  - ±15kV Air-Gap IEC 61000-4-2 on CC1, CC2, SBU1, and SBU2 Pins
  - ±8kV Contact Discharge IEC 61000-4-2 on CC1, CC2, SBU1, and SBU2 Pins
- Saves Board Space
  - 2.62mm x 2.02mm WLP Package

***Ordering Information** appears at end of data sheet.*

*19-100858; Rev 3; 9/21*

maxim integrated™

## Simplified Block Diagram



## Absolute Maximum Ratings

$V_B$ to GND ..... -0.3V to +30V

$V_B$ to OUT ..... -0.3V to +26V

OUT to GND ..... -0.3V to +7.5V

BAT to GND ..... -0.3V to +6.0V

$\overline{INT}$, SDA, SCL, $\overline{CE}$, $\overline{DB}$ to GND ..... -0.3V to +6.0V

CDN, CDP to GND ..... -0.3V to +6.0V

CDN, CDP to GND (AudioCPEn enabled, switches off) ... -3.0V to +6.0V

SBU1, SBU2 to GND ..... -0.3V to +6.0V

CC1, CC2 to GND (Note 1) ..... -0.3V to +6.0V

TDN, TDP to GND ..... -0.3V to +6.0V

UT, UR to GND ..... -0.3V to +6.0V

$V_{DD}$ to GND ..... -0.3V to +2.2V

Continuous Power Dissipation (Multilayer Board) ($T_A$ = +70°C, derate 18.85mW/°C above +70°C) ..... 1.508W

Continuous Current into $V_B$, OUT ..... 2000mA

Current into $V_B$, OUT ($T_A$ = +70°C, 1500 hours) ..... 3000mA

Continuous Current into CC1, CC2 ..... 600mA

Continuous Current into any other terminal ..... 100mA

Operating Temperature Range ..... -40°C to +85°C

Junction Temperature Range ..... -40°C to +150°C

Storage Temperature Range ..... -40°C to +150°C

Soldering Temperature (reflow) ..... +260°C

**Note 1:** CC1 and CC2 pins can withstand a short to +20V with a series 10kΩ resistor (sinking 2mA). Continuous Current is guaranteed for 100,000 hours at $T_A$ = 120°C. Throughout the data sheet, Current refers to the aforementioned condition of Continuous Current.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 24-WLP

| | |
|---|---|
| Package Code | W242A2+1 |
| Outline Number | *21-100430* |
| Land Pattern Number | Refer to *Application Note 1891* |
| **THERMAL RESISTANCE, FOUR LAYER BOARD** | |
| Junction-to-Ambient ($\theta_{JA}$) | 53.04°C/W |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

($V_{BAT}$ = 3.6V , $V_B$ = 5V, $C_{VDD}$ = 1µF, $C_{VB}$ = 1µF, $C_{OUT}$ = 1µF, $C_{BAT}$ = 1µF, limits are production tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. )

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GENERAL ELECTRICAL CHARACTERISTICS** | | | | | | |
| Supply Voltage Range Output | VBAT | | 2.75 | | 5.5 | V |
| Supply Voltage Range Input | VB | | 4.4 | | 28.0 | V |
| Internal VB Regulator Voltage | VB_REG | | | 3.75 | | V |
| Internal VCCINT Switchover Rising Threshold | VCCINT_SWOVER_THR | VCCINTOnBAT = '0', measured as (VB_REG - VBAT) rising, VCCINT = VB_REG above this threshold | | 180 | | mV |
| Internal VCCINT Switchover Falling Threshold | VCCINT_SWOVER_THF | VCCINTOnBAT = '0', measured as (VB_REG - VBAT) falling, VCCINT = VBAT below this threshold | | 50 | | mV |
| Internal VCCINT POR Rising Threshold | VCCINT_POR | Measured on internal VCCINT rising | | 1.81 | | V |
| Internal VCCINT POR Threshold Hysteresis | VCCINT_POR_HYS | Measured on internal VCCINT | | 150 | | mV |
| VDD Output Voltage | VDD | IDD = 20mA | 1.7 | 1.8 | 1.9 | V |
| VDD Undervoltage Lockout Rising Threshold | VDD_UVLO | VDD rising | | 1.62 | | V |
| VDD Undervoltage Lockout Threshold Hysteresis | VDD_UVLO_HYS | | | 100 | | mV |
| BAT Shutdown Quiescent Current | IBAT_SHDN | ShdnMode = '1', VBAT = 3.6V | | 2.5 | 4.2 | µA |
| BAT Low-Power UFP Quiescent Current | IBAT_LP_UFP | LPUFP = '1', moisture detection enabled, VBAT = 3.6V, VB = 0.0V | | 16.4 | 27.0 | µA |
| BAT Low-Power Low-Corrosion DRP Quiescent Current | IBAT_LP_DRPLC | LPDRP = '1', moisture detection enabled, DRP toggling state, VBAT = 3.6V, VB = 0.0V | | 16.7 | 28.0 | µA |
| BAT UFP Quiescent Current | IBAT_UFP | Moisture detection enabled, UFP state, VBAT = 3.6V, VB = 0.0V | | 148.9 | | µA |
| BAT DFP Quiescent Current | IBAT_DFP | Moisture detection enabled, DFP state, VBAT = 3.6V, VB = 0.0V | | 181.8 | | µA |
| BAT DRP Quiescent Current | IBAT_DRP | Moisture detection enabled, DRP toggling state, VBAT = 3.6V, VB = 0.0V | | 166.3 | | µA |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| BAT Quiescent Current with VB Present | IBAT_VB | VCCINTOnBAT = '0', Attached Sink state, VBAT = 4.2V, VB = 5.0V | | 3.2 | | µA |
| | | VCCINTOnBAT = '1', Attached Sink state, VBAT = 4.2V, VB = 5.0V | | 292.6 | | |
| BAT Undervoltage Lockout Rising Threshold | VBAT_UVLO | VBAT rising | 2.73 | 2.80 | 2.85 | V |
| BAT Undervoltage Lockout Threshold Hysteresis | VBAT_UVLO_HYS | | | 100 | | mV |
| BAT Overvoltage Lockout Rising Threshold | VBAT_OVLO | VBAT rising | 5.20 | 5.35 | 5.50 | V |
| BAT Overvoltage Lockout Threshold Hysteresis | VBAT_OVLO_HYS | | | 200 | | mV |
| Shutdown/Low-Power UFP CC1 and CC2 Pulldown Resistor | RLP_UFP_PD | | | 40 | | kΩ |
| Shutdown/Low-Power UFP CC1 and CC2 Detection Rising Threshold | VLP_UFP_THR | CC1/CC2 rising | | 0.49 | | V |
| Shutdown/Low-Power UFP CC1 and CC2 Detection Falling Threshold | VLP_UFP_THF | CC1/CC2 falling | | 0.45 | | V |
| Low-Power Low-Corrosion CC1 and CC2 Detection Driving Resistor | RLP_DRP_DET | | | 400 | | kΩ |
| Low-Power Low-Corrosion DRP CC1 and CC2 Detection Rising Threshold | VLP_DRPLC_THR | CC1/CC2 rising | | 1.15 | | V |
| Low-Power Low-Corrosion DRP CC1 and CC2 Detection Falling Threshold | VLP_DRPLC_THF | CC1/CC2 falling | | 0.68 | | V |
| Shutdown CC1 and CC2 Detection Debounce Time | tSHDN_CCDEB | | | 85 | | µs |
| Low-Power UFP/Low Corrosion DRP CC1 | tLP_CCDEB | | | 1 | | ms |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| and CC2 Detection Debounce Time | | | | | | |
| Thermal Shutdown Rising Threshold | TSHDN | TJ rising | | 165 | | °C |
| Thermal Shutdown Threshold Hysteresis | TSHDN_HYS | | | 15 | | °C |
| $V_B$ OVERVOLTAGE PROTECTOR | | | | | | |
| VB Detect Threshold Rising Threshold | VBDET | VB rising | 4.19 | 4.30 | 4.40 | V |
| VB Detect Threshold Hysteresis | VBDET_HYS | | | 400 | | mV |
| VB Clamp Voltage | VB_CLAMP | IVB = 10mA | | 35 | | V |
| VB Quiescent Current | IVB | | | 360 | | µA |
| VB to OUT On-Resistance | RON_VB_OUT | VB = 5.0V, IOUT = 100mA, TA = +25ºC | | 47 | 60 | mΩ |
| VB Overvoltage Lockout Rising Threshold | VB_OVLO | VB rising | 5.790 | 5.852 | 5.915 | V |
| VB Overvoltage Lockout Threshold Hysteresis | VB_OVLO_HYS | | | 25 | | mV |
| VB Detect Debounce Time | tVBDET_DEB | | | 10 | | ms |
| VB Fault Recovering Debounce Time | tVBFLT_DEB | Applies to overvoltage event | | 10 | | ms |
| VB Soft-Start Time | tVB_SS | Measured from VOUT = 10% x VB to VOUT = 90% x VB, COUT = 1000µF | | 15 | | ms |
| VB-OUT Switch OK Time | tVB_OUT_SWT_OK | From soft-start end to VB_OUT switch interrupt OK | | 5 | | ms |
| VB Overvoltage Lockout Turn-Off Time | tVB_OVLO_OFF | From VB > VB_OVLO to VOUT stop rising, ROUT = 100Ω | | 100 | | ns |
| **DFP MODE** | | | | | | |
| OUT Connected Current Limit Source | IOUT_CUR_LIMIT | | | | 2 | A |
| OUT Connected Voltage Source | VOUT_LVL | | | | 5.5 | V |
| **USB TYPE-C** | | | | | | |
| **USB TYPE-C/BC1.2 - PROPRIETARY CHARGER DETECTION** | | | | | | |
| BC1.2 State Timeout | tTMO | | 180 | 200 | 220 | ms |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Contact Detect Timeout | tDCDtmo | DCDCpl = 0b0 | 1800 | 2000 | 2200 | ms |
| Proprietary Charger Debounce | tPRDeb | | 5 | 7.5 | 10 | ms |
| Primary to Secondary Timer | tPDSDWait | | 27 | 35 | 39 | ms |
| Charger Detection Debounce | tCDDeb | | 45 | 50 | 55 | ms |
| VB64 Threshold | VB64 | CDP and CDN pins. Threshold in percent of VB voltage 3.8V < VB < 5.8V | 57 | 64 | 71 | % |
| VB64 Hysteresis | VB64_H | | | 0.015 | | V |
| VB47 Threshold | VB47 | CDP and CDN pins. Threshold in percent of VB voltage 3.8V < VB < 5.8V | 43.3 | 47 | 51.7 | % |
| VB47 Hysteresis | VB47_H | | | 0.015 | | V |
| VB31 Threshold | VB31 | CDP and CDN pins. Threshold in percent of VB voltage 3.8V < VB < 5.8V | 26 | 31 | 36 | % |
| VB31 Hysteresis | VB31_H | | | 0.015 | | V |
| IWEAK Current | IWEAK | | 0.01 | 0.1 | 0.5 | µA |
| RDM_DWN Resistor | RDM_DWN | | 14.25 | 20 | 24.8 | kΩ |
| IDP_SRC Current | IDP_SRC/IDCD | 0V to 2.5V | 7 | 10 | 13 | µA |
| IDM_SINK Current | IDM_SINK/IDATSINK | 0.15V to 3.6V | 50 | 80 | 110 | µA |
| VLGC Threshold | VLGC | | 1.62 | 1.7 | 1.9 | V |
| VLGC Hysteresis | VLGC_H | | | 0.015 | | V |
| VDAT_REF Threshold | VDAT_REF | | 0.25 | 0.32 | 0.4 | V |
| VDAT_REF Hysteresis | VDAT_REF_H | | | 0.015 | | V |
| VD33 Voltage | VDPDM_3P3VSR/VSRC33 | With IDP_SRC = 0 to 200µA | 2.6 | 3.0 | 3.4 | V |
| VSRC33ILIM Current Limit | ILIMVSRC33 | VCDP/VCDN = 1.6V | | 1.5 | 3 | mA |
| VDN_SRC Voltage | VDN_SRC/VSRC06 | 0 to 200µA | 0.5 | 0.6 | 0.7 | V |
| VDP_SRC Voltage | VDP_SRC/VSRC06 | 0 to 200µA | 0.5 | 0.6 | 0.7 | V |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DP/DM Pulldown Resistor | RUSB | | 3 | 6.1 | 12 | MΩ |
| **USB TYPE-C/CC DETECTION** | | | | | | |
| CC Pin Clamp Voltage | VCC_CLAMP | 60µA ≤ ICC1, ICC2 ≤ 600µA | | 1.1 | 1.32 | V |
| CC Pin Clamp Voltage (5.5V) | VCC_CLAMP_5P5 | ICC2, IICC2 < 2mA | | 5.25 | 5.5 | V |
| CC UFP Pulldown Resistance | RPD_UFP | | 4.59 | 5.10 | 5.61 | kΩ |
| CC DFP 0.5A Current Source | IDFP0.5_CC | | -20% | 80 | +20% | µA |
| CC DFP 1.5A Current Source | IDFP1.5_CC | | -8% | 180 | +8% | µA |
| CC DFP 3A Current Source | IDFP3A_CC | | -8% | 330 | +8% | µA |
| CC RA RD Threshold | VRA_RD0.5 | | 0.15 | 0.2 | 0.25 | V |
| CC RA RD Hysteresis | VRA_RD0.5_H | | | 0.015 | | V |
| CC UFP 0.5A RD Threshold | VUFP_RD0.5 | | 0.61 | 0.66 | 0.7 | V |
| CC UFP 0.5A RD Hysteresis | VUFP_RD0.5_H | | | 0.015 | | V |
| CC UFP 1.5A RD Threshold | VUFP_RD1.5 | | 1.16 | 1.23 | 1.31 | V |
| CC UFP 1.5A RD Hysteresis | VUFP_RD1.5_H | | | 0.015 | | V |
| CC DFP Vopen Detect Threshold | VDFP_VOPEN | | 1.5 | 1.575 | 1.65 | V |
| CC DFP Vopen Detect Hysteresis | VDFP_VOPEN_H | | | 0.030 | | V |
| CC DFP Vopen with 3.0A Detect Threshold | VDFP_VOPEN3A | | 2.45 | 2.6 | 2.75 | V |
| CC DFP Vopen with 3.0A Detect Hysteresis | VDFP_VOPEN3A_H | | | 0.030 | | V |
| CC V1P0 Threshold | VCC_V1P0 | | 0.92 | 1.00 | 1.08 | V |
| CC V1P0 Hysteresis | VCC_V1P0_H | | | 0.015 | | V |
| VB Discharge Value Threshold | VSAFE0V | Falling voltage level where a connected UFP finds VB removed | 0.6 | 0.67 | 0.75 | V |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| VB Discharge Value Hysteresis | VSAFE0V_H | Rising hysteresis | | 45 | | mV |
| CC Pin Power-Up Time | tClampSwap | Maximum time allowed from removal of voltage clamp till 5.1kΩ resistor attached | | | 15 | ms |
| CC Detection Debounce | tCCDeb | | 100 | 119 | 200 | ms |
| USB Type-C Debounce | tPDDeb | | 10 | 15 | 20 | ms |
| USB Type-C Quick Debounce | tQDeb | | 0.9 | 1 | 1.1 | ms |
| VSAFE0V Debounce | tVSAFE0VDeb | | 9 | 10 | 11 | ms |
| USB Type-C Error Recovery Delay | tErrorRecovery | | 25 | | | ms |
| USB Type-C DRP Toggle Time | tDRP | | 50 | 75 | 100 | ms |
| DFP Duty Cycle at DRP | DDRP_DCYC | Programmable from 35% to 50% in 5% step, CCDRPPhase = 0b00 | | 35 | | % |
| USB Type-C DRP Try | tDRPtry | | 90 | 100 | 110 | ms |
| DRP Transition Time | tDRPTrans | Time a role swap from DFP to UFP or reverse is completed | | | 1 | ms |
| VCONN Enable Time | tVCONNON | | | | 2 | ms |
| VCONN Disable Time | tVCONNOFF | Time from UFP detached or as directed by $I^2C$ command until VCONN is removed | | | 35 | ms |
| CC Pin Current Change Time | tSINKADJ | Time from CC pin changes state in UFP mode till current drawn from DFP reaches new value | | | 60 | ms |
| VB On Time | tVBON | Time from UFP is attached till VB ON | | | 275 | ms |
| VB Off Time | tVBOFF | Time from UFP is detached till VB reaches VSAFE0V | | | 650 | ms |
| USB TYPE-C/$V_{CONN}$ SWITCH | | | | | | |
| VCONN Source Requirements | VCONN | | 3.0 | | 5.5 | V |
| VCONN Switch On Resistance | RON_VCON_SW | VBAT = 4.2V, ICC = 0.1A | | 1.00 | 1.55 | Ω |
| VCONN Overcurrent Protection Thresholds Accuracy | IOCP_VCONN_ACC | VBAT = 4.2V, TA = +25ºC | -15 | | +15 | % |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| VCONN Short Circuit Current Protection Rising Threshold | ISCCP_VCONN | CC load current rising | 0.425 | 0.500 | 0.575 | A |
| VCONN Overcurrent Protection Threshold Programmable Step | IOCP_VCONN_STEP | Programmable range is 200mA to 350mA | | 50 | | mA |
| VCONN Overcurrent Protection Interrupt Debounce Time | tOCP_VCONN_DEB | From detecting OCP to generating INT | | 2 | | ms |
| VCONN Overcurrent Protection Wait Time Before Turn Off | tOCP_VCONN_OFF | From generating INT to turning OFF VCONN switch | | 12 | | ms |
| VCONN Startup Time | tVCONN_90 | Time from VCONN switch enable to CC settled at 90% of final value with VBAT = 4.2V | | 12 | 35 | µs |
| **SBU RESISTOR AND MOISTURE DETECTION MEASUREMENT** | | | | | | |
| SBU1/SBU2 Continuous Resistor Detection Quiescent Current | IQ_SBUDET | 200ms period, ADCAvgNum[2:0] ≤ 3 | | < 1.0 | | µA |
| Periodic Moisture Detection Quiescent Current | IQ_MOISTDET | 10s period | | < 1.0 | | µA |
| Pullup Current 1X | IPU1X_RDET_SBU | Pullup current on SBU1 or SBU2 | 1.952 | 2.000 | 2.048 | µA |
| | IPU1X_RDET_CCCD | Pullup current on CC1 or CC2 or CDP or CDN | 1.840 | 2.000 | 2.160 | |
| Pullup Current 4X | IPU4X_RDET_SBU | Pullup current on SBU1 or SBU2 | 7.809 | 8.000 | 8.191 | µA |
| | IPU4X_RDET_CCCD | Pullup current on CC1 or CC2 or CDP or CDN | 7.720 | 8.000 | 8.280 | |
| Pullup Current 16X | IPU16X_RDET_SBU | Pullup current on SBU1 or SBU2 | 31.234 | 32.000 | 32.766 | µA |
| | IPU16X_RDET_CCCD | Pullup current on CC1 or CC2 or CDP or CDN | 31.000 | 32.000 | 33.000 | |
| Pullup Current 64X | IPU64X_RDET_SBU | Pullup current on SBU1 or SBU2 | 124.941 | 128.000 | 131.059 | µA |
| | IPU64X_RDET_CCCD | Pullup current on CC1 or CC2 or CDP or CDN | 124.400 | 128.000 | 131.600 | |
| Pulldown Switches On Resistance | RMOIST_SWPD | Enabled during moisture detection only | 50 | 150 | 280 | Ω |
| Pullup Forcing/Sensing | RMOIST_SWPU | (Note 2) | 200 | 500 | 1050 | Ω |

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| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Switches On Resistance | | | | | | |
| SAR ADC Full Scale Voltage | VADC_FS | | 1.485 | 1.500 | 1.515 | V |
| SAR ADC DAC Voltage Accuracy | VADC_DAC ACC | | -0.3 | | +0.3 | % |
| SAR ADC Comparator Static Error | VADC_COM PTH | | -2.85 | | +2.85 | mV |
| SAR ADC Comparator Maximum Dynamic Error | VADC_COM P_DYN | | | 1.5 | | mV |
| SAR ADC Least Significant Bit | VADC_LSB | 8 bits | | 0.392 | | % V_ADC _FS |
| SAR ADC RC Antialiasing Filter Time Constant | tADC_FILT | | | 90 | | µs |
| SAR ADC Conversion Time | tADC_CONV | 1.1ms (typ) additional delay prior to the first conversion | | 104 | | µs |
| ADC Worst Case Accuracy | VADC_ERR | Voltage on pullup pin(s) = 0.375V | -1.47 | | +1.47 | V_ADC _LSB (typ) |
| | | Voltage on pullup pin(s) = 1.500V | -4.18 | | +4.18 | |
| | | Voltage on pullup pin(s) = 0.375V | -2.31 | | +2.31 | % |
| | | Voltage on pullup pin(s) = 1.500V | -1.64 | | +1.64 | |
| Auto Detectable SBU1/SBU2 Resistance Range | RSBU_RNG | IPU1X_RDET_SBU pullup current applied on SBU1 or SBU2 | 187.5 | | 714.7 | kΩ |
| | | IPU4X_RDET_SBU pullup current applied on SBU1 or SBU2 | 46.88 | | 170.2 | |
| | | IPU16X_RDET_SBU pullup current applied on SBU1 or SBU2 | 11.72 | | 42.57 | |
| | | IPU64X_RDET_SBU pullup current applied on SBU1 or SBU2 | 2.93 | | 10.64 | |
| SBU1/SBU2 Resistance Ground Condition Range | RSBU_RNG _GND | IPU64X_RDET_SBU pullup current applied on SBU1 or SBU2. ADCGroundVth[3:0] = 0b0100 | 0 | | 100.11 | Ω |
| Auto Detectable CC/CD Moisture Resistance Range | RCCCD_RN G | IPU1X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | 187.5 | | 672.6 | kΩ |
| | | IPU4X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | 46.88 | | 149.7 | |

($V_{BAT}$ = 3.6V , $V_B$ = 5V, $C_{VDD}$ = 1µF, $C_{VB}$ = 1µF, $C_{OUT}$ = 1µF, $C_{BAT}$ = 1µF, limits are production tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. )

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | | IPU16X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | 11.72 | | 39.30 | |
| | | IPU64X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | 2.93 | | 9.86 | |
| CC/CD Resistance Ground Condition Range | RCCCD_RNG_GND | IPU64X_RDET_CCCD pullup current applied on CDP and/or CDN. ADCGroundVth[3:0] = 0b0100 | 0 | | 99.70 | Ω |
| SBU1/SBU2 Resistance Measurement Accuracy | RSBU_ACC | Within RSBU_RNG resistive range and under IPU1X_RDET_SBU pullup current applied on SBU1 or SBU2 | -4.70 | | +4.70 | % |
| | | Within RSBU_RNG resistive range and under IPU4X_RDET_SBU pullup current applied on SBU1 or SBU2 | -4.70 | | +4.70 | |
| | | Within RSBU_RNG resistive range and under IPU16X_RDET_SBU pullup current applied on SBU1 or SBU2 | -4.70 | | +4.70 | |
| | | Within RSBU_RNG resistive range and under IPU64X_RDET_SBU pullup current applied on SBU1 or SBU2 | -4.70 | | +4.70 | |
| CC/CD Resistance Measurement Accuracy | RCCCD_ACC | Within RCCCD_RNG resistive range and under IPU1X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | -10.31 | | +10.31 | % |
| | | Within RCCCD_RNG resistive range and under IPU4X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | -5.81 | | +5.81 | |
| | | Within RCCCD_RNG resistive range and under IPU16X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | -5.44 | | +5.44 | |
| | | Within RCCCD_RNG resistive range and under IPU64X_RDET_CCCD pullup current applied on CC1 or CC2 or CDP or CDN | -5.13 | | +5.13 | |
| **USB DATA SWITCHES (TDP/TDN)** | | | | | | |
| Analog Signal Range | VTDP/N | | 0 | | 5.5 | V |
| On-Resistance | RON_TD | | | 3.7 | 6.0 | Ω |
| On-Resistance Match Between Channels | ΔRON_TD | ITDP/N = 10mA, VTDP/N = 0.0V | | 0.02 | | Ω |

($V_{BAT}$ = 3.6V , $V_B$ = 5V, $C_{VDD}$ = 1µF, $C_{VB}$ = 1µF, $C_{OUT}$ = 1µF, $C_{BAT}$ = 1µF, limits are production tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. )

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| On-Resistance Flatness | RFLAT_TD | ITDP/N = 10mA, VTDP/N = 0.0V to 5.5V | | 0.005 | | Ω |
| Off Leakage Current | IOFF_TD | VCDP/N = 0V, VTDP/N = 2.5V | -0.5 | 0.5 | +1.5 | µA |
| On Leakage Current | ION_TD | VTDP/N = 2.5V, VCDP/N = open | -1 | | +1.5 | µA |
| Turn-On Time | tON_TD | VTDP/N = 1.5V, RLOAD = 50Ω | | 55 | | µs |
| Turn-Off Time | tOFF_TD | VTDP/N =1.5V, RLOAD = 50Ω | | 20 | | µs |
| Output Skew Same Switch | tSK(P)_TD | | | 40 | | ps |
| Output Skew Between Switch | tSK(O)_TD | | | 40 | | ps |
| Break-Before-Make Time Delay | tBBM_TD | RLOAD = 50Ω, delay between one side of the switch opening and the other side closing | 0 | 3 | | µs |
| -3dB Bandwidth | fBW_TD | VD_= 0dBm, RS = RL = 50Ω | | 400 | | MHz |
| Off-Isolation | VISO_TD | f = 20kHz, VD_ = 0.4Vp-p, RL = 50Ω | | -80 | | dB |
| Crosstalk | VCRTLK_TD | f = 20kHz, VD_ = 0.4Vp-p, RL = 50Ω | | -80 | | dB |
| PSRR | VPSRR_TD | V = 400mVpp, f = 20kHz, RS = RL = 50Ω | | -60 | | dB |
| **UART Switches (UR_UT)** | | | | | | |
| Analog Signal Range | VUR/T | | 0 | | 5.5 | V |
| On-Resistance | RON_U | | | 23 | 36 | Ω |
| On-Resistance Match Between Channels | ΔRON_U | IUR/T = 1mA, VUR/T = 0.0V | | 0.3 | | Ω |
| On-Resistance Flatness | RFLAT_U | IUR/T = 10mA, VUR/T = 0.0V to 5.5V | | 0.01 | | Ω |
| Off Leakage Current | IOFF_U | VCDP/N = 0V, VUR/T= 2.5V | -0.5 | 0.5 | +1.5 | µA |
| On Leakage Current | ION_U | VUR/T = 2.5V, VCDP/N = floating | -1 | | +1.5 | µA |
| Turn-On Time | tON_U | VUR/T = 1.5V, RLOAD = 50Ω | | 30 | | µs |
| Turn-Off Time | tOFF_U | VUR/T = 1.5V, RLOAD = 50 Ω | | 15 | | µs |
| Break-Before-Make Time Delay | tBBM_U | RLOAD = 50Ω, delay between one side of the switch opening and the other side closing | 0 | 38 | | µs |
| -3dB Bandwidth | fBW_U | VD = 0dBm, RS = RL = 50Ω | | 350 | | MHz |
| Off-Isolation | VISO_U | f = 20kHz, VD = 0.4Vp-p, RL = 50Ω | | -90 | | dB |
| Crosstalk | VCRTLK_U | f = 20kHz, VD = 0.4Vp-p, RL = 50Ω | | -70 | | dB |
| PSRR | VPSRR_U | V = 400mVpp, f = 20kHz, RS = RL = 50Ω | | -60 | | dB |
| I²C INTERFACE TIMING | | | | | | |
| Clock Frequency | fSCL | | | | 1000 | kHz |

($V_{BAT}$ = 3.6V , $V_B$ = 5V, $C_{VDD}$ = 1µF, $C_{VB}$ = 1µF, $C_{OUT}$ = 1µF, $C_{BAT}$ = 1µF, limits are production tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. )

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Hold Time (Repeated) START Condition | tHD:STA | | 0.26 | | | µs |
| CLK Low Period | tLOW | | 0.5 | | | µs |
| CLK High Period | tHIGH | | 0.26 | | | µs |
| Setup Time Repeated START Condition | tSU:STA | | 0.26 | | | µs |
| DATA Hold Time | tHD:DAT | | 0 | | | µs |
| DATA Valid Time | tVD:DAT | | | | 0.45 | µs |
| DATA Valid Acknowledge Time | tVD:ACK | | | | 0.45 | µs |
| DATA Setup time | tSU:DAT | | 50 | | | ns |
| Setup Time for STOP Condition | tSU:STO | | 0.26 | | | µs |
| Bus-Free Time Between STOP and START | tBUF | | 0.5 | | | µs |
| Pulse Width of Spikes that Must be Suppressed by the Input Filter | tsp | | | 50 | | ns |
| Input Logic High | VIN_IH | | 1.5 | | | V |
| Input Logic Low | VIN_IL | | | | 0.3 | V |
| Input Logic Leakage Current | IIN_LKG | | -1 | | +1 | µA |
| OPEN DRAIN OUTPUTS ($\overline{CE}$, $\overline{DB}$, $\overline{INT}$) | | | | | | |
| Open Drain Logic low | VOD_OL | IOD = 2mA | | | 0.4 | V |
| Open Drain Output High Leakage Current | IOD_LKG | | -1 | | +1 | µA |
| **ESD PROTECTION** | | | | | | |
| HBM | | CDP/CDN | | ±6 | | kV |
| | | SBU1/SBU2, CC1/CC2, VB (connected to 1µF capacitor) | | ±15 | | |
| IEC61000-4-2 Contact Discharge | | SBU1/SBU2, CC1/CC2, VB (connected to 1µF capacitor) | | ±8 | | kV |
| IEC61000-4-2 Air Gap | | SBU1/SBU2, CC1/CC2, VB (connected to 1µF capacitor) | | ±15 | | kV |
| **SURGE PROTECTION** | | | | | | |
| IEC61000-4-5 Surge | | VB | | ±120 | | V |

($V_{BAT}$ = 3.6V , $V_B$ = 5V, $C_{VDD}$ = 1µF, $C_{VB}$ = 1µF, $C_{OUT}$ = 1µF, $C_{BAT}$ = 1µF, limits are production tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. )

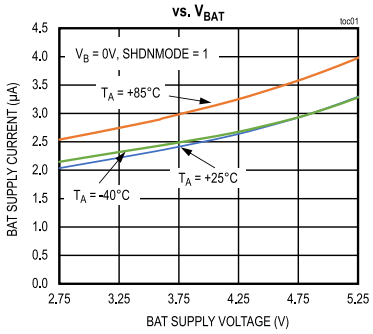
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | | CC1/CC2, SBU1/SBU2 | | ±45 | | |

**Note 2:** During moisture detection in manual configuration, if more than one pin among SBU1, SBU2, CDP, CDN, CC1, and CC2 is pulled up at the same time, the pullup current is forced on a common internal node shared by the forcing switches, while the voltage measured by the ADC is that of another common internal node shared by the sensing switches. Both forcing and sensing switches have an $R_{MOIST\_SWPU}$ resistance. For example, if just two pins are pulled up, an overall equivalent resistance equal to $R_{MOIST\_SWPU}$ is applied between them. If the pullup pins are more than two, the resistive mesh internally applied between the pins is that shown in *Figure 7*, where the SWP[n] switches are the forcing/sensing ones with $R_{MOIST\_SWPU}$ resistance.

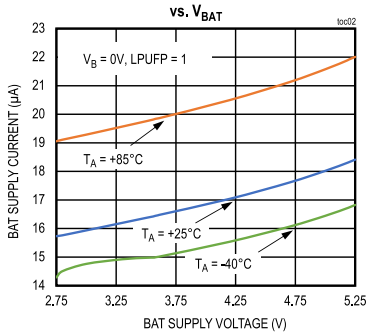
## Typical Operating Characteristics

($T_A$ = +25ºC, $V_B$ = 5V, unless otherwise noted.)

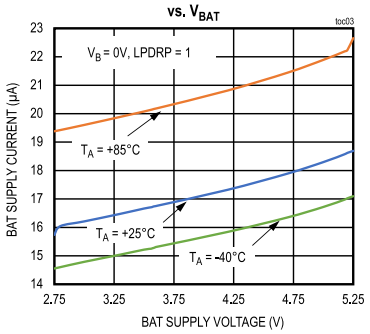
BAT SUPPLY CURRENT vs. $V_{BAT}$



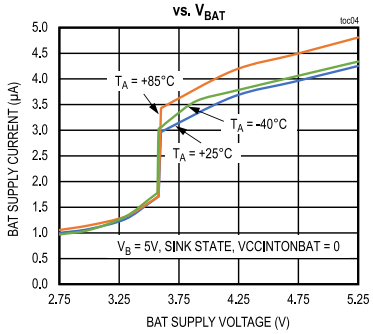

BAT SUPPLY CURRENT vs. $V_{BAT}$



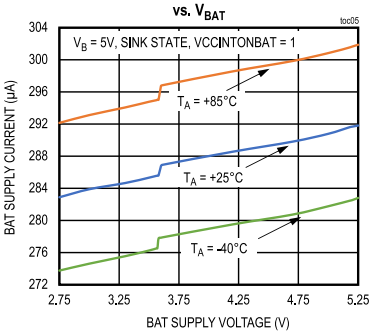

BAT SUPPLY CURRENT vs. $V_{BAT}$



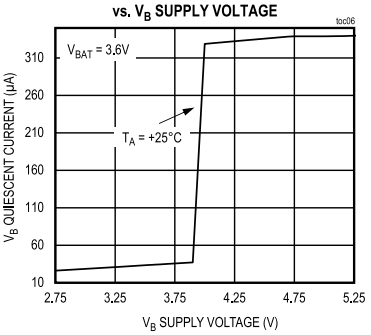

BAT SUPPLY CURRENT vs. $V_{BAT}$



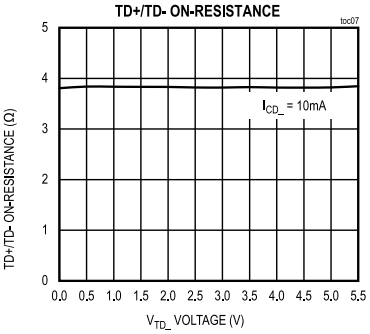

BAT SUPPLY CURRENT vs. $V_{BAT}$



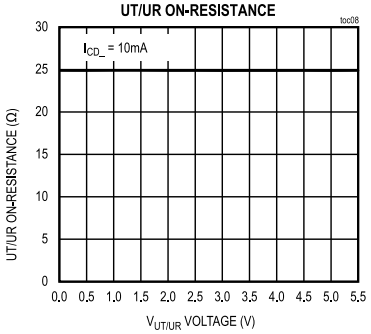

$V_B$ QUIESCIENT CURRENT (RETAKE) vs. $V_B$ SUPPLY VOLTAGE



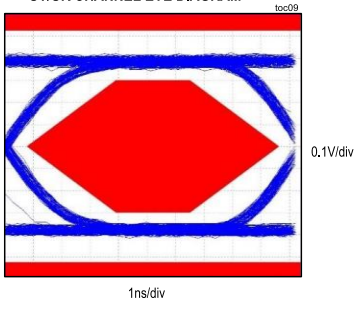

TD+/TD- ON-RESISTANCE



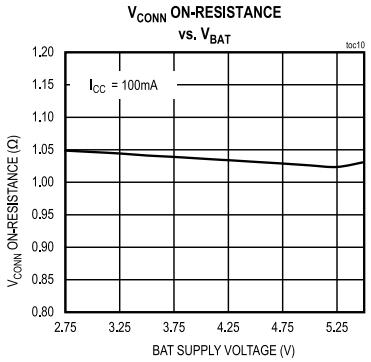

UT/UR ON-RESISTANCE

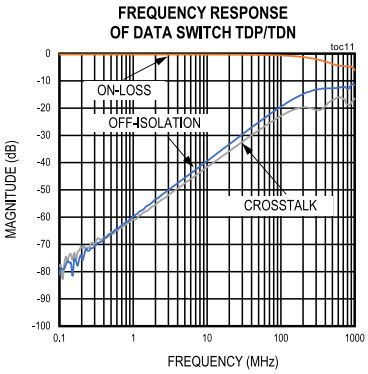


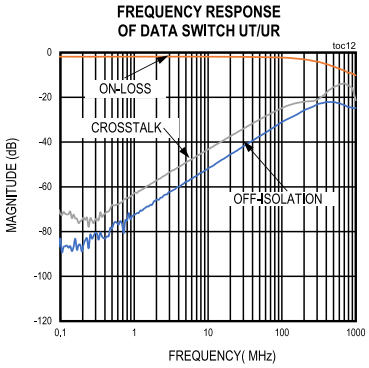

UT/UR CHANNEL EYE DIAGRAM



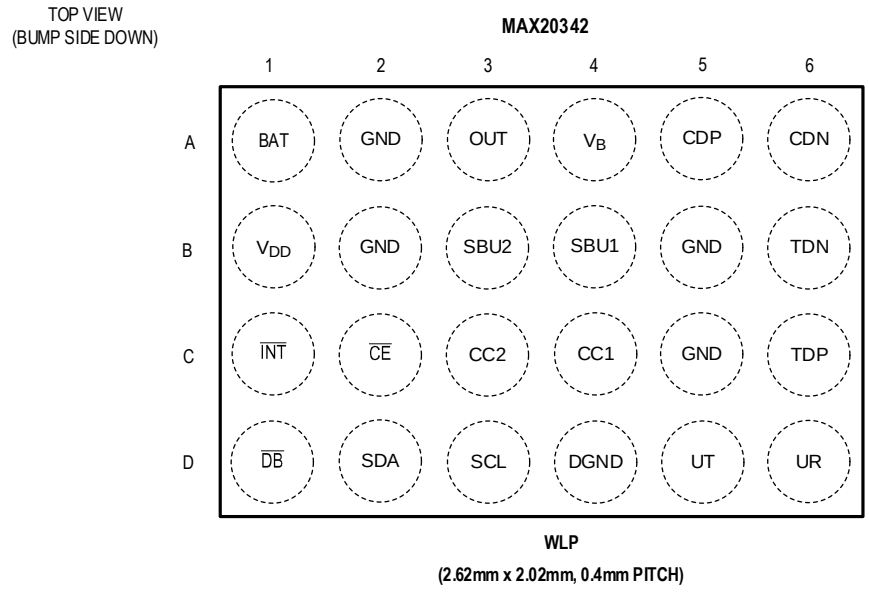
($T_A$ = +25ºC, $V_B$ = 5V, unless otherwise noted.)



## Bump Configuration

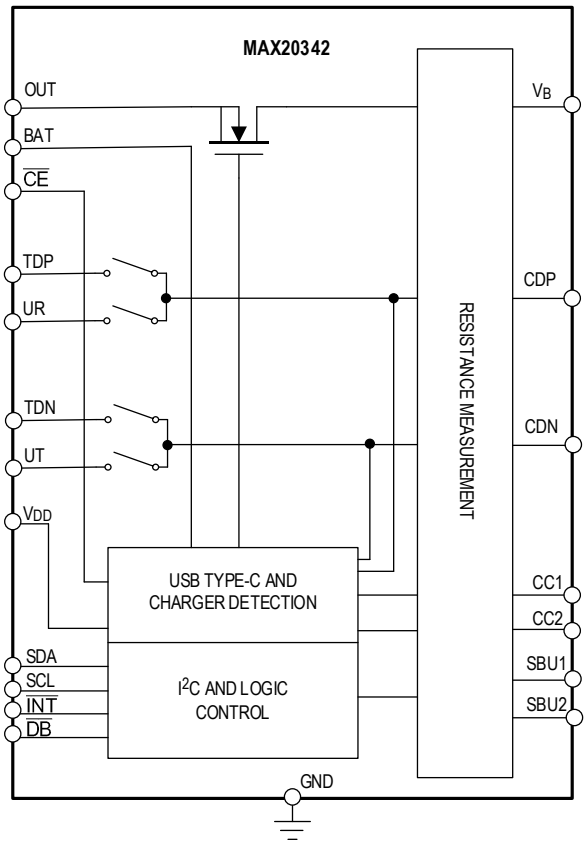



## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| A1 | BAT | Battery Connection Input. Bypass BAT to GND with a capacitor of 1µF effective capacitance. |
| A2 | GND | Ground |
| A3 | OUT | Overvoltage-Protected $V_B$ Power Output. Bypass OUT to GND with a capacitor of 1µF effective capacitance. |
| A4 | VB | USB Type-C $V_{BUS}$ Connection. Bypass $V_B$ to GND with a capacitor of 1µF effective capacitance. |
| A5 | CDP | USB Connector D+ Connection |
| A6 | CDN | USB Connector D- Connection |
| B1 | VDD | Internal Supply Input. Bypass $V_{DD}$ to GND with a capacitor of 1µF effective capacitance. |
| B2 | GND | Ground |
| B3 | SBU2 | USB Type-C SBU2 Connection |
| B4 | SBU1 | USB Type-C SBU1 Connection |
| B5 | GND | Ground |
| B6 | TDN | USB Transceiver D- Connection |
| C1 | INT | Active-Low, Open-Drain Interrupt Output. Connect $\overline{INT}$ to an external pullup resistor. |
| C2 | CE | Active-Low, Open-Drain Charger Control Enable Output. Connect $\overline{CE}$ to an external pullup resistor. |
| C3 | CC2 | USB Type-C CC2 Connection |
| C4 | CC1 | USB Type-C CC1 Connection |

| | | |
|---|---|---|
| C5 | GND | Ground |
| C6 | TDP | USB Transceiver D+ Connection |
| D1 | DB | Active-Low, Open-Drain Output. This pin is driven low when an 80kΩ resistor is connected to SBU1 or SBU2. Connect $\overline{DB}$ to an external pullup resistor. |
| D2 | SDA | I²C Serial-Data Input/Output. Connect SDA to an external pullup resistor. |
| D3 | SCL | I²C Serial-Clock Input. Connect SCL to an external pullup resistor. |
| D4 | DGND | Digital Ground |
| D5 | UT | UART Tx Device Connection |
| D6 | UR | UART Rx Device Connection |

## Functional Diagram



## Detailed Description

### USB BC1.2 Charger Detection

The MAX20342 USB charger detection block supports USB BC1.2 with the additional capability to automatically detect some common proprietary charger types. Note that after the secondary detection of USB BC1.2 finishes, the device does not keep $V_{DP\_SRC}$ enabled if DCP is detected. While this behavior can cause the device to fail the DCP test in USB BC1.2 compliance, this is not expected to cause any issue in the detection of BC1.2 chargers.

The Charger Detection State Machine follows USB BC1.2 requirements and detects SDP, CDP, and DCP charger types (see Table 1) In addition to the USB BC1.2 State Machine, the MAX20342 also detects a limited number of proprietary charger types (Apple, Samsung, and generic 500mA). The MAX20342 always reports SDP/CDP/DCP in addition to a detected proprietary type. For example, the Samsung proprietary charger uses D+/D- short and bias on D+/D-. The bias voltage is chosen so that, with a USB BC1.2 compliant state machine, it is detected as a DCP. The device reports this charger detected as both a DCP and a Samsung charger. See Table 2 and Table 3 for more details.

The MAX20342 also reports the operation status of the Charger Detection State Machine in the ChgTypRun interrupt bit in the register map.

## Table 1. USB BC1.2 Charger Type Detection

| CHGTYP[1:0] | CHARGER DETECTED |
|---|---|
| 0b00 | No CHGIN |
| 0b01 | SDP |
| 0b10 | CDP |
| 0b11 | DCP |

***Note:*** *Charge Detect running state is indicated until the Charger Detection State Machine is complete.*

## Table 2. Proprietary Detection Table

| | | D+ | | | | |
|---|---|---|---|---|---|---|
| | | 0 TO 0.32V | 0.32V TO 31% OF VB | 31% TO 47% OF VB | 47% TO 64% OF VB | 64% TO 100% OF VB |
| D- | 0 TO 0.32V | Unknown | Unknown | Unknown | Unknown | Unknown |
| | 0.32V TO 31% OF VB | Unknown | Samsung | Unknown | Unknown | Unknown |
| | 31% TO 47% OF VB | Unknown | Unknown | Apple 0.5A | Apple 2.0A | Unknown |
| | 47% TO 64% OF VB | Unknown | Unknown | Apple 1.0A | Apple 12W | Unknown |
| | 64% TO 100% OF VB | Unknown | Unknown | Unknown | Unknown | Unknown |

Examples of ChgTyp[1:0] and PrChgTyp[2:0] values found for common chargers on the market are listed in *Table 3*. When the MAX20342 detects the charger, it sets the $\overline{CE}$ output based on the charger type found. *Table 4* shows D+/D- termination for Apple chargers, Samsung charger, dedicated charger, and a standard USB host charging downstream port.

## Table 3. Charger Control Table

| ADAPTER TYPE | CHGTYP[1:0] | PRCHGTYP[2:0] | CE OUTPUT | |
|---|---|---|---|---|
| | | | NOTUSBCMPL = 0b0 | NOTUSBCMPL = 0b1 |
| Nothing connected | | | High | High |
| DCP | 0x03 DCP | 0x00 unknown | Low | Low |
| SDP | 0x01 SDP | 0x00 unknown | High | Low |
| CDP | 0x02 CDP | 0x00 unknown | Low | Low |
| Samsung 2A DCP | 0x03 DCP | 0x01 Samsung 2A | Low | Low |
| Apple 500mA | 0x01 SDP | 0x02 Apple 0.5A | Low | Low |
| Apple 1A | 0x02 CDP | 0x03 Apple 1A | Low | Low |
| Apple 2A | 0x01 SDP | 0x04 Apple 2A | Low | Low |
| Apple 12W | 0x03 DCP | 0x05 Apple 12W | Low | Low |

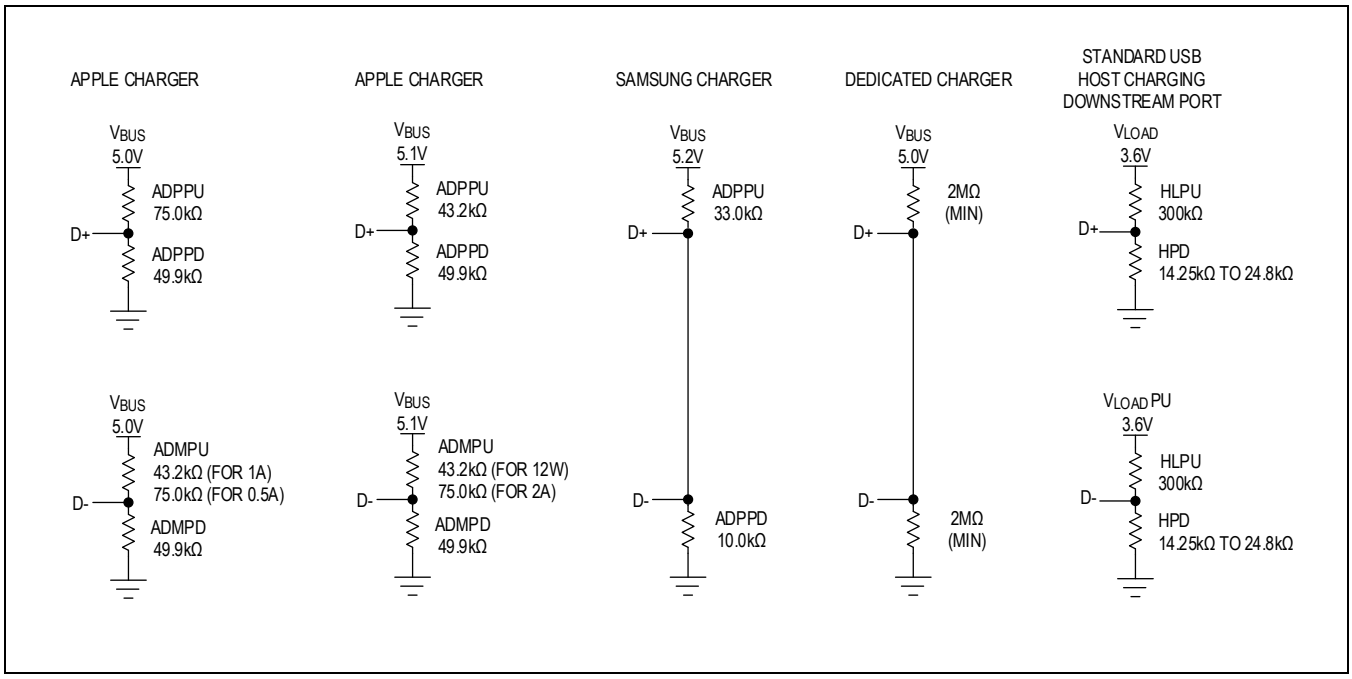



*Figure 1. Apple Chargers, Samsung Charger, Dedicated Charger, and Standard USB Host Charging Downstream Port*

### Autoconfiguration Mode

The MAX20342 is capable of automatically setting the position of the internal analog switches, and $\overline{CE}$ and $\overline{DB}$ outputs based on the state of $V_B$ voltage, CC resistor value, and SBU resistor value. See *Table 4* for more details.

The autoconfiguration state machine starts when either the device is in Debug Accessory Sink Mode and FactAuto = 1, or the device is connected to the valid $V_B$ voltage and USBAuto = 1. If FactAuto = 0 and USBAuto = 0, the autoconfiguration cannot start.

## Table 4. Autoconfiguration Mode Table

| MAX20342 DEVICE CONFIGURATION BASED ON VB, CC PINS, AND SBU PINS | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **RESET** | **INVALID** | **UART** | **USB/ FACTORY** | **UART/ FACTORY** | **USB CHARGER (OTHER THAN SDP FOUND)** | **USB HOST (SDP FOUND)** | **USB DEVICE (SOURCE MODE, DRP ONLY)** | **ANALOG AUDIO ACCESSORY** | **$V_{CONN}$ POWERED DEVICE (E.G., DIGITAL HEADSET)** |
| FACTAUTO/ USBAUTO | - | - | FactAuto = 1 | FactAuto = 1 | FactAuto = 1 | USBAuto = 1 | USBAuto = 1 | USBAuto = 1 | USBAuto = 1 | USBAuto = 1 |
| $V_B$ | Not connected | Outside valid range | Valid | Valid | Valid | Valid | Valid | - | Not Connected | Not Connected |
| CC PINS | - | - | CC1 and CC2 = $R_p$ | CC1 and CC2 = $R_p$ | CC1 and CC2 = $R_p$ | Only CC1 = $R_p$, or only CC2 = $R_p$ | Only CC1 = $R_p$, or only CC2 = $R_p$ | Only CC1 = $R_d$, or only CC2 = $R_d$ | CC1 and CC2 = $R_a$ | CC1 = $R_d$ and CC2 = $R_a$, or CC1 = $R_a$ and CC2 = $R_d$ Connect BAT ($V_{CONN}$) to CC_ with $R_a$ through switch |
| SBU PINS | - | - | SBU1 or SBU2 = 30kΩ | SBU1 or SBU2 = 80.2kΩ | SBU1 or SBU2 = 150kΩ | - | - | - | - | - |
| OUT | High-Z | High-Z | High-Z | $V_B$ | $V_B$ | $V_B$ | $V_B$ | OVP switch requires manual setting (**) | High-Z | High-Z |
| CDP/CDN SWITCH POSITION | - | - | UR/UT | TDP/TDN | UR/UT | OPEN | TDP/TDN | TDP/TDN | OPEN | TDP/TDN |
| $\overline{CE}$ | High-Z | High-Z | High-Z | GND | GND | GND | High-Z or GND (*) | High-Z | High-Z | High-Z |
| $\overline{DB}$ | High-Z | High-Z | High-Z | GND | High-Z | High-Z | High-Z | High-Z | High-Z | High-Z |
| $\overline{INT}$ | High-Z | GND | GND | High-Z | High-Z | High-Z | High-Z | High-Z | High-Z | High-Z |

*(*) $\overline{CE}$ setting depends on NotUSBCmpl bit.*

*(**) If a USB device is detected, the OVP switch must be manually set as described in the OVP Manual Setting section.*

## OVP Manual Setting

In the case where a USB device is detected and the MAX20342 needs to source power from OUT to $V_B$, and then to the USB Type-C receptacle, the OVP switch needs to be manually set. When the MAX20342 has detected through the USB Type-C that a USB device has been attached, the user must follow the procedure to source power from OUT to $V_B$.

1. Manually close the OVP switch setting (VBOVPEn = 0x3). At this point, no power source must be attached to OUT.
2. Wait for SwtClosedInt interrupt request. At this point the OVP switch is closed and power can be attached to OUT.
3. Enable power source on OUT.

The user must follow the procedure to stop power sourcing to $V_B$.

1. Disable power source on OUT.
2. Manually open the OVP switch setting (VBOVPEn = 0x0). Wait for SwtClosedInt interrupt request. At this point the OVP switch is actually open.

The power source on OUT must not exceed 2A and 5.5V to avoid triggering the OVLO threshold. This restriction avoids a voltage drop between OUT and $V_B$ ($OUT - V_B = R_{ON} \times I_{MAX}$) that is greater than the diode forward voltage (0.3V), which prevents current flow through the diode.

## USB Type-C Detection

The MAX20342 is a complete solution for USB Type-C port charger detection and multiplexing USB and UART on a single USB Type-C connector.

The USB Type-C block detects connected accessories by using USB Type-C and USB BC1.2 charger detection. The USB Type-C block can also measure resistances on the SBU pin and automatically set switch positions and output status signals accordingly. In addition, the USB Type-C block can auto-configure switches for common connected accessories including USB cables (SDP/CDP, etc.) and customer-specific factory cables. A moisture/corrosion detection block allows the system to detect the presence of moisture in the USB Type-C port and alert the user to take specific action.

### Dead Battery

In the case of a dead battery and no $V_B$ attached, 1V voltage clamps are attached to CC1 and CC2 to ensure charging can start from a USB Type-C adapter.

### CC Description

The MAX20342 can be configured to function as an Upstream Facing Port (UFP) or Dual Role Port (DRP) compliant with the USB Type-C 1.3 specification. The USB Type-C functions are controlled by a logic state machine which follows the USB Type-C standard requirements. When configured as a DRP, there is support for the optional Try.SNK function, placing priority on the Sink role.

### Try.SNK Support

The MAX20342 operates as a UFP by default but can be configured to operate as a DRP. A DRP can act as either a Power Sink or a Power Source. The USB Type-C logic state machine cycles between Source and Sink at a rate of 75ms (typ). When the MAX20342 is connected to another device which is also a DRP, the source and sink roles are randomly assigned. The MAX20342 includes support for the Try.SNK state that allows the MAX20342 to be set to strongly prefer the sink role when connected to a standard DRP. If two devices with Try.SNK enable are connected, the role setting is again random.

### Analog Audio Accessory Detection

The MAX20342 provides detection support for USB Type-C analog audio adapter detection by notifying the system microprocessor with an interrupt when an analog audio adapter is detected on the CC1 and CC2 pins. When an audio adapter is detected, the system is required to properly connect the audio codec to the CDP/CDN and SBU1/SBU2 with an external analog switch.

### Moisture Detection

The MAX20342 supports resistance measurement between selected pins on the USB Type-C connector. This measurement can be used to determine if there is moisture or some other form of conductive debris present in the connector. The moisture detection function can be automatically configured (MoistDetAutoCfg = 1) or manually configured (MoistDetAutoCfg = 0) and also supports manual triggering (MoistDetManEn = 1) or periodic triggering (MoistDetPerEn = 1). The moisture detection function is run only when the MAX20342 is not in shutdown mode and $V_B$ or a CC connection has not been detected.

#### Moisture Detection Threshold $R_{MOIST}$

The $R_{MOIST}$ is defined by the combination of the ADC voltage threshold RMoistDetVth[7:0] and the selected pullup current RMoistDetIpu[1:0]. When the measured resistance is below $R_{MOIST}$, the ResMoistInt interrupt is asserted. Since both the voltage and current are needed to calculate resistance, the IpuResult[1:0] and ADCResultAvg[7:0] results are evaluated together to determine if moisture is detected (measured resistance < $R_{MOIST}$). *Table 5* lists the conditions for the indication of moisture. The resistance of the moisture threshold must be set with respect to the resistance constraints listed in *Table 7* and *Table 8.*

## Table 5. Moisture Detection Result

| IPURESULT[1:0] | ADCRESULTAVG[7:0] | MOISTURE DETECTED (MEASURED RESISTANCE < $R_{MOIST}$) |
|---|---|---|
| < RMoistDetIpu[1:0] | Don't Care | No |
| == RMoistDetIpu[1:0] | < RMoistDetVth[7:0] | Yes |
| > RMoistDetIpu[1:0] | Don't Care | Yes |

#### Automatic Configuration

If the automatic configuration mode is selected (MoistDetAutoCfg = 1), all the pulldown and pullup switches described in the *Resistive Measurement* section are automatically controlled during moisture detection. When an automatically configured moisture detection is triggered either manually (MoistDetManEn = 1) or periodically (MoistDetPerEn = 1), the resistance is measured between one of the CC pins and ground while all other USB Type-C pins ($V_B$, CDP, CDN, SBU1, SBU2, and the other CC) are grounded.

If the result is Open or Abort, the moisture detection ends, no interrupt is triggered, and the result is reported in IpuResult[1:0] and ADCResultAvg[7:0]. If the result is a finite resistance above the moisture threshold defined by RMoistDetVth[7:0] and RMoistDetIpu[1:0], the detection ends, ResFiniteInt interrupt is asserted, and the result is reported. If the result is below the moisture threshold, ResMoistInt interrupt is asserted and a burst of consecutive resistive measurements is performed on CC1/CC2/SBU1/SBU2 (pulled up one at a time) to ground while the other USB Type-C pins are grounded. Finally, the burst measurement results are reported in the registers MoistDetAutoCC1/CC2Result1, MoistDetAutoCC1/CC2Result2, MoistDetAutoSBU1/SBU2Result1, and MoistDetAutoSBU1/SBU2Result2. *Figure 2* shows the detection flow for automatically configured moisture detection.

Automatically configured moisture detection always starts on the alternate CC pin when the next detection is triggered either periodically or manually as shown in *Figure 4*.

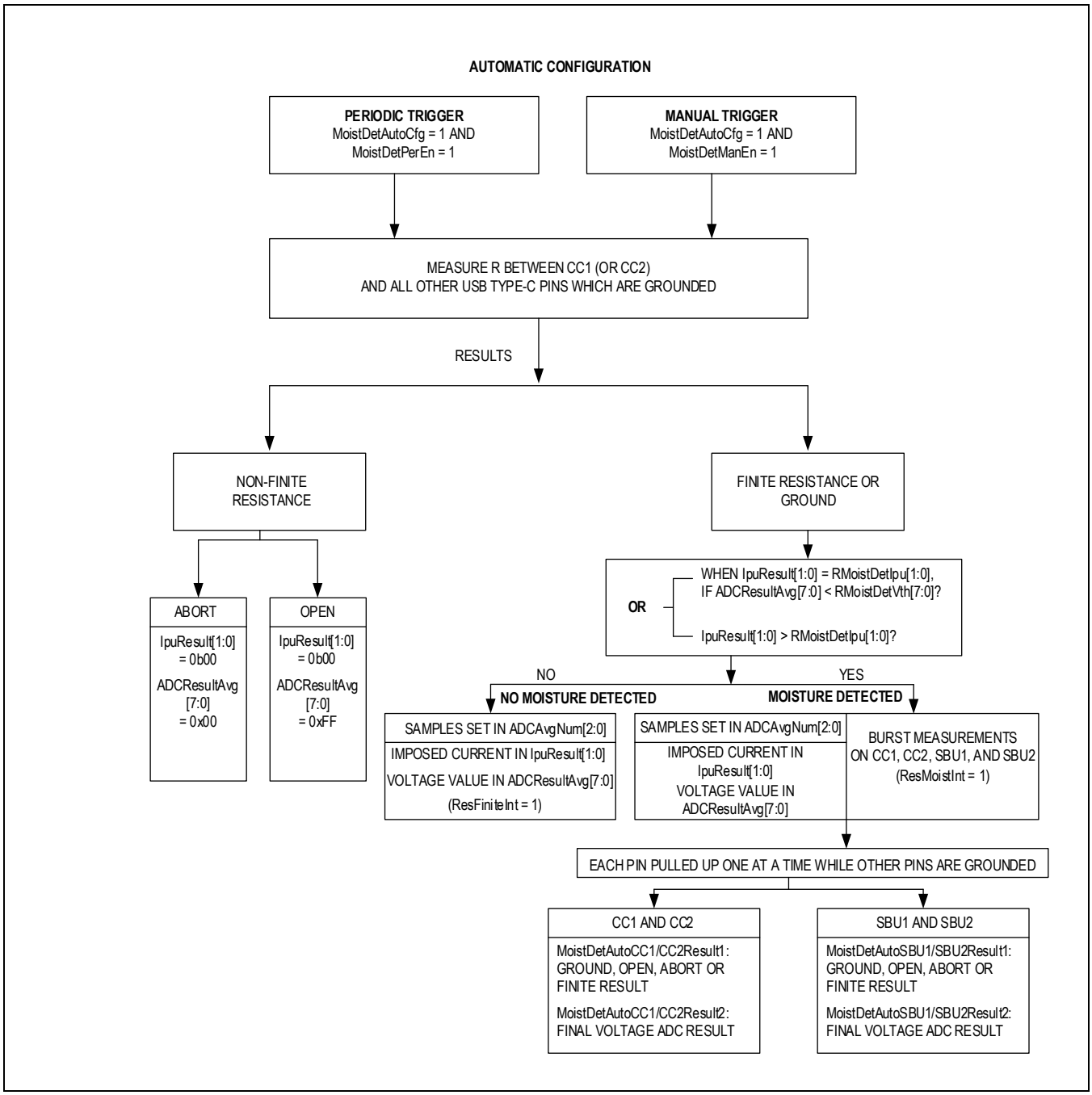



*Figure 2. Automatically Configured Moisture Detection Flow*

### Manual Configuration

If manual configuration mode is selected (MoistDetAutoCfg = 0), all the pulldown and pullup switches described in the *Resistive Measurement* section are configured manually by MoistDetPUConfig[5:0] and MoistDetPDConfig[6:0]. The two pullup and one pulldown switches associated with each USB Type-C pin can be independently configured. This mode allows measuring resistance between the USB Type-C pins in different user-defined configurations. This manually configured moisture detection can also be triggered either manually (MoistDetManEn = 1) or periodically (MoistDetPerEn = 1).

If the result of the measurement is an Abort or Open, the corresponding ResAbortInt or ResOpenInt interrupt is asserted. If the resistance result is higher than or equal to the moisture resistance threshold, ResFiniteInt interrupt is asserted. If the result (including Ground) is lower than the moisture resistance threshold, the ResMoistInt interrupt is asserted instead.

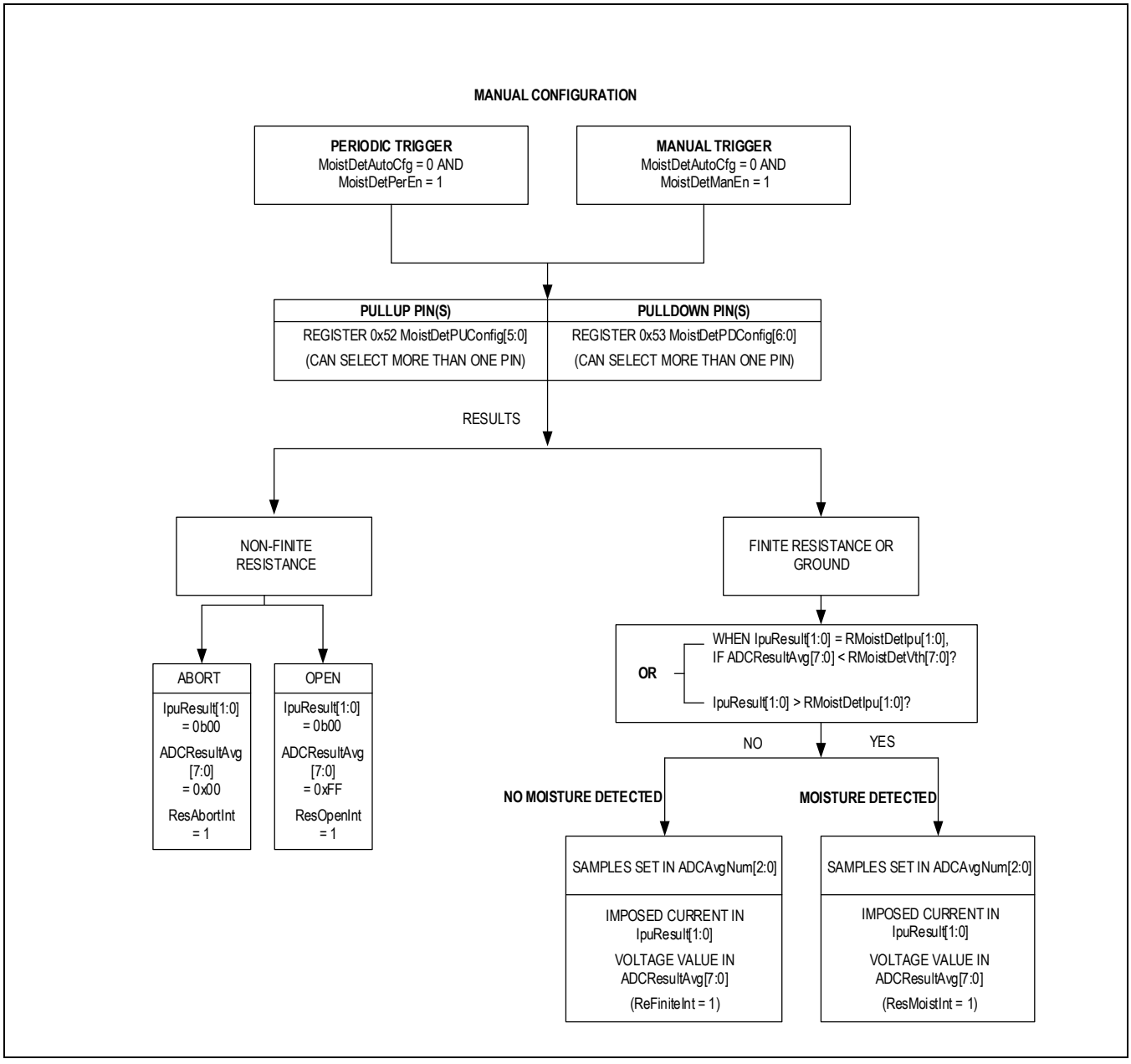



*Figure 3. Manually Configured Moisture Detection Flow*

### Periodic and Manual Trigger

Moisture detection, either automatically or manually configured, can be triggered either manually or periodically. Moisture detection is manually triggered when MoistDetManEn is set to 1; it starts a single moisture detection. MoistDetManEn bit stays high until the end of the measurement and is then self-cleared. If MoistDetManEn is set to 1 while VB or a CC connection is detected, a moisture detection starts as soon as the cable is detached. It is also possible to cancel the pending manual triggered detection by writing a 0 to MoistDetManEn while VB or a CC connection has been detected.

When periodic triggering is enabled by setting MoisetDetPerEn to 1, the moisture detection is run periodically every 10 seconds (typ). It is also possible to manually trigger a moisture detection while periodic trigger is enabled. The 10-second timer does not reset by the manual trigger as shown in *Figure 4* and *Figure 5*.

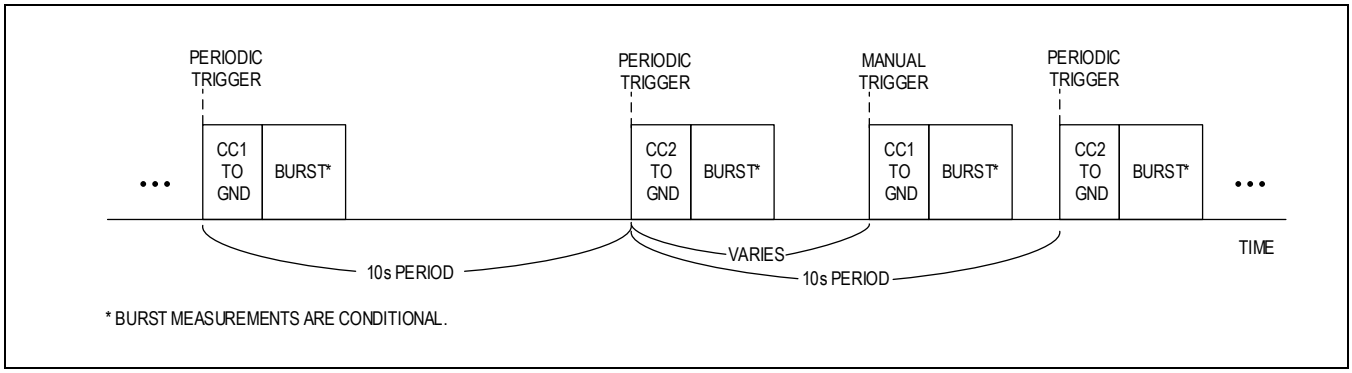



*Figure 4. Moisture Detection Triggering for Automatic Configuration*

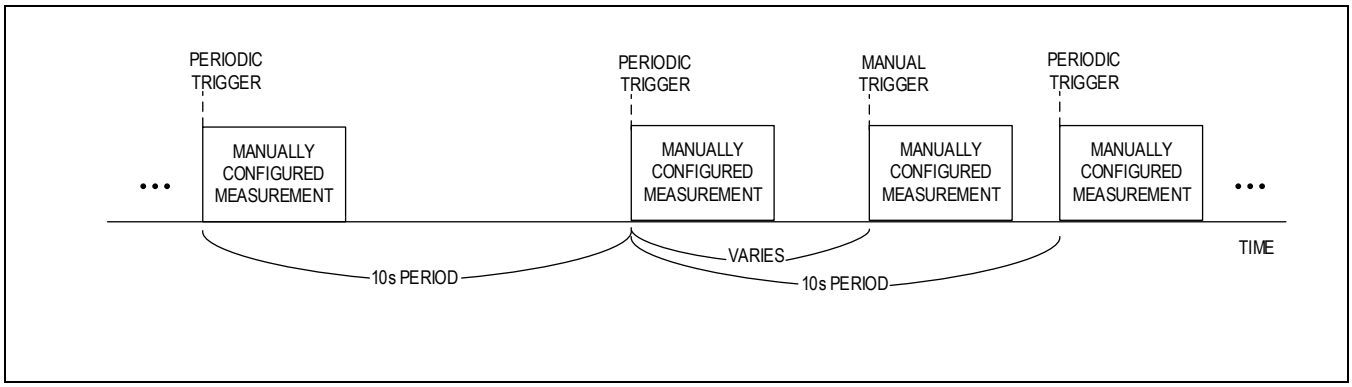



*Figure 5. Moisture Detection Triggering for Manual Configuration*

## Debug Accessory Modes

The MAX20342 can automatically detect up to five accessory modes based on the measured resistance between SBU1 (or SBU2) and ground. These five resistance thresholds are selected by the corresponding RAcc1-5DetVMax[7:0], RAcc1-5DetVMin[7:0], and RAcc1-5DetIpu[1:0] register bits.

If any one of the RaccDet1-5 ranges is detected, the corresponding ResAcc1-5Int interrupt is asserted. In addition, RaccDet1-3 values also define the UART and factory modes. If one of the RaccDet1-3 is detected, the MAX20342 is configured according to *Table 4*.

### Accessory Mode Detection

The five accessory modes (Accessory 1-5) are detected by measuring the resistance on the SBU1 and SBU2 pins using the scheme detailed in the *Resistive Measurement* section. The detection can be triggered manually (SBUDetManEn = 1), continuously (SBUDetContEn = 1), or one-shot (SBUDetOneShotEn = 1). One detection consists of measuring the resistances on SBU1/SBU2 to ground in sequence, reporting the results, and asserting the corresponding interrupts.

Manual trigger runs one detection as soon as SBUDetManEn is set to 1 (except in shutdown mode). Continuous and one-shot triggering work only when the device is in Debug Accessory Sink Mode (CCStat[2:0] = 0b111). With one-shot triggering, a single detection is run upon entering Debug Accessory Sink Mode. For continuous triggering, the detection is run periodically every 200ms until a resistance is found within one of the five accessory mode resistance ranges, or until the Debug Accessory Sink Mode is exited.

After both the SBU1 and SBU2 resistive measurements are completed, individual results are reported in the SBU1DetResult1/2 and SBU2DetResult1/2 registers, and the ResSBUInt interrupt is asserted. The overall result is derived based on these individual results and the SBUDetAbortPriority value as listed in *Table 6*. The corresponding ResAbortInt, ResOpenInt, or ResGroundInt interrupt is also asserted respectively if the overall result is Abort, Open, or Ground. If the overall result is a Finite resistance but not in any of the five accessory mode resistance ranges, a ResFiniteInt is asserted. If it is within one of these ranges, the corresponding ResAcc1-5Int interrupt is asserted.

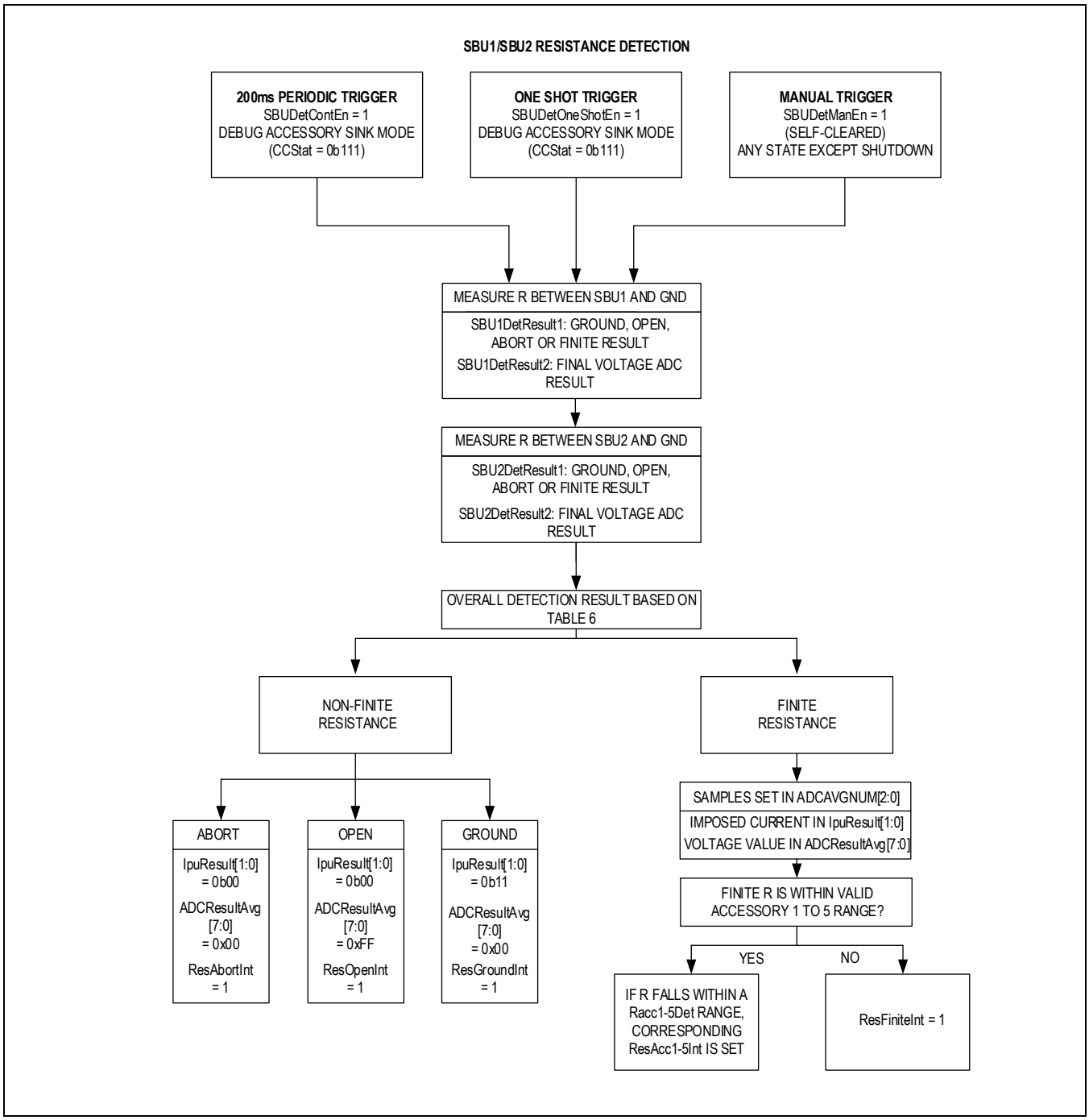



*Figure 6. SBU1/SBU2 Resistance Detection*

## Table 6. SBU Detection Overall Result

| RESULT ON EACH PIN | | OVERALL RESULT | |
|---|---|---|---|
| **SBU1** | **SBU2** | **SBUDETABORTPRIORITY = '0'** | **SBUDETABORTPRIORITY = '1'** |
| Open | Open | Open | |
| Ground | Ground | Ground | |
| Open | Ground | Ground | |
| Ground | Open | Ground | |
| Open | Finite | Finite | |
| Finite | Open | Finite | |
| Ground | Finite | Finite | |
| Finite | Ground | Finite | |
| Finite | Finite | Abort | |
| Abort | Finite | Finite | Abort |
| Finite | Abort | Finite | Abort |
| Abort | Abort | Abort | |
| Open | Abort | Open | Abort |
| Abort | Open | Open | Abort |
| Ground | Abort | Ground | Abort |
| Abort | Ground | Ground | Abort |

### Resistive Measurement

The resistive measurement circuitries used for both moisture detection and SBU1/SBU2 accessory mode detection are the same. As shown in *Figure 7*, it consists of an 8-bit SAR ADC, four switchable pullup currents, one bank of pullup switches, and one bank of pulldown switches. Each USB Type-C pin has one pulldown switch and two pullup switches associated with it. The pulldown switch (each with RMOIST_SWPD on-resistance) connects the pin to ground, while the two pullup switches (each with RMOIST_SWPU on-resistance) connect the pin to the forced node where the pullup current source is connected and to the sensed node where the ADC is connected, respectively.

For example, to measure resistance between SBU1 and the other USB Type-C pins, the two pullup switches of SBU1 are closed, connecting SBU1 to the forced and sensed nodes. The pulldown switches of the other USB-C pins are also closed so that those pins are all grounded. When the pullup current is switched onto the forced node, the current flows through the resistance (between SBU1 and ground) and the voltage on SBU1 is sensed by the ADC on the sensed node. The resistance can then be determined, knowing the forced pullup current and the sensed voltage. These pullup and pulldown switches can be automatically or manually configured as described in the *Moisture Detection* section. In accessory mode detection, only the pullup switches on SBU1 and SBU2 (alternately) are enabled.

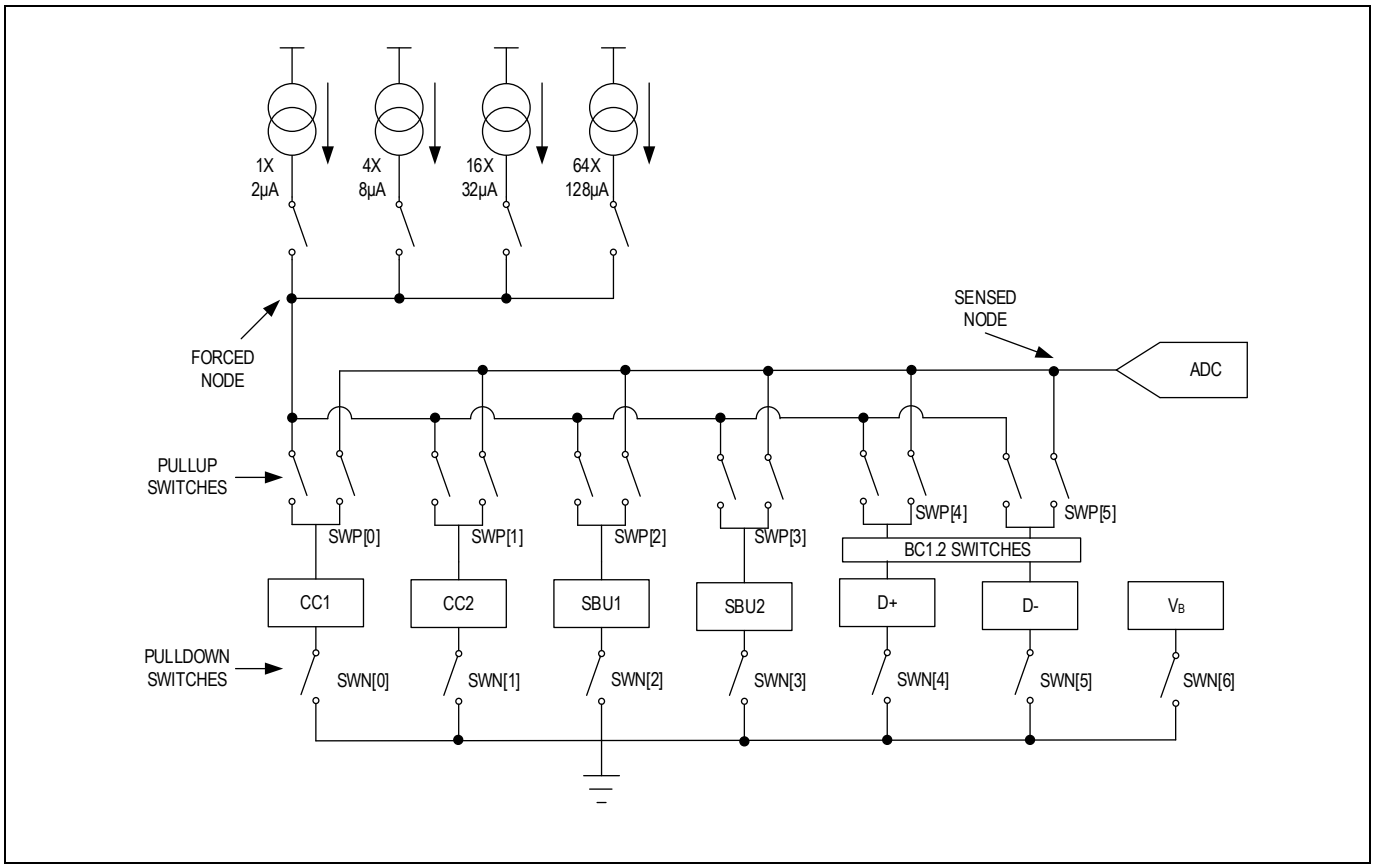



*Figure 7. Resistive Measurement Simplified Diagram*

For each measurement, the ADC takes N = $2_{ADCAvgNum[2:0]}$ samples and records the maximum, minimum, and average values among these samples. To avoid operating the ADC with a small input level where the offset error is dominant, the device starts with the 2µA pullup current and increases it by a factor of four when the average ADC reading is lower than nearly a quarter of the ADC full scale value (see *Figure 8* for details), this continues until the maximum 128µA pullup current is reached. The final measurement result is reported in the ADCResultAvg/Min/Max[7:0] and IpuResult[1:0] register bits.

To address the intrinsic resistive measurement errors of the MAX20342, ADC shift factors are set and the device compares the ADC average reading to the threshold of (0x3F - ADC shift factor) when deciding whether or not to increase the pullup current by a factor of four. This helps prevent clamping the average ADC reading when the pullup current is increased prematurely due to the measurement errors (quantified by the RSBU_ACC and RCCCD_ACC parameters in the ECT).

The parameters ADCSBUCorrNum[4:0], RSBU_ACC, RSBU_RNG, and RSBU_RNG_GND apply when only the SBU1 and/or SBU2 pins are pulled up. In specific, these parameters always apply in accessory mode detection. For moisture detection, these parameters only apply in the following cases: during two of the four burst measurements (when SBU1 and SBU2 are pulled up), and when only SBU1 and/or SBU2 (not any other pins) are pulled up in Manual Configuration. In all the other moisture detection cases, the parameters ADCCorrNum[5:0], RCCCD_ACC, RCCCD_RNG, and RCCCD_RNG_GND apply.

### Open/Ground/Abort/Finite Result

The flow of the resistive measurement is depicted in Figure 8. There are four possible results for each measurement, namely Open, Ground, Abort, and Finite:

**Open:** If the resistance on the node is open, the final imposed pullup current should be 2µA, while ADCResultMax[7:0] and ADCResultAvg[7:0] clamp at 0xFF (assuming ADCNoiseClampRng[5:0] is set to 0x00, as it should be in most cases). The Open result is reported with IpuResult[1:0] = 00 and ADCResultAvg/Min/Max = 0xFF.

**Ground:** If the resistance on the node is ground, the final imposed pullup current should be 128µA and the average ADC reading should be lower or equal than ADCGroundVth[3:0]. The Ground result is reported with IpuResult[1:0] = 11 and ADCResultAvg/Min/Max = 0x00.

**Abort:** If the resistive measurement returns one of the two listed results, it retries for up to ADCRetryNum[3:0] times. If the same result is returned for ADCRetryNum[3:0] times, the Abort result is reported with IputResult[1:0] = 00 and ADCResultAvg/Min/Max = 0x00. Abort indicates that the device is unable to determine the resistance due to unfiltered noise or uncorrected measurement error on the node. It is not expected to occur in most applications.

1. (ADCResultMax[7:0] = 0xFF) AND (IputResult[1:0] = 2µA) AND (ADCResultAvg[7:0] < (0xFF - ADCNoiseClampRng[5:0]))
2. (ADCResultMax[7:0] = 0xFF) AND (IputResult[1:0] = 8µA, 32µA, or 128µA)

**Finite:** The Finite resistance is reported if one of the two listed conditions is met. ADC_shift factor is equal to ADCSBUCorrNum[4:0] when only SBU1 and/or SBU2 are pulled up and equal to ADCCorrNum[5:0] in other cases. The detected resistance can be calculated with the final imposed current reflected in IpuResult[1:0], the sensed voltage reflected in ADCResultAvg[7:0], and the LSB of the ADC: R = ADCResultAvg[7:0] x LSB / IpuResult[1:0].

1. (ADCResultAvg[7:0] > (0x3F – ADC shift factor)) AND (ADCResultMax[7:0] < 0xFF)
2. (ADCResultAvg[7:0] ≤ (0x3F – ADC shift factor)) AND (ADCResultAvg[7:0] > ADCGroundVth[3:0] AND IputResult[1:0] = 128µA)

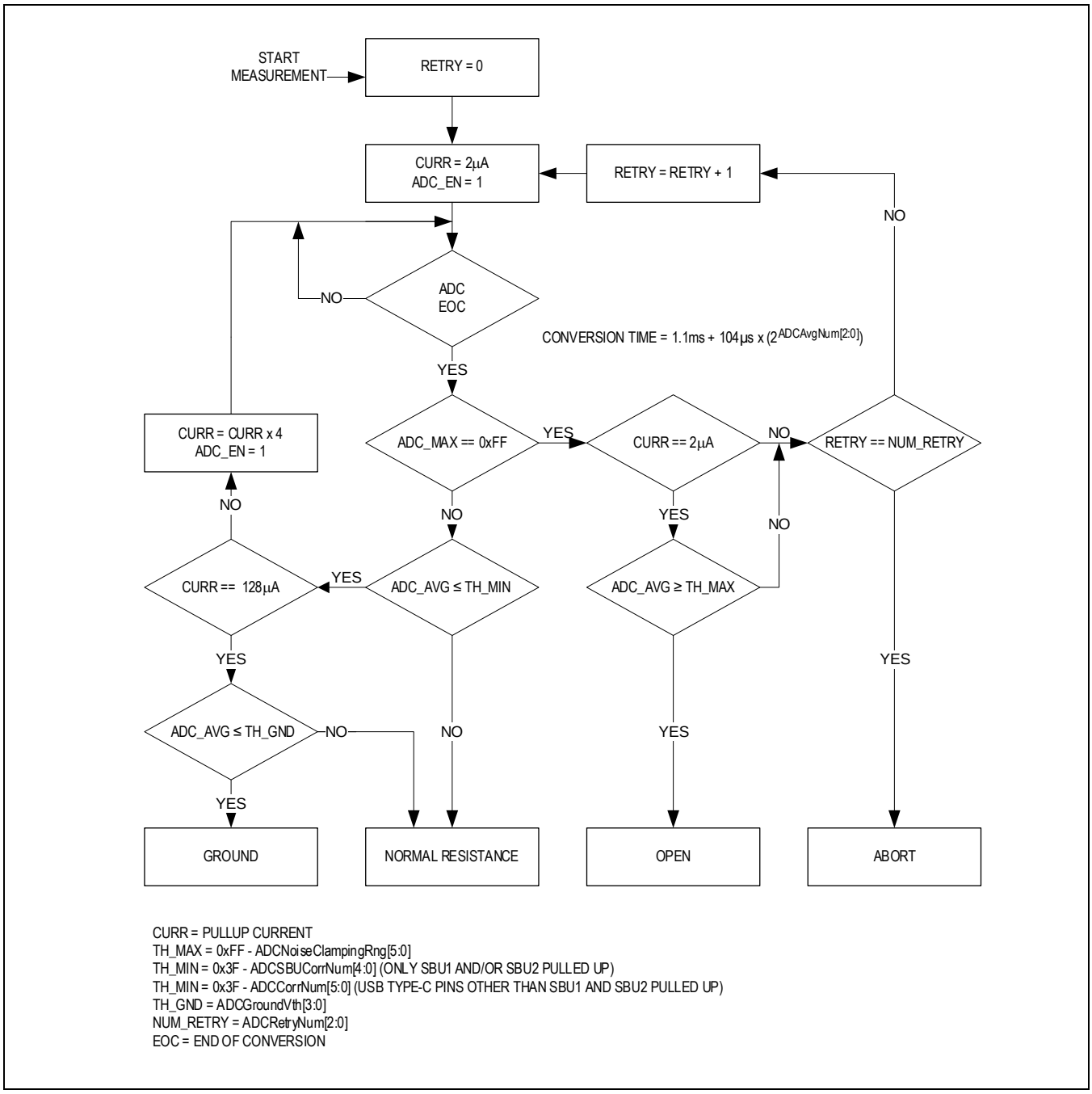



*Figure 8. Resistive Measurement Flow*

**Moisture Detection and Accessory Mode Detection Auto-Detectable Resistances and Voltage Thresholds Setting**

The allowed ranges from which the user can pick the target resistance values to be automatically detected are shown in *Table 7* and *Table 8*.

To account for the resistance measurement errors ($R_{SBU\_ACC}$ and $R_{CCCD\_ACC}$), the moisture detection voltage threshold, RMoistDetVth[7:0], must be set with the corresponding accuracy percentage with the chosen pullup current. For the accessory mode detection, the minimum and maximum voltage thresholds, RAcc_DetVMin[7:0] and RAcc_DetVMax[7:0], for each of the five accessory modes also need to be adjusted with the corresponding accuracy percentage with the chosen pullup current. If the resistor on the SBU1 (or SBU2) has additional tolerance, error band RBAND needs to be widened by decreasing RAcc_DetVMin[7:0] and increasing RAcc_DetVMax[7:0] to account for the additional resistance variat

## Table 7. Auto Detectable Resistance Ranges and Accuracies - Accessory Mode Detection and Moisture Detection When Only SBU1 and/or SBU2 Are Pulled Up

| Pullup Current | Auto Detectable Resistance Range $R_{SBU\_RNG}$ | | Resistance Measurement Accuracy $R_{SBU\_ACC}$ | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 2µA | 187.5kΩ | 714.7kΩ | -4.70% | +4.70% |
| 8µA | 46.88kΩ | 170.2kΩ | -4.70% | +4.70% |
| 32µA | 11.72kΩ | 42.57kΩ | -4.70% | +4.70% |
| 128µA | 2.93kΩ | 10.64kΩ | -4.70% | +4.70% |

For example, to detect an accessory resistance value of 30kΩ, perform the following procedure:

- The target resistance is 30kΩ. Use *Table 7* to find the resistance range and measurement accuracy in which 30kΩ falls into. In this example, the target resistance belongs to the 32µA pullup current range.
- Compute the typical voltage target: 30kΩ x 32µA = 0.96V.
- Since only SBU pins are pulled up, RSBU_ACC applies, namely the combined accuracy of the ADC and the 32µA pullup current (see *Table 7*). Compute the minimum and maximum accessory mode detection voltage thresholds with the measurement accuracy (4.75%).
- Minimum threshold: 0.96V x (1 – 4.70%) = 0.91488V. With conversion, RAcc_DetVMin[7:0] = 155 = 0x9B.
- Maximum threshold: 0.96V x (1 + 4.70%) = 1.00512V. With conversion, RAcc_DetVMax[7:0] = 171 = 0xAB.
- The calculation refers to an ideal external resistance with zero tolerance. In practice, decreasing the minimum and increasing the maximum voltage thresholds by an amount dictated by the actual tolerance is necessary.
- With an external resistor (1% tolerance), the minimum and maximum voltage thresholds would be:
- Minimum threshold: 0.91488V x (1 – 1%) = 0.90573V. With conversion, RAcc_DetVMin[7:0] = 153 = 0x99.
- Maximum threshold: 1.00512V x (1 + 1%) = 1.01517V. With conversion, RAcc_DetVMax[7:0] = 173 = 0xAD.

## Table 8. Auto Detectable Resistance Ranges and Accuracies - Moisture Detection in Other Cases

| PULLUP CURRENT | AUTO DETECTABLE RESISTANCE RANGE $R_{CCCD\_RNG}$ | | RESISTANCE MEASUREMENT ACCURACY $R_{CCCD\_ACC}$ | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 2µA | 187.5kΩ | 672.6kΩ | -10.31% | +10.31% |
| 8µA | 46.88kΩ | 149.7kΩ | -5.81% | +5.81% |
| 32µA | 11.72kΩ | 39.30kΩ | -5.44% | +5.44% |
| 128µA | 2.93kΩ | 9.86kΩ | -5.13% | +5.13% |

For example, to detect a moisture resistance threshold of 20kΩ, perform the following procedure (the CC1 or CC2 pin is pulled up):

- The target resistance is 20kΩ. Use **Table 8** to find the resistance range and measurement accuracy in which 20kΩ falls into. In this example, the target resistance belongs to the 32µA pullup current range.
- Compute the typical voltage target: 20kΩ x 32µA = 0.64V.
- Since pin(s) different from SBU1 and/or SBU2 only (i.e., CC1 and CC2) are pulled up, RCCCD_ACC applies, namely the combined accuracy of the ADC and the 32µA pullup current (see **Table 8**). Compute the minimum moisture detection voltage threshold with the measurement accuracy (5.44%).
- Moisture threshold: 0.64V x (1 – 5.44%) = 0.60518V. With conversion, RMoistDetVth[7:0] = 102 = 0x66.
- The calculation refers to an ideal external resistance with zero tolerance. In practice, decreasing the moisture detection voltage threshold by an amount dictated by the actual tolerance is necessary.
- With an external resistor (1% tolerance), the moisture threshold would be 0.60518V x (1 – 1%) = 0.59913V. With conversion, RMoistDetVth[7:0] = 101 = 0x65.

**Ground Threshold for Accessory Mode Detection and Moisture Detection**

The actual resistance ground condition ranges, $R_{SBU\_RNG\_GND}$ and $R_{CCCD\_RNG\_GND}$, are determined by setting ADCGroundVth[3:0] with the following formulas:

$R_{SBU\_RNG\_GND}$ = [ 5.823mV x (ADCGroundVth[3:0] – 1) – 4.35mV ] / 131.059µA

$R_{CCCD\_RNG\_GND}$ = [ 5.823mV x (ADCGroundVth[3:0] – 1) – 4.35mV ] / 131.600µA

For example, the default of ADCGroundVth[3:0] is 0b0100 or decimal 4. Therefore:

$R_{SBU\_RNG\_GND}$ = [ 5.823mV x (4 – 1) – 4.35mV ] / 131.059µA = 100.11Ω (The ECT value)

$R_{CCCD\_RNG\_GND}$ = [ 5.823mV x (4 – 1) – 4.35mV ] / 131.600µA = 99.70Ω (The ECT value)

## $V_B$ Overvoltage Protection

The device features overvoltage protection up to +28V on the $V_B$ line. If the input voltage exceeds the overvoltage lockout threshold ($V_{B\_OVLO}$), the low 50mΩ (typ) on-resistance internal FET disconnects $V_B$ from OUT to protect low-voltage systems against voltage faults. The device features soft-start capability to minimize inrush current by slowly turning the internal FET on when the $V_B$ voltage is valid for a period longer than the debounce time ($t_{VBFLT\_DEB}$). When an overvoltage event occurs, the fault flag or interrupt is asserted depending on the INTEn configuration in the COMM_CTRL1 register.

## USB Data Switch (TDN/TDP)

The device supports Hi-Speed, full-speed, and low-speed USB signal levels. The USB channel is bidirectional and has low $R_{ON\_TD}$ 3.2Ω (typ) on-resistance and $C_{ON\_TD}$ 4.5pF (typ) on-capacitance. The low on-resistance is stable as the analog input signals are swept from ground to 5.5V for low signal distortion.

## UART Switch (UT, UR)

The MAX20342 supports standard single-supply UART signals. The UART channel supports high-speed signals. The UART channel is bidirectional and has a $R_{ON\_U}$ 23Ω (typ) on-resistance.

## Fault State

The device enters the Fault state when there is either an overvoltage condition on BAT ($V_{BAT} > V_{BAT\_OVLO}$) or a thermal condition ($T_{DIE} > T_{SHDN}$). In either condition, the FAULT bit (bit 7 of register 0x07) becomes 1. After the device exits the overvoltage and thermal conditions, the FAULT bit remains asserted and the user needs to clear it by writing 1 to the FaultUnlock bit (bit 0 of register 0x19) to resume normal operation.

## Thermal Shutdown

The MAX20342 features a thermal shutdown protection feature to protect the device from fault conditions. When the die temperature is $T_{SHDN}$, the device enters thermal shutdown mode and the fault flag or interrupt is asserted depending on the INTEn configuration in the COMM_CTRL1 register. When the die temperature drops below 150°C (typ), the user can write 1 to the FaultUnlock bit to clear the FAULT status bit and resume operation.

## Supply Voltage Selector

The MAX20342 features an internal supply voltage selector that chooses between $V_B$ and BAT inputs to power the internal blocks. If $V_B$ is not present, the internal power supply, $V_{CCINT}$, is supplied from BAT. A typical 100µs POR is provided at the rising edge of $V_{CC}$. When the device is connected to $V_B$, the user can force the device to use BAT as the supply of $V_{CC}$ through the COMM_CTRL1 register VCCINTOnBAT bit.

## Low-Power Modes

To minimize power consumption, the MAX20342 supports three different low power modes: shutdown (ShdnMode), low-power UFP (LPUFP), and low-power DRP (LPDRP). Shutdown is the lowest power consumption mode. LPUFP has the UFP emulation on. LPDRP has the DRP emulation on.

### Shutdown

To minimize power consumption to the lowest possible level when inactive, the MAX20342 features a low-power shutdown mode that is activated through the register COMM_CTRL1 ShdnMode enable bit in the I²C interface. When ShdnMode = 1, the device enters low-power state, and the battery current is reduced to $I_{BAT\_SHDN}$. In this condition, the only blocks that are active are the I²C interface and the CC pin monitoring to detect the charger connection. All other blocks are disabled. On the I²C bus, the device exits shutdown mode when a logic-low is detected on either SDA or SCL for more than 50ns (typ).

## Interrupts

The MAX20342 generates an interrupt for any bit status change in the I²C status register. The INTEn bit enables the interrupt output. When INTEn is disabled, all interrupts are masked but not cleared. The $\overline{INT}$ pin is defaulted as a flag function when the interrupt is disabled (INTEn = 0). In this condition, the $\overline{INT}$ pin is pulled low when an invalid or an unknown charger is inserted or when a UART factory cable is detected.

## I²C Interface

The MAX20342 contains an $I_2C$-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 1000kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

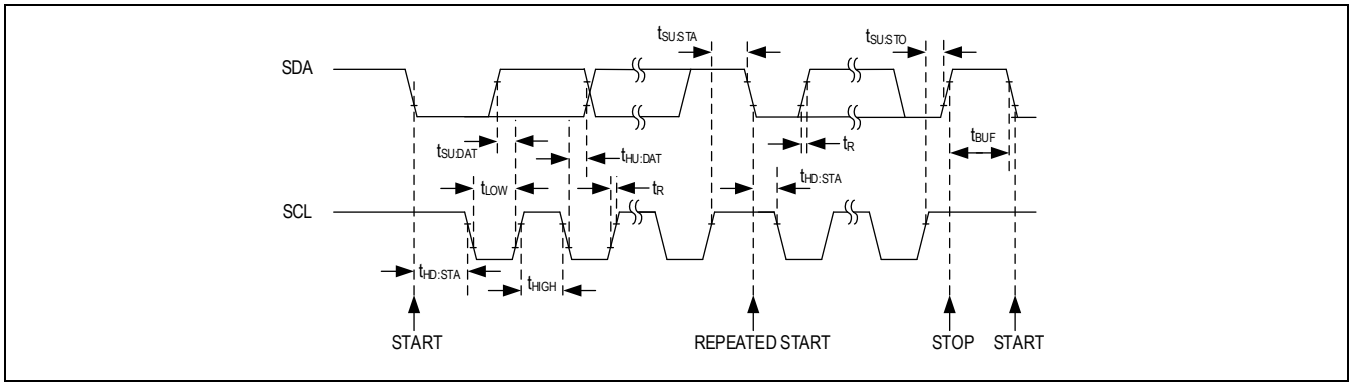



*Figure 9. I²C Interface Timing*

When writing to the MAX20342 using the I²C interface, the master sends a START condition (S) followed by the MAX20342 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave.

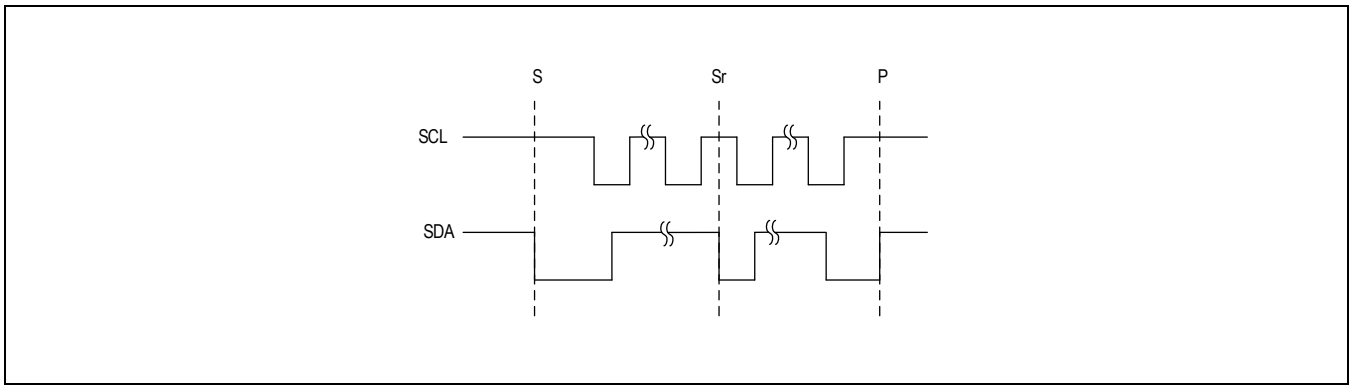



*Figure 10. I²C START, STOP, and REPEATED START Conditions*

## Slave Address

The MAX20342 slave address is 0b0110101 (0x35) plus the Read/Write bit. Set the Read/Write bit high to configure the MAX20342 to read mode (0x6B). Set the Read/Write bit low to configure the MAX20342 to write mode (0x6A).

## Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see **Figure 10**). Both SDA and SCL remain high when the bus is not active.

## Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device. The following procedure describes the single byte write operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends 8 data bits.
7. The slave asserts an ACK on the data line.
8. The master generates a STOP condition.

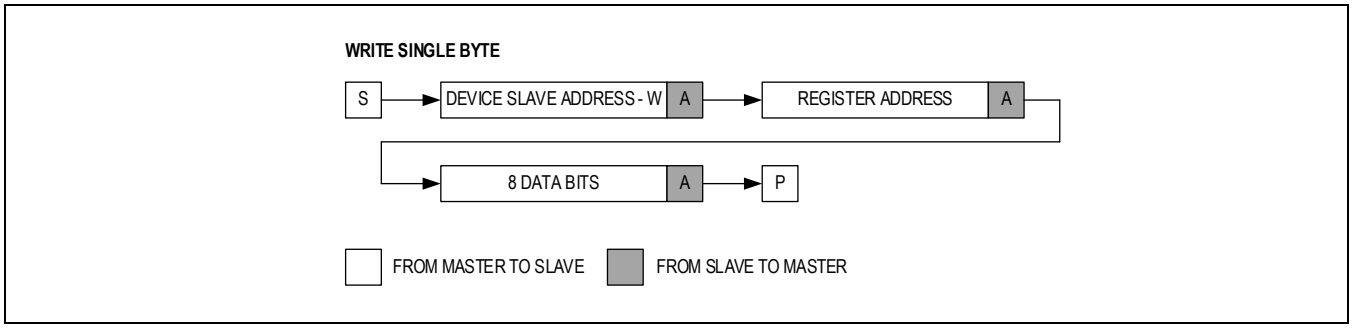



*Figure 11. Write Byte Sequence*

### Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device. The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends 8 data bits.
7. The slave asserts an ACK on the data line.
8. Repeat step 6 and step 7 N-1 times.
9. The master generates a STOP condition.

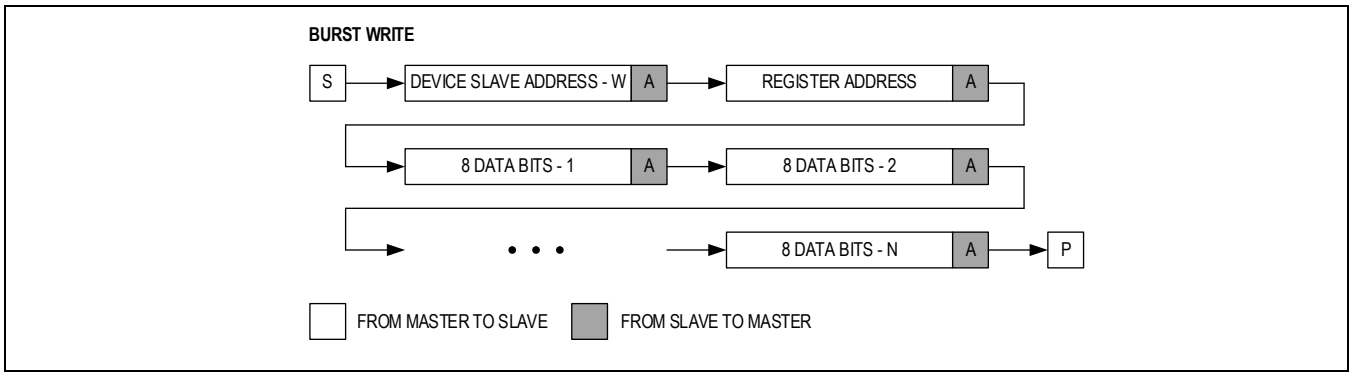



*Figure 12. Burst Write Sequence*

### Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device. The following procedure describes the single byte read operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address plus a read bit (high).
8. The addressed slave asserts an ACK on the data line.
9. The slave sends 8 data bits.
10. The master asserts a NACK on the data line.
11. The master generates a STOP condition.

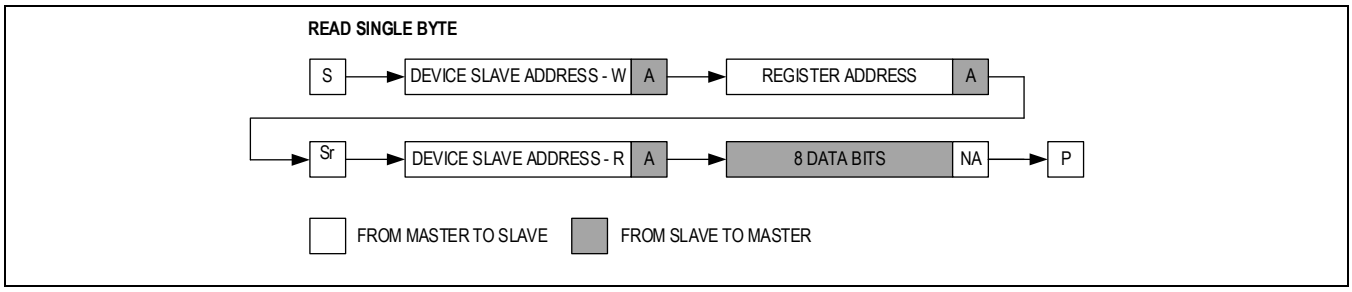



*Figure 13. Read Byte Sequence*

## Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device. The following procedure describes the burst byte read operation:

1. The master sends a START condition.
2. The master sends the 7-bit slave address plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address plus a read bit (high).
8. The slave asserts an ACK on the data line.
9. The slave sends 8 data bits.
10. The master asserts an ACK on the data line.
11. Repeat step 9 and step 10 N-2 times.
12. The slave sends the last 8 data bits.
13. The master asserts a NACK on the data line.
14. The master generates a STOP condition.

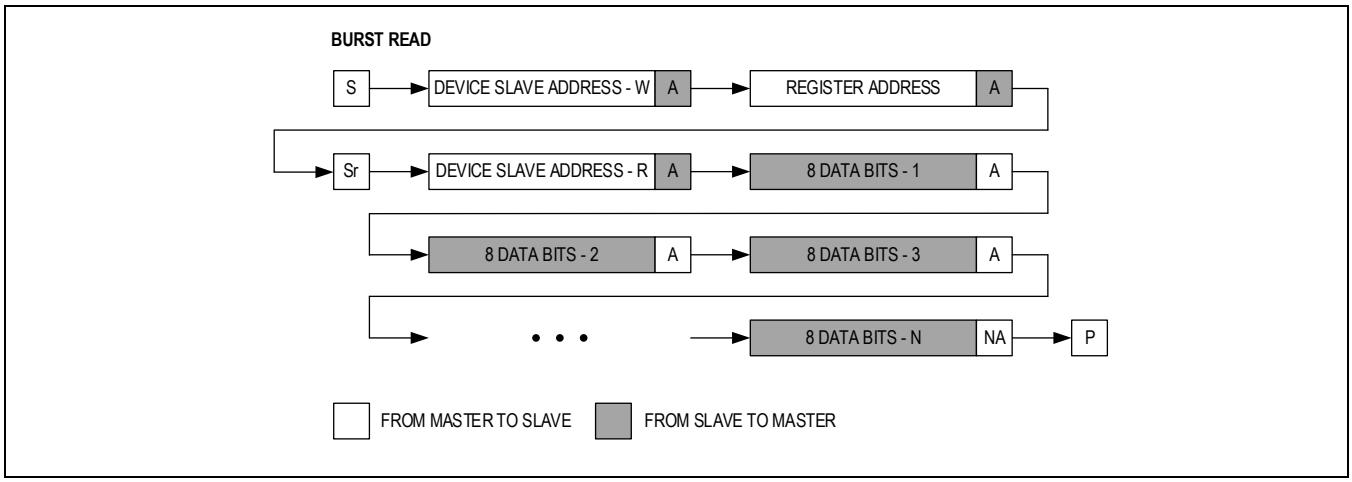



*Figure 14. Burst Read Sequence*

### Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20342 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse. To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

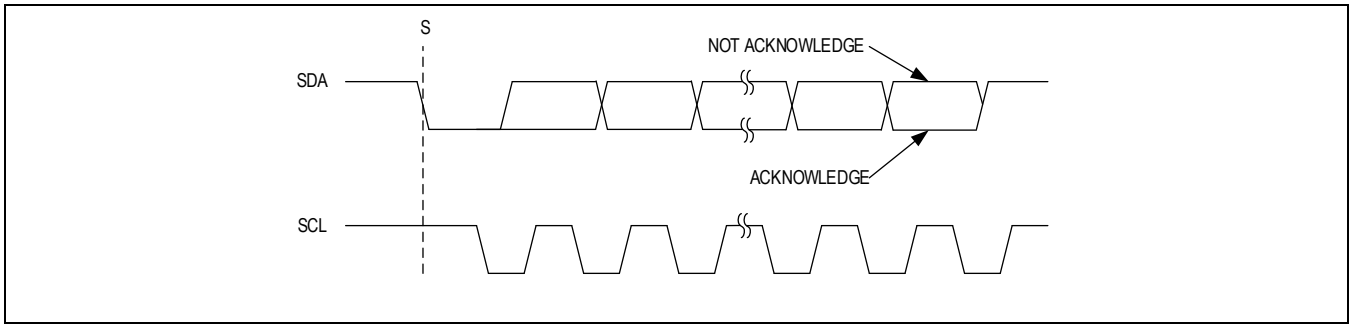



*Figure 15. Acknowledge Bits*

## Register Map

### MAX20342

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| **USER_INTERRUPTS** | | | | | | | | | |
| 0x00 | REVISION_ID[7:0] | Revision_id[7:0] | | | | | | | |
| 0x01 | COMMON_INT[7:0] | FAULTInt | BatOVLOInt | BatUVLOInt | THMInt | LowPwrInt | ShdnWakeInt | VSAFE0VInt | VBvalidInt |
| 0x02 | CC_INT[7:0] | – | – | CCStatInt | CCPinStatInt | CCIStatInt | CCVcnStatInt | VCONNOCPInt | DetAbrtInt |
| 0x03 | BC_INT[7:0] | – | – | – | ChgTypInt | PrChgTypInt | CHgDetRunRInt | CHgDetRunFInt | DCDTmoInt |
| 0x04 | OVP_INT[7:0] | – | – | – | – | – | – | SwtClosedInt | OVLOInt |
| 0x05 | RES_INT1[7:0] | – | – | – | ResAcc5Int | ResAcc4Int | ResAcc3Int | ResAcc2Int | ResAcc1Int |
| 0x06 | RES_INT2[7:0] | – | – | ResGroundInt | ResSBUInt | ResFiniteInt | ResOpenInt | ResAbortInt | ResMoistInt |
| 0x07 | COMMON_STATUS[7:0] | FAULT | BatOVLO | BatUVLO | THM | LowPwr | – | VSAFE0V | VBvalid |
| 0x08 | CC_STATUS1[7:0] | – | – | – | – | VCONNSC | CCVcnStat | VCONNOCP | ChgDetAbort |
| 0x09 | CC_STATUS2[7:0] | – | CCStat[2:0] | | | CCPinStat[1:0] | | CCIStat[1:0] | |
| 0x0A | BC_STATUS[7:0] | – | ChgTyp[1:0] | | PrChgTyp[2:0] | | | CHgDetRun | DCDTmo |
| 0x0B | OVP_STATUS[7:0] | ItfRdy | – | – | – | – | – | SwtClosed | OVLO |
| 0x0C | COMMON_MASK[7:0] | FAULTM | BatOVLOM | BatUVLOM | THMM | LowPwrM | ShdnWakeM | VSAFE0VM | VBvalidM |
| 0x0D | CC_MASK[7:0] | – | – | CCStatM | CCPinStatM | CCIStatM | CCVcnStatM | VCONNOCPM | DetAbrtM |
| 0x0E | BC_MASK[7:0] | – | – | – | ChgTypM | PrChgTypM | CHgDetRunRM | CHgDetRunFM | DCDTmoM |
| 0x0F | OVP_MASK[7:0] | – | – | – | – | – | – | SWT_closedM | OVLOM |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 0x10 | RES_MASK1[7:0] | – | – | – | ResAcc5IntM | ResAcc4IntM | ResAcc3IntM | ResAcc2IntM | ResAcc1IntM |
| 0x11 | RES_MASK2[7:0] | – | – | ResGroundIntM | ResSBUIntM | ResFiniteIntM | ResOpenIntM | ResAbortIntM | ResMoistIntM |
| **USER_COMMON** | | | | | | | | | |
| 0x15 | COMM_CTRL1[7:0] | INTEn | FactAuto | USBAuto | AudioCPEn | VCCINTOnBAT | LPDRP | LPUFP | ShdnMode |
| 0x16 | COMM_CTRL2[7:0] | USBSWC[1:0] | | NotUSBCmpl | DB | DBFrc | – | CE | CEFrc |
| 0x17 | RFU_RW[7:0] | – | – | – | – | – | – | – | – |
| 0x18 | RFU_RO[7:0] | – | – | – | – | – | – | – | – |
| 0x19 | COMM_CTRL3[7:0] | – | – | – | – | – | – | SwReset | FaultUnlock |
| **USER_OVP** | | | | | | | | | |
| 0x1A | OVP_CTRL[7:0] | – | – | – | VBPDEn | VBPDTmr[1:0] | | VBOVPEn[1:0] | |
| **USER_USBC** | | | | | | | | | |
| 0x20 | CC_CTRL0[7:0] | – | – | CCSrcCurCh | CCForceError | SnkAttachedLock | CCVcnSwp | CCSrcRst | CCSnkRst |
| 0x21 | CC_CTRL1[7:0] | CCVcnEn | CCTrySnkEn | – | CCDbgSrcEn | CCDbgSnkEn | CCAudEn | CCSrcEn | CCSnkEn |
| 0x22 | CC_CTRL2[7:0] | – | CCSrcCurAd[1:0] | | CCLpModeSel[1:0] | | CCRpCtrl[2:0] | | |
| 0x23 | CC_CTRL3[7:0] | – | – | RSVD | RSVD | – | – | – | CCDetEn |
| 0x24 | CC_CTRL4[7:0] | – | – | TryWaitShortDeb | CCErrorLock | – | – | ccDRPPhase[1:0] | |
| 0x25 | CC_CTRL5[7:0] | – | – | – | – | – | – | VBMask | ccSnkExitEn |
| 0x26 | CC_CTRL6[7:0] | – | CCLadderDis | – | – | – | – | tQDebounce2[1:0] | |
| 0x28 | VCONN_ILIM[7:0] | – | – | – | CCVcnOcpEn | VCONN_ILIM[3:0] | | | |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| **USER_BC12** | | | | | | | | | |
| 0x2A | BC_CTRL0[7:0] | – | – | – | – | – | – | – | ChgDetMan |
| 0x2B | BC_CTRL1[7:0] | DCDTmo | – | – | DCP3PDet | RSVD | – | – | ChgDetEn |
| **SBUDetResult** | | | | | | | | | |
| 0x2C | SBU1DetResult1[7:0] | SBUDetAbortPriority | – | – | SBU1DetGround | SBU1DetAbort | SBU1DetOpen | SBU1DetIpu[1:0] | |
| 0x2D | SBU1DetResult2[7:0] | SBU1DetVADC[7:0] | | | | | | | |
| 0x2E | SBU2DetResult1[7:0] | – | – | – | SBU2DetGround | SBU2DetAbort | SBU2DetOpen | SBU2DetIpu[1:0] | |
| 0x2F | SBU2DetResult2[7:0] | SBU2DetVADC[7:0] | | | | | | | |
| **SBUDetConfig** | | | | | | | | | |
| 0x30 | SBUDetCtrl[7:0] | – | – | – | – | – | SBUDetContEn | SBUDetOneShotEn | SBUDetManEn |
| 0x31 | RAcc1DetVMax[7:0] | RAcc1DetVMax[7:0] | | | | | | | |
| 0x32 | RAcc1DetVMin[7:0] | RAcc1DetVMin[7:0] | | | | | | | |
| 0x33 | RAcc1DetIpu[7:0] | – | – | – | – | – | – | RAcc1DetIpu[1:0] | |
| 0x34 | RAcc2DetVMax[7:0] | RAcc2DetVMax[7:0] | | | | | | | |
| 0x35 | RAcc2DetVMin[7:0] | RAcc2DetVMin[7:0] | | | | | | | |
| 0x36 | RAcc2DetIpu[7:0] | – | – | – | – | – | – | RAcc2DetIpu[1:0] | |
| 0x37 | RAcc3DetVMax[7:0] | RAcc3DetVMax[7:0] | | | | | | | |
| 0x38 | RAcc3DetVMin[7:0] | RAcc3DetVMin[7:0] | | | | | | | |
| 0x39 | RAcc3DetIpu[7:0] | – | – | – | – | – | – | RAcc3DetIpu[1:0] | |
| 0x3A | RAcc4DetVMin[7:0] | RAcc4DetVMin[7:0] | | | | | | | |
| 0x3B | RAcc4DetVMax[7:0] | RAcc4DetVMax[7:0] | | | | | | | |
| 0x3C | RAcc4DetIpu[7:0] | – | – | – | – | – | – | RAcc4DetIpu[1:0] | |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 0x3D | RAcc5DetVMax[7:0] | RAcc5DetVMax[7:0] | | | | | | | |
| 0x3E | RAcc5DetVMin[7:0] | RAcc5DetVMin[7:0] | | | | | | | |
| 0x3F | RAcc5DetIpu[7:0] | – | – | – | – | – | – | RAcc5DetIpu[1:0] | |
| **MoistDet** | | | | | | | | | |
| 0x50 | RMoistDetVth[7:0] | RMoistDetVth[7:0] | | | | | | | |
| 0x51 | MoistDetCtrl[7:0] | – | – | – | MoistDetAutoCfg | MoistDetPerEn | MoistDetManEn | RMoistDetIpu[1:0] | |
| 0x52 | MoistDetPUConfig[7:0] | – | – | MoistDetPUConfig[5:0] | | | | | |
| 0x53 | MoistDetPDConfig[7:0] | – | MoistDetPDConfig[6:0] | | | | | | |
| 0x54 | MoistDetAutoCC1Result1[7:0] | – | – | – | CC1MoiGnd | CC1MoiAbrt | CC1MoiOpn | CC1MoistIpu[1:0] | |
| 0x55 | MoistDetAutoCC1Result2[7:0] | CC1MoistVADC[7:0] | | | | | | | |
| 0x56 | MoistDetAutoCC2Result1[7:0] | – | – | – | CC2MoiGnd | CC2MoiAbrt | CC2MoiOpn | CC2MoistIpu[1:0] | |
| 0x57 | MoistDetAutoCC2Result2[7:0] | CC2MoistVADC[7:0] | | | | | | | |
| 0x58 | MoistDetAutoSBU1Result1[7:0] | – | – | – | SBU1MoiGnd | SBU1MoiAbrt | SBU1MoiOpn | SBU1MoistIpu[1:0] | |
| 0x59 | MoistDetAutoSBU1Result2[7:0] | SBU1MoistVADC[7:0] | | | | | | | |
| 0x5A | MoistDetAutoSBU2Result1[7:0] | – | – | – | SBU2MoiGnd | SBU2MoiAbrt | SBU2MoiOpn | SBU2MoistIpu[1:0] | |
| 0x5B | MoistDetAutoSBU2Result2[7:0] | SBU2MoistVADC[7:0] | | | | | | | |
| **ADCConfig** | | | | | | | | | |
| 0x5C | ADCCtrl1[7:0] | – | ADCGroundVth[3:0] | | | | ADCRetryNum[2:0] | | |
| 0x5D | ADCCtrl2[7:0] | IpuResult[1:0] | | ADCCorrNum[5:0] | | | | | |
| 0x5E | ADC_CTRL3[7:0] | ADCAvgNum[2:0] | | | ADCSBUCorrNum[4:0] | | | | |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 0x5F | ADC_CTRL4[7:0] | – | – | ADCNoiseClampRng[5:0] | | | | | |
| 0x60 | ADCResultAvg[7:0] | ADCResultAvg[7:0] | | | | | | | |
| 0x61 | ADCResultMax[7:0] | ADCResultMax[7:0] | | | | | | | |
| 0x62 | ADCResultMin[7:0] | ADCResultMin[7:0] | | | | | | | |
| **USER_VB** | | | | | | | | | |
| 0x63 | VB_CTRL[7:0] | – | – | – | – | – | – | ACTIV_DISCH_EN | – |

Register Details

## REVISION_ID (0x00)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | Revision_id[7:0] | | | | | | | |
| **Reset** | 0x1 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| Revision_id | 7:0 | Information about the hardware revision. |

## COMMON_INT (0x01)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | FAULTInt | BatOVLOInt | BatUVLOInt | THMInt | LowPwrInt | ShdnWakeInt | VSAFE0VInt | VBvalidInt |
| **Reset** | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FAULTInt | 7 | Fault Status Interrupt Bit. Asserted for any fault status change.<br><br>0b0: No fault status change<br>0b1: New fault status interrupt |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| BatOVLOInt | 6 | Battery Overvoltage Status Bit Interrupt<br><br>0b0: No interrupt<br>0b1: New BatOVLO status interrupt |
| BatUVLOInt | 5 | Battery Undervoltage Status Bit Interrupt<br><br>0b0: No interrupt<br>0b1: New BatUVLO status interrupt |
| THMInt | 4 | Thermal Shutdown Interrupt<br><br>0b0: No interrupt<br>0b1: New THM status interrupt |
| LowPwrInt | 3 | Low Power Mode Status Change Interrupt<br><br>0b0: No interrupt<br>0b1: New LowPwr status interrupt |
| ShdnWakeInt | 2 | Shutdown Mode Wake Up Interrupt. It is set upon exiting from shutdown due to toggling the I²C interface or something attached to the USB Type-C port<br><br>0b0: No exit from shutdown<br>0b1: Exit from shutdown |
| VSAFE0VInt | 1 | $V_{SAFE0V}$ Interrupt<br><br>0b0: No interrupt<br>0b1: New $V_{SAFE0V}$ status interrupt |
| VBvalidInt | 0 | $V_B$ Valid Range Detection Interrupt<br><br>0b0: $V_B < V_{BDET}$ or $V_B > V_{B\_OVLO}$<br>0b1: $V_B > V_{BDET}$ and $V_B < V_{B\_OVLO}$ |

## CC_INT (0x02)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | CCStatInt | CCPinStatInt | CCIStatInt | CCVcnStatInt | VCONNOCPInt | DetAbrtInt |
| **Reset** | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCStatInt | 5 | CC State Interrupt<br><br>0b0: No interrupt<br>0b1: New CCStat status interrupt |
| CCPinStatInt | 4 | CC Pin State Interrupt<br><br>0b0: No interrupt<br>0b1: New CCPinStat status interrupt |
| CCIStatInt | 3 | CCIStat Interrupt<br><br>0b0: No interrupt<br>0b1: New CCIStat status interrupt |
| CCVcnStatInt | 2 | CCVcnStat Interrupt<br><br>0b0: No interrupt<br>0b1: New CCVcnStat status interrupt |
| VCONNOCPInt | 1 | $V_{CONN}$ Overcurrent Protection Interrupt<br><br>0b0: No interrupt<br>0b1: New VCONNOCP status interrupt |
| DetAbrtInt | 0 | Charger Detection Abort Interrupt<br><br>0b0: No interrupt<br>0b1: New charger detection abort interrupt |

## BC_INT (0x03)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | ChgTypInt | PrChgTypInt | CHgDetRunRInt | CHgDetRunFInt | DCDTmoInt |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ChgTypInt | 4 | Charger Type Interrupt<br><br>0b0: No interrupt<br>0b1: New ChgTyp status interrupt |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| PrChgTypInt | 3 | Propietary Charger Type Interrupt<br><br>0b0: No interrupt<br>0b1: New PrChgTyp status interrupt |
| CHgDetRunRInt | 2 | Charger Detection Runnning Rising Edge Interrupt<br><br>0b0: No rising edge detected on ChgDetRun<br>0b1: Rising edge detected on ChgDetRun |
| CHgDetRunFInt | 1 | Charger Detection Runnning Falling Edge Interrupt<br><br>0b0: No falling edge detected on ChgDetRun<br>0b1: Falling edge detected on ChgDetRun |
| DCDTmoInt | 0 | DCD Timer Interrupt<br><br>0b0: No interrupt<br>0b1: New DCDTmo status interrupt |

## OVP_INT (0x04)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | SwtClosedInt | OVLOInt |
| **Reset** | – | – | – | – | – | – | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SwtClosedInt | 1 | Status of the $V_B$ Switch Interrupt<br><br>0b0: No interrupt<br>0b1: New $V_B$ switch status interrupt |
| OVLOInt | 0 | $V_B$ Overvoltage Interrupt<br><br>0b0: No interrupt<br>0b1: New overvoltage status interrupt |

## RES_INT1 (0x05)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Field | – | – | – | ResAcc5Int | ResAcc4Int | ResAcc3Int | ResAcc2Int | ResAcc1Int |
|---|---|---|---|---|---|---|---|---|
| Reset | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| Access Type | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ResAcc5Int | 4 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 5 Resistor Result Interrupt<br><br>0b0: SBU1/SBU2 resistor detection Valid Accessory 5 not detected<br>0b1: SBU1/SBU2 resistor detection Valid Accessory 5 detected |
| ResAcc4Int | 3 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 4 Resistor Result Interrupt<br><br>0b0: SBU1/SBU2 resistor detection Valid Accessory 4 not detected<br>0b1: SBU1/SBU2 resistor detection Valid Accessory 4 detected |
| ResAcc3Int | 2 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 3 Resistor Result Interrupt<br><br>0b0: SBU1/SBU2 resistor detection Valid Accessory 3 not detected<br>0b1: SBU1/SBU2 resistor detection Valid Accessory 3 detected |
| ResAcc2Int | 1 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 2 Resistor Result Interrupt<br><br>0b0: SBU1/SBU2 resistor detection Valid Accessory 2 not detected<br>0b1: SBU1/SBU2 resistor detection Valid Accessory 2 detected |
| ResAcc1Int | 0 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 1 Resistor Result Interrupt<br><br>0b0: SBU1/SBU2 resistor detection Valid Accessory 1 not detected<br>0b1: SBU1/SBU2 resistor detection Valid Accessory 1 detected |

## RES_INT2 (0x06)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | ResGroundInt | ResSBUInt | ResFiniteInt | ResOpenInt | ResAbortInt | ResMoistInt |
| Reset | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| Access Type | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ResGroundInt | 5 | Ground Resistive Measurement Result Interrupt<br><br>0b0: Ground resistive value not detected<br>0b1: Ground resistive value detected |
| ResSBUInt | 4 | SBU1/SBU2 Resistor Detection Measurement Result Interrupt<br><br>0b0: SBU1/SBU2 resistor detection measurement not completed<br>0b1: SBU1/SBU2 resistor detection measurement completed |
| ResFiniteInt | 3 | Finite But Not Valid Resistive Measurement Result Interrupt<br><br>0b0: Finite but not valid resistive value not detected<br>0b1: Finite but not valid resistive value detected |
| ResOpenInt | 2 | Open Resistive Measurement Result Interrupt<br><br>0b0: Open resistive value not detected<br>0b1: Open resistive value detected |
| ResAbortInt | 1 | Abort Resistive Measurement Result Interrupt<br><br>0b0: Abort resistive value not detected<br>0b1: Abort resistive value detected |
| ResMoistInt | 0 | Moisture Detection Measurement Valid Result Interrupt<br><br>0b0: Moisture detection valid value not detected<br>0b1: Moisture detection valid value detected |

## COMMON_STATUS (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | FAULT | BatOVLO | BatUVLO | THM | LowPwr | – | VSAFE0V | VBvalid |
| **Reset** | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | – | 0x0 | 0x0 |
| **Access Type** | Read Only | Read Only | Read Only | Read Only | Read Only | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FAULT | 7 | Fault Status Bit. The Finite State Machine enters fault state in the case of a BAT Overvoltage or Thermal fault. Fault state is exited by asserting FaultUnlock bit with no BATOVLO or THM present. |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: Not in fault state<br>0b1: In fault state |
| BatOVLO | 6 | Battery Overvoltage Status Bit<br><br>0b0: $V_{BAT} < V_{BAT\_OVLO}$<br>0b1: $V_{BAT} > V_{BAT\_OVLO}$ |
| BatUVLO | 5 | Battery Undervoltage Status Bit<br><br>0b0: $V_{BAT} > V_{BAT\_UVLO}$<br>0b1: $V_{BAT} < V_{BAT\_UVLO}$ |
| THM | 4 | Thermal Shutdown Status<br><br>0b0: Thermal fault not active<br>0b1: Thermal fault active |
| LowPwr | 3 | Low-Power Mode Status<br><br>0b0: Low-power mode (UFP or DRP) not active<br>0b1: Low-power mode (UFP or DRP) entered |
| VSAFE0V | 1 | Status of $V_B$ Detection<br><br>0b0: $V_B < V_{SAFE0V}$<br>0b1: $V_B > V_{SAFE0V}$ |
| VBvalid | 0 | Status of $V_B$ Valid Range<br><br>0b0: $V_B < V_{BDET}$ or $V_B > V_{B\_OVLO}$<br>0b1: $V_B > V_{BDET}$ and $V_B < V_{B\_OVLO}$ |

## CC_STATUS1 (0x08)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | VCONNSC | CCVcnStat | VCONNOCP | ChgDetAbort |
| **Reset** | – | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| VCONNSC | 3 | $V_{CONN}$ Short Circuit Detection |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: $V_{CONN}$ current < $I_{SCCP\_VCONN\_THR}$<br>0b1: $V_{CONN}$ current > $I_{SCCP\_VCONN\_THR}$ |
| CCVcnStat | 2 | Status of $V_{CONN}$ Output<br><br>0b0: $V_{CONN}$ Disabled<br>0b1: $V_{CONN}$ Enabled |
| VCONNOCP | 1 | $V_{CONN}$ Overcurrent Detection<br><br>0b0: $V_{CONN}$ current < $V_{CONN\_ILIM}$<br>0b1: $V_{CONN}$ current > $V_{CONN\_ILIM}$ |
| ChgDetAbort | 0 | Charger Detection Abort Status<br><br>0b0: CC FSM is not gating BC FSM<br>0b1: CC FSM is gating BC FSM. ChgDetMan allows manual run of charger detection |

## CC_STATUS2 (0x09)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | CCStat[2:0] | | | CCPinStat[1:0] | | CCIStat[1:0] | |
| **Reset** | – | 0x0 | | | 0x0 | | 0x0 | |
| **Access Type** | – | Read Only | | | Read Only | | Read Only | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCStat | 6:4 | CC Pin State Machine Detection<br><br>0b000: No connection<br>0b001: Sink mode<br>0b010: Source mode<br>0b011: Audio accessory mode<br>0b100: Debug accessory source mode<br>0b101: Error<br>0b110: Disabled<br>0b111: Debug accessory sink mode |
| CCPinStat | 3:2 | Status of Active CC Pin<br><br>0b00: No determination<br>0b01: CC1 Active<br>0b10: CC2 Active<br>0b11: RFU |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCIStat | 1:0 | CC Pin Detected and $V_B$ Current Allowed in UFP Mode<br><br>0b00: Not in sink mode<br>0b01: 500mA<br>0b10: 1.5A<br>0b11: 3.0A |

## BC_STATUS (0x0A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | ChgTyp[1:0] | | PrChgTyp[2:0] | | | CHgDetRun | DCDTmo |
| **Reset** | – | 0x0 | | 0x0 | | | 0x0 | 0x0 |
| **Access Type** | – | Read Only | | Read Only | | | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ChgTyp | 6:5 | Output of Charger Detection<br><br>0b00: Nothing attached<br>0b01: SDP, USB cable attached<br>0b10: Charging downstream port (CDP). Current depends on USB operating speed.<br>0b11: Dedicated charger port (DCP). Current ranges up to 1.5A. |
| PrChgTyp | 4:2 | Output of Proprietary Charger Detection<br><br>0b000: Unknown<br>0b001: Samsung 2A<br>0b010: Apple 0.5A<br>0b011: Apple 1A<br>0b100: Apple 2A<br>0b101: Apple 12W<br>0b110: 3A DCP (if enabled and chgTyp = DCP)<br>0b111: Unidentified |
| CHgDetRun | 1 | Charger Detection Run Status<br><br>0b0: No charger detection running<br>0b1: Charger detection running or completed |
| DCDTmo | 0 | During Charger Detection, DCD Detection Timed Out<br>Indicates D+/D- are open. BC1.2 detection continues as required by BC1.2 specification but SDP most likely is found. |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: No timeout or detection has not run<br>0b1: DCD timeout occurred |

## OVP_STATUS (0x0B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ItfRdy | – | – | – | – | – | SwtClosed | OVLO |
| **Reset** | 0x0 | – | – | – | – | – | 0x0 | 0x0 |
| **Access Type** | Read Only | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ItfRdy | 7 | OTP Loading Complete. RegMap ready (reset deasserted).<br><br>0b0: OTP loading not completed<br>0b1: OTP loading completed |
| SwtClosed | 1 | Status of the $V_B$ Switch<br><br>0b0: Open or in soft-start<br>0b1: Closed |
| OVLO | 0 | $V_B$ Overvoltage Condition<br><br>0b0: No $V_B$ overvoltage<br>0b1: $V_B$ overvoltage detected |

## COMMON_MASK (0x0C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | FAULTM | BatOVLOM | BatUVLOM | THMM | LowPwrM | ShdnWakeM | VSAFE0VM | VBvalidM |
| **Reset** | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x1 | 0x0 | 0x0 |
| **Access Type** | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FAULTM | 7 | Fault Status Mask Bit |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: Mask<br>0b1: Unmask |
| BatOVLOM | 6 | Battery Overvoltage Status Bit Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| BatUVLOM | 5 | Battery Undervoltage Status Bit Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| THMM | 4 | Thermal Shutdown Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| LowPwrM | 3 | Low-Power Mode Status Change Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ShdnWakeM | 2 | Shutdown Mode Wake-up Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| VSAFE0VM | 1 | $V_{SAFE0V}$ Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| VBvalidM | 0 | $V_B$ Valid Range Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |

## CC_MASK (0x0D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | CCStatM | CCPinStatM | CCIStatM | CCVcnStatM | VCONNOCPM | DetAbrtM |
| **Reset** | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCStatM | 5 | CCStat Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| CCPinStatM | 4 | CCPinStat Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| CCIStatM | 3 | CCIStat Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| CCVcnStatM | 2 | CCVcnStat Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| VCONNOCPM | 1 | VCONNOCP Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| DetAbrtM | 0 | DetAbrt Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |

## BC_MASK (0x0E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | ChgTypM | PrChgTypM | CHgDetRunRM | CHgDetRunFM | DCDTmoM |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ChgTypM | 4 | ChgTyp Interrupt Mask |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: Mask<br>0b1: Unmask |
| PrChgTypM | 3 | PrChgTyp Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| CHgDetRunRM | 2 | Charger Detection Rising Run Status Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| CHgDetRunFM | 1 | Charger Detection Falling Run Status Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| DCDTmoM | 0 | DCDTmo Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |

## OVP_MASK (0x0F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | SWT_closedM | OVLOM |
| **Reset** | – | – | – | – | – | – | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SWT_closedM | 1 | Status of $V_B$ Switch Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| OVLOM | 0 | $V_B$ Overvoltage Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |

## RES_MASK1 (0x10)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | ResAcc5IntM | ResAcc4IntM | ResAcc3IntM | ResAcc2IntM | ResAcc1IntM |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ResAcc5IntM | 4 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 5 Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResAcc4IntM | 3 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 4 Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResAcc3IntM | 2 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 3 Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResAcc2IntM | 1 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 2 Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResAcc1IntM | 0 | SBU1/SBU2 Resistor Detection Measurement Valid Accessory 1 Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |

## RES_MASK2 (0x11)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | ResGroundIntM | ResSBUIntM | ResFiniteIntM | ResOpenIntM | ResAbortIntM | ResMoistIntM |
| **Reset** | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ResGroundIntM | 5 | Ground Resistive Measurement Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResSBUIntM | 4 | SBU1/SBU2 Resistor Detection Measurement Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResFiniteIntM | 3 | Finite But Not Valid Resistive Measurement result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResOpenIntM | 2 | Open Resistive Measurement Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResAbortIntM | 1 | Abort Resistive Measurement Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |
| ResMoistIntM | 0 | Moisture Detection Measurement Valid Result Interrupt Mask<br><br>0b0: Mask<br>0b1: Unmask |

## COMM_CTRL1 (0x15)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | INTEn | FactAuto | USBAuto | AudioCPEn | VCCINTOnBAT | LPDRP | LPUFP | ShdnMode |
| **Reset** | 0x1 | 0x1 | 0x1 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| INTEn | 7 | Interrupt Enable to INTb<br><br>0b0: INTb acts as a THM, OVP, or autoconfiguration flag<br>0b1: INTb is set as an interrupt output |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FactAuto | 6 | Autoconfiguration Enable Gating. Autoconfiguration FSM starts if USBAuto = 1 or if Debug Acccessory Sink Mode is entered and FactAuto = 1.<br><br>0b0: Debug accessory sink mode gated<br>0b1: Debug accessory sink mode not gated |
| USBAuto | 5 | Autoconfiguration Enable Gating. Autoconfiguration FSM starts if USBAuto = 1 or if Debug Acccessory Sink Mode is entered and FactAuto = 1.<br><br>0b0: USB valid gated<br>0b1: USB valid not gated |
| AudioCPEn | 4 | Enable of the Internal USB Switches Charge Pump to Support Audio Negative Rail<br><br>0b0: USB switches charge pump enable controlled automatically<br>0b1: USB switches charge pump forced enabled |
| VCCINTOnBAT | 3 | $V_{CCINT}$ Switchover Forcing On BAT Side<br><br>0b0: Internal $V_{CCINT}$ switchover is set on the highest between BAT and $V_B$ or on $V_B$ if $V_B > V_{BDET}$<br>0b1: Internal $V_{CCINT}$ switchover forced on BAT unless $V_{BAT} < V_{BAT\_UVLOB}$ |
| LPDRP | 2 | Low-Power DRP Mode Enable<br><br>0b0: No low-power DRP mode enabled<br>0b1: Procedure to enter low-power DRP mode is triggered |
| LPUFP | 1 | Low-Power UFP Mode Enable<br><br>0b0: No low-power UFP mode enabled<br>0b1: Procedure to enter low-power UFP mode is triggered |
| ShdnMode | 0 | Shutdown Mode Enable<br><br>0b0: No shutdown mode enabled<br>0b1: Procedure to enter into shutdown mode is triggered |

## COMM_CTRL2 (0x16)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | USBSWC[1:0] | | NotUSBCmpl | DB | DBFrc | – | CE | CEFrc |
| **Reset** | 0x3 | | 0x0 | 0x0 | 0x0 | – | 0x0 | 0x0 |
| **Access Type** | Write, Read | | Write, Read | Write, Read | Write, Read | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| USBSWC | 7:6 | USB Switch Control<br><br>0b00: All switches open<br>0b01: USB SW to UT/UR position<br>0b10: USB SW to TDP/TDN position<br>0b11: Follow the automatic hardware setting |
| NotUSBCmpl | 5 | Not USB Compliant in Case of SDP Detection. CEb is set low in case of SDP if NotUSBCompl = 1.<br><br>0b0: Compliant<br>0b1: Not compliant |
| DB | 4 | DB Output. With DBFrc = 0, registers are set by the result of charger FSM. With DBFrc = 1, registers are set by I²C command only. DB is the control of open drain output: DBb = !DB |
| DBFrc | 3 | Enable Force DB Outputs |
| CE | 1 | CE Output. With CEFrc = 0, registers are set by the result of charger FSM. With CEFrc = 1, registers are set by I²C command only. CE is the control of open drain output: CEb = !CE |
| CEFrc | 0 | Enable Force CE Outputs<br><br>0b0: CE outputs follow the charger detection FSM<br>0b1: CE outputs follows CEb register regardless of the result from charger detection FSM |

## COMM_CTRL3 (0x19)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | SwReset | FaultUnlock |
| **Reset** | – | – | – | – | – | – | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SwReset | 1 | Software Reset Bit. If set, it forces the part to reboot. This bit is self-cleared after action is completed.<br><br>0b0: Software reset not triggered<br>0b1: Software reset triggered |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FaultUnlock | 0 | Fault Status Unlock. If set, it forces the system to exit from fault state if BATOVLO and THM faults are not present. This bit is self-cleared after action is completed.<br><br>0b0: Fault unlock not triggered<br>0b1: Fault unlock triggered |

## OVP_CTRL (0x1A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | VBPDEn | VBPDTmr[1:0] | | VBOVPEn[1:0] | |
| **Reset** | – | – | – | 0x0 | 0x0 | | 0x2 | |
| **Access Type** | – | – | – | Write, Read | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| VBPDEn | 4 | $V_B$ 8kΩ Discharge Pulldown Enable. The bit is cleared after pulldown timer expires.<br><br>0b0: Pulldown disabled<br>0b1: Pulldown enabled |
| VBPDTmr | 3:2 | $V_B$ 8kΩ Discharge Pulldown Timer Duration<br><br>0b00: 5ms<br>0b01: 15ms<br>0b10: 30ms<br>0b11: 60ms |
| VBOVPEn | 1:0 | $V_B$ Overvoltage Protector (OVP) Enable Control<br><br>0b00: Force OVP switch open<br>0b01: OVP switch closed when $V_B > V_{BDET}$<br>0b10: OVP switch controlled by logic (closed after $V_B$ attach based on Table 4)<br>0b11: OVP switch closed |

## CC_CTRL0 (0x20)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | CCSrcCurCh | CCForceError | SnkAttachedLock | CCVcnSwp | CCSrcRst | CCSnkRst |
| **Reset** | – | – | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Access Type** | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCSrcCurCh | 5 | Source Current Change Request. Request new pullup value to advertise a new allowed max current value while in Source (DFP) mode. Note this bit resets to 0 automatically when action is done.<br><br>0b0: No change request/previous change done<br>0b1: Request value in CCSrcCur to be read/previous change waiting to be in Source Mode (UFP) |
| CCForceError | 4 | Bit Automatically Resets to 0 After Action Is Done<br><br>0b0: No action<br>0b1: Force transition to ErrorRecovery state |
| SnkAttachedLock | 3 | Bit Automatically Resets to 0 After Action Is Done<br><br>0b0: Exit Sink Attached when $V_B < V_{BDET}$ for more than $t_{PDDebounce}$<br>0b1: Locked in Sink Attached for a minimum of 1.1s if $V_B$ is missing |
| CCVcnSwp | 2 | Signal State Machine to Swap $V_{CONN}$ Roles. Bit resets to 0 after a write (Note this bit resets to 0 automatically when action is done)<br><br>0b0: No change in $V_{CONN}$ role<br>0b1: Force change in $V_{CONN}$ |
| CCSrcRst | 1 | Force a Reset of the State Machine – Immediate transition to Unattached.SRC state. Bit resets to 0 after a write (Note this bit resets to 0 automatically when action is done)<br><br>0b0: No reset<br>0b1: Request reset |
| CCSnkRst | 0 | Force a Reset of the State Machine – Immediate Transition to Unattached.SNK State. Bit resets to 0 after a write (Note this bit resets to 0 automatically when action is done)<br><br>0b0: No reset<br>0b1: Request reset |

## CC_CTRL1 (0x21)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | CCVcnEn | CCTrySnkEn | – | CCDbgSrcEn | CCDbgSnkEn | CCAudEn | CCSrcEn | CCSnkEn |
| **Reset** | 0x1 | 0x0 | – | 0x0 | 0x1 | 0x1 | 0x0 | 0x1 |
| **Access Type** | Write, Read | Write, Read | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCVcnEn | 7 | Force State of $V_{CONN}$<br><br>0b0: Force $V_{CONN}$ off<br>0b1: Automatic operation based on State Machine |
| CCTrySnkEn | 6 | Allow Transition to Try.SNK States<br><br>0b0: Try.SNK is disabled<br>0b1: Try.SNK is enabled |
| CCDbgSrcEn | 4 | Enable Detection of USB Type-C Debug Accessory Source Mode<br><br>0b0: Disabled<br>0b1: Enabled |
| CCDbgSnkEn | 3 | Enable Detection of USB Type-C Debug Accessory Sink Mode<br><br>0b0: Disabled<br>0b1: Enabled |
| CCAudEn | 2 | Enable Detection of USB Type-C Audio Adapter<br><br>0b0: Disabled<br>0b1: Enabled |
| CCSrcEn | 1 | Enable Detection of USB Type-C Source Mode<br><br>0b0: Disabled<br>0b1: Enabled |
| CCSnkEn | 0 | Enable Detection of USB Type-C Sink Mode<br><br>0b0: Disabled<br>0b1: Enabled |

## CC_CTRL2 (0x22)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | CCSrcCurAd[1:0] | | CCLpModeSel[1:0] | | CCRpCtrl[2:0] | | |
| **Reset** | – | 0x0 | | 0x0 | | 0x0 | | |
| **Access Type** | – | Write, Read | | Write, Read | | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCSrcCurAd | 6:5 | New Request Value for Source Mode Pullup. Note this value is latched in when CCSrcCurCh bit is written to 1. Changes to the pullup value only take place if the operation state is DFP (CCStat = 0b010).<br><br>0b00: 0.5A Advertised when in Source Mode (DFP)<br>0b01: 1.5A Advertised when in Source Mode (DFP)<br>0b10: 3.0A Advertised when in Source Mode (DFP) (Cannot source 3A on $V_B$. This is only for USB_PD collision avoidance support)<br>0b11: Reserved |
| CCLpModeSel | 4:3 | CC Detection with Low-Power Mode<br><br>0b00 : Normal operation<br>0b01: Use 5.0µA current source in Unattached.SRC state instead of 80µA<br>0b10: Use 1.0µA current source in Unattached.SRC state instead of 80µA |
| CCRpCtrl | 2:0 | Current Source Value to be Forced<br><br>0b000: Current sources driven by state machine<br>0b001: 1µA on CC line not pulled down and not used as $V_{CONN}$<br>0b010: 5µA on CC line not pulled down and not used as $V_{CONN}$<br>0b011: 80µA on CC line not pulled down and not used as $V_{CONN}$<br>0b100: 180µA on CC line not pulled down and not used as $V_{CONN}$<br>0b101: 330µA on CC line not pulled down and not used as $V_{CONN}$<br>0b110, 0b111: No source |

## CC_CTRL3 (0x23)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | RSVD | RSVD | – | – | – | CCDetEn |
| **Reset** | – | – | | | – | – | – | 0x1 |
| **Access Type** | – | – | Write, Read | Write, Read | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RSVD | 5 | Reserved |
| RSVD | 4 | Reserved |
| CCDetEn | 0 | USB Type-C Detection FSM Enable<br><br>0b0: USB Type-C FSM disabled<br>0b1: USB Type-C FSM enabled |

## CC_CTRL4 (0x24)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | TryWaitShortDeb | CCErrorLock | – | – | ccDRPPhase[1:0] | |
| **Reset** | – | – | 0x0 | 0x0 | – | – | 0x0 | |
| **Access Type** | – | – | Write, Read | Write, Read | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| TryWaitShortDeb | 5 | Debounce Time from TryWait.SRC to Attached.SRC<br><br>0b0:120ms<br>0b1:15ms |
| CCErrorLock | 4 | Lock FSM in ErrorRecovery State<br><br>0b0: No effect<br>0b1: Stay in ErrorRecovery state |
| ccDRPPhase | 1:0 | Percent of Time Device is Acting as Unattached.SRC when CCSnkEn = 1 and CCSrcEn = 1<br><br>0b00: 35%<br>0b01: 40%<br>0b10: 45%<br>0b11: 50% |

## CC_CTRL5 (0x25)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | VBMask | ccSnkExitEn |
| **Reset** | – | – | – | – | – | – | 0x1 | 0x1 |
| **Access Type** | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| VBMask | 1 | Ignore $V_B$ Status In Transition from Unattached.SNK to Attached.SNK<br><br>0b0: $V_B$ is checked<br>0b1: $V_B$ is ignored |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ccSnkExitEn | 0 | Exit Attached.SNK State Selection<br><br>0b0: Exit Attached.SNK state based on $V_B$ level only<br>0b1: Exit Attached.SNK state based on $V_B$ level or when CC < $V_{RA\_RD0.5}$ |

## CC_CTRL6 (0x26)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | CCLadderDis | – | – | – | – | tQDebounce2[1:0] | |
| **Reset** | – | 0x0 | – | – | – | – | 0x0 | |
| **Access Type** | – | Write, Read | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCLadderDis | 6 | When High, Disable CC Resistor Ladder. To be used in case of "Manual" power role swap, to make CC "more" Hi-Z |
| tQDebounce2 | 1:0 | Quick Debounce2 Selection<br><br>0b00: 1ms<br>0b01: 2ms<br>0b10: 3ms<br>0b11: 20ms |

## VCONN_ILIM (0x28)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | CCVcnOcpEn | VCONN_ILIM[3:0] | | | |
| **Reset** | – | – | – | 0x1 | 0x8 | | | |
| **Access Type** | – | – | – | Write, Read | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CCVcnOcpEn | 4 | $V_{CONN}$ Overcurrent Protection Enable<br><br>0b0: VCONNOCP does have impact on $V_{CONN}$ switch<br>0b1: VCONNOCP turns off the $V_{CONN}$ switch after 12ms |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| VCONN_ILIM | 3:0 | $V_{CONN}$ Switch Overcurrent Threshold<br><br>0b0000: Reserved<br>0b0001: 200mA<br>0b0010: 250mA<br>0b0011: 300mA<br>0b0100: 350mA<br>>=0b0101: Reserved |

## BC_CTRL0 (0x2A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | – | ChgDetMan |
| **Reset** | – | – | – | – | – | – | – | 0x0 |
| **Access Type** | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ChgDetMan | 0 | Manual Charger Detection Run Enable. The bit auto resets to '0'.<br><br>0b0: Not enabled<br>0b1: Request manual run of charger detection |

## BC_CTRL1 (0x2B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | DCDTmo | – | – | DCP3PDet | RSVD | – | – | ChgDetEn |
| **Reset** | 0x0 | – | – | 0x0 | 0x0 | – | – | 0x1 |
| **Access Type** | Write, Read | – | – | Write, Read | Write, Read | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| DCDTmo | 7 | Data Contact Detection Wait Time<br><br>0b0: 2000ms<br>0b1: 800ms |
| DCP3PDet | 4 | Enable Detection of 3A DCP (adds detection step after BC1.2 completes to detect presence of 3A DCP – D+/D- short with 2 series diode clamp) |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: Not enabled<br>0b1: Enabled |
| RSVD | 3 | Reserved |
| ChgDetEn | 0 | Charger Detection Enable<br><br>0b0: Not enabled<br>0b1: Enabled, charger detection runs every time $V_B > V_{BDET}$ and ChgDetAbort = 0 |

## SBU1DetResult1 (0x2C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | SBUDetAbortPriority | – | – | SBU1DetGround | SBU1DetAbort | SBU1DetOpen | SBU1DetIpu[1:0] | |
| **Reset** | 0x0 | – | – | 0x0 | 0x0 | 0x0 | 0x0 | |
| **Access Type** | Write, Read | – | – | Read Only | Read Only | Read Only | Read Only | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBUDetAbortPriority | 7 | Priority of Abort Condition in SBU1/SBU2 Resistor Detection Measurement<br><br>0b0: During SBU1/SBU2 resistor detection, an Abort result on one of the two pins is Don't Care unless an Abort result is found also on the other pin.<br>0b1: During SBU1/SBU2 resistor detection, an Abort result on one of the two pins has high priority and an overall Abort result is reported. |
| SBU1DetGround | 4 | SBU1 Resistor Detection Measurement Ground Result<br><br>0b0: Latest SBU1 resistor detection measurement result was not a Ground.<br>0b1: Latest SBU1 resistor detection measurement result was a Ground. |
| SBU1DetAbort | 3 | SBU1 Resistor Detection Measurement Abort Result<br><br>0b0: Latest SBU1 resistor detection measurement result was not an Abort.<br>0b1: Latest SBU1 resistor detection measurement result was an Abort. |
| SBU1DetOpen | 2 | SBU1 Resistor Detection Measurement Open Result<br><br>0b0: Latest SBU1 resistor detection measurement result was not an Open.<br>0b1: Latest SBU1 resistor detection measurement result was an Open. |
| SBU1DetIpu | 1:0 | SBU1 Resistor Detection Measurement Final Imposed Pullup Current. If the result is Abort or Open, this is set to 0b00. If the result is Ground, this is set to 0b11. |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## SBU1DetResult2 (0x2D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SBU1DetVADC[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU1DetVADC | 7:0 | SBU1 Resistor Detection Measurement Final Voltage ADC Result. If the result is Abort or Ground, this is set to 0x00. If the result is Open, this is set to 0xFF. LSB = 5.882mV = 0.392% typ. |

## SBU2DetResult1 (0x2E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | SBU2DetGround | SBU2DetAbort | SBU2DetOpen | SBU2DetIpu[1:0] | |
| Reset | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | |
| Access Type | – | – | – | Read Only | Read Only | Read Only | Read Only | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU2DetGround | 4 | SBU2 Resistor Detection Measurement Ground Result<br><br>0b0: Latest SBU2 resistor detection measurement result was not a Ground.<br>0b1: Latest SBU2 resistor detection measurement result was a Ground. |
| SBU2DetAbort | 3 | SBU2 Resistor Detection Measurement Abort Result<br><br>0b0: Latest SBU2 resistor detection measurement result was not an Abort.<br>0b1: Latest SBU2 resistor detection measurement result was an Abort. |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU2DetOpen | 2 | SBU2 Resistor Detection Measurement Open Result<br><br>0b0: Latest SBU2 resistor detection measurement result was not an Open.<br>0b1: Latest SBU2 resistor detection measurement result was an Open. |
| SBU2DetIpu | 1:0 | SBU2 Resistor Detection Measurement Final Imposed Pullup Current. If the result is Abort or Open, this is set to 0b00. If the result is Ground, this is set to 0b11.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## SBU2DetResult2 (0x2F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | SBU2DetVADC[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU2DetVADC | 7:0 | SBU2 Resistor Detection Measurement Final Voltage ADC Result. If the result is Abort or Ground, this is set to 0x00. If the result is Open, this is set to 0xFF. LSB = 5.882mV = 0.392% typ. |

## SBUDetCtrl (0x30)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | SBUDetContEn | SBUDetOneShotEn | SBUDetManEn |
| **Reset** | – | – | – | – | – | 0x1 | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBUDetContEn | 2 | Enable of SBU1/SBU2 Continuous Resistor Detection Measurements in Debug Accessory Sink Mode |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: SBU1/SBU2 resistor detection continuous measurements in debug accessory mode sink disabled.<br>0b1: SBU1/SBU2 resistor detection continuous measurements in debug accessory mode sink enabled. |
| SBUDetOneShotEn | 1 | Enable of SBU1/SBU2 One-Shot Resistor Detection Measurement in Debug Accessory Sink Mode<br><br>0b0: SBU1/SBU2 resistor detection one-shot measurement in debug accessory mode sink disabled.<br>0b1: SBU1/SBU2 resistor detection one-shot measurement in debug accessory mode sink enabled. |
| SBUDetManEn | 0 | Enable of SBU1/SBU2 Resistor Detection Manual Measurement<br><br>0b0: SBU1/SBU2 resistor detection manual measurement disabled.<br>0b1: SBU1/SBU2 resistor detection manual measurement enabled. |

## RAcc1DetVMax (0x31)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc1DetVMax[7:0] | | | | | | | |
| Reset | 0xAE | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc1DetVMax | 7:0 | SBU1/SBU2 Valid Accessory 1 Resistor Maximum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc1DetVMin (0x32)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc1DetVMin[7:0] | | | | | | | |
| Reset | 0x99 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc1DetVMin | 7:0 | SBU1/SBU2 Valid Accessory 1 Resistor Minimum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc1DetIpu (0x33)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | RAcc1DetIpu[1:0] | |
| **Reset** | – | – | – | – | – | – | 0x2 | |
| **Access Type** | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc1DetIpu | 1:0 | Accessory 1 Resistor Final Imposed Pullup Current. If the final pullup current is equal to the configured RAcc1DetIpu[1:0] setting and the ADC result is within the [RAcc1DetVMin[7:0],RAcc1DetVMax[7:0]] range, SBU1/SBU2 Valid accessory 1 resistor is detected.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## RAcc2DetVMax (0x34)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RAcc2DetVMax[7:0] | | | | | | | |
| **Reset** | 0x74 | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc2DetVMax | 7:0 | SBU1/SBU2 Valid Accessory 2 Resistor Maximum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc2DetVMin (0x35)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Field | RAcc2DetVMin[7:0] |
|---|---|
| Reset | 0x66 |
| Access Type | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc2DetVMin | 7:0 | SBU1/SBU2 Valid Accessory 2 Resistor Minimum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc2DetIpu (0x36)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | RAcc2DetIpu[1:0] | |
| Reset | – | – | – | – | – | – | 0x1 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc2DetIpu | 1:0 | Accessory 2 Resistor Final Imposed Pullup Current. If the final pullup current is equal to the configured RAcc2DetIpu[1:0] setting and the ADC result is within the [RAcc2DetVMin[7:0],RAcc2DetVMax[7:0]] range, SBU1/SBU2 Valid accessory 2 resistor is detected.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## RAcc3DetVMax (0x37)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc3DetVMax[7:0] | | | | | | | |
| Reset | 0xD9 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc3DetVMax | 7:0 | SBU1/SBU2 Valid Accessory 3 Resistor Maximum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc3DetVMin (0x38)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc3DetVMin[7:0] | | | | | | | |
| Reset | 0xBF | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc3DetVMin | 7:0 | SBU1/SBU2 Valid Accessory 3 Resistor Maximum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc3DetIpu (0x39)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | RAcc3DetIpu[1:0] | |
| Reset | – | – | – | – | – | – | 0x1 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc3DetIpu | 1:0 | Accessory 3 Resistor Final Imposed Pullup Current. If the final pullup current is equal to the configured RAcc3DetIpu[1:0] setting and the ADC result is within the [RAcc3DetVMin[7:0],RAcc3DetVMax[7:0]] range, SBU1/SBU2 Valid accessory 3 resistor is detected.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## RAcc4DetVMin (0x3A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Field | RAcc4DetVMin[7:0] |
|---|---|
| Reset | 0x00 |
| Access Type | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc4DetVMin | 7:0 | SBU1/SBU2 Valid Accessory 4 Resistor Maximum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc4DetVMax (0x3B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc4DetVMax[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc4DetVMax | 7:0 | SBU1/SBU2 Valid Accessory 4 Resistor Minimum Final Voltage ADC Result Threshold. LSB = 5.882mV = 0.392% typ. |

## RAcc4DetIpu (0x3C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | RAcc4DetIpu[1:0] | |
| Reset | – | – | – | – | – | – | 0x0 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc4DetIpu | 1:0 | Accessory 4 Resistor Final Imposed Pullup Current. If the final pullup current is equal to the configured RAcc4DetIpu[1:0] setting and the ADC result is within the [RAcc4DetVMin[7:0],RAcc4DetVMax[7:0]] range, SBU1/SBU2 Valid accessory 4 resistor is detected.<br><br>0b00: 2µA<br>0b01: 8µA |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b10: 32µA<br>0b11: 128µA |

## RAcc5DetVMax (0x3D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc5DetVMax[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc5DetVMax | 7:0 | SBU1/SBU2 Valid Accessory 5 Resistor Maximum Final Voltage ADC Result Threshold.<br>LSB = 5.882mV = 0.392% typ. |

## RAcc5DetVMin (0x3E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAcc5DetVMin[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc5DetVMin | 7:0 | SBU1/SBU2 Valid Accessory 5 Resistor Minimum Final Voltage ADC Result Threshold.<br>LSB = 5.882mV = 0.392% typ. |

## RAcc5DetIpu (0x3F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | RAcc5DetIpu[1:0] | |
| Reset | – | – | – | – | – | – | 0x0 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RAcc5DetIpu | 1:0 | Accessory 5 Resistor Final Imposed Pullup Current. If the final pullup current is equal to the configured RAcc5DetIpu[1:0] setting and the ADC result is within the [RAcc5DetVMin[7:0],RAcc5DetVMax[7:0]] range, SBU1/SBU2 Valid accessory 5 resistor is detected.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## RMoistDetVth (0x50)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RMoistDetVth[7:0] | | | | | | | |
| Reset | 0x66 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| RMoistDetVth | 7:0 | Moisture Detection Valid Final Voltage ADC Result Threshold.<br>LSB = 5.882mV = 0.392% typ. |

## MoistDetCtrl (0x51)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | MoistDetAutoCfg | MoistDetPerEn | MoistDetManEn | RMoistDetIpu[1:0] | |
| Reset | – | – | – | 0x1 | 0x1 | 0x0 | 0x2 | |
| Access Type | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| MoistDetAutoCfg | 4 | Enable Automatic Configuration of Moisture Detection Measurements.<br><br>If MoistDetAutoCfg = 1, the system measures the resistance between CC1 (alternately CC2) and all other pins of the USB Type-C connector. If MoistDetAutoCfg = 0, the pins to be pulled up and those to be grounded are determined by MoistDetPUConfig[5:0] and MoistDetPDConfig[6:0] settings. |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: Moisture detection measurements automatic configuration disabled.<br>0b1: Moisture detection measurements automatic configuration enabled. |
| MoistDetPerEn | 3 | Enable of Unattached Mode Moisture Detection Periodic Measurements.<br>If set high, moisture detection measurements are executed every 10s in unattached mode. In attached states, moisture detection is skipped.<br><br>0b0: Moisture detection periodic measurements disabled.<br>0b1: Moisture detection periodic measurements enabled. |
| MoistDetManEn | 2 | Enable of Unattached Mode Moisture Detection Manual Measurement.<br>If set high, a single moisture detection measurement is executed. Self-clearing.<br><br>If set high while not in unattached mode, it stays armed until detachment is detected and can optionally be cleared through $I^2C$ interface.<br><br>0b0: Moisture detection manual measurement disabled.<br>0b1: Moisture detection manual measurement enabled. |
| RMoistDetIpu | 1:0 | Target Pullup Current Used to Specify Moisture Resistance Threshold $R_{MOIST}$. Together with RMoistDetVth[7:0], it sets the desired resistance threshold for moisture: $R_{MOIST}$ = RMoistDetIpu[1:0] x RMoistDetVth[7:0] x LSB, where LSB = 5.882mV = 0.392% (typ).<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## MoistDetPUConfig (0x52)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | MoistDetPUConfig[5:0] | | | | | |
| **Reset** | – | – | 0x00 | | | | | |
| **Access Type** | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| MoistDetPUConfig | 5:0 | Pullup Switch Control for Manually Configured Moisture Detection. Active when MoistDetAutoCfg = 0.<br><br>Bit 0: Enables CC1 pullup force/sense switches<br>Bit 1: Enables CC2 pullup force/sense switches<br>Bit 2: Enables SBU1 pullup force/sense switches<br>Bit 3: Enables SBU2 pullup force/sense switches |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | Bit 4: Enables CDP pullup force/sense switches<br>Bit 5: Enables CDN pullup force/sense switches |

## MoistDetPDConfig (0x53)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | MoistDetPDConfig[6:0] | | | | | | |
| **Reset** | – | 0x00 | | | | | | |
| **Access Type** | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| MoistDetPDConfig | 6:0 | Pulldown Switch Control for Manually Configured Moisture Detection. Active when MoistDetAutoCfg = 0.<br><br>Bit 0: Enables CC1 pulldown switch<br>Bit 1: Enables CC2 pulldown switch<br>Bit 2: Enables SBU1 pulldown switch<br>Bit 3: Enables SBU2 pulldown switch<br>Bit 4: Enables CDP pulldown switch<br>Bit 5: Enables CDN pulldown switch<br>Bit 6: Enables $V_B$ pulldown switch |

## MoistDetAutoCC1Result1 (0x54)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | CC1MoiGnd | CC1MoiAbrt | CC1MoiOpn | CC1MoistIpu[1:0] | |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | |
| **Access Type** | – | – | – | Read Only | Read Only | Read Only | Read Only | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CC1MoiGnd | 4 | Moisture Detection Burst Measurement Ground Result Indicator for CC1<br><br>0b0: Latest CC1 moisture detection burst measurement result was not a Ground.<br>0b1: Latest CC1 moisture detection burst measurement result was a Ground. |
| CC1MoiAbrt | 3 | Moisture Detection Burst Measurement Abort Result Indicator for CC1 |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| | | 0b0: Latest CC1 moisture detection burst measurement result was not an Abort.<br>0b1: Latest CC1 moisture detection burst measurement result was an Abort. |
| CC1MoiOpn | 2 | Moisture Detection Burst Measurement Open Result Indicator for CC1<br><br>0b0: Latest CC1 moisture detection burst measurement result was not an Open.<br>0b1: Latest CC1 moisture detection burst measurement result was an Open. |
| CC1MoistIpu | 1:0 | Moisture Detection Burst Measurement Final Pullup Current for CC1. If the result is Abort or Open, this is set to 0b00. If the result is Ground, this is set to 0b11.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## MoistDetAutoCC1Result2 (0x55)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | CC1MoistVADC[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CC1MoistVADC | 7:0 | Moisture Detection Burst Measurement Final ADC Value for CC1. If the result is Abort or Ground, this is set to 0x00. If the result is Open, this is set to 0xFF. LSB = 5.882mV = 0.392% (typ). |

## MoistDetAutoCC2Result1 (0x56)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | CC2MoiGnd | CC2MoiAbrt | CC2MoiOpn | CC2MoistIpu[1:0] | |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | |
| **Access Type** | – | – | – | Read Only | Read Only | Read Only | Read Only | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CC2MoiGnd | 4 | Moisture Detection Burst Measurement Ground Result Indicator for CC2<br><br>0b0: Latest CC2 moisture detection burst measurement result was not a Ground.<br>0b1: Latest CC2 moisture detection burst measurement result was a Ground. |
| CC2MoiAbrt | 3 | Moisture Detection Burst Measurement Abort Result Indicator for CC2<br><br>0b0: Latest CC2 moisture detection burst measurement result was not an Abort.<br>0b1: Latest CC2 moisture detection burst measurement result was an Abort. |
| CC2MoiOpn | 2 | Moisture Detection Burst Measurement Open Result Indicator for CC2<br><br>0b0: Latest CC2 moisture detection burst measurement result was not an Open.<br>0b1: Latest CC2 moisture detection burst measurement result was an Open. |
| CC2MoistIpu | 1:0 | Moisture Detection Burst Measurement Final Pullup Current for CC2. If the result is Abort or Open, this is set to 0b00; if the result is Ground, this is set to 0b11.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## MoistDetAutoCC2Result2 (0x57)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | CC2MoistVADC[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| CC2MoistVADC | 7:0 | Moisture Detection Burst Measurement Final ADC Value for CC2. If the result is Abort or Ground, this is set to 0x00. If the result is Open, this is set to 0xFF. LSB = 5.882mV = 0.392% (typ). |

## MoistDetAutoSBU1Result1 (0x58)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | SBU1MoiGnd | SBU1MoiAbrt | SBU1MoiOpn | SBU1MoistIpu[1:0] | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | – | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU1MoiGnd | 4 | Moisture Detection Burst Measurement Ground Result Indicator for SBU1<br><br>0b0: Latest SBU1 moisture detection burst measurement result was not a Ground.<br>0b1: Latest SBU1 moisture detection burst measurement result was a Ground. |
| SBU1MoiAbrt | 3 | Moisture Detection Burst Measurement Abort Result Indicator for SBU1<br><br>0b0: Latest SBU1 moisture detection burst measurement result was not an Abort.<br>0b1: Latest SBU1 moisture detection burst measurement result was an Abort. |
| SBU1MoiOpn | 2 | Moisture Detection Burst Measurement Open Result Indicator for SBU1<br><br>0b0: Latest SBU1 moisture detection burst measurement result was not an Open.<br>0b1: Latest SBU1 moisture detection burst measurement result was an Open. |
| SBU1MoistIpu | 1:0 | Moisture Detection Burst Measurement Final Pullup Current for SBU1. If the result is Abort or Open, this is set to 0b00. If the result is Ground, this is set to 0b11.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## MoistDetAutoSBU1Result2 (0x59)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | SBU1MoistVADC[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU1MoistVADC | 7:0 | Moisture Detection Burst Measurement Final ADC Value for SBU1. If the result is Abort or Ground, this is set to 0x00. If the result is Open, this is set to 0xFF. LSB = 5.882mV = 0.392% (typ). |

## MoistDetAutoSBU2Result1 (0x5A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | SBU2MoiGnd | SBU2MoiAbrt | SBU2MoiOpn | SBU2MoistIpu[1:0] | |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | 0x0 | |
| **Access Type** | – | – | – | Read Only | Read Only | Read Only | Read Only | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU2MoiGnd | 4 | Moisture Detection Burst Measurement Ground Result Indicator for SBU2<br><br>0b0: Latest SBU2 moisture detection burst measurement result was not a Ground.<br>0b1: Latest SBU2 moisture detection burst measurement result was a Ground. |
| SBU2MoiAbrt | 3 | Moisture Detection Burst Measurement Abort Result Indicator for SBU2<br><br>0b0: Latest SBU2 moisture detection burst measurement result was not an Abort.<br>0b1: Latest SBU2 moisture detection burst measurement result was an Abort. |
| SBU2MoiOpn | 2 | Moisture Detection Burst Measurement Open Result Indicator for SBU2<br><br>0b0: Latest SBU2 moisture detection burst measurement result was not an Open.<br>0b1: Latest SBU2 moisture detection burst measurement result was an Open. |
| SBU2MoistIpu | 1:0 | Moisture Detection Burst Measurement Final Pullup Current for SBU2. If the result is Abort or Open, this is set to 0b00. If the result is Ground, this is set to 0b11.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |

## MoistDetAutoSBU2Result2 (0x5B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | SBU2MoistVADC[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| SBU2MoistVADC | 7:0 | Moisture Detection Burst Measurement Final ADC Value for SBU2. If the result is Abort or Ground, this is set to 0x00. If the result is Open, this is set to 0xFF. LSB = 5.882mV = 0.392% (typ). |

## ADCCtrl1 (0x5C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | ADCGroundVth[3:0] | | | | ADCRetryNum[2:0] | | |
| **Reset** | – | 0x4 | | | | 0x1 | | |
| **Access Type** | – | Write, Read | | | | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ADCGroundVth | 6:3 | ADC Ground Threshold. It applies to resistive measurements used in both Moisture Detection and Accessory Mode Detection. The actual ground condition range, namely the $R_{SBU\_RNG\_GND}$ and $R_{CCCD\_RNG\_GND}$, depends on the setting of ADCGroundVth[3:0]. If the final average ADC reading of a measurement is ≤ the actual ground threshold, the Ground result is reported. LSB = 5.882mV = 0.392% (typ). |
| ADCRetryNum | 2:0 | Number of Resistive Measurement Retries. It applies to resistive measurement used in both moisture detection and accessory mode detection. The device retries the measurement if one of the following conditions is true:<br>1. (maximum ADC reading = 0xFF) AND (pullup current = 2µA) AND (average ADC reading < (0xFF - ADCNoiseClampRng[5:0]))<br>2. (maximum ADC reading = 0xFF) AND (pullup current ≠ 2µA)<br><br>If the condition is still true after this number of retries, the Abort result is reported.<br><br>0x0: No retry.<br>>0x0: Number of retry attempts. |

## ADCCtrl2 (0x5D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | IpuResult[1:0] | | ADCCorrNum[5:0] | | | | | |
| **Reset** | 0x0 | | 0x7 | | | | | |
| **Access Type** | Read Only | | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| IpuResult | 7:6 | Final Imposed Pullup Current Once a Resistive Measurement is Complete. It is set to 0b00 if the result is Abort or Open. It is set to 0b11 if the result is Open.<br><br>0b00: 2µA<br>0b01: 8µA<br>0b10: 32µA<br>0b11: 128µA |
| ADCCorrNum | 5:0 | ADC Shift Factor for USB Type-C Pins When Not Only SBU1 and/or SBU2 are Pulled Up. It applies to resistive measurements used in Moisture Detection. This register must NOT be set lower than the default value. |

## ADC_CTRL3 (0x5E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ADCAvgNum[2:0] | | | ADCSBUCorrNum[4:0] | | | | |
| **Reset** | 0x1 | | | 0x3 | | | | |
| **Access Type** | Write, Read | | | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ADCAvgNum | 7:5 | Number of Samples in ADC Reading Averaging. It applies to any resistive measurements used in moisture detection and accessory mode detection.<br><br>0x0: 1 sample<br>0x1: 2 samples<br>0x2: 4 samples<br>0x3: 8 samples<br>0x4: 16 samples<br>0x5: 32 samples<br>0x6: 64 samples<br>0x7: 128 samples |
| ADCSBUCorrNum | 4:0 | ADC Shift Factor for When Only SBU1 and/or SBU2 Are Pulled Up. It applies to SBU1/SBU2 resistive measurements used in both Moisture Detection and Accessory Mode detection. This register must NOT be set lower than the default value. |

## ADC_CTRL4 (0x5F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | ADCNoiseClampRng[5:0] | | | | | |

| | | | |
|---|---|---|---|
| **Reset** | – | – | 0x0 |
| **Access Type** | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ADCNoiseClampRng | 5:0 | ADC Result Margin to Account for External Noise and Avoid Result Clamping Close to Full-Scale. This register must NOT be changed from the default value. |

## ADCResultAvg (0x60)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ADCResultAvg[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ADCResultAvg | 7:0 | Final Average ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open. LSB = 5.882mV = 0.392% typ. |

## ADCResultMax (0x61)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ADCResultMax[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ADCResultMax | 7:0 | Final Maximum ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open. LSB = 5.882mV = 0.392% typ. |

## ADCResultMin (0x62)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ADCResultMin[7:0] | | | | | | | |

| | |
|---|---|
| **Reset** | 0x00 |
| **Access Type** | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ADCResultMin | 7:0 | Final Minimum ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open. LSB = 5.882mV = 0.392% typ. |

## VB_CTRL (0x63)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | ACTIV_DISCH_EN | – |
| **Reset** | – | – | – | – | – | – | 0x0 | – |
| **Access Type** | – | – | – | – | – | – | Write, Read | – |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ACTIV_DISCH_EN | 1 | Active Discharge Control<br><br>0b0: Active discharge disabled on $V_B$<br>0b1: Active discharge enabled on $V_B$ |

## Applications Information

### Hi-Speed USB

Hi-Speed USB requires careful PCB layout with 45Ω single-ended/90Ω differential controlled-impedance traces that are matched by equal lengths.

### Power Supply Bypassing

Bypass $V_B$, $V_{DD}$, and BAT with 1µF ceramic capacitors to GND as close as possible to the device.

### Power-On Reset (POR)

The MAX20342 provides secure operation with the power-on reset circuits. When the power supply for the device exceeds the POR rising value 1.6V (typ) and stays above the maximum falling edge, the internal logic is in a known state for safe operation. However, the *Electrical Characteristics* table parameters are not guaranteed until the $V_B$ and BAT voltages meet the specified global conditions.

### Choosing I²C Pullup Resistors

The I²C interface requires pullup resistors to provide a logic-high level to data and clock lines. There are trade-offs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. The I²C interface specifies 120ns rise time to go from low to high (30% to 70%) for fast mode plus, which is defined for a clock frequency up to 1000kHz (see the I²C specifications in the *Electrical Characteristics* table for details). To meet the rise time requirement, choose pullup resistors so that the rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 120ns$. If the transition time becomes too slow, the setup and hold times might not be met and waveforms might not be recognized.

### Resetting the I²C Bus from Suspend

If the I²C bus is suspended due to a weak or dead battery, an I²C STOP command needs to be performed after enabling the I²C buffers and pullup bias. The I²C STOP command is necessary before restarting the I²C traffic.

### Extended ESD Protection

The CDP and CDN pins are protected against ESD up to ±6kV. The CC1, CC2, SBU1 and SBU2 pins are further protected up to ±15kV (HBM) without damage. The VB input withstands up to ±15kV (HBM) if bypassed with a 1µF ceramic capacitor close to the pin. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX20342 continues to function without latch-up.

### ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

## Human Body Model

Figure 16 shows the human-body model, while Figure 17 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

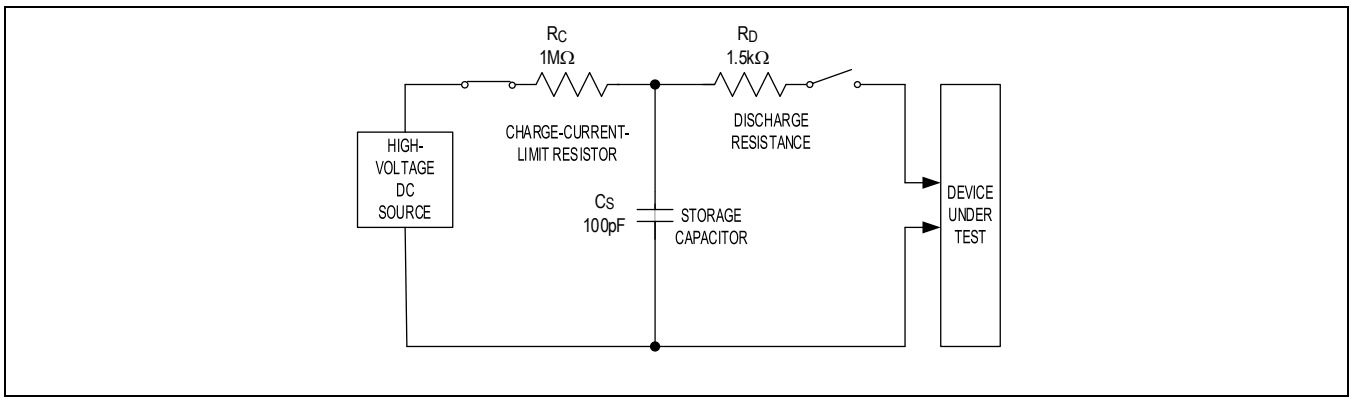



*Figure 16. Human Body ESD Test Model*

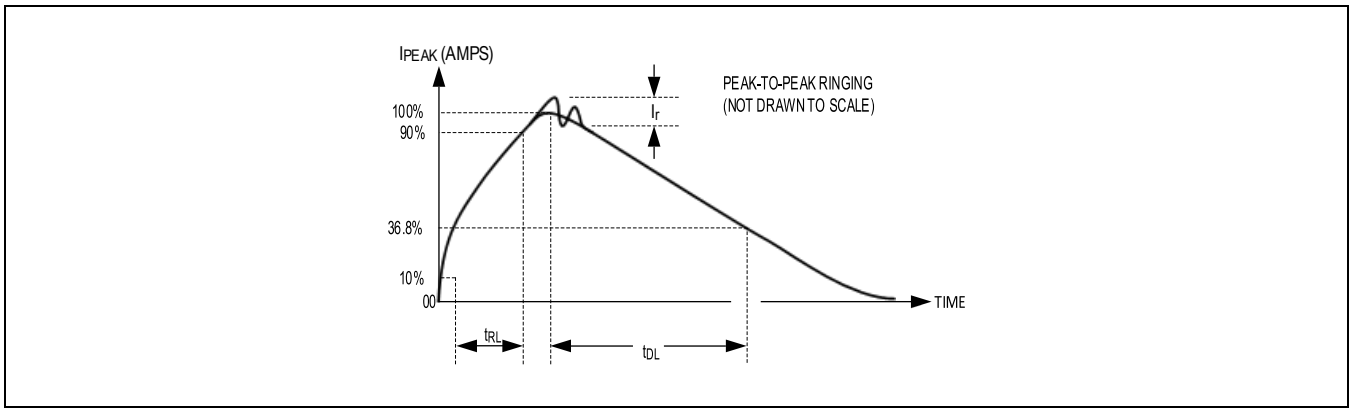



*Figure 17. Human Body Current Waveform*

## IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX20342 is specified for ±15kV Air-Gap and ±8kV Contact Discharge IEC 61000-4-2 on the CC1, CC2, SBU1, and SBU2 pins.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (*Figure 18*), the ESD-withstand voltage measured to this standard is generally lower than that measured using the HBM. *Figure 19* shows the current waveform for the ±6kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Contact Discharge method connects the probe to the device before the probe is energized.

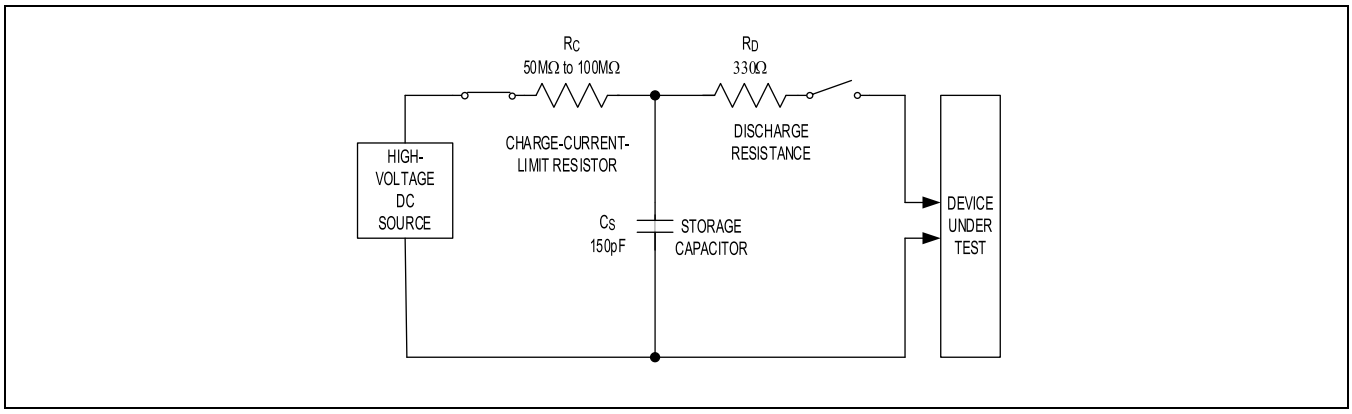



*Figure 18. IEC61000-4-2 ESD Test Model*

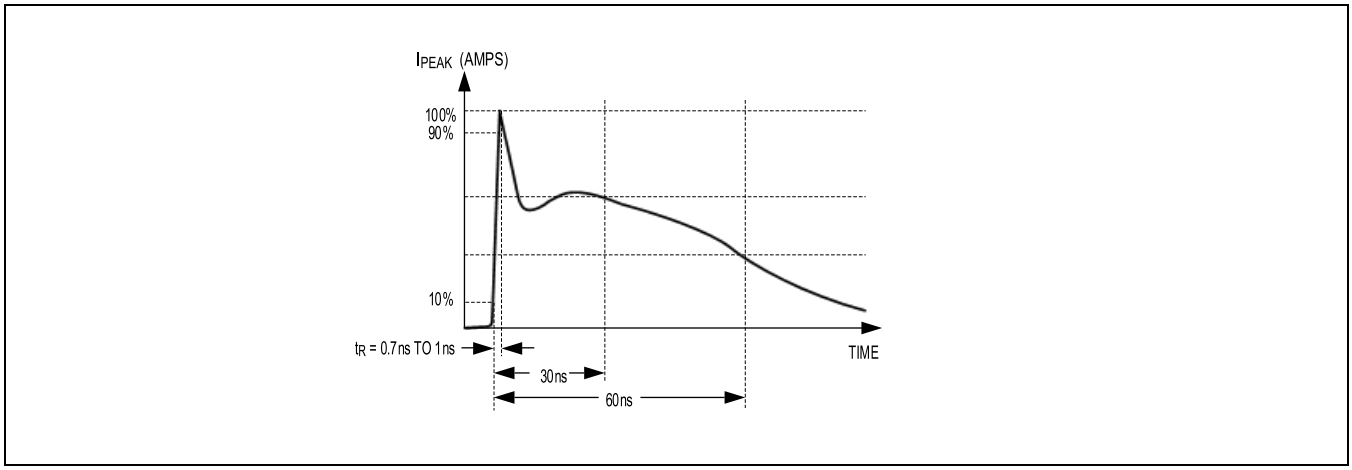
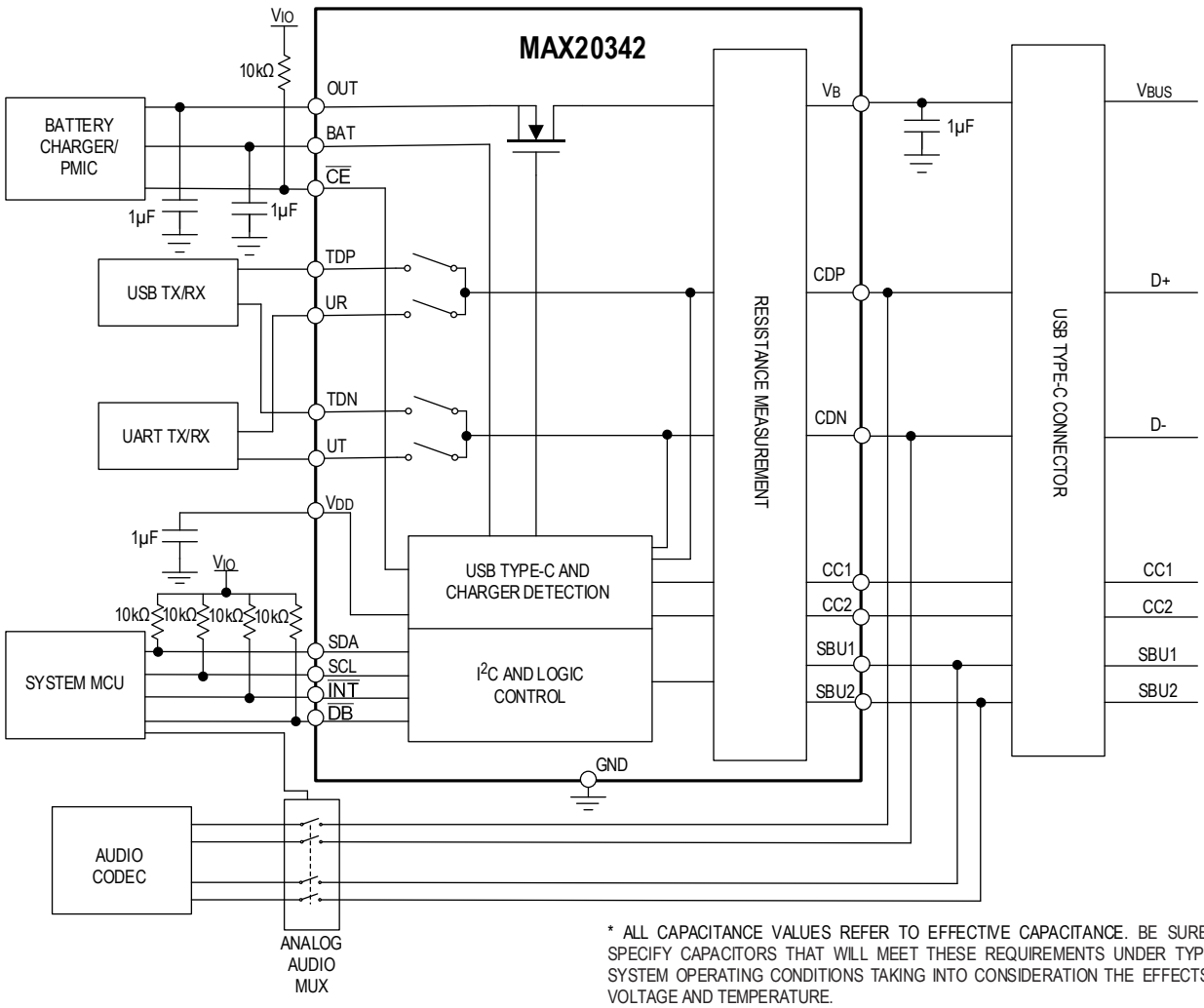



*Figure 19. IEC61000-4-2 ESD Generator Current Waveform*

## Typical Application Circuits




## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX20342EWG+ | -40°C to +85°C | 24 WLP |
| MAX20342EWG+T | -40°C to +85°C | 24 WLP |

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/20 | Initial release | — |
| 1 | 11/20 | Updated the *Shutdown* section | 37 |
| 2 | 6/21 | Updated *Absolute Maximum Ratings* section | 3 |
| 3 | 9/21 | Updated *Benefits and Features* and *USB BC1.2 Charger Detection* sections, *Electrical Characteristics* table; added *Fault State* section | 1, 6, 20, 35 |

# Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX20342EWG+ MAX20342EWG+T