

# K- & Ka-Band High Power Reflective SPDT PIN Switch Die

## 20 - 40 GHz



MASW-011144-DIE

Rev. V4

### Features

- Broadband Performance, 20 - 40 GHz
- Low Loss: <1 dB, 30 - 40 GHz
- High Isolation: >30 dB, 20 - 40 GHz
- 40 dBm CW Power @ 35 GHz
- Die with G-S-G RF Pads and DC Bias Pads
- Includes DC blocking Capacitor at each RF input and Bias Low Pass filters with Series Resistor
- RoHS\* Compliant

### Applications

- K- and Ka-Band applications, including point-to-point radio and military products.

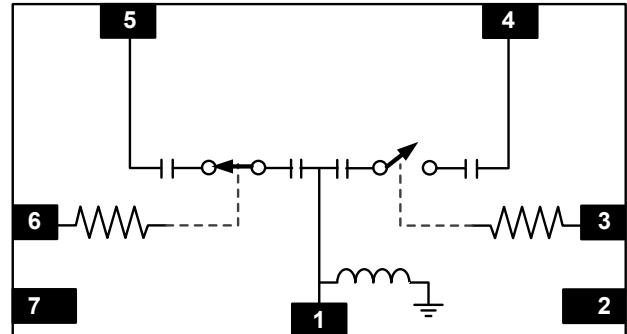
### Description

The MASW-011144-DIE is a high power SPDT, reflective, broadband, high linearity, Aluminum Gallium Arsenide (AlGaAs) PIN diode switch for K- and Ka-Band applications, including point-to-point radio and military products.

The switch utilizes one shunt PIN diode per RF channel. The diode is controlled through an on-chip bias network that includes a current limiting resistor. These bias networks simplify the control of the switch; no external components are required.

The SPDT MMIC utilizes MACOM's proven AlGaAs PIN diode technology. The switch is fully passivated with silicon nitride and has an added polymer layer for scratch protection. The protective coating prevents damage to the junctions and the anode air-bridges during handling and assembly. The die has backside metallization to facilitate an epoxy die attach process.

### Functional Schematic



### Pad Configuration<sup>1</sup>

Pad #	Function
1	RF Common
2	No Connection
3	BIAS1
4	RF1
5	RF2
6	BIAS2
7	No Connection

1. The die backside must be connected to RF, DC and thermal ground.

### Ordering Information

Part Number	Package
MASW-011144-DIE	Die in Gel Pack

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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**Electrical Specifications:  $T_A = +25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$ ,  $V_F = 4.5 \text{ V}$  /  $V_R = -9 \text{ V}$ ,  $P_{IN} = 0 \text{ dBm}$**

Parameter	Conditions	Units	Min.	Typ.	Max.
Insertion Loss	26 GHz	dB	—	0.90	—
	32 GHz			0.65	1.0
	34 GHz			0.65	0.9
	38 GHz			0.75	1.1
Insertion Loss	34 GHz, $P_{IN} = 30 \text{ dBm}$	dB	—	0.65	—
Isolation	26 GHz	dB	—	30	—
	32 GHz		—		
	34 GHz		25		
	38 GHz		—		
Input Return Loss	34 GHz	dB	14.5	22	—
Output Return Loss	34 GHz	dB	14.0	20	—
CW Input Power <sup>2</sup>	-9 V @ 85°C, 29 GHz	dBm	—	39.0	—
	-25 V @ 85°C, 29 GHz			41.2	
Switching Speed	10 dBm, 10 - 90% RF, 500 $\mu\text{s}$ pulse, 26.5 GHz	ns	—	40	—
0.1 dB Compression Point	-9 V @ 85°C, 29 GHz	dBm	—	34	—
	-25 V @ 85°C, 29 GHz			40	
Forward Current	$V_F = 4.5 \text{ V}$	mA	6.0	8.5	11.0

2. Reverse bias voltage should be determined based on working conditions. For example, -25 V @ 40 dBm input power. For lower power applications, a less negative voltage can be used.

## Absolute Maximum Ratings

Parameter	Absolute Maximum
$T_x$ Incident CW Power	42 dBm @ 29 GHz
Reverse DC Bias Voltage	-50 V
Forward Bias Current	15 mA
Junction Temperature	+150°C
Operating Temperature	-55°C to +85°C
Storage Temperature	-65°C to +150°C

## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1A devices.

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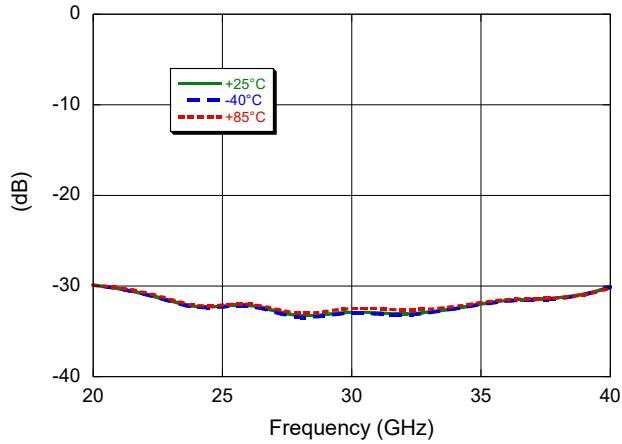


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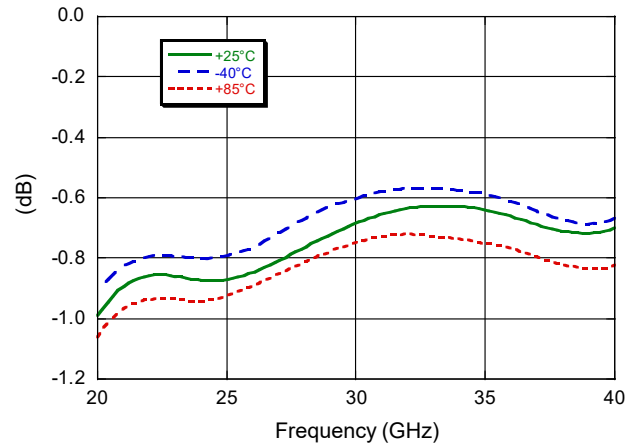
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### Typical Performance Curves: $V_R = -9\text{ V}$

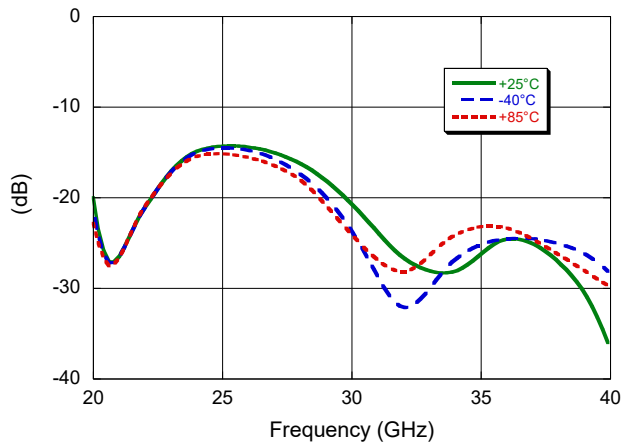
**Isolation over Temperature**



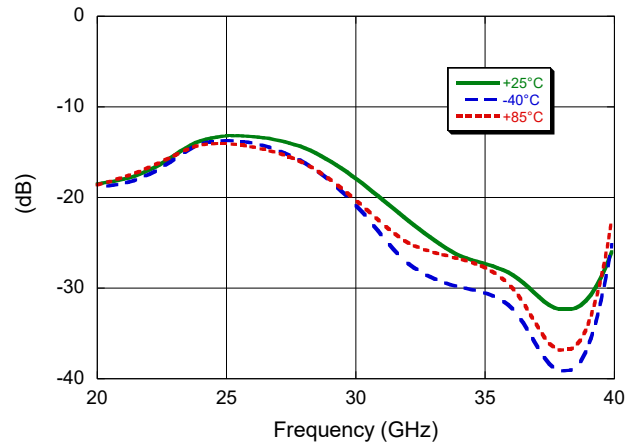
**Insertion Loss over Temperature**



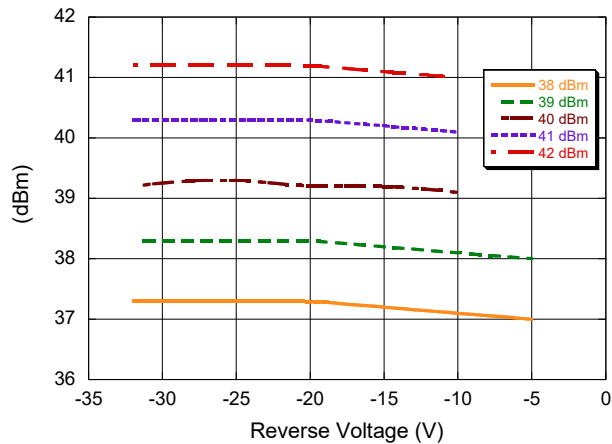
**RF1, RF2 Return Loss over Temperature**



**Common Return Loss over Temperature**



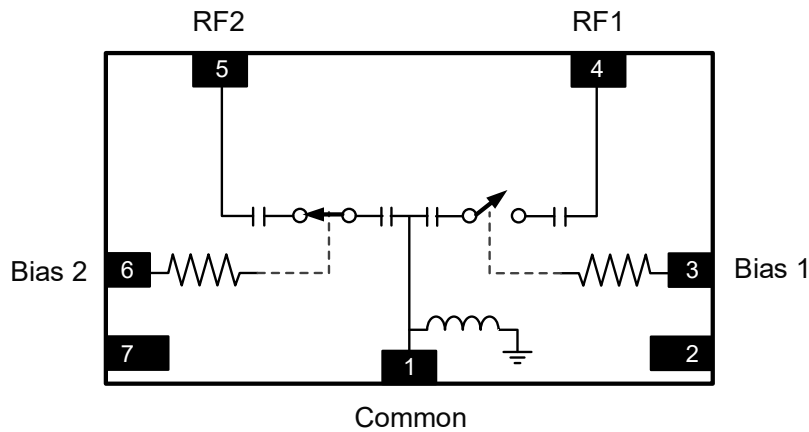
**Output Power over Reverse Bias Voltage @ +85°C, 29 GHz**



### Bias Diagrams & Tables

#### Functional Diagram

Showing the switch in following state: **RF1** = Isolation, **RF2** = Low Loss



#### Truth Table

Pin	Bias 1	Bias 2
	Pin 3	Pin 6
RF1 - Low Loss RF2 - Isolation	$V_R = -9\text{ V}$	$V_F = 4.5\text{ V}^3$
RF2 - Low Loss RF1 - Isolation	$V_F = 4.5\text{ V}^3$	$V_R = -9\text{ V}$

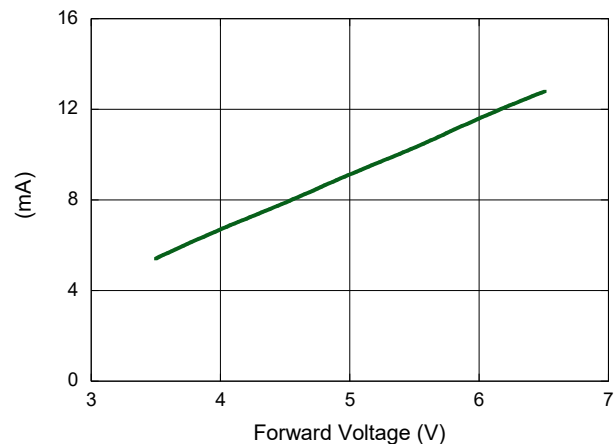
3. Internal bias resistors ( $400\ \Omega$ ) control the forward bias current ( $I_F$ ).

#### Bias Control

Optimal operation is achieved by simultaneous application of negative  $V_R$  voltage to the low loss switch path and positive  $V_F$  voltage to the isolating switch path.

In the low loss path, the diodes are reverse biased. In the isolating path, the diodes are forward biased.

**Forward Bias Current over Forward Bias Voltage**



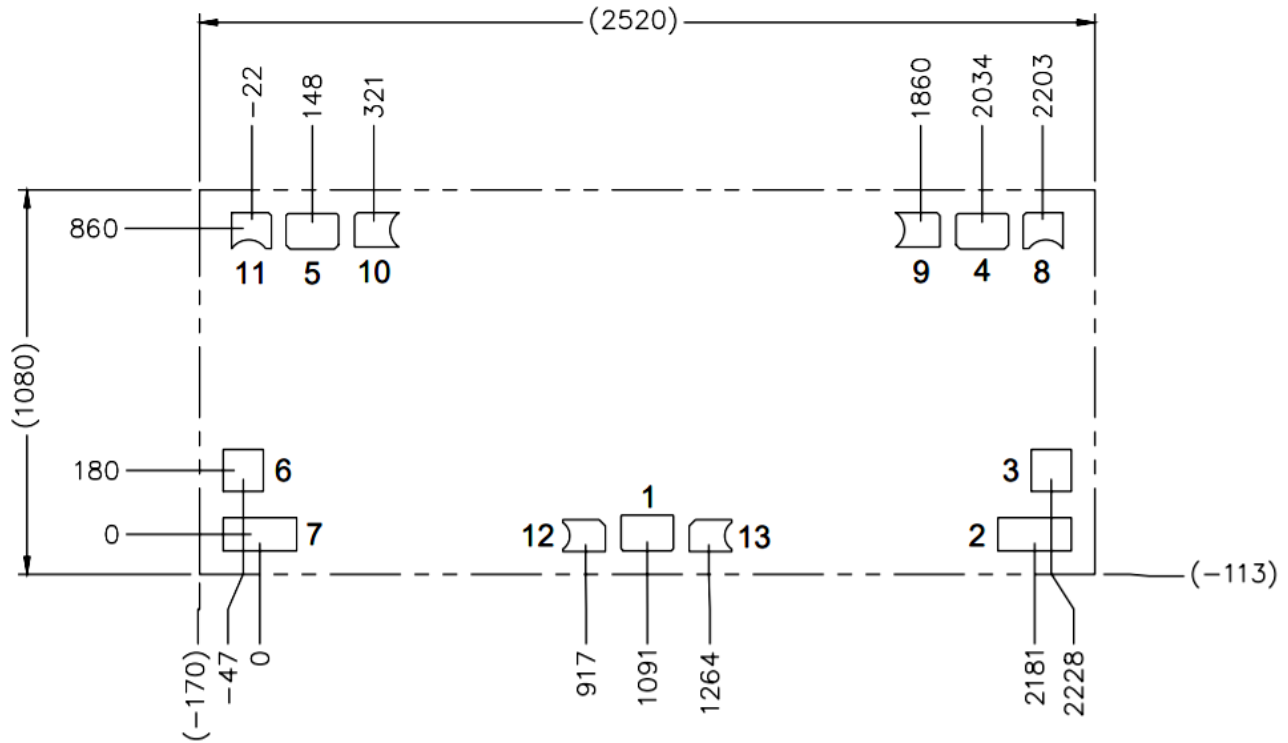
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## Outline Drawing



Dimensions indicated in  $\mu\text{m}$ .  
 Chip Thickness: 100  $\mu\text{m}$   
 RF Pads (1,4,5): 110 x 148  $\mu\text{m}$   
 DC Bias Pads (3 & 6): 113 x 118  $\mu\text{m}$   
 DC Pads (2 & 7): 93 x 207  $\mu\text{m}$

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