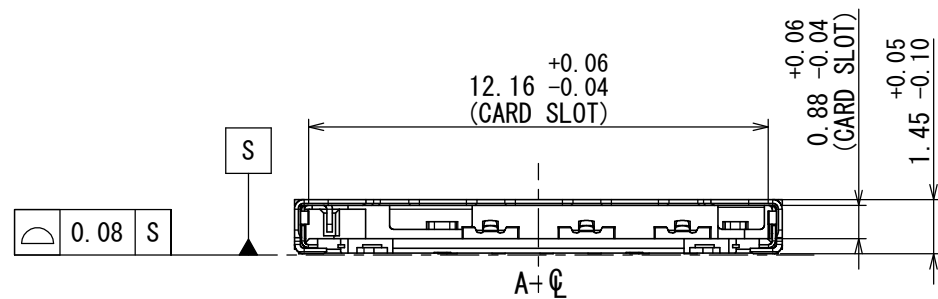
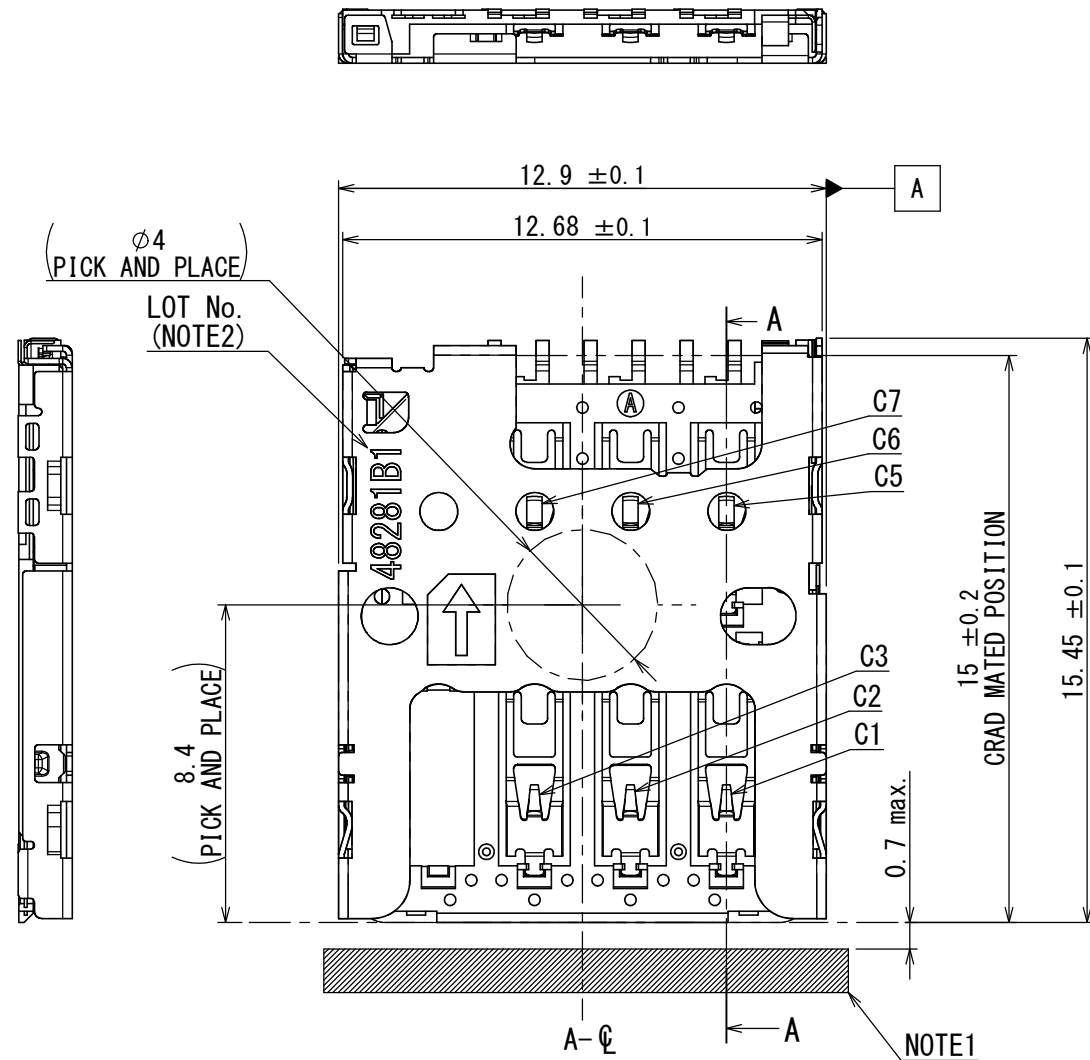
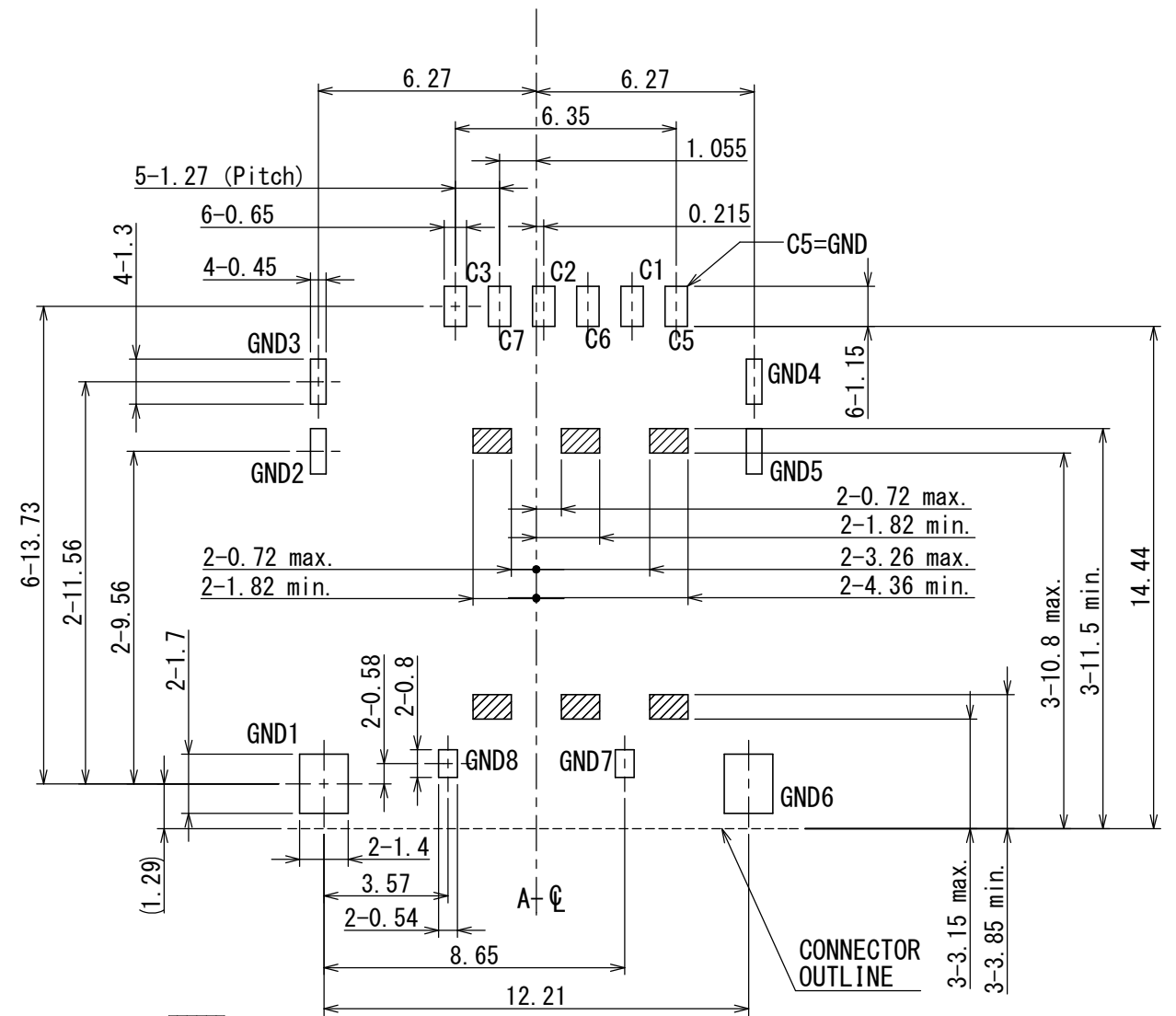
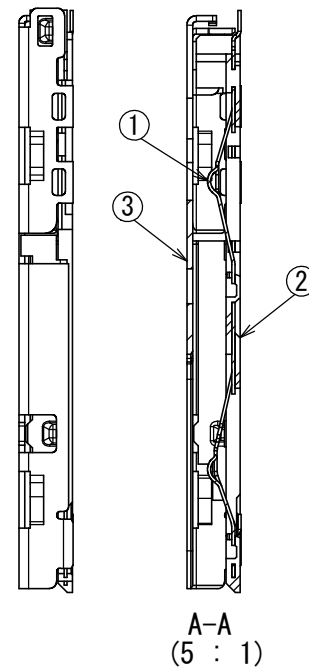


版数 VER.	年月日 DATE	CN NO.	変更内容 DESCRIPTION	製図 DR.	担当 CHK.	査閲 APPD.	承認 APPD.
2	29/JAN/2015	011160	Version No. added		K. MIKAWA	M. SHIMADA	A. NATORI



NOTE1. CARD STOPPER POSITION
NOTE2. LOT INFORMATION IS SHOWN AS BELOW.
i. e. 4 8 2 8 1 B 1

VERSION NO. (B1 or V*)
PRODUCTION LINE NO.
PRODUCT DATE (YMDD)

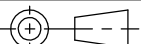


RESTRICTED AREA (No pattern and Via hole)

All patterns and Via holes under the connector should be coated by resist.

Recommended P.C.B Layout

3	COVER	1	STAINLESS	TERMINAL AREA :Au OVER Ni	-
2	INSULATOR	1	GLASS FILLED LCP	-	-
1	CONTACT	6	COPPER ALLOY	CONTACT AREA :Au OVER Ni TERMINAL AREA :Au OVER Ni	-
符号 NO.	名 称 DESCRIPTION	個 数 QTY.	材 料 MATERIAL	仕 上 FINISH	備 考 REMARKS

仕様書 (SPECIFICATION) JACS-11066*		第1版 (ORIGINAL DATE) 06/OCT/2014		尺度 (SCALE) 5:1	シリーズ (SERIES) SF53	日本航空電子工業株式会社  JAPAN AVIATION ELECTRONICS INDUSTRY, LTD.	図面番号 (DRAWING NO.) SJ115712	版数 (VER.) 2
一般公差 (GENERAL TOLERANCE) 寸法 (DIMENSION)		製図 DR.	名称 (TITLE) SF53S006VCB	質量 (MASS) —				
±0.8 × ±0.4 ×× ±0.1 ××× ±	角度 (ANGLES) ° ± °' ± 単位 (UNIT) : mm	担当 CHK. 査閲 APPD. 承認 APPD.						

Mouser Electronics

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