IS32LT3183A

AUTOMOTIVE MCU WITH LIN INTERFACE FOR RGB LED DRIVER

January 2023

GENERAL DESCRIPTIONS

The IS32LT3183A is a single chip RGB driver with a LIN interface suitable for automotive ambient color applications. The LIN master can send RGB color, intensity and control instructions over the LIN Bus and receives back status and error information. It is fully conformed to LIN standard, for data transmission rates up to 19.2kbps. The IS32LT3183A supports LIN SNPD (Slave Node Position Detection) using BSM (Bus Shunt Method).

The IS32LT3183A integrates key functional features for developing compact multicolor LED LIN nodes. An integrated low-drop voltage regulator to support internal circuit operation. It can sink a constant current of 60mA to each of the RGBW LEDs. In order to minimize current consumption, the IS32LT3183A supports a Sleep mode to power down with wake-up capability via the LIN bus. The integrated MCU is an 8051 based CPU core with 32kB embedded flash, of which each byte is protected by ECC. This is the highest reliability level of code storage for the challenging environment of automobile applications.

IS32LT3183A offers strong Electro Static Discharge (ESD) performance and can withstand high voltages on the LIN bus. LIN bus signal is designed to minimize Electro Magnetic Emissions (EME).

APPLICATIONS

- LIN RGB LED ambient lighting
- Dome LED lighting
- Dash board lighting
- LIN to SPI or LIN to I2C bridge
- General purpose MCU for LIN node slave operation

HV I/O CONFIGURATIONS

- 4x high voltage I/Os with up to 60mA configurable current source for RGBW LEDs
- 4x 16-bit PWM outputs
- Open/short diagnostic capability for LED
- 12-bit ADC
- SPI master interface
- I2C master interface
- Interrupt capability for all inputs
- GPIO with input de-bounce

FEATURES

- Wide supply voltage 5.5V ~ 18V continuous with max input voltage up to 40V
- Sleep mode supply current 60μA(max.) with wake-up via LIN bus capability
- 4 independent LED current sinks
  - Software programmable LED current, up to 60mA
  - Reconfigurable as GPIO, SPI master interface or I2C master interface
- Integrated MCU for LIN protocol handling and LIN message decoding
  - 1-T enhance 8051 core
  - 16MHz (±5%) internal OSC
  - 32kB Flash and 2kB SRAM
  - Each nibble of code is protected by ECC for double bit detection and single bit correction
  - LIN Interface
  - SPI/I2C master interface
  - GPIO and external Interrupt/wake-up
  - 12-Bit SAR ADC with conversion time up to 10μs
  - On-chip temperature sensor
  - Math Co-processor for 16-bit MUL and 32-bit DIV Operations
- LIN Interface
  - Baud rate up to 19.2kbps
  - Integrated LIN transceiver
  - Internal LIN slave termination resistor
  - Compliant to LIN 2.2A
  - Support SNPD (BSM) auto addressing
- Protections and ESD
  - 40V load dump protected
  - ±8kV for GPIO
  - Temperature compensation to protect LED
- LED drivers
  - LED color calibration via matrix calculation
  - Flash storage for calibration values
  - Intensity control (linear or logarithmic)
  - Dimming and color transition function with programmable transition time
  - Up to 16-Bit LED color range
  - PWM with spread spectrum to optimize EMI
  - LED temperature compensation
- Diagnostics
  - Open/Short LED detection
  - High temperature warning and shutdown
  - LIN retry mode on error detection
- SOP-8-EP package
- AEC-Q100 Qualified
- RoHS & Halogen-Free Compliance
- TSCA Compliance

TYPICAL APPLICATION CIRCUITE

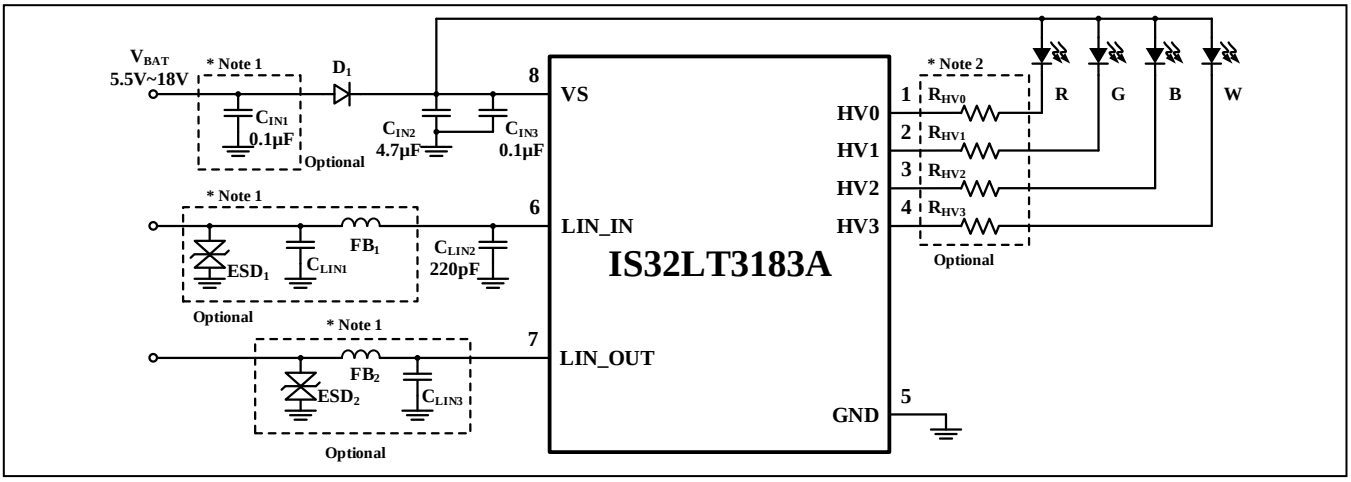
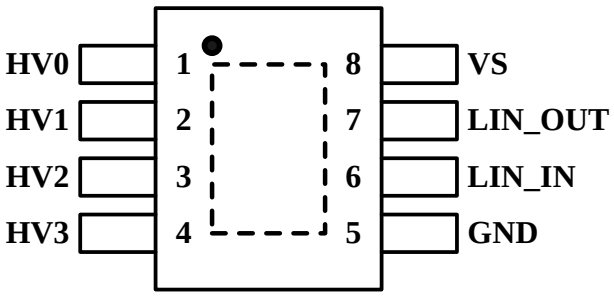


Figure 1 Typical Application Circuit

Note 1: These components are optional to optimize EMC and ESD performance.

Note 2: These power resistors are optional to minimize the power consumption on the driver.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-8-EP	

PIN DESCRIPTION

No.	Pin	Voltage Range	Description
1~4	HV0~HV3	IO HV	High voltage I/O.
5	GND	Power	Ground pin.
6	LIN_IN	Analogue HV	Connection to LIN bus, LIN bus shunt input.
7	LIN_OUT	Analogue HV	LIN bus shunt output.
8	VS	Power HV	Battery supply voltage; external protection against reverse polarity needed.
	Thermal Pad	-	Must be connected to GND.

Voltage Code	Voltage Range
Analogue	Analogue pin
Power	Power/supply pin
IO	Multifunctional pin (configurable pin)
HV	High voltage, VBAT or VS related

ORDERING INFORMATION
Automotive Range: -40°C To +125°C

Order Part No.	Package	QTY/Reel
IS32LT3183A-GRLA3-TR	SOP-8-EP, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS (NOTE 3)

Voltage at VS	-0.3V ~ +44V
Voltage at LIN_IN, LIN_OUT	-30V ~ +40V
Voltage at HV0, HV1, HV2, HV3	-0.3V ~ +44V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Power dissipation, $P_{D(MAX)}$	2.84W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	44°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	1.41°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

The IC can have 7 different hardware modes. The exact functionality of these modes depends on the hardware and software configuration:

Reset

- Triggered by hardware. When V_S drop below a critical level, the complete chip is powered down
- The analogue and digital supply regulators are disabled. No functionality is available in this mode

Normal Mode Main application running

- Microcontroller fully functional
- Analogue fully functional

Idle Mode Triggered by the software. Digital part can run at lower frequency (24kHz)

- Internal peripherals inaccessible (T0/T1/T2, UART2, I2C)
- LIN not possible
- External peripherals (external Interrupts) can wake up the CPU from Idle mode

Stop Mode Triggered by the software

- LIN not possible
- IOSC oscillator is disabled

Sleep Mode Triggered by the software

- Microcontroller powered down
- Digital and analogue supply powered down
- Sleep mode and wake-up functionality running on help supply VAUX

Under Voltage Triggered by the hardware under voltage detection Interrupt (EXIF_INT3: UVF)

- Microcontroller fully functional
- Power down behavior can be managed via software
- Reduced current capability on HVx below V_S=5.5V

Over Voltage Triggered by the hardware over voltage detection Interrupt (EXIF_INT3: OVF)

- Microcontroller fully functional
- Behaviour can be managed via software

OPERATING CONDITIONS (CONTINUE)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		5.5		18	V
T_A	Ambient temperature		-40		125	°C

ELECTRICAL CHARACTERISTICS

Following characteristics are valid over the full temperature range of $T_J=T_A$= -40°C ~ +125°C and a supply range of 5.5V ≤ V_S ≤ 18V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Global Parameters						
I_{NOM}	Normal mode working current	All pins are inputs, R30K_EN=1		10	15	mA
I_{SLEEP}	Sleep mode current	All pins are inputs, chip in Sleep mode; V_S=12V, T_A=25°C		40	60	µA
Frequencies						
ΔI_{OSC}	Tolerance of RC oscillator	I_{OSC}=16MHz	-5		+5	%
f_{SOSC}	Frequency separate 24kHz RC oscillator			24		kHz
$t_{STARTUP\_POR}$	Startup time of the system after power on	Time until internal dig reset is inactive (Note 4)			500	µs
$t_{STARTUP\_SLEEP}$	Startup time of the system after release of Sleep Mode	Time until internal dig reset is inactive (Note 4)			250	µs
VS – Programmable Under Voltage Interrupt Parameters						
$V_{UV\_RANGE\_VS}$	Programmable range for under voltage level UVOVTRIM (TM_UV [2:0])	000 (default)	4.5	5	5.5	V
		100	6.5	7.0	7.5	
		111	8.0	8.5	9.0	
$V_{HYST\_UV\_VS}$	Hysteresis for under voltage		0.1		1	V
t_{UV_VS}	Debouncing for under voltage	(Note 4)	10	30	60	ms
VS – Over Voltage (Load Dump) Interrupt Related Parameters						
V_{LDH}	Level for load dump Interrupt		29	31	33	V
V_{HYST_LD}	Hysteresis for load dump Interrupt		1	2.5	4	V
T_{LD}	Debouncing for load dump Interrupt	(Note 4)	50		100	µs
ADC (12Bit) Related Parameters						
V_{REF}	Ref voltage		2.46	2.5	2.54	V
DNL	Differential nonlinearity	(Note 4)	-5		+5	LSB
INL	Integral nonlinearity	(Note 4)	-8		+8	LSB
RESADC	Quantization steps			4096		LSB
ADCERR	Quantification error		-0.5		+0.5	LSB
t_{CONV}	Min. conversion Time	For max. ADC input frequency = 4MHz (Note 4)		8		µs

ELECTRICAL CHARACTERISTICS (CONTINUE)

Following characteristics are valid over the full temperature range of T_J =T_A= -40°C ~ +125°C and a supply range of 5.5V ≤ V_S ≤ 18V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Multi-Purpose High Voltage IOs (HV0~HV3)						
Common Parameters						
$I_{LEAKHVX}$	Leakage current in case HV0~HV3 are inputs		-5		5	µA
t_{DEBHVX}	Programmable Debounce time for HV0~HV3 HVx_DBWID [2:0] (Note 4)	000 (Default)		1.33		ms
		001		2.66		
		010		5.33		
		011		10.6		
		100		21.3		
		101		42.6		
		110		85.3		
		111		170.6		
Digital Input for Wake Up						
V_{INLH_WUHVX}	Digital WU input threshold level L => H	Active in Sleep Mode			2.4	V
V_{INHL_WUHVX}	Digital WU input threshold level H => L	Active in Sleep Mode	1.2			V
V_{HYST_WUHVX}	Hysteresis		0.1			V
Fast Digital Input (Not Active in Sleep Mode)						
$V_{INLHHVX}$	Fast Digital Input threshold level L => H				2.4	V
$V_{INHLHVX}$	Fast Digital Input threshold level H => L		1.2			V
$V_{HYSTHVX}$	Hysteresis		0.1			V
T_{MAXHVX}	Max. delay	For rising and falling edge (Note 4)			25	ns
Open Drain Switch						
$R_{OUTLHVX}$	ON – resistance of HVx	V_S=12V, HvxOD_EN=1 HV0~HV3=0.2V		20	40	Ω
Open Drain Constant Current Source						
I_{OUTHVX}	Output current of HVx	V_S>5.5V	0		60	mA
	Output current of HVx stepsize	V_S>5.5V, HVx _FS[4:0]=0x1F TM_GAIN[3:0] adjustment		4		mA
		V_S>5.5V, TM_GAIN[3:0]=0x0F HVx _FS[4:0] adjustment		2		

ELECTRICAL CHARACTERISTICS (CONTINUE)

Following characteristics are valid over the full temperature range of T_J=T_A= -40°C ~ +125°C and a supply range of 5.5V ≤ V_S ≤ 18V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{HR_MIN}	Min. headroom voltage	HVx current = 60mA, V_S=12V		0.9	1.2	V
		HVx current = 20mA, V_S=12V		0.6	0.8	V
I_{OUT_ERRHVX}	Output current of HVx relative error	5.5V≤ V_S ≤18V, 8mA< I_{OUT} ≤60mA	-7		+7	%
I_{OUT_ERRHVX}	Output current of HVx relative error	5.5V≤ V_S ≤18V, 4mA≤ I_{OUT} ≤8mA	-10		+10	%
HV0 Monitor						
Monitor Current						
I_{MON}	Monitor current	R2MAEN= 1	1.8	2	2.4	mA
$I_{MON\_VOUTSWING}$	Output voltage swing		V_S-4		V_S	V
Differential Amplifier						
V_{S_MON}	Monitor input voltage range	Vs≥ 8.5V	V_S-3.7		V_S-1.5	V
Gain	Vs Monitor Gain			0.2		-
Wake Up Related Parameters						
t_{WU}	Wake up filter time pins HVx	Sleep Mode, HVx rising & falling edge (Note 4)	25		50	µs
t_{WU_LIN}	Wake up filter time pin LIN	Time for dominant level after Sleep mode (Note 4)	15		150	µs
Temperature Sensor related parameters						
Temperature Shutdown Circuit						
T_{OT_ON}	Over temperature shutdown	Tested by special test mode only		160		°C
T_{OT_OFF}				140		°C
T_{OT_HYST}		(Note 4)		20		°C
Temperature Sensor (For ADC Measurement)						
T_{RANGE}	Temperature range	(Note 4)	-40		150	°C
T_{ACC}	Accuracy	(Note 4)	-10		10	°C
ΔV_{TC}	Sensitivity	(Note 4)		5		mV/°C

Note 4: Guaranteed by design & characterization, not tested in production.

ELECTRICAL CHARACTERISTICS (CONTINUE)

Following characteristics are valid over the full temperature range of $T_J = T_A$= -40°C ~ +125°C and a supply range of 8V ≤ V_S ≤ 18V unless otherwise noted.

LIN Related Parameters (adapted from Lin spec rev. 2.x) (8V ≤ V_{BAT} ≤ 18V)						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Pin LIN_IN						
Transmitter						
I_{BUS_LIM}	Short circuit bus current	V_{LIN_IN}=V_S, LIN driver on	40		200	mA
R_{SLAVE}	Pull up resistance bus, normal & standby mode	V_S=12V, V_{LIN_IN}=0V	28	30	40	kΩ
$I_{LIN\_PU-SLEEP}$	Pull up current, Sleep mode	V_{LIN_IN}=0V, V_S=12V, Sleep mode, RWK_EN=1	-100			µA
$I_{BUS\_PAS\_DOM}$	Input Leakage at the receiver include 30k pull up	V_{LIN_IN}=0V, V_S=12V, R30K_EN=1	-1			mA
$I_{BUS\_PAS\_REC}$	Bus reverse current, recessive	LIN driver off, V_S=8V, V_{LIN_IN}=18V			20	µA
$I_{BUS\_NO\_BAT}$	Bus reverse current loss of battery	V_S= 0V, V_{LIN_IN}=18V, LIN 2.1			50	µA
$I_{BUS\_NO\_GND}$	Bus current during loss of ground	V_S= V_{GND}=12V, 0< V_{LIN_IN}< 18V, J2602	-0.5		1	mA
V_{OLBUS}	Transmitter dominant voltage	Network load= 500Ω, TXD=0 (LIN driver on)	0		0.2	V_S
V_{OHBUS}	Transmitter recessive voltage	TXD= High	0.8		1	V_S
C_{BUS}	BUS input capacitance; Value for LIN conformance test	Pulse response via 10kΩ, V_{LIN_PULSE}= 12V, V_S open (Note 10)		25	35	pF
Receiver						
V_{BUSDOM}	Receiver dominant voltage				0.4	V_S
V_{BUSREC}	Receiver recessive voltage		0.6			V_S
V_{BUS_CNT}	Centre point of receiver threshold	V_{BUS_CNT}= (V_{BUSDOM}+V_{BUSREC})/2	0.475	0.5	0.525	V_S
V_{BUS_HYS}	Receiver Hysteresis	V_{BUS_HYS} = (V_{BUSREC}- V_{BUSDOM})			0.175	V_S
AC Parameters						
t_{RX_PDF}	Propagation delay receiver (Note 5, 6, 9)	C_{RXD}= 25pF falling edge			6	µs
t_{RX_PDR}	Propagation delay receiver (Note 5, 6, 9)	C_{RXD}= 25pF rising edge			6	µs
t_{RX_SYM}	Prop. Delay receiver symmetry	t_{RX_PDF} - t_{RX_PDR} (Note 9)	-2		2	µs
t_{REC_DEB}	Receiver debounce time (Note 10)	LIN rising & falling edge	0.5		4	µs
D_1	LIN duty cycle 1 (Note 6,7)	20kbps operation, Normal mode	0.396			-
D_2	LIN duty cycle 2 (Note 6,7)	20kbps operation, Normal mode			0.581	-
D_3	LIN duty cycle 3 (Note 6,7)	10.4kbs operation, Low speed mode	0.417			-

ELECTRICAL CHARACTERISTICS (CONTINUE)

Following characteristics are valid over the full temperature range of T_J =T_A= -40°C ~ +125°C and a supply range of 8V ≤ V_S ≤ 18V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
D_4	LIN duty cycle 4 (Note 6,7)	10.4kbs operation, Low speed mode			0.590	-
Δt_3	$t_{REC(MAX)}$ –$t_{DOM(MIN)}$ (Note 8)	10.4kbs operation, Low speed mode			15.9	µs
Δt_4	$t_{REC(MIN)}$ –$t_{DOM(MAX)}$ (Note 8)	10.4kbs operation, Low speed mode			17.28	µs
t_{TXD_TO}	TXD dominant time out (Note 10)	Normal mode, V_{TXD}= 0V		64		ms
LIN Auto-Addressing LIN_IN/LIN_OUT						
V_{S_RG}	Functional range LIN auto-addressing		9		15	V
$R_{PU\_LIN\_SLAVE}$	LIN slave pull up resistance		28	30	40	kΩ
I_{SHUNT}	Bus pull-up source current for auto-addressing			2		mA
V_{LIN}	LIN bus voltage range		0		2.5	V
R_{SHUNT}	LIN shunt resistor (Internal)			1		Ω

Note 5: This parameter is tested by applying a square wave signal to the LIN. The access to internal signals RXD, TXD will be performed by test mode. The minimum slew rate for the LIN rising and falling edges is 50V/us.

Note 6: See Figure 2: LIN timing diagram

Note 7: Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled

Note 8: In accordance to SAE J2602

Note 9: Parameter in relation to internal signal TXD

Note 10: Guaranteed by design & characterization, not measured in production.

As shown in figure, both worst case duty cycles can be calculated as follows:

Dwc1 = $t_{BUS\_rec(min)}$ / 2 × t_{Bit}

Dwc2 = $t_{BUS\_rec(max)}$ / 2 × t_{Bit}

Thresholds for duty cycle calculation in accordance to LIN2.x:

Baud Rate	20k Baud	10.4k Baud
t_{BIT}	50µs	96µs
Dwc1	D1	D3
Dwc2	D2	D4
THREC(MAX)	0.744 VS_TX	0.778 VS_TX
THDOM(MAX)	0.581 VS_TX	0.616 VS_TX
THREC(MIN)	0.422 VS_TX	0.389 VS_TX
THDOM(MIN)	0.284 VS_TX	0.251 VS_TX

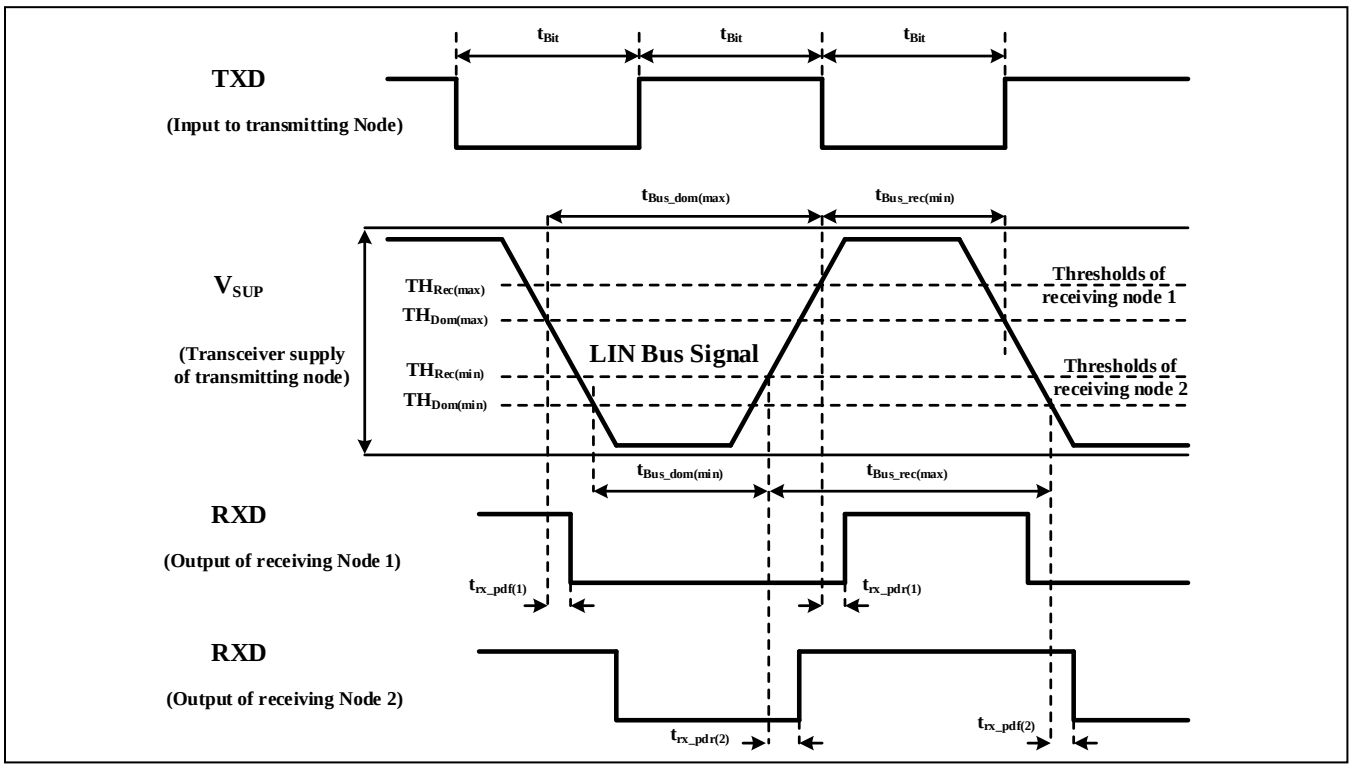
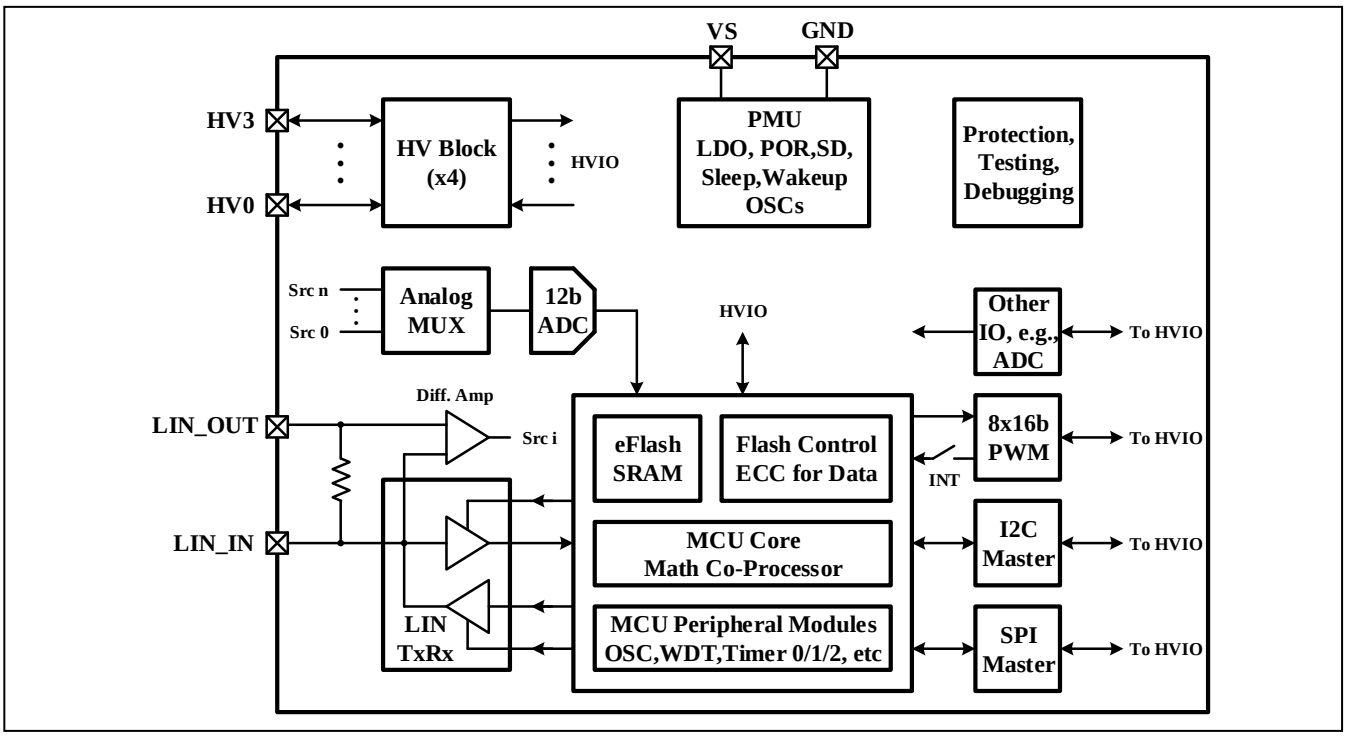


Figure 2 LIN Timing Diagram: Relation Between Propagation Delay And Duty Cycle

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

ENHANCED 1-CYCLE 8051 CPU

The CPU core is an enhanced version of standard 8051, which a RISC architecture and maintains binary instruction set compatible with the industry standard 8051. An average of 10 times performance enhancement in typical applications can be easily achieved. The CPU operates at 20-bit addressing space that allows up to 1M bytes of program and data space for expansion. It also includes the following enhanced features compared with standard 8051:

- 16-bit LARGE addressing mode and 20-bit FLAT addressing mode control register ACON
- Two data pointers DPTR and DPTR1, and additional DPS, DPX, DPX1, MXAX registers for MOVX instruction
- 8-bit stack pointer for LARGE mode and 16-bit extended stack pointer for FLAT mode control register ESP
- Hardware Multiplication and Division Unit (MDU) provides 12 times faster performance using MD[5-0] and ARCON
- Programmable wait state for program space for on-chip flash memory using WTST register
- 256 Bytes of Direct Data Memory
- Enhanced Interrupt Controller allows 15 Interrupt sources and 2 priority levels.
- Power Saving modes include Idle mode, Sleep mode and Stop mode.
- Access Control of critical registers – TA and TB registers

In addition to standard 8051 peripherals, the CPU core also integrates the following peripherals, which are in the same CPU clock domain.

- 4 I/O ports, HV0-HV3 related to port[3:0]
- 30-bit Watchdog Timer. WDT, WDCON, and CKCON registers
- Three 16-bit Timers, T0/T1 and T2. TCON, RLDL, RLDH, TL2, TH2, and T2CON registers
- I2C Master Controller. I2CMSA, I2CMCR, I2CMBUF, and I2CMTP register
- SPI Master Controller
- Two 16-bit Timers T3/T4 and one 24-bit Timer T5

MEMORY MAP

The following chart shows the memory mapping of IS32LT3183A. On the right, it shows the flash memory space. IS32LT3183A has a 32KB embedded flash, which is organized as 64 pages and each page has storage space of 512 byte. Boot code is stored between 0x7000H to 0x7FFFH, from page 56 to 63. Page 0 is reserved for Interrupt, while page 55 is reserved for protected key (from 0x6FF8 to 0x6FFF).

The flash has a separate, independent128 byte of information block page (IFB). IFB serves two purposes in upper and lower locations. Lower location 0x00 – 0x3F is used for storing manufacturing and calibration parameters in manufacturing tests. IFB upper location 0x40 – 0x7B is used for one-time programmable memory for user program. IFB is protected and cannot be erased by end users. For details of IFB information, please refer to ISSI's customer support.

On the left, it shows the 8051 standard memory mapping. These mapped areas are described in detail in this document, along with the register's associated functions. Assuming readers are familiar with 8051 standard operations and peripherals, the compatible functions are not covered here.

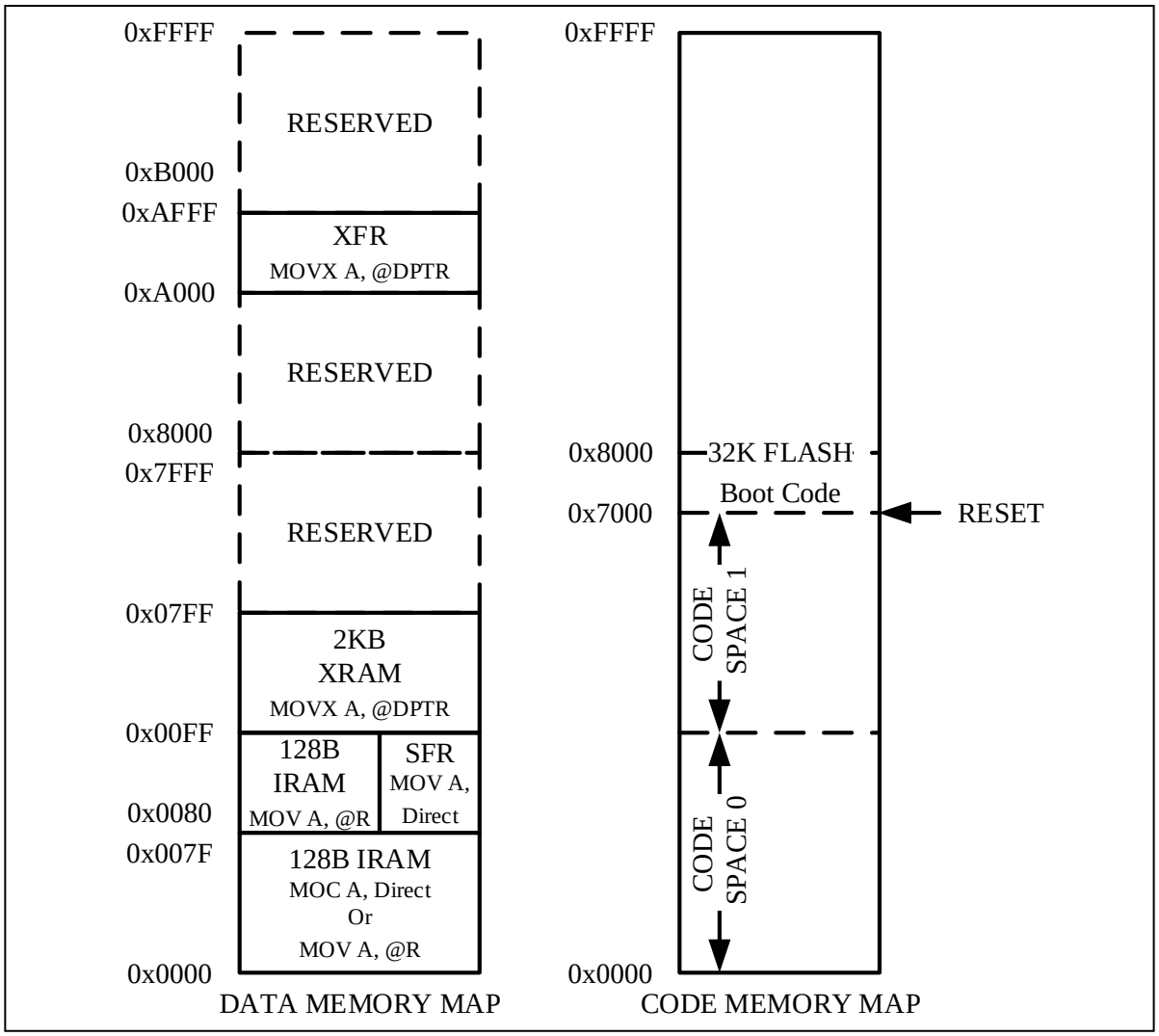


Figure 3 Memory Mapping of IS32LT3183A

REGISTER MAP: SFR (0x80 – 0xFF) and XFR (0xA000 – 0xAFFF)

The SFR address map maintains maximum compatibilities to most commonly used 8051 like MCU. The following table shows the SFR address map. Since SFR can be accessed by direct addressing mode, registers of built-in peripherals that require fast access are mostly located in SFR. XFR is mainly used for on-chip peripheral control and configurations.

REGISTER MAP: SFR (0x80 – 0xFF)

Address	0	1	2	3	4	5	6	7
0XF0	B	-	-	-	I2CMSA	I2CMCR	I2CMBUF	I2CMTP
0XE0	ACC	-	-	-	-	-	-	-
0XD0	PSW	-	-	-	-	-	-	-
0XC0	SCON1	SBUF1	SCON2	I2CMTO	PMR	STATUS	MCON	TA
0XB0	P3	-	CCAPM0	CCAPM1	CCAPM2	CCAPM3	CCAPM4	CCAPM5
0XA0	P2	SPICR	SPIMR	SPIST	SPIDATA	SFIFO2	SBUF2	SINT2
0X90	P1	EXIF	WTST	DPX	CMPST	DPX1	-	-
0X80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON
	8	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0XF8	EXIP	MD0	MD1	MD2	MD3	MD4	MD5	ARCON
0XE8	EXIE	CH	MXAX	-	-	-	-	P4
0XD8	WDCON	CL	DPXR	I2CSCON2	I2CSST2	I2CSADR2	I2CSDAT2	P5
0XC8	T2CON	TB	RLDL	RLDH	TL2	TH2	ADCCFG3	T34CON
0XB8	IP	ADCCFG1	ADCAL	ADCAH	ADCBL	ADCBH	ADCCL	ADCCH
0XA8	IE	ADCCFG2	ADCDL	ADCDH	TL4	TH4	TL3	TH3
0X98	SCON0	SBUF0	-	ESP	-	ACON	-	WKMASK
0X88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CKSEL

REGISTER MAP: XFR (0xA000 – 0xAFFF)

Address	0	1	2	3	4	5	6	7
A000	-	-	-	T5CON	TL5	TH5	TT5	-
A010	-	-	FLSHSPRT	FLSHCPRT	-	-	-	-
A020	FLSHCMD	FLSHDAT	FLSHADH	FLSHADL	ISPCLKF	ECCSTA	ECCCFG	-
A030	-	-	-	-	-	-	-	-
A040	HVIOCFA0	HVIOCFB0	HVIOCFC0	HVIOCFD0	HVIOCFA1	HVIOCFB1	HVIOCFC1	-
A050	HVIOINT0	HVIOINT1	HVIOINT2	HVIOINT3	-	-	-	-
	8	**9**	**A**	**B**	**C**	**D**	**E**	**F**
A008	REGTRIM	REFTRIM	REFILED	REFGLED	REF2MA	UVOVTRIM	BTTRIM	PWRINT
A018	IOSCFTRM	-	-	-	-	-	-	-
A048	HVIOCFA2	HVIOCFB2	HVIOCFC2	-	HVIOCFA3	HVIOCFB3	HVIOCFC3	HFFILTER
A058	HVIODBN0	HVIODBN1	HVIODBN2	HVIODBN3	-	-	-	-

Address	0	1	2	3	4	5	6	7
A080	PWMHRL	PWMHRH	PWMHGL	PWMHGH	PWMHBL	PWMHBH	PWMHWL	PWMHWH
A090	LINCTRL	LINCNTRH	LINCNTRL	LINSBRH	LINSBRL	LININT	LININTEN	-
A0A0	LINTCON	TXDTOL	TXDTOH	RXDTOL	RXDTOH	BSDCLR	BSDCLRH	BSDWKC
	8	**9**	**A**	**B**	**C**	**D**	**E**	**F**
A088	-	PWMHUPD	PWMHOSC	OSDLY	PWMHTRG	PWMINTE	PWMHCFG	PWMHINT
A098	-	-	-	-	-	-	R2MACFG	SSCCFG
A0A8	BSDACT	-	XCVRCFG	SNPDCFG	SNPDINT	-	-	-

CPU REGISTERS

ACC **Accumulator** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	ACC[7:0]							
WR	ACC[7:0]							

SFR Address: 0xE0 **Default: 0b00000000**

ACC is the CPU accumulator register and is involved in direct operations of many instructions. ACC is bit addressable.

B **B Register** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	B[7:0]							
WR	B[7:0]							

SFR Address: 0xF0 **Default: 0b00000000**

B register is used in standard 8051 multiply and divide instructions and also used as an auxiliary register for temporary storage. B is also bit addressable.

PSW **Program Status Word** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	CY	AC	FO	RS1	RS0	OV	UD	P
WR	CY	AC	FO	RS1	RS0	OV	UD	P

SFR Address: 0xD0 **Default: 0b00000000**

CY	Carry Flag
AC	Auxiliary Carry Flag (BCD Operations)
FO	General Purpose
RS1, RS0	Register Bank Select
OV	Overflow Flag
UD	User Defined (reserved)
P	Parity Flag

SP **Stack Pointer** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	SP[7:0]							
WR	SP[7:0]							

SFR Address: 0x81 **Default: 0b00000000**

PUSH will result ACC to be written to SP+1 address. POP will load ACC from IRAM with the address of SP.

ESP **Extended Stack Pointer** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	ESP[7:0]							
WR	ESP[7:0]							

SFR Address: 0x9B **Default: 0b00000000**

In FLAT address mode, ESP and SP together form a 16-bit address for stack pointer. ESP holds the higher byte of the 16-bit address.

STATUS **Program Status Word** **RO**

Bit	7	6	5	4	3	2	1	0
RD	-	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0
WR	-	-	-	-	-	-	-	-

SFR Address: 0xC5 **Default: 0b00000000**

HIP High Priority (HP) Interrupt Status
HIP=0 indicates no HP Interrupt
HIP=1 indicates HP Interrupt progressing

LIP Low Priority (LP) Interrupt Status
LIP=0 indicates no LP Interrupt
LIP=1 indicates LP Interrupt progressing

SPTA1 UART1 Transmit Activity Status
SPTA1=0 indicates no UART1 transmit activity
SPTA1=1 indicates UART1 transmit active

SPRA1 UART1 Receive Activity Status
SPRA1=0 indicates no UART1 receive activity
SPRA1=1 indicates UART1 receive active

SPTA0 UART0 Transmit Activity Status
SPTA0=0 indicates no UART0 transmit activity
SPTA0=1 indicates UART0 transmit active

SPRA0 UART0 Receive Activity Status
SPRA0=0 indicates no UART0 receive activity
SPRA0=1 indicates UART0 receive active

The program should check status conditions before entering SLEEP, STOP, IDLE, or PMM modes to prevent loss of intended functions from delayed entry until these events are finished.

Addressing Timing and Memory Modes

The clock speed of an MCU with embedded flash memory is usually limited by the access time of on-chip flash memory. While in modern process technology, the CPU can operate faster, the access time of flash memory is usually around 40 nanoseconds, which becomes a bottleneck for CPU performance. To mitigate this problem, a programmable wait state function is incorporated to allow faster CPU clock rate to access slower embedded flash memory. The wait state is controlled by WTST register as shown in the following.

WTST **TA Protected** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	WTST3	WTST2	WTST1	WTST0
WR	-	-	-	-	WTST3	WTST2	WTST1	WTST0

SFR Address: 0x92 **Default: 0b00000111**

WTST[3:0] Wait State Control register. WTST sets the wait state in CPU clock period

WTST3	WTST2	WTST1	WTST0	Wait State Cycle
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

The default setting of the program wait state register after reset is 0x07 and the software must initialize the setting to change the wait state setting. If ISOCDIV=0, then WTST should be set higher than 1 to allow enough read access time, others can set WTST to minimum.

MCON XRAM Relocation Register R/W TA Protected

Bit	7	6	5	4	3	2	1	0
RD	MCON[7:0]							
WR	MCON[7:0]							

SFR Address: 0xC6 **Default: 0b00000000**

MCON holds the starting address of XRAM in 4KB steps. For example, if MCON[7:0]=0x01, the starting address is 0x001000. MCON is not meaningful in IS32LT3183A because it only contains on-chip XRAM and MCON should not be modified from 0x00.

The LARGE mode, addressing mode is compatible with standard 8051 in 16-bit address. FLAT mode extends the program address to 20-bit and expands the stack space to 16-bit data space. The data space is always 16-bit in either LARGE or FLAT mode.

ACON R/W TA Protected

Bit	7	6	5	4	3	2	1	0
RD	-	-	IVECSEL	-	DPXREN	SA	AM1	AM0
WR	-	-	IVECSEL	-	DPXREN	SA	AM1	AM0

SFR Address: 0x9D **Default: 0b00000000**

ACON is addressing mode control register.

IVECSEL Interrupt Vector Selection
INTVSEC=1 maps the Interrupt vector to 0x7000 space.
INTVSEC=0 maps to normal 0x0000 space

DPXREN DPXR Register Control Bit.
If DPXREN is 0, “MOVX, @Ri” instruction uses P2 (0xA0) register and XRAM Address [15:8]. If DPXREN is 1, DPXR (0xDA) register and XRAM Address [15:8] is used.

SA	Extended Stack Address Mode Indicator. This bit is read-only. 0 – 8051 standard stack mode where stack resides in internal 256-byte memory 1 – Extended stack mode. Stack pointer is ESP:SP in 16-bit addressing to data space.
AM1, AM0	AM1 and AM0 Address Mode Control Bits 00 – LARGE address mode in 16-bit 1x – FLAT address mode with 20-bit program address

MOVX A, @Ri Instructions

DPXR **R/W**

Bit	7	6	5	4	3	2	1	0
RD	DPXR[7:0]							
WR	DPXR[7:0]							

SFR Address: 0xDA **Default: 0b00000000**

DPXR is used to replace P2[7:0] for high byte of XRAM address bit[15:8] for ”MOVX, @Ri” instructions only if DPXREN=1.

MXAX **MOVX Extended Address Register** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	MXAX[7:0]							
WR	MXAX[7:0]							

SFR Address: 0xEA **Default: 0b00000000**

MXAX is used to provide top 8-bit address for “MOVX @Ri” instructions only. MXAX does not affect other MOVX instructions.

When accessing XRAM using “MOVX, @DPTR” instruction, the address of XRAM access is formed by DPHi:DPLi depending on which data pointer is selected. Another form of MOVX instruction is “MOVX, @Ri”. This instruction provides an efficient programming method to move content within a 256-byte data block. In “@RI” instruction, the XRAM address [15:8] can be derived from two sources. If ACON.DPXREN = 0, the high order address [15:8] is from P2 (0xA0), if ACON.DPXREN = 1, the high order address is from DPXR (0xDA) register.

The maximum addressing space of XRAM is up to 16MB thus requiring 24-bit address. For “MOVX, @DPTR”, the XRAMADDR [23:16] is from either DPX (0x93) or DPX1 (0x95) depending on which data pointer is selected. For “MOVX, @Ri”, the XRAMUADDR [23:16] is from MXAX (0xEA) register.

Dual Data Pointers And MOVX Operations

In standard 8051, there is only one data pointers DPH:DPL to perform MOVX. The enhanced CPU provides 2nd data pointer DPH1:DPL1 to speed up the movement, or copying of data block. The active DPTR is selected by setting DPS (Data Pointer Select) register. Through the control DPS, efficient programming can be achieved.

DPS **Data Pointer Select** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	ID1	ID0	TSL	-	-	-	-	SEL
WR	ID1	ID0	TSL	-	-	-	-	SEL

SFR Address: 0x86 **Default: 0b00000000**

ID[1:0]	Define the operation of Increment Instruction of DPTR, “INC DPTR”. Standard 8051 only have increment DPTR instruction. ID[1:0] changes the definitions of “INC DPTR” instruction and allows flexible modifications of DPTR when “INC DPTR” instructions is executed.

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR	INC DPTR1
0	1	DEC DPTR	INC DPTR1
1	0	INC DPTR	DEC DPTR1
1	1	DEC DPTR	DEC DPTR1

TSL Enable toggling selection of DPTR selection. When this bit is set, the selection of DPTR is toggled when DPTR is used in an instruction and executed.

SEL DPTR selection bit. Set to select DPTR1, and clear to select DPTR. SEL is also affected by the state of ID[1:0] and TSL after DPTR is used in an instruction. When read, SEL reflects the current selection of command.

DPL Data Pointer Low R/W

Bit	7	6	5	4	3	2	1	0
RD	DPL[7:0]							
WR	DPL[7:0]							

SFR Address: 0x82 **Default: 0b00000000**

DPL register holds the low byte of data pointer, DPTR.

DPH Data Pointer High R/W

Bit	7	6	5	4	3	2	1	0
RD	DPH[7:0]							
WR	DPH[7:0]							

SFR Address: 0x83 **Default: 0b00000000**

DPH register holds the high byte of data pointer, DPTR.

DPL1 Extended Data Pointer Low R/W

Bit	7	6	5	4	3	2	1	0
RD	DPL1[7:0]							
WR	DPL1[7:0]							

SFR Address: 0x84 **Default: 0b00000000**

DPL1 register holds the low byte of extended data pointer 1, DPTR1.

DPH1 Extended Data Pointer High R/W

Bit	7	6	5	4	3	2	1	0
RD	DPH1[7:0]							
WR	DPH1[7:0]							

SFR Address: 0x85 **Default: 0b00000000**

DPH1 register holds the high byte of extended data pointer 1, DPTR1.

DPX Data Pointer Top R/W

Bit	7	6	5	4	3	2	1	0
RD	DPX[7:0]							
WR	DPX[7:0]							

SFR Address: 0x93 **Default: 0b00000000**

DPX is used to provide top 8-bit address of DPTR when address above 64KB. The lower 16-bit address is formed by DPH and DPL.DPX is not affected in Large mode, and will form full 24-bit address in Flat mode, meaning auto increment and decrement when DPTR is changed. Since IS32LT3183A only has on-chip data space, DPX value has no effect.

DPX1 Extended Data Pointer Top R/W

Bit	7	6	5	4	3	2	1	0
RD	DPX1[7:0]							
WR	DPX1[7:0]							

SFR Address: 0x95 **Default: 0b00000000**

DPX1 is used to provide top 8-bit address of DPTR when address above 64KB. The lower 16-bit address is formed by DPH1 and DP1L.DPX1 is not affected in Large mode, and will form full 24-bit address in Flat mode, meaning auto increment and decrement when DPTR is changed. Since 3183A only has on-chip data space, DPX1 value has no effect.

INTERRUPT SYSTEM

The CPU implements an enhanced Interrupt Control that allows total 15 Interrupt sources and each with two programmable priority levels. The Interrupts are sampled at rising edge of SYSCLK. If Interrupts are present and enabled, the CPU enters Interrupt service routine by vectoring to the highest priority Interrupt. Of the 15 Interrupt sources, 7 of them are from CPU internal integrated peripherals, 6 of them are for on-chip external peripherals, and 2 of them are used for external pin Interrupt expansion. When an Interrupt is shared, the Interrupt service routine must determine which source is requesting the Interrupt by examining the corresponding Interrupt flags of sharing peripherals.

The following table shows the Interrupt sources and corresponding Interrupt vectors. The Flag Reset column shows whether the corresponding Interrupt flag is cleared by hardware (self-cleared) or software. Please note the software can only clear the Interrupt flag but not set the Interrupt flag. The Natural Priority column shows the inherent priority if more than one Interrupts are assigned to the same priority level. Please note that the Interrupts assigned with higher priority levels always get serviced first compared with Interrupts assigned with lower priority levels regardless of the natural priority sequence.

Interrupt	Peripheral Source Description	Vectors IVECSEL=0/1	FLAG RESET	Natural Priority
PINT0	Expanded Pin INT0.x	0x0003/0x7003	Software	1
TF0	Timer 0	0x000B/0x700B	Hardware	2
PINT1	Expanded Pin INT1.x	0x0013/0x7013	Software	3
TF1	Timer 1	0x001B/0x701B	Hardware	4
TF2	Timer 2	0x002B/0x702B	Software	6
TI2/RI2	EUART2/LIN/LIN_FAULT	0x0033/0x7033	Software	7
I2CM	I^2C Master	0x003B/0x703B	Software	8
INT2	PWMH/HV Fault	0x0043/0x7043	Software	9
INT3	Power Supply and Thermal Shut Down	0x004B/0x704B	Software	10
INT4	ADC	0x0053/0x7053	Software	11
WDIF	Watchdog	0x005B/0x705B	Software	12
INT7	SPI/ECC	0x006B/0x706B	Software	14
INT8	T3/T4/T5	0x0073/0x7073	Software	15

The Interrupt related registers are listed in the following. Each Interrupt can be individually enabled or disabled by setting or clearing corresponding bits in IE, EXIE and integrated peripherals' control registers.

IE Interrupt Enable Register R/W

Bit	7	6	5	4	3	2	1	0
RD	EA	ES2	ET2	-	ET1	PINT1EN	ET0	PINT0EN
WR	EA	ES2	ET2	-	ET1	PINT1EN	ET0	PINT0EN

SFR Address: 0xA8 **Default: 0b00000000**

EA Global Interrupt Enable bit.
ES2 LIN-capable16550-like UART2 Interrupt Enable bit.
ET2 Timer 2 Interrupt Enable bit.
ET1 Timer 1 Interrupt Enable bit.
PINT1EN Pin PINT1.x Interrupt Enable bit.
ET0 Timer 0 Interrupt Enable bit.
PINT0EN Pin PINT0.x Interrupt Enable bit.

EXIE Extended Interrupt Enable Register R/W

Bit	7	6	5	4	3	2	1	0
RD	EINT8	EINT7	EINT6	EWDI	EINT4	EINT3	EINT2	EI2CM
WR	EINT8	EINT7	EINT6	EWDI	EINT4	EINT3	EINT2	EI2CM

SFR Address: 0xE8 **Default: 0b00000000**

EINT8 Timer 3/4/5 Interrupt Enable bit.
EINT7 SPI, ECC Interrupt Enable bit.
EWD1 Watchdog Timer Interrupt Enable bit.
EINT4 ADC Interrupt Enable bit.
EINT3 Power Supply and Thermal Shut Down Interrupt Enable bit.
EINT2 PWMH and HV Fault Detection Interrupt Enable bit.
EI2CM I2C Master Interrupt Enable bit.

Each Interrupt can be individually assigned to either high or low. When the corresponding bit is set to 1, it indicates it is of high priority.

IP Interrupt Priority Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	PS2	PT2	PS0	PT1	PX1	PT0	PX0
WR	-	PS2	PT2	PS0	PT1	PX1	PT0	PX0

SFR Address: 0xB8 **Default: 0b00000000**

PS2 LIN-capable 16550-like UART2 Priority bit.
PT2 Timer 2 Priority bit.
PT1 Timer 1 Priority bit.
PX1 Pin Interrupt INT1 Priority bit.
PT0 Timer 0 Priority bit.
PX0 Pin Interrupt INT0 Priority bit.

EXIP Extended Interrupt Priority Register R/W

Bit	7	6	5	4	3	2	1	0
RD	EINT8	EINT7	EINT6	EWDI	EINT4	EINT3	EINT2	EI2CM
WR	EINT8	EINT7	EINT6	EWDI	EINT4	EINT3	EINT2	EI2CM

SFR Address: 0xF8 **Default: 0b00000000**

EINT8 INT8 Timer 3/4/5 Priority bit.
EINT7 INT7 SPI/ECC Priority bit.
EWDI Watchdog Priority bit.
EINT4 INT4 ADC Priority bit.

EINT3 INT3 Power Supply and Thermal Shut Down Priority bit.
EINT2 INT2 PWMH and HV Fault Detection Priority bit.
EI2CM I2C Master Priority bit.

EXIF Extended Interrupt Flag R/W

Bit	7	6	5	4	3	2	1	0
RD	INT8F	INT7F	INT6F	-	INT4F	INT3F	INT2F	I2CMIF
WR	-	-	-	-	-	-	-	I2CMIF

SFR Address: 0x91 **Default: 0b00000000**

INT8F INT8 Timer ¾/5 Interrupt Flag bit
INT7F INT7 SPI, ECC Interrupt Flag bit
INT4F INT4 ADC Interrupt Flag bit
INT3F INT3 Power Supply and Thermal Shut Down Interrupt Flag bit
INT2F INT2 PWMH and HV Fault Detection Interrupt Flag bit
I2CMIF I2C Master Interrupt Flag bit. This bit must be cleared by software

Writing to INT2F to INT8F has no effect.

The Interrupt flag of internal peripherals are stored in the corresponding flag registers in the peripheral and EXIF registers. These peripherals include T0, T1, T2, and WDT. Therefore, to clear the Interrupt flags, the software needs to clear the corresponding flags located in the peripherals (for T0, T1, and T2, and WDT). For I2CM, the Interrupt flag is located in the EXIF register bit I2CMIF. This needs to be cleared by software.

INT2 to INT8 are used to connect to the external peripherals. INT2F to INT8F are direct equivalents of the Interrupt flags from the corresponding peripherals. These peripherals include ECC, I2Cs, PWM, ADC, etc.

HVIO are used for external GPIO pin Interrupts. All GPIO pin can be enabled to generate the HVIO depending on its IO configured registers setting. Each GPIO pin also contains the rising/falling edge detections and either or both edges can be used for Interrupt triggering. The same signaling can be used for generating wake-up.

TCON R/W

Bit	7	6	5	4	3	2	1	0
RD	TF1	TR1	TF0	TR0	PINT1F	-	PINT0F	-
WR	-	TR1	-	TR0	PINT1F	-	PINT0F	-

SFR Address: 0x88 **Default: 0b00000000**

TF1 Timer 1 Interrupt Flag bit. TF1 is cleared by hardware when entering the Interrupt routine.
TR1 Timer 1 Run Control bit. Set to enable Timer 1.
TF0 Timer 0 Interrupt Flag. TF0 is cleared by hardware when entering the Interrupt routine.
TR0 Timer 0 Run Control bit. Set to enable Timer 0.
PINT1F Pin INT1 Interrupt Flag bit.
PINT0F Pin INT0 Interrupt Flag bit.

REGISTER ACCESS CONTROL

One important aspect of the embedded MCU is its reliable operations under a harsh environment. Many system failures result from the accidental loss of data or changes of critical registers that may lead to catastrophic effects. The CPU provides several protection mechanisms, which are described in this section.

TA Time Access A Control Register2 WO

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	-	TASTAT
WR	TA Register							

SFR Address: 0xC7 **Default: 0b00000000**

TA access control emulates a ticket that must be purchased before modifying a critical register. To modify or write into a TA protected register, TA must be accessed in a predefined sequence to obtain the ticket. The ticket is used when an intended modification operation is done to the TA protected register. To obtain the next access a new ticket must be obtained again by performing the same predefined sequence on TA. TA does not limit the read access of the TA protect registers. The TA protected register includes WDCON (0xD8), MCON (0xC6), and ACON (0x9D) registers. The following predefined sequence is required to modify the content of MCON.

MOV TA, #0xAA;

MOV TA, #0x55;

MOV MCON, #0x01;

Once the access is granted, there is no time limitation of the access. The access is voided if any operation is performed in TA address. When read, the bit of TA indicates whether TA is locked or not (1 indicates “unlock” and 0 indicates “lock”).

TB Time Access B Control Register2 R/W

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	-	TBSTAT
WR	TB Register							

SFR Address: 0xC9 **Default: 0b00000000**

TB access control functions are similar to TA control, except the ticket is for multiple uses with a time limit. Once access is granted, the access is open for 256 clock periods and then expires. The software can also read TB address to obtain the current TB status. The TB protected registers include two SFR registers, CKSEL (0x8F) and WKMASK (0x9F), and twelve XFR registers lodging FLSHCMD (0xA020), FLSHDAT (0xA021), FLSHADL (0xA023), FLSHADH (0xA022), ISPCLKF (0xA024), FLSHSPRT (0xA012), FLSHCPRT (0xA013). To modify registers with TB protection, the following procedure must be performed.

MOV TB, #0xAA

MOV TB, #0x55

This action creates a timed window of 256 SYSCLK periods to allow write access of these TB protected registers. If any above-mentioned sequences are repeated before the 128 cycles expires, a new 128 cycles is extended. The current 256 cycles can be terminated immediately by writing #0x00 to TB registers, such as

MOV TB, #0x00

It is recommended to terminate the TB access window once the user program finishes the modifications of TB protected registers.

Because TA and TB are critical reassurance of the reliable operation of the MCU that prevents accidental hazardous uncontrollable modifications of critical registers, the operation of these two registers should bear extreme cautions. It is strongly advised that these two registers should be turned on only when needed.Both registers use synchronous CPU clock, therefore it is imperative that any running tasks of TA and TB should be terminated before entering Idle mode or Stop mode. Both modes turn off the CPU clock and if TA and TB are enabled, they stay enabled until the CPU clock resumes thus may create vulnerabilities for critical registers.

Another reliability concern of embedded Flash MCU is that the important content on the Flash can be accidentally erased. This concern is addressed by the content protection in the Flash controller.

CLOCK CONTROL AND POWER MANAGEMENT MODES

This section describes the clock control and power saving modes of the CPU and its integrated peripherals. The settings are controlled by PCON (0x87) and PMR (0xC4) registers. The register description is defined as following.

PCON **R/W**

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	-	-
WR	-	-	-	-	-	SLEEP	STOP	IDLE

SFR Address: 0x87 **Default: 0b00000000**

SLEEP Sleep mode control bit. When this bit and the STOP bit are set to 1, the clock of the CPU and all peripherals is disabled and enters Sleep mode. The Sleep mode exits when non-clocked Interrupts or resets occur. Upon exiting Sleep mode, SLEEP bit and STOP bit in PCON is automatically cleared. In terms of power consumption, the following relationship applies: Idle mode > Stop mode > Sleep mode. Sleep mode is the same as Stop mode, except it also turns off the band gap and the regulator. It uses a very low power back-up regulator (< 5μA). When waking up from Sleep mode, it takes longer time (< 64 IOSC clock cycles, compared with Stop mode) because the regulator requires more time to stabilize.

STOP Stop mode control bit. The clock of the CPU and all peripherals is disabled and enters Stop mode if the SLEEP bit is in the reset state. The Stop mode can only be terminated by non-clocked Interrupts or resets. Upon exiting Stop mode, STOP bit in PCON is automatically cleared.

IDLE Idle mode control bit. If the IDLE bit is set, the system goes into Idle mode. In Idle mode, CPU clock becomes inactive and the CPU and its integrated peripherals such as WDT, T0/T1/T2, and UART0 are reset. But the clocks of external peripherals and CPU like PCA, ADC, LIN-capable16550-like UART2, SPI, T3, I2C slave and the others are still active. This allows the Interrupts generated by these peripherals and external Interrupts to wake the CPU. The exit mechanism of Idle mode is the same as Stop mode. IDLE bit is automatically cleared at the exit of the Idle mode.

PMR **R/W**

Bit	7	6	5	4	3	2	1	0
RD	CD1	CD0	SWB	-	-	-	-	-
WR	-	CD0	SWB	-	-	-	-	-

SFR Address: 0xC4 **Default: 0b010xxxxx**

CD1, CD0 Clock Divider Control bit. These two bits control the entry of PMM mode. When CD0=1, and CD1=0, full speed operation is in effect. When CD0=1, and CD1=1, the CPU enters PMM mode where CPU and its integrated peripherals operate at a clock rate divided by 257. Note that in PMM mode, all integrated peripherals such as UART0, LIN-capable 16550-like UART2, WDT, and T0/T1/T2 run at this reduced rate, thus may not function properly. All external peripherals to CPU still operate at full speed in PMM mode.

NOTE: CD1 is internally hardwired to 0. This implementation does not support PMM mode.

SWB Switch Back Control bit. Setting this bit allows the actions to occur in integrated peripherals to automatically switch back to normal operation mode.

CKSEL **System Clock Selection Register** **R/W** **TB Protected**

Bit	7	6	5	4	3	2	1	0
RD	IOSCDIV[3:0]				REGRDY[1:0]		-	
WR	IOSCDIV[3:0]				REGRDY[1:0]		-	

SFR Address: 0x8F **Default: 0b10011000**

IOSCDIV[3:0] IOSC Pre-Divider

IOSCDIV[3:0]	SYSCLK
0000	IOSC
0001	IOSC/2
0010	IOSC/4
0011	IOSC/6
0100	IOSC/8
0101	IOSC/10
0110	IOSC/12
0111	IOSC/14
1000	IOSC/15
1001	IOSC/16
1010	IOSC/32
1011	IOSC/64
1100	IOSC/128
1101	IOSC/256
1110	IOSC/512
1111	IOSC/1024

REGRDY[1:0] Wake up delay time for main regulator stable time from reset or from Sleep mode wakeup

REGRDY[1:0]	Delay time
00	64 IOSC cycle
01	128 IOSC cycle
10	256 IOSC cycle
11	512 IOSC cycle

WKMASK Wake-Up Mask Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	WEINT8	WEINT7	-	WEINT4	WEINT3	WEINT2	WEPINT1	WEPINT0
WR	WEINT8	WEINT7	-	WEINT4	WEINT3	WEINT2	WEPINT1	WEPINT0

SFR Address: 0x9F **Default: 0b11111111**

WEINT8 Set this bit to allow INT8 to trigger the wake up of CPU from Stop modes.
WEINT7 Set this bit to allow INT7 to trigger the wake up of CPU from Stop modes.
WEINT4 Set this bit to allow INT4 to trigger the wake up of CPU from Stop modes.
WEINT3 Set this bit to allow INT3 to trigger the wake up of CPU from Stop modes.
WEINT2 Set this bit to allow INT2 to trigger the wake up of CPU from Stop modes.
WEPINT1 Set this bit to allow INT1 to trigger the wake up of CPU from Stop modes.
WEPINT0 Set this bit to allow INT0 to trigger the wake up of CPU from Stop modes.

WKMASK register defines the wake up control of the Interrupt signals from the Stop mode. The wake-up is performed by these Interrupts and if enabled the internal oscillator is turned on and SYSCLK resumes. The Interrupt can be set as a level trigger or an edge trigger and the wake-up always runs in accordance with the edge. Please note the wake-up control is wired separately from the Interrupt logic, therefore, after waking up, the CPU does not necessarily enter the Interrupt service routine if the corresponding Interrupt is not enabled. In this case, the CPU continues onto the next instruction,which initiates the Stop mode. Extra attention should be exercised as designing the exit and re-entry of modes to ensure proper operation.

Please note that all clocks are stopped in Stop mode, therefore peripherals require clock such as I²C slave, UART2, ADC, LVD, and T3/T4 cannot perform wake-up function. Only external pins and peripherals that do not require a clock can be used for wake up purposes. Such peripherals are LIN WakeUp and Timer5 with SOSC

Idle Mode

Idle mode provides a further power saving than PMM mode by stopping the clock for CPU and its integrated peripherals while keeping the external peripherals at normal operating conditions.The external peripherals still function normally thus can generate Interrupts that wake up the CPU from Idle mode. The Idle mode is introduced by setting Idle bit to 1.

When the CPU is in Idle mode, no processing is possible. All integrated internal peripherals such as T0/T1/T2, LIN-capable 16550-like UART2 and I2C Master are inaccessible during idling. The Idle mode can be excited by hardware reset through RSTN pin (no such pin) or by external Interrupts as well as the Interrupts from external peripherals that are OR-ed with the external Interrupts. The triggering external Interrupts need be enabled properly. Upon exiting from Idle mode, the CPU resumes operation as the clock is being turned on. CPU immediately vectors to the Interrupt service routine of the corresponding Interrupt sources that wake up the CPU. When the Interrupt service routine completes, RETI returns to the program and immediately follows the one that invokes the Idle mode. Upon returning from Idle mode to Normal mode, IDLE bit in PCON is automatically cleared. As the purpose of the Idle mode is to save power, the use of IOSC clock is strongly recommended in place of SYSCLK before entering Idle mode since it consumes significantly less power than the crystal oscillator or other clock sources.

Stop Mode

Stop mode provides the lowest power consumption by stopping clocks to all components in the system. Stop mode is entered by setting STOP=1. To achieve minimum power consumption, before entering Stop mode, it is essential to turn off all peripherals and the current operating clock oscillator. It is also important that the software switches to the IOSC clock and disables all other clock generator before entering Stop mode. This is critical to ensure a smooth transition when resuming its normal operations. Upon entering Stop mode, the system uses the last edge of IOSC clock to shut down the IOSC clock generator. The minimum power consumption state is achieved through this mechanism.

Hardware reset Interrupts generated via external pins (INT0 and INT1) or INT2 to INT8 brings the system out of Stop mode. Since all clocks are inactive, none of the peripherals like UART, Timers, I2C master and slave, ADC, or LVD contribute to the exit of Stop mode. Peripherals like Analog comparator and RTC Interrupt, however, can be used to trigger the exit of Stop mode as they are implemented asynchronously or their own clock sources.

The triggering Interrupt source must be enabled and its Wake-up bit is set in the WKMASK register. External pins require LOW level triggers; however the INT flags of on-chip external peripherals require HIGH level triggers. The IOSC circuit is activated by triggering event and the CPU is woken up at the first IOSC clock edge. Please note that the IOSC is activated as soon as Stop mode exits. As CPU resumes the normal operation using the IOSC clock when an Interrupt presents, the CPU immediately vectors to the Interrupting service routine of the corresponding Interrupt source. When the Interrupt service routine completes, RETI returns to the program immediately to execute the instruction that invokes the Stop mode. The STOP bit in PCON is automatically cleared by hardware reset during the waking up.

Please note the wake-up control WKMASK register and Interrupt enable registers IE and EXIE which are specifically responsible for the wake-up and Interrupt. Extra attention should be taken while programming for coherent application design. In Stop mode, clocks of CPU and peripherals are disabled (except RTC). Therefore only external pins and peripherals such as analog comparator and RTC that do not require clock can be used to initiate the wake-up process. Peripherals such as UART, Timers, I²C master and slave, ADC, or LVD cannot generate wake-up Interrupt in this mode.

Sleep Mode

In Stop mode, the main regulator providing 1.8V (VDDD) to internal logic, memory and flash circuits are still active. The regulator and its internal Bandgap reference circuits consumes approximately about 200uA. Sleep mode is used to further reduce the standby power through turning off the regulator and reference circuits. The logic behavior of Sleep mode is the same as Stop mode and is entered by setting both STOP and SLEEP bits to 1 in PCON register. In Sleep mode, a very low-power back-up regulator is used to provide supply voltage to the internal logic, memory and flash circuits. The back-up regulator consumes about 10uA to 20uA, and can supply up to 1mA of load. The output voltage of the back-up regulator is lower than the main regulator, and typically is around 1.45V.

The exit of Sleep mode Is the same as exit of Stop mode by wake-up events, and exits directly back to normal operation and the main regulator is turned on. Note the enabling time of the main regulator is about 10usec, therefore, after wake-up from Sleep mode, the software should be kept at NOP for at least 20usec before resuming. It is also recommended that if Sleep mode is used, the decoupling capacitor on VDDD should contains at least 10uF if external decoupling capacitor is used. In IS32LT3183A, 1.8V is generated internally without external capacitor pin.

Clock Control

The clock selection is defined by CKSEL register (0x8F). An IOSC is a critical component in MCU although not integrated in the CPU core. It is enabled except in Stop/Sleep mode. An IOSC also handles critical timing conformance for flash programming and the default manufactured calibrated IOSC is set at 16MHz.

WATCHDOG TIMER

The Watchdog Timer is a 30-bit timer that can be used by a system supervisor or as an event timer. The Watchdog timer can be used to generate an Interrupt or to issue a system reset depending on the control settings. This section describes the register related to the operation of Watchdog Timer and its functions. The following diagram shows the structure of the Watchdog Timer. Note WDT shares the same clock with the CPU, thus WDT is disabled in Idle mode or Stop mode however it runs at a reduced rate in PMM mode.

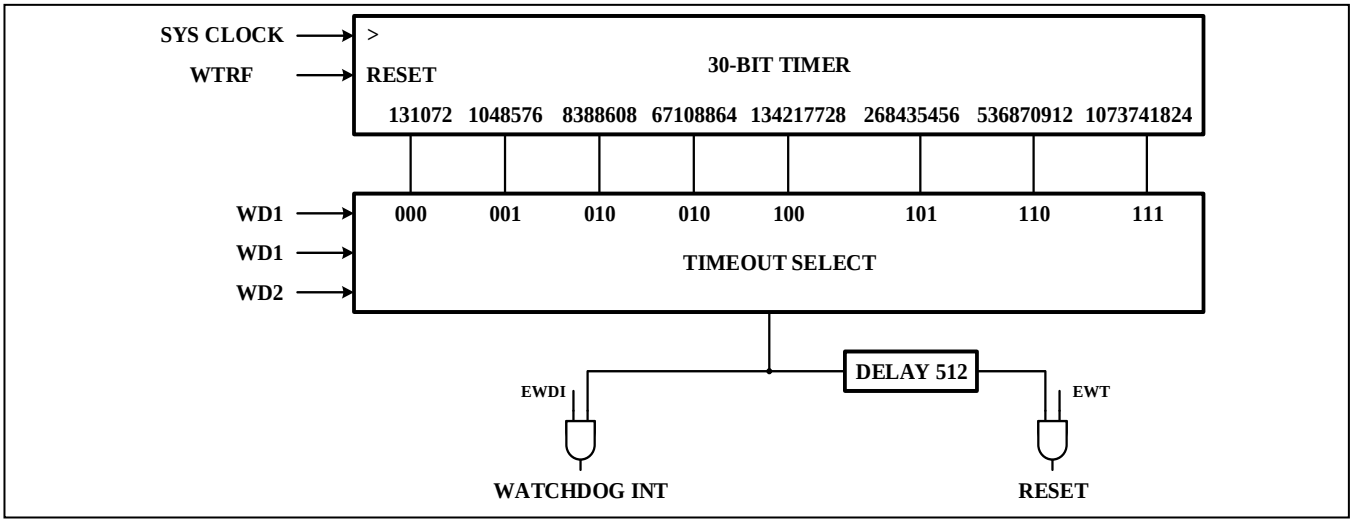


Figure 4 Watchdog Timer Block Diagram

WDCON WDT Interrupt Flag Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	WDIF	WTRF	EWT	-
WR	-	-	-	-	WDIF	WTRF	EWT	RWT

SFR Address: 0x8D **Default: 0b00000000**

WDIF WDT Interrupt Flag bit. This bit is set when the session expires regardless of a WDT Interrupt is enabled or not.

WTRF WDT Reset Flag bit. WDRF is cleared by hardware reset including RSTN, POR etc. WTRF is set to 1 after a WDT reset occurs. It can be cleared by software. WTRF can be used by software to determine if a WDT reset has occurred.

EWT Watchdog Timer Reset Enable bit. Set this bit to enable the watchdog reset function. The default WDT reset is enabled and WDT timeout is set to maximum.

RWT Reset the Watchdog timer. Writing 1 to RWT resets the WDT timer. RWT bit is not a register and does not hold any value. The clearing action of Watchdog timer is protected by TA access. In another word, to clear Watchdog timer, TA must be unlocked then and then followed by writing RWT bit to 1. If TA is still locked, the program can write 1 into RWT bit, but it does not reset the Watchdog timer.

Note the WDT Interrupt enable control is located in EXIE (0xE8) EWDI bit. It must be cleared by software

CKCON Clock Control and WDT R/W

Bit	7	6	5	4	3	2	1	0
RD	WD1	WD0	T2CKDCTL	T1CKDCTL	T0CKDCTL	WD2	-	-
WR	WD1	WD0	T2CKDCTL	T1CKDCTL	T0CKDCTL	WD2	-	-

SFR Address: 0x8E **Default: 0b11000111**

T2CKDCTL Timer 2 Clock Source Division Factor Control Flag. Setting this bit to 1 sets the Timer 2 division factor to 4, the Timer 2 clock frequency equals CPU clock frequency divided by 4. Setting this bit to 0 (the default power on value) sets the Timer 2 division factor to 12, the Timer 2 clock frequency equals CPU clock frequency divided by 12.

T1CKDCTL Timer 1 Clock Source Division Factor Control Flag. Setting this bit to 1 sets the Timer 1 division factor to 4, the Timer 1 clock frequency equals CPU clock frequency divided by 4. Setting this bit to 0 (the default power on value) sets the Timer 1 division factor to 12, the Timer 1 clock frequency equals CPU clock frequency divided by 12.

T0CKDCTL Timer 0 Clock Source Division Factor Control Flag. Setting this bit to 1 sets the Timer 0 division factor to 4, the Timer 0 clock frequency equals CPU clock frequency divided by 4. Setting this bit to 0 (the default power on value) sets the Timer 0 division factor equals 12, the Timer 0 clock frequency equals CPU clock frequency divided by 12.

WD[2:0] This register controls the time out value of WDT as the following table. The time out value is shown as follows and the default is set to maximum:

WD2	WD1	WD0	Time Out Value
0	0	0	131072
0	0	1	1048576
0	1	0	8388608
0	1	1	67108864
1	0	0	134217728
1	0	1	268435456
1	1	0	536870912
1	1	1	1073741824

SYSTEM TIMERS – T0 AND T1

The CPU contains three 16-bit timers/counters, Timer 0, Timer 1 and Timer 2. In timer mode, Timer 0, Timer 1 registers are incremented every 12 SYSCLK period when the appropriate timer is enabled. In the timer mode, Timer 2 registers are incremented every 12 or 2 SYSCLK period (depending on the operating mode). In the counter mode, the timer registers are incremented every falling edge on their corresponding inputs: T0, T1, and T2. These inputs are read every SYSCLK period.

Timer 0 and Timer 1 are fully compatible with the standard 8051. Timer 0 and 1 are controlled by TCON (0x88) and TMOD (0x89) registers while each timer consists of two 8-bit registers TH0 (0x8C), TL0 (0x8A), TH1 (0x8D), TL1 (0x8B).

TCON Timer 0 and 1 Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
WR	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

SFR Address: 0x88 **Default: 0b00000000**

TF1 Timer 1 Overflow Interrupt Flag bit. TF1 is cleared by hardware when entering ISR.

TR1 Timer 1 Run Control bit. Set to enable Timer 1, and clear to disable Timer 1.

TF0 Timer 0 Overflow Interrupt Flag bit. TF0 is cleared by hardware when entering ISR.

TR0 Timer 0 Run Control bit. Set to enable Timer 0, and clear to disable Timer 0.

IE1, IT1, IE0, IT0 These bits are related to configurations of expanded Interrupt INT1 and INT0. These are described in the Interrupt System section.

TMOD **Timer 0 and 1 Mode Control Register** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	GATE1	CT1	T1M1	T1M0	GATE0	CT0	T0M1	T0M0
WR	GATE1	CT1	T1M1	T1M0	GATE0	CT0	T0M1	T0M0

SFR Address: 0x89 **Default: 0b00000000**

GATE1 Timer 1 Gate Control bit. Set to enable external T1 to function as gating control of the counter.

CT1 Counter or Timer Mode Select bit. Set CT1 to access external T1 as the clock source. Clear CT1 to use internal clock.

T1M1 Timer 1 Mode Select bit.

T1M0 Timer 1 Mode Select bit.

GATE0 Timer 0 Gate Control bit. Set to enable external T0 to function as gating control of the counter.

CT0 Counter or Timer Mode Select bit. Set CT0 to use external T0 as the clock source. Clear CT0 to use internal clock.

T0M1 Timer 0 Mode Select bit.

T0M0 Timer 0 Mode Select bit.

TxM1	TxM0	Mode	Mode Descriptions
0	0	0	TL serves as a 5-bit pre-scaler and TH functions as an 8-bit counter/timer. They form a 13-bit operation.
0	1	1	TH and TL are cascaded to form a 16-bit counter/timer.
1	0	2	TL functions as an 8-bit counter/timer and auto-reloads from TH.
1	1	3	TL functions as an 8-bit counter/timer. TH functions as an 8-bit timer which is controlled by GATE1. Only Timer 0 can be configured in Mode 3. When this happens, Timer 1 can only be used where its Interrupt is not required.

Mode 0

In this mode, TL serves as a 5-bit pre-scaler and TH functions as an 8-bit counter/timer, together working as a 13-bit counter/timer. The Mode 0 operation is shown in the following diagram.

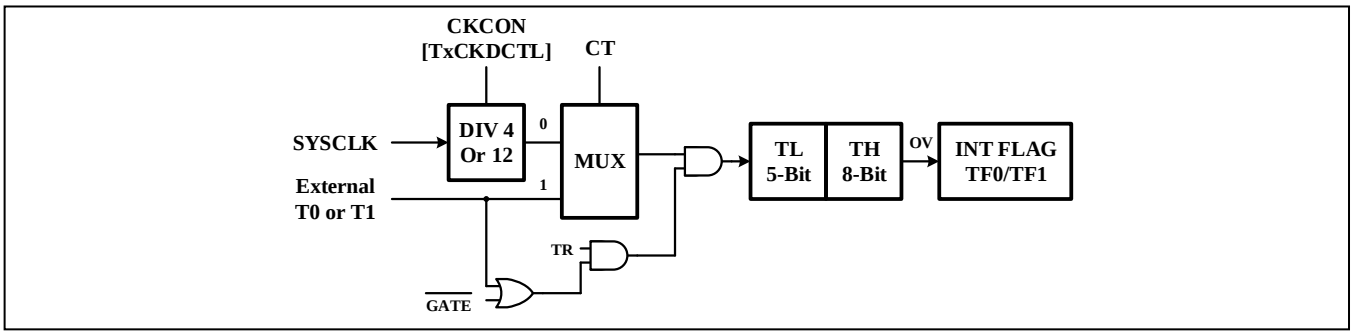


Figure 5 Timer 0 and 1 Mode 0 Block Diagram

Mode 1

Mode 1 operates the same way Mode 0 does, except TL is configured as 8-bit and thus forming a 16-bit counter/timer. This is shown as the following diagram.

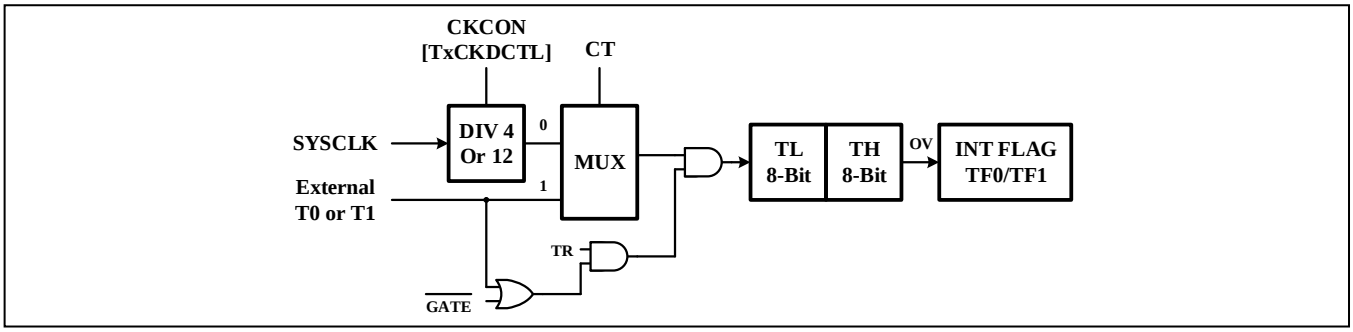


Figure 6 Timer 0 and 1 Mode 1 Block Diagram

Mode 2

Mode 2 configures the timer as an 8-bit re-loadable counter. The counter is TL while TH stores the reload data. The reload occurs when TL overflows. The operation is shown in the following diagram:

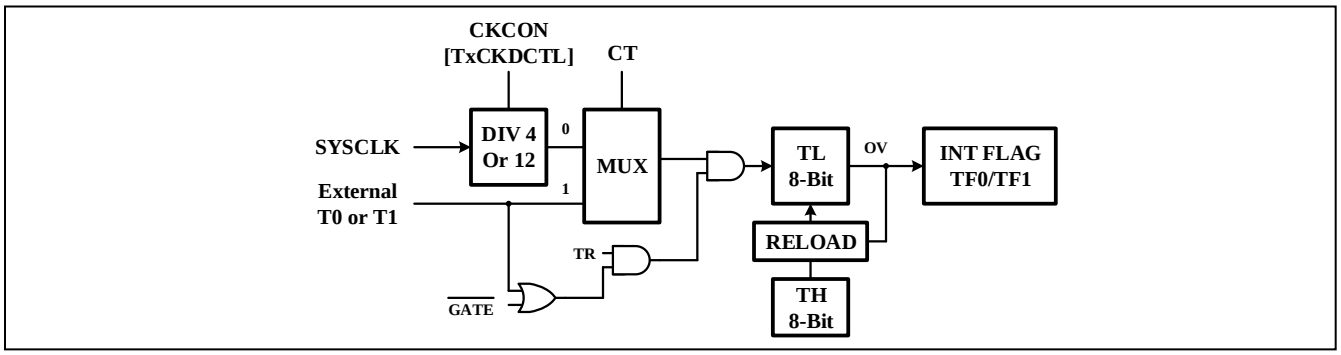


Figure 7 Timer 0 and 1 Mode 2 Block Diagram

Mode 3

Mode 3 is a special mode for Timer 0 only. In this mode, Timer 0 is configured as two separate 8-bit counters. TL0 uses control and Interrupt flags of Timer 0 whereas TH0 uses control and Interrupt flag of Timer 1. Since Timer 1's control and flag are occupied, Timer 2 can only be used for counting purposes such as Baud rate generating while Timer 0 is in Mode 3. The operation flow of Mode 3 is shown in the following diagram.

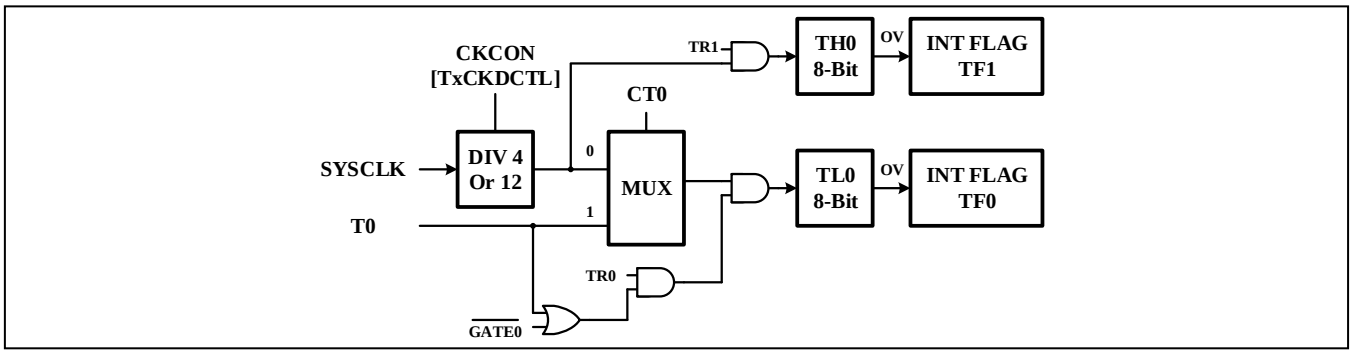


Figure 8 Timer 0 and 1 Mode 3 Block Diagram

SYSTEM TIMER – T2

Timer 2 can be used as the re-loadable counter.

T2CON Timer 2 Control and Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	TF2	-	-	-	-	TR2	CT2	-
WR	TF2	-	-	-	-	TR2	CT2	-

SFR Address: 0xC8 **Default: 0b00000000**

TF2	Timer 2 Interrupt Flag bit. TF2 must be cleared by software.
TR2	Start/Stop Timer 2 Control bit 1: Enable Timer 2 and Auto-reload counter 0: Disable Timer 2 counter
CT2	Timer 2 Timer/Counter Mode Select bit This bit must set 0

The block diagram of the Timer 2 operating in Auto-reload Counter mode is shown in the following diagram:

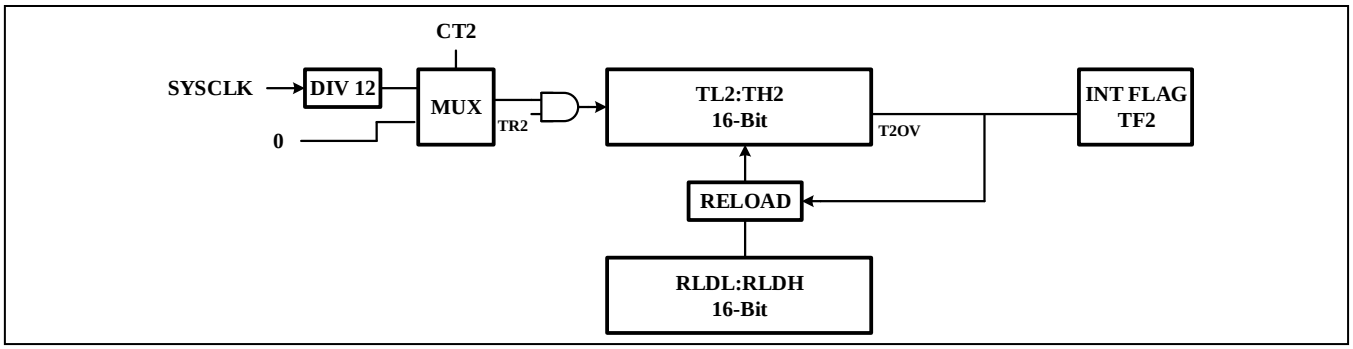


Figure 9 Timer 2 Block Diagram

SYSTEM TIMER – T3 AND T4

Both Timer 3 and Timer 4 are simple 16-Bit reload timers or free-run counters and are clocked by the system clock. The block diagram is shown as below.

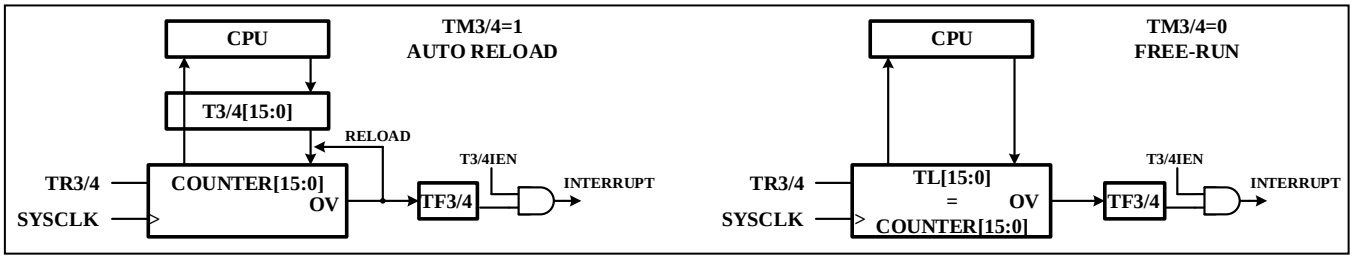


Figure 10 Timer 3 And 4 Block Diagram

T34CON Timer 3 and Timer 4 Control and Status Register R/W

Bit	7	6	5	4	3	2	1	0
RD	TF4	TM4	TR4	T4IEN	TF3	TM3	TR3	T3IEN
WR	TF4	TM4	TR4	T4IEN	TF3	TM3	TR3	T3IEN

SFR Address: 0xCF **Default: 0b00000000**

TF4	Timer 4 Overflow Interrupt Flag bit. TF4 is set by hardware when overflow condition occurs. TF4 must be cleared by software.
TM4	Timer 4 Mode Control bit. TM4 = 1 set timer 4 as auto reload, and TM4=0 set timer 4 as free-run.
TR4	Timer 4 Run Control bit. Set to enable Timer 4, and clear to stop Timer 4.
T4IEN	Timer 4 Interrupt Enable bit. T4IEN=0 disable the Timer 4 overflow Interrupt T4IEN=1 enable the Timer 4 overflow Interrupt
TF3	Timer 3 Overflow Interrupt Flag bit. TF3 is set by hardware when overflow condition occurs. TF3 must be cleared by software.
TM3	Timer 3 Mode Control bit. TM3 = 1 set timer 3 as auto reload, and TM3=0 set timer 3 as free-run.
TR3	Timer 3 Run Control bit. Set to enable Timer 3, and clear to stop Timer 3.

T3IEN Timer 3 Interrupt Enable bit.
T3IEN=0 disable the Timer 3 overflow Interrupt
T3IEN=1 enable the Timer 3 overflow Interrupt

TL3 Timer 3 Low Byte Register R/W

Bit	7	6	5	4	3	2	1	0
RD	T3[7:0]							
WR	T3[7:0]							

SFR Address: 0xAE **Default: 0b00000000**

TH3 Timer 3 High Byte Register R/W

Bit	7	6	5	4	3	2	1	0
RD	T3[15:8]							
WR	T3[15:8]							

SFR Address: 0xAF **Default: 0b00000000**

TL4 Timer 4 Low Byte Register R/W

Bit	7	6	5	4	3	2	1	0
RD	T4[7:0]							
WR	T4[7:0]							

SFR Address: 0xAC **Default: 0b00000000**

TH4 Timer 4 High Byte Register R/W

Bit	7	6	5	4	3	2	1	0
RD	T4[15:8]							
WR	T4[15:8]							

SFR Address: 0xAD **Default: 0b00000000**

T3[15:0] and T4[15:0] function differently when been read or written. When written in auto-reload mode, its reload value register is written, and in free-run mode, the counter value is written immediately. When been read, the return value is always the present counter value. There is no snapshot buffer in the read operation, so software should always read the high byte then the low byte.

SYSTEM TIMER – T5

T5 is a 24-Bit simple timer. It can select four different clock sources and can be used for extended Sleep mode wake up. The clock sources include IOSC, and SOSC. T5 can be configured either as free-run mode or auto-reload mode. Timer 5 does not depend on the SYSCLK, therefore it continues to count under STOP or Sleep mode if the clock source is present. The following diagram shows the block diagram of Timer 5.

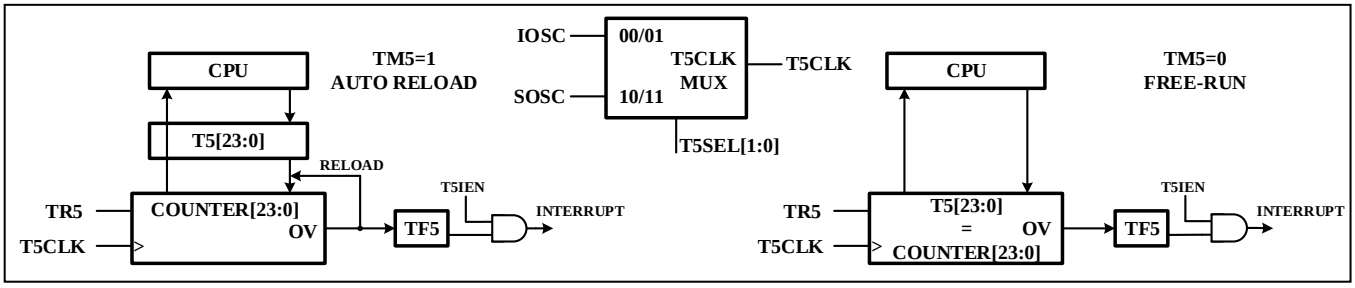


Figure 11 Timer 5 Block Diagram

T5CON Timer 5 Control and Status Register R/W

Bit	7	6	5	4	3	2	1	0
RD	TF5	T5SEL[1]	T5SEL[0]	TM5	TR5	-	-	T5IEN
WR	TF5	T5SEL[1]	T5SEL[0]	TM5	TR5	-	-	T5IEN

SFR Address: 0xA003 **Default: 0b00000000**

TF5 Timer 5 Overflow Interrupt Flag bit.
TF5 is set by hardware when overflow condition occurs. TF5 must be cleared by software.

T5SEL[1:0] Timer 5 Clock Selection bits.
T5SEL[1:0] = 00, IOSC
T5SEL[1:0] = 01, IOSC
T5SEL[1:0] = 10, SOSC
T5SEL[1:0] = 11, SOSC

TM5 Timer 5 Mode Control bit. TM5=1 set timer 5 as auto reload, and TM5=0 set timer 5 as free-run.

TR5 Timer 5 Run Control bit. Set to enable Timer 5, and clear to stop Timer 5.

T5IEN Timer 5 Interrupt Enable bit.
T5IEN=0 disable the Timer 5 overflow Interrupt
T5IEN=1 enable the Timer 5 overflow Interrupt

TL5 Timer5 Low Byte Register R/W

Bit	7	6	5	4	3	2	1	0
RD	T5[7:0]							
WR	T5[7:0]							

SFR Address: 0xA004 **Default: 0b00000000**

TH5 Timer5 Medium Byte Register R/W

	7	6	5	4	3	2	1	0
RD	T5[15:8]							
WR	T5[15:8]							

SFR Address: 0xA005 **Default: 0b00000000**

TT5 Timer5 High Byte Register R/W

Bit	7	6	5	4	3	2	1	0
RD	T5[23:16]							
WR	T5[23:16]							

SFR Address: 0xA006 **Default: 0b00000000**

T5[23:0] functions differently when been read or written. When written in auto-reload mode, its reload value register is written, and in free-run mode, the counter value is written immediately. When been read, the return value is always the present counter value. There is no snapshot buffer in the read operation, so software should always read the high byte then the low byte.

Multiplication and Division Unit (MDU)

MDU provides acceleration on unsigned integer operations of 16-bit multiplications, 32-bit division, and shifting and normalizing operations. The following table shows the execution characteristics of these operations. The MDU does not contain the operation completion status flag. Therefore the most efficient utilization of MDU uses NOP delay for the required clock time of the MDU operation types. The number of the clock cycles required for each operation is shown in the following table and it is counted from the last write of the writing sequence.

Operations	Result	Reminder	Number of Clock Cycle
32-bit division by 16-bit	32-bit	16-bit	17
16-bit division by 16-bit	16-bit	16-bit	9
16-bit multiplication by 16-bit	32-bit	-	10
32-bit normalization	-	-	3 – 20
32-bit shift left/right	-	-	3 – 18

The MDU is accessed through MD0 to MD5 that contains the operands and the results, and the operation is controlled by ARCON register.

ARCON MDU Control R/W

Bit	7	6	5	4	3	2	1	0
RD	MDEF	MDOV	SLR	SC4	SC3	SC2	SC1	SC0
WR	MDEF	MDOV	SLR	SC4	SC3	SC2	SC1	SC0

SFR Address: 0xFF **Default: 0b00000000**

MDEF MDU Error Flag bit. Set by hardware to indicate MDx being written before the previous operation completes. MDEF is automatically cleared after reading ARCON.

MDOV MDU Overflow Flag bit. MDOV is set by hardware if dividend is zero or the result of multiplication is greater than 0x0000FFFFh

SLR Shift Direction Control bit. SLR = 1 indicates a shift to the right and SLR =0 indicates a shift to the left.

SC[4:0] Shift Count Control and Result bit. If SC[4:0] is written with 00000, the normalization operation performed by MDU. When the normalization is completed, SC[4:0] contains the number of shift performed in the normalization. If SC[4:0] is written with a non-zero value, then the shift operation is performed by MDU with the number of shift specified by SC[4:0] value.

MD0 MDU Data Register 0 R/W

Bit	7	6	5	4	3	2	1	0
RD	MD0[7:0]							
WR	MD0[7:0]							

SFR Address: 0xF9 **Default: 0b00000000**

MD1 MDU Data Register 1 R/W

Bit	7	6	5	4	3	2	1	0
RD	MD1[7:0]							
WR	MD1[7:0]							

SFR Address: 0xFA **Default: 0b00000000**

MD2 MDU Data Register 2 R/W

Bit	7	6	5	4	3	2	1	0
RD	MD2[7:0]							
WR	MD2[7:0]							

SFR Address: 0xFB **Default: 0b00000000**

MD3 MDU Data Register 3 R/W

Bit	7	6	5	4	3	2	1	0
RD	MD3[7:0]							
WR	MD3[7:0]							

SFR Address: 0xFC **Default: 0b00000000**

MD4 MDU Data Register 4 R/W

Bit	7	6	5	4	3	2	1	0
RD	MD4[7:0]							
WR	MD4[7:0]							

SFR Address: 0xFD **Default: 0b00000000**

MD5 MDU Data Register 5 R/W

Bit	7	6	5	4	3	2	1	0
RD	MD5[7:0]							
WR	MD5[7:0]							

SFR Address: 0xFE **Default: 0b00000000**

MDU operation consists of three phases.

Loading MD0 to MD5 data registers in an appropriate order depending on the operation.

Execution of the operations.

Reading result from MD0 to MD5 registers.

The following list shows the MDU read and write sequences. Each operation has its unique writing sequence and reading sequence of MD0 to MD5 registers therefore a precise access sequence is required.

Division – 32-bit divide by 16-bit or 16-bit divide by 16-bit

Follow the following write-sequence. The first write of MD0 resets the MDU and initiates the MDU error flag mechanism. The last write incites calculation of MDU.

Write MD0 with Dividend LSB byte

Write MD1 with Dividend LSB+1 byte

Write MD2 with Dividend LSB+2 byte (ignore this step for 16-bit divide by 16-bit)

Write MD3 with Dividend MSB byte (ignore this step for 16-bit divide by 16-bit)

Write MD4 with Divisor LSB byte

Write MD5 with Divisor MSB byte

Then follow the following read-sequence. The last read prompts MDU for the next operations.

Read MD0 with Quotient LSB byte

Read MD1 with Quotient LSB+1 byte

Read MD2 with Quotient LSB+2 byte (ignore this step for 16-bit divide by 16-bit)

Read MD3 with Quotient MSB byte (ignore this step for 16-bit divide by 16-bit)

Read MD4 with Remainder LSB byte

Read MD5 with Remainder MSB byte

Read ARCON to determine error or overflow condition

Please note if the sequence is violated, the calculation may be Interrupted and result in errors.

Multiplication – 16-bit multiply by 16-bit

Follow the following write sequence.

Write MD0 with Multiplicand LSB byte

Write MD4 with Multiplier LSB byte

Write MD1 with Multiplicand MSB byte

Write MD5 with Multiplier MSB byte

Then follow the following read sequence.

Read MD0 with Product LSB byte

Read MD1 with Product LSB+1 byte

Read MD2 with Product LSB+2 byte

Read MD3 with Product MSB byte

Read ARCON to determine error or overflow condition

Normalization – 32-bit

Normalization is obtained with integer variables stored in MD0 to MD3. After normalization, all leading zeroes are removed by shift left operations. To start the normalization operation, SC[4:0] in ARCON is first written with 00000. After completion of the normalization, SC[4:0] is updated with the number of leading zeroes and the normalized result is restored on MD0 to MD3. The number of the shift of the normalization can be used as exponents.The following write sequence should be followed. The last write to ARCON initiates the normalization operations by MDU.

Write MD0 with Operand LSB byte

Write MD1 with Operand LSB+1 byte

Write MD2 with Operand LSB+2 byte

Write MD3 with Operand MSB byte

Write ARCON with SC[4:0] = 00000

Then follow the following read sequence.

Read MD0 with Result LSB byte

Read MD1 with Result LSB+1 byte

Read MD2 with Result LSB+2 byte

Read MD3 with Result MSB byte

Read SC[4:0] from ARCON for normalization count or error flag

Shift – 32-bit

Shift is done with integer variables stored in MD0 to MD3. To start the shift operation, SC[4:0] in ARCON is first written with shift count and SLR with shift direction. After completion of the Shift, the result is stored back to MD0 to MD3.The following write sequence should be followed. The last write to ARCON initiates the normalization operations by MDU.

Write MD0 with Operand LSB byte

Write MD1 with Operand LSB+1 byte

Write MD2 with Operand LSB+2 byte

Write MD3 with Operand MSB byte

Write ARCON with SC[4:0] = Shift count and SLR with shift direction

Then follow the following read sequence.

Read MD0 with Result LSB byte

Read MD1 with Result LSB+1 byte

Read MD2 with Result LSB+2 byte

Read MD3 with Result MSB byte

Read ARCON's for error flag

MDU Flag

The error flag (MDEF) of MDU indicates improperly performed operations. The error mechanism starts at the first MD0 write and finishes with the last read of MD result register. MDEF is set if current operation is Interrupted or restarted by improper write of MD register before the operation completes. MDEF is cleared if the operations and proper write/read sequences successfully complete.The overflow flag (MDOV) of MDU indicates an error of operations.

MDOV is set if

The divisor is zero

Multiplication overflows

Normalization operation is performed on already normalized variables ((Check if MD3 register bit 7 =1)

I2C MASTER

The I²C master controller provides the interface to I²C slave devices. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master configurations. The master uses SCL and SDA pins. The controller contains a built-in 8-bit timer to allow various I²C bus speed. The maximum I²C bus speed is limited to 1MHz.

I2CMTP I²C Master Time Period R/W

Bit	7	6	5	4	3	2	1	0
RD	I2CMTP[7:0]							
WR	I2CMTP[7:0]							

SFR Address: 0xF7 **Default: 0b00000000**

This register set the period time of I²C bus clock – SCL. The SCL period time is set according to

SCL_PERIOD = 8 * (1 + I2CMTP[7:0]) * (1/SYSCLK)

The maximum I²C bus speed is limited to 1MHz, So the I2CMTP[7:0] minimum setting is 1.

I2CMSA I²C Master Slave Address R/W

Bit	7	6	5	4	3	2	1	0
RD	SA[6:0]							RS
WR	SA[6:0]							RS

SFR Address: 0xF4 **Default: 0b00000000**

SA[6:0] Slave Address. SA[6:0] defines the slave address the I²C master uses to communicate.

RS Receive/Send Bit. RS determines if the following operation is to RECEIVE (RS=1) or SEND (RS=0).

I2CMBUF I²C Master Data Buffer Register R/W

Bit	7	6	5	4	3	2	1	0
RD	RD[7:0]							
WR	TD[7:0]							

SFR Address: 0xF6 **Default: 0b00000000**

I2CMBUF functions as a transmit-data register when written and as a receive-data register when read. When written, TD is sent to the bus by the next SEND or BURST SEND operations. TD[7] is sent first. When read, RD contains the 8-bit data received from the bus upon the last RECEIVE or BURST RECEIVE operation.

I2CMCR **I²C Master Control and Status Register** **R/W**

Bit	7	6	5	4	3	2	1	0
RD	-	BUSBUSY	I2CIDLE	ARBLOST	DATANACK	ADDRNACK	ERROR	BUSY
WR	CLEAR	INFILEN	-	-	ACK	STOP	START	RUN

SFR Address: 0xF5 **Default: 0b00000000**

The I2CMCR register is used for setting control when it is written, and as a status signal when read.

BUSBUSY This bit indicates that the external I²C bus is busy and access to the bus is not possible. This bit is set/reset by START and STOP conditions.

I2CIDLE This bit indicates that I²C master is in the Idle mode.

ARBLOST This bit is automatically set when the last operation I²C master controller loses the bus arbitration.

DATANACK This bit is automatically set when the last transmitted data is not acknowledged.

ADDRNACK This bit is automatically set when the last operation slave address transmitted is not acknowledged.

ERROR This bit indicates that an error occurs in the last operation. The errors include slave address was not acknowledged, or transmitted data is not acknowledged, or the master controller loses arbitration.

BUSY This bit indicates that I²C master is receiving or transmitting data, and other status bits are not valid.

CLEAR Reset I2C Master State Machine

Set CLEAR=1 will reset the state machine. CLEAR is self-cleared when reset is completed.

INFILEN Input Noise Filter Enable. When IFILEN is set, pulses shorter than 50n sec on inputs of SDA and SCL are filtered out.

START, STOP, RUN and RS, ACK bits are used to drive I²C Master to initiate and terminate a transaction. The start bit generates START, or REPEAT START protocol. The STOP bit determines if the cycle stops at the end of the data cycle or continues to a burst. To generate a single read cycle, the designated address is written in SA, RS is set to 1, ACK=0, STOP=1, START=1, RUN=1 are set in I2CMCR to perform the operation and then STOP. When the operation is completed (or aborted due to errors), I²C master generates an Interrupt. The ACK bit must be set to 1. This causes the controller to send an ACK automatically after each byte transaction. The ACK bit must be reset when set to 0 when the master operates in receive mode and not to receive further data from the slave devices.

The following table lists the permitted control bits combinations in master Idle mode.

RS	ACK	STOP	START	RUN	OPERATIONS
0	-	0	1	1	START condition followed by SEND. Master remains in TRANSMITTER mode
0	-	1	1	1	START condition followed by SEND and STOP
1	0	0	1	1	START condition followed by RECEIVE operation with negative ACK. Master remains in RECEIVER mode
1	0	1	1	1	START condition followed by RECEIVE and STOP
1	1	0	1	1	START condition followed by RECEIVE. Master remains in RECEIVER mode
1	1	1	1	1	Illegal command

The following table lists the permitted control bits combinations in master TRANSMITTER mode.

RS	ACK	STOP	START	RUN	OPERATIONS
-	-	0	0	1	SEND operation. Master remains in TRANSMITTER mode
-	-	1	0	0	STOP condition
-	-	1	0	1	SEND followed by STOP condition
0	-	0	1	1	REPEAT START condition followed by SEND. Master remains in TRANSMITTER mode
1	-	1	1	1	REPEAT START condition followed by SEND and STOP condition
1	0	0	1	1	REPEAT START condition followed by RECEIVE operation with negative ACK. Master remains in TRANSMITTER mode
1	0	1	1	1	REPEAT START condition followed by SEND and STOP condition.
1	1	0	1	1	REPEAT START condition followed by RECEIVE. Master remains in RECEIVER mode.
1	1	1	1	1	Illegal command

The following table lists the permitted control bits combinations in master RECEIVER mode.

RS	ACK	STOP	START	RUN	OPERATIONS
-	0	0	0	1	RECEIVE operation with negative ACK. Master remains in RECEIVE mode
-	-	1	0	0	STOP condition
-	0	1	0	1	RECEIVE followed by STOP condition
-	1	0	0	1	RECEIVE operation. Master remains in RECEIVER mode
-	1	1	0	1	Illegal command
1	0	0	1	1	REPEAT START condition followed by RECEIVE operation with negative ACK. Master remains in RECEIVER mode
1	0	1	1	1	REPEAT START condition followed by RECEIVE and STOP conditions
1	0	1	1	1	REPEAT START condition followed by RECEIVE. Master remains in RECEIVER mode
0	-	0	1	1	REPEAT START condition followed by SEND. Master remains in TRANSMITTER mode.
0	-	1	1	1	REPEAT START condition followed by SEND and STOP conditions.

All other control-bit combinations not included in three tables above are NOP. In Master RECEIVER mode, STOP should be generated only after data negative ACK executed by Master or address negative ACK executed by slave. Negative ACK means SDA is pulled low when the acknowledge clock pulse is generated.

I2CMTO I²C Time Out Control Register R/W

Bit	7	6	5	4	3	2	1	0
RD	I2CMTOF	I2CMTO[6:0]						
WR	I2CMTOEN	I2CMTO[6:0]						

SFR Address: 0xC3 **Default: 0b00000000**

I2CMTOEN I2CM Time Out Enable

I2CMTOF I2CM Time Out Flag
This bit is set when a time out occurs. It is cleared when I2CM CLEAR command is issued.

I2CMTO[6:0] I2CM Time Out Setting
The TO time is set to 8*(I2CMTO[6:0]+1)* SCL_PERIOD. When time out occurs an I2CM Interrupt will be generated.

FLASH CONTROLLER

The flash controller connects the CPU to the on-chip embedded FLASH memory. The FLASH memory functions as the program storage as well as non-volatile data storage. The program access of the FLASH does not require any special attention. When the FLASH is used as data storage, the software sends commands to the FLASH controller through the XFR registers. And when the FLASH controller processes these commands, CPU is held idle until the command is completed. The embedded Flash memory contains two blocks – Main Memory and Information Block (IFB). The Main Memory is 32KB with uniform 512 Byte page (sector) size. The Information Block is 128 Byte and sits in a separate sector and is accessed through separate command.

The commands performed by a Flash Controller are defined in FLSHCMD registers. The defined operations allow the user program to use on-chip flash as a program memory and a non-volatile data memory in In-System-Programming as well as In-Application-Programming. The manufacturer provides a default ISP boot program located on the top 4KB of the flash.

The access of flash through Flash Controller is limited to protect critical contents not be altered accidentally. IFB can only be programmed once, not erased. Boot code area (0xB000 – 0xBFFF) cannot be erased of modified. The remaining 28KB of flash is partitioned into eight areas for separate protections defined by FLSHPRT register. Erase or modifications through Flash Controller commands of a protected area will results fail result status.

The whole embedded Flash can be accessed through WRITER Mode. A special 8-byte code security key is located at 0x6FF8 – 0x6FFF. A matched key must be supplied through WRITER mode to allow full access. Otherwise in locked state, only mass erase can be performed.

FLSHCMD Flash Controller Command Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	WRVFY	BUSY	FAIL	CMD4	CMD3	CMD2	CMD1	CMD0
WR	CYC[2:0]			CMD4	CMD3	CMD2	CMD1	CMD0

SFR Address: 0xA020 **Default: 0b10000000**

WRVFY Byte Write Result Verify. At the end of a write cycle, hardware reads back the data and compares it with which should be written to the flash. If there is a mismatch, this bit represents 0. It is reset to 1 by hardware when another ISP command is executed.

BUSY Flash command is in processing. This bit indicates that Flash Controller is executing the Flash Read, Write, or Sector Erase and other commands are not valid.

FAIL Command Execution Result. It is set if the previous command execution fails due to any reasons. It is recommended that the program should verify the command execution after issuing a command to the Flash controller. It is not cleared by reading but when a new command is issued. Possible causes of FAIL include address over range, or address falls into protected region.

CYC[2:0] Flash Command Time Out

CYC[2:0] defines command time out cycle count. Cycle period is defined by ISPCLK, which is SYSCLK/256/(ISPCLKF[7:0]+1). The number of cycles is tabulated as following.

CYC[2:0]			WRITE	ERASE
0	0	0	55	5435
0	0	1	60	5953
0	1	0	65	6452
0	1	1	69	6897
1	0	0	75	7408
1	0	1	80	7906
1	1	0	85	8404
1	0	0	89	8889

For normal operations, CYC[2:0] should be set to 111.

CMD4 – CMD0 Flash Command

These bits define commands for the Flash controller. The valid commands are listed in the following table. Any invalid commands do not get executed but return with a Fail bit.

CMD4	CMD3	CMD2	CMD1	CMD0	COMMAND
1	0	0	0	0	Main Memory Byte Read
0	1	0	0	0	Main Memory Sector Erase
0	0	1	0	0	Main Memory Sector Byte Write
0	0	0	1	0	IFB Byte Read
0	0	0	0	1	IFB Byte Write
0	0	0	1	1	-
1	0	0	1	0	-

FLSHDAT Flash Controller Data Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	Flash Data Register FLASH_DATA [7:0]							
WR	Flash Data Register FLASH_DATA [7:0]							

SFR Address: 0xA021 **Default: 0b00000000**

FLSHADL Flash Controller Low Address Data Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	Flash Address Low Byte Register ADDR[7:0]							
WR	Flash Address Low Byte Register ADDR[7:0]							

SFR Address: 0xA023 **Default: 0b00000000**

FLSHADH Flash Controller High Address Data Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	Flash Address High Byte Register ADDR[15:8]							
WR	Flash Address High Byte Register ADDR[15:8]							

SFR Address: 0xA022 **Default: 0b00000000**

ISPCLKF Flash Command Clock Scaler R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	ISPCLKF[7:0]							
WR	ISPCLKF[7:0]							

SFR Address: 0xA024 **Default: 0b00100101**

ISPCLKF[7:0] configures the clock time base for generation of Flash erase and write timing. ISPCLK = SYSCLK * (ISPCLKF[7:0]+1)/256. For correct timing, ISPCLK should be set to approximately at 2MHz.

FLSHSPRT Flash Controller Section Protection Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	FLSHPRT[7:0]							
WR	FLSHPRT[7:0]							

SFR Address: 0xA012 **Default: 0b00001111**

All bits in FLSHPRT are set to 1 by power-on or reset. A bit can only be written to “0” by software and cannot be set to “1”. When a bit is “0”, the protection is on and disallowed erasure or modifications.

FLSHPRT[7] Flash Protect 7
This bit protect area 0xE000 – 0xEFFF

FLSHPRT[6] Flash Protect 6
This bit protect area 0xD000 – 0xDFFF

FLSHPRT[5] Flash Protect 5
This bit protect area 0x8000 – 0xCFFF

FLSHPRT[4] Flash Protect 4
This bit protect area 0x7000 – 0x7FFF

FLSHPRT[3] Flash Protect 3
This bit protect area 0x5000 – 0x6FFF
FLSHPRT[2] Flash Protect 2
This bit protect area 0x3000 – 0x4FFF
FLSHPRT[1] Flash Protect 1
This bit protect area 0x1000 – 0x2FFF. This section is further protected by FLSHCPRT.
FLSHPRT[0] Flash Protect 0
This bit protect area 0x0000 – 0x0FFF. This section is further protected by FLSHCPRT.

For contents reliability, the user program should turn off the corresponding access after initialization.

For 32K Flash version, FLSHPRT[7:4] are tied to VSS.

FLSHCPRT Flash Controller Code Protection Register R/W TB Protected

Bit	7	6	5	4	3	2	1	0
RD	-							STAT
WR	FLSHCPRT[7:0]							

SFR Address: 0xA013 **Default: 0b00000000**

This register further protects the code space (0x0000 – 0x6FFF). The protection is on after any reset. Within 5 second after reset, a specific waveform sequence through LININ pin can be used to turn off protection. This is determined by hardware. Software can also write “55” into this register to turn off protection. However, software turn off action does not take into effect until a wait time (approximately one second) has expired. Any write other than “55” will turn on the protection. STAT indicates the protection, STAT=1 indicates the protection is off, and STAT=0 indicates the protection is on.

Please note, boot code area (0x7000 – 0x7FFF) cannot be modified by Flash Controller.

EUART2 WITH LIN CONTROLLER (EUART2)

LIN-capable 16550-like EUART2 is an enhanced UART controller (EUART) with separate transmit and receive FIFO. Both transmit and receive FIFO are 15-bytes deep and can be parameterized for Interrupt triggering. The addition of FIFO significantly reduces the CPU load to handle high-speed serial interface. Transmit FIFO and receive FIFO have respective Interrupt trigger levels that can be set based on optimal CPU performance adjustment. The EUART2 also has dedicated 16-bit Baud Rate generator and thus provides accurate baud rate under wide range of system clock frequency. The EUART2 also provides LIN extensions that incorporate message handling and baud-rate synchronization. The block diagram of EUART2 is shown in the following.

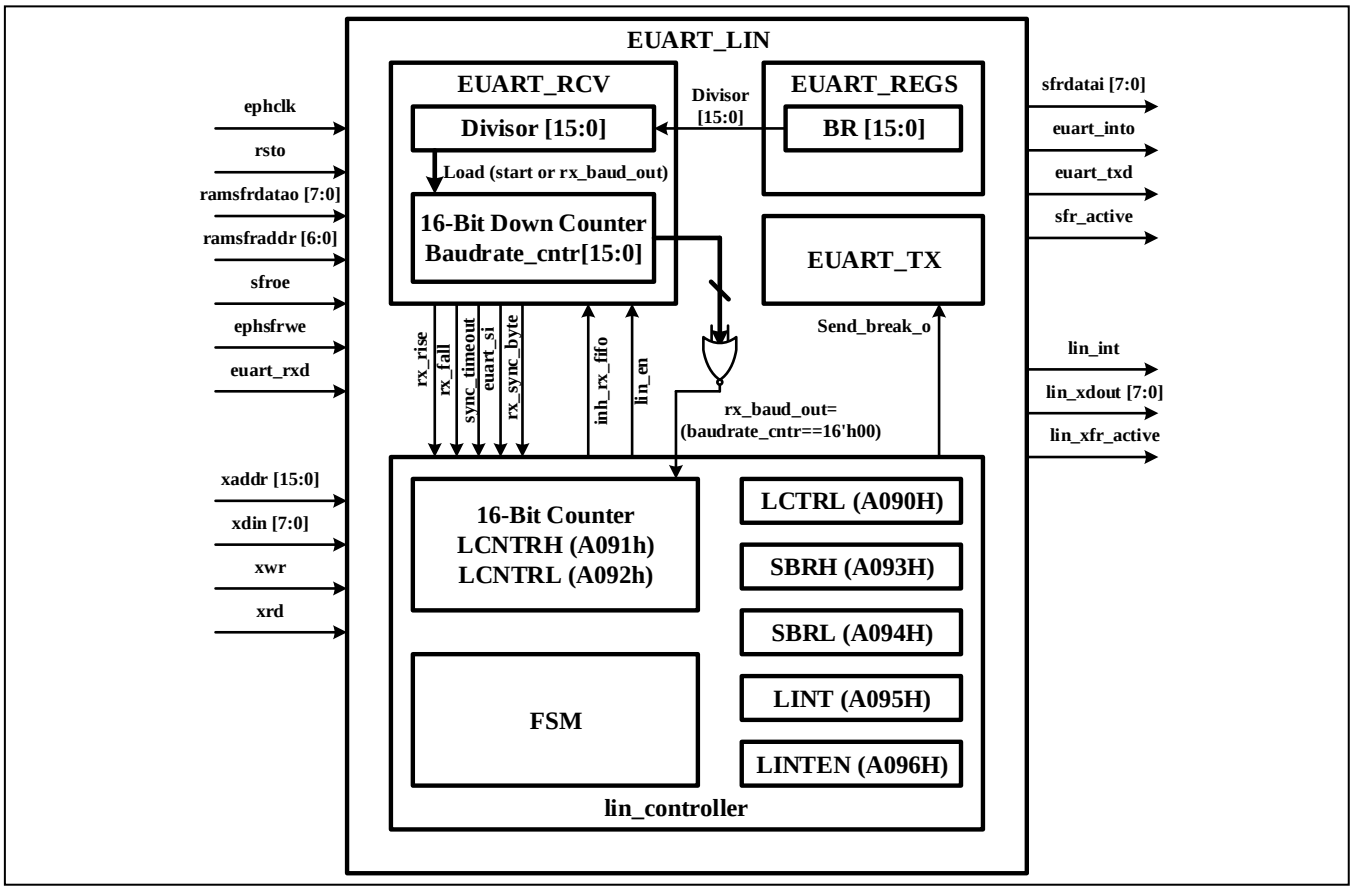


Figure 12 Block Diagram of EUART2

The following registers are used for configurations of and interface with EUART2.

SCON2 EUART2 Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	EUARTEN	SB	WLS[1]	WLS[0]	BREAK	OP	PERR	SP
WR	EUARTEN	SB	WLS[1]	WLS[0]	BREAK	OP	PE	SP

SFR Address: 0xC2 **Default: 0b00000000**

EUARTEN Transmit and Receive Enable bit
Set to enable EUART2 transmit and receive functions: To transmit messages in the TX FIFO and to store received messages in the RX FIFO.

SB Stop Bit Control
Set to enable 2 Stop bits, and clear to enable 1 Stop bit.

WLS[1:0] The number of bits of a data byte. This does not include the parity bit when parity is enabled.
00: 5 bits
01: 6 bits
10: 7 bits
11: 8 bits

BREAK Break Condition Control Bit.
Set to initiate a break condition on the UART interface by holding UART output at low until BREAK bit is cleared.

OP Odd/Even Parity Control Bit

PE/PERR Parity Enable / Parity Error status
Set to enable parity and clear to disable parity checking functions. If read, PERR=1 indicates a parity error in the current data of RX FIFO.

SP Parity Set Control Bit
When SP is set, the parity bit is always transmitted as 1.

SFIFO2 EUART2 FIFO Status/Control Register R/W

Bit	7	6	5	4	3	2	1	0
RD	RFL[3:0]				TFL[3:0]			
WR	RFLT[3:0]				TFLT[3:0]			

SFR Address: 0xA5 **Default: 0b00000000**

RFL[3:0] Current Receive FIFO level. This is read only and indicate the current receive FIFO byte count.

RFLT[3:0] Receive FIFO trigger threshold. This is write-only. RDA Interrupt will be generated when RFL[3:0] is greater than RFLT[3:0].

RFLT[3:0]	Description
0000	RX FIFO trigger level = 0
0001	RX FIFO trigger level = 1
0010	RX FIFO trigger level = 2
0011	RX FIFO trigger level = 3
0100	RX FIFO trigger level = 4
0101	RX FIFO trigger level = 5
0110	RX FIFO trigger level = 6
0111	RX FIFO trigger level = 7
1000	RX FIFO trigger level = 8
1001	RX FIFO trigger level = 9
1010	RX FIFO trigger level = 10
1011	RX FIFO trigger level = 11
1100	RX FIFO trigger level = 12
1101	RX FIFO trigger level = 13
1110	RX FIFO trigger level = 14
1111	Reserved

TFL[3:0] Current Transmit FIFO level. This is read only and indicate the current transmit FIFO byte count.

TFLT[3:0] Transmit FIFO trigger threshold. This is write-only. TRA Interrupt will be generated when TFL[3:0] is less than TFLT[3:0].

TFLT[3:0]	Description
0000	Reserved
0001	TX FIFO trigger level = 1
0010	TX FIFO trigger level = 2
0011	TX FIFO trigger level = 3
0100	TX FIFO trigger level = 4
0101	TX FIFO trigger level = 5
0110	TX FIFO trigger level = 6
0111	TX FIFO trigger level = 7
1000	TX FIFO trigger level = 8
1001	TX FIFO trigger level = 9
1010	TX FIFO trigger level = 10
1011	TX FIFO trigger level = 11
1100	TX FIFO trigger level = 12
1101	TX FIFO trigger level = 13
1110	TX FIFO trigger level = 14
1111	TX FIFO trigger level = 15

Receive and transmit FIFO can be reset by clear FIFO operation. This is done by setting BR[15:0]=0 and EUARTEN=0. This also clears RFO, RFU and TFO Interrupt flags without writing the Interrupt register. The LIN counter LCNTR is also cleared.

SINT2 EUART2 Interrupt Status/Enable Register R/W

Bit	7	6	5	4	3	2	1	0
RD	INTEN	TRA	RDA	RFO	RFU	TFO	FERR	TI
WR	INTEN	TRAEN	RDAEN	RFOEN	RFUEN	TFOEN	FERREN	TIEN

SFR Address: 0xA7 **Default: 0b00000000**

INTEN Interrupt Enable bit. (Write only)
Set to enable UART2 Interrupt. Clear to disable Interrupt. Default is 0.

TRA/TRAEN Transmit FIFO is ready to be filled.
This bit is set when transmit FIFO has been emptied below FIFO threshold. Write “1” to enable Interrupt. The flag is automatically cleared when the condition is absent.

RDA/RDAEN Receive FIFO is ready to be read.
This bit is set by hardware when receive FIFO exceeds the FIFO threshold. Write “1” to enable Interrupt. RDA will also be set when RFL < RFLT for bus idle duration longer than RFLT * 16 * Baud Rate. This is to inform software that there are still remaining unread received bytes in the FIFO. The flag is cleared when RFL < RFLT and writing “0” on the bit (the Interrupts is disabled simultaneously).

RFO/RFOEN Receive FIFO Overflow Enable bit.
This bit is set when overflow condition of receive FIFO occurs. Write “1” to enable Interrupt. The flag can be cleared by software, writing “0” on the bit (the Interrupt is disabled simultaneously), or by FIFO reset action.

RFU/RFUEN Receive FIFO Underflow Enable bit.
This bit is set when underflow condition of receive FIFO occurs. Write “1” to enable Interrupt. The flag can be cleared by software, writing “0” on the bit (the Interrupt is disabled simultaneously), or by FIFO reset action.

TFO/TFOEN Transmit FIFO Overflow Interrupt Enable bit.
This bit is set when overflow condition of transmit FIFO occurs. Write “1” to enable Interrupt. The flag can be cleared by software, writing “0” on the bit (the Interrupt is disabled simultaneously), or by FIFO reset action.

FERR/FERREN Framing Error Enable bit.
This bit is set when framing error occurs as the byte is received. Write “1” to enable Interrupt. The flag must be cleared by software, writing “0” on the bit (the Interrupt is disabled simultaneously).

TI/TIEN Transmit Message Completion Interrupt Enable bit.
This bit is set when all messages in the TX FIFO are transmitted and thus the TX FIFO becomes empty. Write “1” to enable Interrupt. The flag must be cleared by software, writing “0” on the bit (the Interrupt is disabled simultaneously).

SBUF2 EUART2 Data Buffer Register R/W

Bit	7	6	5	4	3	2	1	0
RD	EUART2 Receive Data Register							
WR	EUART2 Transmit Data Register							

SFR Address: 0xA6 **Default: 0b00000000**

This register is the virtual data buffer register for both receive and transmit FIFO. When being read, it reads out the top byte of the RX FIFO; when being written, it writes into the top byte of the TX FIFO.

EUART2 can be configured to add LIN capability. The major enhancement of LIN includes master/slave configurations, auto baud-rate synchronization, and frame based protocol with header. Under LIN extension mode, all EUART2 registers and functions are still effective and operational. LIN is a single-wire bus and it requires external components to combine RX and TX signals externally. LIN is frame based and consists of message protocols with master/slave configurations. The following diagram shows the basic composition of a header message sent by the master. It starts with BREAK, the SYNC byte, ID bytes, DATA bytes, and CRC bytes.

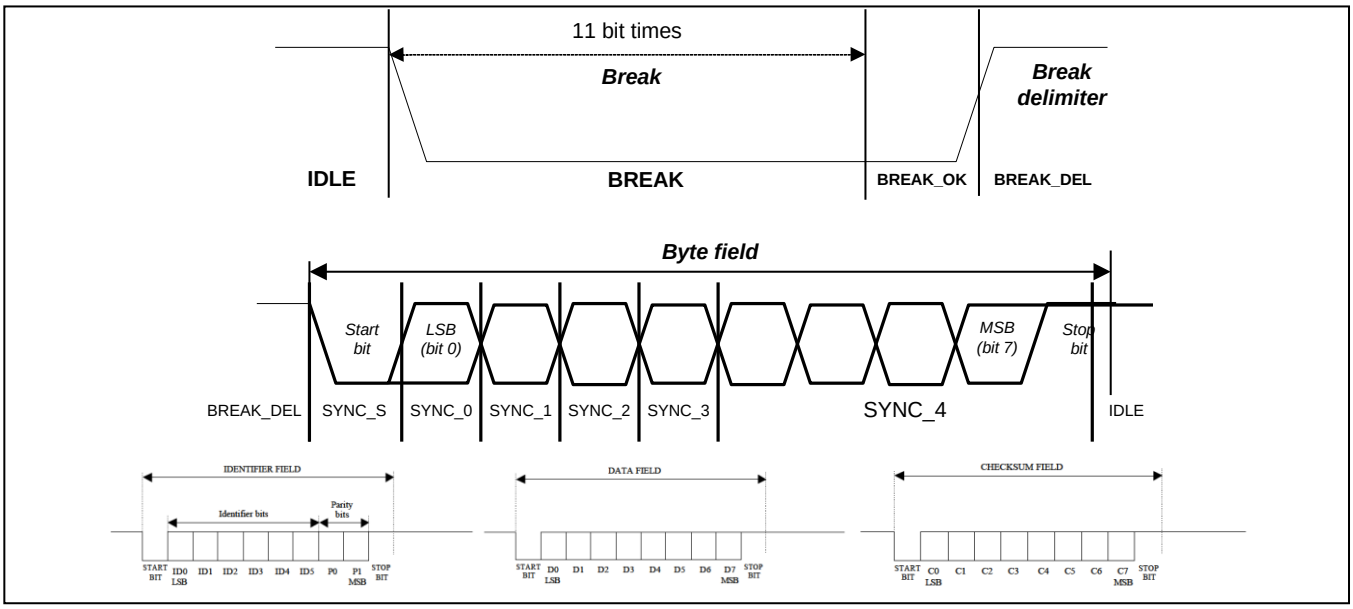


Figure 13 Basic Composition Of A Header Message

A LIN frame structure is shown and the frame time matches the number of bits sent and has a fixed timing.

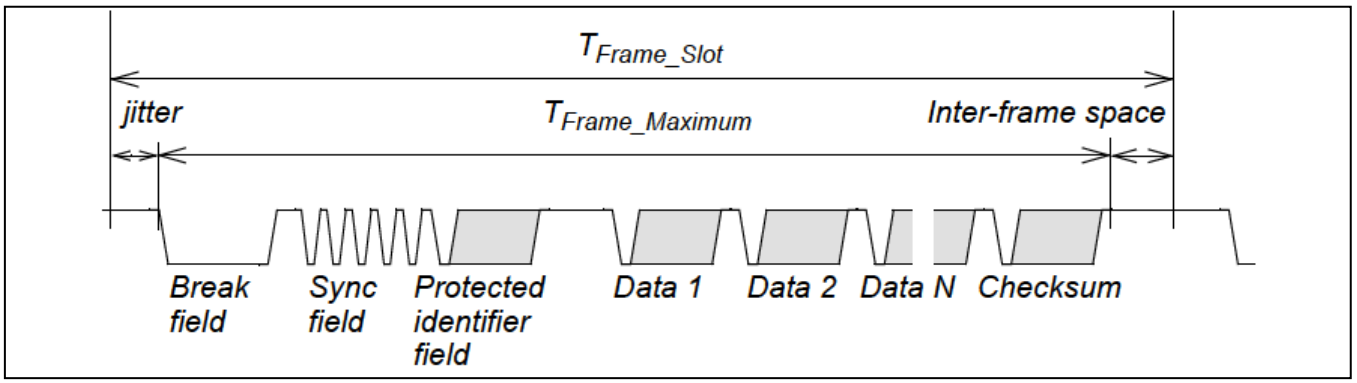


Figure 14 LIN Frame Structure

LIN bus protocol is based on frame. Each frame is partitioned into several parts as shown above. For master to initiate a frame, the software follows the following procedure.

STEP1: Initiate a SBK command. (SW needs to check if the bus is in idle state, and there is no pending transmit data).

STEP2: Write “55” into TFIFO.

STEP3: Write “PID” into TFIFO.

Wait for SBK to complete Interrupts and then write the following transmit data if applicable. (This is optional).

The following diagram shows Finite State Machine (FSM) of the LIN extension and is followed by registers within EUART2.

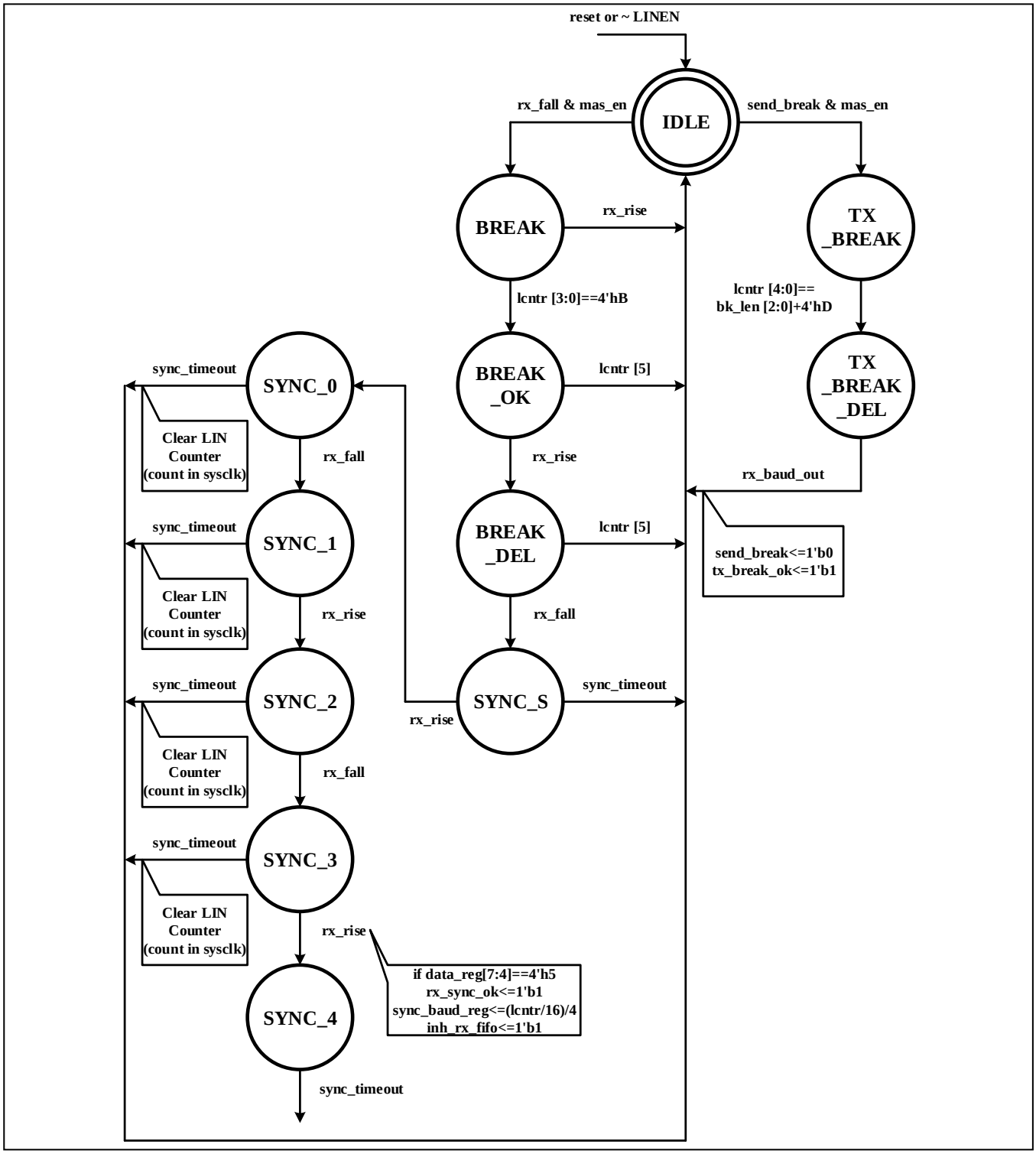


Figure 15 Finite State Machine (FSM) of the LIN Extension

LINCTRL LIN Status/Control Register R/W

Bit	7	6	5	4	3	2	1	0
RD	LINEN	MASEN	ASU	MASU	SBK	BL[2:0]		
WR	LINEN	MASEN	ASU	MASU	SBK	BL[2:0]		

SFR Address: 0xA090 **Default: 0b00000000**

LINEN LIN Enable (1: Enable / 0: Disable)
LIN header detection / transmission is functional when LINEN = 1.
Before enabling LIN functions, the EUART2 registers must be set correctly: 0xB0 is recommended for SCON2.

MASEN Master Enable bit (1: Master / 0: Slave) LIN operating mode selection. This bit is changeable only when LINEN = 0 (must clear LINEN before changing MASEN).

ASU Auto-Sync Update Enable (1: Enable / 0: Disable), Write Only
If ASU is 1, the LIN controller will automatically overwrite BR[15:0] with SBR[15:0] and issue an ASUI Interrupt when received a valid SYNC field.
If ASU is 0, the LIN controller will only notice the synchronized baud rate in SBR[15:0] by issuing an RSI Interrupt.
Please note, ASU should not be set under UART mode. ASU capability is based on the message containing BREAK and SYNC field in the beginning.
When ASU=1, the auto sync update is performed on every receiving frame, And is updated frame by frame.

MASU Message Auto Sync Update Enable.
MASU is meaningful only if ASU=0. MASU=1 will enable the auto sync update on the next received frame only. It is self-cleared when the sync update is completed. The software must set MASU again if another auto sync operation is desired.

SBK Send Break (1: Send / 0: No send request)
LINEN and MASEN should be set before setting SBK. When LINEN and MASEN are both 1, set SBK to send a bit sequence of 13+BL[2:0] consecutive dominant bits and 1 recessive bit (Break Delimiter). Once SBK is set, this bit represents the “Send Break” status and CANNOT be cleared by writing to “0”; instead, clearing LINEN cancels the “Send Break” action. In normal cases, SBK is cleared automatically when the transmission of Break Delimiter is completed.

BL[2:0] Break Length Setting
Break Length = 13 + BL[2:0]. Default BL[2:0] =0.

LINCNTRH LIN Timer Register High R/W

Bit	7	6	5	4	3	2	1	0
RD	LCNTR[15:8]							
WR	LINTMR[15:8]							

SFR Address: 0xA091 **Default: 0b11111111**

LINCNTRL LIN Time Register Low R/W

Bit	7	6	5	4	3	2	1	0
RD	LCNTR[7:0]							
WR	LINTMR[7:0]							

SFR Address: 0xA092 **Default: 0b11111111**

LCNTR[15:0] is read only and is an internal 16-bit counter clocked by the baud rate clock. LINTMR[15:0] is write only and is the timer limit for LCNTR[15:0]. If MASEN=1 as LIN master mode, this timer is used to generate Frame time base. The internal counter LCNTR[15:0] is cleared whenever a “SEND BREAK” command is executed, and when the counter reaches LINTMR [15:0] (LCNTR[15:0] >= LINTMR[15:0]), a LCNTRO Interrupt is generated. Thus the software can write a Frame Time value into LINTMR and use Interrupts to initiate frames. If MASEN=0 as LIN slave mode, this timer is used for determining the accumulated bus idle time. The internal counter is cleared whenever a RX transition occurs. When the internal counter reaches LINTMR[15:0], an LCNTRO Interrupt is generated. The software can use this Interrupt to enter Sleep mode by writing the required bus idling time into LINTMR[15:0].

LINSBRH EUART/LIN Baud Rate Register High byte RO

Bit	7	6	5	4	3	2	1	0
RD	SBR[15:8]							
WR	BR[15:8]							

SFR Address: 0xA093 **Default: 0b00000000**

LINSBRL EUART/LIN Baud Rate Register Low byte RO

Bit	7	6	5	4	3	2	1	0
RD	SBR[7:0]							
WR	BR[7:0]							

SFR Address: 0xA094 **Default: 0b00000000**

SBR[15:0] The acquired Baud Rate under LIN protocol. This is read-only.
SBR[15:0] is the acquired baud rate from last received valid sync byte. SBR is meaningful only in LIN-Slave mode.

BR[15:0] The Baud Rate Setting of EUART/LIN. This is write-only. BR[15:0] cannot be 0.
BUAD RATE = SYSCLK/(BR[15:0]+1).

When a slave receives a BREAK followed by a valid SYNC field, an RSI Interrupt is generated and the acquired baud rate from SYNC field is stored in SBR[15:0]. The acquired baud rate is BAUD RATE = SYSCLK/(BR[15:0]+1). The software can just update this acquired value into BR[15:0] to achieve synchronization with the master. If Auto-Sync Update (ASU) register bit is enabled under LIN slave mode, LIN controller will automatically perform the update of BR[15:0] with SBR[15:0] and issue another ASUI Interrupt when received a valid SYNC field.

LININT LIN Interrupt Flag Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	BITERR	LSTAT	LIDLE	ASUI	SBKI	RSI	LCNTRO
WR	-	BITERR	-	-	ASUI	SBKI	RSI	LCNTRO

SFR Address: 0xA095 **Default: 0b00000000**

BITERR Bit Error
BITERR is set by hardware when received bit does not match with transmit bit in transmit mode. If BERIE=1, then this error generates an Interrupt. BITERR must be cleared by software. It must be cleared by writing “0” in the bit.

LSTAT LIN Bus Status bit (1: Recessive / 0: Dominant), Read only.
LSTAT = 1 indicates that the LIN bus (RX pin) is in recessive state.

LIDLE LIDLE is 1 when LIN bus is idle and not transmitting/receiving LIN header or data bytes. This bit read only. It is 1 when LINEN = 0.

ASUI Auto-Sync Updated completion Interrupt (1: Set / 0: Clear)
This flag is set when auto baud rate synchronization has been completed and BR[15:0] has been updated with SBR[15:0] by hardware. It must be cleared by writing “1” on the bit.

SBKI Send Break Completion Interrupt bit (1: Set / 0: Clear)
This flag is set when Send Break completes. It must be cleared by writing “1” in the bit.

RSI Receive Sync Completion Interrupt bit (1: Set / 0: Clear)
This flag is set when a valid Sync byte is received following a Break. It must be cleared by writing “1” in the bit.

LCNTRO LIN Counter Overflow Interrupt bit (1: Set / 0: Clear).
This flag is set when the LIN counter reaches 0xFFFF. It must be cleared by writing “1” in the bit.

LININTEN LIN Interrupt Enable Register R/W

Bit	7	6	5	4	3	2	1	0
RD	LINTEN	BERIE	-	SYNCVALID	ASUIE	SBKIE	RSIE	LCNTRIE
WR	LINTEN	BERIE	SYNCMD	TXPOL	ASUIE	SBKIE	RSIE	LCNTRIE

SFR Address: 0xA096 **Default: 0b00000000**

LINTEN	LIN Interrupt Enable (1: Enable / 0: Disable) Set to enable all LIN Interrupts. LINT flags should be checked before setting or modifying.
BERIE	Bit Error Interrupt Enable (1: Enable / 0: Disable)
SYNCMD	1: ASU and MASU auto sync tracking function for new baud rate 0: ASU and MASU auto sync tracking function for a little baud rate changed
SYNCVALID	valid sync waveform
TXPOL	transmit output polarity
ASUIE	Auto-Sync Update Interrupt Enable (1: Enable / 0: Disable)
SBKIE	Send Break Completion Interrupt Enable (1: Enable / 0: Disable)
RSIE	Receive Sync Completion Interrupt Enable (1: Enable / 0: Disable)
LCNTRIE	LIN Counter Overflow Interrupt Enable (1: Enable / 0: Disable)

LINTCON LIN Time Out configuration R/W

Bit	7	6	5	4	3	2	1	0
RD	RXDTO[0]	LINRXFEN	-	-	RXDD_F	TXDD_F	RXDDEN	TXDDEN
WR	RXDTO[0]	LINRXFEN	-	-	RXDD_F	TXDD_F	RXDDEN	TXDDEN

SFR Address: 0xA0A0 **Default: 0b00000000**

RXDTO[0]	RXD Dominant Time Out Timer [0] This is combined with RXDTOH and RXDTOL to form RXDTO[16:0]
LINRXFEN	Set LIN Controller leave BREAK state when RXD Dominant Fault
RXDDEN	RXD Dominant Fault Interrupt Enable
RXDD_F	RXD Dominant Fault Interrupt Flag RXDD_F is set to 1 by hardware and must be cleared by software
TXDDEN	TXD Dominant Fault Interrupt Enable
TXDD_F	TXD Dominant Fault Interrupt Flag TXDD_F is set to 1 by hardware and must be cleared by software

TXDTOL LIN TXD Dominant TimeOut LOW Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	TXDTO[7:0]							
WR	TXDTO[7:0]							

SFR Address: 0xA0A1 **Default: 0b00000000**

TXDTOH LIN TXD Dominant TimeOut HIGH Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	TXDTO[15:8]							
WR	TXDTO[15:8]							

SFR Address: 0xA0A2 **Default: 0b00000000**

TXDTO TXD Dominant Time Out =(TXDTO[15:0] +1) * SYSCLK

RXDTOL LIN RXD Dominant TimeOut LOW Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	RXDTO[8:1]							
WR	RXDTO[8:1]							

SFR Address: 0xA0A3 **Default: 0b00000000**

RXDTOH LIN RXD Dominant Time Out HIGH Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	RXDTO[16:8]							
WR	RXDTO[16:8]							

SFR Address: 0xA0A4 **Default: 0b00000000**

RXDTO RXD Dominant Time Out =(RXDTO[16:0] +1) * SYSCLK

BSDCLR Bus Stuck Dominant Clear Width Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	BSDCLR [7:0]							
WR	BSDCLR [7:0]							

SFR Address: 0xA0A5 **Default: 0b00000000**

BSDCLR Bus Stuck Dominant Clear Time = (BSDCLR[7:0] +1) * SOSC

BSDCLRH Bus Stuck Dominant Clear Width Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	BSDCLR [15:8]							
WR	BSDCLR [15:8]							

SFR Address: 0xA0A6 **Default: 0b00000000**

BSDWKC Bus Stuck Dominant Fault Wakeup configuration R/W

Bit	7	6	5	4	3	2	1	0
RD	BSDW_F	BFW_F	BSDWEN	BFWEN	WKFLT[3:0]			
WR	BSDW_F	BFW_F	BSDWEN	BFWEN	WKFLT[3:0]			

SFR Address: 0xA0A7 **Default: 0b00000000**

WKFLT LIN Wakeup time = (WKFLT[3:0]+1) * SOSC

BFWEN LIN Wakeup /Interrupt Enable.

BFW_F LIN Wakeup Interrupt Flag.
BFW_F is set to 1 by hardware and must be cleared by software.

BSDWEN LIN Bus Stuck Wakeup / Interrupt Enable.

TXDD_F LIN Bus Stuck Wakeup Interrupt Flag.
TXDD_F is set to 1 by hardware and must be cleared by software.

BSDACT Bus Stuck Dominant Active Width Registers R/W

Bit	7	6	5	4	3	2	1	0
RD	BSDACT[7:0]							
WR	BSDACT[7:0]							

SFR Address: 0xA0A8 **Default: 0b00000000**

BSDACT Bus Stuck Dominant Active Time =(BSDCLR[7:0] +1) * SOSC

SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is an enhanced synchronous serial hardware which is compatible with Motorola's SPI specifications. The SPI Controller includes 4-bytes FIFO for both transmit and receive. SPI Interface uses Master-Out-Slave-In (MOSI), Master-In-Slave-Out (MISO), Serial Clock (SCK) and Slave Select (SSN) for interface. SSN is low active and only meaningful in slave mode.

SPICR SPI Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	SPIE	SPEN	MSTR	CPOL	CPHA	SCKE	-	-
WR	SPIE	SPEN	MSTR	CPOL	CPHA	SCKE	-	-

SFR Address: 0xA1 **Default: 0b001000xx**

SPIE SPI interface Interrupt Enable bit.
SPEN SPI interface Enable bit.
MSTR SPI Master/Slave Switch. Set as a master, clear as a slave.
CPOL SPI interface Polarity bit: Set to configure the SCK to stay HIGH while the SPI interface is idling and clear to keep it LOW.
CPHA Clock Phase Control bit: If CPOL=0, set to shift output data at rising edge of SCK, and clear to shift output data at falling edge of SCK. If CPOL=1, set to shift output data at falling edge of SCK and clear to shift output data at rising edge of SCK.
SCKE Clock Selection bit in Master Mode: Set to delay 0.5 period of SCK to sample the input data. Clear to use normal edge of SCK to sample the input data.

In Slave mode, the sampling phase is determined by the combinations of CPOL and CPHA setting shown in the following table.

CPOL	CPHA	(Slave mode) SCK edge used for sampling input data	Data shift out
0	0	Rising edge	Falling edge
0	1	Falling edge	Rising edge
1	0	Falling edge	Rising edge
1	1	Rising edge	Falling edge

SPIMR SPI Mode Control Register R/W

Bit	7	6	5	4	3	2	1	0
RD	ICNT1	ICNT0	FCLR	-	SPR[2]	SPR[1]	SPR[0]	DIR
WR	ICNT1	ICNT0	FCLR	-	SPR[2]	SPR[1]	SPR[0]	DIR

SFR Address: 0xA2 **Default: 0b00000000**

ICNT1, ICNT0 FIFO Byte Count Threshold. This sets the FIFO threshold for generating SPI Interrupts.
00 The Interrupt is generated after 1 byte is sent or received.
01 The Interrupt is generated after 2 bytes are sent or received.
10 The Interrupt is generated after 3 bytes are sent or received.
11 The Interrupt is generated after 4 bytes are sent or received.

FCLR FIFO Clear/Reset. Set to clear and reset the transmit and receive FIFO
SPR[2:0] SPI Clock Rate Setting. This is used to control the SCK clock rate of SPI interface.
000 SCK = SYSCLK/4
001 SCK = SYSCLK/6
010 SCK = SYSCLK/8
011 SCK = SYSCLK/16
100 SCK = SYSCLK/32
101 SCK = SYSCLK/64
110 SCK = SYSCLK/128
111 SCK = SYSCLK/256

DIR SPI Transfer Format
0 SPI uses LSB-first format.
1 SPI uses MSB-first format.

SPIST SPI Status Register R/W

Bit	7	6	5	4	3	2	1	0
RD	SSPIF	ROVR	TOVR	TUDR	RFULL	REMPT	TFULL	TEMPT
WR	SSPIF	ROVR	TOVR	TUDR	-	-	-	-

SFR Address: 0xA3 **Default: 0b00000000**

SSPIF SPI Interrupt Flag bit. Set by hardware to indicate the completion of data transfer. Clear by assigning this bit to 0 or disabling SPI.

ROVR Receive FIFO-overrun Error Flag bit. When Receiver FIFO Full Status occurs and SPI receives new data, ROVR is set and generates an Interrupt. Clear by assigning this bit to 0 or disabling SPI.

TOVR Transmit FIFO-overrun Error Flag bit. When Transfers FIFO Full Status occurs and new data is written, TOVR is set and generates an Interrupt. Clear by assigning this bit to 0 or disabling SPI.

TUDR Transmit Under-run Error Flag bit. When Transfers FIFO Empty Status and new data transmission occur, TOVR is set and generates an Interrupt. Clear by written 0 to this bit or disable SPI.

RFULL Receive FIFO Full Status bit. Set when receiver FIFO is full. Read only.

REMPT Receive FIFO Empty Status bit. Set when receiver FIFO is empty. Read only.

TFULL Transmitter FIFO Full Status bit. Set when transfer FIFO is full. Read only.

TEMPT Transmitter FIF0 Empty Status bit. Set when transfer FIFO is empty. Read only.

SPIDATA SPI Data Register R/W

Bit	7	6	5	4	3	2	1	0
RD	SPI Receive Data Register							
WR	SPI Transmit Data Register							

SFR Address: 0xA4 **Default: 0bxxxxxxxx**

SPI Master Timing Illustration

CPOL=0 CPHA=0

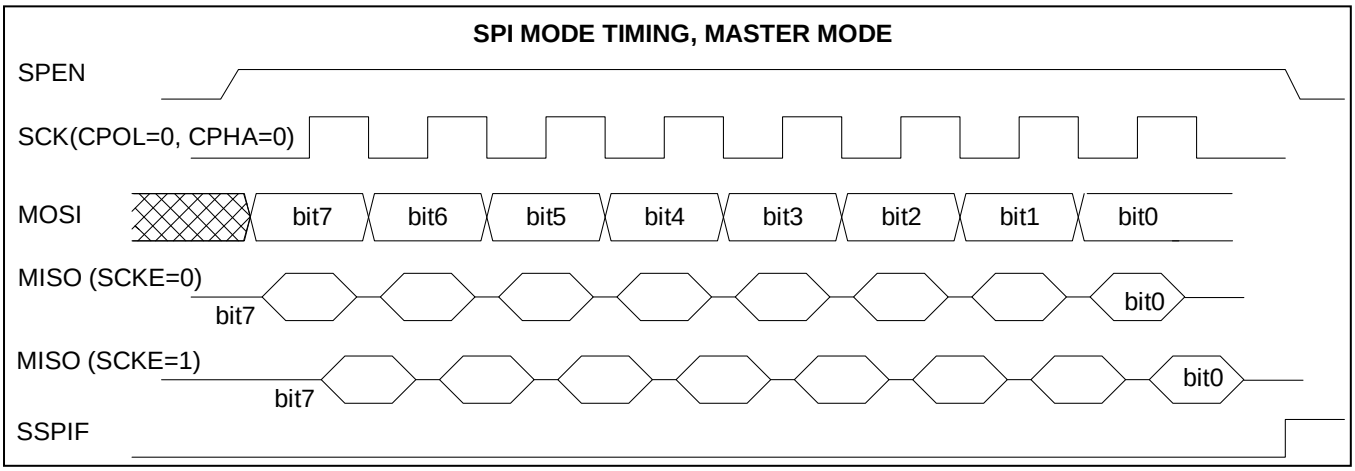


Figure 16 SPI Master Timing CPOL=0 CPHA=0

CPOL=0 CPHA=1

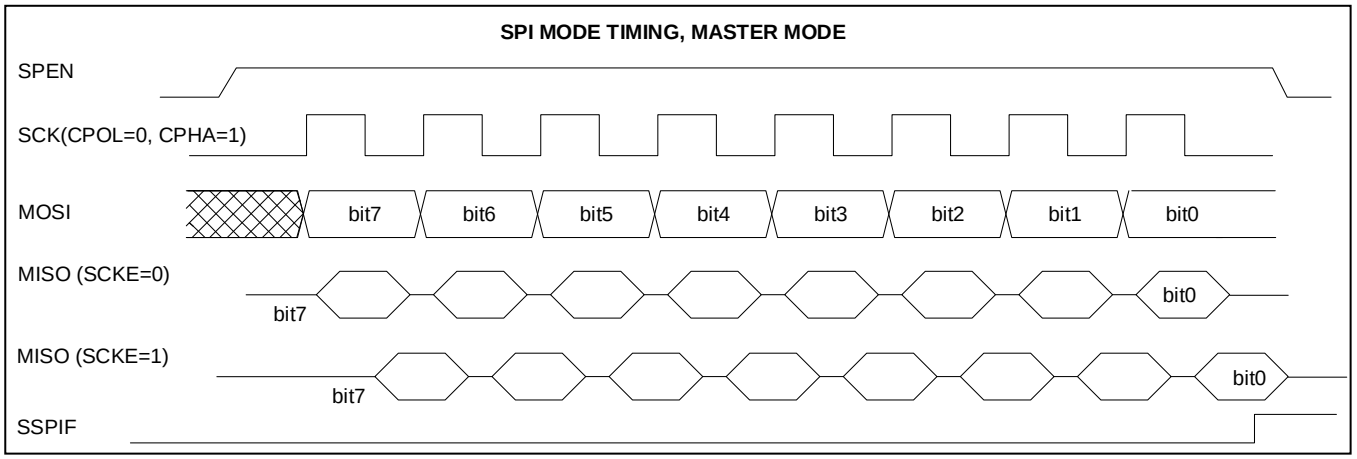


Figure 17 SPI Master Timing CPOL=0 CPHA=1

CPOL=1 CPHA=0

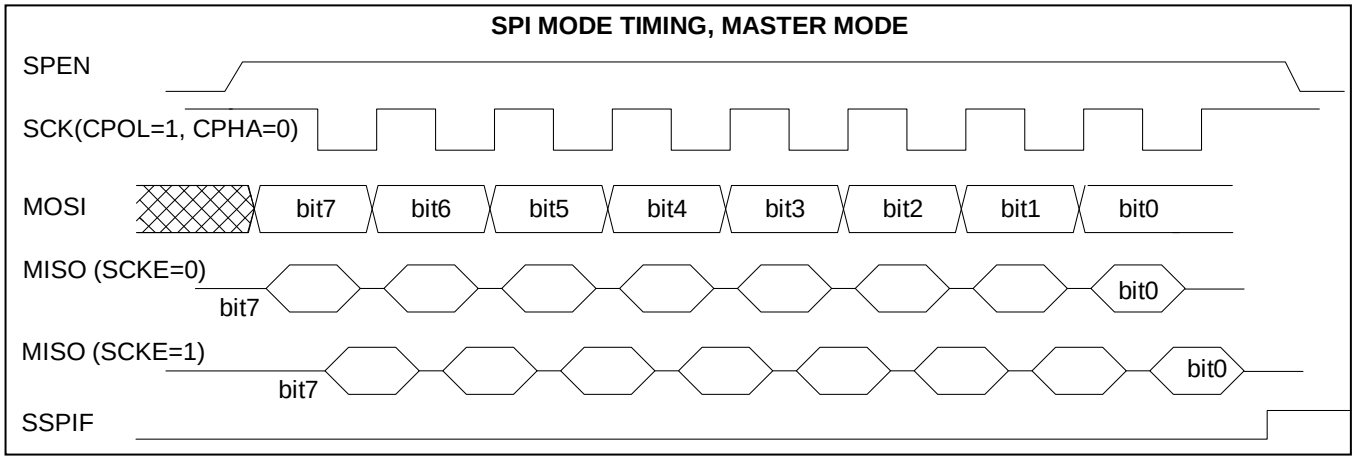


Figure 18 SPI Master Timing CPOL=1 CPHA=0

CPOL=1 CPHA=1

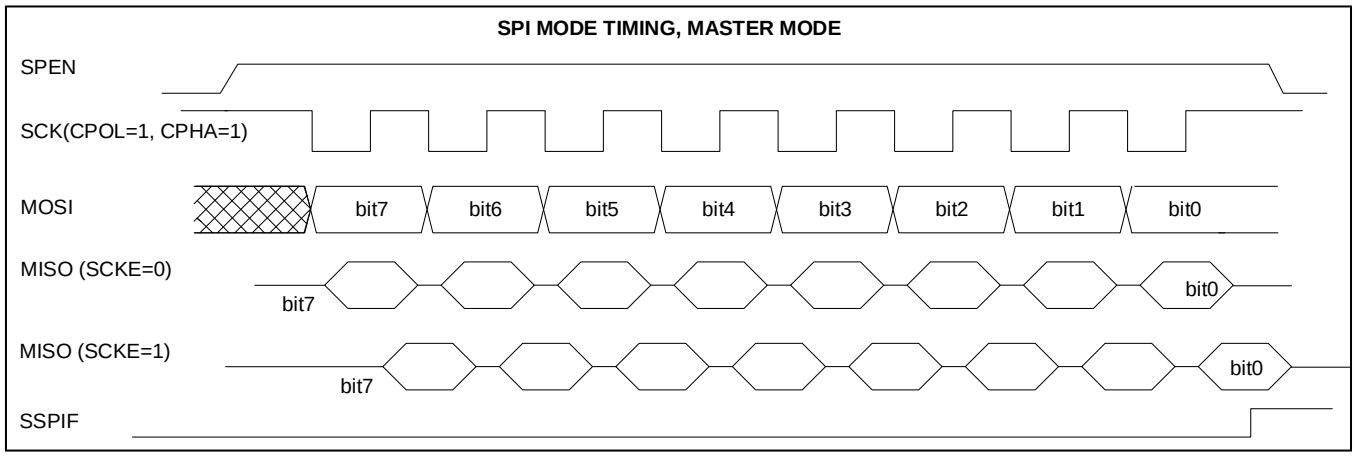


Figure 19 SPI Master Timing CPOL=1 CPHA=1

PWMH CONTROLLER

The PWM is based on a 16-bit Programmable Counter, which generates a counting value according to mode setting preferably, The PWM controller also provides synchronous ADC conversion and software Interrupt trigger. The block diagram and timing relationship is shown as following.

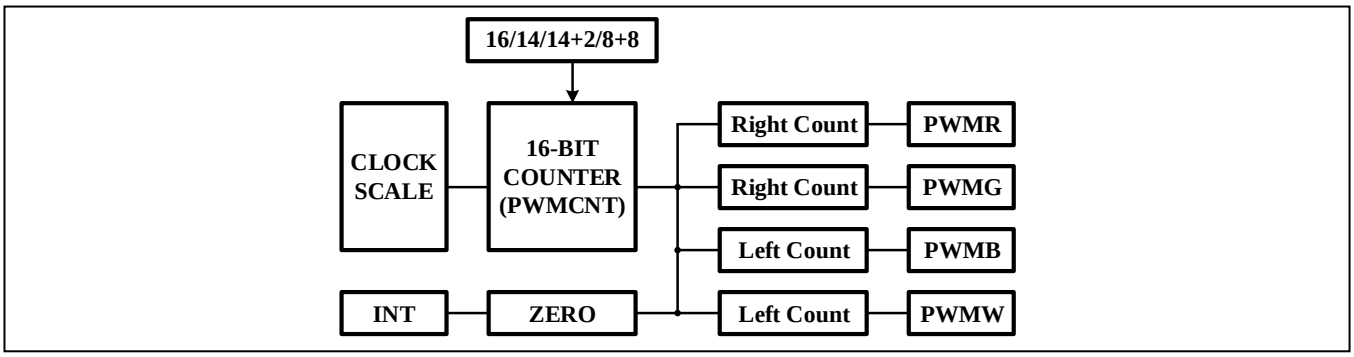


Figure 20 PWM Block Diagram

There are four PWM channels defined as PWMR(HV0), PWMG(HV1), PWMB(HV2), and PWMW(HV3), which are routed to HVIO outputs for LED driving.

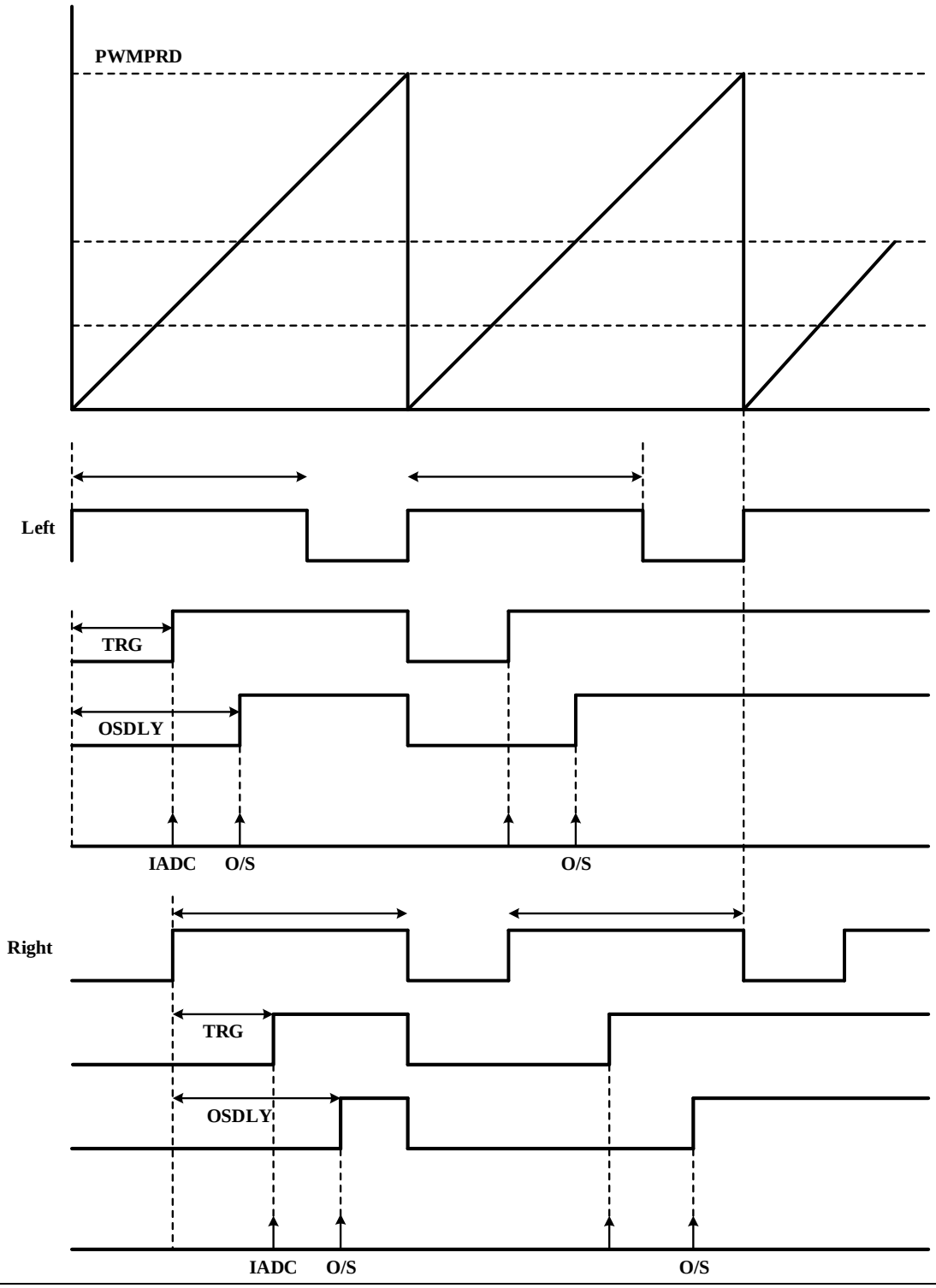


Figure 21 PWM Timing Relationship

PWMHCFG PWMH Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWMEN	PWMSTOP	PWMPOL	CS[4:0]				
WR	PWMEN	PWMSTOP	PWMPOL	CS[4:0]				

SFR Address: 0xA08E **Default: 0b00000010**

PWMEN PWM Enable

PWMEN=0 disables the PWM. It also clears all counter and forces all outputs to 0.
PWMEN=1 enables the PWM. When enabled, the PWM always starts at PWMCNT=0.

PWMSTOP — PWM Stop Bit
PWMSTOP=1 will temporarily stop the PWM counting.
PWMSTOP=0 resumes the PWM counting.

PWMPOL — PWM Output Polarity
PWMPOL=1 will invert the output polarity. PWMPOL=0 for normal operation.

CS[4:0] — PWM Clock Scaling Setting bits.
The PWMCLK is derived from SYSCLK/(CS[4:0]+1)

PWMHUPD PWMH Update Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-							PUDEN
WR	PWMHUPDATE [7:0]							

SFR Address: 0xA089 **Default: 0b00000000**

Writer 0xA5 update PWMH value and will auto clear to 0x00.

PUDEN=1, PWM controller will update at next PWM ending.

PWMHOSC PWMH Mode Register R/W

Bit	7	6	5	4	3	2	1	0
RD	OSCPWM_EN	OSCPWM [2:0]			Dithering [1:0]		VBATDIV_SEL	VBATADC_EN
WR	OSCPWM_EN	OSCPWM [2:0]			Dithering [1:0]		VBATDIV_SEL	VBATADC_EN

SFR Address: 0xA08A **Default: 0b11111111**

OSCPWM_EN — PWM OSC Enable.

OSCPWM [2:0] — PWMH Spread Spectrum Frequency.

OSCPWM [2]	OSCPWM [1]	OSCPWM [0]	Function
x	x	0	SSC OFF
x	1	1	FRE=625Hz
x	0	1	FRE=5kHz
1	x	1	SSC±10%
0	x	1	SSC±15%

Dithering [1:0] — Dithering Mode.
00: 16 bits mode
01: 14 bits mode
10: 14+2 mode
11: 8+8 mode

VBATDIV_SEL — VBAT DIV Select.
VBATDIV_SEL = 1 turns on the 1/6 attenuation circuit and connect the attenuated input to ADC input
VBATDIV_SEL = 0 turns on the 1/12 attenuation circuit and connect the attenuated input to ADC input

VBATADC_EN — VBAT ADC Enable.

PWMHRL PWMH RED Duty Low Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWMHR[7:0]							
WR	PWMHR[7:0]							

SFR Address: 0xA080 **Default: 0b00000000**

PWMHRH PWMH RED Duty High Register RW

Bit	7	6	5	4	3	2	1	0
RD	PWMHR[15:8]							
WR	PWMHR[15:8]							

SFR Address: 0xA081 **Default: 0b00000000**

PWMHGL PWMHGREEN Duty Low Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWMHG[7:0]							
WR	PWMHG[7:0]							

SFR Address: 0xA082 **Default: 0b00000000**

PWMGH PWMH GREEN Duty High Register RW

Bit	7	6	5	4	3	2	1	0
RD	PWMHG[15:8]							
WR	PWMHG[15:8]							

SFR Address: 0xA083 **Default: 0b00000000**

PWMHBL PWMH BLUE Duty Low Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWMHB[7:0]							
WR	PWMHB[7:0]							

SFR Address: 0xA084 **Default: 0b00000000**

PWMHBH PWMH BLUE Duty High Register RW

Bit	7	6	5	4	3	2	1	0
RD	PWMHB[15:8]							
WR	PWMHB[15:8]							

SFR Address: 0xA085 **Default: 0b00000000**

PWMHWL PWMH WHITE Duty Low Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWMHW[7:0]							
WR	PWMHW[7:0]							

SFR Address: 0xA086 **Default: 0b00000000**

PWMHWH PWM WHITE Duty High Register RW

Bit	7	6	5	4	3	2	1	0
RD	PWMHW[15:8]							
WR	PWMHW[15:8]							

SFR Address: 0xA087 **Default: 0b00000000**

OSDLY Open/Short Detected delay Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	OSDLY[3:0]			
WR	-	-	-	-	OSDLY[3:0]			

SFR Address: 0xA08B **Default: 0b00000111**

OSDLY [3:0] Open/Short Detected delay
The turn-on Open/Short Detection is specified at
PWM start position +((OSDLY[3:0] +1)*8 -1)* PWMCLK

PWMHTRG PWMH Trigger Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWMHTRG[7:0]							
WR	PWMHTRG[7:0]							

SFR Address: 0xA08C **Default: 0b00000000**

PWMHTRG [7:0] ADC trigger delay
The turn-on ADC calculation is specified at
PWM start position +((PWMHTRG[7:0]*2)+1)* PWMCLK

PWMINTE PWM Interrupt Control Register R/W

Bit	7	6	5	4	3	2	1	0
RD	TRGEN	TRGCH[1:0]		R2HEIE	TRGIE	UNDIE	OVERIE	ZIE
WR	TRGEN	TRGCH[1:0]		R2HEIE	TRGIE	UNDIE	OVERIE	ZIE

SFR Address: 0xA08D **Default: 0b00000000**

TRGEN Trigger Enable, if R2MAEN=0.
TRGEN is set to 1 by software and auto clear when Trigger condition occurs.

TRGCH[1:0] Selected Trigger channel.
00: Red Channel
01: Greed Channel
10: Blue Channel
11: White Channel

R2HEIE R2MA hold time violation Interrupt Enable.

TRGIE Trigger Interrupt Enable.

UNDIE Under Run Interrupt Enable.

OVERIE Over Run Interrupt Enable.

ZIE Zero Interrupt Enable.

PWMINTF PWM Interrupt Flag Register R/W

Bit	7	6	5	4	3	2	1	0
RD	WTRGF	BTRGF	GTRGF	RTRGF	ADCBUSY	UNDF	OVERF	ZF
WR	WTRGF	BTRGF	GTRGF	RTRGF	-	UNDF	OVERF	ZF

SFR Address: 0xA08F **Default: 0b00000000**

WTRGF White channel trigger Interrupt Flag
WTRGF is set to 1 by hardware when WTRGF Interrupt occurs. This bit must be cleared by software.

BTRGF Blue channel trigger Interrupt Flag
BTRGF is set to 1 by hardware when BTRGF Interrupt occurs. This bit must be cleared by software.

GTRGF	Green channel trigger Interrupt Flag GTRGF is set to 1 by hardware when GTRGF Interrupt occurs. This bit must be cleared by software.
RTRGF	Red channel trigger Interrupt Flag RTRGF is set to 1 by hardware when RTRGF Interrupt occurs. This bit must be cleared by software.
ADCBUSY	ADC busy
UNDF	PWM go low, during ADC calculation period UNDF is set to 1 by hardware when Under Run condition occurs. This bit must be cleared by software.
OVERF	ADC calculation over PWM period OVERF is set to 1 by hardware when over condition occurs. This bit must be cleared by software.
ZF	Zero Interrupt Flag ZF is set to 1 by hardware when Zero Interrupt occurs. This bit must be cleared by software.

R2MACFG RVF 2MA Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	R2MAEN	HOLDEF	TS2MA[5:0]					
WR	R2MAEN	HOLDEF	TS2MA[5:0]					

SFR Address: 0xA09E **Default: 0b00000000**

R2MAEN	VF 2mA Reference Control Enable R2MAEN=1 enables the VF reference control. This does not control the reference circuit itself only controls the HVIO's output.
HOLDEF	Hold time violation flag Red PWM change to "High" during temperature measurement.
TS2MA[5:0]	VF Setup Time The turn-on is started on PWMCNT= ((TS2MA[5:0] +1) *16) *SYSCLK

SSCCFG PWMH SSC Configure Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	SSCEN	SSCSET[2:0]		
WR	-	-	-	-	SSCEN	SSCSET[2:0]		

SFR Address: 0xA09F **Default: 0b00000000**

SSCEN	Enable PWMSSC Reset
SSCSET [2:0]	PWM SSC Reset Period PWMSSC Reset condition is ((SSCSET +1) * PWM Period) and PWMEN rising.

ESSENTIAL ANALOG CIRCUITS

Power Supply and Reference

The power supply is from VS pin typically connected to an external power supply such as battery (VBAT) with voltage range of 5.5V~18V. Ignoring the voltage drop between VBAT and VS due to wiring harness or other protection devices, let's assume that VBAT = VS in this document. The power supply and internal regulators and reference generator are shown in the following block diagram.

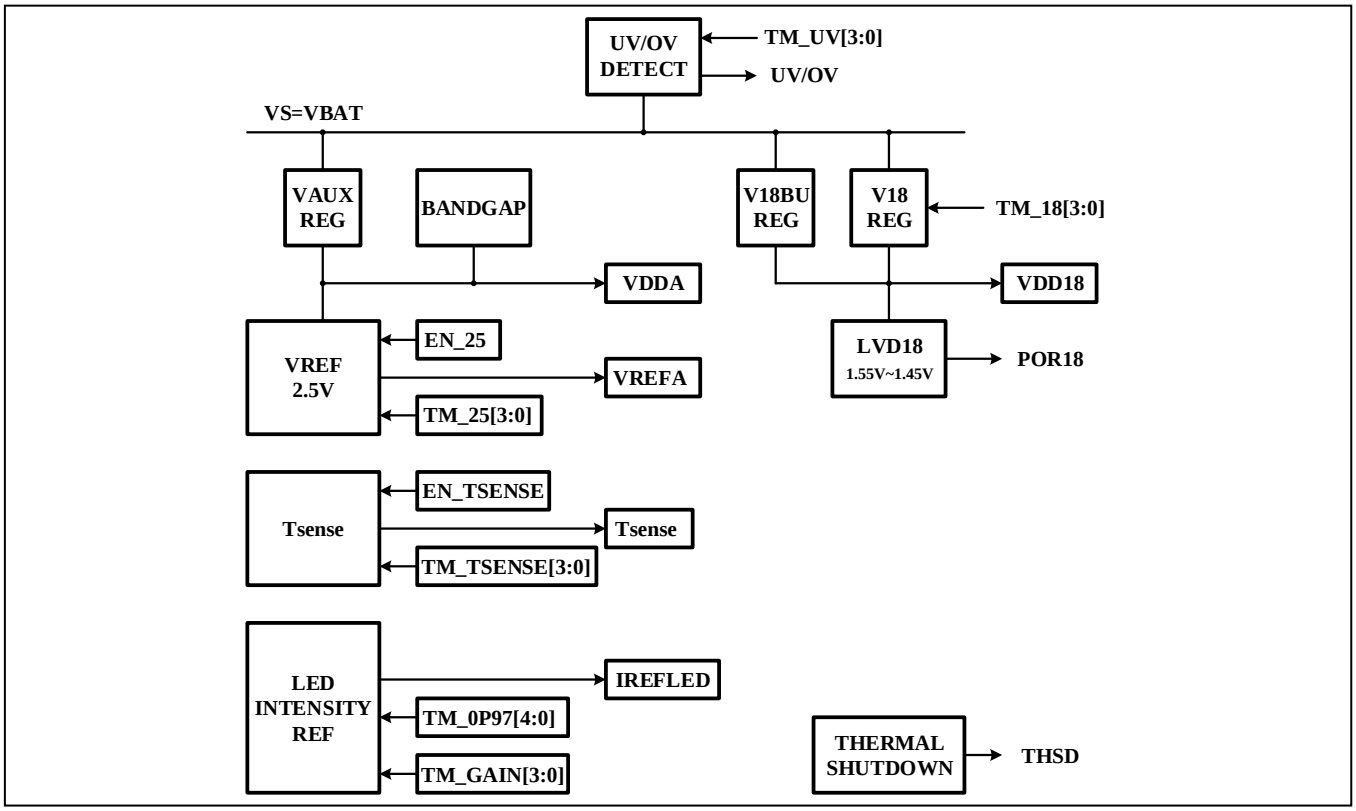


Figure 22 The Power Supply And Internal Regulators And Reference Generator Block Diagram

There are three regulators. VAUX provides VDDA (approximately 5V) for internal analog circuit. VAUX regulator is always active. VDD18 has a main regulator and back-up regulator and provides power for internal logic and embedded flash. The main V18 regulator can be trimmed to exact 1.8V and is active during normal operation. When CPU enters Sleep mode, the main regulator is turned off and the backup regulator provides VDD18 with 1.65V and up to 1mA capability.

VREF (2.5V) is generated from internal band-gap and used as ADC full-scale reference. VREF can be trimmed and calibrated.

The power-on reset is VDD18 < 1.45V. This condition is providing power-on reset to the internal logic and CPU.

An under-voltage and over-voltage detector with programmable detect level monitors the battery voltage. When enabled it generates Interrupt and software can take appropriate actions. A thermal shutdown detection circuit is there detection chip temperature of 160°C and can trigger Interrupt.

A number of voltage references can be trimmed such as V18 and V25. Trimming is performed in factory during production final test stage (FT). The trimmed data will be stored in flash. During system initialization, the trimmed data is loaded from flash to Trim registers for circuit operation by software. Trim registers are write protected and they should not be altered in any way by the end user.

REGTRIM Regulator Trim Register R/W TB protected

Bit	7	6	5	4	3	2	1	0
RD	-	-			TM_18[3:0]			
WR	-	-			TM_18[3:0]			

SFR Address: 0xA008 **Default: 0b00000000**

TM_18[3:0]	0000: +0mV	0001:	+16mV	0010: +31.7mV	0011: +47mV
	0100: +62.7mV	0101:	+78.2mV	0110: +93.6mV	0111: +106.6mV
	1000: -11mV	1001:	-25.6mV	1010: -40.9mV	1011: -56.3mV
	1100: -71.7mV	1101:	-87.2mV	1110: -102.7mV	1111: -118.2mV

REFTRIM REF 2.5V Generator Trim Register R/W TB protected

Bit	7	6	5	4	3	2	1	0
RD	THSDEN	LDOADC_EN	EN_TSENSE	EN_25	TM_25[3:0]			
WR	THSDEN	LDOADC_EN	EN_TSENSE	EN_25	TM_25[3:0]			

SFR Address: 0xA009 **Default: 0b00000000**

THSDEN Thermal Shutdown Detection Circuit Enable
LDOADC_EN Improve ADC performance when VBAT>6V
EN_TSENSE On die temperature sensor enable
EN_25 VREF25 Circuit Enable
TM_25[3:0] VREF25 Trim

0000:	+0mV	0001:	+22mV	0010:	+44.2mV	0011:	+66mV
0100:	+88mV	0101:	+110mV	0110:	+132mV	0111:	+154mV
1000:	-21mV	1001:	-43mV	1010:	-65mV	1011:	-87mV
1100:	-109mV	1101:	-131mV	1110:	-153mV	1111:	-175mV

REFILED REF LED Intensity Current Trim Register R/W TB protected

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	TM_0P97[4:0]				
WR	-	-	-	TM_0P97[4:0]				

SFR Address: 0xA00A **Default: 0b00000000**

TM_0P97[4:0]

00000:	+0mV	00001:	+11.6mV	00010:	+23.2mV	00011:	+34.7mV
00100:	+46.3mV	00101:	+57.8mV	00110:	+69.4mV	00111:	+80.9mV
01000:	+92.5mV	01001:	+104mV	01010:	+115.5mV	01011:	+127.1mV
01100:	+138.7mV	01101:	+150.2mV	01110:	+161.7mV	01111:	+173.3mV
10000:	-11.5mV	10001:	-23mV	10010:	-34.5mV	10011:	-46mV
10100:	-57.5mV	10101:	-69mV	10110:	-80.5mV	10111:	-92mV
11000:	-103.5mV	11001:	-115mV	11010:	-126.5mV	11011:	-138mV
11100:	-149.5mV	11101:	-161mV	11110:	-172.5mV	11111:	-184mV

REFGLED REF LED Intensity Current Gain Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	TM_GAIN[3:0]			
WR	-	-	-	-	TM_GAIN[3:0]			

SFR Address: 0xA00B **Default: 0b00000000**

TM_GAIN[3:0]

0000:	+0mA	0001:	+4mA	0010:	+8mA	0011:	+12mA
0100:	+16mA	0101:	+20mA	0110:	+24mA	0111:	+28mA
1000:	+32mA	1001:	+36mA	1010:	+40mA	1011:	+44mA
1100:	+48mA	1101:	+52mA	1110:	+56mA	1111:	+60mA

UVOVTRIM Under Voltage and Over Voltage Detection Trim Register R/W TB protected

Bit	7	6	5	4	3	2	1	0
RD	EN_UV	TM_UV[2:0]			EN_OV	-		
WR	EN_UV	TM_UV[2:0]			EN_OV	-		

SFR Address: 0xA00D **Default: 0b00000000**

EN_UV Under-Voltage Detect Circuit Enable
TM_UV[2:0] Under Voltage Level

000: 5.0V 001:5.5V 010:6.0V 011:6.5V

100: 7.0V 101:7.5V 110:8.0V 111:8.5V

EN_OV Over-Voltage Detect Circuit Enable

BTTRIM BG And TSENSE Voltage Trim Register R/W TB protected

Bit	7	6	5	4	3	2	1	0
RD	TM_BG[3:0]				TM_TSENSE[3:0]			
WR	TM_BG[3:0]				TM_TSENSE[3:0]			

SFR Address: 0xA00E **Default: 0b00000000**

TM_BG[3:0] Band Gap Trim Values

0000: 1235+0mV 0001: +13.2mV 0010: +26.4mV 0011: +39.6mV

0100: +52.8mV 0101: +66mV 0110: +79.2mV 0111: +92.4mV

TM_TSENSE[3:0] Temperature Sense Reference Trim Values

0000: 1600+0mV 0001: +26.8mV 0010: +53.6mV 0011: +80.4mV

0100: +107.2mV 0101: +134mV 0110: +160.8mV 0111:+187.6mV

PWRINT Power Supply Interrupt Register R/W

Bit	7	6	5	4	3	2	1	0
RD	PWRIEN	OVF	UVF	THSDF	-	OV	UV	THSD
WR	PWRIEN	OVF	UVF	THSDF	-	-	-	-

SFR Address: 0xA00F **Default: 0b00000000**

PWRIEN Power Supply and Thermal Shut Down Interrupt Enable

OVF Over Voltage Flag

OVF is set to 1 by hardware and must be cleared by software

UVF Under Voltage Flag

UVF is set to 1 by hardware and must be cleared by software

THSDF Thermal Shut Down Flag (what is OT set and release temperature)

THSDF is set to 1 by hardware and must be cleared by software

OV Over Voltage Real Time Status

UV Under Voltage Real Time Status

THSD Thermal Shut Down Real Time Status

IOSC 16MHz

An on-chip 16MHz Oscillator with low temperature coefficient provides the system clock to the CPU and other logic. IOSC uses VDD18 as supply and can be calibrated and trimmed. The accuracy of the frequency is +/- 2% within the operating conditions. This oscillator is stopped and enters into stand-by mode when CPU is in Stop/Sleep mode and resumes oscillation when CPU wakes up.

IOSCFTRM IOSC Fine Trim Register RW TB protected

Bit	7	6	5	4	3	2	1	0
RD	IOSCFTRM[7:0]							
WR	IOSCFTRM[7:0]							

SFR Address: 0xA018 **Default: 0b00000000**

This is used to trim the IOSC clock frequency.

IOSCFTRM[7:0] 00000000: 16M+00Hz 00000001: +36.58kHz

01111111: +4.667MHz 11111111: -26.62kHz

10000000: -3.3811MHz

Frequency increase LSB: +36.58kHz (0.23%)

Frequency decrease LSB: -26.62kHz (0.17%)

SOSC 24kHz

An ultra-low power slow oscillator of 24kHz is also present for use as wake-up (through T5) or Sleep mode system clock. SOSC is never powered down and consumes about 1uA from VAUX.

12-BIT SAR ADC

The ADC uses an internal generated reference voltage source of VREFA 2.5V as full range reference. This reference can be calibrated and trimmed. The ADC is a two-stage R ladder architecture and guarantees monotonicity. It also includes an offset cancellation circuit to minimize nonlinearity.

The ADC has four intrinsic channels – A, B, C, and D, and thus four result registers. ADC conversion can be started either by software command or by PWMH trigger. Each start event will automatically do conversions according to selected intrinsic channels A through D in sequence. The four intrinsic channels are further multiplexed to 10 channels as labeled in the block diagram.

To start ADC conversion, ADCEN must be set to 1 and wait for 2usec to stabilize circuit. Each channel conversion takes 16 ADC clock cycle (CHOPDIS=1/0). The maximum ADC clock rate is 4MHz.PRE[1:0] provide clock scaling from system clock.

ADC conversion can be started either by software command (setting CSTART=1) or by PWMH trigger. Each event will automatically do conversions according to enabled intrinsic channels A through D in sequence. When conversion completes, an ADC Interrupt is generated. A STAT bit is hardware set to 1 if ADC conversion is in progress and cleared to 0 by hardware when ADC is in idle. If a software start or hardware trigger is issued before previous conversion is completed, the ongoing one is aborted and a new conversion sequence is started. Software and hardware trigger must be coordinated correctly to avoid such conflict.

The block diagram of a 12-bit SAR ADC is shown below.

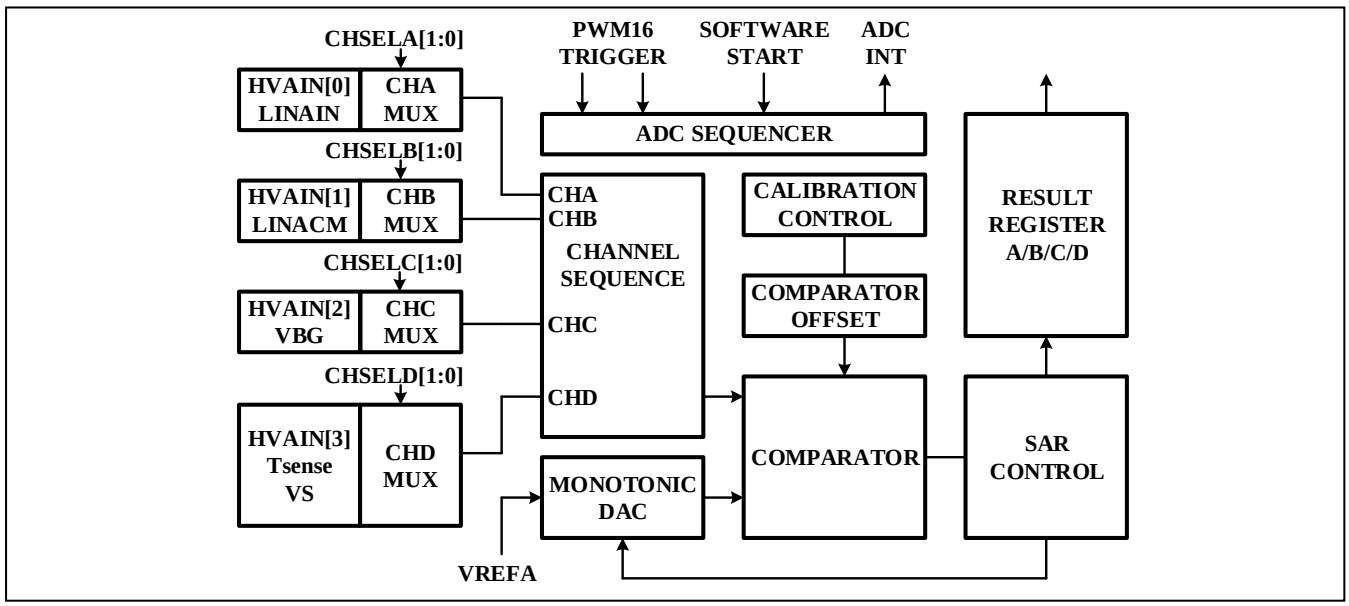


Figure 23 SAR ADC Block Diagram

ADCCFG1 ADC Configuration Register 1 RW

Bit	7	6	5	4	3	2	1	0
RD	ADCAZ	ADCEN	ADCIEN	ADCFM	AVG[1:0]		PRE[1:0]	
WR	ADCAZ	ADCEN	ADCIEN	ADCFM	AVG[1:0]		PRE[1:0]	

SFR Address: 0xB9 **Default: 0b00000000**

ADCAZ Auto Zero Reference Select
ADCAZ=0 use ADCIN for OPAMP auto offset cancellation
ADCAZ=1 use 1V for OPAMP auto offset cancellation

ADCEN ADC Enable bit
ADCEN=1 enables ADC.

ADCEN=0 puts ADC into power down mode.
When ADCEN is set from 0 to 1, the program needs to wait at least 2us to allow analog bias to stabilize to ensure ADC's proper functionality.

ADCIEN ADC Interrupt Enable bit
ADCINTE=1 enables the ADC Interrupt when conversion completes.
ADCINTE=0 disables the ADC Interrupt

ADCFM ADC Result Format Control bit
ADCFM = 1 sets ADC result as MSB justified. ADCAH contains the MSB bits of the result. ADCAL[7:4] contains LSB results and ADCAL[3:0] is filled with 0000.
ADCFM = 0 sets ADC result as LSB justified. ADCAH[7:4] is filled with 0000. ADCAH[3:0] contains MSB result. ADCAL contains the LSB results.

AVG[1:0] AVG[2:0] controls the hardware averaging logic of ADC readout. It is recommended the setting is changed only when ADC is stopped. If multiple channels are enabled, then each channel is averaged in sequence. The default is 00.

AVG[1:0]		ADC Result
0	0	No Average
0	1	2 Times Average
1	0	4 Times Average
1	1	8 Times Average

PRE[1:0] ADC Clock Divider Default is 11.

PRE[1:0]		ADC Clock
0	0	SYSCLK/32
0	1	SYSCLK/16
1	0	SYSCLK/8
1	1	SYSCLK/4

ADCCFG2 ADC Configuration Register2 RW

Bit	7	6	5	4	3	2	1	0
RD	CHSELA[1:0]		CHSELB[1:0]		CHSELC[1:0]		CHSELD[1:0]	
WR	CHSELA[1:0]		CHSELB[1:0]		CHSELC[1:0]		CHSELD[1:0]	

SFR Address: 0xA9 **Default: 0b00000000**

CHSELA[1:0] CH A Multiplexer Select.
CHSELA[1:0] = 00, HVAIN[0]
CHSELA[1:0] = 11, LINAIN

CHSELB[1:0] CH B Multiplexer Select.
CHSELB[1:0] = 00, HVAIN[1]
CHSELB[1:0] = 11, LINACM

CHSELC[1:0] CH C Multiplexer Select.
CHSELC[1:0] = 00, HVAIN[2]
CHSELC[1:0] = 11,VBG

CHSELD[1:0] CH D Multiplexer Select.
CHSELD[1:0] = 00, HVAIN[3]
CHSELD[1:0] = 01,Tsense
CHSELD[1:0] = 10, VS
CHSELD[1:0] = 11, VPTAT

ADCCFG3 ADC Configuration Register 3 RW

Bit	7	6	5	4	3	2	1	0
RD	CHENA	CHENB	CHENC	CHEND	FAULT	-	INTF	STAT
WR	CHENA	CHENB	CHENC	CHEND	CHOPDIS	AZDIS	INTF	CSTART

SFR Address: 0xCE **Default: 0b00000000**

ADCCHA ADCCHA=1 enables ADC Channel A for conversion cycle
ADCCHB ADCCHB=1 enables ADC Channel B for conversion cycle
ADCCHC ADCCHC=1 enables ADC Channel C for conversion cycle
ADCCHD ADCCHD=1 enables ADC Channel D for conversion cycle
CHOPDIS Comparator Chop Disable
CHOPDIS=1 disables comparator offset chop cancellation
AZDIS OPAMP Auto Offset Zero Disable
AZDIS=0 disables OPAMP offset zero mechanism
FAULT ADC Conversion Fault
FAULT is set to 1 by hardware when ADC conversion sequence error has occurred, for example, a new trigger is issued before previous conversion completes. FAULT is cleared to 0 when INTF is cleared to 0.
INTF ADC Interrupt Flag
INTF is set to 1 by hardware when conversion sequence is completed. INTF must be cleared by software by writing 0.
CSTART Software Start Conversion bit
Set this CSTART=1 to trigger an ADC conversion on selected channels. This bit is self-cleared when the conversion is done.
STAT ADC Status (Read Only)
STAT is set to 1 by hardware to indicate conversion is ongoing
STAT is cleared to 0 by hardware indicating ADC idle

ADCAH to ADCDH and ADCAL to ADCDL are the low and high byte result registers respectively, and are read-only. The format of the high byte and low byte depends on ADCFM setting.

ADCAL Channel A Result Register Low Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH A Result							
WR	-							

SFR Address: 0xBA **Default: 0bxxxxxxxx**

ADCAH Channel A Result Register High Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH A Result							
WR	-							

SFR Address: 0xBB **Default: 0bxxxxxxxx**

ADCBL Channel B Result Register Low Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH B Result							
WR	-							

SFR Address: 0xBC **Default: 0bxxxxxxxx**

ADCBH Channel B Result Register High Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH B Result							
WR	-							

SFR Address: 0xBD **Default: 0bxxxxxxxx**

ADCCL Channel C Result Register Low Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH C Result							
WR	-							

SFR Address: 0xBE **Default: 0bxxxxxxxx**

ADCCH Channel C Result Register High Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH C Result							
WR	-							

SFR Address: 0xBF **Default: 0bxxxxxxxx**

ADCDL Channel D Result Register Low Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH D Result							
WR	-							

SFR Address: 0xAA **Default: 0bxxxxxxxx**

ADCDH Channel D Result Register High Byte RO

Bit	7	6	5	4	3	2	1	0
RD	CH D Result							
WR	-							

SFR Address: 0xAB **Default: 0bxxxxxxxx**

LIN TRANSCEIVER

The LIN transceiver consists of two parts. One is for bus interface, which converts logic signaling to bus compatible levels. The second part is the bus voltage measurement unit for SNPD.

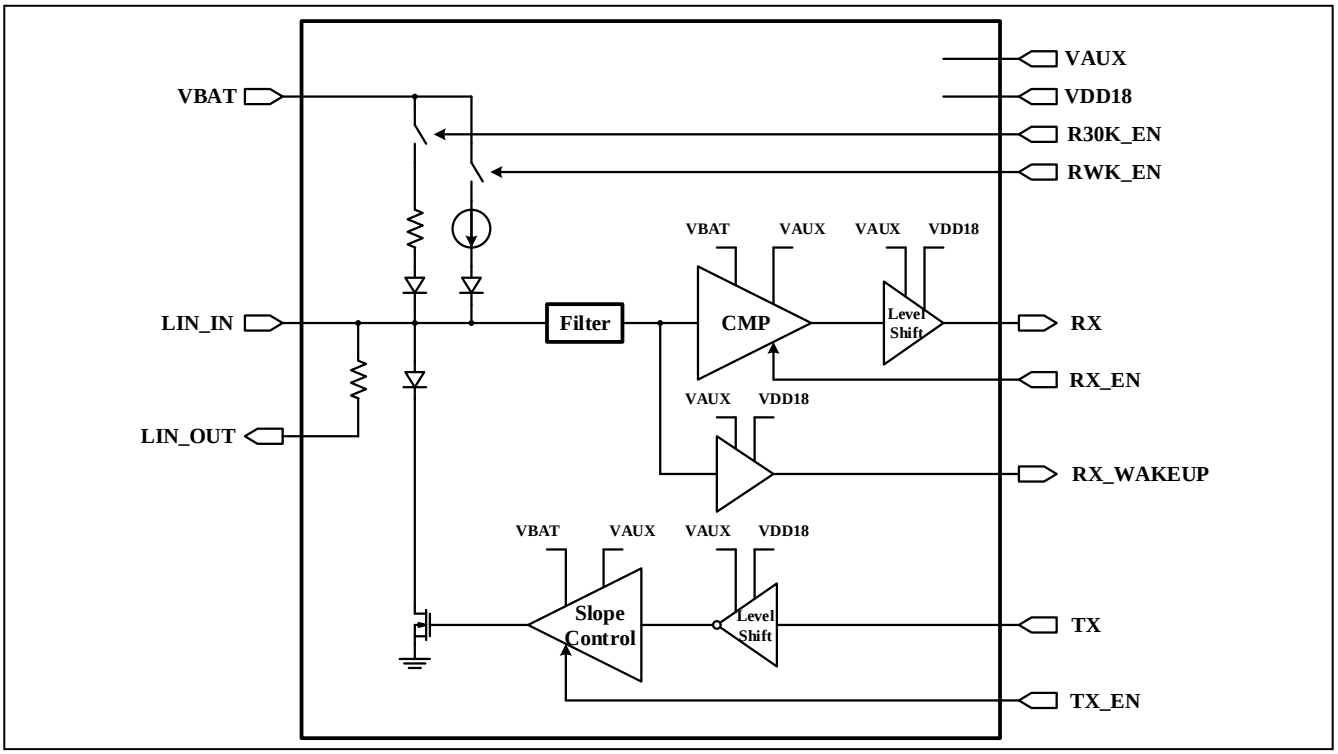


Figure 24 LIN Transceiver Block Diagram

XCVRCFG LIN Transceiver Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	-	-	P05EN	SNPD_IEN	RWK_EN	R30K_EN	RX_EN	TX_EN
WR	-	-	P05EN	SNPD_IEN	RWK_EN	R30K_EN	RX_EN	TX_EN

SFR Address: 0xA0AA **Default: 0b00000000**

P05EN Enable LININ/LINOUT as P05
P05EN=1 will use RX to be P05 input and use as Interrupt. And use P05 as TX output.
SNPD_IEN Enable 2mA for SNPD
RWK_EN Enable Weak Pull High Resistor
R30K_EN Enable 30K Pull High Resistor
RX_EN Enable LIN Received Function
TX_EN Enable LIN Transmit Function

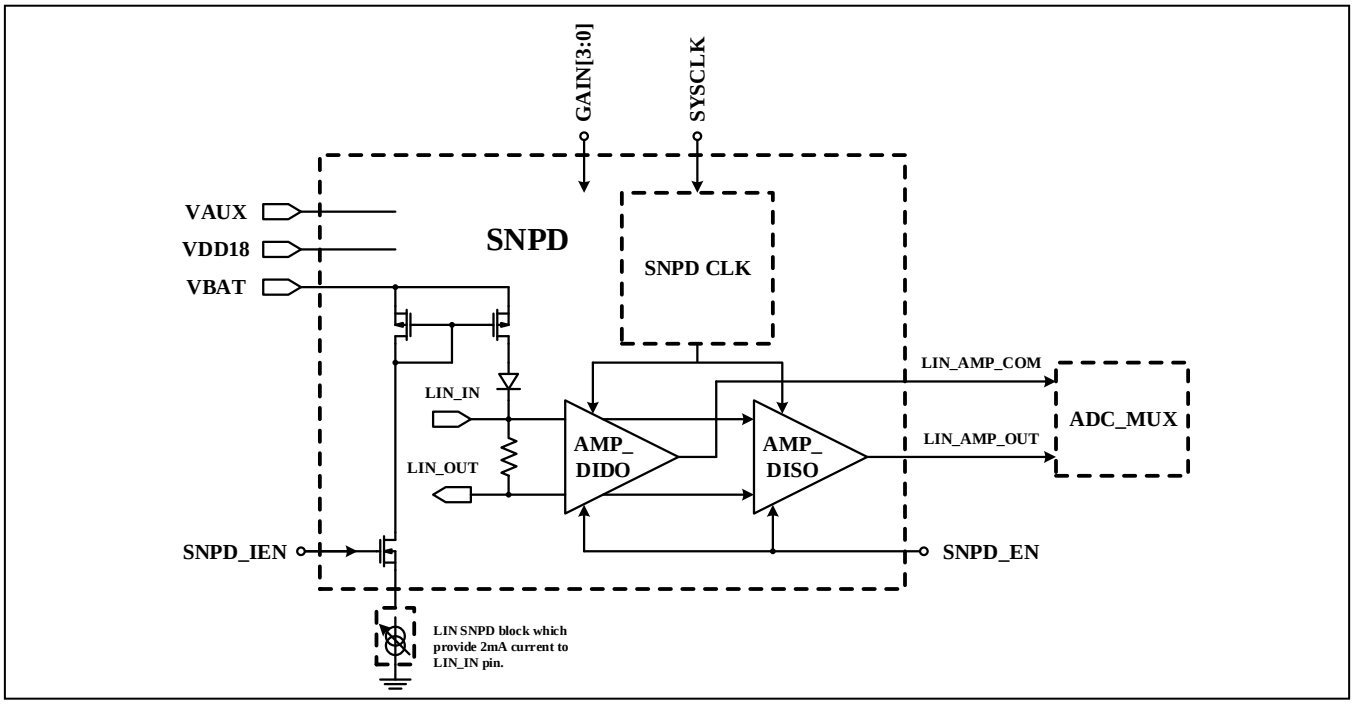


Figure 25 LIN SNPD Block Diagram

SNPDCFG LIN SNPD Configuration Register R/W

Bit	7	6	5	4	3	2	1	0
RD	SNPD_EN	-			-	-	GAIN[1:0]	
WR	SNPD_EN	-			-	-	GAIN[1:0]	

SFR Address: 0xA0AB **Default: 0b00000000**

SNPD_EN Enable differential amp of SNPD

GAIN[1:0] Gain of LIN SNPD Differential Amp

00: 40

01: 60

10: 80

11: 20

SNPDINT SNPD Interrupt configuration R/W

Bit	7	6	5	4	3	2	1	0
RD	SNPD_ST	-	-	RXF_EN	-	-	-	RXF_F
WR	SNPD_ST	-	-	RXF_EN	-	-	-	RXF_F

SFR Address: 0xA0AC **Default: 0b00000000**

SNPD_ST Start SNPD detection

SNPD_ST is set to 1 when receive LIN SNPD Start Command and clear to 0 when SNPD end, updated by software

RXF_EN RXD Falling Interrupt Enable

RXF_F RXD Falling Interrupt Flag

RXF_F is set to 1 by hardware and must be cleared by software

HVIO

There are four HVIO pins. Each serves two purposes, one as High Voltage GPIO with multi-functions and one as LED driver. HV[3:0] corresponds to P00 to P03 and LEDR/LEDG/LEDB/LEDW.

When function as GPIO, it can only have open-drain pull-down drive. Thus to keep the output high-impedance, a logic level 1 should be used. The input buffer needs to be enabled for taking input. The input buffer has a typical TTL threshold with hysteresis. There is an internal weak pull-up resistor can be switched on. There is also an attenuation network that can be switched on to provide HVAIN for ADC measurement.

When function as LED driver, it receive PWMH Controller PWM output and switches the programmable current sink. The FS[3:0] trim provides local correction of the LED current. There is an LED OPEN/SHORT detection circuit can be enabled for detecting LED faults. The sampling of the OPEN/SHORT status is done at PWM center. The fault status is then update every PWM cycle, and can be used to generate software Interrupt. Aging measurement involve two circuits, a preset precision 2mA current is used to drive the LED during proper PWM timing. And a differential sense amplifier amplifies the LED voltage drops and sends the output to ADC through HVAIN signal. Please note AINEN and DIFFEN cannot be on at the same time.

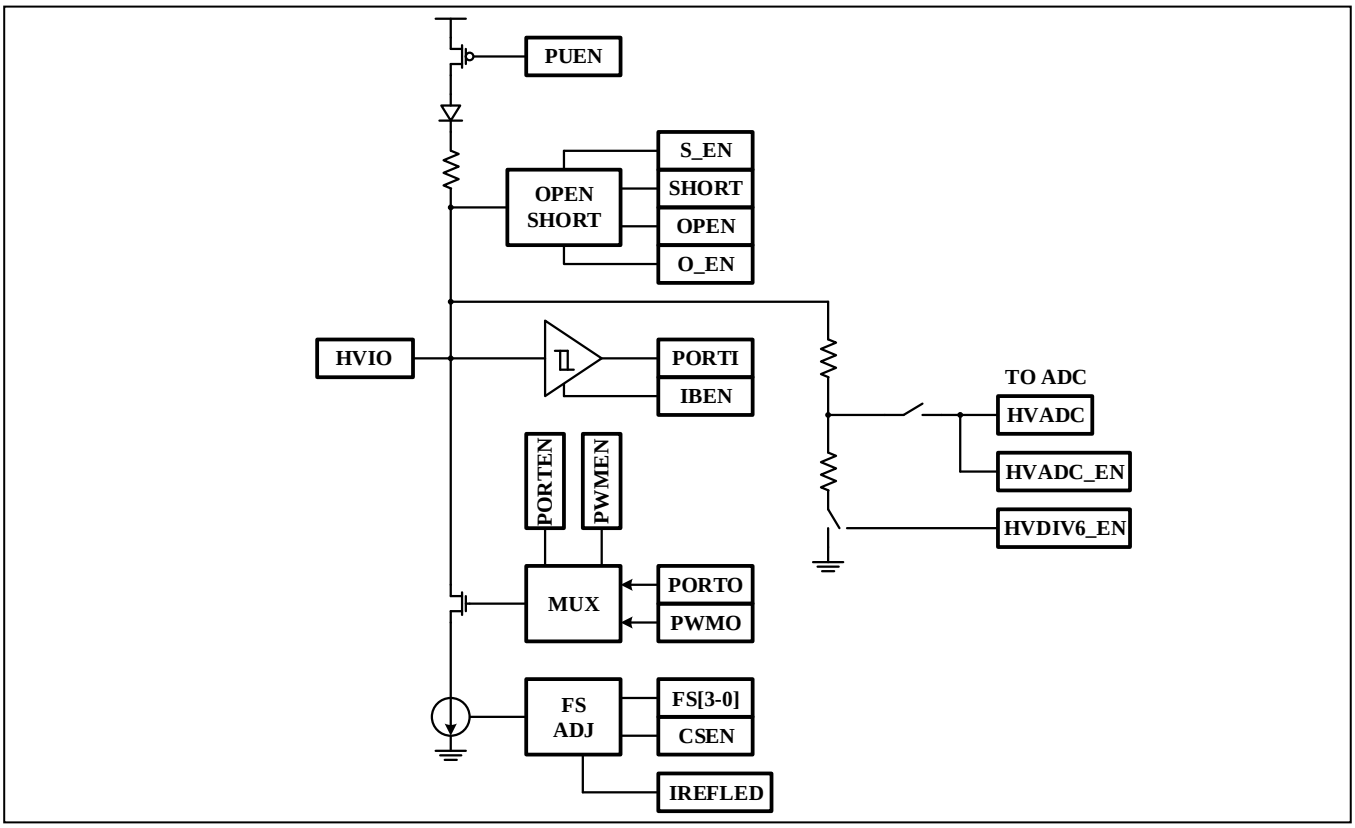


Figure 26 HVIO Block Diagram

HVIOCFA0 HV0 General Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	MSDAEN	HV0ADC_EN	CSNEN	HV0OD_EN	PWMHREN	HV0DIV6_EN	HV0IN_EN	HV0PUSEL
WR	MSDAEN	HV0ADC_EN	CSNEN	HV0OD_EN	PWMHREN	HV0DIV6_EN	HV0IN_EN	HV0PUSEL

SFR Address: 0xA040 **Default: 0b00000000**

MSDAEN Enable MSDA Function
HV0ADC_EN Enable HV0 ADC Function
CSNEN Enable SPI CSN Function
HV0ODEN Enable P0.0 Port Function
PWMHREN Enable PWMHR function
HV0DIV6_EN Analog Attenuation Circuit Enable
HV0DIV6_EN =1 turns on the 1/6 attenuation circuit and connect the attenuated input to ADC input.
HV0IN_EN HV0 Input Buffer Enable

HV0PUSEL Internal Pull-Up Select.

HVIOCFB0 HV0 LED Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV0IEN	RDIFF_EN	ENR_2mA	HV0_FS[4:0]				
WR	HV0IEN	RDIFF_EN	ENR_2mA	HV0_FS[4:0]				

SFR Address: 0xA041 **Default: 0b00000000**

HV0IEN Enable LED Current Sink Circuit for PWMHR Output Function
RDIFF_EN Enable Differential Sense Amplifier Circuit
ENR_2mA Enable 2mA Switch
HV0_FS[4:0] Local Full-Scale LED Current Sink Adjust

HVIOCFC0 HV0 LED Fault Status and Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV0_FILTER	HV0_FINTEN	HV0_O_EN	HV0_S_EN	HV0_OPEN	HV0_SHORT	HV0_OPENF	HV0_SHORTF
WR	HV0_FILTER	HV0_FINTEN	HV0_O_EN	HV0_S_EN	-	-	HV0_OPENF	HV0_SHORTF

SFR Address: 0xA042 **Default: 0b00000000**

HV0_FINTEN HV0 Open/Short Interrupt Enable
HV0_FILTER HV0 Digital Filter Enable
HV0_FILTER=1 use digital filter for assertion and de-assertion of the fault condition.
HV0_O_EN HV0 Open Detection Circuit Enable
If HV0_O_EN=0, then detected OPEN should always de-asserted.
HV0_S_EN HV0 Short Detection Circuit Enable
If HV0_S_EN=0, then detected SHORT should always de-asserted.
HV0_OPEN HV0 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.
HV0_SHORT HV0 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.
HV0_SHORTF HV0 Short Fault Interrupt and Latched Flag
HV0_SHORTF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV0_FINTEN=1. If HV0_FINTEN=0, HV0_SHORTF is the latched short fault status. HV0_SHORTF must be cleared by software.
HV0_OPENF HV0 Open Fault Flag
HV0_OPENF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV0_FINTEN=1. If HV0_FINTEN=0, HV0_OPENF is the latched short fault status. HV0_OPENF must be cleared by software.

HVIOCFD0 HV0 Differential Divider Select Register RW

Bit	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	HV0_DIFFDIV_SEL [1:0]	
WR	-	-	-	-	-	-	HV0_DIFFDIV_SEL [1:0]	

SFR Address: 0xA043 **Default: 0b00000000**

HV0_DIFFDIV_SEL [1:0]	Divider Gain
00	1/5
01	1/3
10	1/2
11	1

HVIOCFA1 HV1 General Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	MSCLEN	HV1ADC_EN	SCKEN	HV1OD_EN	PWMHGEN	HV1DIV6_EN	HV1IN_EN	HV1PUSEL
WR	MSCLEN	HV1ADC_EN	SCKEN	HV1OD_EN	PWMHGEN	HV1DIV6_EN	HV1IN_EN	HV1PUSEL

SFR Address: 0xA044 **Default: 0b00000000**

MSCLEN Enable MSCL Function
HV1ADC_EN Enable HV1 ADC Function
SCKEN Enable SPI SCK Function
HV1OD_EN Enable P0.1 Port Function
PWMHGEN Enable PWMHG function
HV1DIV6_EN Analog Attenuation Circuit Enable
HV1DIV6_EN =1 turns on the 1/6 attenuation circuit and connect the attenuated input to ADC input.
HV1IN_EN Input Buffer Enable
HV1PUSEL Internal Pull-Up Enable

HVIOCFB1 HV1 LED Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV1IEN	-	-	HV1_FS[4:0]				
WR	HV1IEN	-	-	HV1_FS[4:0]				

SFR Address: 0xA045 **Default: 0b00000000**

HV1IEN Enable LED Current Sink Circuit for PWMH Output Function
HV1_FS[4:0] Local Full-Scale LED Current Sink Adjust

HVIOCFC1 HV1 LED Fault Status and Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV1_FILTER	HV1_FINTEN	HV1_O_EN	HV1_S_EN	HV1_OPEN	HV1_SHORT	HV1_OPENF	HV1_SHORTF
WR	HV1_FILTER	HV1_FINTEN	HV1_O_EN	HV1_S_EN	-	-	HV1_OPENF	HV1_SHORTF

SFR Address: 0xA046 **Default: 0b00000000**

HV1_FINTEN HV1 Open/Short Interrupt Enable
HV1_FILTER HV1 Digital Filter Enable
HV1_FILTER=1 use digital filter for assertion and de-assertion of the fault condition.
HV1_O_EN HV1 Open Detection Circuit Enable
If HV1_O_EN=0, then detected HV1_OPEN should always de-asserted.
HV1_S_EN HV1 Short Detection Circuit Enable
If HV1_S_EN=0, then detected HV1_SHORT should always de-asserted.
HV1_OPEN HV1 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.

HV1_SHORT HV1 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.
HV1_SHORTF HV1 Short Fault Interrupt and Latched Flag
HV1_SHORTF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV1_FINTEN=1. If HV1_FINTEN=0, HV1_SHORTF is the latched short fault status. HV1_SHORTF must be cleared by software.
HV1_OPENF HV1 Open Fault Flag
HV1_OPENF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV1_FINTEN=1. If HV1_FINTEN=0, HV1_OPENF is the latched short fault status. HV1_OPENF must be cleared by software.

HVIOCFA2 HV2 General Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	MSDAEN	HV2ADC_EN	MISOEN	HV2OD_EN	PWMHBEN	HV2DIV6_EN	HV2IN_EN	HV2PUSEL
WR	MSDAEN	HV2ADC_EN	MISOEN	HV2OD_EN	PWMHBEN	HV2DIV6_EN	HV2IN_EN	HV2PUSEL

SFR Address: 0xA048 **Default: 0b00000000**

MSDAEN Enable MSDA Function
HV2ADC_EN Enable HV2 ADC Function
MISOEN Enable SPI MISO Function
HV2OD_EN Enable P0.2 Port Function
PWMHBEN Enable PWMHB function
HV2DIV6_EN Analog Attenuation Circuit Enable
HV2DIV6_EN =1 turns on the 1/6 attenuation circuit and connect the attenuated input to ADC input.
HV2IN_EN Input Buffer Enable
HV2PUSEL Internal Pull-Up Enable

HVIOCFB2 HV2 LED Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV2IEN	-	-	HV2_FS[4:0]				
WR	HV2IEN	-	-	HV2_FS[4:0]				

SFR Address: 0xA049 **Default: 0b00000000**

HV2IEN Enable LED Current Sink Circuit for PWMH Output Function
HV2_FS[4:0] Local Full-Scale LED Current Sink Adjust

HVIOCFC2 HV2 LED Fault Status and Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV2_FILTER	HV2_FINTEN	HV2_O_EN	HV2_S_EN	HV2_OPEN	HV2_SHORT	HV2_OPENF	HV2_SHORTF
WR	HV2_FILTER	HV2_FINTEN	HV2_O_EN	HV2_S_EN	-	-	HV2_OPENF	HV2_SHORTF

SFR Address: 0xA04A **Default: 0b00000000**

HV2_FINTEN HV2 Open/Short Interrupt Enable
HV2_FILTER HV2 Digital Filter Enable
HV2_FILTER=1 use digital filter for assertion and de-assertion of the fault condition.
HV2_O_EN HV2 Open Detection Circuit Enable
If HV2_O_EN=0, then detected HV2_OPEN should always de-asserted.
HV2_S_EN HV2 Short Detection Circuit Enable
If HV2_S_EN=0, then detected HV2_SHORT should always de-asserted.

HV2_OPEN HV2 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.
HV2_SHORT HV2 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.
HV2_SHORTF HV2 Short Fault Interrupt and Latched Flag
HV2_SHORTF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV2_FINTEN=1. If HV2_FINTEN=0, HV2_SHORTF is the latched short fault status. HV2_SHORTF must be cleared by software.
HV2_OPENF HV2 Open Fault Flag
HV2_OPENF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV2_FINTEN=1. If HV2_FINTEN=0, HV2_OPENF is the latched short fault status. HV2_OPENF must be cleared by software.

HVIOCFA3 HV3 General Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	MSCLEN	HV3ADC_EN	MOSIEN	HV3OD_EN	PWMHWEN-	HV3DIV6_EN	HV3IN_EN	HV3PUSEL
WR	MSCLEN	HV3ADC_EN	MOSIEN	HV3OD_EN	PWMHWEN-	HV3DIV6_EN	HV3IN_EN	HV3PUSEL

SFR Address: 0xA04C **Default: 0b00000000**

MSCLEN Enable MSCL Function
HV3ADC_EN Enable HV3 ADC Function
MOSIEN Enable SPI MOSI Function
HV3OD_EN Enable P0.3 Port Function
PWMHWEN Enable PWMHW function
HV3DIV6_EN Analog Attenuation Circuit Enable
HV3DIV6_EN =1 turns on the 1/6 attenuation circuit and connect the attenuated input to ADC input. AINEN and DIFFEN cannot be on at the same time.
HV3IN_EN Input Buffer Enable
HV3PUSEL Internal Pull-Up Enable

HVIOCFB3 HV3 LED Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV3IEN	-	ENW_1mA	HV3_FS[4:0]				
WR	HV3IEN	-	ENW_1mA	HV3_FS[4:0]				

SFR Address: 0xA04D **Default: 0b00000000**

HV3IEN Enable LED Current Sink Circuit for PWMH Output Function
ENW_1mA Enable 1mA Switch, high-side current for NTC resister
HV3_FS[4:0] Local Full-Scale LED Current Sink Adjust

HVIOCFC3 HV3 LED Fault Status and Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV3_FILTER	HV3_FINTEN	HV3_O_EN	HV3_S_EN	HV3_OPEN	HV3_SHORT	HV3_OPENF	HV3_SHORTF
WR	HV3_FILTER	HV3_FINTEN	HV3_O_EN	HV3_S_EN	-	-	HV3_OPENF	HV3_SHORTF

SFR Address: 0xA04E **Default: 0b00000000**

HV3_FINTEN HV3 Open/Short Interrupt Enable
HV3_FILTER HV3 Digital Filter Enable
HV3_FILTER=1 use digital filter for assertion and de-assertion of the fault condition.
HV3_O_EN HV3 Open Detection Circuit Enable

If HV3_O_EN=0, then detected HV3_OPEN should always de-asserted.

HV3_S_EN HV3 Short Detection Circuit Enable
If HV3_S_EN=0, then detected HV3_SHORT should always de-asserted.

HV3_OPEN HV3 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.

HV3_SHORT HV3 Real Time Open Status
This is updated every PWMH cycle and sampled at mid PWM.

HV3_SHORTF HV3 Short Fault Interrupt and Latched Flag
HV3_SHORTF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV3_FINTEN=1. If HV3_FINTEN=0, HV3_SHORTF is the latched short fault status. HV3_SHORTF must be cleared by software.

HV3_OPENF HV3 Open Fault Flag
HV3_OPENF is set to 1 by hardware to indicate a short fault caused the Interrupt if HV3_FINTEN=1. If HV3_FINTEN=0, HV3_OPENF is the latched short fault status. HV3_OPENF must be cleared by software.

HFFILTER HVIO FAULT Filter Configuration Register RW

Bit	7	6	5	4	3	2	1	0
RD	OPENFILT[3:0]				SHRTFILT[3:0]			
WR	OPENFILT[3:0]				SHRTFILT[3:0]			

SFR Address: 0xA04F **Default: 0b00000000**

OPENFILT[3:0] Open Fault Filter Setting
OPENFILT[3:0] set the number of PWM cycles for fault condition to be asserted. It is based on continuous increment/decrement filtering.

SHRTFILT[3:0] Short Fault Filter Setting
SHRTFILT[3:0] set the number of PWM cycles for fault condition to be asserted. It is based on continuous increment/decrement filtering.

PIN INTERRUPT AND WAKE UP

Every HVIO can be used as external Interrupt and wake up source. These are defined by individual HVIO separately.

HVIOINT0 HV0 Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV0_WKEN	HV0_PINTEN	HV0_REN	HV0_FEN	HV0_WKF	HV0_INTF	HV0_RF	HV0_FF
WR	HV0_WKEN	HV0_PINTEN	HV0_REN	HV0_FEN	HV0_WKF	HV0_INTF	HV0_RF	HV0_FF

SFR Address: 0xA050 **Default: 0b00000000**

HV0_WKEN HV0 Enable as Wake Up Source

HV0_PINTEN HV0 External Pin Interrupt Enable
Enable pin Interrupt. HVIO uses PINT0.

HV0_REN HV0 Rising Edge Enable

HV0_FEN HV0 Falling Edge Enable

HV0_WKF HV0 Wake Up Flag
HV0_WKF is set by hardware if HV0_WKEN=1 and a wakeup event occurred. It must be cleared by software.

HV0_INTF HV0 Interrupt Flag
HV0_INTF is set by hardware if HV0_PINTEN=1 and an Interrupt event occurred. It must be cleared by software.

HV0_RF HV0 Rising Edge Flag
HV0_RF is set by hardware if HV0_REN=1 and a rising edge occurred. It must be cleared by software.

HV0_FF HV0 Falling Edge Flag

HV0_FF is set by hardware if HV0_FEN=1 and a falling edge occurred. It must be cleared by software.

HVIOINT1 HV1 Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV1_WKEN	HV1_PINTEN	HV1_REN	HV1_FEN	HV1_WKF	HV1_INTF	HV1_RF	HV1_FF
WR	HV1_WKEN	HV1_PINTEN	HV1_REN	HV1_FEN	HV1_WKF	HV1_INTF	HV1_RF	HV1_FF

SFR Address: 0xA051 **Default: 0b00000000**

HV1_WKEN HV1Enable as Wake Up Source

HV1_PINTEN HV1External Pin Interrupt Enable
Enable pin Interrupt. HVIO uses PINT0.

HV1_REN HV1Rising Edge Enable

HV1_FEN HV1Falling Edge Enable

HV1_WKF HV1Wake Up Flag
HV1_WKF is set by hardware if HV1_WKEN=1 and a wakeup event occurred. It must be cleared by software.

HV1_INTF HV1Interrupt Flag
HV1_INTF is set by hardware if HV1_PINTEN=1 and an Interrupt event occurred. It must be cleared by software.

HV1_RF HV1Rising Edge Flag
HV1_RF is set by hardware if HV1_REN=1 and a rising edge occurred. It must be cleared by software.

HV1_FF HV1Falling Edge Flag
HV1_FF is set by hardware if HV1_FEN=1 and a falling edge occurred. It must be cleared by software.

HVIOINT2 HV2 Interrupt Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV2_WKEN	HV2_PINTEN	HV2_REN	HV2_FEN	HV2_WKF	HV2_INTF	HV2_RF	HV2_FF
WR	HV2_WKEN	HV2_PINTEN	HV2_REN	HV2_FEN	HV2_WKF	HV2_INTF	HV2_RF	HV2_FF

SFR Address: 0xA052 **Default: 0b00000000**

HV2_WKEN HV2 Enable as Wake Up Source

HV2_PINTEN HV2 External Pin Interrupt Enable
Enable pin Interrupt. HVIO uses PINT0.

HV2_REN HV2 Rising Edge Enable

HV2_FEN HV2 Falling Edge Enable

HV2_WKF HV2 Wake Up Flag
HV2_WKF is set by hardware if HV2_WKEN=1 and a wakeup event occurred. It must be cleared by software.

HV2_INTF HV2 Interrupt Flag
HV2_INTF is set by hardware if HV2_PINTEN=1 and an Interrupt event occurred. It must be cleared by software.

HV2_RF HV2 Rising Edge Flag
HV2_RF is set by hardware if HV2_REN=1 and a rising edge occurred. It must be cleared by software.

HV2_FF HV2 Falling Edge Flag
HV2_FF is set by hardware if HV2_FEN=1 and a falling edge occurred. It must be cleared by software.

HVIOINT3 HV3 Interrupt Register RW

Bit	7	6	5	**4**	3	2	1	0
RD	HV3_WKEN	HV3_PINTEN	HV3_REN	HV3_FEN	HV3_WKF	HV3_INTF	HV3_RF	HV3_FF
WR	HV3_WKEN	HV3_PINTEN	HV3_REN	HV3_FEN	HV3_WKF	HV3_INTF	HV3_RF	HV3_FF

SFR Address: 0xA053 **Default: 0b00000000**

HV3_WKEN HV3 Enable as Wake Up Source

HV3_PINTEN HV3 External Pin Interrupt Enable
Enable pin Interrupt. HVIO uses PINT0.

HV3_REN HV3 Rising Edge Enable

HV3_FEN HV3 Falling Edge Enable

HV3_WKF HV3 Wake Up Flag
HV3_WKF is set by hardware if HV3_WKEN=1 and a wakeup event occurred. It must be cleared by software.

HV3_INTF HV3 Interrupt Flag
HV3_INTF is set by hardware if HV3_PINTEN=1 and an Interrupt event occurred. It must be cleared by software.

HV3_RF HV3 Rising Edge Flag
HV3_RF is set by hardware if HV3_REN=1 and a rising edge occurred. It must be cleared by software.

HV3_FF HV3 Falling Edge Flag
HV3_FF is set by hardware if HV3_FEN=1 and a falling edge occurred. It must be cleared by software.

HVIODBN0 HV0 De-Bounce Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV0_REDBM	HV0_FEDBM	HV0_DBEN	-	-	HV0_DBWID[2:0]		
WR	HV0_REDBM	HV0_FEDBM	HV0_DBEN	-	-	HV0_DBWID[2:0]		

SFR Address: 0xA058 **Default: 0b00000000**

HV0_REDBM HV0 Rising Edge De-Bounce Method, 1: Immediate 0: Delay

HV0_FEDBM HV0 Falling Edge De-Bounce Method, 1: Immediate 0: Delay

HV0_DBEN HV0 De-Bounce enable

HV0_DBWID[2:0] HV0 De-Bounce Width Setting, De-bounce time is derived from SIOC so these are approximations.
000 = 1.33msec
001 = 2.66msec
010 = 5.33msec
011 = 10.6msec
100 = 21.3msec
101 = 42.6msec
110 = 85.3msec
111 = 170.6msec

HVIODBN1 HV1 De-Bounce Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV1_REDBM	HV1_FEDBM	HV1_DBEN	-	-	HV1_DBWID[2:0]		
WR	HV1_REDBM	HV1_FEDBM	HV1_DBEN	-	-	HV1_DBWID[2:0]		

SFR Address: 0xA059 **Default: 0b00000000**

HV1_REDBM HV1 Rising Edge De-Bounce Method, 1: Immediate 0: Delay

HV1_FEDBM HV1 Falling Edge De-Bounce Method, 1: Immediate 0: Delay

HV1_DBEN HV1 De-Bounce enable

HV1_DBWID[2:0] HV1 De-Bounce Width Setting, De-bounce time is derived from SIOC so these are approximations.
000 = 1.33msec
001 = 2.66msec
010 = 5.33msec
011 = 10.6msec
100 = 21.3msec
101 = 42.6msec
110 = 85.3msec
111 = 170.6msec

HVIODBN2 HV2 De-Bounce Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV2_REDBM	HV2_FEDBM	HV2_DBEN	-	-	HV2_DBWID[2:0]		
WR	HV2_REDBM	HV2_FEDBM	HV2_DBEN	-	-	HV2_DBWID[2:0]		

SFR Address: 0xA05A **Default: 0b00000000**

HV2_REDBM HV2 Rising Edge De-Bounce Method, 1: Immediate 0: Delay
HV2_FEDBM HV2 Falling Edge De-Bounce Method, 1: Immediate 0: Delay
HV2_DBEN HV2 De-Bounce enable
HV2_DBWID[2:0] HV2 De-Bounce Width Setting, De-bounce time is derived from SIOC so these are approximations.
000 = 1.33msec
001 = 2.66msec
010 = 5.33msec
011 = 10.6msec
100 = 21.3msec
101 = 42.6msec
110 = 85.3msec
111 = 170.6msec

HVIODBN3 HV3 De-Bounce Register RW

Bit	7	6	5	4	3	2	1	0
RD	HV3_REDBM	HV3_FEDBM	HV3_DBEN	-	-	HV3_DBWID[2:0]		
WR	HV3_REDBM	HV3_FEDBM	HV3_DBEN	-	-	HV3_DBWID[2:0]		

SFR Address: 0xA05B **Default: 0b00000000**

HV3_REDBM HV3 Rising Edge De-Bounce Method, 1: Immediate 0: Delay
HV3_FEDBM HV3 Falling Edge De-Bounce Method, 1: Immediate 0: Delay
HV3_DBEN HV3 De-Bounce enable
HV3_DBWID[2:0] HV3 De-Bounce Width Setting, De-bounce time is derived from SIOC so these are approximations.
000 = 1.33msec
001 = 2.66msec
010 = 5.33msec
011 = 10.6msec
100 = 21.3msec
101 = 42.6msec
110 = 85.3msec
111 = 170.6msec

ECC

Two Hamming Code (8,4) plus 1-bit parity engine to achieve enhanced two error bits detection and correction.

Bit position

position	8	7	6	5	4	3	2	1
name	P8	D7	D6	D5	P4	D3	P2	P1

Encode:

P1 = D3 ^ D5 ^ D7
P2 = D3 ^ D6 ^ D7
P4 = D5 ^ D6 ^ D7
P8 = P1^P2^P4 ^ D7^D6 ^D5^D3
{ D7 ,D6 , D5, D3 } = Data[3:0]
ECC[3:0] = { P8,P4,P2,P1 }

Decode:

C1 = P1 ^D3 ^ D5 ^ D7
C2 = P2 ^D3 ^ D6 ^ D7
C4= P4 ^D5 ^ D6 ^ D7
R[2:0] = { C4,C2,C1}
Parity= P1^P2^P4^P8^ D7^D6 ^D5^D3
Data[3:0] = { D7 ,D6 , D5, D3 }
{ P8,P4,P2,P1 } = ECC[3:0]

Condition	Comment	Data[3:0]
R=0 and parity=0	No error occurred	No change
R > 0 and parity=1	A single error occurred that can be corrected	Inversed bit D(R)
R > 0 and parity=0	A double error occurred that is detected but cannot be corrected	No change
R=0 and parity=1	An error occurred in the *P*8 bit	No change

Flash Data format

DOUT[15:12]	DOUT[11:8]	DOUT[7:4]	DOUT[3:0]
HighECC[3:0]	LowECC[3:0]	HighData[3:0]	LowData[3:0]

ECCCFG ECC Configuration Register RW

	7	6	5	4	3	2	1	0
RD	RSTEN	PECCEN	ECCCUE	ECCCRE	ECCCU	ECCCR	ECCCUF	ECCCRF
WR	RSTEN	PECCEN	ECCCUE	ECCCRE	ECCCU	ECCCR	ECCCUF	ECCCRF

SFR Address: 0xA026 **Default: 0b00000000**

RSTEN Enable two-bit Errors reset

PECCEN Enable ECC function for program read

ECCCUE Enable Uncorrectable error Interrupt

ECCCRE Enable correctable error Interrupt

ECCCR ECC Error Correction Bit
ECCCR is set to 1 by ECC hardware logic if one or more than one correctable error were detected during the just completed operation. ECCCR is cleared by software.

ECCCU ECC Error Uncorrectable Bit
ECCCU is set to 1 by ECC hardware logic if one or more than one un-correctable error were detected during the just completed operation. ECCCU is cleared by software.

ECCCRF ECC correctable error Interrupt Bit
ECCCRF is set to 1 by ECC hardware logic. It must be cleared by software.

ECCCUF ECC Error Uncorrectable Interrupt Bit
ECCCUF is set to 1 by ECC hardware logic. It must be cleared by software.

ECCSTA ECC Decode Statue Register RW

	7	6	5	4	3	2	1	0
RD	ECCRST	FECCEN	PGMCU	PGMCR	FLSHHCU	FLSHHCR	FLSHLCU	FLSHLCR
WR	ECCRST	FECCEN	PGMCU	PGMCR	FLSHHCU	FLSHHCR	FLSHLCU	FLSHLCR

SFR Address: 0xA025 **Default: 0b00000000**

FLSHLCR ECC Error Correction Bit
FLSHLCR is set to 1 by ECC hardware logic if one correctable error were detected in low nibble byte during the ISP operation. ISPLNCR is cleared by software.

FLSHLCU ECC Error Uncorrectable Bit
FLSHLCU is set to 1 by ECC hardware logic if one or more than one un-correctable error were detected in low nibble byte during the ISP operation. ISPLNCU is cleared by software.

FLSHHCR ECC Error Correction Bit
FLSHHCR is set to 1 by ECC hardware logic if one correctable error were detected in high nibble byte during the ISP operation. ISPHNCR is cleared by software.

FLSHHCU ECC Error Uncorrectable Bit
FLSHHCU is set to 1 by ECC hardware logic if one or more than one un-correctable error were detected in high nibble byte during the ISP operation. ISPHNCU is cleared by software.

PGMCR ECC Error Correction Bit
PGMCR is set to 1 by ECC hardware logic if one correctable error were detected during the MCU read operation. PGMCR is cleared by software.

PGMCU ECC Error Uncorrectable Bit
PGMCU is set to 1 by ECC hardware logic if one or more than one un-correctable error were detected during the MCU read operation. PGMCU is cleared by software.

FECCEN Enable ECC function for Flash Command Read

ECCRST ECC reset Bit
ECCRST is set to 1 by ECC hardware logic if ECC reset execution. ECCRST is cleared by power on reset or software. Software/WDT reset does not clear this.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (1):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (1)$$

So, $P_{D(MAX)} = \frac{150°C - 25°C}{44°C/W} \approx 2.84W$

Figure 27, shows the power derating of the IS32LT3183A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

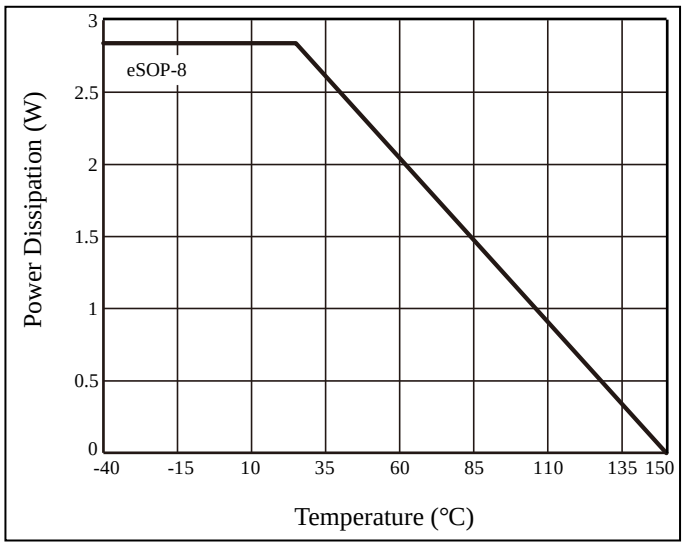


Figure 27 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

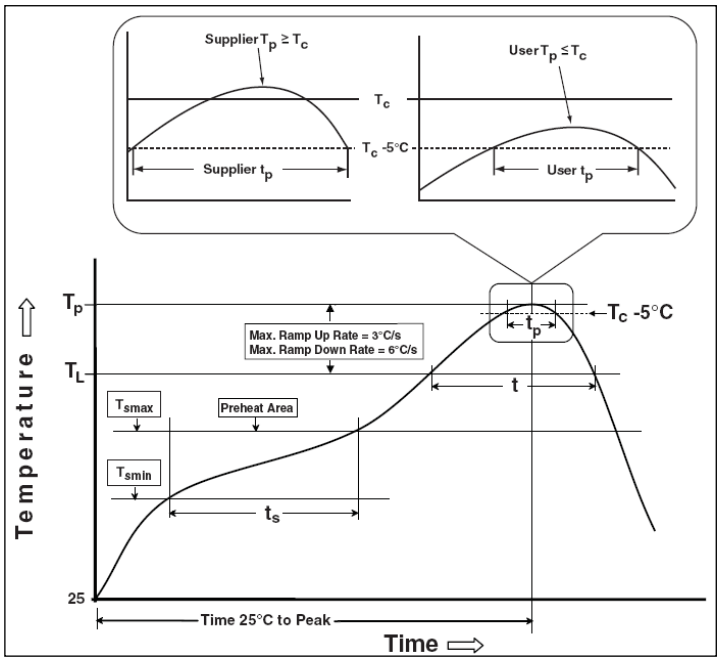
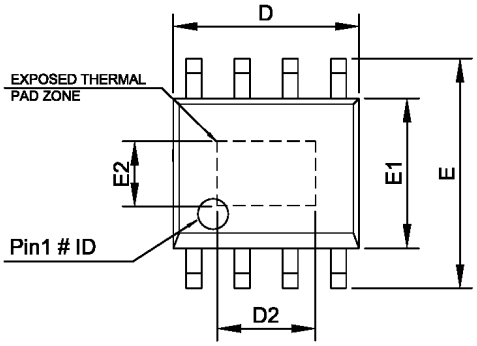
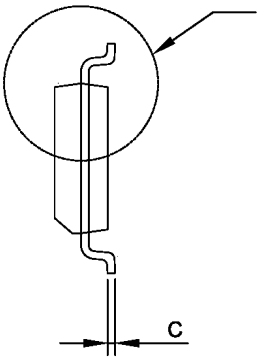


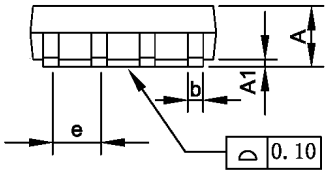
Figure 28 Classification Profile

PACKAGE INFORMATION

SOP-8-EP

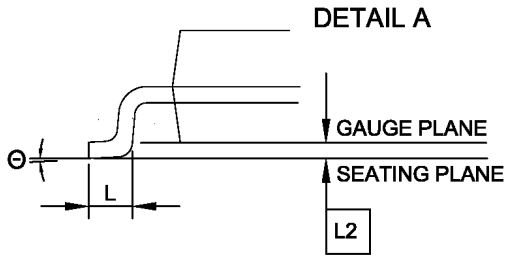






SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.70
A1	–	–	0.15
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
D	4.70	4.90	5.10
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.10	–	0.25
D2	1.50	–	–
E2	1.00	–	–

233-570-289 Rev. B

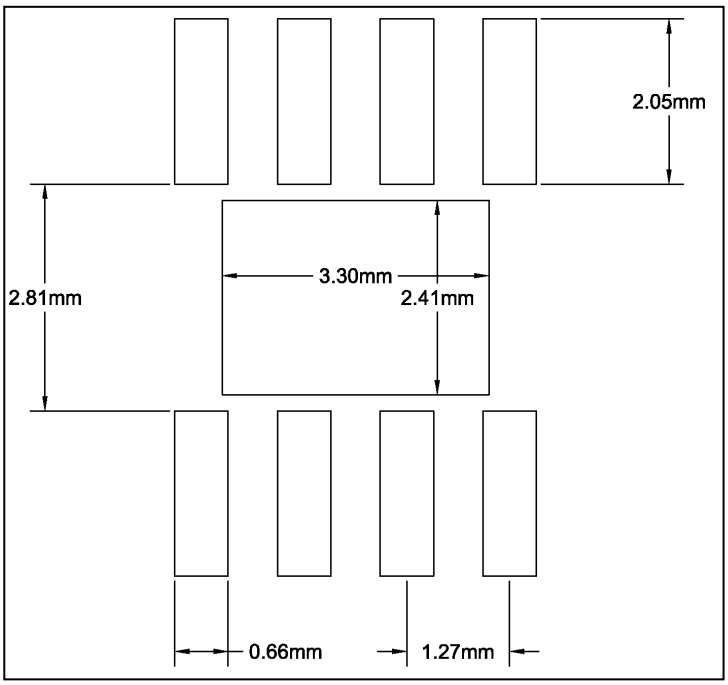


NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

SOP-8-EP



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Final version	2022.12.13

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