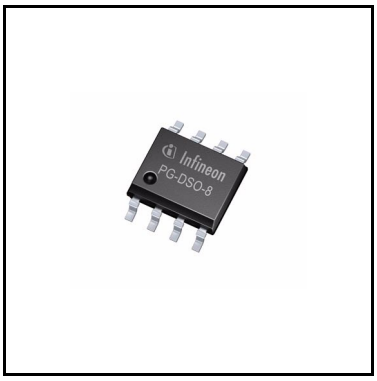
TLE9350BVSJ

High speed CAN FD transceiver



Features

- Fully compliant to ISO 11898-2:2016 and SAE J2284-4/-5
- Loop delay symmetry for CAN FD data frames up to 5 Mbit/s
- Very low electromagnetic emission (EME) allows the use without additional common mode choke
- V_{IO} input for voltage adaption to the microcontroller interface (3.3 V or 5 V)
- Excellent ESD robustness
- TxD timeout function
- Very low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients according to ISO 7637 and SAE J2962-2
- Power-save mode
- Green Product (RoHS compliant)

Potential applications

- Engine control units (ECU)
- Electric power steering
- Transmission control units (TCUs)
- Chassis control modules

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE9350BVSJ is a high speed CAN transceiver, used in HS CAN systems for automotive applications as well as for industrial applications. It is designed to fulfill the requirements of ISO 11898-2:2016 physical layer specification as well as SAE J1939 and SAE J2284.

The TLE9350BVSJ is available in a RoHS compliant, halogen free PG-DSO-8 package.

As an interface between the physical bus layer and the HS CAN protocol controller, the TLE9350BVSJ is designed to protect the microcontroller against interferences generated inside the network. A very high ESD robustness and the optimized RF immunity allows the use in automotive applications without additional protection devices, such as suppressor diodes or common mode chokes.

Based on the high symmetry of the CANH and CANL output signals, the TLE9350BVSJ provides a very low level of electromagnetic emission (EME) within a wide frequency range. The TLE9350BVSJ fulfills even stringent EMC test limits without an additional external circuit, such as a common mode choke.

The optimized transmitter symmetry combined with the optimized delay symmetry of the receiver enables the TLE9350BVSJ to support CAN FD data frames. The device supports data transmission rates up to 5 Mbit/s, depending on the size of the network and the inherent parasitic effects.

Fail-safe features, such as overtemperature protection, output current limitation or the TxD timeout feature are designed to protect the TLE9350BVSJ and the external circuitry from irreparable damage.

Type	Package	Marking
TLE9350BVSJ	PG-DSO-8	9350BV

Table of contents

1 Block diagram

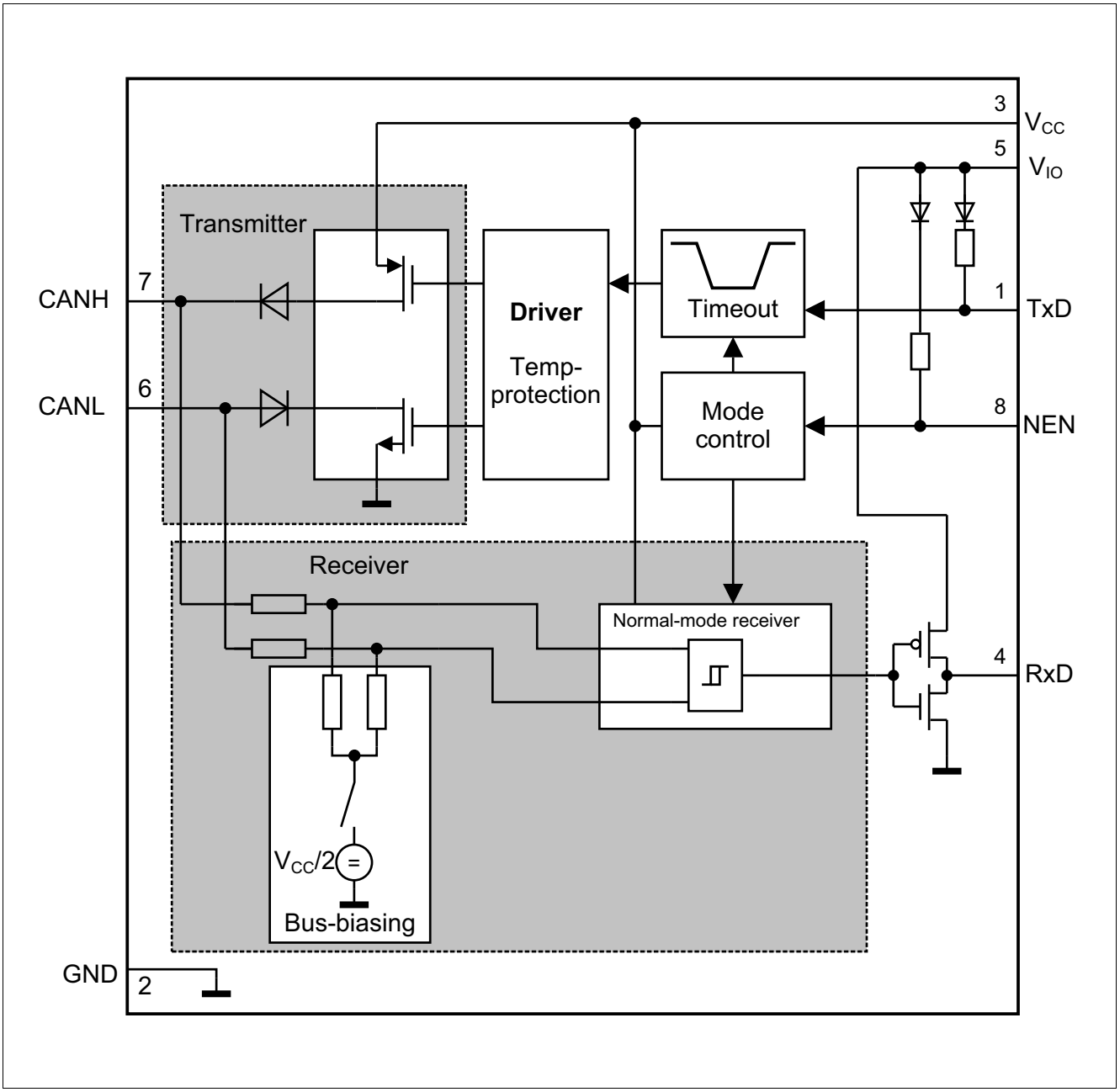


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

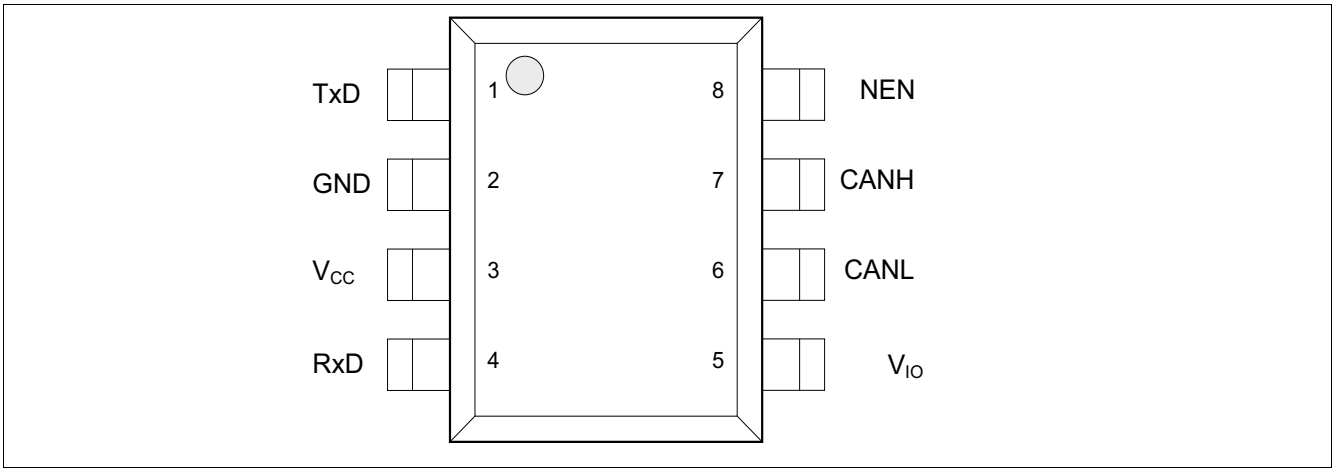


Figure 2 Pin configuration

2.2 Pin definitions

Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	**Transmit data input;** Internal pull-up to V_{IO}, "low" for dominant state.
2	GND	**Ground**
3	V_{CC}	**Transmitter supply voltage;** A decoupling capacitor of 1 µF to GND is recommended, V_{CC} can be turned off in power-save mode.
4	RxD	**Receive data output;** "Low" in dominant state.
5	V_{IO}	**Digital supply voltage input;** Adapts the logical input voltage level and output voltage level of the transceiver to the voltage level of the microcontroller supply, A 100 nF decoupling capacitor to GND is recommended.
6	CANL	**CAN bus low level I/O;** Bus level on the CANL input/output.
7	CANH	**CAN bus high level I/O;** Bus level on the CANH input/output.
8	NEN	**Not enable input;** Internal pull-up to V_{IO}, "low" for normal-operating mode.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_7.1.1
Digital supply voltage	V_{IO}	-0.3	–	6.0	V	–	P_7.1.2
CANH and CANL DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_7.1.3
Differential voltage between CANH and CANL	V_{CAN_Diff}	-40	–	40	V	–	P_7.1.4
Voltage at the digital input pins: NEN, TxD	V_{MAX_IO}	-0.3	–	6.0	V	–	P_7.1.5
Voltage at the digital output pin: RxD	V_{MAX_RxD}	-0.3	–	V_{IO} +0.3	V	–	P_7.1.9
Currents							
RxD output current	I_{RxD}	-5	–	5	mA	–	P_7.1.6
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_7.1.7
Storage temperature	T_S	-55	–	150	°C	–	P_7.1.8
ESD immunity							
ESD robustness at CANH, CANL versus GND	$V_{ESD\_HBM\_CAN}$	-10	–	10	kV	HBM; (100 pF via 1.5 kΩ)[2)]	P_7.1.10
ESD robustnessat all other pins	$V_{ESD\_HBM\_ALL}$	-2	–	2	kV	HBM; (100 pF via 1.5 kΩ)[2)]	P_7.1.11
ESD robustness at corner pins	$V_{ESD\_CDM\_CP}$	-750	–	750	V	CDM[3)]	P_7.1.14
ESD immunity at any other pins	V_{ESD_CDM}	-500	–	500	V	CDM[3)]	P_7.1.12

1) Not subject to production test, specified by design.
2) Human body model (HBM) robustness according to AE - Q100-002.
3) Charge device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard.

Note: Latchup robustness: class II according to AEC - Q100-04.

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Transmitter supply voltage	V_{CC}	4.5	–	5.5	V	–	P_7.2.1
Digital supply voltage	V_{IO}	3.0	–	5.5	V	–	P_7.2.2
Thermal parameters							
Junction temperature	T_j	-40	–	150	°C	1)	P_7.2.3

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance							
Junction to ambient PG-DSO-8	R_{thJA_DSO8}	–	120	–	K/W	2)	P_7.3.2
Thermal shutdown (junction temperature)							
Thermal shutdown temperature, rising	T_{JSD}	170	180	190	°C	temperature falling: minimum 150°C	P_7.3.3
Thermal shutdown hysteresis	ΔT	5	10	20	K	-	P_7.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to JEDEC JESD51-2,-7 at natural convection on FR4 2s2p board. The product was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two inner copper layers (2 × 70µm Cu, 2 × 35µm Cu).

4 High speed CAN functional description

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. ISO 11898 describes the use of the Controller Area Network (CAN) within road vehicles. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other CAN nodes available within the network. The physical layer specification of a CAN bus system includes all electrical specifications of a CAN. The CAN transceiver is part of the physical layer specification.

4.1 High speed CAN physical layer

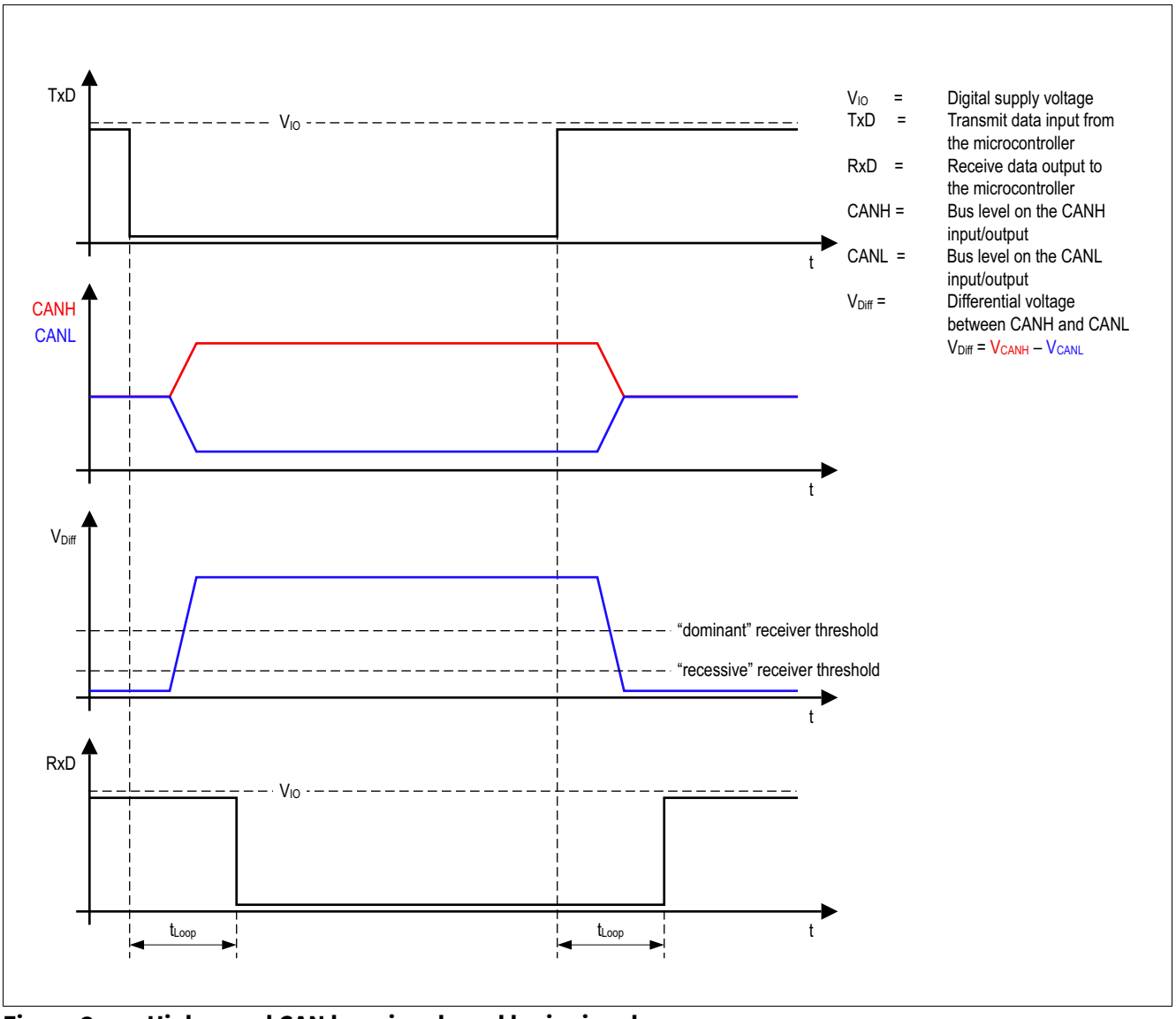


Figure 3 High speed CAN bus signals and logic signals

The TLE9350BVSJ operates as an interface between the CAN controller and the physical bus medium. A HS CAN is a two wire differential network which allows data transmission rates up to 5 Mbit/s. The characteristics for a HS CAN are the two signal states on the CAN bus: dominant and recessive (see **Figure 3**).

The CANH and CANL pins are the interface to the CAN bus and both pins operate as an input and output simultaneously. The RxD and TxD pins are the interface to the microcontroller. The pin TxD is the serial data input from the CAN controller, the RxD pin is the serial data output to the CAN controller. As shown in **Figure 1**, the TLE9350BVSJ includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time. The TLE9350BVSJ converts the serial data stream which is available on the transmit data input TxD, into a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the TLE9350BVSJ monitors the data on the CAN bus and converts them to a serial, single-ended signal on the RxD output pin. A "low" signal on the TxD pin creates a dominant signal on the CAN bus, followed by a logical "low" signal on the RxD pin (see **Figure 3**). The feature of broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within CAN.

ISO 11898-2:2016 specifies the voltage levels for HS CAN transceivers. Whether a data bit is dominant or recessive depends on the voltage difference between the CANH and CANL pins ($V_{Diff} = V_{CANH} - V_{CANL}$).

To transmit a dominant signal to the CAN bus the amplitude of the differential signal V_{Diff} is higher than or equal to 1.5 V. To receive a recessive signal from the CAN bus the amplitude of the differential V_{Diff} is lower than or equal to 0.5 V.

In partially-supplied high speed CAN network, the bus nodes of one common network have different power supply conditions. Some nodes are connected to the power supply, while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus subscriber is supplied or not, each subscriber connected to the common bus media must not interfere with the communication. The TLE9350BVSJ is designed to support partially-supplied networks. In power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

For permanently supplied ECUs, the HS CAN transceiver TLE9350BVSJ provides a power-save mode. In power-save mode, the power consumption of the TLE9350BVSJ is optimized to a minimum

The voltage level on the digital input TxD and the digital output RxD is determined by the power supply level at the V_{IO} pin. Depending on the voltage level at the V_{IO} pin, the signal levels on the logic pins (STB, TxD and RxD) are compatible with microcontrollers having a 5 V or 3.3 V I/O supply. Usually the digital power supply V_{IO} of the transceiver is connected to the I/O power supply of the microcontroller (see **Figure 12**).

5 Modes of operation

The TLE9350BVSJ supports the following modes of operation):

- Normal-operating mode
- Power-save mode

The mode selection input pin NEN triggers mode changes. Undervoltage on V_{CC} disables the transmitter output stage. An undervoltage event on the digital supply V_{IO} powers down the device.

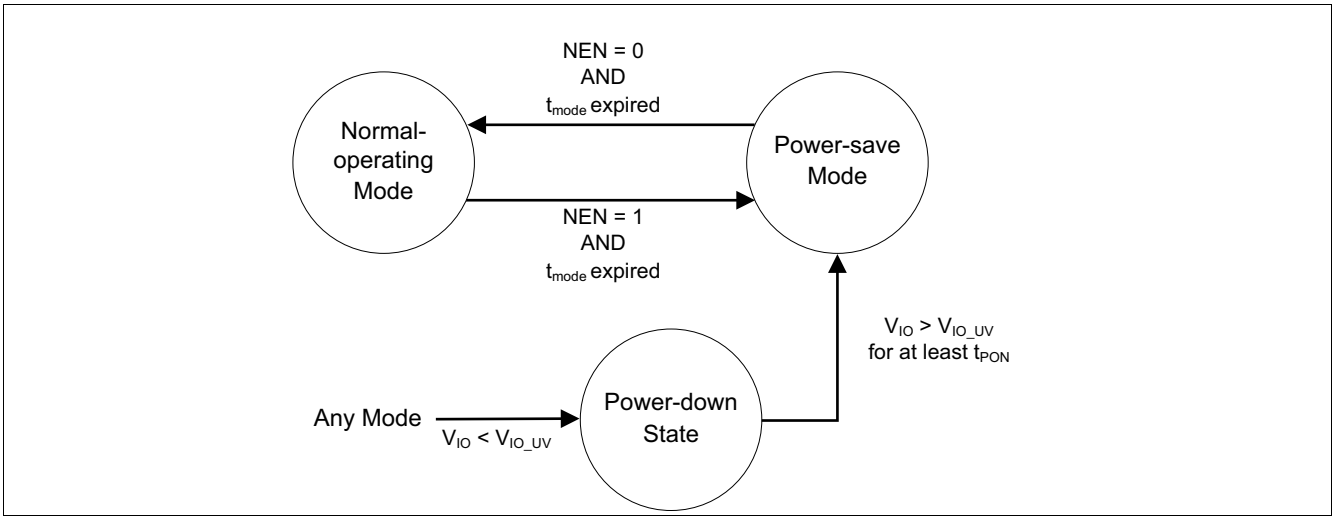


Figure 4 Mode state diagram

5.1 Normal-operating mode

In normal-operating mode all functions of the device are available and the device is fully functional. Data can be received from the HS CAN bus as well as transmitted to the HS CAN bus.

- The transmitter is enabled and drives the serial data stream on the TxD input pin to the bus pins CANH and CANL.
- The receiver is enabled and converts the signal from the bus to a serial data stream on the RxD output pin.
- The bus biasing is connected to $V_{CC}/2$ for $V_{CC} > V_{CC\_UV}$
- The TxD timeout function is enabled (see **Chapter 6.4**).
- The overtemperature protection is enabled (see **Chapter 6.6**).
- The undervoltage detection on V_{CC} and V_{IO} are enabled (see **Chapter 6.3** and **Chapter 5.3**).

The device enters normal-operating mode by setting the mode selection pin NEN to "low", see **Figure 4**. Normal-operating mode can be entered if the device supply V_{CC} is higher than V_{CC_UV}. The device enters normal-operating mode after t_{mode} expires.

Note: If the device recognizes a recessive signal on the TxD input pin during a mode change from any mode to normal-operating mode, then it enables the transmit path after the mode change.
If the device recognizes a dominant signal on the TxD input pin during a mode change to normal-operating mode, then it keeps the transmit path disabled and it blocks the dominant signal in order to not disturb the bus communication . As soon as the device recognizes a recessive signal on the TxD input pin, it enables the transmit path again.

5.2 Power-save mode

In power-save mode the transmitter and receiver are disabled. (see also):

- The transmitter is disabled and the data available on the TxD input is blocked.
- The receiver is disabled and the data available on the bus is blocked.
- The RxD output pin is permanently set to logical "high".
- The bus biasing is connected to high impedance.
- The NEN input pin is active and if set to "low" it changes the mode of operation to normal-operating mode.
- The overtemperature protection is disabled.
- The undervoltage detection on V_{CC} is disabled. In power-save mode the device can operate without the transmitter supply V_{CC}.
- The undervoltage detection on V_{IO} is enabled.

Power-save mode can be entered from normal-operating mode by setting the NEN pin to logical "high". The device enters this mode after t_{mode} expires or after the period of t_{PON} when coming from power-down state.

5.3 Power-down State

If the supply voltage $V_{IO} < V_{IO\_UV}$, then the device powers down independently of Independent of the transmitter supply V_{CC} and NEN input pin (see **Figure 5**). In power-down state all functions of the device are disabled and the device is switched off. The input resistors of the receiver are disconnected. The CANH and CANL bus interface of the device is floating and acts as a high impedance input with a very low leakage current. The high impedance input does not influence the recessive level of the CAN and allows an optimized EME performance of the entire network. In power-down state the transceiver is an invisible node to the bus. t_{pon} must expire as a prerequisite for the device to exit power-down state.

- The transmitter and receiver are disabled.
- The bus biasing is connected to high impedance.
- The TxD timeout function is disabled.
- The overtemperature protection is disabled.
- The undervoltage detection on V_{CC} is disabled .
- The undervoltage detection on V_{IO} is enabled.

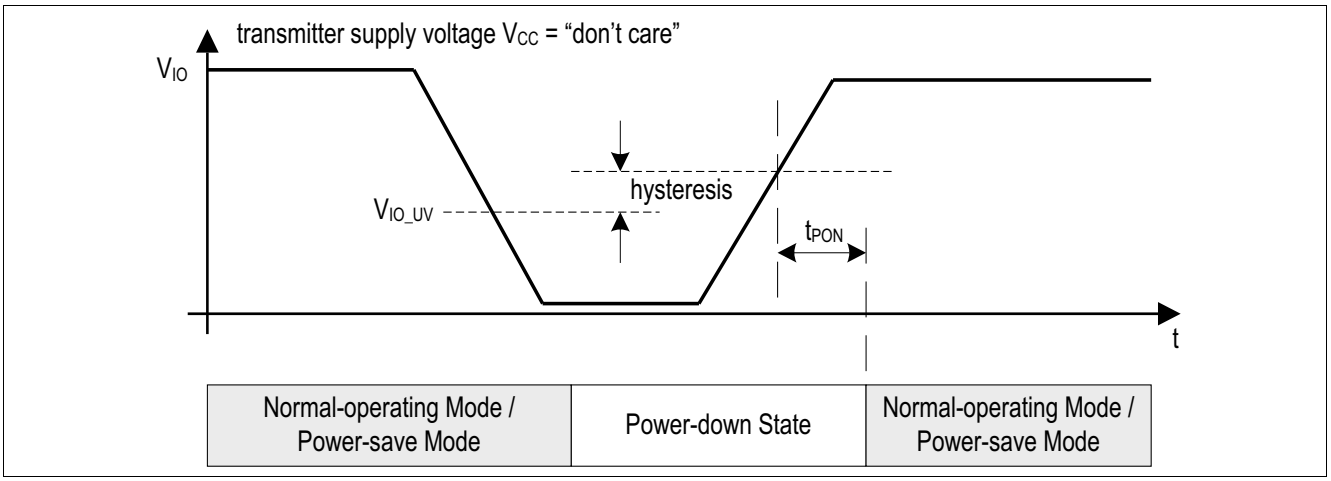


Figure 5 Power-down and power-up behavior and V_{IO}

6 Fail safe functions

6.1 Short circuit protection

The CANH and CANL bus outputs are short circuit proof to GND and short circuit proof to a supply voltage. The current limiting circuit is designed to protect the transceiver from damage. If the device heats up due to a continuous short on the CANH or CANL, then the internal overtemperature protection switches off the bus transmitter.

6.2 Unconnected logic pins

All logic input pins have an internal pull-up resistor to V_{IO}. If the V_{IO} and V_{CC} supply is active and the logical pins are open, the device enters the power-save mode by default.

6.3 V_{CC} undervoltage

If the transmitter supply is in undervoltage condition $V_{CC} < V_{CC\_UV}$, then the device might not be able to provide the correct bus levels on the CANH and CANL output pins. During this time the transmitter is blocked in normal-operating mode, to avoid any interference with the network.

During undervoltage condition $V_{CC} < V_{CC\_UV}$, the bus biasing is switched to ground in normal-operating mode.

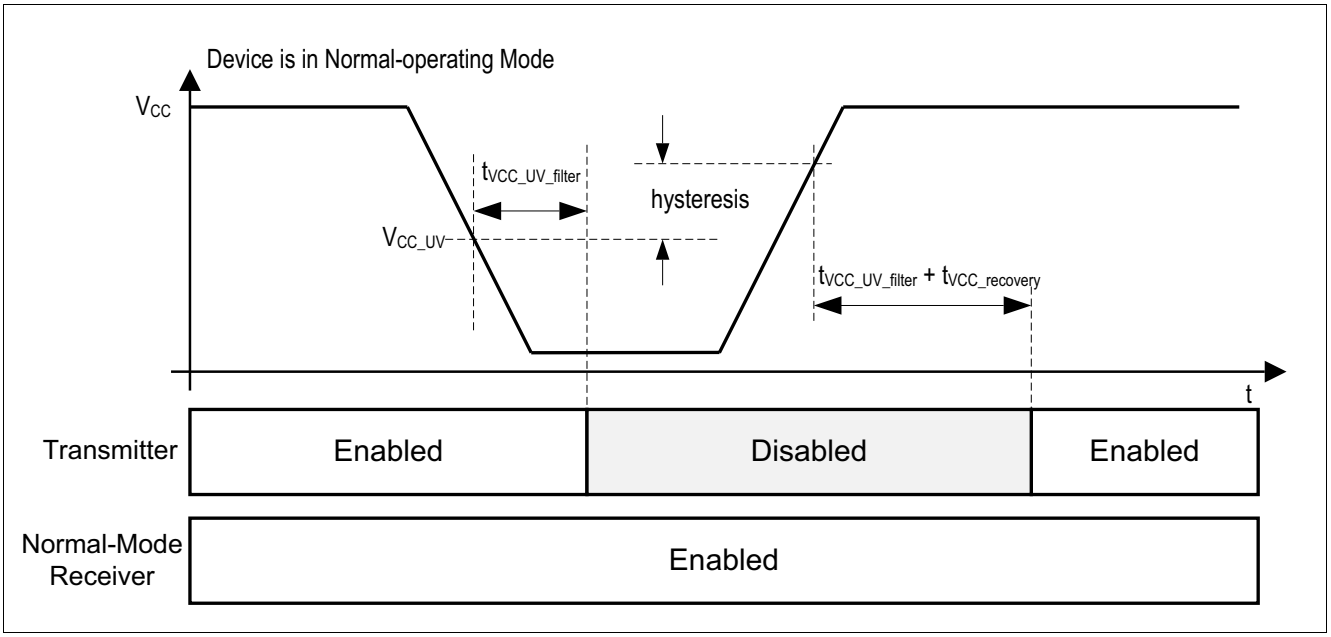


Figure 6 Undervoltage on the transmitter supply V_{CC}

6.4 TxD timeout feature

The TxD timeout feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously "low". A continuous "low" signal on the TxD pin might have its root cause in a locked-up microcontroller or in a short circuit on the printed circuit board, for example.

In normal-operating mode, a "low" signal on the TxD pin for the time $t > t_{TxD}$ enables the TxD timeout feature and the device disables the transmitter (see **Figure 7**). The receiver is still active and the device continues to monitor data on the bus via the RxD output pin.

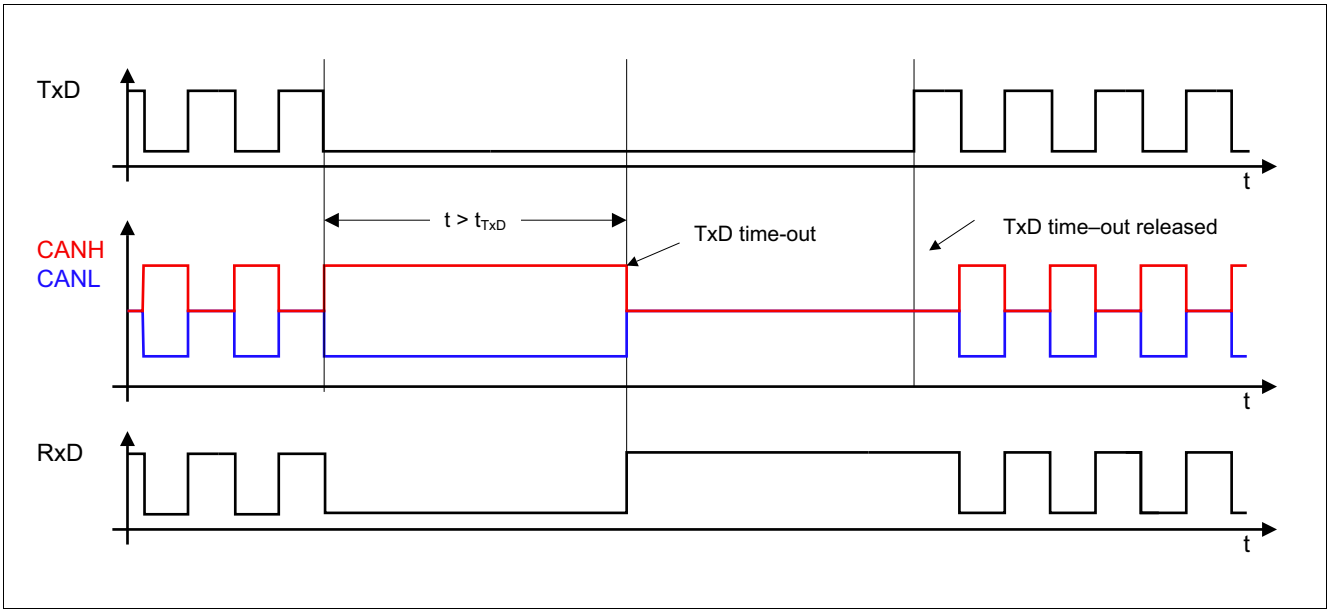


Figure 7 TxD timeout function

Figure 7 shows how the transmitter is deactivated and activated again. A permanent "low" signal on the TxD input pin activates the TxD timeout and deactivates the transmitter. To release the transmitter after a TxD timeout event, the device requires a signal change on the TxD input pin from "low" to "high".

6.5 Delay time for mode change

The device changes the mode of operation within the time window t_{Mode}. During the mode change from power-save mode to non-low power mode the device sets the RxD output "high" permanently, so it does not reflect the status on the CANH and CANL input pins.
After the mode change is completed, the device releases the RxD output pin.

6.6 Overtemperature protection

The TLE9350BVSJ has an integrated overtemperature detection, which is designed to protect the device against thermal overstress of the transmitter. The overtemperature protection is only active in normal-operating mode. In case of an overtemperature condition, the temperature sensor disables the transmitter while the transceiver remains in normal-operating mode. After the device cools down it enables the transmitter again (see **Figure 8**). A hysteresis is implemented within the temperature sensor.

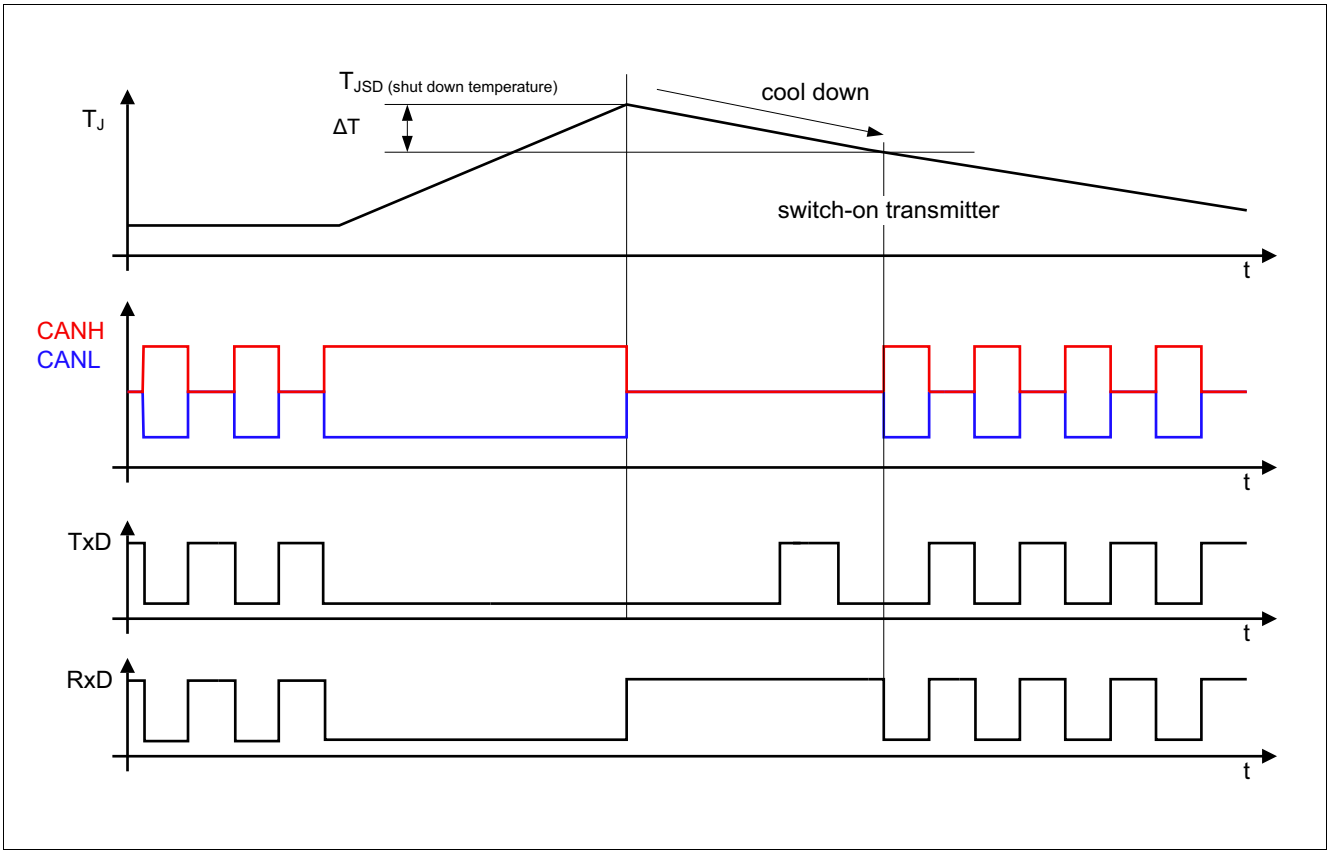


Figure 8 Overtemperature protection

7 Electrical characteristics

7.1 Power supply interface

7.1.1 Electrical characteristics current consumption

Table 5 Electrical characteristics current consumption

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at V_{CC} normal-operating mode, recessive state	I_{CC_R}	–	1.4	4	mA	V_{TxD} = V_{IO}; V_{NEN} = 0 V; V_{CANH} = V_{CANL} = V_{CC}/2	P_8.1.1
Current consumption at V_{CC} normal-operating mode, dominant state	I_{CC_D}	–	34	48	mA	V_{TxD} = V_{NEN} = 0 V	P_8.1.2
Current consumption at V_{IO} normal-operating mode	I_{IO}	–	0.9	1.5	mA	V_{NEN} = 0 V; V =V_{IO} ; V_{Diff} = 0 V; recessive	P_8.1.3
Current consumption at V_{CC} power-save mode	$I_{CC(PSM)}$	–	0.005	5	µA	V_{TxD} = V_{NEN} = V_{IO}	P_8.1.4
Current consumption at V_{IO} power-save mode	$I_{IO(PSM)}$	–	7	18	µA	V_{TxD} = V_{NEN} = V_{IO}; 0 V < V_{CC} < 5.5 V	P_8.1.6

7.1.2 Electrical characteristics undervoltage detection

Table 6 Electrical characteristics undervoltage detection

4.5 V $< V_{CC} <$ 5.5 V; 3.0 V $< V_{IO} <$ 5.5 V; R_L = 60 Ω; -40°C $< T_j <$ 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
V_{CC} undervoltage threshold	V_{CC_UV}	3.8	4.2	4.5	V	see **Figure 6**	P_8.1.11
V_{CC} undervoltage filter time	$t_{VCC\_UV\_filter}$	4	6	10	µs	1) see **Figure 6**	P_8.1.13
V_{CC} undervoltage recovery time	$t_{VCC\_recovery}$	–	7	70	µs	1) see **Figure 6**	P_8.1.14
V_{IO} undervoltage threshold	V_{IO_UV}	2.0	2.6	3.0	V	–	P_8.1.15
V_{IO} delay time power-up	t_{PON}	–	40	280	µs	1) see **Figure 5**	P_8.1.19

1) Not subject to production test, specified by design.

7.2 Electrical characteristics CAN controller interface

Table 7 Electrical characteristics CAN controller interface

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver output RxD							
"High" level output current	I_{RxD_H}	–	-2.5	-1	mA	V_{RxD} = V_{IO} -0.4 V; V_{Diff} < 0.5 V	P_8.2.1
"Low" level output current	I_{RxD_L}	1	2.5	–	mA	V_{RxD} = 0.4 V; V_{Diff} > 0.9 V	P_8.2.2
Transmission input TxD							
"High" level input voltage	V_{TxD_H}	0.7 × V_{IO}	–	6.0	V	recessive state	P_8.2.3
"Low" level input voltage	V_{TxD_L}	-0.3	–	0.3 × V_{IO}	V	dominant state	P_8.2.4
Internal pull-up resistor TxD	R_{TxD}	35	55	70	kΩ	–	P_8.2.7
Input capacitance	C_{TxD}	–	–	10	pF	1)	P_8.2.8
TxD permanent dominant timeout	t_{TxD}	1	2.3	4	ms	normal-operating mode	P_8.2.9
non-enable input NEN							
"High" level input voltage	V_{NEN_H}	0.7 × V_{IO}	–	6.0	V	power-save mode	P_8.2.13
"Low" level input voltage	V_{NEN_L}	-0.3	–	0.3 × V_{IO}	V	normal-operating mode	P_8.2.14
Internal pull-up resistor NEN	R_{NEN}	35	55	70	kΩ	–	P_8.2.16
Input capacitance	$C_{(NEN)}$	–	–	10	pF	1)	P_8.2.20

1) Not subject to production test, specified by design.

7.3 Electrical characteristics receiver

Table 8 Electrical characteristics receiver

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Differential range dominant normal-operating mode	$V_{Diff\_D\_Range}$	0.9	–	8.0	V	1) -12 V ≤ V_{CMR} ≤ 12 V	P_8.3.3
Differential range recessive normal-operating mode	$V_{Diff\_R\_Range}$	-3.0	–	0.5	V	1) -12V ≤ V_{CMR} ≤ 12 V	P_8.3.5
Common mode range	CMR	-12	–	12	V	–	P_8.3.11
Single ended internal resistance	R_{CAN_H}, R_{CAN_L}	6	40	50	kΩ	1) recessive state; -2 V ≤ V_{CANH} ≤ 7 V; -2 V ≤ V_{CANL} ≤ 7 V	P_8.3.12
Differential internal resistance	R_{Diff}	12	80	100	kΩ	1) recessive state; -2 V ≤ V_{CANH} ≤ 7 V; -2 V ≤ V_{CANL} ≤ 7 V	P_8.3.14
Input resistance deviation between CANH and CANL	ΔR_i	-2	–	2	%	1) recessive state; V_{CANH} = V_{CANL} = 5 V	P_8.3.16
Input capacitance CANH, CANL versus GND	C_{In}	–	–	40	pF	1)2) recessive state; normal-operating mode	P_8.3.17
Differential input capacitance	C_{InDiff}	–	4	20	pF	1)2) recessive state; normal-operating mode	P_8.3.18

1) Not subject to production test, specified by design.

2) S2P-Method; f = 10 MHz.

7.4 Electrical characteristics transmitter

Table 9 Electrical characteristics transmitter

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANL, CANH recessive output voltage normal-operating mode	$V_{CANL,H}$	2.0	2.5	3.0	V	V_{TxD} = V_{IO}; no load	P_8.4.1
CANH, CANL recessive output voltage difference normal-operating mode	$V_{Diff\_R\_NM}$ = V_{CANH} - V_{CANL}	-50	-10	50	mV	V_{TxD} = V_{IO}; no load	P_8.4.2
CANL dominant output voltage normal-operating mode	V_{CANL}	0.5	1.5	2.25	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω	P_8.4.3
CANH dominant output voltage normal-operating mode	V_{CANH}	2.75	3.4	4.5	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω	P_8.4.4
Differential voltage dominant normal-operating mode V_{Diff} = V_{CANH} - V_{CANL}	$V_{Diff\_D\_NM}$	1.5	1.9	2.5	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω 4.75V < V_{CC} < 5.25V	P_8.4.5
Differential voltage dominant extended bus load normal-operating mode	$V_{Diff\_EXT\_BL}$	1.4	1.9	3.3	V	V_{TxD} = 0 V; 45 Ω < R_L < 70 Ω 4.75V < V_{CC} < 5.25V	P_8.4.6
Differential voltage dominant high extended bus load normal-operating mode	$V_{Diff\_HEXT\_BL}$	1.5	3.5	5.0	V	[1] V_{TxD} = 0 V; R_L = 2240Ω; static behavior 4.75V < V_{CC} < 5.25V	P_8.4.7
Driver symmetry (V_{SYM} = V_{CANH} + V_{CANL})	V_{SYM}	0.9 × V_{CC}	1.0 × V_{CC}	1.1 × V_{CC}	V	[1)2)] C_1 = 4.7 nF	P_8.4.10
CANL short circuit current	I_{CANLsc}	-115	90	115	mA	[1] -3 V < $V_{CANLshort}$ < 18 V; t < t_{TxD}; V_{TxD} = 0 V	P_8.4.11
CANH short circuit current	I_{CANHsc}	-115	-90	115	mA	[1] -3 < $V_{CANHshort}$ < 18 V; t < t_{TxD}; V_{TxD} =0 V	P_8.4.13
Leakage current, CANH	$I_{CANH,lk}$	-5	1	5	µA	V_{CC} = V_{IO} = 0 V; 0 V < V_{CANH} ≤ 5 V; V_{CANH} = V_{CANL};	P_8.4.19
Leakage current, CANL	$I_{CANL,lk}$	-5	1	5	µA	V_{CC} = V_{IO} = 0 V; 0 V < V_{CANL} ≤ 5 V; V_{CANH} = V_{CANL}	P_8.4.20

Table 9 Electrical characteristics transmitter (Continued)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	–	42	70	V/µs	[1] 30% to 70% of measured differential bus voltage, C_2 = 100 pF, R_L = 60 Ω, 4.75 V < V_{CC} < 5.25 V	P_8.4.21
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	-70	-42	–	V/µs	[1] 70% to 30% of measured differential bus voltage, C_2 = 100 pF, R_L = 60 Ω, 4.75 V < V_{CC} < 5.25 V	P_8.4.22

1) Not subject to production test, specified by design.

2) V_{SYM} is observed during dominant and recessive state and also during the transition from dominant to recessive state and vice versa, while TxD is stimulated by a square wave signal with a frequency of 1 MHz .

7.5 Electrical characteristics dynamic transceiver parameters

Table 10 Electrical characteristics dynamic transceiver parameters

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay TxD-to-RxD	t_{Loop}	80	150	235	ns	C_1 = 0 pF, C_2 = 100 pF, C_{RxD} = 15 pF; (see **Figure 10**)	P_8.5.1
Propagation delay increased load TxD-to-RxD	t_{Loop_150}	80	180	330	ns	C_1 = 0 pF, C_2 = 100 pF, C_{RxD} = 15 pF, R_L = 150 Ω [1)]	P_8.5.2
Propagation delay TxD to bus "low" to dominant	$t_{d(L)\_T}$	30	70	140	ns	C_1 = 0 pF, C_2 = 100 pF, C_{RxD} = 15 pF; (see **Figure 10**)	P_8.5.3
Propagation delay TxD to bus "high" to recessive	$t_{d(H)\_T}$	30	90	140	ns	C_1 = 0 pF, C_2 = 100 pF, C_{RxD} = 15 pF; (see **Figure 10**)	P_8.5.4
Propagation delay bus to RxD dominant to "low"	$t_{d(L)\_R}$	30	90	140	ns	C_{RxD} = 15 pF, Independent of t_{Bit}; (see **Figure 10**)	P_8.5.5
Propagation delay bus to RxD recessive to "high"	$t_{d(H)\_R}$	30	100	140	ns	C_{RxD} = 15 pF, Independent of t_{Bit}; (see **Figure 10**)	P_8.5.6
Delay times							
Delay time for mode change	t_{Mode}	–	12	20	µs	[1)]	P_8.5.7
CAN FD characteristics							
Received recessive bit width at 2 Mbit/s	$t_{Bit(RxD)\_2M}$	420	450	520	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 500 ns; see **Figure 11**	P_8.5.13
Received recessive bit width at 5 Mbit/s	$t_{Bit(RxD)\_5M}$	120	150	220	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 200 ns; see **Figure 11**	P_8.5.14
Transmitted recessive bit width at 2 Mbit/s	$t_{Bit(Bus)\_2M}$	455	470	510	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 500 ns; see **Figure 11**	P_8.5.15

Table 10 Electrical characteristics dynamic transceiver parameters (Continued)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmitted recessive bit width at 5 Mbit/s	$t_{Bit(Bus)\_5M}$	155	170	210	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 200 ns; see **Figure 11**	P_8.5.16
Receiver timing symmetry at 2 Mbit/s $\Delta t_{Rec\_2M} = t_{Bit(RxD)\_2M} - t_{Bit(Bus)\_2M}$	Δt_{Rec_2M}	-45	-23	15	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 500 ns; 4.75 V < V_{CC} < 5.25 V; see **Figure 11**	P_8.5.17
Receiver timing symmetry at 5 Mbit/s $\Delta t_{Rec\_5M} = t_{Bit(RxD)\_5M} - t_{Bit(Bus)\_5M}$	Δt_{Rec_5M}	-45	-23	15	ns	C_2 = 100 pF; C_{RxD} = 15 pF; t_{Bit} = 200 ns; 4.75 V < V_{CC} < 5.25 V; see **Figure 11**	P_8.5.18

1) Not subject to production test, specified by design.

7.6 Diagrams

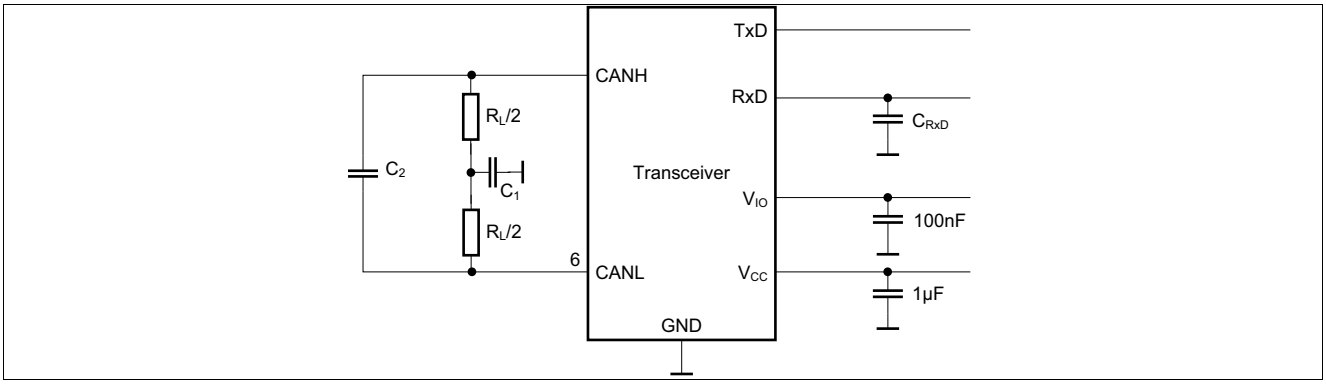


Figure 9 Test circuit

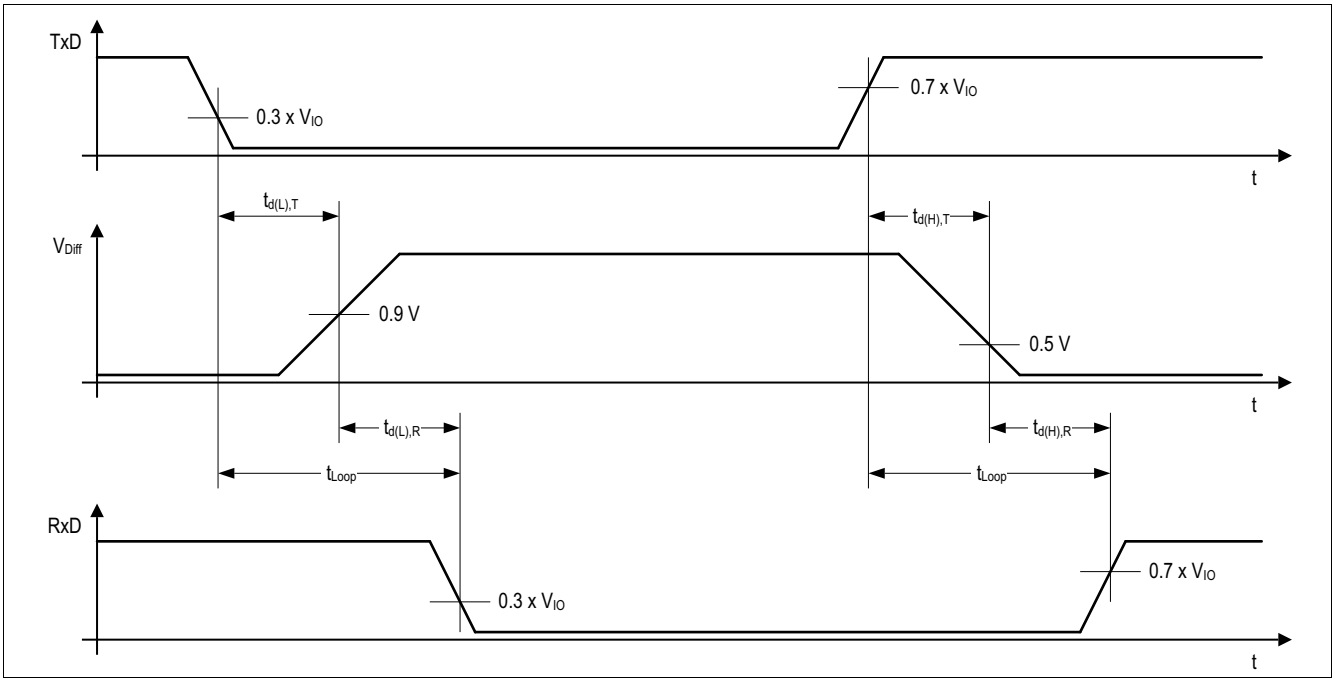


Figure 10 Timing diagrams for dynamic characteristics

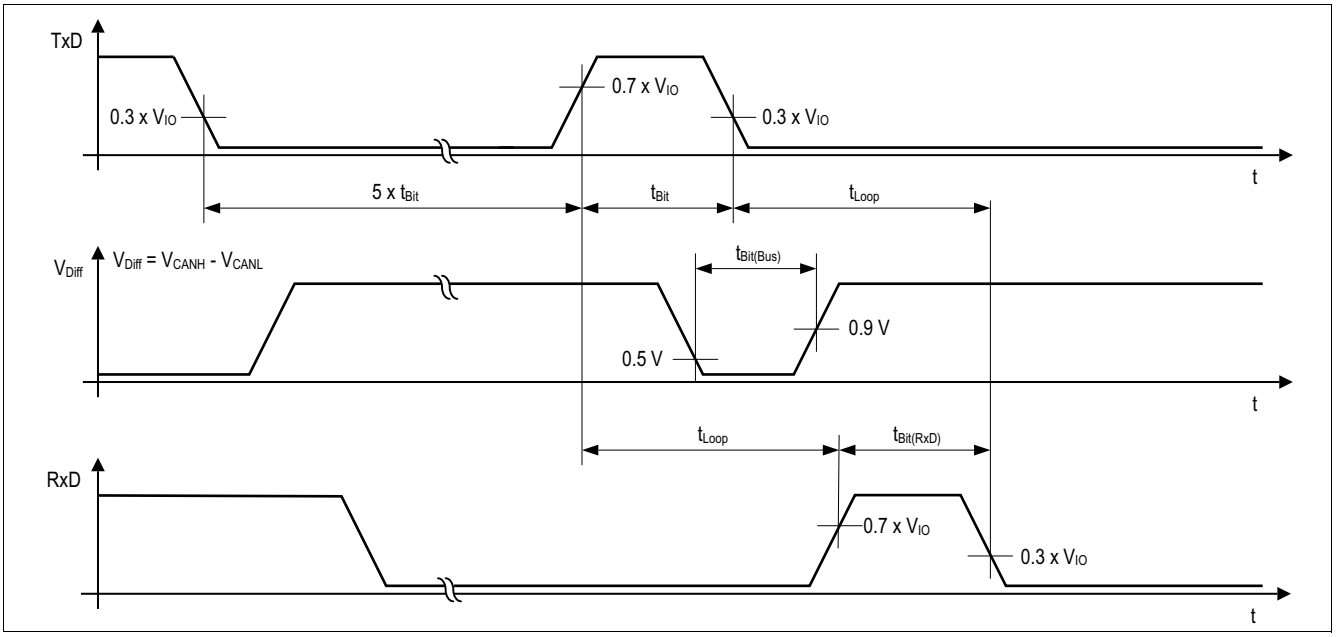


Figure 11 Recessive bit time for five dominant bits followed by one recessive bit

8 Application information

8.1 ESD robustness according to IEC 61000-4-2

Tests for ESD robustness according to IEC 61000-4-2 Gun test (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 11 ESD robustness according to IEC 61000-4-2

Performed test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus GND	≥ +8	kV	1) positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	≤ -8	kV	1) negative pulse

1) Not subject to production test. ESD susceptibility "ESD GUN" according to GIFT/ICT paper: "EMC Evaluation of CAN Transceivers, version IEC TS62228", section 4.3. (DIN EN61000-4-2)
Tested by external test facility (IBEE Zwickau).

8.2 Application example

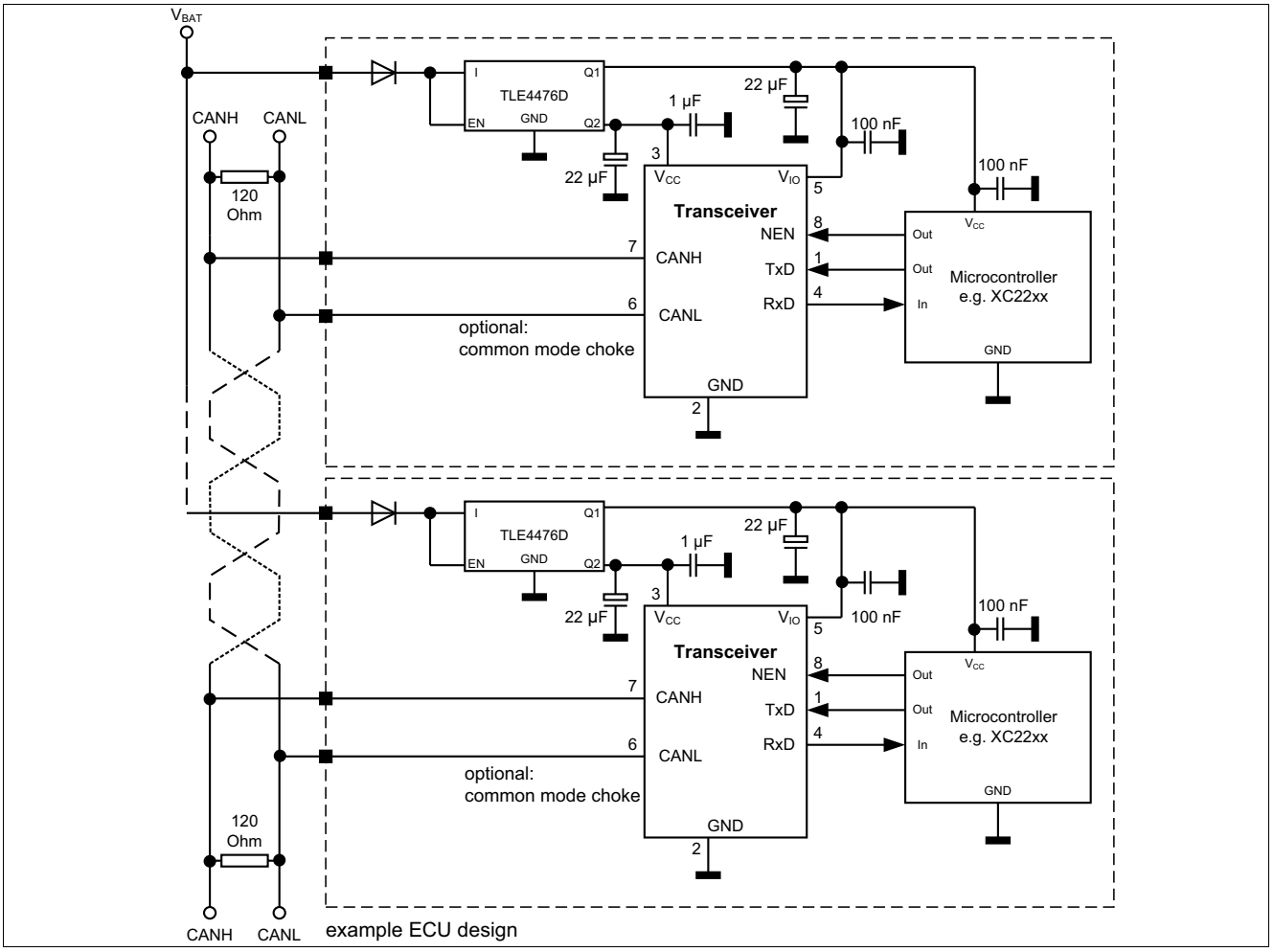


Figure 12 Application circuit

8.3 Voltage adaption to the microcontroller supply

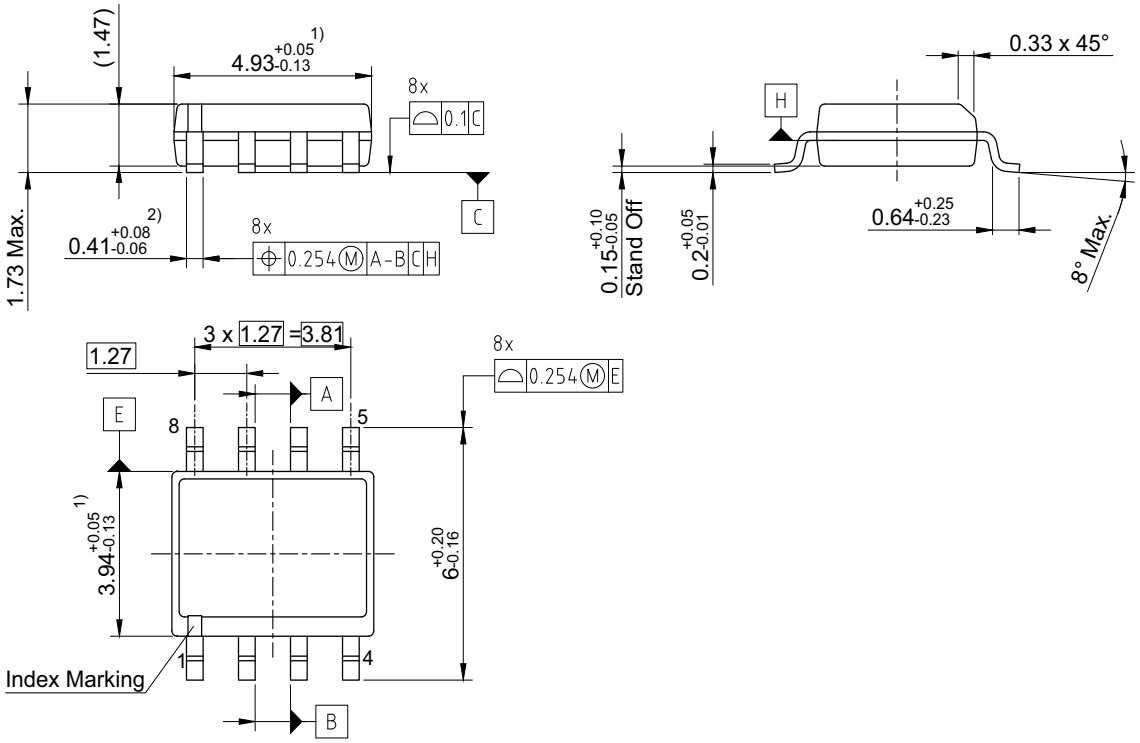
To adapt the digital input and output levels of the device to the I/O levels of the microcontroller, connect the power supply pin V_{IO} to the microcontroller voltage supply, see **Figure 12**.

Note: If case no dedicated digital supply voltage V_{IO} is required in the application, then connect the digital supply voltage V_{IO} to the transmitter supply V_{CC}.

8.4 Further application information

For further information you may visit: **https://www.infineon.com/automotive-transceiver**

9 Package information



1) Does not include plastic or metal protrusion of 0.25 Max. per side
2) Does not include dambar protrusion of 0.1 Max. per side
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 13 PG-DSO-8

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

10 Revision history

Revision	Date	Changes
1.0	2023-08-11	Datasheet created

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-08-11
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Z8F80194911

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:

TLE9350BVSJXTMA1