256-Mb, 1.8-V SEMPER™ Nano

Quad SPI Flash with multi-pass programming

General description

This supplementary datasheet contains information for the SEMPER™ Nano Quad SPI Flash. Specifications contained in this supplement supersede those in the S25FS256T datasheet. This device supports multi-pass programming. Refer to the latest S25FS512T datasheet for full features specifications.

Affected documents/related documents

Title	Publication number
S25FS256T, 256-Mb (32-MB), FS-T (1.8-V) SEMPER™ Nano	002-27914

Data integrity

Program / erase (PE) endurance - commercial (0 °C to +70 °C)

Sectors size and configuration	Minimum PE cycles	Minimum retention time	Unit
128 KB 2bpc	5,000	25	Years
64 KB 1bpc	60,000	2	
	72,000	1	
	100,000	0.28	

Note: Data integrity is for use case with < 2% ECC off in the entire array, where most ECC off data units are in 64 KB 1 bps sectors and < 200 bytes ECC of data units for 128 KB 2 bps sectors.

1 Features

1.1 Program granularity

The device supports multi-pass programming where programming a ‘0’ over a ‘1’ without performing the sector erase operation. Multi-pass programming without an erase operation will disable the device’s ECC functionality for that data unit. Data Integrity for this data unit will be effected. It is required to program only in 16-byte data unit granularity to keep ECC enabled. Note that if 2-bit ECC is enabled CFR4N[3] = 1, multi-pass Programming within the same sector will result in a Program Error.

1.2 Page programming

Page programming is done by loading a page buffer with data to be programmed and issuing a programming transaction to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with single programming transaction. Page programming allows up to a page size (either 256- or 512-bytes) to be programmed in one operation. The page size is determined by the Configuration Register 1 bit CFR3V[4]. The page is aligned on the page size address boundary. It is possible to program from one byte up to a page size in each page programming operation. It is recommended that a multiple of 16-byte length and aligned program blocks be written. This ensures that ECC is not disabled. For the very best page program throughput, programming should be done in full pages of 512 bytes aligned on 512-byte boundaries with each page being programmed only once.

1.3 Program secure silicon region transaction

The program secure silicon transaction (PRSSR_C_1) programs data in the SSR, which is in a different address space from the main array data and is OTP. The SSR is 1024 bytes, so the address bits from A31 to A10 must be zero for this transaction. It is required to align start address to 32 bits while programming SSR space, which means the address bits A1 and A0 should be 0'b and host should deassert CS# to align with 32 bits.

The PRGERR bit in STR1V[6] may be checked to determine if any error occurred during the operation.

To program the OTP array in bit granularity, the rest of the bits within a data byte can be set to ‘1’.

Each SSR memory space can be programmed one or more times, provided that the region is not locked. Attempting to program zeros in a region that is locked will fail with the PRGERR bit in STR1V[6] set to ‘1’. Programming once, even in a protected area does not cause an error and does not set PRGERR bit. Subsequent programming can be performed only on the unprogrammed bits (that is, 1 data). Programming more than once within an ECC unit will disable ECC on that data unit.

1.4 Error detection and correction

The device supports error detection and correction by generating an embedded Hamming ECC during memory array programming. This ECC code is then used for error detection and correction during read operations. The ECC is based on a 16-byte data unit. When the 16-byte data unit is loaded into the program buffer and is transferred to the 128-bits flash memory array Line for programming (after an erase), an 8-bit ECC for each data unit is also programmed into a portion of the memory array that is not visible to the host system software. This ECC information is then checked during each Flash array read operation. Any 1-bit error within the data unit will be corrected and 2-bit error detected by the ECC logic. The 16-byte data unit is the smallest program granularity on which ECC is enabled.

When any amount of data is first programmed within a 16-byte data unit, the ECC value is set for the entire data unit. If additional data is subsequently programmed into the same data unit, ECC for that data unit is disabled and the 1-bit ECC disable bit is set. A sector erase is needed to again enable ECC on that data unit. The disable ECC, will affect the data integrity on data unit.

It is required to program only in 16-byte data unit granularity to keep ECC enabled to meet data integrity specification.

These are automatic operations transparent to the user. The transparency of the ECC feature enhances data reliability for typical programming operations which write data once to each data unit while also facilitating software compatibility with previous generations of products by still allowing for single-byte programming and bit-walking (in this case, ECC will be disabled) in which the same data unit is programmed more than once.

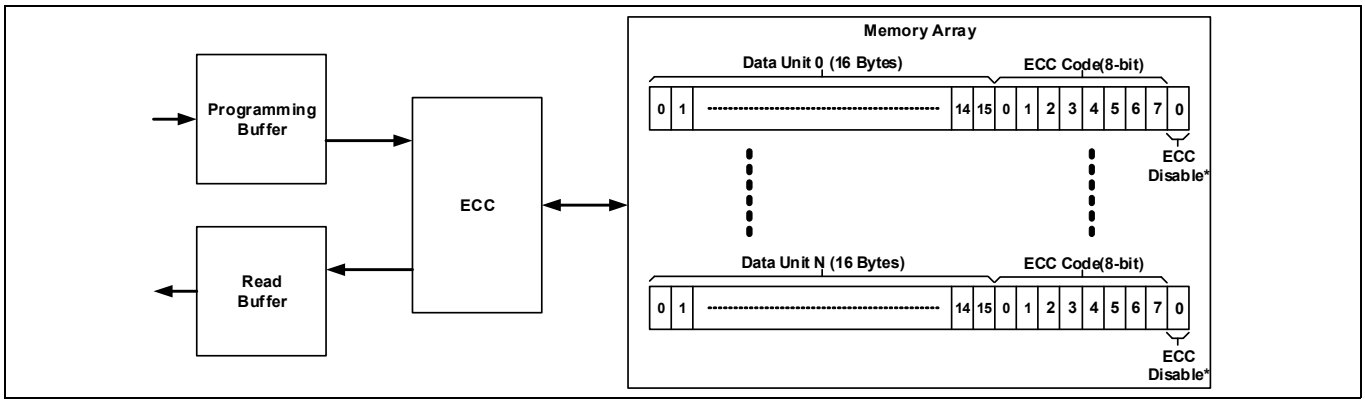


Figure 1-1 16-byte ECC data unit example

Device 1-bit error correction and 2-bit error detection is enabled when CFR4x[3] = 1. The 16-byte unit data requires a 9-bit error correction code (ECC) for 2-bit error detection. In this configuration, any 1-bit error in a data unit is corrected and any 2-bit error is detected and reported. When 2-bit error detection is enabled, byte-programming, bit-walking, or multiple program operations to the same data unit (without an erase) are not allowed and will result in a Program Error. Changing the ECC mode from 1-bit error detection to 2-bit error detection, or from 2-bit error detection to 1-bit error detection will invalidate all data in the memory array. When changing the ECC mode, the host must first erase all sectors in the device. If the ECC mode is changed without erasing programmed data, subsequent read operations will result in undefined behavior.

1.4.1 ECC error reporting

There are two methods for reporting to the host system when ECC errors are detected.

- ECC data unit status provides the status of 1-bit and 2-bit errors in data units.
- ECC status register provides the status of 1-bit and 2-bit errors since the last ECC clear or reset.

1.4.1.2 ECC data unit status (EDUS)

- The status of ECC in each data unit is provided by the 8-bit ECC data unit status.
- The ECC status transaction outputs the ECC status of the addressed data unit. The contents of the ECC data unit status then indicate, for the selected data unit, whether there is a 1-bit error corrected, 2-bit error detected or the ECC is disabled for that data unit.

Table 1-1 EDUS

Bits	Field name	Function	Read/write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EDUS[7:4]	RESRVD	Reserved For future use	V => R	0000	These bits are reserved for future use.
EDUS[3]	ECC2BD	ECC error 2-bit error detection flag	V => R	0	This bit indicates whether a two bit error is detected in the data unit. **Selection options:** 1 = Two bit error detected 0 = No error
EDUS[2]	RESRVD	Reserved for future use	V => R	0	This bit is Reserved for future use.

Table 1-1 EDUS (Continued)

Bits	Field name	Function	Read/write N = Nonvolatile V = Volatile	Factory default (binary)	Description
EDUS[1]	ECC1BC	ECC error 1-bit error detection and correction flag	V => R	0	This bit indicates whether an error is corrected in the data unit. **Selection options:** 1 = Single bit error corrected in the addressed data unit 0 = No single bit error was corrected in the addressed data unit
EDUS[0]	ECCOFF	Data unit ECC OFF/ON flag	V => R	0	This bit indicates whether the ECC syndrome is OFF in the data unit. **Selection options:** 1 = ECC is OFF in the selected data unit 0 = ECC is ON in the selected data unit

1.4.1.3 ECC status register (ECSV)

- An 8-bit ECC status register provides the status of 1-bit or 2-bit errors during normal reads since last ECC clear or reset. ECC status register does not have user programmable nonvolatile bits, all defined bits are volatile read only bits. The default state of these bits are set by hardware.
- ECC status register can be accessed through the Read Any Register transaction. The correct sequence for Read Any Register based ECSV is read as follows:
  - Read data from memory array using any of the Read transaction
  - ECSV is updated by the device
  - Read Any Register transaction of ECSV provides the status of any ECC event since the last clear or reset.
- ECSV is cleared by POR, CS# signaling reset, hardware/software reset, or a clear ECC status register transaction.

2 Registers

2.1 Configuration register 4 (CFR4x)

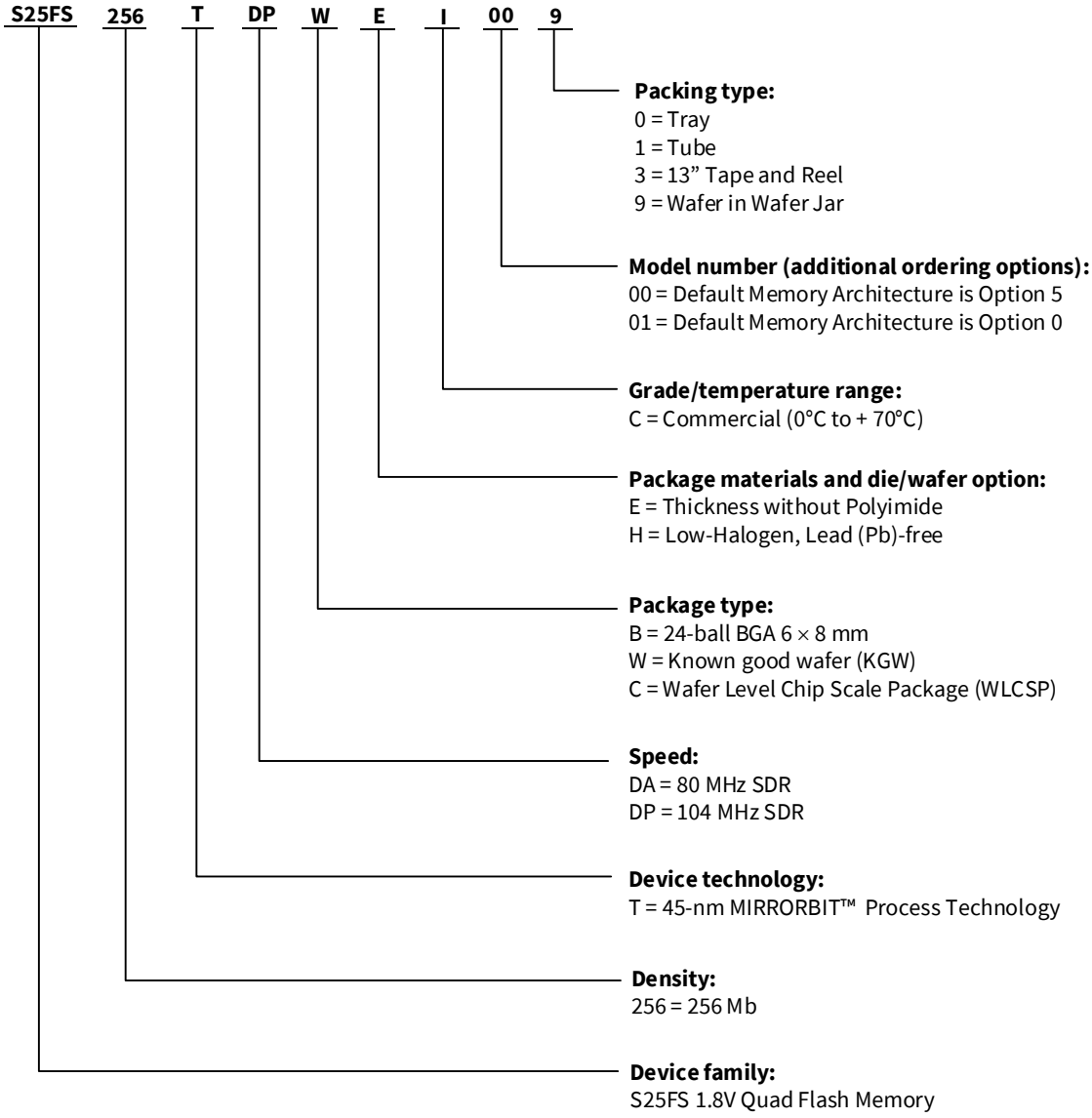
Configuration register 4 controls output driver impedance.

Table 1 Configuration register 4

Bit number	Name	Function	Read/write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR4N[7:5] CFR4V[7:5]	IOIMPD[2:0]	I/O driver output impedance selection	N -> R/W V -> R/W	000	Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration bits adjust the drive strength during normal device operation to meet system signal integrity requirements. Selection options: 000 = 45Ω (Factory Default) 001 = 120Ω 010 = 90Ω 011 = 60Ω 100 = 45Ω 101 = 30Ω 110 = 20Ω 111 = 15Ω
CFR4N[4] CFR4V[4]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	This bit is reserved for future use. This bit must always be written/loaded to its default state.
CFR3N[3] CFR3V[3]	ECC12S	Error correction code (ECC) 1-bit or 1-bit/2-bit error correction selection	N -> R/W V -> R/W	0	Description: The ECC12S bit selects between 1-bit ECC error detection/correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection. The host needs to erase and reprogram the data in the SEMPER™ Flash memory upon ECC configuration change (1-bit correction to 1-bit correction and 2-bit detection or vice versa). Selection options: 0 = 1-bit ECC Error Detection/Correction and Multi-pass programming in the data unit will disable ECC, effecting the Data Integrity on data unit. 1 = 1-bit ECC Error Detection/Correction and 2-bit ECC error detection and Multi-pass programming in the ECC data unit will cause a program error. Dependency: N/A
CFR4N[2:0] CFR4V[2:0]	RESRVD	Reserved for future use	N -> R/W V -> R/W	000	This bit is reserved for future use. This bit must always be written/loaded to its default state.

3 Ordering information

The ordering part number is formed by a valid combination of the following:



Note

1. See Packing and Packaging Handbook on www.cypress.com for further information.

3.1 Valid combinations

Valid Combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 3-1 Valid combinations — sampling

Base ordering part number	Speed option	Package and die/wafer	Temperature range	Model number	Packing type	Ordering part number (x = Packing type)	Package marking
S25FS256T	DA	WE	C	00	9	S25FS256TDAWEC00x	–
S25FS256T	DA	WE	C	01	9	S25FS256TDAWEC01x	–
S25FS256T	DA	CH	C	00	3	S25FS256TDACHC00x	S256AC0
S25FS256T	DA	CH	C	01	3	S25FS256TDACHC01x	S256AC1

Table 3-2 Valid combinations — contact sales

Base ordering part number	Speed option	Package and die/wafer	Temperature range	Model number	Packing type	Ordering part number (x = Packing type)	Package marking
S25FS256T	DP	BH	C	01	0, 3	S25FS256TDPBHC01x	25FS256TPC01
S25FS256T	DP	BH	C	00	0, 3	S25FS256TDPBHC00x	25FS256TPC00
S25FS256T	DP	CH	C	01	3	S25FS256TDPCHC01x	S256PC1

Revision history

Document version	Date of release	Description of changes
**	2021-07-22	Initial release

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