Isolated gate driver IC with a configurable floating bipolar auxiliary supply for SiC MOSFETs

KIT_1EDB_AUX_SiC

About this document

Scope and purpose

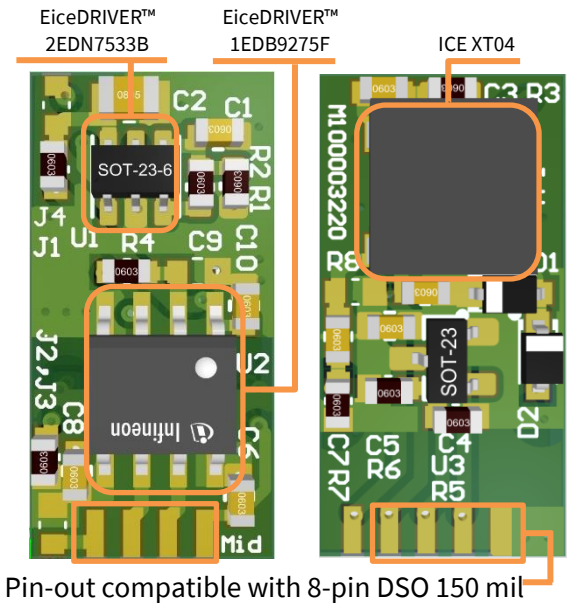
KIT_1EDB_AUX_SiC is a complete driving solution for silicon carbide (SiC) MOSFETs that includes an isolated single-channel gate driver IC (**EiceDRIVER™ 1EDB9275F**) and its floating auxiliary supply enabled by a compact dual-channel non-isolated gate driver IC (**EiceDRIVER™ 2EDN7533B**).

The board is pin-out compatible with the EiceDRIVER™ 1EDB9275F itself and with equivalent drivers in the industry-standard 150 mil DSO-8 package. Therefore, it is an easy plug-in solution in designs that already include those isolated gate drivers and allows testing the EiceDRIVER™ 1EDB9275F in combination with an isolated bipolar auxiliary supply; one potential replacement scenario is for example when bootstrap is originally used in the design but cannot be used due to the modulation scheme or topology change. Compared to the standard 150 mil DSO-8 footprint, the output ground pin (GNDO) on the main board is replaced with the midpoint of the auxiliary supply; this allows testing with bipolar supply that is particularly relevant to drive SiC MOSFETs with poor C_{GD}/C_{GS} ratio or low $V_{(GS)th}$ threshold.

The board allows driving of SiC MOSFETs with typical bipolar gate-to-source voltages that can be easily configured by means of R5, R6 and R7 resistors. It also allows 1 percent regulation of the positive rail independently of the driven device, switching frequency and temperature. High common-mode transient immunity (CMTI) is also ensured thanks to the very low input-to-output capacitance (3 pF) of the XT04 transformer and the high robustness of EiceDRIVER™ 1EDB9275F (more than 300 V/ns).

Intended audience

This document targets power electronic engineers and designers who are interested in a bipolar auxiliary supply for their SiC design featuring compactness, high efficiency, good regulation and attractive cost.



V_{pos}, regulated	V_{neg} at 10 mA	V_{CCI}	R5, R6, R7
+18 V	-1 V	10 V	31.6 kΩ, 5.1 kΩ, 510 Ω
+18 V	-5 V	12 V[1]	31.6 kΩ, 5.1 kΩ, 3 kΩ
+15 V	-4 V	10 V	31.6 kΩ, 6.2 kΩ, 2.4 kΩ
+20 V	-3 V	12 V[1]	36 kΩ, 5.1 kΩ, 1 kΩ

[1] This combination is possible only by replacing EiceDRIVER™ 1EDB9275F with EiceDRIVER™ 1ED3124MU12F, which has a higher V_{DD} rating.

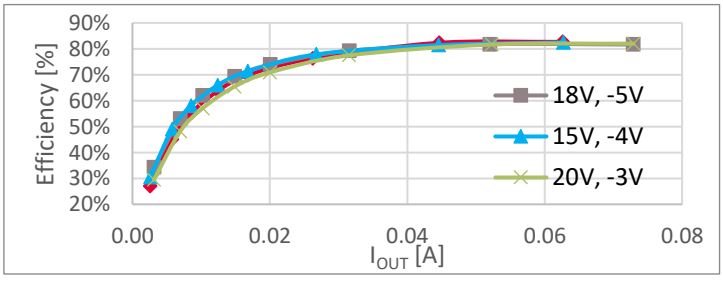


Figure 1 Overview of KIT_1EDB_AUX_SiC

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1 Driving a SiC MOSFET – requirements

1.1 High $R_{DS(on)}$ to V_{GS} dependency of SiC MOSFETs and the need for an accurate positive supply

Figure 2 gives a market overview of the gate-to-source voltage (V_{GS}) requirements for several SiC MOSFETs. Technology limits in DC and transient are shown, including the recommendation (at the time of Revision 1.0 of this application note) from each vendor in terms of operating V_{GS}; it considers several factors as proper margins from the technology limits and the device re-turn-on immunity (see Section **1.2**).

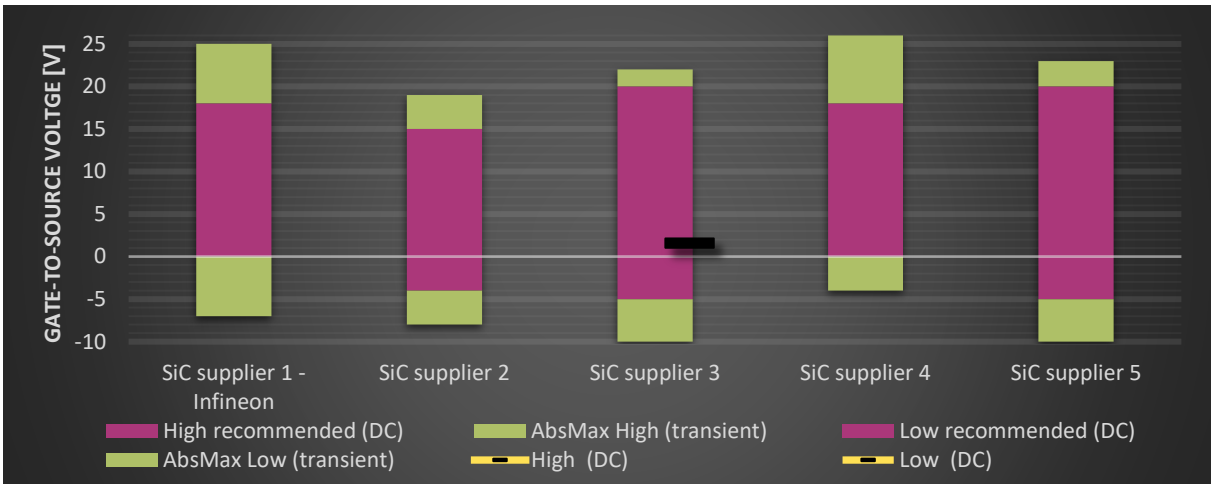

Figure 2 Overview of gate-to-source voltage requirements for available SiC MOSFETs

Compared to standard silicon (Si) MOSFETs, the driving voltage requirements for SiC devices increases with positive gate-to-source voltages from 15 V to 20 V (18 V is recommended for Infineon CoolSiC™). Additionally, SiC devices show a strong linear behavior of the transconductance g_m: small V_{GS} differences (e.g., 1 or 2 V) can cause significant $R_{DS(on)}$ change. Therefore, it is fundamental to consider auxiliary supplies with high accuracy. KIT_1EDB_AUX_SiC can be dimensioned for a typical 15 V, 18 V or 20 V driving and by default offers a regulated positive rail with 1 percent accuracy. As an example, driving Infineon **CoolSiC™ IMW65R027M1H** at 18 V with ±1 percent accuracy ensures less than 2 percent $R_{DS(on)}$ changes at a given temperature (see **Figure 3**).

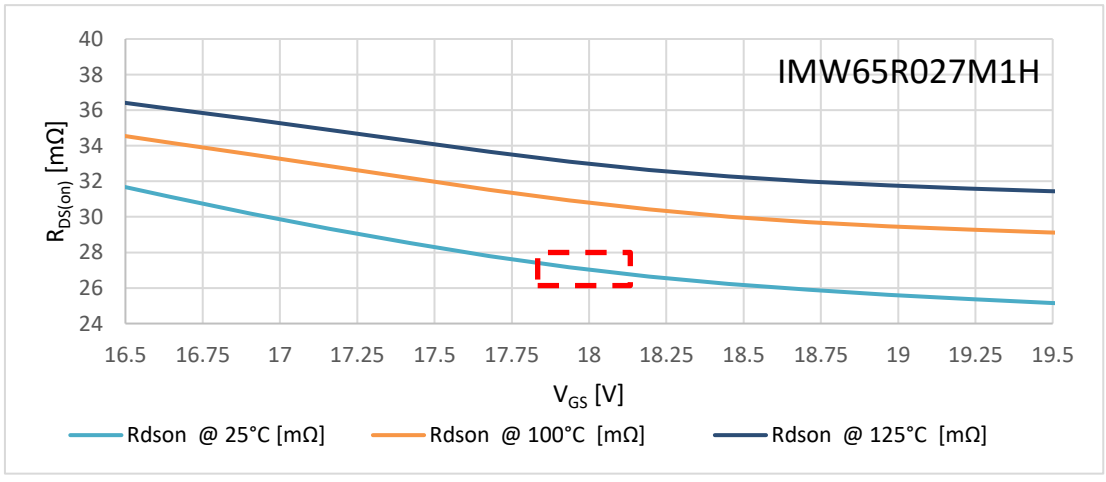

Figure 3 Infineon CoolSiC™ IMW65R027M1H and $R_{DS(on)}$ variation with V_{GS}

1.2 Parasitic re-turn-on and the need for negative V_{GS} voltage

It is well known that in a half-bridge configuration, during hard-switching turn-on of either the low-side or high-side MOSFET, the high dV/dt of the switching node induces a Miller current; this current flows through the C_{GS} and C_{GD} gate capacitances of the complementary device and pulls up its gate-to-source voltage. This induced voltage at the gate must be kept below the $V_{(GS)th}$ gate threshold voltage to avoid extra losses or severe re-turn-on. An example is provided in **Figure 4**; it refers to an hard-switching turn-on transition at 16 A of Infineon's **CoolSiC™ IMZA65R048M1H** driven with unipolar 18 V and with 6.8 Ω on/off gate resistors; the platform used for the measurement is EVAL_2EDB_HB_SiC_Si (see **[1]**) in reverse double pulse.

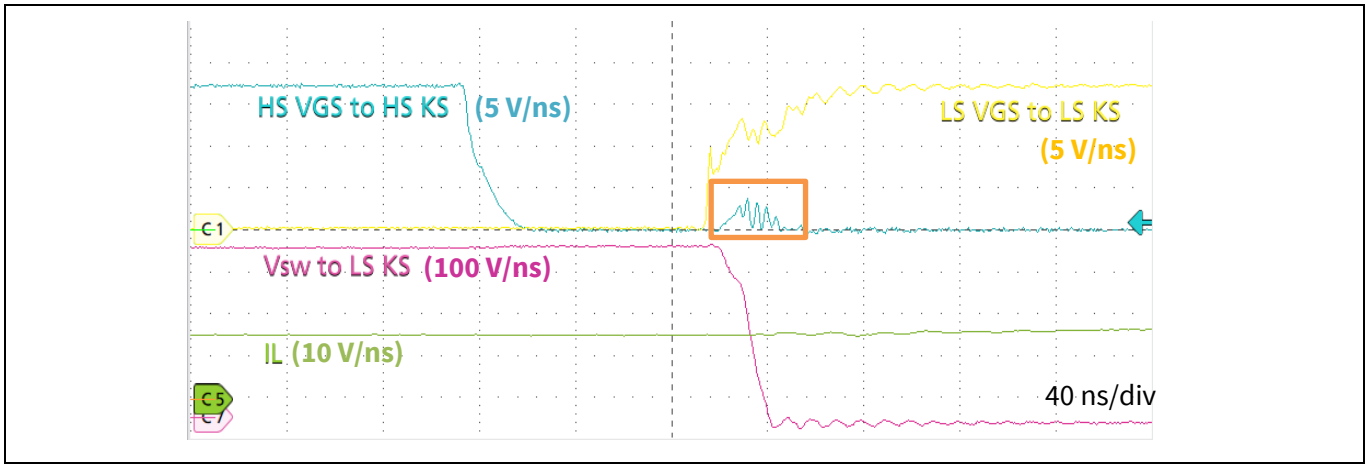

Figure 4 Induced gate-to-source voltage during hard-switching of the complementary switch

Thanks to the good re-turn-on immunity and the relatively high gate threshold (min. 3.5 V) of Infineon's CoolSiC™, this induced gate-to-source voltage is usually not critical and therefore unipolar 18 V driving is recommended. Eventually, for more safety margin, bipolar supply can be considered with a negative voltage down to -1.5 V (Infineon SiC allows -2 V static operating V_{GS} and it is good practice to keep some margin for undershoots in the auxiliary supply). Per default configuration, KIT_1EDB_AUX_SiC allows bipolar driving with a regulated 18 V positive rail and unregulated -1 V rail at 10 mA (see **Figure 10**) that is roughly the current required to drive Infineon's IMZA65R048M1H at 100 kHZ.

Not all available SiC on the market has a good re-turn-on immunity (see **Figure 5**) due to poor C_{GD}/C_{GS} ratio and/or low $V_{(GS)th}$ threshold. Clearly, for those devices the use of bipolar driving is strongly recommended (see recommendation in **Figure 2**); whenever this is not possible due to degradation phenomena at negative V_{GS}, the use of drivers with a Miller clamp feature is needed.

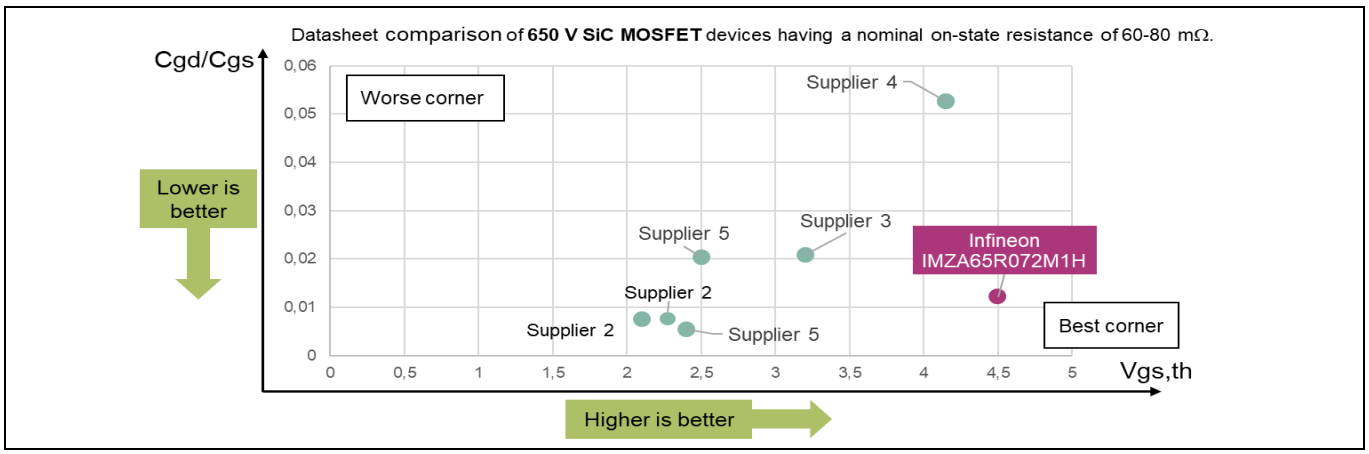

Figure 5 Re-turn-on immunity of several 650 V SiC MOSFETs

2 Board description

2.1 Schematic and general description

The schematic of KIT_1EDB_AUX_SiC is shown in **Figure 6**.

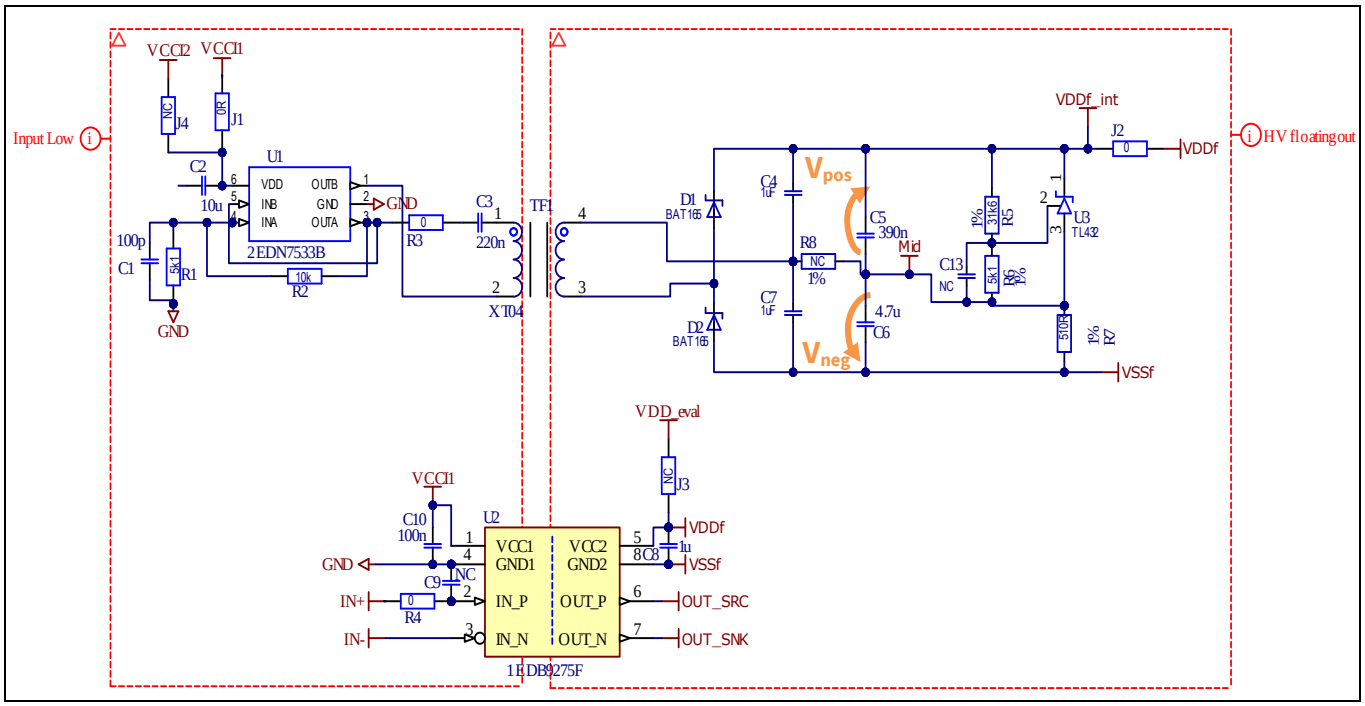

Figure 6 KIT_1EDB_AUX_SiC schematic

The board includes the EiceDRIVER™ 1EDB9275F, a single-channel isolated gate driver IC featuring 3 kV_{RMS} input-to-output isolation thanks to Infineon's coreless transformer (CT) technology. This driver is optimized to drive high-side SiC devices and can be used in combination with EiceDRIVER™ 1EDN9550B for low-side driving as described in Section 6.4 of **[2]**.

The circuit on the top side of the schematic is the auxiliary supply that operates as an isolated DC-DC converter and provides the floating supply V_{DDf} to V_{SSf} to the secondary side of EiceDRIVER™ 1EDB9275F.

The board operates by default with a single supply voltage (V_{CCI1}), which supplies both the EiceDRIVER™ 1EDB9275F primary side and the isolated DC-DC converter; alternatively, different voltages (V_{CCI1} and V_{CCI2}) can be used by disconnecting the jumper J1 and shorting the jumper J2.

The operating voltages of the auxiliary supply are shown in **Figure 7** for ease of understanding.

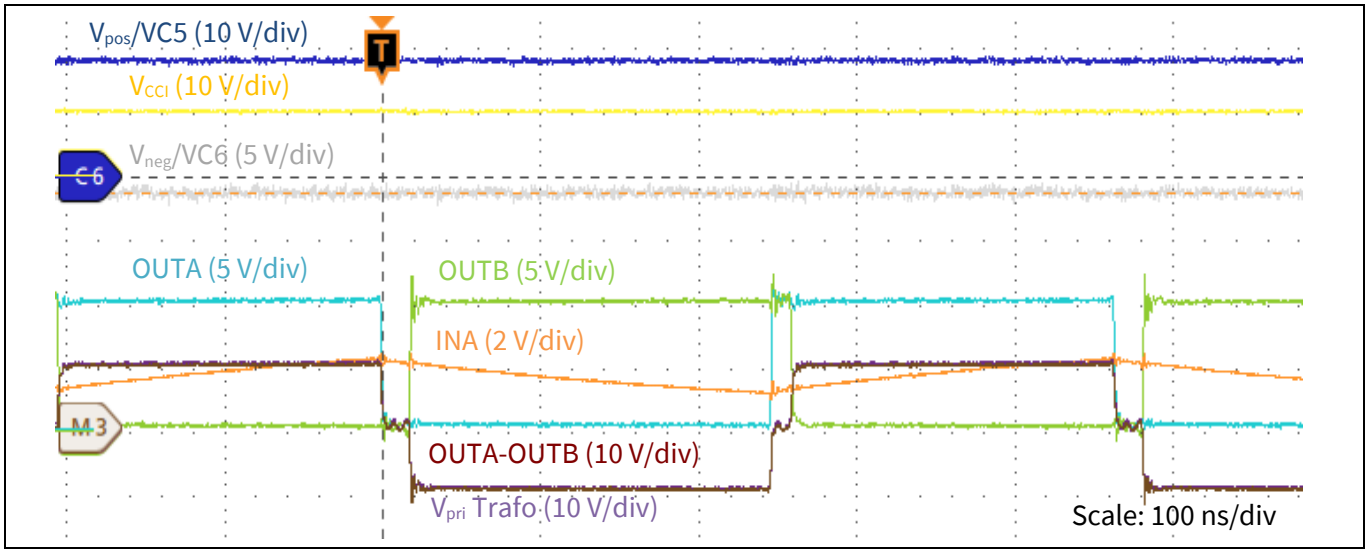

Figure 7 Operating waveform of the auxiliary supply for the default configuration with V_{CCI} = 10 V and V_{pos} = 18 V, V_{neg} = -1 V

The V_{CCI} voltage (10 V by default) is shaped by the EiceDRIVER™ 2EDN7533B in a three-level waveform (see brown, OUTA-OUTB) with levels V_{CCI1}, 0 V, -V_{CCI1}; the frequency and duty cycle are set via feedback components C1, R1 and R2 to 2.1 MHz and 50 percent duty cycle. With 1:1 ratio, the XT04 transformer is only responsible for isolation and therefore the signal on the transformer's secondary side still shows an amplitude equal to two times V_{CCI1}. This voltage is rectified by D1 and D2 Schottky diodes and with 50 percent duty cycle the capacitors C4 and C7 charge to approximately V_{CCI} while C5 and C6 charge to a voltage set by the TL432 shunt regulator (see blue V_{pos}, gray V_{neg}). If the midpoint is connected to the MOSFET source, then C5 and C6 represent the positive and negative bipolar supplies, respectively; by default, the positive rail is regulated to 18 V and the remaining unregulated portion stays across C6 (see Section **3.1.1**).

2.2 Auxiliary ring oscillator concept

The auxiliary supply is based on the EiceDRIVER™ 2EDN7533B, a two-channel non-isolated gate driver IC. This driver has inverting outputs and one of them (OUTA) is feedbacked to the input to create a "ring oscillator".

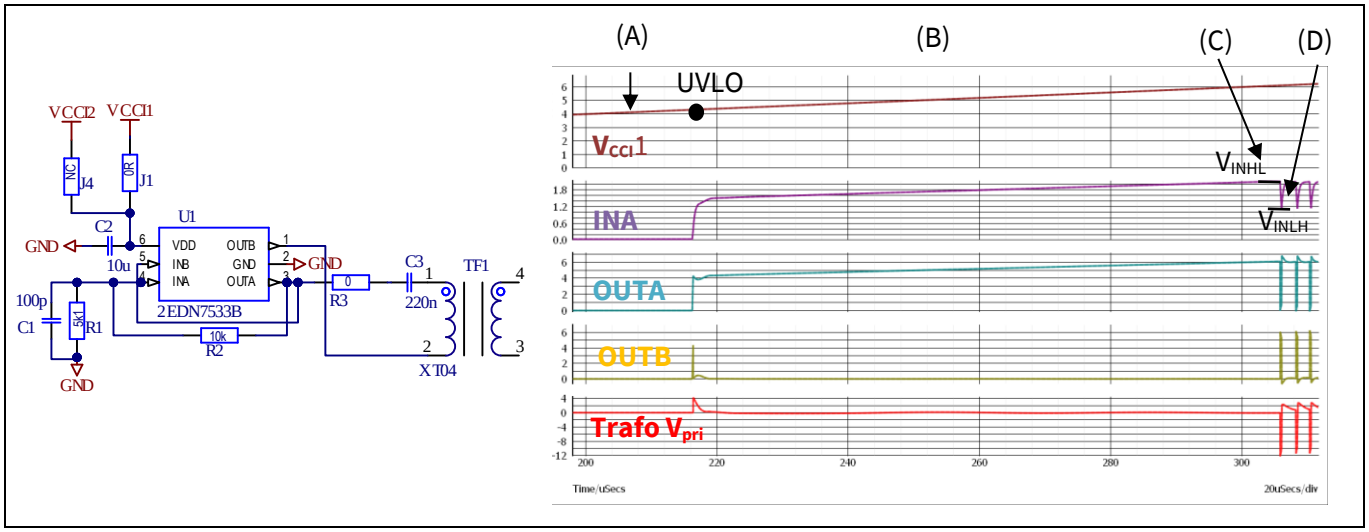

Figure 8 Ring oscillator behavior

The oscillator behavior of the circuit is explained by referring to the start-up behavior shown in **Figure 8**:

(A) When the supply V_{CCI} is below the 4 V undervoltage lockout (UVLO) level of the EiceDRIVER™ 2EDN7533B, both outputs are actively held low by the driver.

(B) When the supply reaches the UVLO the driver wakes up; due to the discharged capacitor C1 (INA low) and the inverting nature of the driver, OUTA goes high and OUTB stays low (OUTA is indeed directly feedbacked on INB and is high). At the same time, high OUTA starts to charge C1 via the resistive feedback path; INA increases.

(C) When INA reaches the driver input high threshold (V_{INH} = 2.1 V), the EiceDRIVER™ 2EDN7533B drives OUTA (and then INB) low. Consequently, OUTB goes high after one propagation delay period (19 ns typ.). At the same time, INA is discharging on the parallel R1//R2.

(D) When INA reaches the driver low input threshold (V_{INHL} = 1.2 V), everything is reversed again; the oscillation is then established.

2.3 Dimensioning of the bipolar split V_{pos}/V_{neg}

As introduced in Section **2.1**, the shunt regulator TL432 is responsible for the bipolar V_{pos}/V_{neg} split by regulation of the positive rail. Alternatively, whenever the 1 percent regulation is not required and the required V_{pos} and V_{neg} are not too unbalanced ($V_{pos}/2\ V_{CCI}$ less than 80 percent as a rule of thumb), the split can be obtained by simply tuning the duty cycle of the OUTA-OUTB signal to the desired $V_{pos}/2\ V_{CCI}$ ratio. In this case the TL432 regulator (U3) and surrounding resistors (R5, R6 and R7) can be removed and R8 should be shorted. This use case is not considered here; however, waveform examples and indications of proper dimensioning can be found in **Appendix A**.

In the default configuration, TL432 regulates the positive rail to 18 V but a different regulation is possible by simply adapting either R5 or R6. When active, the regulator establishes 2.5 V between its reference node and cathode and therefore on R6; the target positive voltage V_{pos} can be obtained by a simple voltage divider as follows:

$$\frac{R6}{R5 + R6}\ \mathrm{Vpos} = 2.5\ \mathrm{V} \tag{1}$$

It is important to ensure that a cathode–anode current higher than 0.7 mA polarizes the TL432 to ensure proper regulation; this means correctly setting the value of R7 from equation (2). As it can be seen in Section **3.1.1**, the voltage drop Δ target load on the negative rail depends on the auxiliary load, and a margin of 2 V is reasonably considered here for R7 dimensioning. It is not recommended to increase R7 further, because this would not have any benefit but rather would have a negative impact on the efficiency.

$$R7 < \frac{\mathrm{Vneg}_{\mathrm{target\,load}}}{0.7\ \mathrm{mA}} = \frac{2\ \mathrm{VCCI} - \mathrm{V}_{\mathrm{pos(reg)}} - \Delta_{\mathrm{target\,load}}}{0.7\ \mathrm{mA}} \tag{2}$$

By default, KIT_1EDB_AUX_SiC is dimensioned as per Conf. A to drive Infineon CoolSiC™. **Table 1** also shows the dimensioning for different bipolar splits (Conf. B, C and D), relevant for driving SiC MOSFETs from other suppliers, as previously shown in Section **1**. Relevant data such as voltage regulation and efficiency for the different configurations can be found in Section **3**.

Table 1 Recommended dimensioning for different bipolar voltage levels

Conf.	$V_{pos,\ regulated}$	V_{neg} at 10 mA[1]	V_{CCI}	R5, R6, R7
A	+18 V	-1 V	10 V	31.6 kΩ, 5.1 kΩ, 510 Ω
B	+18 V	-5 V	12 V	31.6 kΩ, 5.1 kΩ, 3 kΩ
C	+15 V	-4 V	10 V	31.6 kΩ, 6.2 kΩ, 2.4 kΩ
D	+20 V	-3 V	12 V	31.6 kΩ, 5.1 kΩ, 1 kΩ

[1]The negative rail is unregulated; see Section **3.1.1** for V_{neg} behavior with the auxiliary load.

Attention:
1. Do not use Conf. B, C or D with Infineon CoolSiC™ MOSFETS because of voltage ratings (static V_{GS} below -2 V is not allowed). For more information, please refer to the respective product datasheet.

2. When using a V_{CCI} supply voltage higher than 10 V (e.g., Conf. B and D), the supply voltage delivered to the EiceDRIVER™ 1EDB9275F would exceed its maximum rating (20 V_{VDD} max. operating). In this case, a different gate driver with higher output voltage capability should be used; one recommendation is the equivalent and pin-out compatible EiceDRIVER™ 1ED3124MU12F.

2.4 Use case example and mounting

The board is intended to replace a single-channel isolated gate driver IC on a main board, as shown in **Figure 9**. With 2.8 mm thickness, the KIT_1EDB_AUX_SiC can be directly soldered into the 8-pin DSO 150 mil footprint, with the shortest possible connection to the main board; this is important for the connection to the gate resistance to minimize the gate loop toward the SiC MOSFET. Alternatively, proper connectors with 1.27 mm pitch could also be used.

Compared to the standard 150 mil DSO-8 footprint, the output ground pin (GNDO) on the main board is replaced with the midpoint of the auxiliary supply; this enables the testing with bipolar supply. It also includes an additional input supply pad (V_{CCI2}) that can eventually provide flexibility to supply the EiceDRIVER™ 1EDB9275F input side and the auxiliary circuit with different voltages.

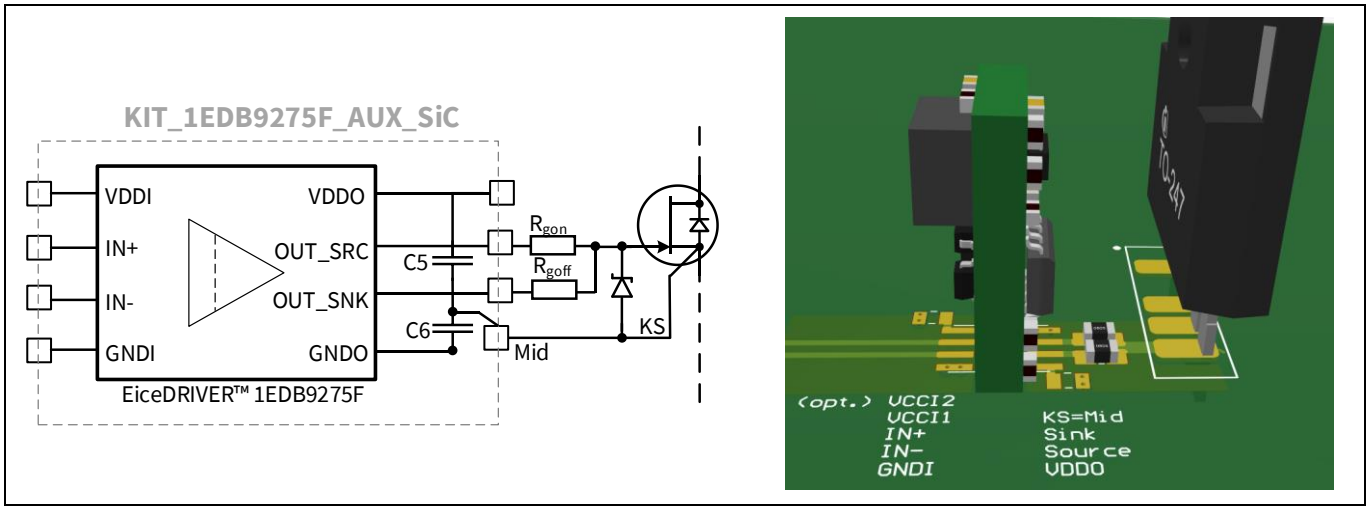

Figure 9 Mounting of KIT_1EDB_AUX_SiC on a main board

3 Experimental results

3.1 Output regulation

As previously described, by default only the positive rail is regulated while the negative rail is not. V_{neg} therefore changes with the auxiliary load that depends on the switching frequency and on the selected SiC MOSFET (by means of its charge). Additionally, if the V_{CCI} input voltage is different from the nominal value due to some inaccuracy, this is also reflected in the value of V_{neg}; in the worst case, if V_{CCI} gets too low it will definitely affect the regulation. Those two aspects are investigated in the next two subsections, where the output regulation with load and the output regulation with inaccurate V_{CCI} are shown.

3.1.1 Output regulation with load

Figure 10 shows the behavior of the auxiliary output voltages V_{pos} and V_{neg} with different loads. The characterization over different loads is performed on the auxiliary circuit alone by removing the EiceDRIVER™ 1EDB9275F and simply using resistors as loads. The voltages are measured with a 6½ digit multimeter.

Note: On this board the regulation is made on the positive rail but alternatively it could be performed on the negative rail by moving the regulator and adapting its surrounding resistors. In the second case, if TL432 is properly polarized, V_{neg} would be 1 percent regulated and V_{pos} would become load-dependent and show a load-dependent drop similar to the one measured in **Figure 10** for V_{neg}. This drop is in fact only given by the primary-to-secondary parasitics and components (rectifier diodes, transformer).

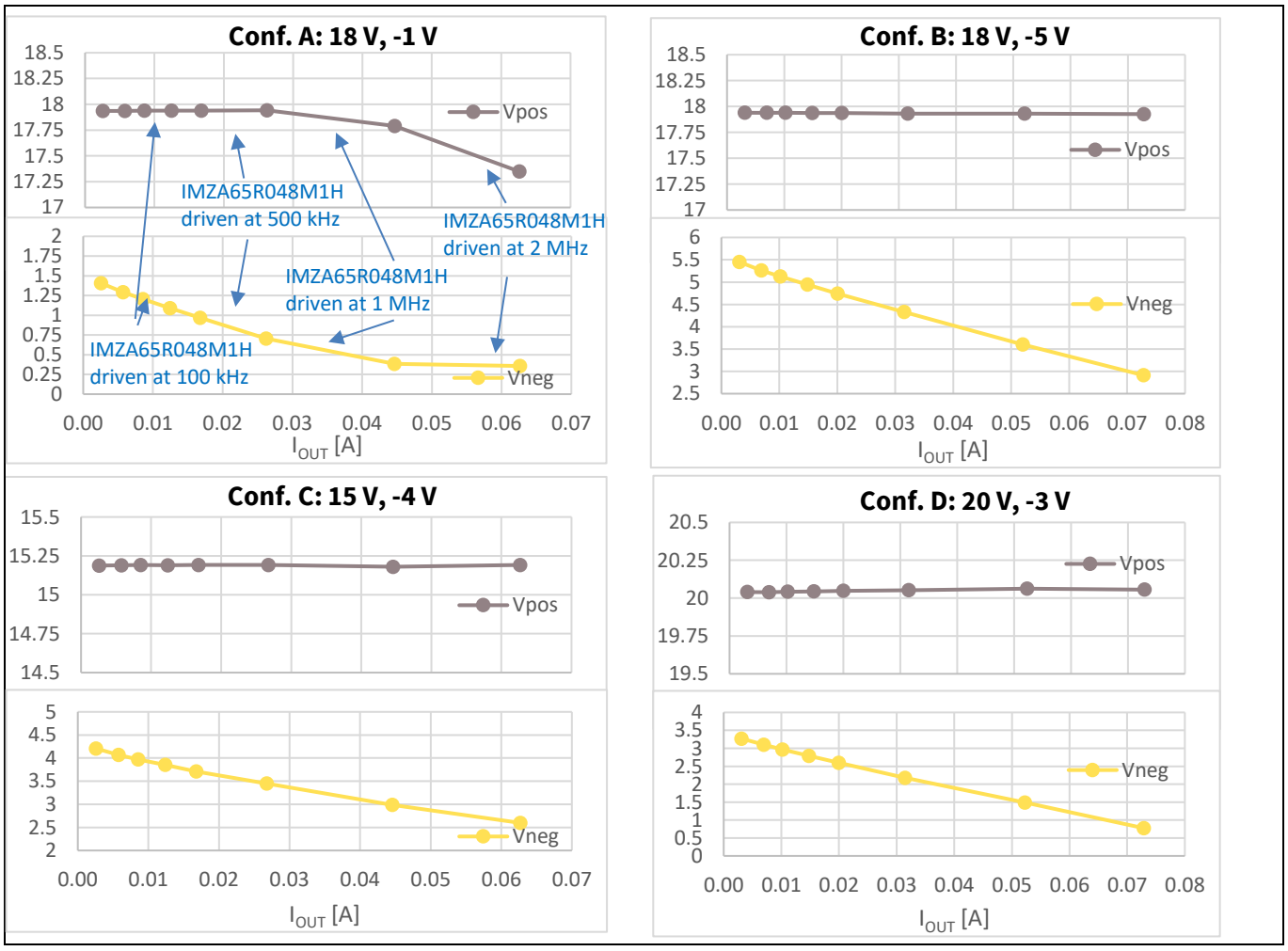

Figure 10 Auxiliary output voltage V_{pos}, V_{neg} over output current load I_{OUT}

Experimental results

For Conf. A, the 1 percent positive rail regulation is lost around 35 mA output current because the negative voltage (voltage on R7) becomes very low and therefore the minimum 0.7 mA polarizing current for the TL432 is not ensured anymore. This is normal due to the very large $V_{tot}/2$ V_{CCI} ratio considered for Conf. A; a compromise should then be considered and eventually accepted. 35 mA load current covers most of the potential use cases for this board; e.g., it allows driving Infineon's **CoolSiC™ IMW65R048M1H** up to 1 MHz with 1 percent V_{pos} regulation. If higher current is needed, then R7 can be further reduced.

Clearly, because of the tight split, an inaccuracy of the auxiliary supply could also impact the regulation for Conf. A more easily compared to the other configurations. As can be seen in Section **3.1.2**, Conf. A is recommended to supply the auxiliary circuit with a V_{CCI} voltage with at least 2 percent accuracy.

Figure 11 also shows the auxiliary output voltage behavior with different input currents. This is just a different view of **Figure 10**, and is provided for convenience because, when driving a SiC device with the KIT_1EDB_AUX_SIC, the user can more easily read I_{IN} from the DC power supply providing V_{CCI}. Here the I_{IN} mapping has been provided for Conf. A when driving Infineon's CoolSiC™ IMW65R048M1H at different frequencies. It should be mentioned that, in this measurement, no bulk voltage or current is applied to the switch and therefore I_{OUT} was only the current needed to turn on the Q_{GS}; when bulk voltage is applied, the (small) contribution made by Q_{GD} is added, and when current is applied a Q_{GS} contribution from current is also added.

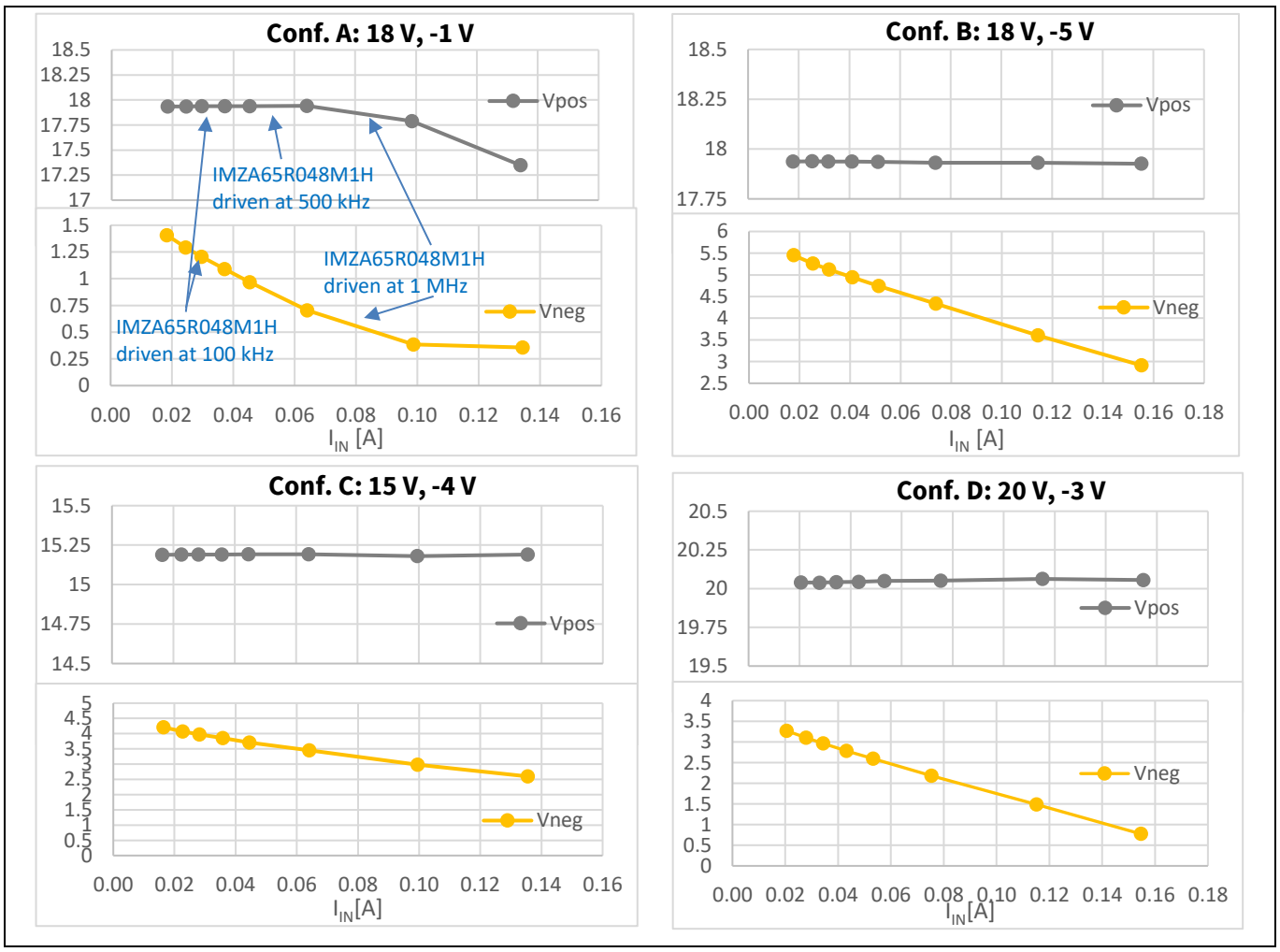

Figure 11 Auxiliary output voltage V_{pos}, V_{neg} over output current load I_{IN}

3.1.2 Output regulation with input supply voltage V_{CCI}

The input supply of the auxiliary DC-DC converter will have a certain inaccuracy that should be considered when looking at the voltage regulation. **Figure 12**, **Figure 13**, **Figure 14** and **Figure 15** show the output regulation for the different configurations considering a typical 5 percent accuracy. A 2 percent accurate V_{CCI} supply is recommended for Conf. A and could also be adopted for Conf. D only in case of heavy load needs.

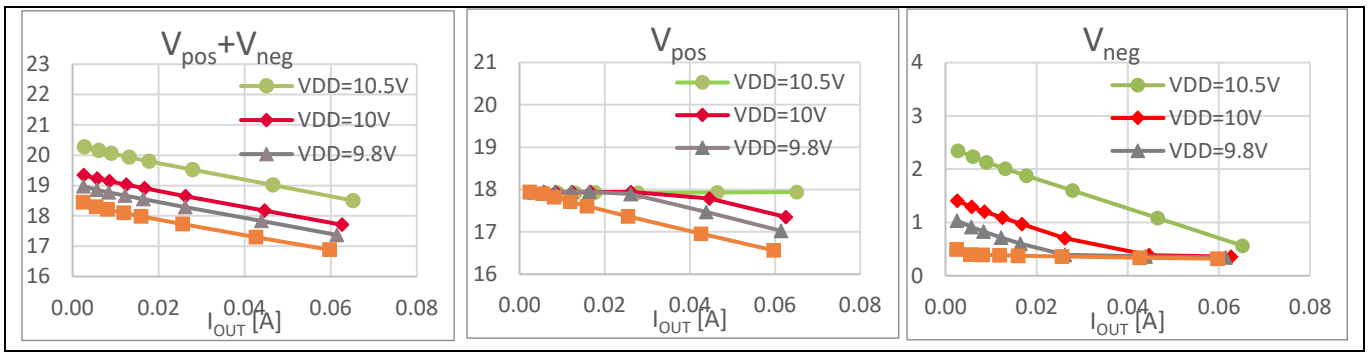

Figure 12 Regulation over output current with 2 to 5 percent inaccurate V_{CCI} voltages for Conf. A (18 V, -1.5 V)

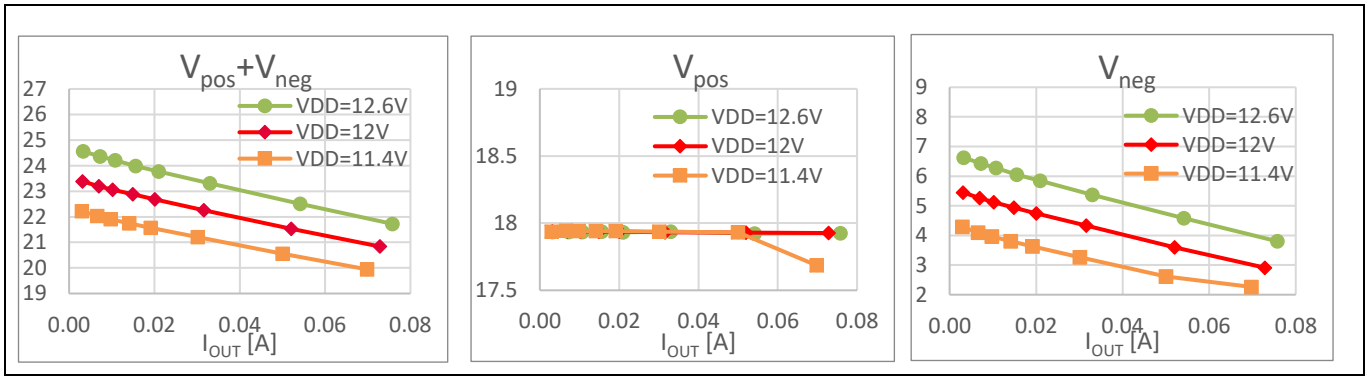

Figure 13 Regulation over output current with 5 percent inaccurate V_{CCI} voltages for Conf. B (18 V, -5.5 V)

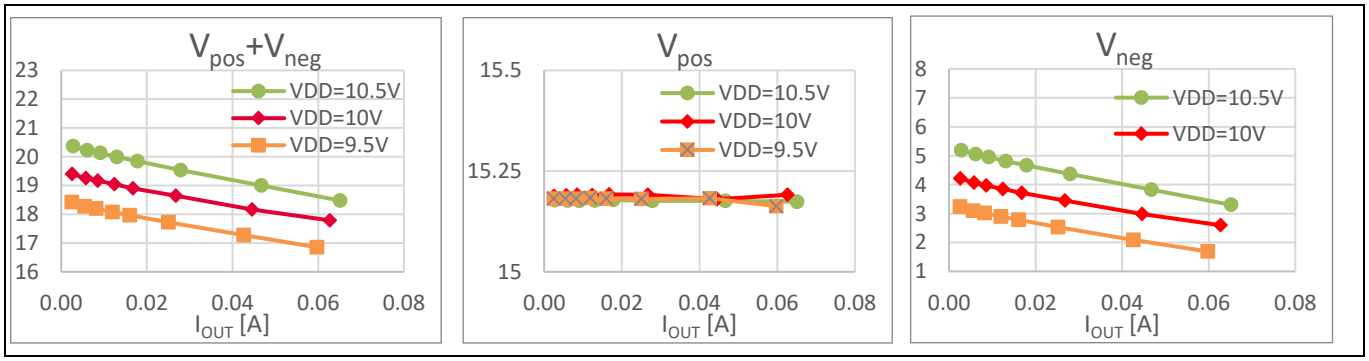

Figure 14 Regulation over output current with 5 percent inaccurate V_{CCI} voltage for Conf. C (15 V, -4.5 V)

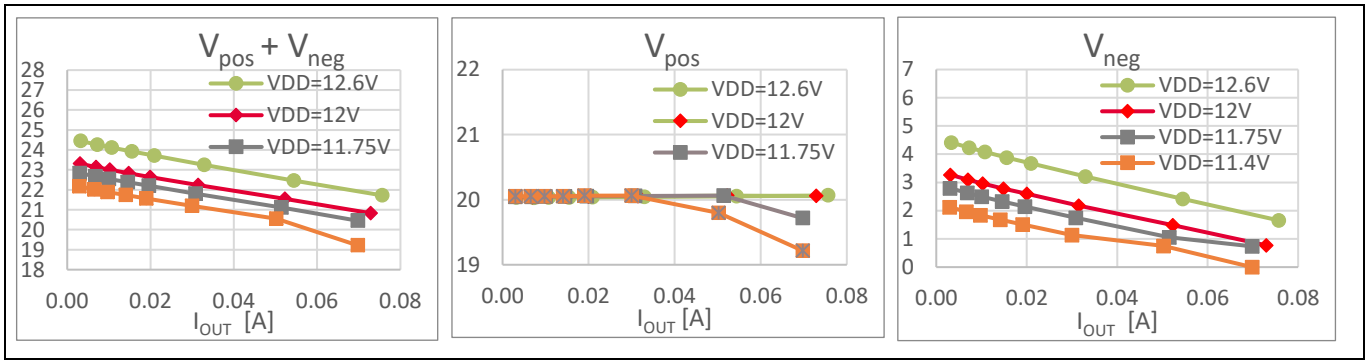

Figure 15 Regulation over output current with 2 to 5 percent inaccurate V_{CCI} voltage for Conf. D (20 V, -3.5 V)

3.2 Efficiency

Figure 16 shows the efficiency for Conf. A, B, C and D with output power and input supply V_{CCI}. As shown previously for the voltage regulation, the efficiency is measured with the auxiliary circuit alone without the EiceDRIVER™ 1EDB9275F; simple resistors have been used as load for the auxiliary supply. 0.1 Ω shunts are used for input and output current measurement, and a 6½ digit multimeter is used to measure the voltages.

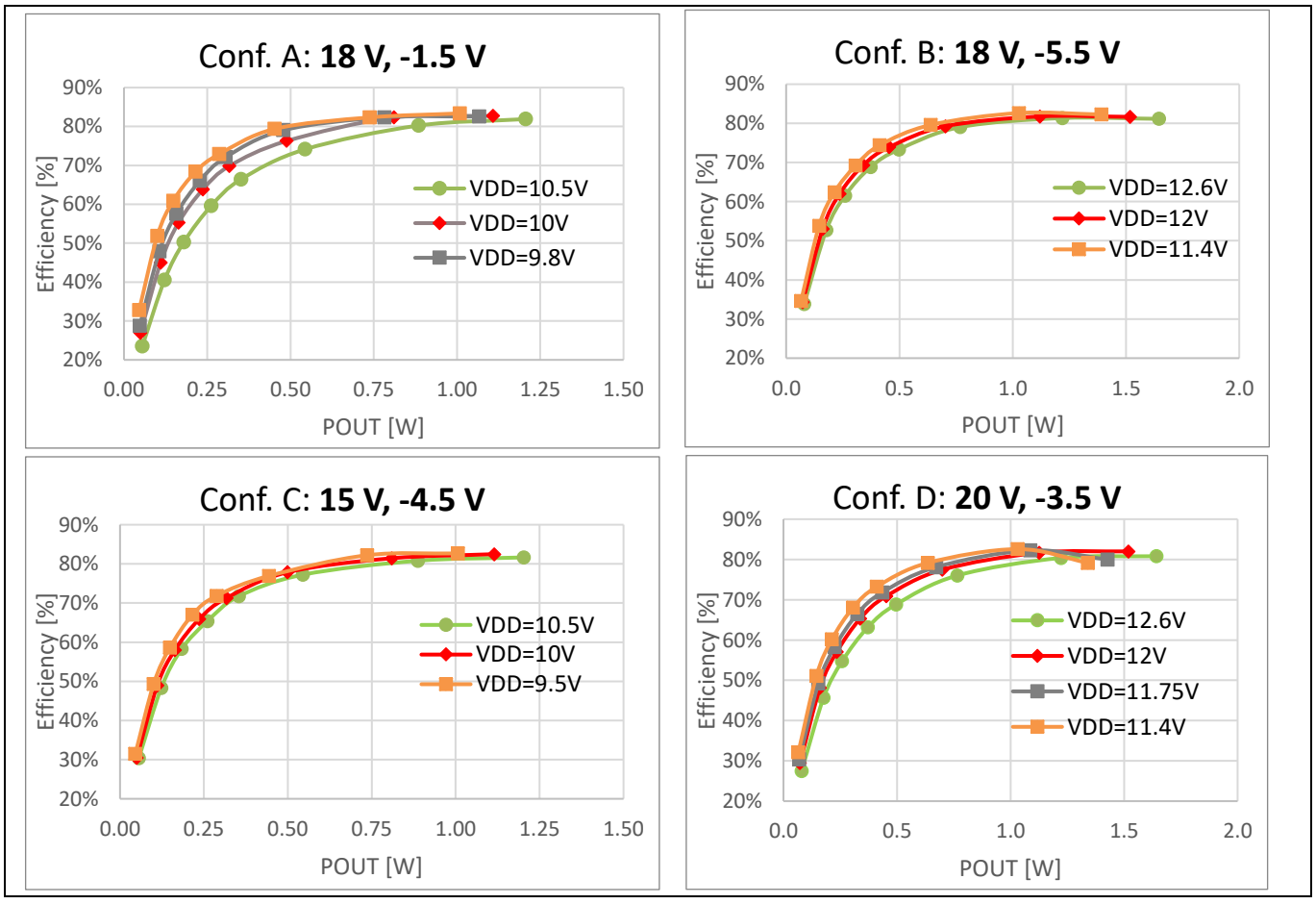

Figure 16 Efficiency over output power for inaccurate 2 to 5 percent V_{CCI}

A different view with the efficiency over output current and input current is provided in **Figure 17**.

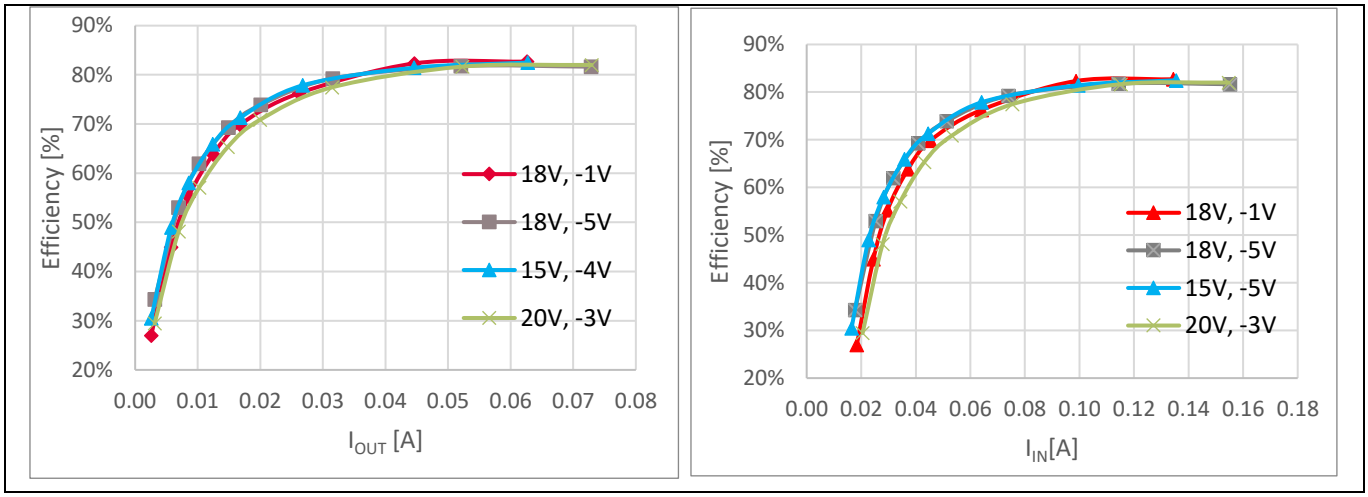

Figure 17 Efficiency at nominal V_{CCI} over output current (left) and input current (right)

The efficiency graph with input current in particular allows easy reading for the user, who can simply read I_{IN} from the DC power supply while providing V_{CCI}. Here the I_{IN} mapping has been provided for Conf. A when driving Infineon's CoolSiC™ IMW65R048M1H at different frequencies; the same considerations as in Section **3.1.1** apply.

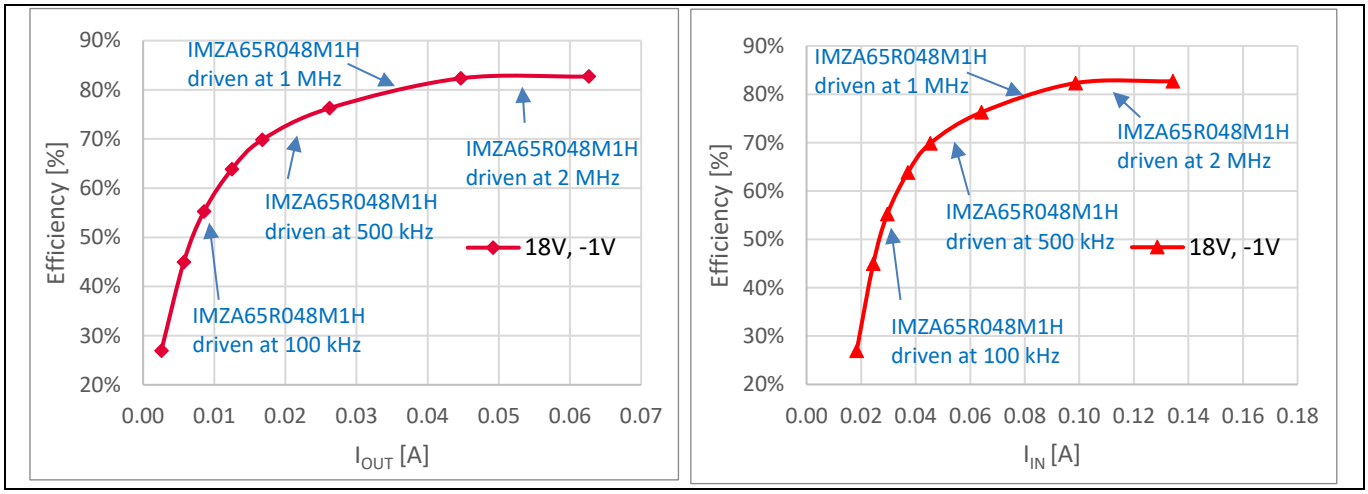

Figure 18 Efficiency contextualized to drive Infineon's CoolSiC™ IMZA65R048M1H with recommended 18 V positive voltage

3.3 Operating waveforms

The operating waveforms for the auxiliary supply are shown in **Figure 19** and **Figure 20**. The switching frequency is selected to provide the highest efficiency while still fulfilling the 6 V/µs saturation limit of the XT04 transformer. The duty cycle of the signal on the transformer (see purple line) is set to almost 50 percent with nominal 10 V V_{CCI} and is slightly smaller with 12 V V_{CCI}.

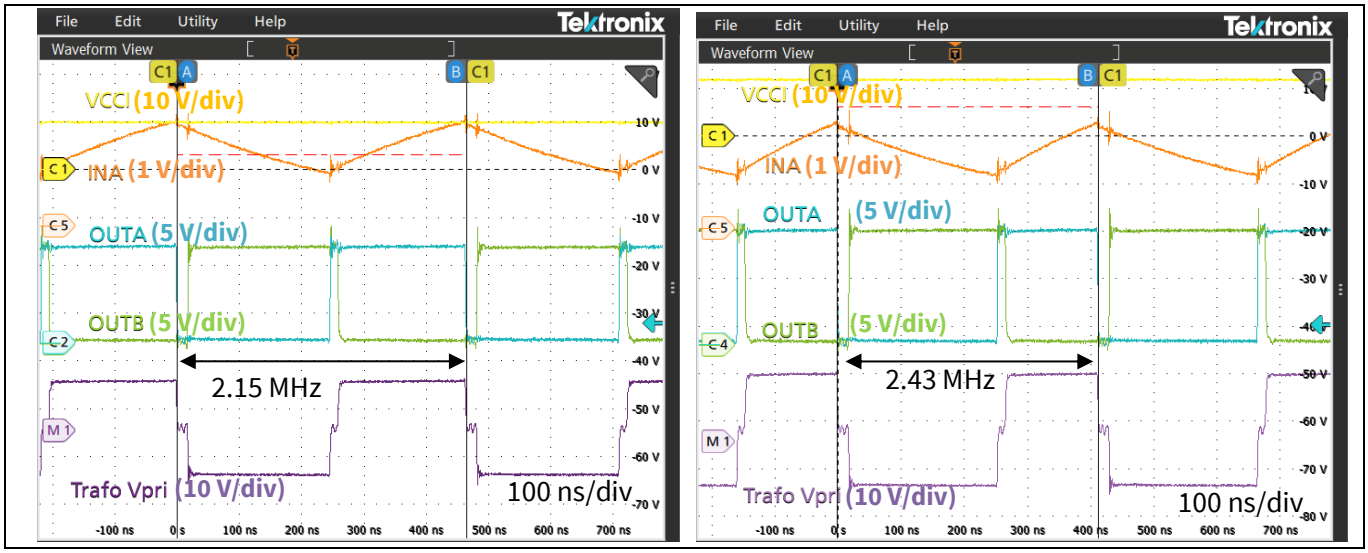

Figure 19 Auxiliary supply operating waveform at V_{CCI} = 10 V and V_{CCI} = 12 V

Figure 20 shows the gate-to-source voltage waveforms when driving Infineon's CoolSiC™ in bipolar Conf. A with the KIT_1EDB_AUX_SiC. This measurement only intends to provide a look and feel of how the on and off gate voltage behaves with the different SiC and switching frequency; however, for the exact voltages it is recommended to refer to Section **3.1.1** and in particular to **Figure 10** and **Figure 11**.

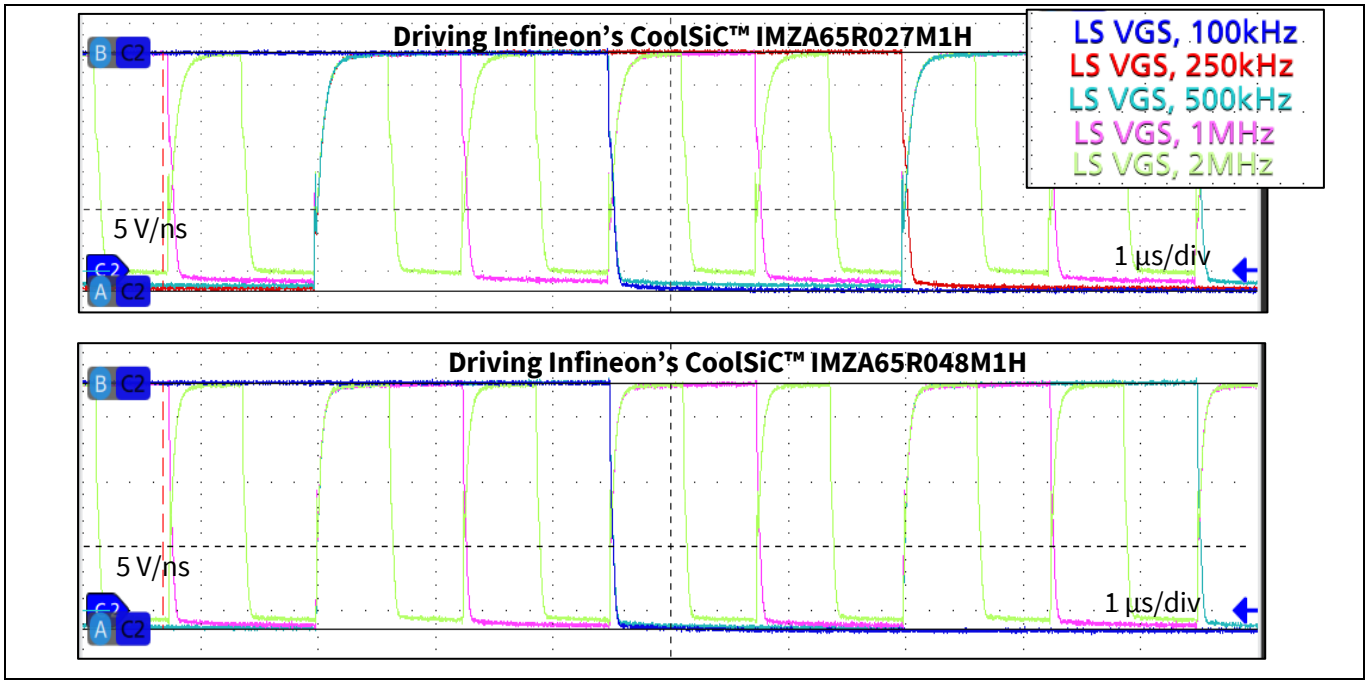

Figure 20 Operating waveforms – driving Infineon's CoolSiC™ IMZA65R027M1H and IMZA65R048M1H

3.4 Start-up behavior

The power supply is designed to work at nominal V_{CCI}; however, when the input supply is ramping up and down (e.g., start-up, shutdown) the auxiliary power supply could work in an unwanted condition. The power supply must be able to leave this operation mode safely. **Figure 21** and **Figure 22** show an auxiliary supply start-up with, respectively, a fast and slow V_{CCI} ramp in high-load condition (270 Ω load resistor, 150 mA input current); high load is the most critical case to look at.

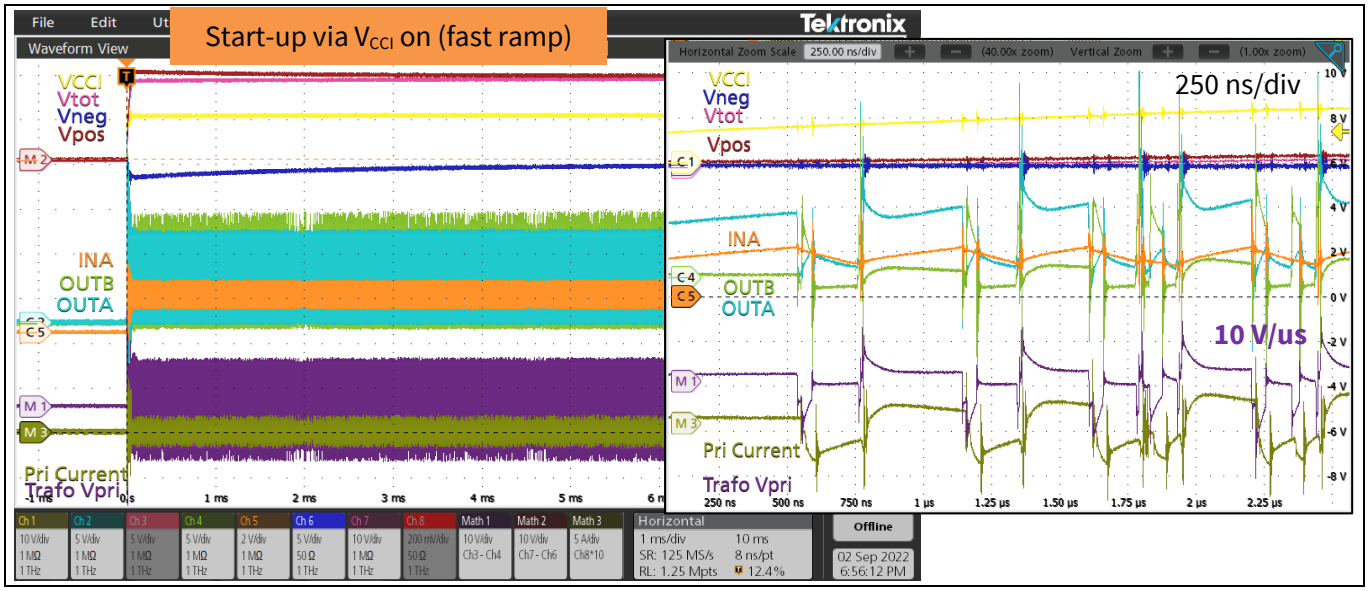

Figure 21 Fast start-up of auxiliary supply alone in Conf. A with a 270 Ω load

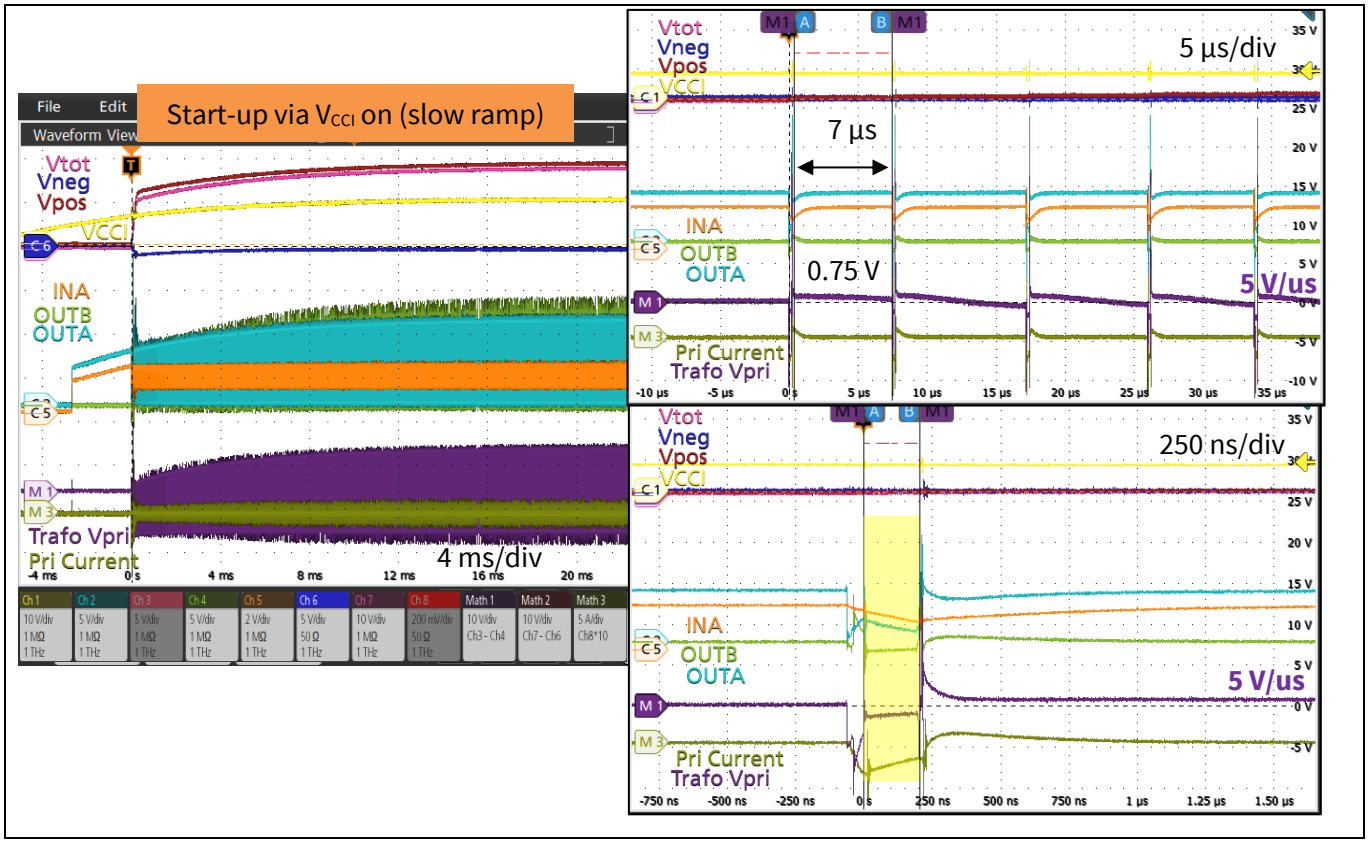

Figure 22 Slow start-up of auxiliary supply alone in Conf. A with a 270 Ω load

Experimental results

Three aspects should be checked during start-up:

a. If the reverse current stress can be handled by the driver

b. If the transformer is not saturating due to low-frequency operation

c. If the generated positive and negative rail voltages show undershoots or overshoots that are not critical for the driven SiC MOSFET

a. Reverse current conditions are caused by the high current (green, waveform M3) flowing in the auxiliary during start-up. Reverse current can be avoided by a limiting resistor (R3); however, in this design R3 is set to 0 Ω for best voltage regulation and efficiency thanks to the high reverse current robustness of EiceDRIVER™ 2EDN7533B. On this board, the worst reverse current condition is highlighted with the yellow frame in the detail views of **Figure 21** and **Figure 22**; here a reverse current of around 3 A on average flows into the driver nMOS body diode of channel B (OUTB is at -0.8 V) for 150 ns and 202 ns respectively in the fast and slow start-up case. This current is only limited by the parasitics and by the gate driver's output stage resistances. The reverse current is caused by an unwanted toggling of INB, induced by the high primary current. During the discharging phase of INA, OUTB (green, waveform C4) is supposed to be high and OUTA (blue, waveform C2) is supposed to be low; however, the high primary current causes a significant voltage drop on the driver output resistance $R_{DS(on),SNKA}$ that brings OUTA (and then INB) above the V_{INLH} threshold (see part highlighted in yellow). Consequently, OUTB is pulled down and this causes the toggling and the induced reverse current.

b. In case of an input supply (V_{CCI}) rising slowly, the auxiliary start-up operates for long time with a supply voltage lower than the nominal value; therefore, it works at a very low switching frequency, as seen in the upper detail view in **Figure 22**. This can become critical for the transformer flux balance; however, in this design the stress on the transformer stays well below the 6 V/µs saturation limit.

c. No significant over- and undershoots are visible on the supply rails. In particular, the ratio of the capacitances C5 and C6 are selected to keep the undershoot above -2 V in Conf. A to respect Infineon's CoolSiC™ static V_{GS} ratings. A complete overview for the different configurations is provided in **Figure 23**.

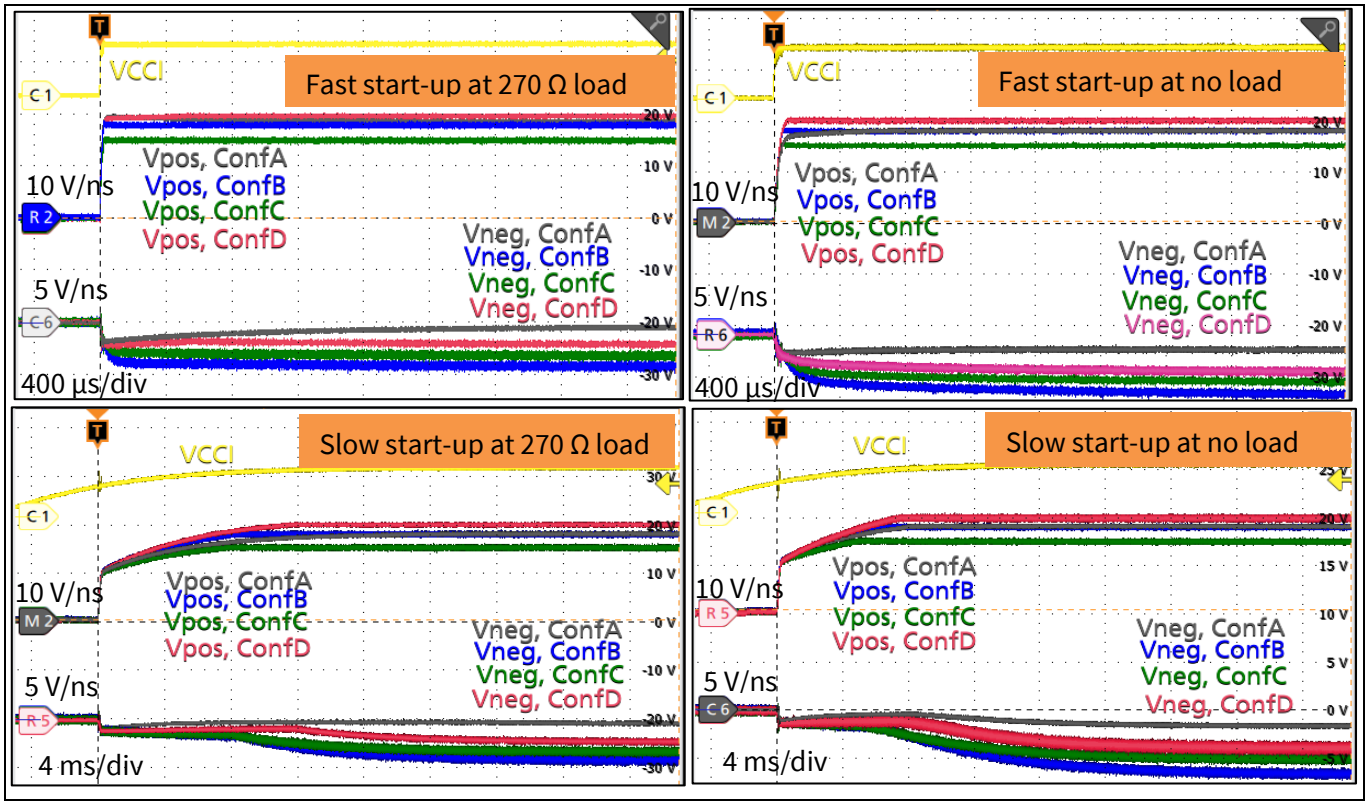

Figure 23 V_{pos} and V_{neg} during fast and slow start-up for Conf. A, B, C and D

For completeness, **Figure 24** shows the start-up of the auxiliary supply when driving a real load: CoolSiC™ IMW65R048M1H switching at 500 kHz in Conf. A.

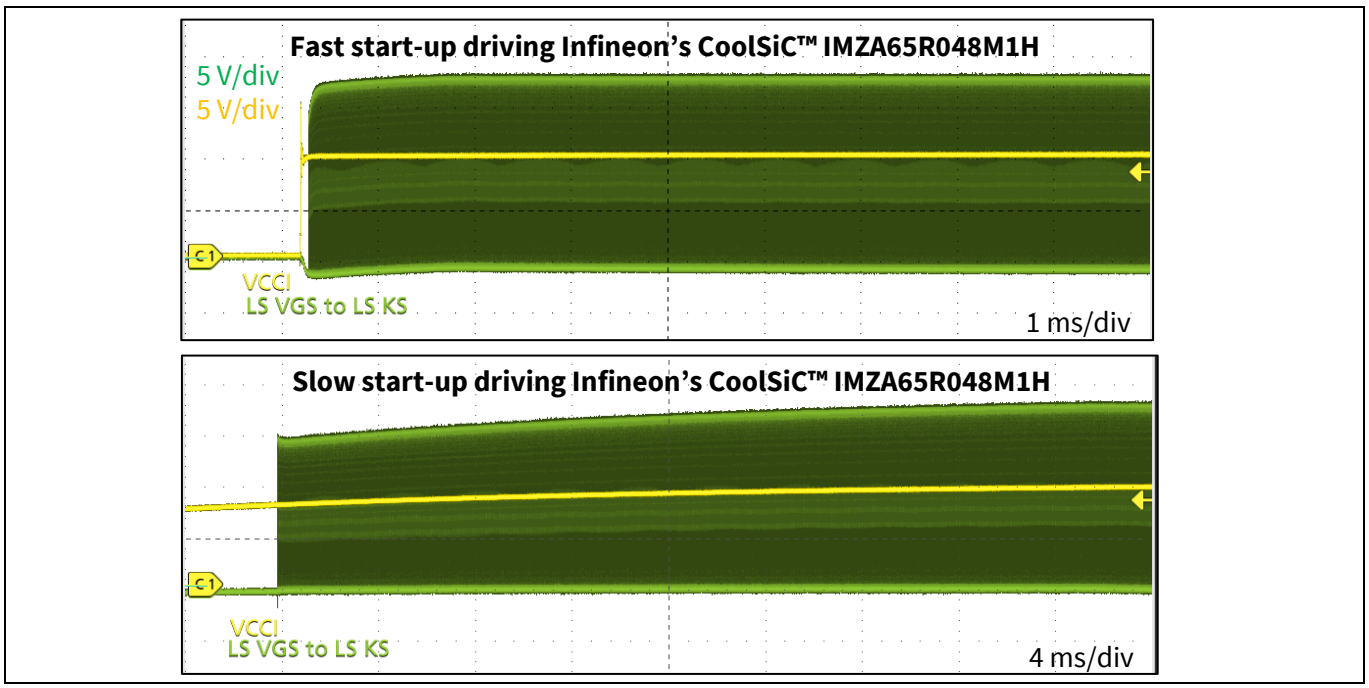

Figure 24 Fast and slow start-up driving Infineon's CoolSiC™ IMZA65R048M1H at 500 kHz in Conf. A

3.5 Shutdown behavior

Figure 25 shows two shutdown scenarios: on the left the input voltage V_{CCI} is turned off via the DC power generator (with its impedance) and on the right side the input voltage is disconnected to emulate a "sudden open". For shutdown the more critical condition is the open load, because the auxiliary takes longer to discharge its output capacitors and then stays longer in this condition.

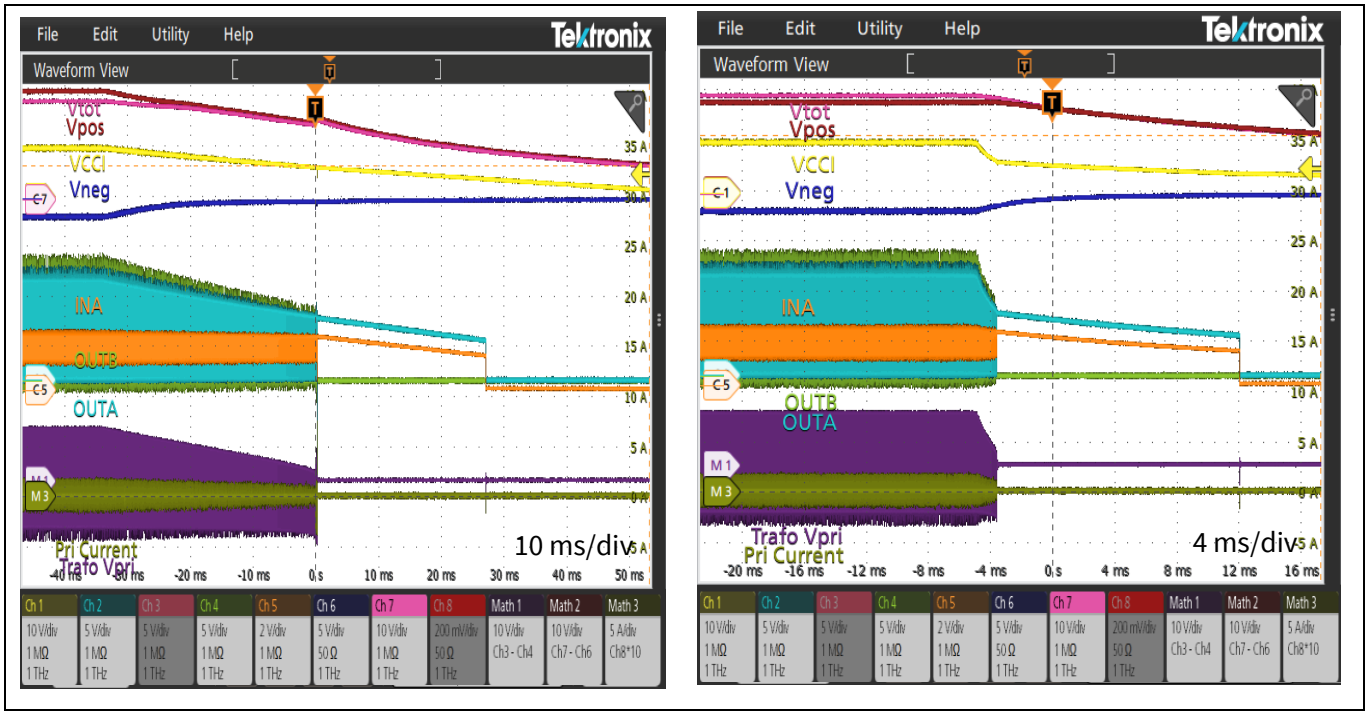

Figure 25 Auxiliary supply shutdown of the auxiliary supply at no load in Conf. A

Figure 26 provides an overview of V_{pos}, V_{neg} during shutdown for the different configurations. No critical under/overshoots are appearing.

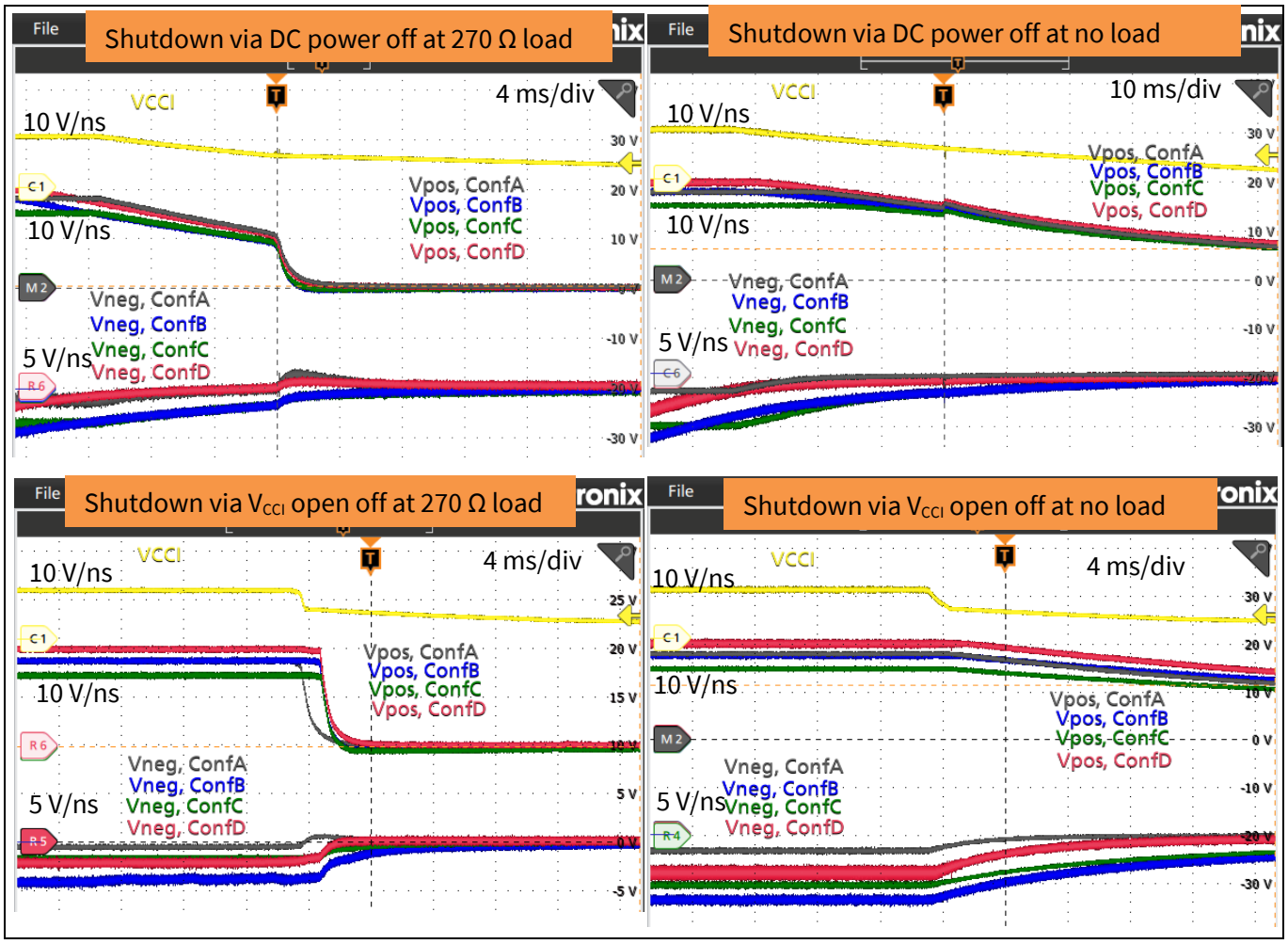

Figure 26 V_{pos} and V_{neg} during shutdown of the auxiliary supply for Conf. A, B, C and D

For completeness, **Figure 27** shows the shutdown of the auxiliary when driving a real load: CoolSiC™ IMW65R048M1H switching at 500 kHz in Conf. A.

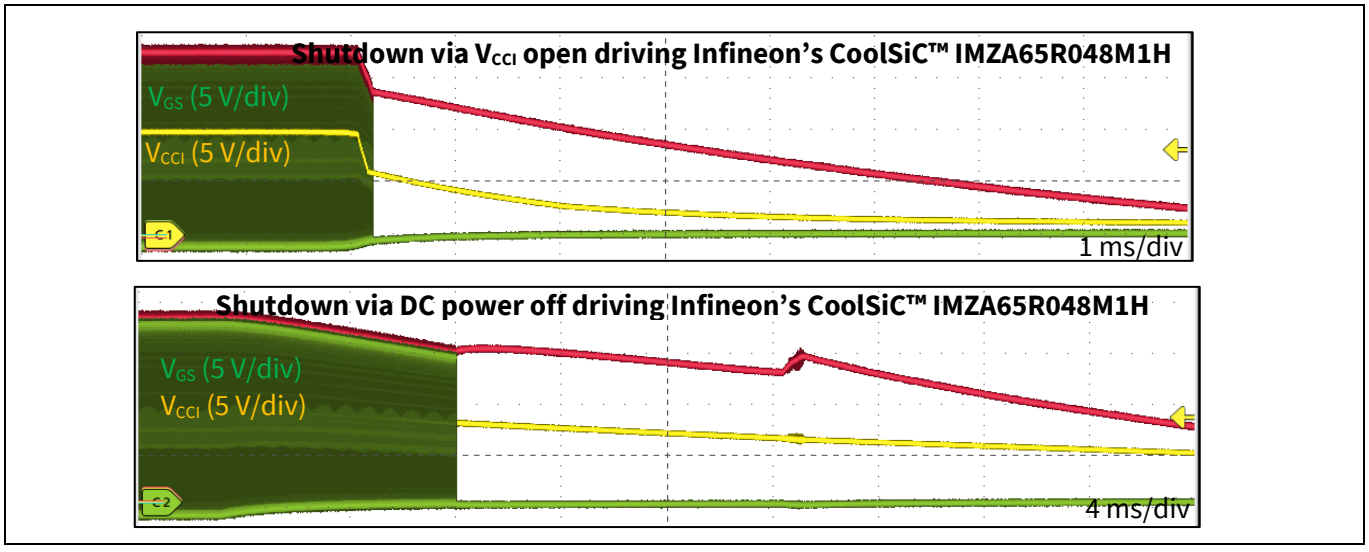

Figure 27 Fast and slow shutdown driving Infineon's CoolSiC™ IMZA65R048M1H at 500 kHz

3.6 Output short circuit

In case of failure in the power stage, the SiC MOSFET gate-to-source and the EiceDRIVER™ 1EDB9275F output stage itself could show a very low impedance toward the auxiliary supply leading to an increased load current; the auxiliary circuit has to survive this special condition.

Figure 28, **Figure 29** and **Figure 30** show what happens on the auxiliary supply when its output (V_{tot}, V_{pos} and V_{neg}, respectively) is short-circuited. The auxiliary survives in the three stress conditions without prolonged saturation of the main transformer and without IC failure.

The worst stress is represented by the short circuit of the complete output (V_{tot}) of the auxiliary circuit. In this case, the high current induces reverse current events like the situation described in Chapter 3.4 for the start-up. Also in this case, thanks to the high reverse current robustness of EiceDRIVER™ 2EDN7533B, the driver can handle this high-stress condition without the need for a limiting current resistor (R3).

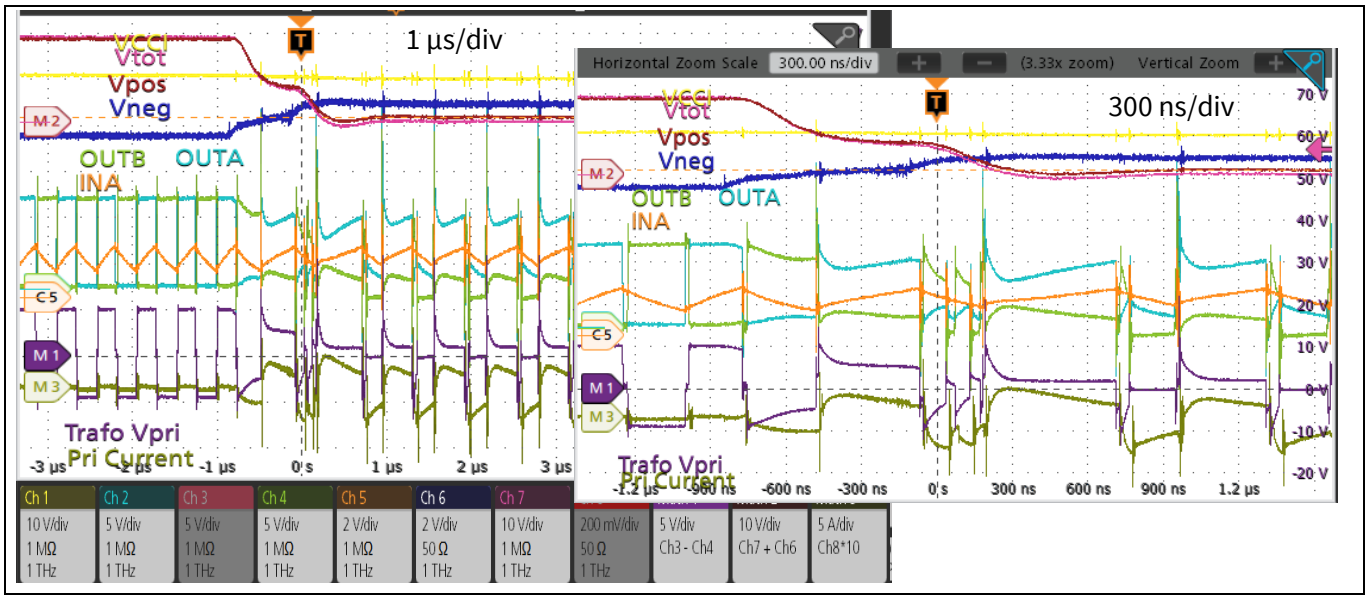

Figure 28 Output short circuit on auxiliary supply output V_{tot} (detail on the right-hand side)

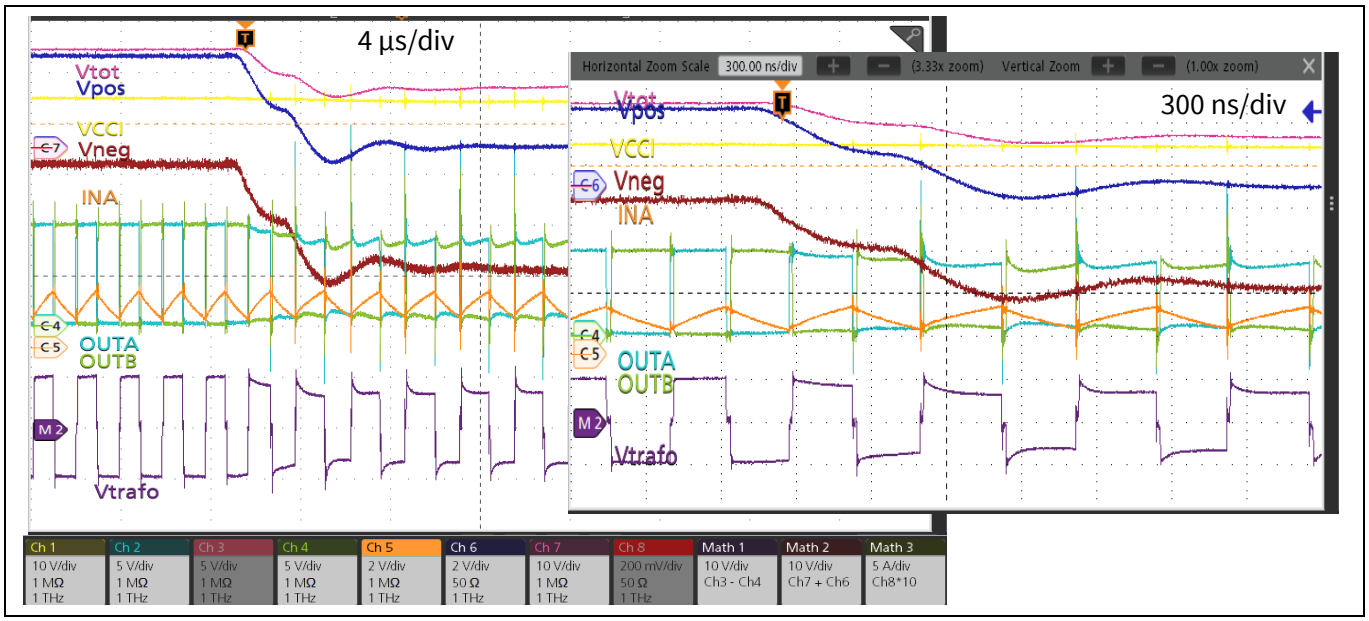

Figure 29 Output short circuit on auxiliary supply output V_{pos} (detail on the right-hand side)

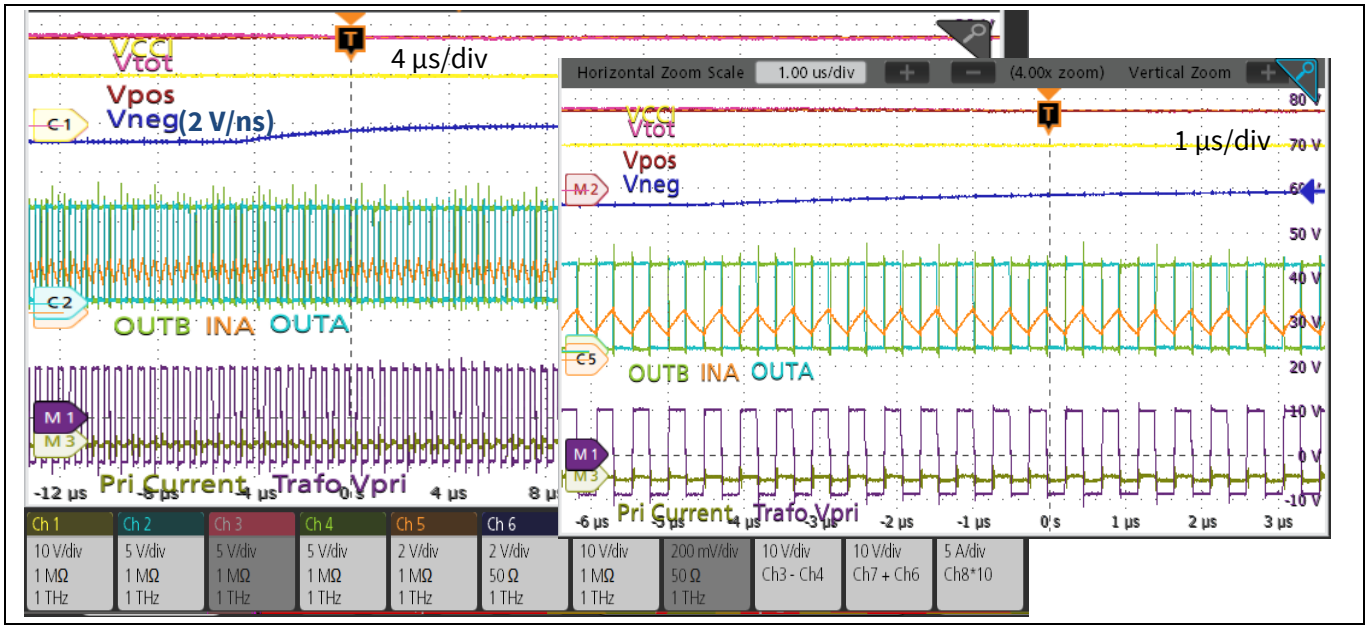

Figure 30 Output short circuit on auxiliary supply output V_{neg} (detail on the right-hand side)

4 Layout

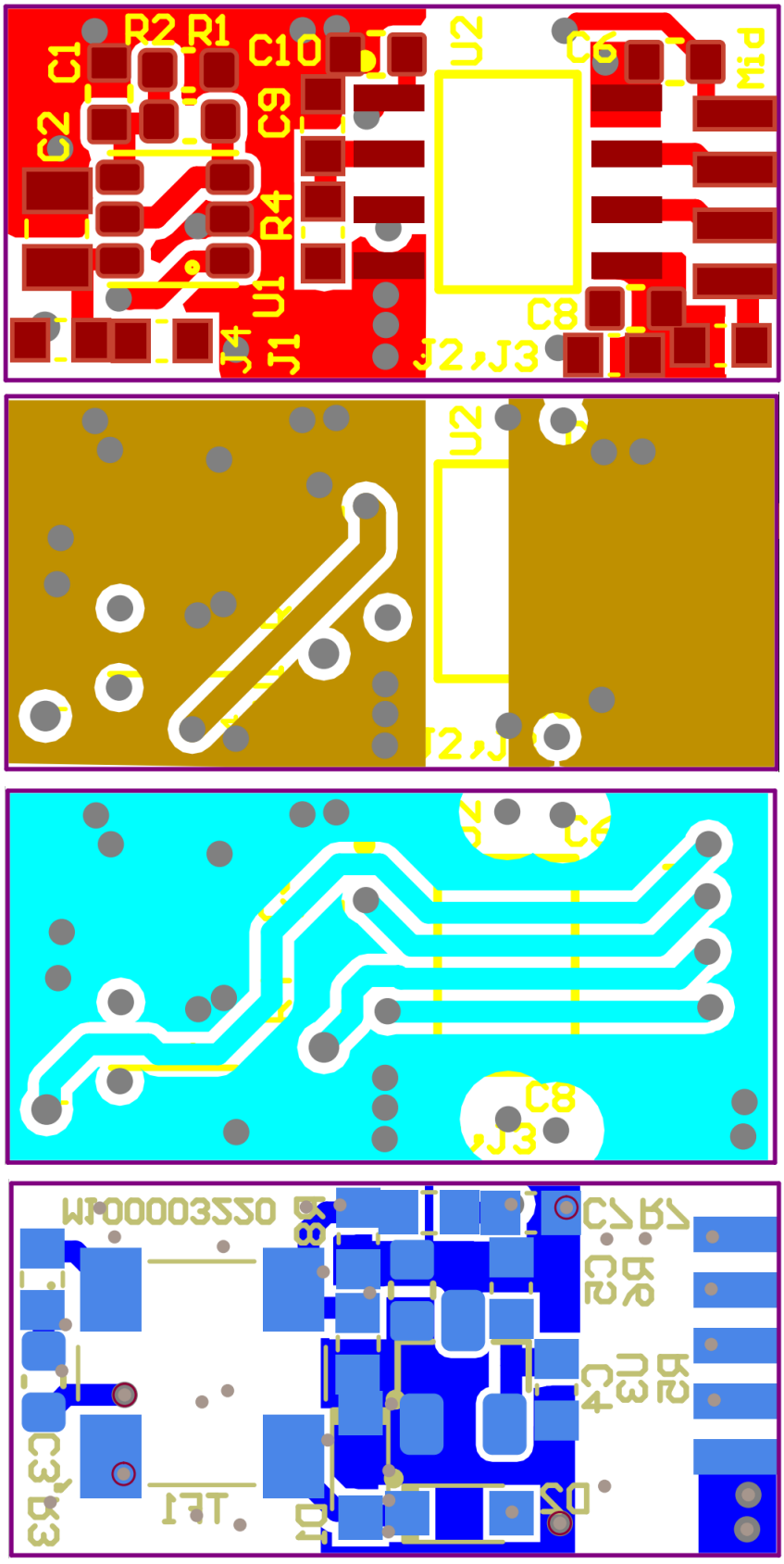

Figure 31 Layout, from top to bottom: top layer, mid-layer1, mid-layer2, bottom layer

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
1	Top Layer		Signal	1oz	0.035mm		
	Dielectric 1	FR-4	Dielectric		0.32004mm	4.8	
2	Mid-Layer 1		Signal	1oz	0.035mm		
	Dielectric2	FR-4	Dielectric		2mm	4.8	
3	Mid-Layer 2		Signal	1oz	0.035mm		
	Dielectric3	FR-4	Dielectric		0.32004mm	4.8	
4	Bottom Layer		Signal	1oz	0.035mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
	Bottom Overlay		Overlay				

Figure 32 Layer stackup

5 Appendix A

5.1 Board functionality when 1 percent regulation is not needed

As mentioned in Section **2.3**, the bipolar V_{pos}/V_{neg} split is set via the shunt regulator TL432 and surrounding resistors. However, if the 1 percent regulation of the positive rail is not needed and the required V_{pos} and V_{neg} are not too unbalanced ($V_{pos}/2\ V_{CCI}$ less than 80 percent as a rule of thumb), the split can be obtained by simply tuning the duty cycle of OUTA-OUTB signal according to formula (3).

$$D \cong \frac{V_{pos}}{2V_{CCI} - 0.5V} \tag{3}$$

0.5 V is the minimum potential drop expected on the auxiliary output at no load.

The OUTA-OUTB duty cycle can be tuned by adapting the oscillator feedback resistors R1 and R2. In this use case the TL432 regulator (U3) and surrounding resistors (R5, R6 and R7) should be removed and R8 should be shorted. **Figure 33** shows a dimensioning example for 12 V V_{CCI} and V_{pos} = 18 V, V_{neg} = -5.5 V at no load.

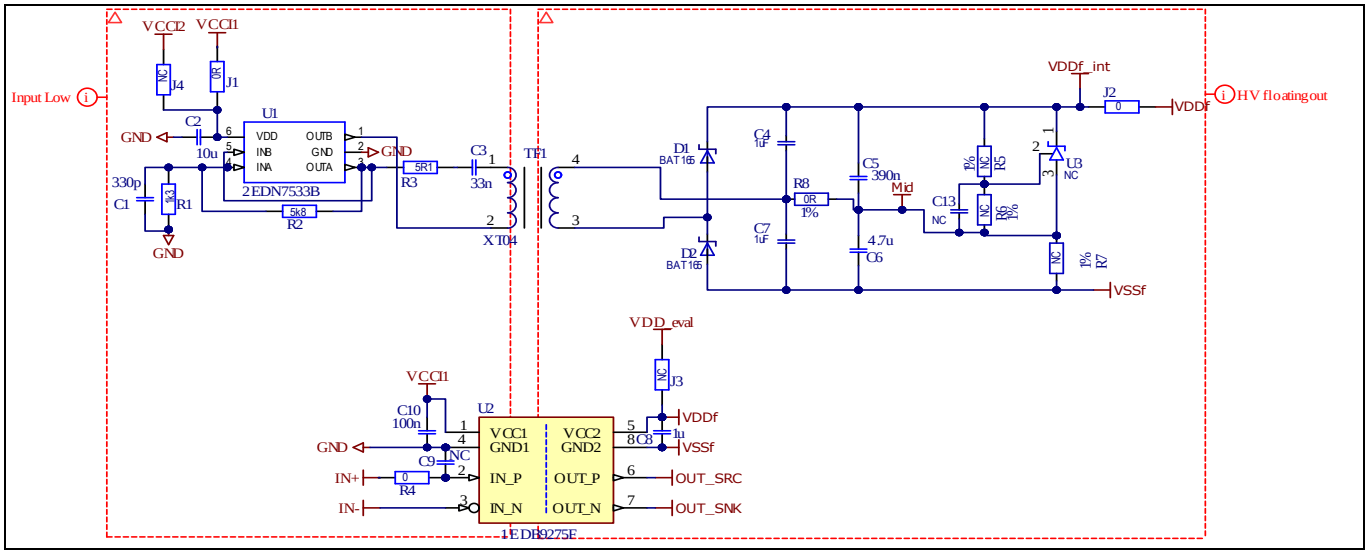

Figure 33 Dimensioning of the auxiliary supply for V_{CCI} = 12 V and unregulated V_{pos} = 18 V, V_{neg} =- 5.5 V when 1 percent regulation of the positive rail is not required

Figure 34 shows the operating waveform of the auxiliary supply with the default Conf. A dimensioning using the TL432 regulator, and the dimensioning shown in **Figure 33** without TL432.

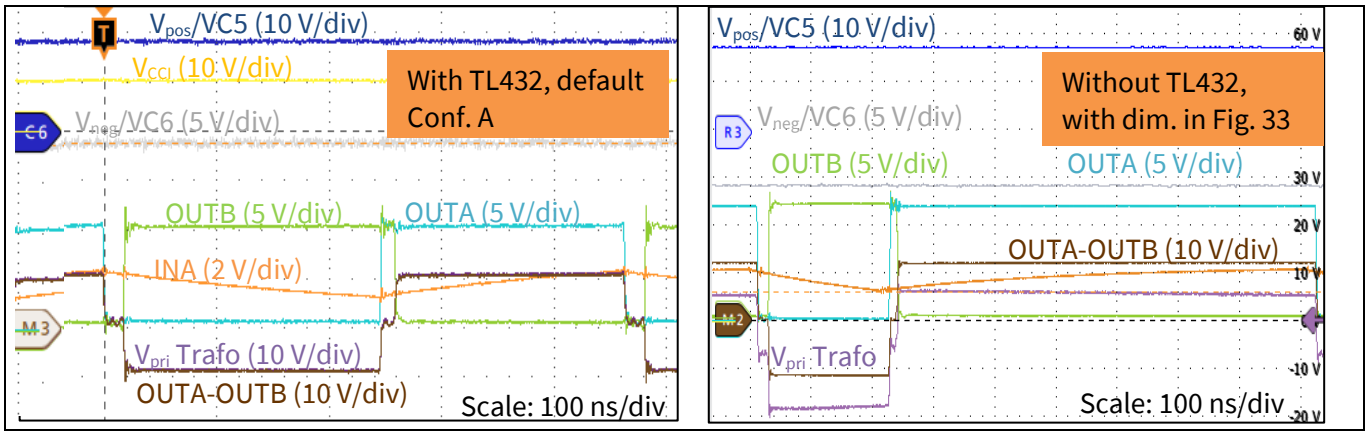

Figure 34 Comparison of auxiliary supply operating waveforms with and without TL432 regulator

As per formula (3) the duty cycle is around 76.5 percent. Similar duty cycle would be required for V_{pos} = 15 V, V_{neg} = -4.5 V split out of 10 V V_{CCI}. In the use case without TL432, OUTA-OUTB is still a three-voltage waveform with levels V_{CCI1}, 0 V, -V_{CCI1}. However, here the duty is not 50 percent and therefore C6 is responsible for removing the DC offset; the voltage seen on the transformer (violet) is therefore shifted down.

As a rule of thumb, for tuning duty cycle and frequency:

- Always consider the core saturation limit of the transformer (6 V/µs for XT04). This limit must not be exceeded in the charging and discharging phase. Therefore, please select the switching frequency accurately.
- Duty cycle only depends on R1 and R2. To reduce the duty cycle, increase R1 and reduce R2, and vice versa to increase it.
- For a fixed R_p = R1//R2, switching frequency can be increased by reducing C1, and vice versa to reduce it.

More detailed formulas can be found in Section **5.1.1**.

5.1.1 Ring oscillator dimensioning of R1, R2 and C1

The ring oscillator behavior has been described in Section **2.2**. Clearly the duty cycle and the frequency of the OUTA-OUTB signal can be tuned by acting on the charging and discharging phase of INA, as illustrated in **Figure 35**.

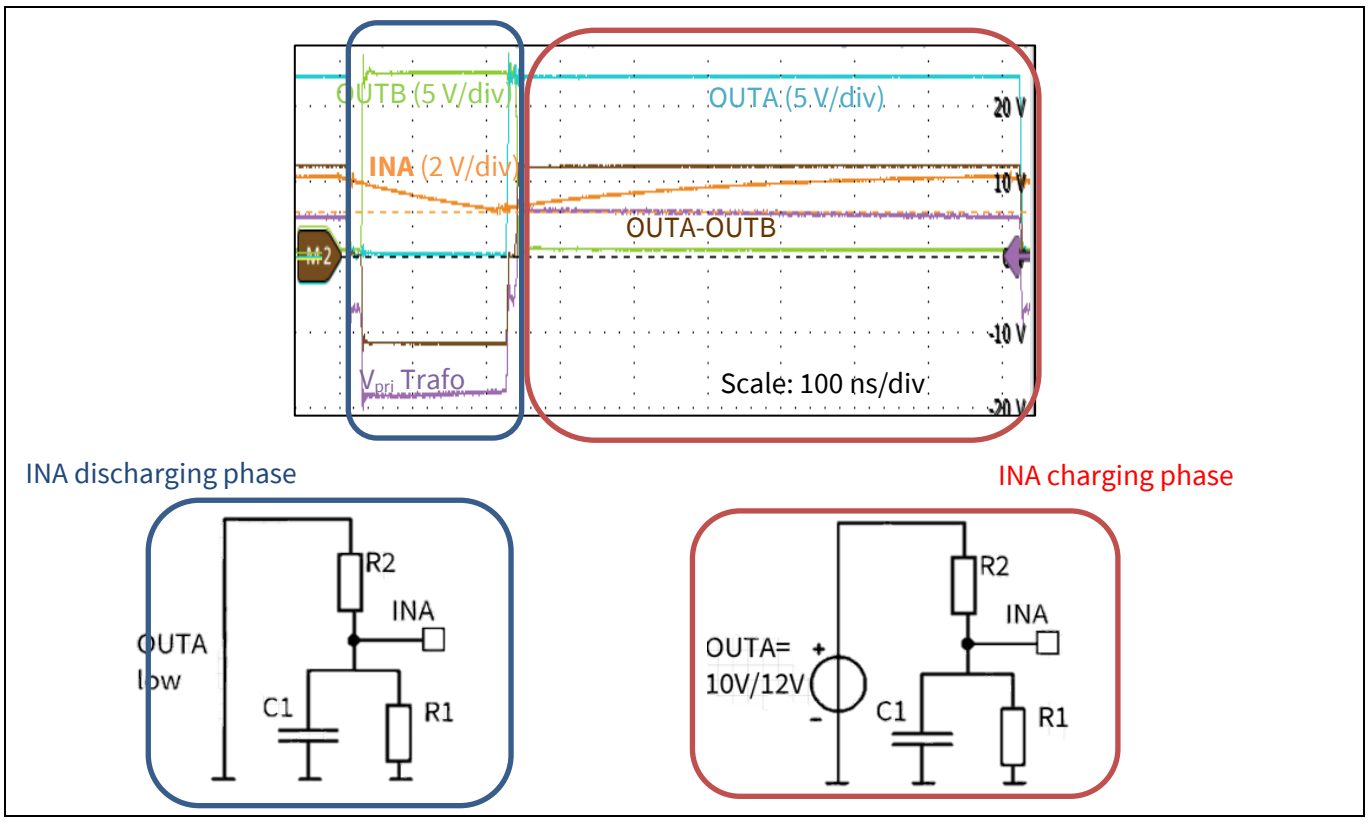

Figure 35 INA charging and discharging mechanisms

Appendix A

Whenever you want to fix the auxiliary V_{pos}/V_{neg} split without using the TL432 regulator, please follow the dimensioning steps described below.

1. Calculate the duty cycle D according to formula (4):

$$D \cong \frac{V_{pos}}{2V_{CCI} - 0.5V} \quad (4)$$

Where 0.5 V is the minimum potential drop expected on the auxiliary output (at no load).

Example: for 18 V, -5.5 V from V_{CCI} = 12 V → D = 76.5 percent

2. Calculate the minimum t_{on}, t_{off} (minimum switching period) allowed from the core-saturation limit of the selected transformer (6 V/µs for XT04). The minimum period T can be selected according to formula (5) with some margin:

$$T_{min} = \frac{t_{off,max}}{D} = \frac{6\ V\ \mu s}{V_{neg} * D} \quad (5)$$

Example: for 18 V, -5.5 V and D = 76.5 percent → T_{min} = 1.42 µs → f_{sw} = 704 kHz → $f_{selected}$ = 1.1 MHz with margin

3. Fix the value of C1 in the range of 100 pF to 1 nF.

Example: Selected 330 pF

4. Calculate R_p = R1//R2 from equation (6):

$$R_p = \frac{1.75 * t_{OFF}}{C1} = \frac{1.75 * (1 - D)T}{C1} \quad (6)$$

Example: With $f_{selected}$ = 1.1 MHz and D = 76.5 percent → R_p = 1.1 kΩ

5. Calculate R2 from equation (7).

$$V_{INH} = e^{-\frac{0.57\,D}{1-D}} (V_{INL} - \frac{R_p}{R2} V_{CCI}) + \frac{R_p}{R2} V_{CCI} \quad (7)$$

Where V_{INH} = 2.1 V, V_{INL} = 1.2 V is the input voltage threshold of the driver.

Example: With R_p = 1.1 kΩ → R2 = 5.8 kΩ according to the dimension in in **Figure 33**.

6. Make sure that the selected values fulfill equation (8):

$$V_{INA} = \frac{R_1}{R_1 + R_2} V_{DD} > V_{INHL} \quad (8)$$

This is necessary to ensure that the oscillation takes place.

Appendix A

Complete calculation of equation (7).

Equation (7) is calculated from INA discharging phase as per equation (9):

$$V_{INA}(t) = V_{INA}(t_0)e^{-\frac{t}{R_P C1}} \tag{9}$$

At the end of the discharging phase for t = t_{off}:

$$V_{INA}(t_{OFF}) = V_{INL} = V_{INH}\, e^{-\frac{t_{off}}{R_P C1}} \rightarrow R_p = \frac{-t_{OFF}}{C1} * \frac{1}{\ln\frac{V_{INL}}{V_{INH}}} \tag{10}$$

Complete calculation of equation (8).

Equation (7) is calculated from the INA charging phase. From Kirchhoff laws:

$$\begin{aligned} i &= \frac{V_{INA}}{R1} + C_1\frac{dV_{INA}}{dt} \\ V_{INA} &= V_{CCI} - R_2 * i \end{aligned} \tag{11}$$

This leads to the following first-order differential equation:

$$\frac{dV_{INA}}{dt} + \frac{1}{R_P\, C_1}\, V_{INA} = \frac{V_{CCI}}{R_2\, C_1} \tag{12}$$

Equation (12) has the following resolution:

$$V_{INA}(t) = e^{-\frac{t}{R_P C1}}\left[V_{INL} - \frac{R_P}{R_2}\, V_{DD}\right] + \frac{R_P}{R_2}\, V_{CCI} \tag{13}$$

At the end of the charging phase for t = t_{ON}:

$$V_{INA}(t_{ON}) = V_{INH} = e^{-\frac{t_{ON}}{R_P C1}}\left[V_{INL} - \frac{R_P}{R_2}\, V_{CCI}\right] + \frac{R_P}{R_2}\, V_{CCI} \tag{14}$$

By including (10) in (14), equation (7) can be derived.

References

[1] Application note “EVAL_2EDB_HB_SiC_Si”, 2022, Infineon Technologies AG.

[2] Whitepaper “**Gate drive solutions for CoolGaN™ GIT HEMT**: Exploiting the full potential of GaN”, 2021-11, Infineon Technologies AG.

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Document revision	Date	Description of changes
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