EZ-PD™ CMG2 USB Type-C EMCA controller

General description

EZ-PD™ CMG2 is a dedicated USB Type-C EMCA controller that complies with the USB Type-C and Power Delivery (PD) standards for electronically marked Type-C thunderbolt and non-thunderbolt passive cable applications. EZ-PD™ CMG2 integrates a complete Type-C transceiver including the R_A termination resistors on the VCONN pins and VBUS short circuit protection on both VCONN and CC pins. EZ-PD™ CMG2 also includes 47 bytes of storage for configuration of vendor, device, and cable specific configuration data. EZ-PD™ CMG2 is targeted for passive EMCA implementations with either one or two e-marker chips on the cable.

Features

- **Type-C support and USB-PD support**
  - Supports USB Power Delivery specification revision 3.1, v1.4 and USB Type-C specification revision 2.1 (including support for the revised minimum VCONN operating voltage of 3 V)
  - Supports USB4, TBT4 and extended power range (EPR) PD protocol
  - Integrated high-voltage protection on CC, VCONN1, and VCONN2 pins to protect against accidental shorts to the VBUS pin on the Type-C connector up to 54 V
  - 47-byte storage programmable over Type-C interface for storing vendor, device, and cable specific configuration data
  - Termination resistor R_A on VCONN1 and VCONN2
  - Supports R_A weakening to reduce power consumption
  - Supports electronically marked passive cable implementations with one or two controllers
  - Supports up to 240W (48V/5A) of power
- **Clocks and oscillators**
- Integrated oscillator eliminating the need for external clock
- **Power**
  - 2.7 V to 5.5 V operation
  - Sleep: 1.7 mA typical
- **System-level electrostatic discharge (ESD) protection**
  - On CC, VCONN1, and VCONN2 pins
  - ± 8 kV contact discharge and ±15 kV air gap discharge based on IEC61000-4-2 level 4C
- **Package**
  - 9-ball WLCSP
  - Supports industrial temperature range (–40°C to +85°C)

Logic block diagram

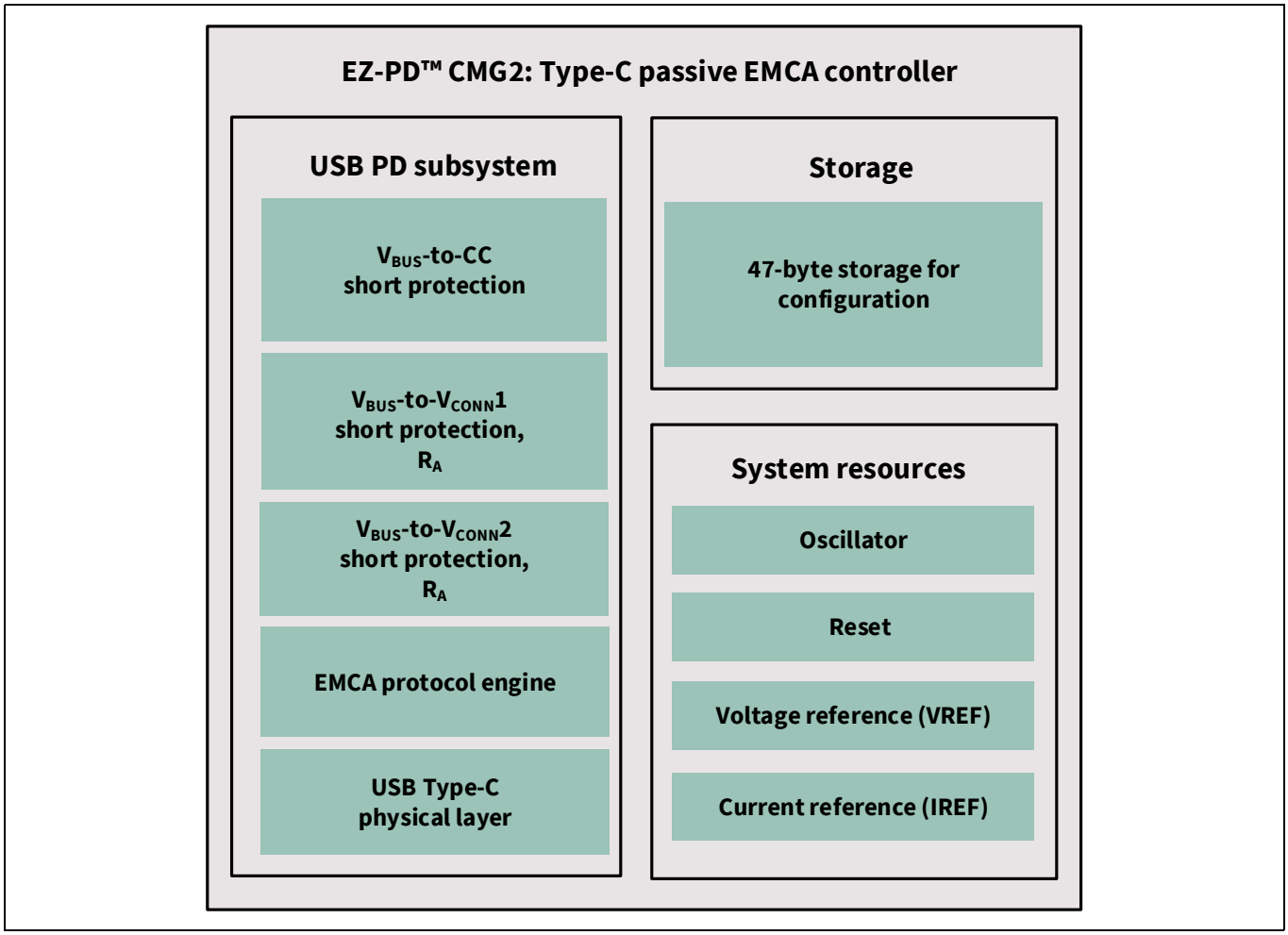


Table of contents

1 Pinout

Table 1 9-ball CSP pin description

9-ball CSP	Pin name	Description
A1	CC	Communication channel (VBUS short protected)/IEC
A2	VCONN2	VCONN2 supply with R_A termination (2.7 V to 5.5 V) (VBUS short protected)/IEC
A3	DNU	Do not use
B1	VCONN1	VCONN1 supply with R_A termination (2.7 V to 5.5 V) (VBUS short protected)/IEC
B2	VSS	Ground pin. Mandatory to connect to system GND.
B3	DNU	Do not use
C1	VCCD	1.8-V core voltage out. Connect to 1-µF capacitor.
C2	DNU	Do not use
C3		

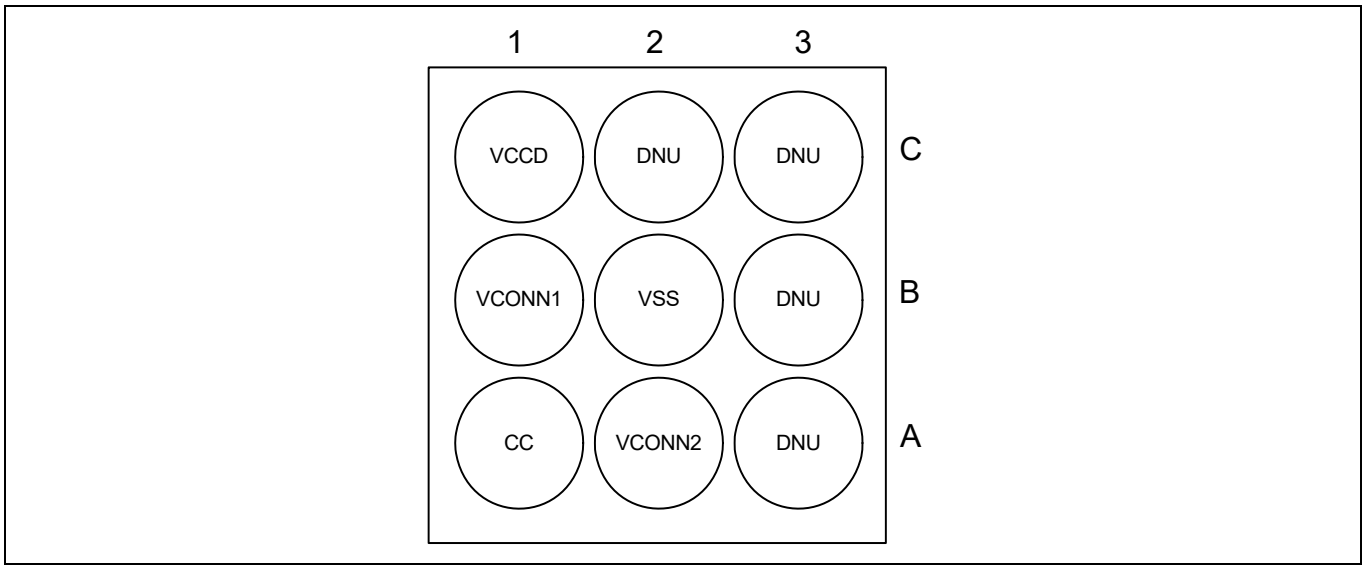


Figure 1 Pinout of 9-WLCSP bottom (balls up) view

2 Power

Figure 2 shows an overview of the EZ-PD™ CMG2 power system requirement. EZ-PD™ CMG2 operates from two possible external supply sources, VCONN1 and VCONN2. The VCONN supplies support operation over 2.7 V–5.5 V. EZ-PD™ CMG2 has two different power modes: Active and Sleep, transitions between which are managed by the Power System. The VCCD pin, the output of the core regulator (1.8 V), is brought out for connecting a 1-µF capacitor for regulator stability only. This pin is not supported as a power supply.

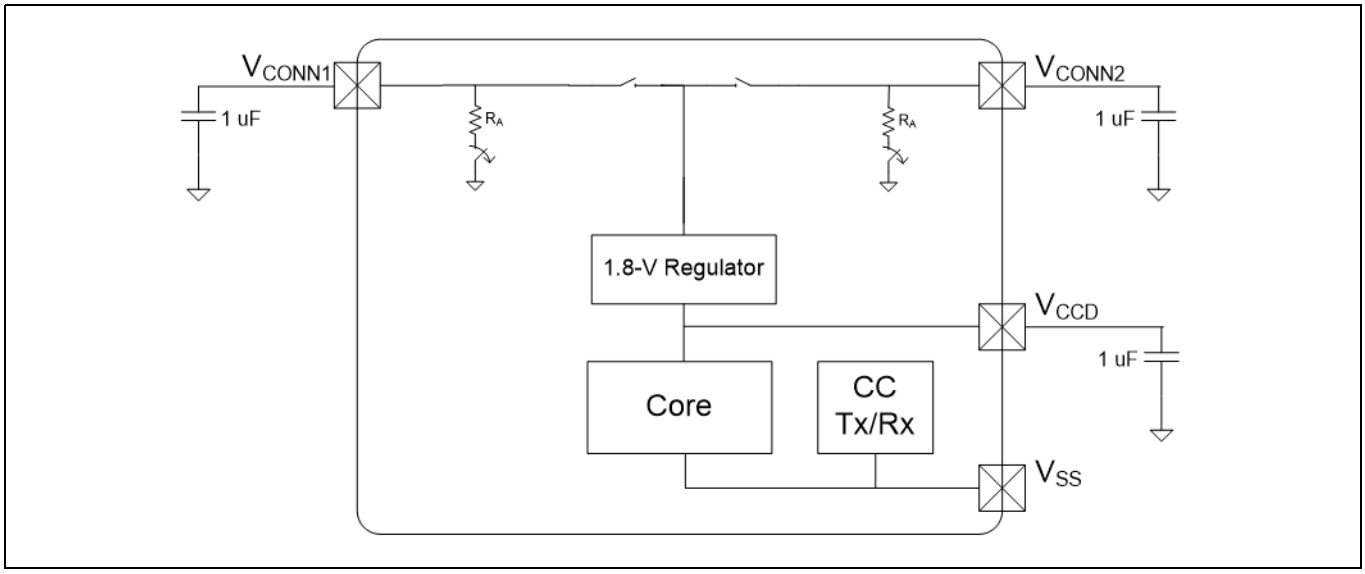


Figure 2 Power system

3 EZ-PD™ CMG2 application configuration update over CC interface

The EZ-PD™ CMG2 manufacturing test kit (MTK) utility is used for updating the configuration parameters of the EZ-PD™ CMG2 devices over the CC interface. The EZ-PD™ CMG2 MTK utility is integrated as a part of the EZ-PD™ configuration utility and is supported from v1.4.0. Vendor-specific and cable-specific parameters can be set using the EZ-PD™ configuration utility. Once the parameters are set, the EZ-PD™ CMG2 MTK utility is used for configuration and testing of EZ-PD™ CMG2-based passive EMCA cables.

To use the EZ-PD™ CMG2 MTK utility, you must use the CY4532 EZ-PD™ CCG3PA EVK as shown in a high-level block diagram in **Figure 3**. The EZ-PD™ CMG2 MTK utility is accompanied with a EZ-PD™ CMG2 MTK-specific firmware solution, which is intended for the CCG4 device present on the CY4532 EZ-PD™ CCG3PA EVK's power board. If customers are using the CY4532 EZ-PD™ CCG3PA EVK for the first time to update the configuration parameters of EZ-PD™ CMG2 devices, then the CCG4 device's firmware needs to be updated to this MTK-specific firmware.

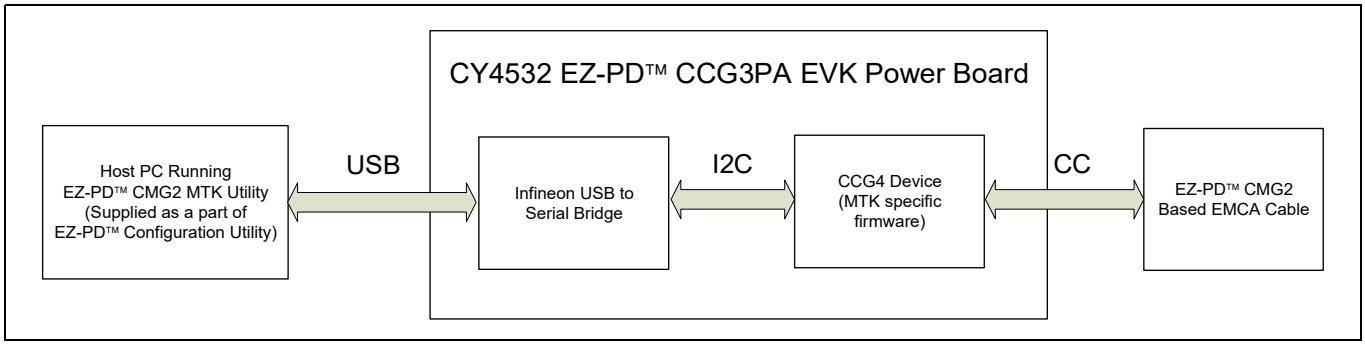


Figure 3 CMG2 application configuration update over CC interface

4 Application diagrams

Figure 4 and **Figure 5** show the application diagrams of a passive EMCA application using EZ-PD™ CMG2 devices. **Figure 4** shows the application using a single EZ-PD™ CMG2 device per cable present at one of the two plugs, whereas **Figure 5** shows the same with two EZ-PD™ CMG2 devices per cable present at each plug. The VBUS signal, the SuperSpeed lines, Hi-Speed lines, and CC lines are connected directly from one end to another. The application diagram shown in **Figure 4** requires a single VCONN wire to run through the cable so that the CMG2 device can be powered irrespective of which plug is connected to the host (DFP). However, in the application diagram shown in **Figure 5**, the VCONN signal does not run through the entire cable, but only runs to the respective VCONN pin of the EZ-PD™ CMG2 device at each end of the plug. Also, only one EZ-PD™ CMG2 device is powered at any given instance, depending on which one is nearer to the DFP that supplies VCONN.

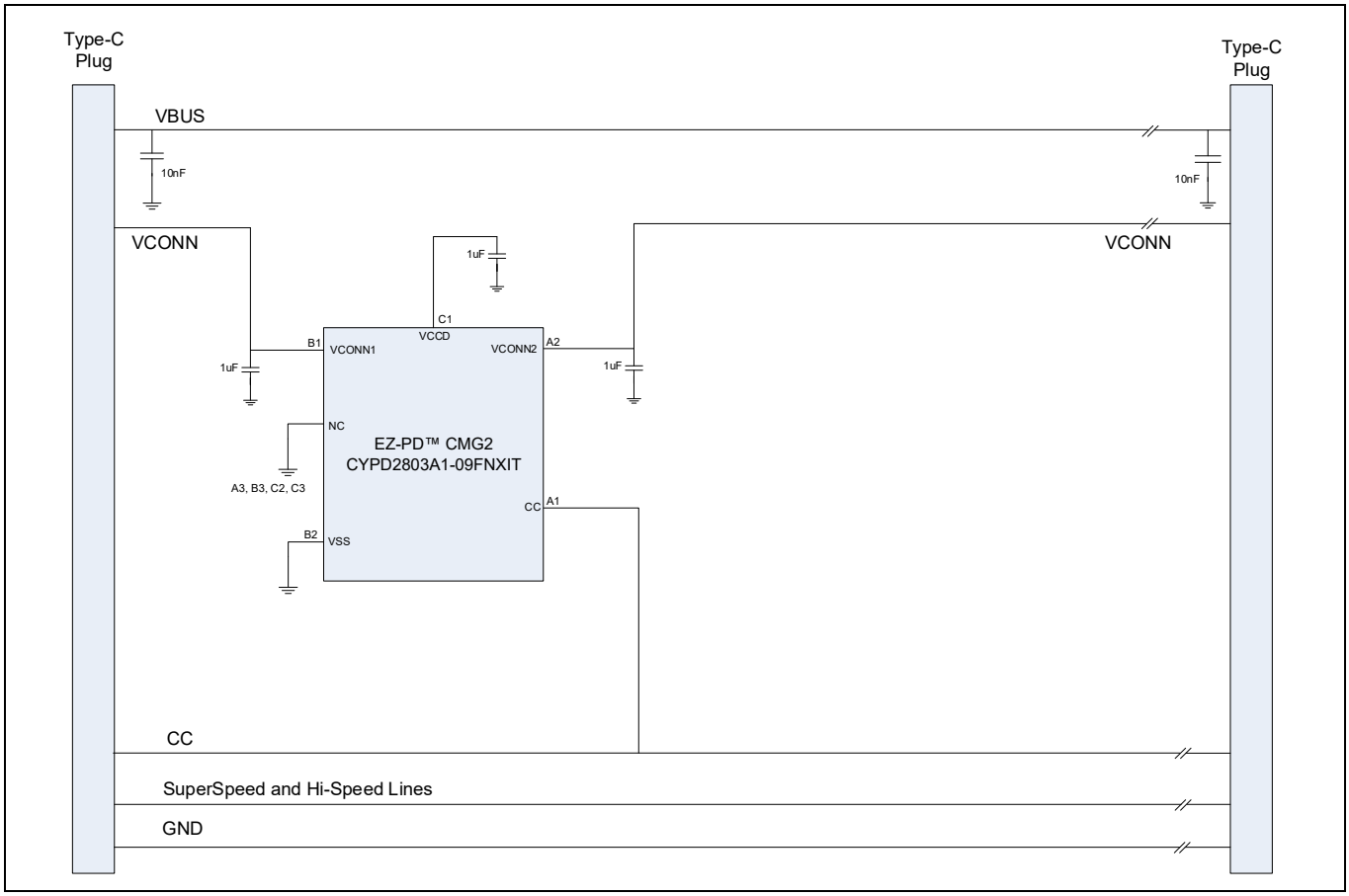


Figure 4 Passive EMCA application - single CMG2 chip per cable

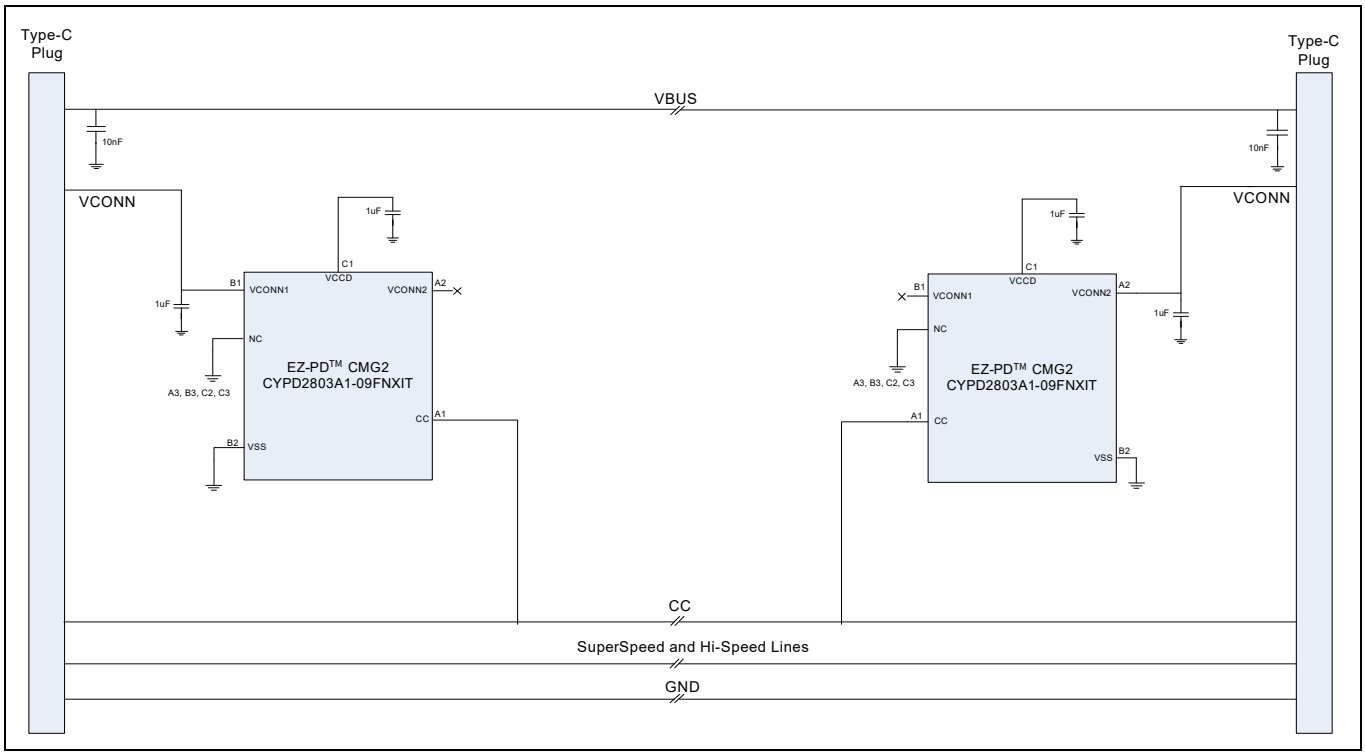


Figure 5 Passive EMCA application - single CMG2 chip per plug

5 Electrical specifications

5.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
$V_{CONN\_SHORT\_MAX}$	Max V_{BUS} short voltage tolerance	–	–	54	V	Absolute max
$V_{CC\_PIN\_ABS}$	Max V_{BUS} short voltage on the CC pin					
ESD_HBM	Electrostatic discharge human body model (ESD-HBM)	2200	–	–		–
ESD_CDM	Electrostatic discharge charged device model (ESD-CDM)	500				
LU	Pin current for latch-up	–100		100	mA	
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000		–	V	VCONN1, VCONN2, and CC pins tolerant for IEC test at system/connector level
ESD_IEC_AIR		15000				

5.2 Device-level specifications

See basic specifications in the following tables. More specifications will be added in a future version of this document.

Table 3 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{CONN1} or V_{CONN2}	Power supply input voltage	2.7	–	5.5	V	–
SID.PWR#5	V_{CCD}	Output voltage (for core logic)	–	1.8	–		
SID.PWR#12	C_{EFC}	External regulator voltage bypass on V_{CCD}	0.8	1	1.2	µF	X5R ceramic or better
SID.PWR#13	C_{VCONN}	Power supply decoupling capacitor on V_{CONN1} and V_{CONN2}			–		
Active mode, V_{CONN1} or V_{CONN2} = 2.7 V to 5.5 V. Typical values measured at V_{CONN1} or V_{CONN2} = 5 V							
SID.PWR#8	I_{DD_A}	Active current	–	5	7.5	mA	CC I/O in Transmit (Tx) or Receive (Rx). CPU at 18 MHz.
Sleep mode, typical values measured at V_{CONN1} or V_{CONN2} = 5 V and T_A = 25°C							
SID25A	I_{DD_S}	Sleep mode current	–	1.7	3.0	mA	CC as wakeup source. One VCONN supply is powered, the other is floating or grounded.

Table 4 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.6	R_A	Power cable termination	0.8	1	1.2	kΩ	All supplies force to 0 V and 0.2 V applied at V_{CONN1} or V_{CONN2}
SID.PD.7	R_{A_OFF}	Power cable termination – disabled	0.2	0.7	–	MΩ	2.7 V applied at V_{CONN1} or V_{CONN2} with R_A disabled
SID.PD.14	I_{LEAK}	Leaker on V_{CONN1} or V_{CONN2} for discharge upon cable detach	150	–		µA	–
SID.PD.15	$V_{GNDOFST}$	Ground offset tolerated by bi-phase mark code (BMC) receiver	–500		500	mV	Relative to remote BMC transmitter
SID.PD.16	Z_{OPEN_PD}	Impedance of CC pin with VCONN1 and VCONN2 unpowered	200		–	kΩ	0 V ≤ CC voltage ≤ 5.5 V

Table 5 Storage specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#3	NVL_ERASE	NVL bulk erase time	25	–	100	ms	–40°C ≤ T_A ≤ 85°C
SID.MEM#4	NVL_WRITE	NVL program	2		10		
SID.MEM#5	NVL_DR	NVL data retention	20		–	years	25°C ≤ T_A ≤ 55°C
SID.MEM#5A			10				55°C ≤ T_A ≤ 85°C
SID.MEM#6	NVL_ENPB	NVL write endurance	100			cycles	25°C ≤ T_A ≤ 55°C

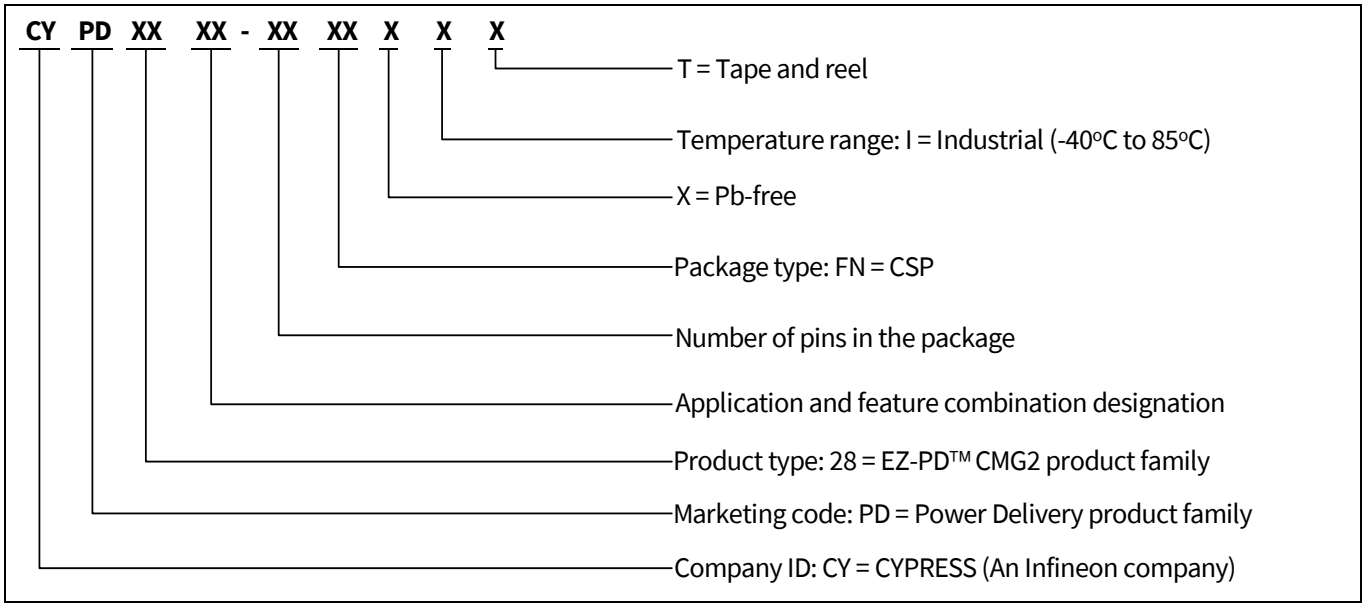
6 Ordering information

Table 6 lists the EZ-PD™ CMG2 part numbers and features.

Table 6 EZ-PD™ CMG2 ordering information

MPN	Application	Type-C ports	Role	Package type	Si ID
CYPD2803A1-09FNXIT	Passive cable	1	EMCA	9-ball CSP	0x3C00

6.1 Ordering code definition



7 Packaging

Table 7 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	–40	–	85	°C
T_J	Operating junction temperature		–45		100	
T_{JA}	Package θ_{JA} (9-pin CSP)	–	–	51.2	–	°C/W
T_{JC}	Package θ_{JC} (9-pin CSP)			1.38		

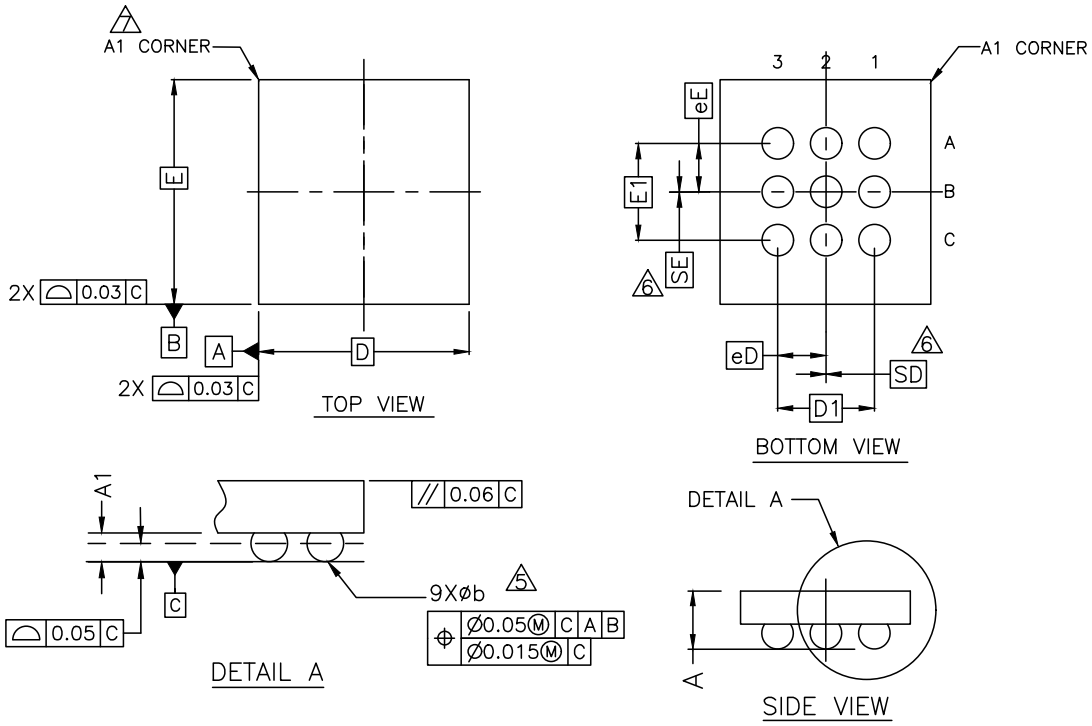
Table 8 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
9-pin CSP	260°C	30 seconds

Table 9 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
9-pin CSP	MSL 1

7.1 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.52
A1	0.175	-	-
D	1.741 BSC		
E	1.856 BSC		
D1	0.80 BSC		
E1	0.80 BSC		
MD	3		
ME	3		
N	9		
Øb	0.231	0.261	0.291
eD	0.40 BSC		
eE	0.40 BSC		
SD/SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. JEDEC SPECIFICATION NO. REF. : N/A.

002-35236 *B

Figure 6 9 Ball WLCSP 1.741 × 1.856 × 0.520 mm FN09B

8 Acronyms

Table 10 Acronyms used in this document

Acronym	Description
BMC	bi-phase mark code
CC	configuration channel
CPU	central processing unit
DFP	downstream facing port
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EPR	extended power range
ESD	electrostatic discharge
HBM	human body model
IEC	International Electrotechnical Commission
IC	integrated circuit
MCU	microcontroller unit
MTK	manufacturing test kit
NC	no connect
NVL	non-volatile latch
PD	power delivery
PHY	physical layer
POR	power-on reset
PSoC™	Programmable System-on-Chip™
RX	receive
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 240W of power
USB	Universal Serial Bus

9 Document conventions

9.1 Units of measure

Table 11 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
kΩ	kilo ohm
MHz	megahertz
MΩ	mega-ohm
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
s	second
V	volt

Revision history

Document revision	Date	Description of changes
*B	2023-05-05	Release to web.

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