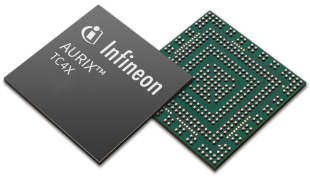
AURIX™ 3rd Generation 32-bit single-chip microcontroller

Features



RoHS

AEC Qualified

- High performance microcontroller with 6 CPU cores and one parallel processing unit (vector DSP)
- CPUs are 32-bit super-scalar TriCore™ CPUs (TC1.8 LS) with virtual machine hardware support and double precision floating point arithmetic; 6 fully lockstepped cores
- Low latency SRAMs close to the CPUs and global SRAM
- 20 MB of embedded program memory with multiple parallel banks and A/B swap option
- Up to 1152 KB of embedded data NVM
- High performance cyber security architecture with 1 MB of program memory and 128 KB of data memory
- 2 DMA controllers each with 128/64 channels and 2 move engines
- ADC sub-system with 8 SAR ADC cores. Each 2 ADC cores share 16 inputs equipped with sample and hold stage (TMADC), 2 embedded DSP cores for flexible post processing of ADC results (CDSP)
- An eGTM timer unit with input and output channels
- High speed communication interfaces (LETH, GETH, PCIe, CANXL, xSPI, HSSL, SDMMC)
- Low speed communication interfaces (CAN, FlexRay, QSPI, ASCLIN, I2C)
- Sensor interfaces (MSC, SENT, PSI5, PSI5-S)
- Sophisticated interrupt system with interrupt router and ECC
- Safety and security alarm Management Unit (SMU) handling safety and cyber security alarms
- Advanced trace and debug with support of run control debugging for multi-core and time aligned multi-core program and data trace for all CPUs in parallel, and 5 Gbps high speed serial trace interface
- Support of 2 DAP (Device Access Port) interfaces and one JTAG interface
- Digital programmable IO ports
- Volatile Memory Test (VMT) unit with ECC, memory initialization, and MBIST functions
- Power Management System and on-chip regulators
- Clock generation unit with system PLL and peripheral PLL
- Embedded voltage regulators

Product validation

Product validation according to AEC-Q100, Grade 1.

Qualified for automotive applications.

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1 Device feature set

1.1 Device feature set description

The TC4Dx product has the following features:

- High performance microcontroller with 6 CPU cores and one parallel processing unit
- 6 fully lock-stepped 32-bit super-scalar TriCore™ CPUs (TC1.8) with virtual machine hardware support and double precision floating point arithmetic
- SRAM
  - Low latency SRAMs close to the CPUs, up to 4896 Kbyte
  - Global SRAM, up to 5120 Kbyte
- Embedded flash
  - Data flash up to 1152 Kbyte
  - Program flash up to 21 Mbyte
  - Support of software over the air (SOTA) updates with improved A/B swap option
- High performance cyber security architecture
  - Cyber security real-time module (CSRM) with TriCore™ CPU with local low latency SRAM, private program and data flash and Security hardware accelerators
  - Cyber security satellite (CSS) with accelerators for various symmetric cryptographic algorithms, such as AES, SHA, and ChaChaPoly, multi-channel architecture for high throughput and accessible for all CPUs
- Parallel processing unit (PPU)
- 2 DMA controllers with 128/64 channels and 2 move engines each
- ADC sub-system with
  - 8 SAR ADC cores. Each 2 ADC cores share 16 inputs equipped with sample and hold stage (TMADC)
  - 2 embedded DSP cores for flexible post processing of ADC results (CDSP)
- An eGTM timer unit with 24 input and 72 output channels
- High speed communication interfaces
  - 2 x up to 5 Gbps Ethernet ports with advanced layer 2 bridging function
  - 4 x 10/100 Mbps Ethernet ports (with 10BASE-T1S support) with advanced layer 2 bridging function
  - A data routing engine (DRE) for low latency CAN routing, CAN to IEEE 1722 Ethernet packet translation, Ethernet to Ethernet routing
  - 2 PCIe Gen3 with 1 lane per module and up to 8 Gbps
  - 4 CANXL nodes supporting up to 20* Mbps (*only with Fast pads)
  - xSPI supporting Quad, Octal SPI and Hyperbus, HyperRam
  - 2 HSSL links
  - 1 SDMMC interface supporting High Speed (HS) mode
- Low speed communication interfaces
  - 20 CAN nodes with CAN-FD support up to 8 Mbps with integrated CAN-to-CAN messages routing
  - 4 FlexRay channels
  - 8 Queued SPI channels with up to 16 chip selects each

  - 28 ASCLIN channels
  - 3 I2C interfaces
- Sensor Interfaces
  - 1 MSC module
  - 2 SENT modules with 15 channels each
  - 2 PSI5 channels, 1 PSI5-S module
- Sophisticated interrupt system with interrupt router and ECC
- Safety and security alarm Management Unit (SMU) handling safety monitor alarms
- Advanced debug and trace
  - Rich support of run control debugging for multi-core, time aligned multi-core program and data trace for all CPUs in parallel
  - SGBT interface based on Aurora protocol
  - Up to 5 Gbps high speed serial trace interface
  - Use of Ethernet ports for debug and trace purposes
  - Support of 2 DAP (Device Access Port) interfaces and one JTAG interface
- Digital programmable IO ports
- Volatile Memory Test with ECC, memory initialization and MBIST functions (VMT)
- Power Management System and on-chip regulators
- Low power CPU subsystem with timer and communication peripherals (SCR)
- Clock Generation Unit with system PLL and peripheral PLL
- Embedded voltage regulators

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself. That is, its function set, the temperature range, and the supply voltage
- The package and the type of delivery

This document describes the derivatives of the device. The following tables enumerates these derivatives and summarizes the differences.

1.2 Device feature set table

Table 1 Device feature set table

Feature		TC4DxAA-step COM
CPUs	Type	TC1.8 LS
	Cores / checker cores	6 / 6
	Maximum frequency	500 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB for CPU 0, 1, 2, 3, 4, and 5
	DSPR	240 KB for CPU 0, 1, 2, 3, 4, and 5
	DLMU	512 KB for CPU 0, 1, 2, 3, 4, and 5

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC4DxAA-step COM
SRAM global	LMU	5120 KB
Program memory	Size	4 MB (2x2 MB) each for CPU 0, 1, 3, and 4; 2 MB (2x1 MB) each for CPU 2 and 5
	Banks	12
Data memory	Size (single-ended)	DF0 1024 KB; DF1 128 KB
CPU-CS	Type	TC1.8 non LS
	Maximum frequency	500 MHz
Cache CPU-CS	Program	32 KB
	Data	16 KB
SRAM CPU-CS	PSPR	64 KB
	DSPR	240 KB
	DLMU	-
Program memory CPU-CS	Size	1 MB
CSS		
PPU		
DMA	Channels	SDMA0 128 ch, SDMA1 64 ch
TMADC	SAR cores	8
	Sample and hold circuitry per 2 SAR cores	16
FC	Channels	-
DSADC	Channels	-
EXMOD	Channels	-
CDSP	Cores	2

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC4DxAA-step COM
	Data SRAM per core	3 KB
	Program SRAM per core	3 KB
GTM Classic	TIM	-
	TOM	-
	ATOM	-
	MCS	-
	PSM RAM (FIFO, 1024 x 29 bit)	-
	TBU channels	-
	SPE	-
	BRC / DPLL	-
	DTM modules	-
eGTM	TIM	3 TIM * 8 ch = 24 input ch
	TOM	3 TOM * 16 ch = 48 16-bit output ch
	ATOM	3 ATOM * 8 ch = 24 24-bit output ch
	TBU channels	3
	SPE	3
	DTM modules	12 @ TOM, 6 @ ATOM
HRPWM	High Resolution PWM channels	-
Timer	GPT12	-
STM	Modules	1 per CPU
FlexRay	Modules	2 modules, each with an A and B channel
	Channels	4
CAN	Modules	5 MCMCAN modules and 1 CANXL module
	Channels	4 channels per MCMCAN and 4 channels per CANXL
	Nodes	20 M_CAN and 4 X_CAN nodes
	Nodes which support TT-CAN	-
	CAN routing accelerator	Yes, via DRE and CRE
	CAN to Ethernet	Yes, via DRE
QSPI	Modules (up to 16 chip select per module)	8
	HSIC Channels	-

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC4DxAA-step COM
ASCLIN	Channels	28
I2C	Interfaces	3
SENT	Modules	2
	Channels	15 channels per module
Audio subsystem	I2S/TDM instances	-
	I2S/TDM sample rate range	-
	Mixer instances	-
	Mixer source:destination conversion ratios	-
	Mixer source sample rate range	-
	Mixer destination sample rate range	-
PSI5	Channels	2
PSI5-S	Modules	1
HSSL	Modules	2
MSC	Modules	1
xSPI	xSPI External Memory Interface (DDR and SDR support)	1
SDMMC	eMMC/SD Interface	1
LETH (10/100/1000 Mbps)		
LETH (10/100 Mbps)		
GETH(100 Mbps, 1 Gbps, 2.5 Gbps, 5 Gbps)	Modules	2
PCIe	Modules	2 modules, 1 lane per module
HSPHY		
FCE	Modules	1
Safety support	SMU	Yes
	IOM	No
SPU	Modules	-
RIF	CSI2 Modules	-
Security	CSRM	1
Debug	OCDS	Yes
	MCDS	1 x MCDS 4P (32 KB TBUF); 1 x MCDS 2P (16 KB TBUF)
	SGBT	Yes

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC4DxAA-step COM
EVR	Type	EVRC Core Regulator
Low power features	Standby RAM	128 KB dLMU0 + 128 KB dLMU1
	SCR	Yes
Packages	Type	PG-F2BGA-436, PG-F2HBGA-436 and PG-F2BGA-292
IO	Type	5 V CMOS, 3.3 V CMOS, LVDS, and 1.8 V pad support

2 Marking options

Naming conventions

Prefix:

- SAK: $T_{ambient}$ Temperature Range from -40°C up to +125°C
- SAA: $T_{ambient}$ Temperature Range from -40°C up to +105°C

Feature package:

- P: Standard
- Q: Standard + CAN-XL
- C: Customer specific
- E: Emulation device
- X: Extended feature

2.1 TC4Dx AA step variants

2.1.1 TC4Dx AA step (part 1)

A table listing the TC4Dx AA step variants.

Table 2 TC4Dx AA step (part 1)

***Note**: Variants marked with * are available on request only.*

Product Name	SAA-TC4D9XP-20MF500CC*	SAA-TC4D9XP-20MF500MC	SAA-TC4D9XQ-20MF500CC*	SAK-TC4D9XP-20MF500CC*
Step	AA	AA	AA	AA
Production Status	Standard	Standard	Standard	Standard
Package Type	PG-F2HBGA-436	PG-F2BGA-436	PG-F2HBGA-436	PG-F2HBGA-436
Pinout	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx

(table continues...)

Table 2 (continued) TC4Dx AA step (part 1)

***Note**: Variants marked with * are available on request only.*

Product Name	SAA-TC4D9XP-20MF500CC*	SAA-TC4D9XP-20MF500MC	SAA-TC4D9XQ-20MF500CC*	SAK-TC4D9XP-20MF500CC*
Temperature Range (Ambient)	SAA	SAA	SAA	SAK
Chip ID	0xF6715540	0xF6715542	0xF672D540	0x76715540
Cores / Checker Cores	6/6	6/6	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	10832	10832	10832	10832
Extension memory (KB)	5120	5120	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0
CDSP Cores	2	2	2	2
HRPWM Instances	0	0	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps

(table continues...)

Table 2 (continued) TC4Dx AA step (part 1)

***Note**: Variants marked with * are available on request only.*

Product Name	SAA-TC4D9XP-20MF500CC*	SAA-TC4D9XP-20MF500MC	SAA-TC4D9XQ-20MF500CC*	SAK-TC4D9XP-20MF500CC*
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	2	2	2	2
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	0	0	1/4	0
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	30	30	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.1.2 TC4Dx AA step (part 2)

A continuation table listing the TC4Dx AA step variants.

Table 3 TC4Dx AA step (part 2)

Note: *Variants marked with * are available on request only.*

Product Name	SAK-TC4D9XP-20MF500MC	SAK-TC4D9XC-20NF500MC	SAK-TC4D9XQ-20MF500CC*	SAK-TC4D9XQ-20MF500MC
Step	AA	AA	AA	AA
Production Status	Standard	Standard	Standard	Standard
Package Type	PG-F2BGA-436	PG-F2BGA-436	PG-F2HBGA-436	PG-F2BGA-436
Pinout	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAK	SAK	SAK	SAK
Chip ID	0x76715542	0x76725142	0x7672D540	0x7672D542
Cores / Checker Cores	6/6	6/3	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	10832	6224	10832	10832
Extension memory (KB)	5120	1024	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0
CDSP Cores	2	2	2	2

(table continues...)

Table 3 (continued) TC4Dx AA step (part 2)

***Note**: Variants marked with * are available on request only.*

Product Name	SAK-TC4D9XP-20MF500MC	SAK-TC4D9XC-20NF500MC	SAK-TC4D9XQ-20MF500CC*	SAK-TC4D9XQ-20MF500MC
HRPWM Instances	0	0	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 2.5 Gbps	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	2	2	2	2
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	0	0	1/4	1/4
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	30	10	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.1.3 TC4Dx AA step (part 3)

A continuation table listing the TC4Dx AA step variants.

Table 4 TC4Dx AA step (part 3)

Note: *Variants marked with * are available on request only.*

Product Name	SAK-TC4D9XQ-20MO500CC*	SAK-TC4D9XQ-20MO500MC	SAK-TC4D9XP-20MO500CC*	SAK-TC4D9XP-20MO500MC
Step	AA	AA	AA	AA
Production Status	Standard	Standard	Standard	Standard
Package Type	PG-F2HBGA-436	PG-F2BGA-436	PG-F2HBGA-436	PG-F2BGA-436
Pinout	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAK	SAK	SAK	SAK
Chip ID	0x7672D5C0	0x7672D5C2	0x767155C0	0x767155C2
Cores / Checker Cores	6/6	6/6	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	10832	10832	10832	10832
Extension memory (KB)	5120	5120	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0
CDSP Cores	2	2	2	2

(table continues...)

Table 4 (continued) TC4Dx AA step (part 3)

***Note**: Variants marked with * are available on request only.*

Product Name	SAK-TC4D9XQ-20MO500CC*	SAK-TC4D9XQ-20MO500MC	SAK-TC4D9XP-20MO500CC*	SAK-TC4D9XP-20MO500MC
HRPWM Instances	0	0	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	2	2	2	2
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	1/4	1/4	0	0
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	30	30	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.2 TC4Dx AB step variants

2.2.1 TC4Dx AB step (part 1)

A table listing the TC4Dx AB step variants.

Table 5 TC4Dx AB step (part 1)

Product Name	SAK-TC4D7XC-20NF500MC	SAK-TC4D7XP-20MF500MC	SAK-TC4D7XQ-20MF500MC	SAK-TC4D7XQ-20MO500MC
Step	AB	AB	AB	AB
Production Status	Custom	Standard	Standard	Standard
Package Type	PG-F2BGA-292	PG-F2BGA-292	PG-F2BGA-292	PG-F2BGA-292
Pinout	BGA292_COM 0.8 mm	BGA292_COM 0.8 mm	BGA292_COM 0.8 mm	BGA292_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAK	SAK	SAK	SAK
Chip ID	0x75F25142	0x75F15542	0x75F2D542	0x75F2D5C2
Cores / Checker Cores	6/3	6/6	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	6224	10832	10832	10832
Extension memory (KB)	1024	5120	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0

(table continues...)

Table 5 (continued) TC4Dx AB step (part 1)

Product Name	SAK-TC4D7XC-20NF500MC	SAK-TC4D7XP-20MF500MC	SAK-TC4D7XQ-20MF500MC	SAK-TC4D7XQ-20MO500MC
CDSP Cores	2	2	2	2
HRPWM Instances	0	0	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 2.5 Gbps	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	1	1	1	1
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	0	0	1/4	1/4
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	10	30	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.2.2 TC4Dx AB step (part 2)

A continuation table listing the TC4Dx AB step variants.

Table 6 TC4Dx AB step (part 2)

Note: *Variants marked with * are available on request only.*

Product Name	SAK-TC4D7XP-20MO500MC	SAK-TC4D9XC-20NF500MC	SAA-TC4D9XM-20MF500MC	SAA-TC4D9XP-20MF500CC*
Step	AB	AB	AB	AB
Production Status	Standard	Custom	Custom	Standard
Package Type	PG-F2BGA-292	PG-F2BGA-436	PG-F2BGA-436	PG-F2HBGA-436
Pinout	BGA292_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAK	SAK	SAA	SAA
Chip ID	0x75F155C2	0x76725142	0xF6705542	0xF6715540
Cores / Checker Cores	6/6	6/3	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	10832	6224	10832	10832
Extension memory (KB)	5120	1024	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0
CDSP Cores	2	2	2	2

(table continues...)

Table 6 (continued) TC4Dx AB step (part 2)

***Note**: Variants marked with * are available on request only.*

Product Name	SAK-TC4D7XP-20MO500MC	SAK-TC4D9XC-20NF500MC	SAA-TC4D9XM-20MF500MC	SAA-TC4D9XP-20MF500CC*
HRPWM Instances	0	0	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 2.5 Gbps	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	1	2	2	2
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	0	0	0	0
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	30	10	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.2.3 TC4Dx AB step (part 3)

A continuation table listing the TC4Dx AB step variants.

Table 7 TC4Dx AB step (part 3)

Note: *Variants marked with * are available on request only.*

Product Name	SAK-TC4D9XP-20MF500CC*	SAK-TC4D9XQ-20MF500CC*	SAK-TC4D9XQ-20MO500CC*	SAK-TC4D9XP-20MO500CC*
Step	AB	AB	AB	AB
Production Status	Standard	Standard	Standard	Standard
Package Type	PG-F2HBGA-436	PG-F2HBGA-436	PG-F2HBGA-436	PG-F2HBGA-436
Pinout	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAK	SAK	SAK	SAK
Chip ID	0x76715540	0x7672D540	0x7672D5C0	0x767155C0
Cores / Checker Cores	6/6	6/6	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	10832	10832	10832	10832
Extension memory (KB)	5120	5120	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0
CDSP Cores	2	2	2	2

(table continues...)

Table 7 (continued) TC4Dx AB step (part 3)

***Note**: Variants marked with * are available on request only.*

Product Name	SAK-TC4D9XP-20MF500CC*	SAK-TC4D9XQ-20MF500CC*	SAK-TC4D9XQ-20MO500CC*	SAK-TC4D9XP-20MO500CC*
HRPWM Instances	0	0	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	2	2	2	2
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	0	1/4	1/4	0
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	30	30	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.2.4 TC4Dx AB step (part 4)

A continuation table listing the TC4Dx AB step variants.

Table 8 TC4Dx AB step (part 4)

Product Name	SAA-TC4D9XP-20MF500MC	SAK-TC4D9XP-20MF500MC	SAK-TC4D9XQ-20MF500MC	SAK-TC4D9XQ-20MO500MC
Step	AB	AB	AB	AB
Production Status	Standard	Standard	Standard	Standard
Package Type	PG-F2BGA-436	PG-F2BGA-436	PG-F2BGA-436	PG-F2BGA-436
Pinout	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm	BGA436_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAA	SAK	SAK	SAK
Chip ID	0xF6715542	0x76715542	0x7672D542	0x7672D5C2
Cores / Checker Cores	6/6	6/6	6/6	6/6
Max. Freq. (MHz)	500	500	500	500
NVM Type	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)	20	20	20	20
Data NVM0 (KB)	1024	1024	1024	1024
Total SRAM (without Cache) (KB)	10832	10832	10832	10832
Extension memory (KB)	5120	5120	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes	Yes	Yes
CSRM Available	1	1	1	1
PPU Availability				
ADC - TMADC (Instances / Cores)	4/8	4/8	4/8	4/8
ADC - Fast Compare Converters	0	0	0	0
ADC - DS Converters	0	0	0	0
CDSP Cores	2	2	2	2
HRPWM Instances	0	0	0	0

(table continues...)

Table 8 (continued) TC4Dx AB step (part 4)

Product Name	SAA-TC4D9XP-20MF500MC	SAK-TC4D9XP-20MF500MC	SAK-TC4D9XQ-20MF500MC	SAK-TC4D9XQ-20MO500MC
GTM Classic / eGTM availability	No / Yes	No / Yes	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)				
PCIe Instances	2	2	2	2
CAN (Modules/ Nodes)	5/5x4	5/5x4	5/5x4	5/5x4
CANXL (Modules/ Nodes)	0	0	1/4	1/4
FlexRay (Modules/ Channels)	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules	2	2	2	2
ASCLIN Modules	28	28	28	28
QSPI Modules	8	8	8	8
I2C Interfaces	3	3	3	3
xSPI Module	1	1	1	1
SENT Channels	30	30	30	30
MSC Modules	1	1	1	1
PSI5 Channels	2	2	2	2
PSI5-S Module	1	1	1	1
SDMMC Module	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces	0	0	0	0
SGBT availability	No	No	No	No
MCDS availability	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
CSI2 Interface	0	0	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0	No/0/0	No/0/0

2.2.5 TC4Dx AB step (part 5)

A continuation table listing the TC4Dx AB step variants.

Table 9 TC4Dx AB step (part 5)

Product Name	SAK-TC4D9XP-20MO500MC	SAA-TC4D7XP-20MF500MC
Step	AB	AB
Production Status	Standard	Standard
Package Type	PG-F2BGA-436	PG-F2BGA-292
Pinout	BGA436_COM 0.8 mm	BGA292_COM 0.8 mm
Reference Silicon	TC4Dx	TC4Dx
Temperature Range (Ambient)	SAK	SAA
Chip ID	0x767155C2	0xF5F15542
Cores / Checker Cores	6/6	6/6
Max. Freq. (MHz)	500	500
NVM Type	eFlash	eFlash
Program NVM (MB)	20	20
Data NVM0 (KB)	1024	1024
Total SRAM (without Cache) (KB)	10832	10832
Extension memory (KB)	5120	5120
DSPR (KB)	240 per CPU and CSRM	240 per CPU and CSRM
DLMU (KB)	512 per CPU	512 per CPU
PSPR (KB)	64 per CPU	64 per CPU
Hypervisor Support	Yes	Yes
CSRM Available	1	1
PPU Availability		
ADC - TMADC (Instances / Cores)	4/8	4/8
ADC - Fast Compare Converters	0	0
ADC - DS Converters	0	0
CDSP Cores	2	2
HRPWM Instances	0	0
GTM Classic / eGTM availability	No / Yes	No / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	2x 5 Gbps	2x 5 Gbps
Light Ethernet (LETH) Instances (Mbps)		
PCIe Instances	2	1
CAN (Modules/Nodes)	5/5x4	5/5x4

(table continues...)

Table 9 (continued) TC4Dx AB step (part 5)

Product Name	SAK-TC4D9XP-20MO500MC	SAA-TC4D7XP-20MF500MC
CANXL (Modules/Nodes)	0	0
FlexRay (Modules/Channels)	2/2x2	2/2x2
HSSL Modules	2	2
ASCLIN Modules	28	28
QSPI Modules	8	8
I2C Interfaces	3	3
xSPI Module	1	1
SENT Channels	30	30
MSC Modules	1	1
PSI5 Channels	2	2
PSI5-S Module	1	1
SDMMC Module	Yes	Yes
Audio-TDM/I2S interfaces	0	0
SGBT availability	No	No
MCDS availability	Limited MCDS	Limited MCDS
CSI2 Interface	0	0
Radar cluster (SPU, RIF) available / SPU instances / RIF Instance	No/0/0	No/0/0

3 Pin definition and functions

***Note**: Functions listed in the largest package of this device might not be available for smaller packages because of pin limitations.*

***Note**: *To fulfill the specified RMII timing requirements, it is necessary to select the correct alternate output function signal (e.g. LETH0_P2_RMIIB_TXEN) and the registered output signals of this (e.g. LETH0_P2_RMIIRB_TXEN) by writing the corresponding PCSR bitfield inside the PCSRSEL register of the pin slice.*

3.1 Logic symbols for package variants

The following figures show the logic symbols for the package variants.

- BGA-436 COM, see Figure 1
- BGA-292 COM, see Figure 2

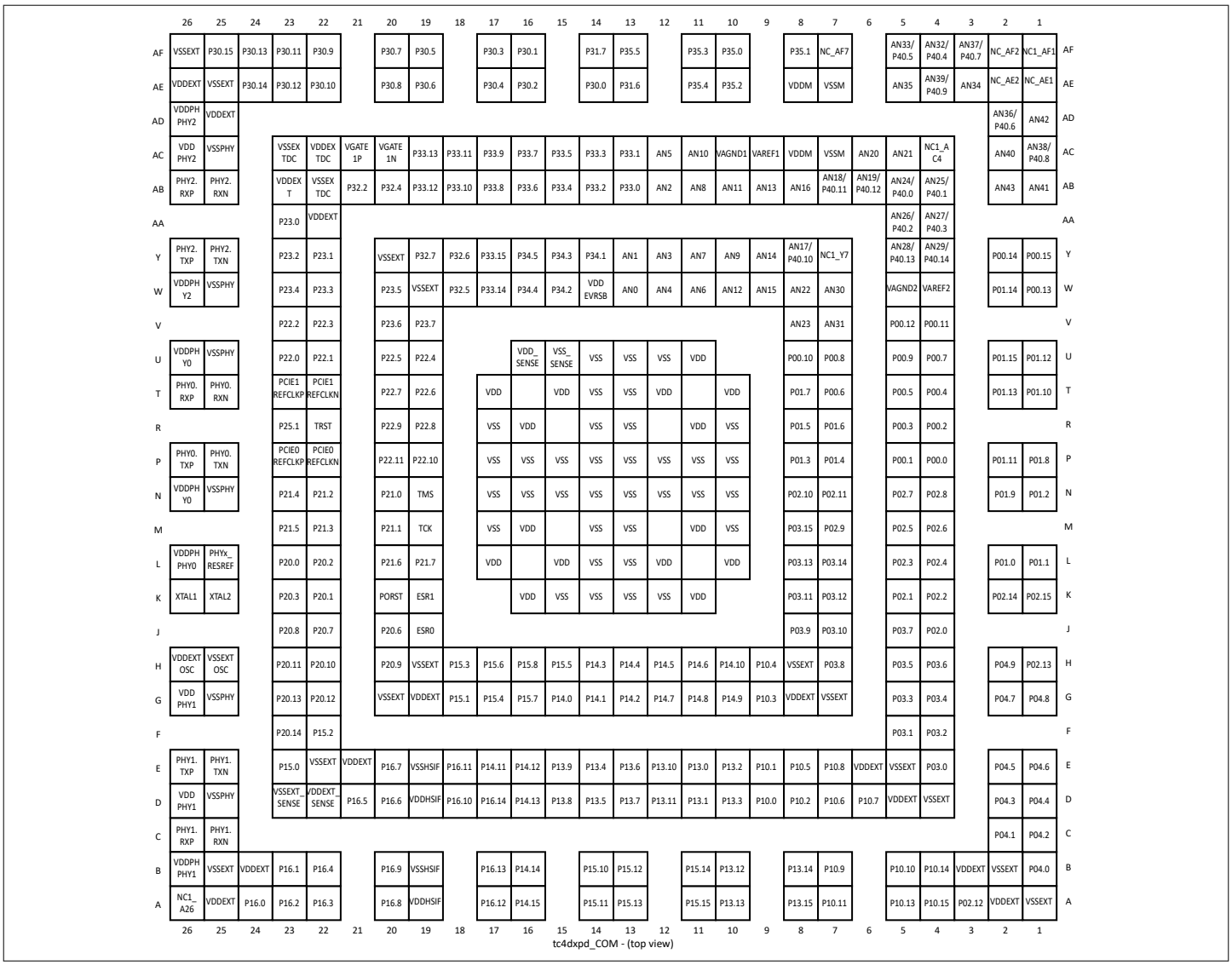

Figure 1 Logic symbol for the package variant BGA-436 COM

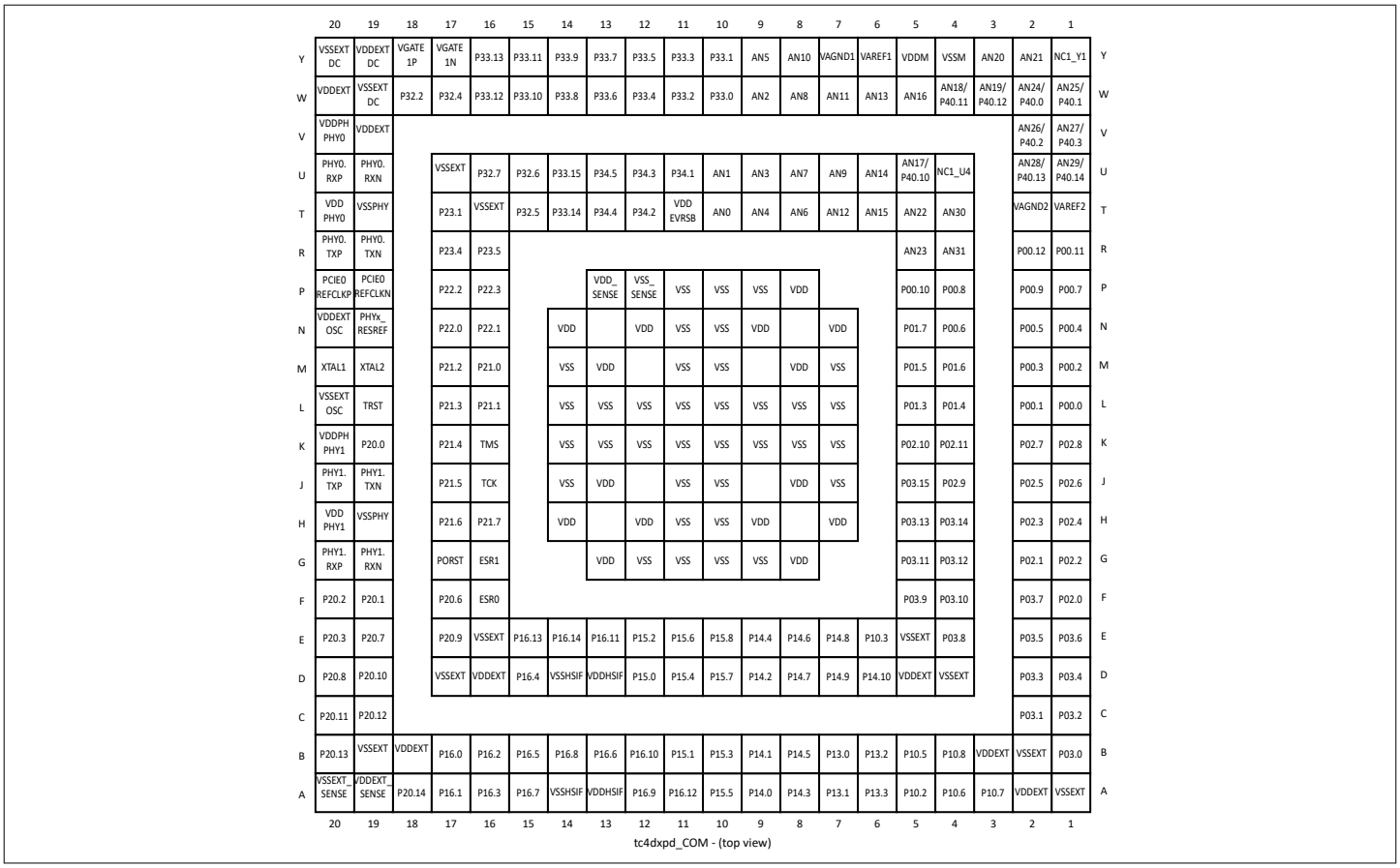

Figure 2 Logic symbol for the package variant BGA-292 COM

Related information

BGA436_COM package variant pin configuration on page 32
BGA292_COM package variant pin configuration on page 245
Pad Sequence on page 384
Legend on page 405

3.2 BGA436_COM package variant pin configuration

Related information

Logic symbols for package variants on page 31
BGA292_COM package variant pin configuration on page 245
Pad Sequence on page 384
Legend on page 405

3.2.1 BGA436_COM port 00

Table 10 Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
P4	P00.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	MSC0_INJ0			Injection signal from port
	GETH0_PX_MDIOA			PortX MDIO input
	EGTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	EGTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	P00.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT9	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	GETH0_PX_MDIO0	O		PortX MDIO output
P5	P00.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	SENT0_SENT0B			Receive input channel 0
	EGTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN2_11			Mux input channel 2 of TIM module 1

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH11	AI		Analog Input for TMADC2 Channel 11
	P00.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	SENT0_SPC0	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT10	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R4	P00.2	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT0B			Receive input channel 0
	ASCLIN24_ARXB_F			Receive input
	EGTM_CDTM1_DTM2_5			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_5			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH10	AI		Analog Input for TMADC2 Channel 10
	P00.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	CAN21_TXD	O3		CAN transmit output node 1
	PSI5_TX0	O4		TXD outputs (send data)
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI3_SLSO4	O6		Master slave select output
	—	O7		Reserved

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT11	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R5	P00.3	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	CAN21_RXDA			CAN receive input node 1
	PSI5S0_RXA			RX data input
	SENT0_SENT1B			Receive input channel 1
	ASCLIN12_ARXA_F			Receive input
	EGTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	EGTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	ADC_TMADC2CH9	AI		Analog Input for TMADC2 Channel 9
	P00.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	ASCLIN12_ATX_F	O3		Transmit output
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT12	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
T4	P00.4	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SCU_E_REQ2C			ERU channel 2 input C
	SENT1_SENT1B			Receive input channel 1
	ASCLIN10_ARXA			Receive input
	EGTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH8	AI		Analog Input for TMADC2 Channel 8
	P00.4	O0		General-purpose output
	—	O1		Reserved
	PSI5S0_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	—	O5		Reserved
	SENT1_SPC1	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT13	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T5	P00.5	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT2B			Receive input channel 2
	CAN11_RXDB			CAN receive input node 1
	ASCLIN12_ARXB_F			Receive input
	EGTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_2			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	ADC_TMADC2CH7	AI		Analog Input for TMADC2 Channel 7
	P00.5	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	SENT0_SPC2	O6		Transmit output
	LETH0_P3_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O8		CANXL transmit output node 3
	EGTM_TOUT14	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T7	P00.6	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	CANXL03_RXDC			CANXL receive input node 3
	SENT1_SENT2B			Receive input channel 2
	ASCLIN5_ARXA			Receive input
	EGTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	ADC_TMADC2CH6	AI		Analog Input for TMADC2 Channel 6
	P00.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC2	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT15	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U4	P00.7	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT3B			Receive input channel 3
	EGTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_3			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_3			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	ADC_TMADC2CH5	AI		Analog Input for TMADC2 Channel 5
	P00.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	SENT0_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT16	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U7	P00.8	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT3B			Receive input channel 3
	ASCLIN10_ARXB			Receive input
	EGTM_CDTM1_DTM3_2			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_10			Mux input channel 7 of TIM module 1
	EGTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	ADC_TMADC2CH4	AI		Analog Input for TMADC2 Channel 4
	P00.8	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	CAN40_TXD	O4		CAN transmit output node 0
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT17	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U5	P00.9	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT4B			Receive input channel 4
	ASCLIN13_ARXA_F			Receive input
	ASCLIN4_ARXG			Receive input
	EGTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	EGTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	ADC_TMADC2CH3	AI		Analog Input for TMADC2 Channel 3
	P00.9	O0		General-purpose output

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	ADC_EMUXCTRL13	O4		EMUX1 Control from TMADC to PORTS
	ASCLIN4_ATX	O5		Transmit output
	SENT0_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT18	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P3_MDC	O15		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
U8	P00.10	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT4B			Receive input channel 4
	ASCLIN10_ARXE			Receive input
	EGTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	ADC_TMADC2CH2	AI		Analog Input for TMADC2 Channel 2
	P00.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN13_ATX_F	O3		Transmit output
	ASCLIN4_ATX	O4		Transmit output
	—	O5		Reserved
	SENT1_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT19	O9		eGTM muxed output

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
V4	P00.11	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT5B			Receive input channel 5
	ASCLIN13_ARXB_F			Receive input
	CAN40_RXDA			CAN receive input node 0
	EGTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	ADC_TMADC2CH1	AI		Analog Input for TMADC2 Channel 1
	P00.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO	O2		Slave select signal output
	ASCLIN13_ATX_F	O3		Transmit output
	—	O4		Reserved
	ASCLIN24_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT20	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
V5	P00.12	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	SENT1_SENT5B			Receive input channel 5
	ASCLIN24_ARXA_F			Receive input
	LETH0_P3_RXDE			LETH PortX TC14 interface receive data input
	CANXL03_RXDE			CANXL receive input node 3
	EGTM_CDTM0_DTM2_5			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_5			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	ADC_TMADC2CH0	AI		Analog Input for TMADC2 Channel 0
	P00.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	ASCLIN24_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT21	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
W1	P00.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN12_ARXD			Receive input
	CAN40_RXDE			CAN receive input node 0

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P00.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	CLOCK_EXTCLK1	O4		External clock output 1
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT167	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
Y2	P00.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_MDIOG			LETH PortX MDIO interface data input
	LETH0_P3_EDG			LETH PortX TC14 interface energy detection input
	P00.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	CAN40_TXD	O6		CAN transmit output node 0
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT166	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 10 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
Y1	P00.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN40_RXDD			CAN receive input node 0
	P00.15	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN12_ATX	O3		Transmit output
	CLOCK_EXTCLK0	O4		External clock output 0
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT168	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 11 Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L2	P01.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN21_RXDE			CAN receive input node 1
	CAN03_RXDF			CAN receive input node 3
	ASCLIN6_ARXB			Receive input
	ASCLIN12_ARXE			Receive input
	EGTM_TIM2_IN6_13			Mux input channel 6 of TIM module 2

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P01.0	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P2_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL02_TXD	O8		CANXL transmit output node 2
	EGTM_TOUT155	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L1	P01.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY1_RXDA1			Receive Channel A1
	SENT0_SENT3C			Receive input channel 3
	LETH0_P2_RXDA			LETH PortX TC14 interface receive data input
	CANXL02_RXDA			CANXL receive input node 2
	P01.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	CAN40_TXD	O6		CAN transmit output node 0
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT159	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
N1	P01.2	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P2_EDE			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOE			LETH PortX MDIO interface data input
	P01.2	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	CAN03_TXD	O3		CAN transmit output node 3
	—	O4		Reserved
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT156	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
P8	P01.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_SLSIB			Slave select input
	SENT1_SENT12A			Receive input channel 12
	CAN32_RXDA			CAN receive input node 2
	LETH0_P0_MDIOB			LETH PortX MDIO interface data input
	LETH0_P0_EDB			LETH PortX TC14 interface energy detection input

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	EGTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	ADC_TMADC2CH14	AI		Analog Input for TMADC2 Channel 14
	P01.3	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	—	O3		Reserved
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT111	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
P7	P01.4	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN01_RXDC			CAN receive input node 1
	SENT0_SENT13A			Receive input channel 13
	EGTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	EGTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH13	AI		Analog Input for TMADC2 Channel 13
	P01.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN9_ASLSO_F	O3		Slave select signal output
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT112	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R8	P01.5	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MRSTC			Master SPI data input
	ASCLIN9_ARXA_F			Receive input
	SENT1_SENT13A			Receive input channel 13
	LETH0_P0_RXDG			LETH PortX TC14 interface receive data input
	CANXL00_RXDG			CANXL receive input node 0
	EGTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	EGTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH12	AI		Analog Input for TMADC2 Channel 12
	P01.5	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT113	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
R7	P01.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MTSRC			Slave SPI data input
	CAN32_RXDD			CAN receive input node 2
	EGTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	P01.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN12_ATX	O2		Transmit output
	ASCLIN9_ASCLK_F	O3		Shift clock output
	QSPI3_MTSR	O4		Master SPI data output
	ASCLIN9_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT114	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T8	P01.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_SCLKC			Slave SPI clock inputs
	ASCLIN9_ARXB_F			Receive input
	EGTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	P01.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN9_ATX_F	O3		Transmit output
	QSPI3_SCLK	O4		Master SPI clock output

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN26_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT115	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P1	P01.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN00_RXDF			CAN receive input node 0
	ERAY1_RXDB1			Receive Channel B1
	LETH0_P3_RXDA			LETH PortX TC14 interface receive data input
	SENT0_SENT4C			Receive input channel 4
	ASCLIN0_ARXC			Receive input
	CAN20_RXDE			CAN receive input node 0
	ASCLIN7_ARXB			Receive input
	CANXL03_RXDA			CANXL receive input node 3
	P01.8	O0		General-purpose output
	—	O1		Reserved
	SENT0_SPC4	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT162	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
N2	P01.9	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT3C			Receive input channel 3
	P01.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT160	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T1	P01.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT4C			Receive input channel 4
	P01.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ASCLK	O2		Shift clock output
	SENT1_SPC4	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT163	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P2	P01.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN13_ARXE			Receive input
	SENT1_SENT6C			Receive input channel 6
	LETH0_P2_COLB			LETH PortX MII collision detection
	P01.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ASLSO	O2		Slave select signal output
	SENT1_SPC6	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT165	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U1	P01.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MRSTH			Master SPI data input
	P01.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX	O2		Transmit output

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY1_TXDA	O6		Transmit Channel A
	LETH0_P2_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL02_TXD	O8		CANXL transmit output node 2
	EGTM_TOUT158	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T2	P01.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P01.13	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	ERAY1_TXDB	O6		Transmit Channel B
	LETH0_P3_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O8		CANXL transmit output node 3
	EGTM_TOUT161	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
W2	P01.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P2_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOA			LETH PortX MDIO interface data input

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN13_ARXD			Receive input
	P01.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY1_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT164	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
U2	P01.15	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P3_MDIOA			LETH PortX MDIO interface data input
	P01.15	O0		General-purpose output
	—	O1		Reserved
	ASCLIN13_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT157	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 11 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

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Table 12 Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
J4	P02.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXG			Receive input
	SCU_E_REQ3C			ERU channel 3 input C
	CAN31_RXDC			CAN receive input node 1
	ADC_TRIG56			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	P02.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLSO1_F	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	ERAY0_TXDA	O6		Transmit Channel A
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT0_F	O9		eGTM muxed output
	—	O10		Reserved
	QSPI3_SLSO5_F	O11		Master slave select output

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN8_ASCLK_F	O12		Shift clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K5	P02.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2B			ERU channel 2 input B
	SENT0_SENT14A			Receive input channel 14
	ADC_TRIG57			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	LETH0_P0_RXDC			LETH PortX TC14 interface receive data input
	CANXL00_RXDC			CANXL receive input node 0
	P02.1	O0		General-purpose output
	—	O1		Reserved
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT1_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
K4	P02.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT7B			Receive input channel 7
	EGTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_6			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	EGTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	P02.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3_F	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDB	O6		Transmit Channel B
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O8		CANXL transmit output node 1
	EGTM_TOUT2_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L5	P02.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	PSI5_RX0B			RXD inputs (receive data) channel 0
	SENT1_SENT6B			Receive input channel 6
	EGTM_CDTM0_DTM3_6			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM3_6			Input mux of CDTM1_DTM3_AUXIN0/1

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	LETH0_P1_RXDC			LETH PortX TC14 interface receive data input
	CANXL01_RXDC			CANXL receive input node 1
	P02.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT3_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
L4	P02.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT6B			Receive input channel 6
	QSPI3_SLSIA			Slave select input
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	EGTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	EGTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOC			LETH PortX MDIO interface data input
	P02.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0_F	O3		Master slave select output
	PSI5S0_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT4_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
M5	P02.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT1C			Receive input channel 1
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S0_RXB			RX data input
	QSPI3_MRSTA_F			Master SPI data input
	EGTM_CDTM1_DTM3_7			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM5_6			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM5_6			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	LETH0_P1_EDC			LETH PortX TC14 interface energy detection input

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIOC			LETH PortX MDIO interface data input
	P02.5	O0		General-purpose output
	—	O1		Reserved
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	—	O4		Reserved
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT5_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
M4	P02.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT0C			Receive input channel 0
	ASCLIN10_ARXH			Receive input
	QSPI3_MTSRA			Slave SPI data input
	EGTM_CDTM0_DTM2_7			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM2_7			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	P02.6	O0		General-purpose output
	—	O1		Reserved
	PSI5S0_TX	O2		TX data output

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI3_MTSR_F	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT6_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N5	P02.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDH			CAN receive input node 2
	SENT0_SENT1C			Receive input channel 1
	SCU_E_REQ0F			ERU channel 0 input F
	QSPI3_SCLKA			Slave SPI clock inputs
	ADC_TRIG58			Triggers from PORTS to ADC
	EGTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	EGTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	EGTM_CDTM2_DTM3_6			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI3_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT7_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N4	P02.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT0C			Receive input channel 0
	CAN30_RXDB			CAN receive input node 0
	SCU_E_REQ5G			ERU channel 5 input G
	ADC_TRIG59			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	P02.8	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO5_F	O2		Master slave select output
	ASCLIN8_ASCLK_F	O3		Shift clock output
	—	O4		Reserved
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	GETH0_P0_MDC	O6		Port0 MDIO Clock
	—	O7		Reserved
	GETH0_P1_MDC	O8		Port1 MDIO Clock
	EGTM_TOUT8_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
M7	P02.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT10B			Receive input channel 10
	ASCLIN8_ARXA			Receive input
	EGTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	EGTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM3_7			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	ASCLIN8_ATX_F	O3		Transmit output
	CAN30_TXD	O4		CAN transmit output node 0
	CAN01_TXD	O5		CAN transmit output node 1
	SENT0_SPC10	O6		Transmit output
	ADC_EMUXCTRL03	O7		EMUX0 Control from TMADC to PORTS
	—	O8		Reserved
	EGTM_TOUT116_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N8	P02.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXC			Receive input
	CAN01_RXDE			CAN receive input node 1
	SENT1_SENT10B			Receive input channel 10
	ASCLIN8_ARXB_F			Receive input
	EGTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM2_6			Input mux of CDTM1_DTM2_AUXIN0/1

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	EGTM_CDTM2_DTM2_7			Input mux of CDTM2_DTM2_AUXIN0/1
	P02.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT1_SPC10	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT117_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N7	P02.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT11B			Receive input channel 11
	ASCLIN26_ARXA_F			Receive input
	CAN30_RXDD			CAN receive input node 0
	SCU_E_REQ7G			ERU channel 7 input G
	EGTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	ADC_TMADC2CH15	AI		Analog Input for TMADC2 Channel 15
	P02.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN8_ASLSO_F	O3		Slave select signal output
	ASCLIN10_ATX	O4		Transmit output

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output
	ASCLIN26_ATX_F	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT118_F	O9		eGTM muxed output
	LETH0_P2_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A3	P02.12	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_COLA			LETH PortX MII collision detection
	SENT0_SENT7C			Receive input channel 7
	EGTM_CDTM0_DTM0_7			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM5_6			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM3_7			Input mux of CDTM0_DTM3_AUXIN0/1
	P02.12	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO11	O2		Master slave select output
	QSPI4_SLSO4	O3		Master slave select output
	ASCLIN6_ASLSO	O4		Slave select signal output
	—	O5		Reserved
	SENT0_SPC7	O6		Transmit output
	ASCLIN2_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT151_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
H1	P02.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN26_ARXB_F			Receive input
	SENT0_SENT2C			Receive input channel 2
	P02.13	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO7_F	O2		Master slave select output
	QSPI4_SLSO6	O3		Master slave select output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT153_F	O9		eGTM muxed output
	LETH0_P0_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K2	P02.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN20_RXDD			CAN receive input node 0
	CAN00_RXDH			CAN receive input node 0
	EGTM_CDTM2_DTM2_6			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM2_IN4_11			Mux input channel 4 of TIM module 2
	P02.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASCLK	O2		Shift clock output
	ASCLIN7_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 12 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT154_F	O9		eGTM muxed output
	LETH0_P3_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K1	P02.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_EDH			LETH PortX TC14 interface energy detection input
	LETH0_P3_MDIOH			LETH PortX MDIO interface data input
	EGTM_TIM2_IN5_13			Mux input channel 5 of TIM module 2
	P02.15	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO12_F	O2		Master slave select output
	QSPI4_SLSO5	O3		Master slave select output
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	ERAY1_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT152_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

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Table 13 Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E4	P03.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN11_ARXH			Receive input
	CAN30_RXDE			CAN receive input node 0
	QSPI6_MRSTC			Master SPI data input
	P03.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	QSPI3_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MRST	O8		Slave SPI data output
	EGTM_TOUT271	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIIB_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRB_TXEN	O		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKB - registered*)
F5	P03.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN5_ARXG			Receive input
	QSPI6_SCLKC			Slave SPI clock inputs
	P03.1	O0		General-purpose output
	—	O1		Reserved
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	—	O4		Reserved

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	CAN23_TXD	O7		CAN transmit output node 3
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT272	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
F4	P03.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDF			CAN receive input node 3
	QSPI6_MTSRA			Slave SPI data input
	P03.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT273	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G5	P03.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN19_ARXC			Receive input

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKB)
	QSPI7_MRSTH			Master SPI data input
	P03.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_MRST	O7		Slave SPI data output
	QSPI6_SLSO4	O8		Master slave select output
	EGTM_TOUT274	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G4	P03.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_CRSD			LETH PortX MII carrier sense
	ASCLIN8_ARXF			Receive input
	CAN11_RXDH			CAN receive input node 1
	QSPI6_SLSIA			Slave select input
	P03.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI3_SLSO0	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	ASCLIN19_ATX	O5		Transmit output
	CAN11_TXD	O6		CAN transmit output node 1
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI6_SLSO5	O8		Master slave select output

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT275	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H5	P03.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P03.5	O0		General-purpose output
	—	O1		Reserved
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_MTSR	O7		Master SPI data output
	QSPI6_SLSO6	O8		Master slave select output
	EGTM_TOUT276	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H4	P03.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN43_RXDC			CAN receive input node 3
	ERAY1_RXDB2			Receive Channel B2
	ASCLIN23_ARXC			Receive input
	P03.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN19_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_SLSO9	O7		Master slave select output
	QSPI6_SLSO7	O8		Master slave select output
	EGTM_TOUT277	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J5	P03.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_COLC			LETH PortX MII collision detection
	LETH0_P3_RXDC			LETH PortX TC14 interface receive data input
	QSPI7_MRSTC			Master SPI data input
	P03.7	O0		General-purpose output
	—	O1		Reserved
	CAN43_TXD	O2		CAN transmit output node 3
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT278	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H7	P03.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT6D			Receive input channel 6
	P03.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN2_ATX	O3		Transmit output
	ASCLIN8_ATX	O4		Transmit output
	CAN23_TXD	O5		CAN transmit output node 3
	SENT0_SPC6	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT279	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIIB_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRB_TXD1	O		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKB - registered*)
J8	P03.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI6_SLSIC			Slave select input
	SENT0_SENT11D			Receive input channel 11
	CAN01_RXDG			CAN receive input node 1
	P03.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN8_ASCLK	O3		Shift clock output
	ASCLIN12_ATX	O4		Transmit output

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT280	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIIB_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKB)
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
	LETH0_P2_RMIIRB_TXD0	O		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKB - registered*)
J7	P03.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN12_ARXC			Receive input
	ASCLIN8_ARXG			Receive input
	P03.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT281	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
K8	P03.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SDAA			Serial Data Input 0
	QSPI7_MTSRC			Slave SPI data input
	QSPI3_SLSIC			Slave select input
	ASCLIN23_ARXD			Receive input
	P03.11	O0		General-purpose output
	—	O1		Reserved
	I2C2_SDA	O2		Serial Data Output
	ASCLIN8_ASLSO	O3		Slave select signal output
	CAN22_TXD	O4		CAN transmit output node 2
	CAN31_TXD	O5		CAN transmit output node 1
	ASCLIN26_ATX	O6		Transmit output
	QSPI7_MTSR	O7		Master SPI data output
	CAN01_TXD	O8		CAN transmit output node 1
	EGTM_TOUT282	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K7	P03.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SCLA			Serial Clock Input 0
	CAN22_RXDF			CAN receive input node 2
	P03.12	O0		General-purpose output
	—	O1		Reserved
	I2C2_SCL	O2		Serial Clock Output
	ASCLIN23_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	QSPI7_SCLK	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT283	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L8	P03.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDF			CAN receive input node 2
	ASCLIN26_ARXD			Receive input
	P03.13	O0		General-purpose output
	—	O1		Reserved
	CAN02_TXD	O2		CAN transmit output node 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT284	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L7	P03.14	I	FAST / PU1 /	General-purpose input
	LETH0_P2_MDIOD			LETH PortX MDIO interface data input

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_EDD		VDDEXT / ES	LETH PortX TC14 interface energy detection input
	CAN01_RXDF			CAN receive input node 1
	QSPI3_MTSRD			Slave SPI data input
	P03.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX	O2		Transmit output
	ASCLIN12_ATX	O3		Transmit output
	ASCLIN9_ASCLK	O4		Shift clock output
	QSPI3_MTSR	O5		Master SPI data output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT285	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
M8	P03.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN11_ARXG			Receive input
	LETH0_P2_RXDD			LETH PortX TC14 interface receive data input
	P03.15	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX	O2		Transmit output
	CAN01_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 13 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT286	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

3.2.5 BGA436_COM port 04

Table 14 Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B1	P04.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT7D			Receive input channel 7
	P04.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN20_ATX	O2		Transmit output
	SENT0_SPC7	O3		Transmit output
	CAN01_TXD	O4		CAN transmit output node 1
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT287	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
C2	P04.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN20_ARXD			Receive input
	LETH0_P3_MII_RXERD			LETH PortX MII receive error (to be used with LETH0_P3_RXCLKD)
	SENT0_SENT4D			Receive input channel 4
	CAN20_RXDH			CAN receive input node 0
	CAN01_RXDH			CAN receive input node 1
	P04.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASCLK	O2		Shift clock output
	SENT0_SPC4	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT288	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
C1	P04.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P2_CRSA			LETH PortX MII carrier sense
	LETH0_P3_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P3_MDIOC			LETH PortX MDIO interface data input
	P04.2	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO12	O2		Master slave select output

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI4_SLSO5	O3		Master slave select output
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	ERAY1_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT289	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D2	P04.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_CRSA			LETH PortX MII carrier sense
	SENT1_SENT7D			Receive input channel 7
	CAN03_RXDH			CAN receive input node 3
	ASCLIN6_ARXH			Receive input
	P04.3	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	SENT1_SPC7	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT290	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_TXD	O12		LETH PortX TC14 interface transmit data output

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CANXL02_TXD	O13		CANXL transmit output node 2
	—	O14		Reserved
	—	O15		Reserved
D1	P04.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SDAB			Serial Data Input 1
	LETH0_P2_COLC			LETH PortX MII collision detection
	SENT1_SENT11D			Receive input channel 11
	LETH0_P2_RXDE			LETH PortX TC14 interface receive data input
	CANXL02_RXDD			CANXL receive input node 2
	P04.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	CAN42_TXD	O3		CAN transmit output node 2
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	CAN40_TXD	O6		CAN transmit output node 0
	—	O7		Reserved
	I2C2_SDA	O8		Serial Data Output
	EGTM_TOUT291	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E2	P04.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SCLB			Serial Clock Input 1
	LETH0_P2_MDIOG			LETH PortX MDIO interface data input
	LETH0_P2_CRSC			LETH PortX MII carrier sense
	CAN42_RXDF			CAN receive input node 2
	LETH0_P2_EDG			LETH PortX TC14 interface energy detection input

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P04.5	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	CAN03_TXD	O3		CAN transmit output node 3
	—	O4		Reserved
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	I2C2_SCL	O8		Serial Clock Output
	EGTM_TOUT292	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E1	P04.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_RXDH			LETH PortX TC14 interface receive data input
	ASCLIN0_ARXH			Receive input
	LETH0_P3_CRSB			LETH PortX MII carrier sense
	ASCLIN10_ARXF			Receive input
	CANXL03_RXDH			CANXL receive input node 3
	P04.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT188	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G2	P04.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI6_SLSIB			Slave select input
	SENT0_SENT11C			Receive input channel 11
	P04.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ATX	O2		Transmit output
	SENT0_SPC11	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT189	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G1	P04.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SDAC			Serial Data Input 2
	SENT0_SENT8D			Receive input channel 8
	LETH0_P2_MII_RXERD			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKD)

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P3_COLD			LETH PortX MII collision detection
	P04.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASLSO	O2		Slave select signal output
	SENT0_SPC8	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C2_SDA	O8		Serial Data Output
	EGTM_TOUT36	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H2	P04.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SCLC			Serial Clock Input 2
	SENT1_SENT12C			Receive input channel 12
	LETH0_P3_CRSC			LETH PortX MII carrier sense
	EGTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	P04.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASCLK	O2		Shift clock output
	SENT1_SPC12	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C2_SCL	O8		Serial Clock Output
	EGTM_TOUT37	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 14 (continued) Port 04 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 15 Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D9	P10.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN11_ARXA			Receive input
	GETH0_P0_RXERC			Port0 MII Receive Error
	SENT0_SENT13B			Receive input channel 13
	QSPI7_MRSTB			Master SPI data input
	EGTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	SENT1_SENT10C			Receive input channel 10
	CAN41_RXDE			CAN receive input node 1
	LETH0_P2_MII_RMII_RXD0B			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD0D			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	LETH0_P2_RXDF			LETH PortX TC14 interface receive data input
	P10.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10_F	O3		Master slave select output
	CAN30_TXD	O4		CAN transmit output node 0
	—	O5		Reserved
	ASCLIN22_ATX_F	O6		Transmit output
	CANXL00_TXD	O7		CANXL transmit output node 0
	QSPI7_SLSO0	O8		Master slave select output

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT102	O9		eGTM muxed output
	ASCLIN0_ATX	O10		Transmit output
	—	O11		Reserved
	ERAY0_TXDA	O12		Transmit Channel A
	ERAY1_TXDB	O13		Transmit Channel B
	CAN01_TXD	O14		CAN transmit output node 1
	ASCLIN0_ASCLK	O15		Shift clock output
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E9	P10.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI1_MRSTA_F			Master SPI data input
	EGTM_CDTM0_DTM0_2			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_2			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM4_3			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_3			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM1_5			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	LETH0_P2_MII_RXD3B			LETH PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKB)
	ASCLIN0_ARXF			Receive input
	SENT0_SENT10C			Receive input channel 10
	P10.1	O0		General-purpose output
	—	O1		Reserved
	QSPI1_MTSR_F	O2		Master SPI data output
	QSPI1_MRST_F	O3		Slave SPI data output
	MSC0_EN1	O4		Chip Select
	—	O5		Reserved
	ASCLIN0_ATX	O6		Transmit output
	CAN41_TXD	O7		CAN transmit output node 1
	QSPI7_SLSO1	O8		Master slave select output
	EGTM_TOUT103	O9		eGTM muxed output
	LETH0_P2_TXD	O10		LETH PortX TC14 interface transmit data output

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D8	P10.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	SCU_E_REQ2A			ERU channel 2 input A
	EGTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	LETH0_P2_MII_RXD2B			LETH PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKB)
	ASCLIN22_ARXC_F			Receive input
	P10.2	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI1_SCLK_F	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	ASCLIN2_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	QSPI7_SLSO2	O8		Master slave select output
	EGTM_TOUT104	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO1	O12		Master slave select output
	—	O13		Reserved

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
G9	P10.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3A			ERU channel 3 input A
	ASCLIN2_ARXH_F			Receive input
	MSC0_SDI5			Upstream assynchronous input signal
	EGTM_CDTM0_DTM3_2			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM2_5			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	EGTM_CDTM2_DTM3_3			Input mux of CDTM2_DTM3_AUXIN0/1
	LETH0_P2_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_RMII_CRSDVD			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_MII_RXDVD			Receive data valid and Carrier sense and receive data valid
	P10.3	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI1_MTSR_F	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	QSPI7_SCLK	O8		Master SPI clock output
	EGTM_TOUT105	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO15	O12		Master slave select output
	ASCLIN1_ASLSO	O13		Slave select signal output
	ASCLIN3_ASLSO	O14		Slave select signal output

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
H9	P10.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI1_MTSRC			Slave SPI data input
	ASCLIN11_ARXB			Receive input
	ASCLIN22_ARXA_F			Receive input
	CAN30_RXDA			CAN receive input node 0
	EGTM_CDTM2_DTM2_3			Input mux of CDTM2_DTM2_AUXIN0/1
	LETH0_P2_CRSB			LETH PortX MII carrier sense
	EGTM_CDTM2_DTM3_5			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	P10.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN22_ATX_F	O2		Transmit output
	QSPI1_SLSO8_F	O3		Master slave select output
	QSPI1_MTSR_F	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
	QSPI7_MTSR	O8		Master SPI data output
	EGTM_TOUT106	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E8	P10.5	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	QSPI1_MRSTE			Master SPI data input
	CAN20_RXDA			CAN receive input node 0
	MSC0_INJ1			Injection signal from port
	ASCLIN22_ARXB_F			Receive input
	EGTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI5_MRSTE			Master SPI data input
	EGTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	LETH0_P3_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P3_RXCLKC)
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX_F	O2		Transmit output
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	—	O5		Reserved
	ASCLIN22_ATX	O6		Transmit output
	—	O7		Reserved
	QSPI1_MRST	O8		Slave SPI data output
	EGTM_TOUT107	O9		eGTM muxed output
	QSPI5_MRST	O10		Slave SPI data output
	LETH0_P3_TXD	O11		LETH PortX TC14 interface transmit data output
	—	O12		Reserved
	ERAY0_TXDB	O13		Transmit Channel B
	ERAY1_TXDB	O14		Transmit Channel B
	—	O15		Reserved
D7	P10.6	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXD_F			Receive input
	QSPI3_MTSRB			Slave SPI data input
	ASCLIN7_ARXH			Receive input
	SENT1_SENT12B			Receive input channel 12
	ASCLIN23_ARXA_F			Receive input
	EGTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P3_MDIOF			LETH PortX MDIO interface data input
	LETH0_P3_EDF			LETH PortX TC14 interface energy detection input
	QSPI1_MRSTC_F			Master SPI data input
	EGTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK_F	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	QSPI1_MRST_F	O6		Slave SPI data output
	ERAY1_TXENB	O7		Transmit Enable Channel B
	—	O8		Reserved
	EGTM_TOUT108	O9		eGTM muxed output
	QSPI5_MTSR	O10		Master SPI data output
	—	O11		Reserved
	QSPI2_SLSO14	O12		Master slave select output
	CAN13_TXD	O13		CAN transmit output node 3
	ERAY0_TXENB	O14		Transmit Enable Channel B
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D6	P10.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ACTSA_F			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0B			ERU channel 0 input B
	ASCLIN23_ARXB			Receive input
	ERAY1_RXDB3			Receive Channel B3
	CAN10_RXDH			CAN receive input node 0
	CAN13_RXDH			CAN receive input node 3
	ASCLIN9_ARXG			Receive input
	ASCLIN20_ARXC_F			Receive input
	CANXL00_RXDE			CANXL receive input node 0
	QSPI7_MTSRD			Slave SPI data input
	EGTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	LETH0_P3_RXDF			LETH PortX TC14 interface receive data input
	LETH0_P2_REFCLKB			LETH PortX RMII reference clock
	LETH0_P2_RXCLKB			LETH PortX MII receive clock
	LETH0_P2_REFCLKD			MII or RMII Clock from PAD
	LETH0_P2_RXCLKD			LETH PortX MII receive clock
	P10.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN23_ATX_F	O2		Transmit output
	QSPI3_MRST	O3		Slave SPI data output
	ASCLIN9_ATX	O4		Transmit output
	CAN20_TXD	O5		CAN transmit output node 0
	CAN12_TXD	O6		CAN transmit output node 2
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI7_MRST	O8		Slave SPI data output
	EGTM_TOUT109	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN0_ARTS	O12		Ready to send output
	QSPI2_SLSO13	O13		Master slave select output
	—	O14		Reserved
	ASCLIN20_ATX_F	O15		Transmit output
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E7	P10.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN12_RXDB			CAN receive input node 2
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1B			ERU channel 1 input B
	QSPI1_SLSIC			Slave select input
	CAN20_RXDB			CAN receive input node 0
	SENT1_SENT14A			Receive input channel 14
	CAN02_RXDG			CAN receive input node 2
	ERAY1_RXDA3			Receive Channel A3

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_MRSTG			Master SPI data input
	EGTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	LETH0_P2_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD1D			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	P10.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ARTS_F	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	ASCLIN23_ATX_F	O4		Transmit output
	ASCLIN5_ASLSO	O5		Slave select signal output
	ASCLIN7_ASLSO	O6		Slave select signal output
	ASCLIN20_ATX_F	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT110	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B7	P10.9	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT7C			Receive input channel 7
	ASCLIN6_ARXD			Receive input
	QSPI5_MTSRF			Slave SPI data input
	LETH0_P2_MDIOB			LETH PortX MDIO interface data input
	LETH0_P2_EDB			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN1_10			Mux input channel 1 of TIM module 0
	LETH0_P2_MII_RXD3D			LETH PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKD)
	P10.9	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN23_TXD	O2		CAN transmit output node 3
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	ERAY1_TXENA	O7		Transmit Enable Channel A
	ERAY1_TXENB	O8		Transmit Enable Channel B
	EGTM_TOUT265	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B5	P10.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT8C			Receive input channel 8
	CAN23_RXDH			CAN receive input node 3
	QSPI2_MRSTH			Master SPI data input
	LETH0_P2_COLA			LETH PortX MII collision detection
	EGTM_TIM0_IN2_11			Mux input channel 2 of TIM module 0
	P10.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	ERAY1_TXDA	O7		Transmit Channel A
	—	O8		Reserved
	EGTM_TOUT266	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_TXD	O11		LETH PortX TC14 interface transmit data output
	CANXL02_TXD	O12		CANXL transmit output node 2
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A7	P10.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT9C			Receive input channel 9
	LETH0_P2_RXDB			LETH PortX TC14 interface receive data input
	CANXL02_RXDB			CANXL receive input node 2
	EGTM_TIM0_IN5_9			Mux input channel 5 of TIM module 0
	LETH0_P2_MII_RXD2D			LETH PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKD)
	P10.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT269	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A5	P10.13	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT9C			Receive input channel 9
	QSPI5_SCLKC			Slave SPI clock inputs

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN4_9			Mux input channel 4 of TIM module 0
	LETH0_P3_TXCLKB			PortX MII transmit clock
	P10.13	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASLSO	O2		Slave select signal output
	QSPI5_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	QSPI7_SLSO14	O8		Master slave select output
	EGTM_TOUT268	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B4	P10.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT8C			Receive input channel 8
	CAN22_RXDG			CAN receive input node 2
	MSC0_SDI6			Upstream assynchronous input signal
	EGTM_TIM0_IN3_11			Mux input channel 3 of TIM module 0
	LETH0_P2_TXCLKB			PortX MII transmit clock
	P10.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	ASCLIN7_ATX	O3		Transmit output
	—	O4		Reserved
	CAN23_TXD	O5		CAN transmit output node 3
	QSPI5_SLSO15	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO13	O8		Master slave select output

(table continues...)

Table 15 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT267	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A4	P10.15	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN5_ARXF			Receive input
	ASCLIN7_ARXG			Receive input
	CAN23_RXDG			CAN receive input node 3
	LETH0_P2_MDIOF			LETH PortX MDIO interface data input
	LETH0_P2_EDF			LETH PortX TC14 interface energy detection input
	QSPI1_MRSTF			Master SPI data input
	EGTM_TIM0_IN6_9			Mux input channel 6 of TIM module 0
	LETH0_P2_TXCLKD			PortX MII transmit clock
	P10.15	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	QSPI5_SLSO14	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO12	O8		Master slave select output
	EGTM_TOUT270	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

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Table 16 Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E11	P13.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN10_ARXC_F			Receive input
	ASCLIN21_ARXA_F			Receive input
	QSPI2_MRSTG_F			Master SPI data input
	CAN11_RXDG			CAN receive input node 1
	EGTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	P13.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ATX_F	O2		Transmit output
	QSPI2_SCLKN_F	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
	—	O8		Reserved
	EGTM_TOUT91	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D11	P13.1	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD_F			Receive input
	EGTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	P13.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI2_SCLKP_F	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
	QSPI2_SCLK_F	O8		Master SPI clock output
	EGTM_TOUT92	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E10	P13.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SDAB			Serial Data Input 1
	CAN33_RXDA			CAN receive input node 3
	EGTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	P13.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASCLK_F	O2		Shift clock output
	QSPI2_MTSRN_F	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	ASCLIN21_ATX_F	O7		Transmit output
	QSPI2_MTSR_F	O8		Master SPI data output
	EGTM_TOUT93	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D10	P13.3	I	LVDS_TX / FAST /	General-purpose input
	ASCLIN21_ARXB			Receive input

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN0_3		PU1 / VDDEXT / ES	Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASLSO_F	O2		Slave select signal output
	QSPI2_MTSRP_F	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	ASCLIN21_ATX_F	O6		Transmit output
	CAN33_TXD	O7		CAN transmit output node 3
	—	O8		Reserved
	EGTM_TOUT94	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E14	P13.4	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SCLF			Serial Clock Input 5
	ASCLIN19_ARXF			Receive input
	CAN42_RXDD			CAN receive input node 2
	LETH0_P3_REFCLKB			LETH PortX RMII reference clock
	LETH0_P3_RXCLKB			LETH PortX MII receive clock
	P13.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN19_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	CAN23_TXD	O7		CAN transmit output node 3
	—	O8		Reserved
	EGTM_TOUT253	O9		eGTM muxed output

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D14	P13.5	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDD			CAN receive input node 3
	I2C0_SDAF			Serial Data Input 5
	LETH0_P3_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	P13.5	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	CAN42_TXD	O4		CAN transmit output node 2
	—	O5		Reserved
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT254	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E13	P13.6	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN10_RXDF			CAN receive input node 0
	LETH0_P3_MDIOD			LETH PortX MDIO interface data input
	LETH0_P3_EDD			LETH PortX TC14 interface energy detection input
	LETH0_P3_MDIOE			LETH PortX MDIO interface data input
	LETH0_P3_EDE			LETH PortX TC14 interface energy detection input

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P3_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P3_RXCLKB or LETH0_P3_REFCLKB)
	P13.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI7_MTSR	O8		Master SPI data output
	EGTM_TOUT255	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D13	P13.7	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_RXDD			LETH PortX TC14 interface receive data input
	ASCLIN19_ARXE			Receive input
	CAN43_RXDD			CAN receive input node 3
	LETH0_P3_MII_RMII_RXD0B			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P3_RXCLKB or LETH0_P3_REFCLKB)
	P13.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT256	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D15	P13.8	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	CAN21_RXDG			CAN receive input node 1
	P13.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	CAN43_TXD	O3		CAN transmit output node 3
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT39	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIB_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P3_TXCLKB)
	LETH0_P3_RMIIB_TXD0	O12		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P3_REFCLKB)
	LETH0_P3_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_RMIIRB_TXD0	O		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P3_REFCLKB - registered*)
E15	P13.9	I	FAST / PU1 /	General-purpose input
	I2C1_SCLB			Serial Clock Input 1

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN33_RXDE		VDDEXT / ES	CAN receive input node 3
	EGTM_TIM2_IN7_10			Mux input channel 7 of TIM module 2
	P13.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	QSPI5_SLSO5	O3		Master slave select output
	—	O4		Reserved
	CAN21_TXD	O5		CAN transmit output node 1
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT248	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIB_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P3_TXCLKB)
	LETH0_P3_RMIIB_TXD1	O12		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P3_REFCLKB)
	LETH0_P2_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_RMIIRB_TXD1	O		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P3_REFCLKB - registered*)
E12	P13.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P2_RXDG			LETH PortX TC14 interface receive data input
	QSPI5_MRSTH			Master SPI data input
	QSPI7_SCLKA			Slave SPI clock inputs
	P13.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT251	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P3_TXCLKB)
	LETH0_P3_RMIIB_TXEN	O12		LETH PortX RMII transmit enable (to be used with LETH0_P3_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	LETH0_P3_RMIIRB_TXEN	O		LETH PortX RMII transmit enable (to be used with LETH0_P3_REFCLKB - registered*)
D12	P13.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN0_ARXE			Receive input
	ASCLIN7_ARXD_F			Receive input
	QSPI5_SLSIC			Slave select input
	P13.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CAN33_TXD	O7		CAN transmit output node 3
	—	O8		Reserved
	EGTM_TOUT250	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIB_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P3_TXCLKB)
	LETH0_P2_MIIC_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
B10	P13.12	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXH			Receive input
	I2C1_SDAB			Serial Data Input 1
	CAN21_RXDB			CAN receive input node 1
	I2C1_SDAF			Serial Data Input 5
	EGTM_TIM0_IN0_11			Mux input channel 0 of TIM module 0
	P13.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX_F	O2		Transmit output
	QSPI5_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT249	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P3_TXCLKB)
	LETH0_P2_MIIC_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A10	P13.13	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	I2C1_SCLF			Serial Clock Input 5
	CAN33_RXDD			CAN receive input node 3
	P13.13	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ASCLK_F	O2		Shift clock output
	QSPI5_SLSO0	O3		Master slave select output
	—	O4		Reserved

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output
	EGTM_TOUT262	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIB_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P3_TXCLKB)
	LETH0_P2_MIIC_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B8	P13.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN10_ARXG			Receive input
	QSPI5_MTSRC			Slave SPI data input
	LETH0_P3_MII_RXD2C			LETH PortX MII receive data bit 2 (to be used with LETH0_P3_RXCLKC)
	P13.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_MTSR	O3		Master SPI data output
	CAN42_TXD	O4		CAN transmit output node 2
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI5_SLSO4	O8		Master slave select output
	EGTM_TOUT252	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 16 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A8	P13.15	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN21_ARXF_F			Receive input
	CAN42_RXDE			CAN receive input node 2
	QSPI5_SCLKD			Slave SPI clock inputs
	LETH0_P3_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P3_RXCLKC)
	P13.15	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ASLSO_F	O2		Slave select signal output
	QSPI5_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ASCLIN10_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT264	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 17 Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
G15	P14.0	I	FAST / PU1 / VDDEXT / ES2	General-purpose input
	SENT1_SENT8D			Receive input channel 8
	CAN41_RXDB			CAN receive input node 1
	EGTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	LETH0_P2_REFCLKA			LETH PortX RMII reference clock

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_RXCLKA			LETH PortX MII receive clock
	LETH0_P2_REFCLKC			MII or RMII Clock from PAD
	LETH0_P2_RXCLKC			LETH PortX MII receive clock
	P14.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT80	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P1_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O15		CANXL transmit output node 1
G14	P14.1	I	FAST / PU1 / VDDEXT / ES2	General-purpose input
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA_F			Receive input
	SENT0_SENT9D			Receive input channel 9
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3B			ERU channel 3 input B
	LETH0_P0_RXDB			LETH PortX TC14 interface receive data input
	CANXL00_RXDB			CANXL receive input node 0
	EGTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	PMS_PINAWKP			PINA (P14.1) pin input
	LETH0_P2_MII_RMII_RXD0A			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	CAN41_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT81	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G13	P14.2	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	LETH0_P2_MII_RXERA			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKA)
	LETH0_P2_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKC)
	LETH0_P1_RXDD			LETH PortX TC14 interface receive data input
	CANXL01_RXDD			CANXL receive input node 1
	EGTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO1	O3		Master slave select output

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved
	GETH0_P0_PPS0B	O8		GETH Port0 Pulse Per Second (output A or B)
	EGTM_TOUT82	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P0_PPS	O13		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H14	P14.3	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream assynchronous input signal
	SCU_E_REQ1A			ERU channel 1 input A
	LETH0_P1_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	PMS_HWCFG3IN			HWCFG3 pin input
	LETH0_P2_MII_RMII_RXD1A			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P0_PPS0A	O8		GETH Port0 Pulse Per Second (output A or B)
	EGTM_TOUT83	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O15		CANXL transmit output node 3
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
H13	P14.4	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	EGTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_1			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_1			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	PMS_HWCFG6IN			HWCFG6 pin input
	LETH0_P1_RXDA			LETH PortX TC14 interface receive data input
	CANXL01_RXDA			CANXL receive input node 1
	P14.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN0_ARTS_F	O3		Ready to send output
	QSPI2_SLSO4	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P1_PPS1A	O8		GETH Port1 Pulse Per Second (output A or B)
	EGTM_TOUT84	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIIA_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)
	LETH0_P3_MIIC_TXD3	O13		LETH PortX MII transmit data bit 3 (to be used with LETH0_P3_TXCLKC)
	LETH0_P3_MDC	O14		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H12	P14.5	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	QSPI5_MRSTB			Master SPI data input
	EGTM_CDTM2_DTM4_1			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P2_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	QSPI2_SLSO4_F	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	ERAY1_TXDB	O7		Transmit Channel B
	—	O8		Reserved
	EGTM_TOUT85	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CANXL03_TXD	O15		CANXL transmit output node 3
H11	P14.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI5_MTSRB			Slave SPI data input
	LETH0_P2_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOC			LETH PortX MDIO interface data input
	LETH0_P2_MII_RXD2C			LETH PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	P14.6	O0		General-purpose output
	—	O1		Reserved
	QSPI5_MTSR	O2		Master SPI data output
	QSPI2_SLSO2_F	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	ASCLIN0_ASLSO	O5		Slave select signal output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	ERAY1_TXENB	O7		Transmit Enable Channel B
	—	O8		Reserved
	EGTM_TOUT86	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
G12	P14.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDB0			Receive Channel B0
	ERAY1_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN20_ARXA			Receive input
	QSPI7_MTSRA			Slave SPI data input
	LETH0_P2_RXDC			LETH PortX TC14 interface receive data input
	CANXL02_RXDC			CANXL receive input node 2
	EGTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	P14.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ARTS_F	O2		Ready to send output
	QSPI2_SLSO4_F	O3		Master slave select output
	ASCLIN9_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN20_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT87	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	LETH0_P2_RMIIRA_TXEN	O		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA - registered*)
G11	P14.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	ERAY1_RXDA0			Receive Channel A0

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_MRSTA			Master SPI data input
	LETH0_P0_RXDA			LETH PortX TC14 interface receive data input
	CANXL00_RXDA			CANXL receive input node 0
	EGTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	LETH0_P2_TXCLKA			PortX MII transmit clock
	LETH0_P2_TXCLKC			PortX MII transmit clock
	P14.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO_F	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN20_ATX	O7		Transmit output
	GETH0_P1_PPS1B	O8		GETH Port1 Pulse Per Second (output A or B)
	EGTM_TOUT88	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G10	P14.9	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN0_ACTSA			Clear to send input
	QSPI2_MRSTFN_F			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	ASCLIN20_ARXB			Receive input
	LETH0_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOA			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	P14.9	O0		General-purpose output

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	CAN23_TXD	O2		CAN transmit output node 3
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	ERAY1_TXENA	O7		Transmit Enable Channel A
	—	O8		Reserved
	EGTM_TOUT89	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
	LETH0_P2_RMIIRA_TXD1	O		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA - registered*)
H10	P14.10	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDA			CAN receive input node 3
	QSPI2_MRSTFP_F			Master SPI data input (LVDS P line)
	EGTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	P14.10	O0		General-purpose output
	—	O1		Reserved
	QSPI5_SCLK	O2		Master SPI clock output
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	ERAY1_TXDA	O7		Transmit Channel A

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_RMIIA_TXD0	O8		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA)
	EGTM_TOUT90	O9		eGTM muxed output
	LETH0_P2_MIIA_TXD0	O10		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKC)
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL02_TXD	O15		CANXL transmit output node 2
	LETH0_P2_RMIIRA_TXD0	O		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA - registered*)
E17	P14.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	MSC0_SDI4			Upstream assynchronous input signal
	P14.11	O0		General-purpose output
	—	O1		Reserved
	CAN23_TXD	O2		CAN transmit output node 3
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT258	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKC)
	LETH0_P3_MIIC_TXER	O13		LETH PortX MII transmit error (to be used with LETH0_P3_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E16	P14.12	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P0_RXDH			LETH PortX TC14 interface receive data input
	CANXL00_RXDH			CANXL receive input node 0
	P14.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	ASCLIN7_ASCLK_F	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	QSPI5_SLSO6	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO4	O8		Master slave select output
	EGTM_TOUT261	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)
	LETH0_P3_MIIC_TXD3	O13		LETH PortX MII transmit data bit 3 (to be used with LETH0_P3_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D16	P14.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI5_SCLKB			Slave SPI clock inputs
	ASCLIN20_ARXE			Receive input
	LETH0_P0_MDIOG			LETH PortX MDIO interface data input
	LETH0_P0_EDG			LETH PortX TC14 interface energy detection input
	P14.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_SCLK	O3		Master SPI clock output
	—	O4		Reserved

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	QSPI7_SLSO3	O8		Master slave select output
	EGTM_TOUT260	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	LETH0_P3_MIIC_TXD2	O13		LETH PortX MII transmit data bit 2 (to be used with LETH0_P3_TXCLKC)
	MSC0_EN1	O14		Chip Select
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B16	P14.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN22_RXDD			CAN receive input node 2
	LETH0_P2_MII_RXD2A			LETH PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKA)
	LETH0_P3_MII_RXD2B			LETH PortX MII receive data bit 2 (to be used with LETH0_P3_RXCLKB)
	P14.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	ASCLIN7_ATX_F	O3		Transmit output
	—	O4		Reserved
	CAN23_TXD	O5		CAN transmit output node 3
	QSPI5_SLSO7	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO6	O8		Master slave select output
	EGTM_TOUT259	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 17 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	MSC0_EN0	O14		Chip Select
	LETH0_P1_MDC	O15		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A16	P14.15	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN5_ARXD			Receive input
	ASCLIN7_ARXA_F			Receive input
	CAN23_RXDC			CAN receive input node 3
	LETH0_P2_MII_RXD3A			LETH PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKA)
	LETH0_P3_MII_RXD3B			LETH PortX MII receive data bit 3 (to be used with LETH0_P3_RXCLKB)
	P14.15	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	QSPI5_SLSO8	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO7	O8		Master slave select output
	EGTM_TOUT263	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 18 Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E23	P15.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SDMMC0_DAT7_IN			Read data in
	EGTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	LETH0_P3_REFCLKA			RMII Clock from PAD
	LETH0_P3_RXCLKA			LETH PortX MII receive clock
	LETH0_P3_REFCLKC			RMII Clock from PAD
	LETH0_P3_RXCLKC			LETH PortX MII receive clock
	P15.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	ASCLIN1_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT71	O9		eGTM muxed output
	—	O10		Reserved
	CANXL00_TXD	O11		CANXL transmit output node 0
	—	O12		Reserved
	LETH0_P3_TXD	O13		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O14		CANXL transmit output node 3
	—	O15		Reserved
	SDMMC0_DAT7	O		Write data out
G18	P15.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA_F			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7B			ERU channel 7 input B
	LETH0_P0_RXDE			LETH PortX TC14 interface receive data input
	LETH0_P3_RXDB			LETH PortX TC14 interface receive data input
	CANXL03_RXDB			CANXL receive input node 3

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	LETH0_P3_MII_RXDVA			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_RMII_CRSDVA			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid
	P15.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	SDMMC0_CLK	O7		Card clock
	—	O8		Reserved
	EGTM_TOUT72	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
F22	P15.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	SENT0_SENT5D			Receive input channel 5
	QSPI2_MRSTE			Master SPI data input
	EGTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	XSPI0_RXD3B			Receive data
	LETH0_P3_TXCLKA			PortX MII transmit clock
	LETH0_P3_TXCLKC			PortX MII transmit clock
	P15.2	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SLSO0	O3		Master slave select output
	ASCLIN1_ATX_F	O4		Transmit output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK	O6		Shift clock output
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT73	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB3	O		Transmit data
H18	P15.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	SDMMC0_CMD_IN			Command in
	EGTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	LETH0_P2_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid
	P15.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT74	O9		eGTM muxed output

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	LETH0_P3_MIIA_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P3_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_CMD	O		Command out
G17	P15.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0A			ERU channel 0 input A
	SENT1_SENT5D			Receive input channel 5
	CAN42_RXDB			CAN receive input node 2
	QSPI7_MRSTF_F			Master SPI data input
	LETH0_P3_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P3_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	P15.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	ASCLIN19_ATX_F	O4		Transmit output
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	QSPI7_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT75	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P3_TXCLKC)

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P3_RMIIA_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P3_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
H15	P15.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN1_ARXB_F			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4D			ERU channel 4 input D
	EGTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	P15.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	CAN42_TXD	O4		CAN transmit output node 2
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT76	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P3_TXCLKC)
	LETH0_P3_RMIIA_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P3_REFCLKA)
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
H17	P15.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MTSRB			Slave SPI data input
	ASCLIN19_ARXA_F			Receive input

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	LETH0_P3_MII_RMII_RXD1A			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P3_RXCLKA or LETH0_P3_REFCLKA)
	LETH0_P3_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P3_RXCLKC or LETH0_P3_REFCLKC)
	P15.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	QSPI5_SLSO3	O4		Master slave select output
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT77	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G16	P15.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	ASCLIN19_ARXB_F			Receive input
	CAN43_RXDB			CAN receive input node 3
	QSPI7_MRSTE_F			Master SPI data input
	EGTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	P15.7	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	ASCLIN19_ATX_F	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_SLSO10_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT78	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P3_TXCLKC)
	LETH0_P3_RMIIA_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P3_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
H16	P15.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5A			ERU channel 5 input A
	GETH0_P0_COLB			Port0 MII Collision detect
	LETH0_P3_RXDG			LETH PortX TC14 interface receive data input
	EGTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	LETH0_P3_MII_RMII_RXD0A			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P3_RXCLKA or LETH0_P3_REFCLKA)
	LETH0_P3_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P3_RXCLKC or LETH0_P3_REFCLKC)
	P15.8	O0		General-purpose output
	—	O1		Reserved
	CAN43_TXD	O2		CAN transmit output node 3
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_SLSO11_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT79	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B14	P15.10	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI5_MRSTA			Master SPI data input
	I2C1_SDAC			Serial Data Input 2
	ASCLIN19_ARXD_F			Receive input
	EGTM_TIM2_IN1_8			Mux input channel 1 of TIM module 2
	P15.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	QSPI7_SLSO9_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT242	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P3_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
A14	P15.11	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI5_SLSIA			Slave select input
	I2C1_SCLC			Serial Clock Input 2
	LETH0_P0_EDF			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOF			LETH PortX MDIO interface data input
	EGTM_TIM2_IN2_8			Mux input channel 2 of TIM module 2
	P15.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT243	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P3_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B13	P15.12	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	LETH0_P3_MII_RXERA			LETH PortX MII receive error (to be used with LETH0_P3_RXCLKA)
	LETH0_P0_RXDF			LETH PortX TC14 interface receive data input
	CANXL00_RXDF			CANXL receive input node 0
	LETH0_P0_COLB			LETH PortX MII collision detection
	LETH0_P3_COLB			LETH PortX MII collision detection

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN3_6			Mux input channel 3 of TIM module 2
	P15.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN19_ATX_F	O2		Transmit output
	QSPI5_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT244	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A13	P15.13	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	LETH0_P3_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P3_RXCLKB)
	EGTM_TIM2_IN4_9			Mux input channel 4 of TIM module 2
	LETH0_P2_MII_RXDVA			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_RMII_CRSDVA			Receive data valid and Carrier sense and receive data valid
	P15.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_SLSO0	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT245	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	—	O14		Reserved
	—	O15		Reserved
B11	P15.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI5_MTSRA			Slave SPI data input
	LETH0_P3_MII_RXD2A			LETH PortX MII receive data bit 2 (to be used with LETH0_P3_RXCLKA)
	EGTM_TIM2_IN5_10			Mux input channel 5 of TIM module 2
	P15.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT246	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A11	P15.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI5_SCLKA			Slave SPI clock inputs
	LETH0_P3_MII_RXD3A			LETH PortX MII receive data bit 3 (to be used with LETH0_P3_RXCLKA)

(table continues...)

Table 18 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN6_9			Mux input channel 6 of TIM module 2
	P15.15	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI5_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT247	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 19 Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A24	P16.0	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RGMII_GREFCLK			Port0 RGMII Gigabit Reference Clock input
	GETH0_P0_TXCLKC			Port0 Transmit Clock Input for MII
	LETH0_P0_TXCLKC			PortX MII transmit clock
	GETH0_P0_RXD1D			Port0 MII and RMII receive data bit 1 (to be used with GETH0_P0_RXCLKD or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD1D			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKD or LETH0_P0_REFCLKD)
	EGTM_TIM0_IN1_11			Mux input channel 1 of TIM module 0
	EGTM_TIM0_IN5_10			Mux input channel 5 of TIM module 0
	P16.0	O0		General-purpose output

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI1_SLSO3	O4		Master slave select output
	CAN13_TXD	O5		CAN transmit output node 3
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT121	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_CLKA_INV	O		Clock out inverted
B23	P16.1	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	QSPI7_SCLKB_F			Slave SPI clock inputs
	CAN13_RXDF			CAN receive input node 3
	GETH0_P0_RGMII_RCTL			Port0 RGMII Receive Control
	SCU_E_REQ1G			ERU channel 1 input G
	GETH0_P0_CRSDVC			Port0 RMII Carrier Sense and Receive Data Valid (P0_CRSDVC must only be used with P0_REFCLKD)
	GETH0_P0_RXDVC			Port0 MII Receive Data Valid
	LETH0_P0_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P0_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid
	P16.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN0_ATX_F	O6		Transmit output

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT97	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_CLKA	O		Clock out
A23	P16.2	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RXCLKD			Port0 MII Receive Clock
	GETH0_P0_RGMII_RXCLK			Port0 RGMII Receive Clock
	GETH0_P0_REFCLKD			Port0 Reference Clock input for RMII
	LETH0_P0_REFCLKC			RMII Clock from PAD
	LETH0_P0_RXCLKC			LETH PortX MII receive clock
	LETH0_P0_REFCLKD			MII or RMII Clock from PAD
	LETH0_P0_RXCLKD			LETH PortX MII receive clock
	ASCLIN0_ARXG_F			Receive input
	EGTM_TIM1_IN6_8			Mux input channel 6 of TIM module 1
	EGTM_TIM1_IN7_7			Mux input channel 7 of TIM module 1
	XSPI0_RWDSA			Data strobe
	P16.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI7_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT96	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_DMA	O		Data mask
A22	P16.3	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RXD1B			Port0 MII and RMII receive data bit 1 (to be used with GETH0_P0_RXCLKB or GETH0_P0_REFCLKB)
	GETH0_P0_RGMII_RXD1			Port0 RGMII Receive data
	LETH0_P0_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKC or LETH0_P0_REFCLKC)
	LETH0_P0_TXCLKD			PortX MII transmit clock
	EGTM_TIM0_IN7_9			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN5_9			Mux input channel 5 of TIM module 1
	XSPI0_RXD1A			Receive data
	P16.3	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN5_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT95	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA1	O		Transmit data

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B22	P16.4	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RXD0B			Port0 MII and RMII receive data bit 0 (to be used with GETH0_P0_RXCLKB or GETH0_P0_REFCLKB)
	GETH0_P0_RGMII_RXD0			Port0 RGMII Receive data
	QSPI3_MRSTF			Master SPI data input
	LETH0_P0_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKC or LETH0_P0_REFCLKC)
	GETH0_P0_RXD0D			Port0 MII and RMII receive data bit 0 (to be used with GETH0_P0_RXCLKD or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD0D			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKD or LETH0_P0_REFCLKD)
	EGTM_TIM0_IN6_10			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN1_10			Mux input channel 1 of TIM module 1
	P16.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	QSPI7_SLSO8_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT120	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	QSPI3_SLSO14	O12		Master slave select output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_CSA1_N	O		Chip Select 1
D21	P16.5	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	ASCLIN5_ARXE			Receive input
	GETH0_P0_RXD2B			Port0 MII receive data bit 2 (to be used with GETH0_P0_RXCLKB)

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_RGMII_RXD2			Port0 RGMII Receive data
	GETH0_P0_RXD2D			Port0 MII receive data bit 2 (to be used with GETH0_P0_RXCLKD)
	LETH0_P0_MII_RXD2C			LETH PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD2D			LETH PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKD)
	EGTM_CDTM1_DTM0_1			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_1			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_1			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_1			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM1_IN0_11			Mux input channel 0 of TIM module 1
	EGTM_TIM1_IN4_10			Mux input channel 4 of TIM module 1
	XSPI0_RXD2A			Receive data
	P16.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	CAN20_TXD	O6		CAN transmit output node 0
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT119	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA2	O		Transmit data
D20	P16.6	I	HSFAST / PU1 /	General-purpose input
	CAN03_RXDG			CAN receive input node 3
	ASCLIN1_ARXH			Receive input

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_SLSIA_F		VDDHSIF / ES	Slave select input
	XSPI0_RXD3A			Receive data
	P16.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P0_MII_TXD0	O8		Port0 MII Transmit data (to be used with GETH0_P0_TXCLKC)
	EGTM_TOUT99	O9		eGTM muxed output
	GETH0_P0_RMIIC_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKC)
	LETH0_P0_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
	XSPI0_TXDA3	O		Transmit data
	GETH0_P0_RGMII_TXD0	O		Port0 RGMII Transmit data
E20	P16.7	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	QSPI7_MTSRB_F			Slave SPI data input
	GETH0_P0_RXD3B			Port0 MII receive data bit 3 (to be used with GETH0_P0_RXCLKB)
	GETH0_P0_RGMII_RXD3			Port0 RGMII Receive data
	GETH0_P0_RXD3D			Port0 MII receive data bit 3 (to be used with GETH0_P0_RXCLKD)
	LETH0_P0_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD3D			LETH PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKD)

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	XSPI0_RXD0A			Receive data
	P16.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT98	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA0	O		Transmit data
A20	P16.8	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN11_RXDE			CAN receive input node 1
	EGTM_TIM1_IN6_9			Mux input channel 6 of TIM module 1
	EGTM_TIM1_IN7_9			Mux input channel 7 of TIM module 1
	XSPI0_RXD4A			Receive data
	P16.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	QSPI7_MTSR_F	O6		Master SPI data output
	—	O7		Reserved
	GETH0_P0_MII_TXD1	O8		Port0 MII Transmit data
	EGTM_TOUT123	O9		eGTM muxed output

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_RMIIC_TXD1	O10		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKC)
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA4	O		Transmit data
	GETH0_P0_RGMII_TXD1	O		Port0 RGMII Transmit data
B20	P16.9	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN12_RXDE			CAN receive input node 2
	I2C0_SCLE			Serial Clock Input 4
	QSPI3_MRSTE			Master SPI data input
	EGTM_TIM1_IN7_8			Mux input channel 7 of TIM module 1
	XSPI0_RXD5A			Receive data
	P16.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	LETH0_P0_MIIC_TXD2	O5		LETH PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKC)
	QSPI7_SCLK_F	O6		Master SPI clock output
	LETH0_P0_MIID_TXD2	O7		LETH PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKD)
	GETH0_P0_MII_TXD2	O8		Port0 MII Transmit data
	EGTM_TOUT124	O9		eGTM muxed output
	GETH0_P0_RMIIC_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKC)

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MIID_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKC)
	I2C0_SCL	O14		Serial Clock Output
	—	O15		Reserved
	XSPI0_TXDA5	O		Transmit data
	GETH0_P0_RGMII_TXD2	O		Port0 RGMII Transmit data
D18	P16.10	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	QSPI1_SLSIB			Slave select input
	I2C0_SDAE			Serial Data Input 4
	GETH0_P0_CRSDVB			Port0 RMII Carrier Sense and Receive Data Valid (P0_CRSDVB must only be used with P0_REFCLKB)
	GETH0_P0_RXDVB			Port0 MII Receive Data Valid
	GETH0_P0_CRSC			Port0 MII Carrier Sense
	LETH0_P0_MII_RXDVD			Receive data valid and Carrier sense and receive data valid
	LETH0_P0_RMII_CRSDVD			Receive data valid and Carrier sense and receive data valid
	XSPI0_RXD6A			Receive data
	P16.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI7_SLSO5_F	O6		Master slave select output
	LETH0_P0_MIIC_TXD3	O7		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKC)
	GETH0_P0_MII_TXD3	O8		Port0 MII Transmit data
	EGTM_TOUT129	O9		eGTM muxed output
	LETH0_P0_MIID_TXD3	O10		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKD)
	—	O11		Reserved
	QSPI3_MRST	O12		Slave SPI data output
	—	O13		Reserved

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	I2C0_SDA	O14		Serial Data Output
	—	O15		Reserved
	XSPI0_TXDA6	O		Transmit data
	GETH0_P0_RGMII_TXD3	O		Port0 RGMII Transmit data
E18	P16.11	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN30_RXDC			CAN receive input node 0
	LETH0_P0_MDIOD			LETH PortX MDIO interface data input
	I2C1_SDAE			Serial Data Input 4
	LETH0_P0_EDD			LETH PortX TC14 interface energy detection input
	QSPI3_MRSTD			Master SPI data input
	P16.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN0_ASLSO	O6		Slave select signal output
	GETH0_P0_MDC	O7		Port0 MDIO Clock
	GETH0_P1_MDC	O8		Port1 MDIO Clock
	EGTM_TOUT128	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	QSPI3_MTSR	O12		Master SPI data output
	—	O13		Reserved
	I2C1_SDA	O14		Serial Data Output
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
A17	P16.12	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	I2C2_SDAD			Serial Data Input 3
	QSPI7_MRSTD_F			Master SPI data input
	QSPI3_SLSID			Slave select input

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MII_RXERD			LETH PortX MII receive error (to be used with LETH0_P0_RXCLKD)
	EGTM_TIM1_IN5_10			Mux input channel 5 of TIM module 1
	XSPI0_RXD7A			Receive data
	P16.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	ASCLIN0_ASLSO	O6		Slave select signal output
	LETH0_P0_MIIC_TXER	O7		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKC)
	GETH0_P0_TXER	O8		Port0 MII Transmit Error
	EGTM_TOUT122	O9		eGTM muxed output
	LETH0_P0_MIID_TXER	O10		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKD)
	GETH0_P0_RMIIC_TXEN	O11		GETH PortX RMII transmit enable (to be used with GETH0_P0_REFCLKD)
	QSPI3_SLSO13	O12		Master slave select output
	—	O13		Reserved
	I2C2_SDA	O14		Serial Data Output
	—	O15		Reserved
	XSPI0_TXDA7	O		Transmit data
	GETH0_P0_RGMII_TXCLK	O		Port0 RGMII Transmit Clock Output
B17	P16.13	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	I2C2_SCLD			Serial Clock Input 3
	CAN20_RXDG			CAN receive input node 0
	QSPI3_MTSRE			Slave SPI data input
	EGTM_TIM1_IN1_11			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN4_11			Mux input channel 4 of TIM module 1
	P16.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH0_P0_MII_TXEN	O6		Port0 MII Transmit Enable
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT100	O9		eGTM muxed output
	GETH0_P0_RMIIC_TXEN	O10		GETH PortX RMII transmit enable (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P0_REFCLKC)
	I2C2_SCL	O14		Serial Clock Output
	—	O15		Reserved
	XSPI0_CSA0_N	O		Chip Select 0
	GETH0_P0_RGMII_TCTL	O		Port0 RGMII Transmit Control
D17	P16.14	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	I2C1_SCLE			Serial Clock Input 4
	GETH0_PX_MDIOB			PortX MDIO input
	QSPI3_SCLKD			Slave SPI clock inputs
	P16.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	EGTM_ECLK2	O4		CGM generated clock
	CAN03_TXD	O5		CAN transmit output node 3
	CLOCK_EXTCLK1	O6		External clock output 1
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT101	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 19 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MDC	O11		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	QSPI3_SCLK	O12		Master SPI clock output
	—	O13		Reserved
	I2C1_SCL	O14		Serial Clock Output
	—	O15		Reserved
	GETH0_PX_MDIO1	O		PortX MDIO output

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Table 20 Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L23	P20.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN03_RXDC			CAN receive input node 3
	CAN21_RXDC			CAN receive input node 1
	CBS_TGI0			Trigger input
	SCU_E_REQ6A			ERU channel 6 input A
	GETH0_P1_RXERC			Port1 MII Receive Error
	SENT1_SENT1D			Receive input channel 1
	LETH0_P0_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	EGTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CLOCK_CLKA_SYSCLK			System clock input
	P20.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX_F	O2		Transmit output
	ASCLIN3_ASCLK_F	O3		Shift clock output
	SENT1_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_MII_TXD2	O8		Port0 MII Transmit data
	EGTM_TOUT59	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_MDC	O12		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSB1_N	O15		chip select
	CBS_TGO0	O		Trigger output
	HSCT0_SYSCLK_OUT	O		sys clock output
K22	P20.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CBS_TGI1			Trigger input
	CAN40_RXDB			CAN receive input node 0
	GETH0_P0_CRSD			Port0 MII Carrier Sense
	EGTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	LETH0_P0_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	P20.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT60	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MIIB_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO1	O		Trigger output
L22	P20.2	I	S / PU / VDDEXT	General-purpose input
	$\overline{\text{TESTMODE}}$			Testmode Enable Input
	PMS_TESTMODEIN			TESTMODE pin input
K23	P20.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXC_F			Receive input
	SENT0_SENT3D			Receive input channel 3
	EGTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	XSPI0_RXD0B			Receive data
	GETH0_P0_TXCLKD			Port0 Transmit Clock Input for MII
	LETH0_P0_TXCLKB			PortX MII transmit clock
	P20.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX_F	O2		Transmit output
	QSPI0_SLSO9_F	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	CAN21_TXD	O6		CAN transmit output node 1
	—	O7		Reserved
	SENT0_SPC3	O8		Transmit output
	EGTM_TOUT61	O9		eGTM muxed output
	LETH0_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	XSPI0_TXDB0	O		Transmit data
J20	P20.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	SENT1_SENT3D			Receive input channel 3
	CAN32_RXDB			CAN receive input node 2
	EGTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	XSPI0_RXD1B			Receive data
	P20.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8_F	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	GETH0_P0_TXER	O8		Port0 MII Transmit Error
	EGTM_TOUT62	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB1	O		Transmit data
J22	P20.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	SDMMC0_DAT0_IN			Read data in
	SENT1_SENT0D			Receive input channel 0

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	EGTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	P20.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	GETH0_P0_MII_TXD3	O8		Port0 MII Transmit data
	EGTM_TOUT63	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT0	O		Write data out
J23	P20.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SDMMC0_DAT1_IN			Read data in
	LETH0_P0_CRSD			LETH PortX MII carrier sense
	EGTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GETH0_P0_RXDVD			Port0 MII Receive Data Valid
	GETH0_P0_CRSDVD			Port0 RMII Carrier Sense and Receive Data Valid (P0_CRSDVD must only be used with P0_REFCLKD)
	LETH0_P0_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P0_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	P20.8	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0_F	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT64	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT1	O		Write data out
H20	P20.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7A			ERU channel 7 input A
	ADC_TRIG62			Triggers from PORTS to ADC
	LETH0_P0_COLD			LETH PortX MII collision detection
	EGTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	XSPI0_RXD2B			Receive data
	P20.9	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI0_SLSO1_F	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	GETH0_P0_RMIIB_TXD1	O7		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P0_REFCLKB)

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_MII_TXD1	O8		Port0 MII Transmit data
	EGTM_TOUT65	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O12		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB2	O		Transmit data
H22	P20.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SDMMC0_DAT2_IN			Read data in
	EGTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI0_SLSO6_F	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	ASCLIN1_ASCLK	O6		Shift clock output
	GETH0_P0_RMIIB_TXD0	O7		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P0_REFCLKB)
	GETH0_P0_MII_TXD0	O8		Port0 MII Transmit data
	EGTM_TOUT66	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O12		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH0_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT2	O		Write data out

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
H23	P20.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SCLKA			Slave SPI clock inputs
	SDMMC0_DAT3_IN			Read data in
	ASCLIN18_ARXD			Receive input
	EGTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	GETH0_P0_RXD1C			Port0 MII and RMII receive data bit 1 (to be used with GETH0_P0_RXCLKC or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	P20.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT67	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT3	O		Write data out
G22	P20.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MRSTA_F			Master SPI data input
	SDMMC0_DAT4_IN			Read data in
	EGTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	GETH0_P0_RXD0C			Port0 MII and RMII receive data bit 0 (to be used with GETH0_P0_RXCLKC or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD0B			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P20.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_MRST	O3		Slave SPI data output
	QSPI0_MTSR_F	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT68	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT4	O		Write data out
G23	P20.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SLSIA			Slave select input
	SDMMC0_DAT5_IN			Read data in
	ASCLIN9_ARXH			Receive input
	ASCLIN18_ARXE			Receive input
	GETH0_P0_RXD2C			Port0 MII receive data bit 2 (to be used with GETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD2B			LETH PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	P20.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SLSO2_F	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK_F	O5		Master SPI clock output

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT69	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CLKB	O15		clock output
	SDMMC0_DAT5	O		Write data out
F23	P20.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MTSRA			Slave SPI data input
	SDMMC0_DAT6_IN			Read data in
	ASCLIN27_ARXB_F			Receive input
	QSPI4_MRSTH			Master SPI data input
	GETH0_P0_RXD3C			Port0 MII receive data bit 3 (to be used with GETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD3B			LETH PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	P20.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_MTSR_F	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT70	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 20 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSB0_N	O15		chip select
	SDMMC0_DAT6	O		Write data out

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Table 21 Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
N20	P21.0	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI4_MRSTDN_F			Master SPI data input (LVDS N line)
	DMU_FDEST			FDEST for NVM
	ASCLIN11_ARXC_F			Receive input
	HSCT1_RXDN			Rx data
	QSPI0_SCLKEN			Slave SPI clock inputs (LVDS N line)
	QSPI4_MRSTE			Master SPI data input
	ASCLIN17_ARXB			Receive input
	ASCLIN18_ARXF			Receive input
	EGTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI0_SCLKD			Slave SPI clock inputs
	P21.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX_F	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT51	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	CSCU_CSRM1	O		Pin Output Value
M20	P21.1	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI4_MRSTDP_F			Master SPI data input (LVDS P line)
	ASCLIN11_ARXD_F			Receive input
	HSCT1_RXDP			Rx data
	QSPI0_SCLKEP			Slave SPI clock inputs (LVDS P line)
	ASCLIN18_ARXA_F			Receive input
	EGTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPI0_SCLKF			Slave SPI clock inputs
	P21.1	O0		General-purpose output
	—	O1		Reserved
	CAN40_TXD	O2		CAN transmit output node 0
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT52	O9		eGTM muxed output
	LETH0_P0_MIIB_TXER	O10		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O12		LETH PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CSCU_CSRM2	O		Pin Output Value
N22	P21.2	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SMU_EXT_EMERGENCYSTOP_REQ			Emergency Stop External Request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN_F			Master SPI data input (LVDS N line)
	ASCLIN11_ARXE_F			Receive input
	QSPI0_MTSRDN			Slave SPI data input (LVDS N line)
	SENT0_SENT2D			Receive input channel 2
	EGTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	QSPI0_MTSRE			Slave SPI data input
	QSPI4_MTSRC			Slave SPI data input
	ASCLIN18_ARXG			Receive input
	P21.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC2	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	GETH0_P1_MDC	O7		Port1 MDIO Clock
	GETH0_P0_MDC	O8		Port0 MDIO Clock
	EGTM_TOUT53	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
M22	P21.3	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP_F			Master SPI data input (LVDS P line)
	GETH0_PX_MDIOD			PortX MDIO input
	QSPI0_MTSRDP			Slave SPI data input (LVDS P line)
	SENT1_SENT2D			Receive input channel 2
	EGTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	QSPI0_MTSRF			Slave SPI data input
	P21.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ASCLK_F	O2		Shift clock output
	ASCLIN18_ATX_F	O3		Transmit output
	SENT1_SPC2	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT54	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	GETH0_PX_MDIO3	O		PortX MDIO output
N23	P21.4	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	SENT0_SENT0D			Receive input channel 0
	ASCLIN18_ARXB_F			Receive input
	EGTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GETH0_P0_REFCLKB			Port0 Reference Clock input for RMII
	GETH0_P0_RXCLKB			Port0 MII Receive Clock
	LETH0_P0_REFCLKB			RMII Clock from PAD
	LETH0_P0_RXCLKB			LETH PortX MII receive clock
	P21.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ASLSO_F	O2		Slave select signal output
	ASCLIN18_ATX_F	O3		Transmit output
	SENT0_SPC0	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTN	O8		Slave SPI inverted data output
	EGTM_TOUT55	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDN	O		Tx data
M23	P21.5	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	ASCLIN11_ARXF_F			Receive input
	SENT0_SENT1D			Receive input channel 1
	ASCLIN18_ARXC_F			Receive input
	EGTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	P21.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX_F	O3		Transmit output
	SENT0_SPC1	O4		Transmit output

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTP	O8		Slave SPI data output
	EGTM_TOUT56	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	GETH0_P0_MII_TXEN	O12		Port0 MII Transmit Enable
	GETH0_P0_RMIIB_TXEN	O13		GETH PortX RMII transmit enable (to be used with GETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDP	O		Tx data
L20	P21.6	I	FAST / PD3 / PU2 / VDDEXT / ES	General-purpose input
	CAN33_RXDB			CAN receive input node 3
	ASCLIN3_ARXF_F			Receive input
	CBS_TGI2			Trigger input
	TDI			PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	QSPI0_SLSIC			Slave select input
	GETH0_P0_COLC			Port0 MII Collision detect
	LETH0_P0_COLC			LETH PortX MII collision detection
	EGTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	P21.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT57	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO2	O		Trigger output
	DAP3	I/O		DAP:DAP3 Data I/O
	DAPE1	I/O		DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)
L19	P21.7	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	CBS_TGI3			Trigger input
	GETH0_P0_RXERB			Port0 MII Receive Error
	LETH0_P0_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P0_RXCLKC)
	EGTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	P21.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	ASCLIN3_ASCLK	O3		Shift clock output
	CAN33_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT58	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 21 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP:DAP2 Data I/O
	DAPE2	I/O		DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
	TDO	O		JTAG Module Data Output

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Table 22 Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U23	P22.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	QSPI5_MRSTC			Master SPI data input
	LETH0_P1_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	GETH0_P1_CRSDVB			Port1 RMII Carrier Sense and Receive Data Valid (P1_CRSDVB must only be used with P1_REFCLKB)
	GETH0_P1_RXDVB			Port1 MII Receive Data Valid
	GETH0_P1_CRSB			Port1 MII Carrier Sense
	LETH0_P1_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P1_CRSB			LETH PortX MII carrier sense
	EGTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	P22.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR_F	O3		Master SPI data output
	QSPI4_SCLKN_F	O4		Master SPI clock output (LVDS N line)
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT47	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U22	P22.1	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_MRSTB_F			Master SPI data input
	ASCLIN7_ARXE			Receive input
	GETH0_P0_RXERD			Port0 MII Receive Error
	GETH0_P1_RXERA			Port1 MII Receive Error
	LETH0_P1_MII_RXERA			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GETH0_P1_REFCLKB			Port1 RMII Reference Clock input
	GETH0_P1_RXCLKB			Port1 MII Receive Clock
	LETH0_P1_REFCLKB			RMII Clock from PAD
	LETH0_P1_RXCLKB			LETH PortX MII receive clock
	P22.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST	O3		Slave SPI data output
	QSPI4_SCLKP_F	O4		Master SPI clock output (LVDS P line)
	—	O5		Reserved
	QSPI5_SLSO9	O6		Master slave select output
	ASCLIN7_ATX	O7		Transmit output
	QSPI4_SLSO9	O8		Master slave select output
	EGTM_TOUT48	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
V23	P22.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_SLSIB			Slave select input
	CAN41_RXDA			CAN receive input node 1
	GETH0_P1_COLA			Port1 MII Collision detect
	LETH0_P1_COLA			LETH PortX MII collision detection
	LETH0_P1_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	P22.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3	O3		Master slave select output
	QSPI4_MTSRN_F	O4		Master SPI data output (LVDS N line)
	—	O5		Reserved
	QSPI5_MTSR	O6		Master SPI data output
	QSPI4_MTSR_F	O7		Master SPI data output
	GETH0_P1_MII_TXEN	O8		Port1 MII Transmit Enable
	EGTM_TOUT49	O9		eGTM muxed output
	GETH0_P1_RMIIA_TXEN	O10		GETH PortX RMII transmit enable (to be used with GETH0_P1_REFCLKA)
	GETH0_P1_RMIIB_TXEN	O11		GETH PortX RMII transmit enable (to be used with GETH0_P1_REFCLKB)
	LETH0_P1_MIIA_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXEN	O13		LETH PortX MII transmit enable (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXEN	O14		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXEN	O15		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB)

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	HSCT1_TXDN	O		Tx data
V22	P22.3	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_SCLKB			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	GETH0_P1_COLB			Port1 MII Collision detect
	GETH0_P1_RXD0B			Port1 MII and RMII receive data bit 0 (to be used with GETH0_P1_RXCLKB or GETH0_P1_REFCLKB)
	LETH0_P1_COLC			LETH PortX MII collision detection
	LETH0_P1_MII_RMII_RXD0B			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GETH0_P1_REFCLKC			Port1 RMII Reference Clock input
	GETH0_P1_RXCLKC			Port1 MII Receive Clock
	LETH0_P1_REFCLKC			RMII Clock from PAD
	LETH0_P1_RXCLKC			LETH PortX MII receive clock
	P22.3	O0		General-purpose output
	—	O1		Reserved
	QSPI5_SCLK	O2		Master SPI clock output
	QSPI4_SCLK_F	O3		Master SPI clock output
	QSPI4_MTSRP_F	O4		Master SPI data output (LVDS P line)
	—	O5		Reserved
	CAN41_TXD	O6		CAN transmit output node 1
	ASCLIN7_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT50	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT1_TXDP	O		Tx data

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U19	P22.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SCU_E_REQ5E			ERU channel 5 input E
	ASCLIN7_ARXF			Receive input
	LETH0_P1_RXDH			LETH PortX TC14 interface receive data input
	GETH0_P1_RXD0A			Port1 MII and RMII receive data bit 0 (to be used with GETH0_P1_RXCLKA or GETH0_P1_REFCLKA)
	GETH0_P1_RXD0C			Port1 MII and RMII receive data bit 0 (to be used with GETH0_P1_RXCLKC or GETH0_P1_REFCLKC)
	LETH0_P1_MII_RMII_RXD0A			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	LETH0_P1_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	P22.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO12	O4		Master slave select output
	—	O5		Reserved
	CAN13_TXD	O6		CAN transmit output node 3
	QSPI6_SLSO15_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT130	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
U20	P22.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MTSRC			Slave SPI data input
	CAN42_RXDA			CAN receive input node 2
	CAN13_RXDC			CAN receive input node 3

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P1_REFCLKA			Port1 RMII Reference Clock input
	GETH0_P1_RXCLKA			Port1 MII Receive Clock
	GETH0_P1_TXCLKB			Port1 Transmit Clock Input for MII
	LETH0_P1_REFCLKA			RMII Clock from PAD
	LETH0_P1_RXCLKA			LETH PortX MII receive clock
	P22.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT131	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T19	P22.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC_F			Receive input
	LETH0_P1_MII_RXDVA			Receive data valid and Carrier sense and receive data valid
	GETH0_P1_CRSDVA			Port1 RMII Carrier Sense and Receive Data Valid (P1_CRSDVA must only be used with P1_REFCLKA)
	GETH0_P1_RXDVA			Port1 MII Receive Data Valid
	GETH0_P1_CRSA			Port1 MII Carrier Sense
	LETH0_P1_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P1_RMII_CRSDVA			Receive data valid and Carrier sense and receive data valid
	LETH0_P1_CRSA			LETH PortX MII carrier sense
	LETH0_P1_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN6_11			Mux input channel 6 of TIM module 2
	P22.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT132	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T20	P22.7	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	GETH0_P1_TXCLKA			Port1 Transmit Clock Input for MII
	LETH0_P1_TXCLKA			PortX MII transmit clock
	LETH0_P1_TXCLKB			PortX MII transmit clock
	LETH0_P1_TXCLKC			PortX MII transmit clock
	P22.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK_F	O2		Shift clock output
	ASCLIN17_ATX_F	O3		Transmit output
	QSPI0_SCLK	O4		Master SPI clock output
	ASCLIN27_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT133	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R19	P22.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SCLKB			Slave SPI clock inputs
	LETH0_P1_RXDE			LETH PortX TC14 interface receive data input
	P22.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT134	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
R20	P22.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD_F			Receive input
	CAN22_RXDE			CAN receive input node 2
	LETH0_P1_EDE			LETH PortX TC14 interface energy detection input

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIOE			LETH PortX MDIO interface data input
	P22.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	GETH0_P1_MII_TXD1	O7		Port1 MII Transmit data (to be used with GETH0_P1_TXCLKB)
	—	O8		Reserved
	EGTM_TOUT135	O9		eGTM muxed output
	GETH0_P1_RMIIC_TXD1	O10		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P1_REFCLKC)
	LETH0_P1_MIIC_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD1	O12		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
P19	P22.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MTSRB			Slave SPI data input
	P22.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	CAN23_TXD	O5		CAN transmit output node 3
	—	O6		Reserved
	GETH0_P1_MII_TXD0	O7		Port1 MII Transmit data
	—	O8		Reserved
	EGTM_TOUT136	O9		eGTM muxed output

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P1_RMIIC_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P1_REFCLKC)
	LETH0_P1_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD0	O12		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output
P20	P22.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDE			CAN receive input node 3
	ASCLIN17_ARXA_F			Receive input
	GETH0_P1_RXD3A			Port1 MII receive data bit 3 (to be used with GETH0_P1_RXCLKA)
	LETH0_P1_MII_RXD3A			LETH PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKA)
	GETH0_P1_RXD3B			Port1 MII receive data bit 3 (to be used with GETH0_P1_RXCLKB)
	LETH0_P1_MII_RXD3B			LETH PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKB)
	P22.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	ASCLIN17_ATX_F	O3		Transmit output
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	CAN42_TXD	O6		CAN transmit output node 2
	GETH0_P1_MII_TXEN	O7		Port1 MII Transmit Enable
	—	O8		Reserved
	EGTM_TOUT137	O9		eGTM muxed output
	GETH0_P1_RMIIC_TXEN	O10		GETH PortX RMII transmit enable (to be used with GETH0_P1_REFCLKC)
	LETH0_P1_MIIC_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXEN	O12		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC)

(table continues...)

Table 22 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.14 BGA436_COM port 23

Table 23 Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AA23	P23.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN10_RXDC			CAN receive input node 0
	ASCLIN17_ARXC			Receive input
	QSPI6_SLSID_F			Slave select input
	EGTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	P23.0	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_SCLK	O7		Master SPI clock output
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT41	O9		eGTM muxed output
	GETH0_P1_TXER	O10		Port1 MII Transmit Error
	LETH0_P1_MIIA_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXER	O13		LETH PortX MII transmit error (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 23 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y22	P23.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN6_ARXF_F			Receive input
	SCU_E_REQ6F			ERU channel 6 input F
	$\overline{\text{PCIE0\_PERSTA\_N}}$			PERST# input
	ADC_TRIG61			Triggers from PORTS to ADC
	QSPI0_MRSTD			Master SPI data input
	LETH0_P1_RXDG			LETH PortX TC14 interface receive data input
	GETH0_P1_RXD1B			Port1 MII and RMII receive data bit 1 (to be used with GETH0_P1_RXCLKB or GETH0_P1_REFCLKB)
	LETH0_P1_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	P23.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6	O3		Master slave select output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	CLOCK_EXTCLK0	O6		External clock output 0
	ASCLIN6_ASCLK_F	O7		Shift clock output
	QSPI6_MTSR_F	O8		Master SPI data output
	EGTM_TOUT42	O9		eGTM muxed output
	EGTM_ECLK0	O10		CGM generated clock
	ASCLIN16_ATX_F	O11		Transmit output
	QSPI6_SCLK_F	O12		Master SPI clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
Y23	P23.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN7_ARXC			Receive input
	QSPI6_MRSTE_F			Master SPI data input

(table continues...)

Table 23 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	P23.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	QSPI6_SCLK_F	O7		Master SPI clock output
	QSPI6_SLSO3_F	O8		Master slave select output
	EGTM_TOUT43	O9		eGTM muxed output
	GETH0_P1_MII_TXD3	O10		Port1 MII Transmit data
	LETH0_P1_MIIA_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD3	O13		LETH PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
W22	P23.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN6_ARXA_F			Receive input
	CAN12_RXDC			CAN receive input node 2
	CAN23_RXDB			CAN receive input node 3
	QSPI6_MTSRB_F			Slave SPI data input
	EGTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	P23.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2

(table continues...)

Table 23 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	QSPI6_SLSO0	O7		Master slave select output
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT44	O9		eGTM muxed output
	GETH0_P1_MII_TXD2	O10		Port1 MII Transmit data
	LETH0_P1_MIIA_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD2	O13		LETH PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
W23	P23.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN27_ARXA_F			Receive input
	PCIE0_WAKE_INA_N			WAKE# input
	QSPI6_MRSTD_F			Master SPI data input
	EGTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	P23.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASLSO_F	O2		Slave select signal output
	QSPI4_SLSO5_F	O3		Master slave select output
	GETH0_P1_MII_TXD1	O4		Port1 MII Transmit data
	—	O5		Reserved
	ASCLIN27_ATX_F	O6		Transmit output
	GETH0_P1_RMIIA_TXD1	O7		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P1_REFCLKA)
	QSPI6_SLSO1_F	O8		Master slave select output
	EGTM_TOUT45	O9		eGTM muxed output
	GETH0_P1_RMIIB_TXD1	O10		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P1_REFCLKB)
	LETH0_P1_MIIA_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKA)

(table continues...)

Table 23 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MIIB_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXD1	O14		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB)
	QSPI6_MTSR_F	O15		Master SPI data output
	$\overline{\text{PCIE0\_WAKE\_N}}$	O		WAKE# output
W20	P23.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN16_ARXA_F			Receive input
	$\overline{\text{PCIE0\_CLKREQ\_INA\_N}}$			CLKREQ# input
	GETH0_P1_RXD3C			Port1 MII receive data bit 3 (to be used with GETH0_P1_RXCLKC)
	LETH0_P1_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	P23.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX_F	O2		Transmit output
	QSPI4_SLSO4_F	O3		Master slave select output
	GETH0_P1_MII_TXD0	O4		Port1 MII Transmit data
	—	O5		Reserved
	CAN22_TXD	O6		CAN transmit output node 2
	GETH0_P1_RMIIA_TXD0	O7		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P1_REFCLKA)
	QSPI6_SLSO2_F	O8		Master slave select output
	EGTM_TOUT46	O9		eGTM muxed output
	GETH0_P1_RMIIB_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P1_REFCLKB)
	LETH0_P1_MIIA_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKA)

(table continues...)

Table 23 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIB_TXD0	O14		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output
	$\overline{\text{PCIE0\_CLKREQ\_N}}$	O		CLKREQ# output
V20	P23.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN22_RXDC			CAN receive input node 2
	QSPI6_MRSTA_F			Master SPI data input
	GETH0_P1_RXD2A			Port1 MII receive data bit 2 (to be used with GETH0_P1_RXCLKA)
	LETH0_P1_MII_RXD2A			LETH PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKA)
	GETH0_P1_RXD2B			Port1 MII receive data bit 2 (to be used with GETH0_P1_RXCLKB)
	LETH0_P1_MII_RXD2B			LETH PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKB)
	GETH0_P1_RXD2C			Port1 MII receive data bit 2 (to be used with GETH0_P1_RXCLKC)
	LETH0_P1_MII_RXD2C			LETH PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	P23.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	QSPI6_SLSO14_F	O7		Master slave select output
	QSPI6_MRST_F	O8		Slave SPI data output
	EGTM_TOUT138	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 23 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI6_MTSR_F	O15		Master SPI data output
V19	P23.7	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN11_RXDC			CAN receive input node 1
	ASCLIN16_ARXB_F			Receive input
	QSPI6_SCLKA_F			Slave SPI clock inputs
	GETH0_P1_RXD1A			Port1 MII and RMII receive data bit 1 (to be used with GETH0_P1_RXCLKA or GETH0_P1_REFCLKA)
	GETH0_P1_RXD1C			Port1 MII and RMII receive data bit 1 (to be used with GETH0_P1_RXCLKC or GETH0_P1_REFCLKC)
	LETH0_P1_MII_RMII_RXD1A			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	LETH0_P1_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	EGTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1
	P23.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX_F	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT139	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.15 BGA436_COM port 25

Table 24 Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
R23	P25.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SCU_E_REQ4G			ERU channel 4 input G
	QSPI6_MRSTB			Master SPI data input
	P25.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	CAN42_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT207	O9		eGTM muxed output
	—	O10		Reserved
	GETH0_P1_TXER	O11		Port1 MII Transmit Error
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.16 BGA436_COM port 30

Table 25 Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE14	P30.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN10_RXDE			CAN receive input node 0
	ASCLIN17_ARXE			Receive input
	GETH0_P1_RXCLKD			Port1 MII Receive Clock
	GETH0_P1_REFCLKD			Port1 RMII Reference Clock input
	LETH0_P1_REFCLKD			LETH PortX RMII reference clock
	LETH0_P1_RXCLKD			LETH PortX MII receive clock
	P30.0	O0		General-purpose output

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT190	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF16	P30.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GETH0_P1_CRSDVD			Port1 RMII Carrier Sense and Receive Data Valid (P1_CRSDVD must only be used with P1_REFCLKD)
	GETH0_P1_RXDVD			Port1 MII Receive Data Valid
	LETH0_P1_MII_RXDVD			Receive data valid and Carrier sense and receive data valid
	LETH0_P1_RMII_CRSDVD			Receive data valid and Carrier sense and receive data valid
	P30.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI4_SLSO12	O3		Master slave select output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT191	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE16	P30.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN8_ARXH			Receive input
	QSPI6_MRSTH			Master SPI data input
	GETH0_P1_RXD3D			Port1 MII receive data bit 3 (to be used with GETH0_P1_RXCLKD)
	LETH0_P1_MII_RXD3D			LETH PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKD)
	P30.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	CAN21_TXD	O4		CAN transmit output node 1
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT192	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF17	P30.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN6_ARXG			Receive input
	CAN12_RXDF			CAN receive input node 2
	CAN21_RXDH			CAN receive input node 1
	GETH0_P1_RXD2D			Port1 MII receive data bit 2 (to be used with GETH0_P1_RXCLKD)

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MII_RXD2D			LETH PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKD)
	P30.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN8_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT193	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE17	P30.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN27_ARXC			Receive input
	GETH0_P1_RXD1D			Port1 MII and RMII receive data bit 1 (to be used with GETH0_P1_RXCLKD or GETH0_P1_REFCLKD)
	LETH0_P1_MII_RMII_RXD1D			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKD or LETH0_P1_REFCLKD)
	P30.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI4_SLSO13	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN27_ATX	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT194	O9		eGTM muxed output

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF19	P30.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN16_ARXC			Receive input
	LETH0_P1_RXDF			LETH PortX TC14 interface receive data input
	GETH0_P1_RXD0D			Port1 MII and RMII receive data bit 0 (to be used with GETH0_P1_RXCLKD or GETH0_P1_REFCLKD)
	LETH0_P1_MII_RMII_RXD0D			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKD or LETH0_P1_REFCLKD)
	P30.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	QSPI4_SLSO14	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT195	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
AE19	P30.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN22_RXDH			CAN receive input node 2
	QSPI6_MRSTG			Master SPI data input

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P30.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI0_SLSO14	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	QSPI6_MRST	O7		Slave SPI data output
	GETH0_P1_MII_TXD2	O8		Port1 MII Transmit data
	EGTM_TOUT196	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIID_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKD)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF20	P30.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN11_RXDF			CAN receive input node 1
	ASCLIN16_ARXD			Receive input
	QSPI6_SCLKD			Slave SPI clock inputs
	P30.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_SCLK	O7		Master SPI clock output
	GETH0_P1_MII_TXD3	O8		Port1 MII Transmit data
	EGTM_TOUT197	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MIID_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKD)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE20	P30.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P30.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT198	O9		eGTM muxed output
	GETH0_P1_TXER	O10		Port1 MII Transmit Error
	LETH0_P1_MIID_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P1_TXCLKD)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF22	P30.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P30.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P1_MII_TXD0	O8		Port1 MII Transmit data
	EGTM_TOUT199	O9		eGTM muxed output
	GETH0_P1_RMIID_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P1_REFCLKD)
	LETH0_P1_MIID_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKD)
	LETH0_P1_RMIID_TXD0	O12		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKD)
	LETH0_P1_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRD_TXD0	O		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKD - registered*)
AE22	P30.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P30.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P1_MII_TXD1	O8		Port1 MII Transmit data
	EGTM_TOUT200	O9		eGTM muxed output
	GETH0_P1_RMIID_TXD1	O10		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P1_REFCLKD)
	LETH0_P1_MIID_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKD)
	LETH0_P1_RMIID_TXD1	O12		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRD_TXD1	O		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKD - registered*)

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AF23	P30.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P30.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_MRST	O7		Slave SPI data output
	GETH0_P1_MII_TXEN	O8		Port1 MII Transmit Enable
	EGTM_TOUT201	O9		eGTM muxed output
	GETH0_P1_RMIID_TXEN	O10		GETH PortX RMII transmit enable (to be used with GETH0_P1_REFCLKD)
	LETH0_P1_MIID_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P1_TXCLKD)
	LETH0_P1_RMIID_TXEN	O12		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRD_TXEN	O		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKD - registered*)
AE23	P30.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P1_MDIOF			LETH PortX MDIO interface data input
	LETH0_P1_EDF			LETH PortX TC14 interface energy detection input
	LETH0_P1_CRSD			LETH PortX MII carrier sense
	P30.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT202	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
AF24	P30.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	$\overline{\text{PCIE1\_PERSTA\_N}}$			PERST# input
	P30.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT203	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE24	P30.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	$\overline{\text{PCIE1\_WAKE\_INA\_N}}$			WAKE# input
	P30.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved

(table continues...)

Table 25 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT204	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	$\overline{\text{PCIE1\_WAKE\_N}}$	O		WAKE# output
AF25	P30.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	$\overline{\text{PCIE1\_CLKREQ\_INA\_N}}$			CLKREQ# input
	P30.15	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT205	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	$\overline{\text{PCIE1\_CLKREQ\_N}}$	O		CLKREQ# output

3.2.17 BGA436_COM port 31

Table 26 Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE13	P31.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT13D			Receive input channel 13
	GETH0_P1_RXERD			Port1 MII Receive Error
	LETH0_P1_MII_RXERD			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKD)
	EGTM_TIM2_IN6_10			Mux input channel 6 of TIM module 2
	P31.6	O0		General-purpose output
	—	O1		Reserved
	SENT1_SPC13	O2		Transmit output
	ASCLIN17_ATX	O3		Transmit output
	—	O4		Reserved
	CAN32_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT180	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF14	P31.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT14C			Receive input channel 14
	ASCLIN17_ARXD			Receive input
	CAN32_RXDE			CAN receive input node 2
	EGTM_TIM2_IN7_11			Mux input channel 7 of TIM module 2
	GETH0_P1_TXCLKD			Port1 Transmit Clock Input for MII
	LETH0_P1_TXCLKD			PortX MII transmit clock
	P31.7	O0		General-purpose output
	—	O1		Reserved
	SENT0_SPC14	O2		Transmit output

(table continues...)

Table 26 (continued) Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT181	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

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Table 27 Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AB21	P32.2	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input
	CAN21_RXDD			CAN receive input node 1
	SMU_FSPIN2			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	UART_RXDH	I#		Receive input H
	WCAN_RXDF			Wake-up input F
	T0D			T0 capture input D
	T21EXG			T21 interrupt input G
	EXINT7			Interrupt 7 input
	P32.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT38	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP2	O		FSP Output Signal - Generated by SMU
AB20	P32.4	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	ASCLIN1_ACTSB			Clear to send input
	ASCLIN15_ARXA_F			Receive input

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	I2C0_SCLD			Serial Clock Input 3
	EGTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	SSC_MRSTD	I#		Master SPI data input D
	T21EXA			T21 interrupt input A
	T2CCU1_0A			T2 capture 1 input 0A
	EXINT8A			Interrupt 8 input A
	EXINT12A			Interrupt 12 input A
	I2CSCLA			Serial clock input A
	P32.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	CAN03_TXD	O3		CAN transmit output node 3
	—	O4		Reserved
	—	O5		Reserved
	CLOCK_EXTCLK1	O6		External clock output 1
	CAN21_TXD	O7		CAN transmit output node 1
	I2C0_SCL	O8		Serial Clock Output
	EGTM_TOUT40	O9		eGTM muxed output
	EGTM_ECLK1	O10		CGM generated clock
	—	O11		Reserved
	ASCLIN25_ATX_F	O12		Transmit output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.1	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_0	O#6		T2 PWM channel 10
	I2CSCL	O#7		Serial clock output

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DCDCSYNCO	O		DC-DC synchronization output
W18	P32.5	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	SENT0_SENT5C			Receive input channel 5
	ASCLIN17_ARXF			Receive input
	SMU_FSPIN3			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	SSC_MTSRD	I#		Slave SPI data input D
	PINRSTC			Reset input C
	T20EXO			T20 interrupt input O
	T2CCU1_1A			T2 capture 1 input 1A
	EXINT9A			Interrupt 9 input A
	EXINT13A			Interrupt 13 input A
	P32.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	SENT0_SPC5	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT140	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP3	O		FSP Output Signal - Generated by SMU
Y18	P32.6	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT1_SENT5C			Receive input channel 5
	I2C0_SDAD			Serial Data Input 3
	UART_RXDI	I#		Receive input I
	T1D			T1 capture input D
	T21A			T21 capture input A
	T2CCU1_2A			T2 capture 1 input 2A
	EXINT10A			Interrupt 10 input A

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT14A			Interrupt 14 input A
	I2CSDAA			Serial data input A
	P32.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	SENT1_SPC5	O3		Transmit output
	ASCLIN17_ATX	O4		Transmit output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	I2C0_SDA	O8		Serial Data Output
	EGTM_TOUT141	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_PPS	O12		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO4	O		Trigger output
Y19	P32.7	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CBS_TGI5			Trigger input
	CAN22_RXDB			CAN receive input node 2
	SENT0_SENT6C			Receive input channel 6
	ASCLIN15_ARXB_F			Receive input
	GETH0_P1_COLC			Port1 MII Collision detect
	GETH0_P1_RXERB			Port1 MII Receive Error
	LETH0_P1_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKB)
	WCAN_RXDH	I#		Wake-up input H
	T20EXH			T20 interrupt input H
	T2CCU1_3A			T2 capture 1 input 3A
	EXINT11A			Interrupt 11 input A
	EXINT15A			Interrupt 15 input A
	P32.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	SENT0_SPC6	O3		Transmit output
	ASCLIN15_ATX_F	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT142	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 27 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P2.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_3	O#6		T2 PWM channel 13
	PMSRTC32_OUT	O#7		RTC oscillator output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO5	O		Trigger output

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Table 28 Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AB13	P33.0	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT9B			Receive input channel 9
	EGTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_3			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_3			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	T21EXB	I#		T20 interrupt input B
	T2CCU0_0A			T2 capture 0 input 0A
	EXINT3A			Interrupt 3 input A

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT12B			Interrupt 12 input B
	ADCOMPCH0			Analog input channel 0
	P33.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX_F	O2		Transmit output
	SENT1_SPC9	O3		Transmit output
	ASCLIN15_ATX_F	O4		Transmit output
	ADC_EMUXCTRL03	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT22	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
AC13	P33.1	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5_RX0C			RXD inputs (receive data) channel 0
	SENT0_SENT9B			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	EGTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	UART_RXDK	I#		Receive input K
	SSC_SCLKD			Slave SPI clock input D
	T0A			T0 capture input A
	T20EXA			T2 interrupt input A
	T2CCU0_1A			T2 capture 0 input 1A
	EXINT4A			Interrupt 4 input A
	EXINT13B			Interrupt 13 input B
	ADCOMPCH1			Analog input channel 1
	P33.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	SENT0_SPC9	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT23	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.1	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AB14	P33.2	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT8B			Receive input channel 8
	ASCLIN14_ARXC_F			Receive input
	EGTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	WCAN_RXDE	I#		Wake-up input E
	DAP0_1			DAP0 input
	T21B			T21 capture input B
	T2CCU0_2A			T2 capture 0 input 2A
	EXINT5A			Interrupt 5 input A
	EXINT14B			Interrupt 14 input B
	ADCOMPCH2			Analog input channel 2
	P33.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN14_ATX_F	O7		Transmit output
	SENT1_SPC8	O8		Transmit output
	EGTM_TOUT24	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AC14	P33.3	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT0_SENT8B			Receive input channel 8
	ASCLIN14_ARXA_F			Receive input
	EGTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	UART_RXDP	I#		Receive input P
	T20A			T20 capture input A

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU0_3A			T2 capture 0 input 3A
	EXINT6A			Interrupt 6 input A
	EXINT15B			Interrupt 15 input B
	ADCOMPCH3			Analog input channel 3
	P33.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK_F	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN14_ATX_F	O7		Transmit output
	SENT0_SPC8	O8		Transmit output
	EGTM_TOUT25	O9		eGTM muxed output
	ASCLIN8_ATX	O10		Transmit output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	DAP1_1	I/O		DAP1 input
	SPD_1	I/O		Single pin DAP1
AB15	P33.4	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT7B			Receive input channel 7
	ASCLIN5_ARXB_F			Receive input
	ASCLIN14_ARXB_F			Receive input
	ASCLIN25_ARXA_F			Receive input
	EGTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_1			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_1			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	UART_RXDC	I#		Receive input C
	WCAN_RXDP			Wake-up input P
	T1B			T1 capture input B
	T2CCU0_3D			T2 capture 0 input 3D
	EXINT0A			Interrupt 0 input A
	EXINT6D			Interrupt 6 input D
	EXINT12C			Interrupt 12 input C
	ADCOMPCH4			Analog input channel 4
	P33.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	CAN13_TXD	O7		CAN transmit output node 3
	SENT1_SPC7	O8		Transmit output

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT26	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN25_ATX_F	O12		Transmit output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.4	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AC15	P33.5	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5S0_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	SENT1_SENT2C			Receive input channel 2
	CAN13_RXDB			CAN receive input node 3
	QSPI4_MRSTG			Master SPI data input
	EGTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	WCAN_RXDD	I#		Wake-up input D
	SSC_MRSTA			Master SPI data input A

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T0B			T0 capture input B
	T20EXB			T20 interrupt input B
	EXINT1A			Interrupt 1 input A
	EXINT13C			Interrupt 13 input C
	ADCOMPCH5			Analog input channel 5
	P33.5	O0		General-purpose output
	—	O1		Reserved
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN5_ASLSO_F	O7		Slave select signal output
	—	O8		Reserved
	EGTM_TOUT27	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.5	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AB16	P33.6	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT0_SENT12B			Receive input channel 12
	ASCLIN8_ARXD			Receive input
	EGTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_2			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_2			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	UART_RXDL	I#		Receive input L
	SSC_MTSRA			Slave SPI data input A
	DAP0_0			DAP0 input
	T2CCU1_0B			T2 capture 1 input 0B
	EXINT2A			Interrupt 2 input A
	EXINT8B			Interrupt 8 input B
	ADCOMPCH6			Analog input channel 6
	P33.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	PSI5S0_TX	O7		TX data output
	SENT0_SPC12	O8		Transmit output
	EGTM_TOUT28	O9		eGTM muxed output
	QSPI4_MTSR	O10		Master SPI data output
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.6	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	SSC_MTSR	O#2		Master SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AC16	P33.7	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	CAN00_RXDE			CAN receive input node 0
	PSI5S0_RXD			RX data input
	SCU_E_REQ4A			ERU channel 4 input A
	SENT1_SENT11B			Receive input channel 11
	ADC_TRIG60			Triggers from PORTS to ADC
	EGTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	WCAN_RXDB	I#		Wake-up input B
	SSC_SCLKA			Slave SPI clock input A
	T20B			T20 capture input B
	T21EXH			T21 interrupt input H
	T2CCU1_1B			T2 capture 1 input 1B
	EXINT0B			Interrupt 0 input B

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT9B			Interrupt 9 input B
	ADCOMPCH7			Analog input channel 7
	P33.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	ADC_EMUXCTRL13	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	QSPI5_SLSO10	O7		Master slave select output
	SENT1_SPC11	O8		Transmit output
	EGTM_TOUT29	O9		eGTM muxed output
	QSPI4_SCLK	O10		Master SPI clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.7	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
	DAP1_0	I/O		DAP1 input
	SPD_0	I/O		Single pin DAP0
AB17	P33.8	I	FAST / HighZ / VDDEVRSB	General-purpose input
	ASCLIN2_ARXE			Receive input
	SMU_FSPIN0			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	UART_RXDF	I#		Receive input F
	WCAN_RXDO			Wake-up input O
	T21EXN			T21 interrupt input N
	T2CCU1_3D			T2 capture 1 input 3D
	EXINT1B			Interrupt 1 input B
	EXINT11D			Interrupt 11 input D
	I2CSDAD			Serial clock input D
	P33.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	QSPI5_SLSO11_F	O7		Master slave select output
	QSPI6_SLSO13	O8		Master slave select output
	EGTM_TOUT30	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.0	O#0		General-purpose output
	—	O#1		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP0	O		FSP Output Signal - Generated by SMU
AC17	P33.9	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	XTAL3			XTAL3.RTC Oscillator
	EGTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	T1A	I#		T1 capture input A
	T20EXC			T2 interrupt input C
	T2CCU0_0B			T2 capture 0 input 0B
	EXINT3B			Interrupt 3 input B
	EXINT14C			Interrupt 14 input C
	I2CSCLD			Serial clock input D
	P33.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO1	O3		Master slave select output
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ATX	O6		Transmit output
	QSPI5_SLSO12	O7		Master slave select output

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI6_SLSO10	O8		Master slave select output
	EGTM_TOUT31	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.1	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	—	O#6		Reserved
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AB18	P33.10	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	EGTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	UART_RXDA	I#		Receive input A
	WCAN_RXDA			Wake-up input A
	RTC32_IN			RTC oscillator input

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T20EXP			T20 interrupt input P
	T21CLK32K			T21 external input
	EXINT2B			Interrupt 2 input B
	EXINT15C			Interrupt 15 input C
	P33.10	O0		General-purpose output
	—	O1		Reserved
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S0_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	QSPI5_SLSO13	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT32	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.2	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	XTAL4	O		XTAL4. RTC Oscillator
AC18	P33.11	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_SCLKA			Slave SPI clock inputs
	SMM_ESR2_PORT_IN			ESR2 pad data from bitslice
	QSPI5_SCLKF			Slave SPI clock inputs
	EGTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	PMS_ESR2WKP			ESR2 pin input
	SSC_SCLKB	I#		Slave SPI clock input B
	PINRSTA			Reset input A
	T20C			T20 capture input C
	T2CCU0_1B			T2 capture 0 input 1B
	T2CCU1_2B			T2 capture 1 input 2B
	EXINT4B			Interrupt 4 input B
	EXINT10B			Interrupt 10 input B
	P33.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT33	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	PMS_RTCOUT	O12		RTC output for P33.11
	—	O13		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.3	O#0		General-purpose output
	—	O#1		Reserved
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_2	O#6		T2 PWM channel 12
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_ESR2PORST	O		ESR2 reset output. For details please refer to the PMS/SMM chapter.
AB19	P33.12	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	SMU_FSPIN1			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	PMS_PINCWKP			PINC (P33.12) pin input
	UART_RXDG	I#		Receive input G
	WCAN_RXDG			Wake-up input G
	SSC_MTSRB			Slave SPI data input B
	T1C			T1 capture input C
	T21C			T21 capture input C
	T2CCU0_2B			T2 capture 0 input 2B
	T2CCU1_3B			T2 capture 1 input 3B

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT5B			Interrupt 5 input B
	EXINT11B			Interrupt 11 input B
	P33.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	QSPI5_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT34	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_3	O#6		T2 PWM channel 13
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
	SMU_FSP1	O		FSP Output Signal - Generated by SMU
AC19	P33.13	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	ASCLIN1_ARXF			Receive input
	QSPI4_MRSTA			Master SPI data input
	CAN22_RXDA			CAN receive input node 2
	QSPI5_MRSTD_F			Master SPI data input
	ASCLIN16_ARXF			Receive input
	EGTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	PMS_PINBWKP			PINB (P33.13) pin input
	UART_RXDB	I#		Receive input B
	WCAN_RXDC			Wake-up input C
	SSC_MRSTB			Master SPI data input B
	T0C			T0 capture input C
	T20EXD			T20 interrupt input D
	T2CCU0_3B			T2 capture 0 input 3B
	EXINT0C			Interrupt 0 input C
	EXINT6B			Interrupt 6 input B
	ADCOMPCH8			Analog input channel 8
	P33.13	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MRST	O3		Slave SPI data output
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT35	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.5	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W17	P33.14	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI2_SCLKD			Slave SPI clock inputs
	CBS_TGI6			Trigger input
	CAN31_RXDB			CAN receive input node 1
	QSPI5_MRSTF			Master SPI data input
	EGTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	SSC_SCLKC	I#		Slave SPI clock input C
	EXTNMI			NMI input
	T21EXC			T21 interrupt input C
	EXINT1C			Interrupt 1 input C
	ADCOMPCH9			Analog input channel 9
	P33.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_MRST	O7		Slave SPI data output
	—	O8		Reserved
	EGTM_TOUT143	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.6	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO6	O		Trigger output
Y17	P33.15	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	CBS_TGI7			Trigger input
	QSPI5_SLSIB			Slave select input
	ASCLIN15_ARXC			Receive input

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SENT14D			Receive input channel 14
	QSPI4_MTSRD			Slave SPI data input
	EGTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	UART_RXDE	I#		Receive input E
	PINRSTB			Reset input B
	T20EXE			T20 interrupt input E
	T2CCU0_0C			T2 capture 0 input 0C
	T2CCU1_0C			T2 capture 1 input 0C
	EXINT2C			Interrupt 2 input C
	EXINT3C			Interrupt 3 input C
	EXINT8C			Interrupt 8 input C
	ADCOMPCH10			Analog input channel 10
	P33.15	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	SENT1_SPC14	O8		Transmit output
	EGTM_TOUT144	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.7	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved

(table continues...)

Table 28 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO7	O		Trigger output

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Table 29 Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y14	P34.1	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT0_SENT12D			Receive input channel 12
	$\overline{\text{PCIE0\_PERSTB\_N}}$			PERST# input
	ASCLIN25_ARXB_F			Receive input
	EGTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	UART_RXDD	I#		Receive input D
	T21EXD			T21 interrupt input D
	T2CCU0_1C			T2 capture 0 input 1C
	T2CCU1_1C			T2 capture 1 input 1C
	EXINT4C			Interrupt 4 input C
	EXINT9C			Interrupt 9 input C
	ADCOMPCH11			Analog input channel 11
	P34.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	SENT0_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT146	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.0	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG0	O		PMS debugging power mode K
W15	P34.2	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	CAN20_RXDC			CAN receive input node 0

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SENT14B			Receive input channel 14
	I2C1_SDAD			Serial Data Input 3
	EGTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	WCAN_RXDI	I#		Wake-up input I
	T20EXF			T20 interrupt input F
	T2CCU0_2C			T2 capture 0 input 2C
	EXINT5C			Interrupt 5 input C
	ADCOMPCH12			Analog input channel 12
	I2CSDAB			Serial data input B
	P34.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT147	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.1	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG1	O		PMS debugging power mode K
Y15	P34.3	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN43_RXDA			CAN receive input node 3
	ASCLIN4_ARXE			Receive input
	SENT1_SENT14B			Receive input channel 14
	I2C1_SCLD			Serial Clock Input 3
	EGTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	PINRSTD	I#		Reset input D
	T21EXE			T21 interrupt input E
	T2CCU0_3C			T2 capture 0 input 3C
	EXINT0D			Interrupt 0 input D
	EXINT6C			Interrupt 6 input C
	ADCOMPCH13			Analog input channel 13
	I2CSCLB			Serial clock input B
	P34.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN4_ATX	O3		Transmit output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output
	EGTM_TOUT148	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.2	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_3	O#6		T2 PWM channel 13
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG2	O		PMS debugging power mode K
W16	P34.4	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	QSPI2_MRSTD			Master SPI data input
	SENT1_SENT13B			Receive input channel 13
	ASCLIN16_ARXE			Receive input
	$\overline{\text{PCIE0\_CLKREQ\_INB\_N}}$			CLKREQ# input
	EGTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	UART_RXDJ	I#		Receive input J
	SSC_MRSTC			Master SPI data input C
	T20EXG			T20 interrupt input P
	T2CCU1_2C			T2 capture 1 input 2C
	EXINT1D			Interrupt 1 input D

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT10C			Interrupt 10 input C
	ADCOMPCH14			Analog input channel 14
	P34.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT149	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
	PCIE0_CLKREQ_N	O		CLKREQ# output
	PMS_DEBUG3	O		PMS debugging power mode K
Y16	P34.5	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	QSPI4_MRSTF			Master SPI data input
	SENT0_SENT13C			Receive input channel 13
	PCIE0_WAKE_INB_N			WAKE# input
	EGTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	WCAN_RXDJ	I#		Wake-up input J
	SSC_MTSRC			Slave SPI data input C
	T21EXF			T21 interrupt input F
	T2CCU1_3C			T2 capture 1 input 3C
	EXINT2D			Interrupt 2 input D
	EXINT11C			Interrupt 11 input C
	ADCOMPCH15			Analog input channel 15
	P34.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN8_ATX	O2		Transmit output
	CAN43_TXD	O3		CAN transmit output node 3
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	SENT0_SPC13	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT150	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 29 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P3.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	$\overline{\text{PCIE0\_WAKE\_N}}$	O		WAKE# output
	PMS_DEBUG4	O		PMS debugging power mode K

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Table 30 Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AF10	P35.0	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	SENT0_SENT10D			Receive input channel 10
	$\overline{\text{PCIE1\_PERSTB\_N}}$			PERST# input
	CAN41_RXDD			CAN receive input node 1
	WCAN_RXDK	I#		Wake-up input K
	T21EXL			T21 interrupt input L
	T2CCU1_0D			T2 capture 1 input 0D
	EXINT8D			Interrupt 8 input D
	I2CSDAC			Serial clock input C
	P35.0	O0		General-purpose output

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	—	O2		Reserved
	SENT0_SPC10	O3		Transmit output
	ASCLIN4_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT182	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.5	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	—	O#6		Reserved
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AF8	P35.1	I	SLOW / PU1 /	General-purpose input
	SENT1_SENT11C			Receive input channel 11

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN41_RXDC		VDDEVRSB / ES	CAN receive input node 1
	ASCLIN4_ARXF			Receive input
	WCAN_RXDL	I#		Wake-up input L
	T21EXM			T21 interrupt input M
	T2CCU0_0D			T2 capture 0 input 3D
	EXINT3D			Interrupt 3 input D
	EXINT12D			Interrupt 12 input D
	I2CSCLC			Serial clock input C
	P35.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	SENT1_SPC11	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT183	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.6	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_2	O#5		T2 PWM channel 02
	—	O#6		Reserved
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AE10	P35.2	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	I2C2_SDAE			Serial Data Input 4
	SENT0_SENT12C			Receive input channel 12
	CAN31_RXDE			CAN receive input node 1
	UART_RXDM	I#		Receive input M
	T20EXM			T20 interrupt input M
	T2CCU1_1D			T2 capture 1 input 1D
	EXINT9D			Interrupt 9 input D
	EXINT13D			Interrupt 13 input D
	P35.2	O0		General-purpose output
	—	O1		Reserved
	I2C2_SDA	O2		Serial Data Output
	SENT1_SPC12	O3		Transmit output
	—	O4		Reserved
	CAN41_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT184	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.7	O#0		General-purpose output

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AF11	P35.3	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN43_RXDE			CAN receive input node 3
	$\overline{\text{PCIE1\_WAKE\_INB\_N}}$			WAKE# input
	UART_RXDN	I#		Receive input N
	WCAN_RXDM			Wake-up input M
	T20EXN			T20 interrupt input N
	T2CCU1_2D			T2 capture 2 input 2D
	EXINT10D			Interrupt 10 input D
	EXINT14D			Interrupt 14 input D
	P35.3	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT185	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.5	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	$\overline{\text{PCIE1\_WAKE\_N}}$	O		WAKE# output
AE11	P35.4	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	I2C2_SCLE			Serial Clock Input 4
	ASCLIN5_ARXH			Receive input
	LETH0_P1_COLB			LETH PortX MII collision detection
	T20D	I#		T20 capture input D
	T21EXO			T21 interrupt input O
	T2CCU0_1D			T2 capture 0 input 3D
	EXINT4D			Interrupt 4 input D
	EXINT15D			Interrupt 15 input D

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P35.4	O0		General-purpose output
	—	O1		Reserved
	I2C2_SCL	O2		Serial Clock Output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT186	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.6	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AF13	P35.5	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	SENT1_SENT14C			Receive input channel 14
	PCIE1_CLKREQ_INB_N			CLKREQ# input
	UART_RXDO	I#		Bidirectional Receive pin O
	WCAN_RXDN			Wake-up input N
	T21D			T21 capture input D
	T21EXP			T21 interrupt input P
	T2CCU0_2D			T2 capture 0 input 3D
	EXINT5D			Interrupt 5 input D
	P35.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	SENT1_SPC14	O3		Transmit output
	CAN43_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT187	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.7	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_5	O#6		T2 PWM channel 15

(table continues...)

Table 30 (continued) Port 35 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PCIE1_CLKREQ_N	O		CLKREQ# output

3.2.22 BGA436_COM analog

Table 31 Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
W13	AN0	I	D / HighZ / VDDM	Analog Input 0
	ADC_TMADC0CH0			Analog Input for TMADC0 Channel 0
Y13	AN1	I	D / HighZ / VDDM	Analog Input 1
	ADC_TMADC0CH1			Analog Input for TMADC0 Channel 1
AB12	AN2	I	D / HighZ / VDDM	Analog Input 2
	ADC_TMADC0CH2			Analog Input for TMADC0 Channel 2
Y12	AN3	I	D / HighZ / VDDM	Analog Input 3
	ADC_TMADC0CH3			Analog Input for TMADC0 Channel 3
W12	AN4	I	D / HighZ / VDDM	Analog Input 4
	ADC_TMADC0CH4			Analog Input for TMADC0 Channel 4
	ADC_TMADC1CH0			Analog Input for TMADC1 Channel 0
AC12	AN5	I	D / HighZ / VDDM	Analog Input 5
	ADC_TMADC0CH5			Analog Input for TMADC0 Channel 5
	ADC_TMADC1CH1			Analog Input for TMADC1 Channel 1
W11	AN6	I	D / HighZ / VDDM	Analog Input 6
	ADC_TMADC0CH6			Analog Input for TMADC0 Channel 6
	ADC_TMADC1CH2			Analog Input for TMADC1 Channel 2

(table continues...)

Table 31 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y11	AN7	I	D / HighZ / VDDM	Analog Input 7
	ADC_TMADC0CH7			Analog Input for TMADC0 Channel 7
	ADC_TMADC1CH3			Analog Input for TMADC1 Channel 3
AB11	AN8	I	D / HighZ / VDDM	Analog Input 8
	ADC_TMADC0CH8			Analog Input for TMADC0 Channel 8
Y10	AN9	I	D / HighZ / VDDM	Analog Input 9
	ADC_TMADC0CH9			Analog Input for TMADC0 Channel 9
AC11	AN10	I	D / HighZ / VDDM	Analog Input 10
	ADC_TMADC0CH10			Analog Input for TMADC0 Channel 10
AB10	AN11	I	D / HighZ / VDDM	Analog Input 11
	ADC_TMADC0CH11			Analog Input for TMADC0 Channel 11
W10	AN12	I	D / HighZ / VDDM	Analog Input 12
	ADC_TMADC0CH12			Analog Input for TMADC0 Channel 12
AB9	AN13	I	D / HighZ / VDDM	Analog Input 13
	ADC_TMADC0CH13			Analog Input for TMADC0 Channel 13
Y9	AN14	I	D / HighZ / VDDM	Analog Input 14
	ADC_TMADC0CH14			Analog Input for TMADC0 Channel 14
W9	AN15	I	D / HighZ / VDDM	Analog Input 15
	ADC_TMADC0CH15			Analog Input for TMADC0 Channel 15
AB8	AN16	I	D / HighZ / VDDM	Analog Input 16
	ADC_TMADC1CH4			Analog Input for TMADC1 Channel 4
Y8	AN17/P40_10	I	S / PU1 / VDDM	Analog Input 17
	ADC_TMADC1CH5			Analog Input for TMADC1 Channel 5
	SENT0_SENT5A			Receive input channel 5
AB7	AN18/P40_11	I	S / PU1 / VDDM	Analog Input 18
	ADC_TMADC1CH6			Analog Input for TMADC1 Channel 6
	SENT1_SENT5A			Receive input channel 5
AB6	AN19/P40_12	I	S / PU1 / VDDM	Analog Input 19
	ADC_TMADC1CH7			Analog Input for TMADC1 Channel 7
	SENT0_SENT6A			Receive input channel 6
AC6	AN20	I	D / HighZ / VDDM	Analog Input 20
	ADC_TMADC1CH8			Analog Input for TMADC1 Channel 8

(table continues...)

Table 31 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
AC5	AN21	I	D / HighZ / VDDM	Analog Input 21
	ADC_TMADC1CH9			Analog Input for TMADC1 Channel 9
W8	AN22	I	D / HighZ / VDDM	Analog Input 22
	ADC_TMADC1CH10			Analog Input for TMADC1 Channel 10
V8	AN23	I	D / HighZ / VDDM	Analog Input 23
	ADC_TMADC1CH11			Analog Input for TMADC1 Channel 11
AB5	AN24/P40_0	I	S / PU1 / VDDM	Analog Input 24
	ADC_TMADC1CH12			Analog Input for TMADC1 Channel 12
	SENT0_SENT0A			Receive input channel 0
AB4	AN25/P40_1	I	S / PU1 / VDDM	Analog Input 25
	ADC_TMADC1CH13			Analog Input for TMADC1 Channel 13
	SENT1_SENT0A			Receive input channel 0
AA5	AN26/P40_2	I	S / PU1 / VDDM	Analog Input 26
	ADC_TMADC1CH14			Analog Input for TMADC1 Channel 14
	SENT0_SENT1A			Receive input channel 1
AA4	AN27/P40_3	I	S / PU1 / VDDM	Analog Input 27
	ADC_TMADC1CH15			Analog Input for TMADC1 Channel 15
	SENT1_SENT1A			Receive input channel 1
Y5	AN28/P40_13	I	S / PU1 / VDDM	Analog Input 28
	ADC_TMADC3CH0			Analog Input for TMADC3 Channel 0
	SENT1_SENT6A			Receive input channel 6
Y4	AN29/P40_14	I	S / PU1 / VDDM	Analog Input 29
	ADC_TMADC3CH1			Analog Input for TMADC3 Channel 1
	SENT0_SENT7A			Receive input channel 7
W7	AN30	I	D / HighZ / VDDM	Analog Input 30
	ADC_TMADC3CH2			Analog Input for TMADC3 Channel 2
V7	AN31	I	D / HighZ / VDDM	Analog Input 31
	ADC_TMADC3CH3			Analog Input for TMADC3 Channel 3
AF4	AN32/P40_4	I	S / PU1 / VDDM	Analog Input 32
	ADC_TMADC3CH4			Analog Input for TMADC3 Channel 4
	SENT0_SENT2A			Receive input channel 2
AF5	AN33/P40_5	I	S / PU1 / VDDM	Analog Input 33
	ADC_TMADC3CH5			Analog Input for TMADC3 Channel 5

(table continues...)

Table 31 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SENT2A			Receive input channel 2
AE3	AN34	I	D / HighZ / VDDM	Analog Input 34
	ADC_TMADC3CH6			Analog Input for TMADC3 Channel 6
AE5	AN35	I	D / HighZ / VDDM	Analog Input 35
	ADC_TMADC3CH7			Analog Input for TMADC3 Channel 7
AD2	AN36/P40_6	I	S / PU1 / VDDM	Analog Input 36
	ADC_TMADC3CH8			Analog Input for TMADC3 Channel 8
	SENT0_SENT3A			Receive input channel 3
AF3	AN37/P40_7	I	S / PU1 / VDDM	Analog Input 37
	ADC_TMADC3CH9			Analog Input for TMADC3 Channel 9
	SENT1_SENT3A			Receive input channel 3
AC1	AN38/P40_8	I	S / PU1 / VDDM	Analog Input 38
	ADC_TMADC3CH10			Analog Input for TMADC3 Channel 10
	SENT0_SENT4A			Receive input channel 4
AE4	AN39/P40_9	I	S / PU1 / VDDM	Analog Input 39
	ADC_TMADC3CH11			Analog Input for TMADC3 Channel 11
	SENT1_SENT4A			Receive input channel 4
AC2	AN40	I	D / HighZ / VDDM	Analog Input 40
	ADC_TMADC3CH12			Analog Input for TMADC3 Channel 12
AB1	AN41	I	D / HighZ / VDDM	Analog Input 41
	ADC_TMADC3CH13			Analog Input for TMADC3 Channel 13
AD1	AN42	I	D / HighZ / VDDM	Analog Input 42
	ADC_TMADC3CH14			Analog Input for TMADC3 Channel 14
AB2	AN43	I	D / HighZ / VDDM	Analog Input 43
	ADC_TMADC3CH15			Analog Input for TMADC3 Channel 15

3.2.23 BGA436_COM special

Table 32 Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
AB25	PHY2_RXN	I	PHY / VDDPHPHY2	(Ball name)
	PCIE1_RXN	I		Receive data (N line)

(table continues...)

Table 32 (continued) Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y25	PHY2_TXN	O	PHY / VDDPHPHY2	(Ball name)
	PCIE1_TXN	O		Transmit data (N line)
	SGBT_TXN1	O		Transmit data (N line)
AB26	PHY2_RXP	I	PHY / VDDPHPHY2	(Ball name)
	PCIE1_RXP	I		Receive data (P line)
Y26	PHY2_TXP	O	PHY / VDDPHPHY2	(Ball name)
	PCIE1_TXP	O		Transmit data (P line)
	SGBT_TXP1	O		Transmit data (P line)
T25	PHY0_RXN	I	PHY / VDDPHPHY0	(Ball name)
	SGMII0_RXN	I		Receive data (N line)
	PCIE0_RXN	I		Receive data (N line)
P25	PHY0_TXN	O	PHY / VDDPHPHY0	(Ball name)
	PCIE0_TXN	O		Transmit data (N line)
	SGMII0_TXN	O		Transmit data (N line)
T26	PHY0_RXP	I	PHY / VDDPHPHY0	(Ball name)
	SGMII0_RXP	I		Receive data (P line)
	PCIE0_RXP	I		Receive data (P line)
P26	PHY0_TXP	O	PHY / VDDPHPHY0	(Ball name)
	PCIE0_TXP	O		Transmit data (P line)
	SGMII0_TXP	O		Transmit data (P line)
E26	PHY1_TXP	O	PHY / VDDPHPHY1	(Ball name)
	SGBT_TXP0	O		Transmit data (P line)
	SGMII1_TXP	O		Transmit data (P line)
C26	PHY1_RXP	I	PHY / VDDPHPHY1	(Ball name)
	SGMII1_RXP	I		Receive data (P line)
E25	PHY1_TXN	O	PHY / VDDPHPHY1	(Ball name)
	SGBT_TXN0	O		Transmit data (N line)
	SGMII1_TXN	O		Transmit data (N line)
C25	PHY1_RXN	I	PHY / VDDPHPHY1	(Ball name)
	SGMII1_RXN	I		Receive data (N line)

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Table 33 System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
T23	PCIE1REFCLKP	I	PHY / VDDPHPHY2	Reference clock (P line)
T22	PCIE1REFCLKN	I	PHY / VDDPHPHY2	Reference clock (N line)
L25	PHYx_RESREF	I/O	—	Reference resistor
	SGMII0_RESREF	I/O		Reference resistor
	SGMII1_RESREF	I/O		Reference resistor
	PCIE0_RESREF	I/O		Reference resistor
	PCIE1_RESREF	I/O		Reference resistor
	SGBT_RESREF	I/O		Reference resistor
P23	PCIE0REFCLKP	I	PHY / VDDPHPHY0	Reference clock (P line)
P22	PCIE0REFCLKN	I	PHY / VDDPHPHY0	Reference clock (N line)
K25	XTAL2	O	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output
K26	XTAL1	I	—	XTAL1. Main Oscillator/PLL/Clock generator input
M19	TCK	I/O	—	Signal with hybrid_probe
	DAP0	I		DAP:DAP0 Clock Input
R22	TRST	I/O	—	Signal with hybrid_probe
	DAPE0	I		DAPE: DAPE0 Data I/O DAPE: DAPE0 Data I/O (PD Devices: VSS)
N19	TMS	I/O	—	Signal with hybrid_probe
	DAP1	I/O		DAP:DAP1 Data I/O
K19	ESR1	I/O	FAST / PU1 / VDDEXT	ESR1 pad data
	SMM_ESR1_PORT_IN	I		ESR1 pad data from bitslice
	PMS_ESR1WKP	I		ESR1 pin input
J19	ESR0	I/O	FAST / OD / VDDEXT	ESR0 pad data
	SMM_ESR0_PORT_IN	I		ESR0 pad data from bitslice
	PMS_ESR0WKP	I		ESR0 pin input

(table continues...)

Table 33 (continued) System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
K20	PORST	I/O	—	Power On Reset Input. Additional strong PD in case of power fail.

3.2.25 BGA436_COM supply

Table 34 Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
A26	NC1_A26	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AC4	NC1_AC4	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AF1	NC1_AF1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
Y7	NC1_Y7	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AE1	NC_AE1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AE2	NC_AE2	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AF2	NC_AF2	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AF7	NC_AF7	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
A1	VSSEXT	I	—	has to be connected to VSSEXT
B2	VSSEXT	I	—	External Vss
AC10	VAGND1	I	—	Negative Analog Reference Voltage 1
W5	VAGND2	I	—	Negative Analog Reference Voltage 1
AC9	VAREF1	I	—	Positive Analog Reference Voltage 1
W4	VAREF2	I	—	Positive Analog Reference Voltage 2
K11, K16, L10, L12, L15, L17, M11, M16, R11, R16, T10, T12, T15, T17, U11	VDD	I	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
W14	VDDEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM

(table continues...)

Table 34 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
A2, A25, AA22, AB23, AD25, AE26, B24, B3, D5, E21, E6, G19, G8	VDDEXT	I	—	External Power Supply (5V / 3.3V)
AC22	VDDEXTDC	I	—	External DCDC Supply (6.5V...5.5V / 5V / 3.3V)
H26	VDDEXTOSC	I	—	External Power Supply for Oscillator (shall be supplied with same level as used for VDDEXT)
D22	VDDEXT_SENSE	I/O	—	External Power Supply (5V / 3.3V)
A19, D19	VDDHSIF	I	—	hs interface supply (3.3V/1.8V)
AC8, AE8	VDDM	I	—	External Power Supply (5V / 3.3V)
L26	VDDPHPHY0	I	—	PHY0 External Power Supply (1.8V)
B26	VDDPHPHY1	I	—	PHY1 External Power Supply (1.8V)
AD26	VDDPHPHY2	I	—	PHY2 External Power Supply (1.8V)
N26, U26	VDDPHY0	I	—	PHY0 Digital Core Power Supply (0.9V / 0.95V / 1V)
D26, G26	VDDPHY1	I	—	PHY1 Digital Core Power Supply (0.9V / 0.95V / 1V)
AC26, W26	VDDPHY2	I	—	PHY2 Digital Core Power Supply (0.9V / 0.95V / 1V)
U16	VDD_SENSE	I/O	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
AC20	VGATE1N	O	—	DCDC N ch MOSFET gate driver output
AC21	VGATE1P	O	—	DCDC P ch MOSFET gate driver output
K12, K13, K14, K15, L13, L14, M10, M13, M14, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R13, R14, R17, T13, T14, U12, U13, U14	VSS	I	—	Digital Ground

(table continues...)

Table 34 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE25, AF26, B25, D4, E22, E5, G20, G7, H19, H8, W19, Y20	VSSEXT	I	—	External Vss
AB22, AC23	VSSEXTDC	I	—	DCDC Ground
H25	VSSEXTOSC	I	—	Oscillator Ground
D23	VSSEXT_SENSE	I/O	—	External Vss
B19, E19	VSSHSIF	I	—	High Speed Interface Digital Ground
AC7, AE7	VSSM	I	—	External Vss
AC25, D25, G25, N25, U25, W25	VSSPHY	I	—	PHY Digital Ground
U15	VSS_SENSE	I/O	—	Digital Ground

3.3 BGA292_COM package variant pin configuration

Related information

Logic symbols for package variants on page 31
BGA436_COM package variant pin configuration on page 32
Pad Sequence on page 384
Legend on page 405

3.3.1 BGA292_COM port 00

Table 35 Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L1	P00.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	MSC0_INJ0			Injection signal from port
	GETH0_PX_MDIOA			PortX MDIO input
	EGTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	EGTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	P00.0	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT9	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	GETH0_PX_MDIO0	O		PortX MDIO output
L2	P00.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	SENT0_SENT0B			Receive input channel 0
	EGTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN2_11			Mux input channel 2 of TIM module 1
	EGTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH11	AI		Analog Input for TMADC2 Channel 11
	P00.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	SENT0_SPC0	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT10	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M1	P00.2	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT0B			Receive input channel 0
	ASCLIN24_ARXB_F			Receive input
	EGTM_CDTM1_DTM2_5			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_5			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH10	AI		Analog Input for TMADC2 Channel 10
	P00.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	CAN21_TXD	O3		CAN transmit output node 1
	PSI5_TX0	O4		TXD outputs (send data)
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI3_SLSO4	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT11	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M2	P00.3	I	SLOW / PU1 /	General-purpose input
	PSI5_RX1A			RXD inputs (receive data) channel 1

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN03_RXDA		VDDEXT / ES1	CAN receive input node 3
	CAN21_RXDA			CAN receive input node 1
	PSI5S0_RXA			RX data input
	SENT0_SENT1B			Receive input channel 1
	ASCLIN12_ARXA_F			Receive input
	EGTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	EGTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	ADC_TMADC2CH9	AI		Analog Input for TMADC2 Channel 9
	P00.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	ASCLIN12_ATX_F	O3		Transmit output
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT12	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N1	P00.4	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SCU_E_REQ2C			ERU channel 2 input C
	SENT1_SENT1B			Receive input channel 1
	ASCLIN10_ARXA			Receive input
	EGTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH8	AI		Analog Input for TMADC2 Channel 8
	P00.4	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PSI5S0_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	—	O5		Reserved
	SENT1_SPC1	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT13	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N2	P00.5	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT2B			Receive input channel 2
	CAN11_RXDB			CAN receive input node 1
	ASCLIN12_ARXB_F			Receive input
	EGTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_2			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	ADC_TMADC2CH7	AI		Analog Input for TMADC2 Channel 7
	P00.5	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	SENT0_SPC2	O6		Transmit output
	LETH0_P3_TXD	O7		LETH PortX TC14 interface transmit data output

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CANXL03_TXD	O8		CANXL transmit output node 3
	EGTM_TOUT14	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N4	P00.6	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	CANXL03_RXDC			CANXL receive input node 3
	SENT1_SENT2B			Receive input channel 2
	ASCLIN5_ARXA			Receive input
	EGTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	ADC_TMADC2CH6	AI		Analog Input for TMADC2 Channel 6
	P00.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC2	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT15	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P1	P00.7	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT3B			Receive input channel 3
	EGTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_3			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_3			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	ADC_TMADC2CH5	AI		Analog Input for TMADC2 Channel 5
	P00.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	SENT0_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT16	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P4	P00.8	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT3B			Receive input channel 3
	ASCLIN10_ARXB			Receive input
	EGTM_CDTM1_DTM3_2			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_10			Mux input channel 7 of TIM module 1
	EGTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	ADC_TMADC2CH4	AI		Analog Input for TMADC2 Channel 4
	P00.8	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO6	O2		Master slave select output

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN10_ATX	O3		Transmit output
	CAN40_TXD	O4		CAN transmit output node 0
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT17	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P2	P00.9	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT4B			Receive input channel 4
	ASCLIN13_ARXA_F			Receive input
	ASCLIN4_ARXG			Receive input
	EGTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	EGTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	ADC_TMADC2CH3	AI		Analog Input for TMADC2 Channel 3
	P00.9	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	ADC_EMUXCTRL13	O4		EMUX1 Control from TMADC to PORTS
	ASCLIN4_ATX	O5		Transmit output
	SENT0_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT18	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P3_MDC	O15		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
P5	P00.10	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT1_SENT4B			Receive input channel 4
	ASCLIN10_ARXE			Receive input
	EGTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	ADC_TMADC2CH2	AI		Analog Input for TMADC2 Channel 2
	P00.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN13_ATX_F	O3		Transmit output
	ASCLIN4_ATX	O4		Transmit output
	—	O5		Reserved
	SENT1_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT19	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R1	P00.11	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	SENT0_SENT5B			Receive input channel 5
	ASCLIN13_ARXB_F			Receive input
	CAN40_RXDA			CAN receive input node 0
	EGTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	ADC_TMADC2CH1	AI		Analog Input for TMADC2 Channel 1
	P00.11	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO	O2		Slave select signal output
	ASCLIN13_ATX_F	O3		Transmit output
	—	O4		Reserved
	ASCLIN24_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT20	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R2	P00.12	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	SENT1_SENT5B			Receive input channel 5
	ASCLIN24_ARXA_F			Receive input
	LETH0_P3_RXDE			LETH PortX TC14 interface receive data input
	CANXL03_RXDE			CANXL receive input node 3
	EGTM_CDTM0_DTM2_5			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_5			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	ADC_TMADC2CH0	AI		Analog Input for TMADC2 Channel 0

(table continues...)

Table 35 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P00.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	ASCLIN24_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT21	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

3.3.2 BGA292_COM port 01

Table 36 Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L5	P01.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_SLSIB			Slave select input
	SENT1_SENT12A			Receive input channel 12
	CAN32_RXDA			CAN receive input node 2
	LETH0_P0_MDIOB			LETH PortX MDIO interface data input
	LETH0_P0_EDB			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	EGTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	ADC_TMADC2CH14	AI		Analog Input for TMADC2 Channel 14
	P01.3	O0		General-purpose output

(table continues...)

Table 36 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	—	O3		Reserved
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT111	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
L4	P01.4	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN01_RXDC			CAN receive input node 1
	SENT0_SENT13A			Receive input channel 13
	EGTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	EGTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH13	AI		Analog Input for TMADC2 Channel 13
	P01.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN9_ASLSO_F	O3		Slave select signal output
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT112	O9		eGTM muxed output

(table continues...)

Table 36 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M5	P01.5	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MRSTC			Master SPI data input
	ASCLIN9_ARXA_F			Receive input
	SENT1_SENT13A			Receive input channel 13
	LETH0_P0_RXDG			LETH PortX TC14 interface receive data input
	CANXL00_RXDG			CANXL receive input node 0
	EGTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	EGTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH12	AI		Analog Input for TMADC2 Channel 12
	P01.5	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT113	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

(table continues...)

Table 36 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
M4	P01.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_MTSRC			Slave SPI data input
	CAN32_RXDD			CAN receive input node 2
	EGTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	P01.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN12_ATX	O2		Transmit output
	ASCLIN9_ASCLK_F	O3		Shift clock output
	QSPI3_MTSR	O4		Master SPI data output
	ASCLIN9_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT114	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N5	P01.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI3_SCLKC			Slave SPI clock inputs
	ASCLIN9_ARXB_F			Receive input
	EGTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	P01.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN9_ATX_F	O3		Transmit output
	QSPI3_SCLK	O4		Master SPI clock output
	ASCLIN26_ATX_F	O5		Transmit output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 36 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT115	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.3 BGA292_COM port 02

Table 37 Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
F1	P02.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXG			Receive input
	SCU_E_REQ3C			ERU channel 3 input C
	CAN31_RXDC			CAN receive input node 1
	ADC_TRIG56			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	P02.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLSO1_F	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	ERAY0_TXDA	O6		Transmit Channel A
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT0_F	O9		eGTM muxed output
	—	O10		Reserved
	QSPI3_SLSO5_F	O11		Master slave select output

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN8_ASCLK_F	O12		Shift clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G2	P02.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2B			ERU channel 2 input B
	SENT0_SENT14A			Receive input channel 14
	ADC_TRIG57			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	LETH0_P0_RXDC			LETH PortX TC14 interface receive data input
	CANXL00_RXDC			CANXL receive input node 0
	P02.1	O0		General-purpose output
	—	O1		Reserved
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT1_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G1	P02.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT7B			Receive input channel 7
	EGTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_6			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	EGTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	P02.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3_F	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDB	O6		Transmit Channel B
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O8		CANXL transmit output node 1
	EGTM_TOUT2_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H2	P02.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	PSI5_RX0B			RXD inputs (receive data) channel 0
	SENT1_SENT6B			Receive input channel 6
	EGTM_CDTM0_DTM3_6			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM3_6			Input mux of CDTM1_DTM3_AUXIN0/1

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	LETH0_P1_RXDC			LETH PortX TC14 interface receive data input
	CANXL01_RXDC			CANXL receive input node 1
	P02.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT3_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H1	P02.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT6B			Receive input channel 6
	QSPI3_SLSIA			Slave select input
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	EGTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	EGTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOC			LETH PortX MDIO interface data input
	P02.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0_F	O3		Master slave select output
	PSI5S0_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT4_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
J2	P02.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT1C			Receive input channel 1
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S0_RXB			RX data input
	QSPI3_MRSTA_F			Master SPI data input
	EGTM_CDTM1_DTM3_7			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM5_6			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM5_6			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	LETH0_P1_EDC			LETH PortX TC14 interface energy detection input

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIOC			LETH PortX MDIO interface data input
	P02.5	O0		General-purpose output
	—	O1		Reserved
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	—	O4		Reserved
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT5_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
J1	P02.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT1_SENT0C			Receive input channel 0
	ASCLIN10_ARXH			Receive input
	QSPI3_MTSRA			Slave SPI data input
	EGTM_CDTM0_DTM2_7			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM2_7			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	P02.6	O0		General-purpose output
	—	O1		Reserved
	PSI5S0_TX	O2		TX data output

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI3_MTSR_F	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT6_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K2	P02.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDH			CAN receive input node 2
	SENT0_SENT1C			Receive input channel 1
	SCU_E_REQ0F			ERU channel 0 input F
	QSPI3_SCLKA			Slave SPI clock inputs
	ADC_TRIG58			Triggers from PORTS to ADC
	EGTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	EGTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	EGTM_CDTM2_DTM3_6			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI3_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT7_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K1	P02.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT0C			Receive input channel 0
	CAN30_RXDB			CAN receive input node 0
	SCU_E_REQ5G			ERU channel 5 input G
	ADC_TRIG59			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	P02.8	O0		General-purpose output
	—	O1		Reserved
	QSPI3_SLSO5_F	O2		Master slave select output
	ASCLIN8_ASCLK_F	O3		Shift clock output
	—	O4		Reserved
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	GETH0_P0_MDC	O6		Port0 MDIO Clock
	—	O7		Reserved
	GETH0_P1_MDC	O8		Port1 MDIO Clock
	EGTM_TOUT8_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
J4	P02.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT10B			Receive input channel 10
	ASCLIN8_ARXA			Receive input
	EGTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	EGTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM3_7			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	ASCLIN8_ATX_F	O3		Transmit output
	CAN30_TXD	O4		CAN transmit output node 0
	CAN01_TXD	O5		CAN transmit output node 1
	SENT0_SPC10	O6		Transmit output
	ADC_EMUXCTRL03	O7		EMUX0 Control from TMADC to PORTS
	—	O8		Reserved
	EGTM_TOUT116_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K5	P02.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXC			Receive input
	CAN01_RXDE			CAN receive input node 1
	SENT1_SENT10B			Receive input channel 10
	ASCLIN8_ARXB_F			Receive input
	EGTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM2_6			Input mux of CDTM1_DTM2_AUXIN0/1

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	EGTM_CDTM2_DTM2_7			Input mux of CDTM2_DTM2_AUXIN0/1
	P02.10	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT1_SPC10	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT117_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K4	P02.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT11B			Receive input channel 11
	ASCLIN26_ARXA_F			Receive input
	CAN30_RXDD			CAN receive input node 0
	SCU_E_REQ7G			ERU channel 7 input G
	EGTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	ADC_TMADC2CH15	AI		Analog Input for TMADC2 Channel 15
	P02.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN8_ASLSO_F	O3		Slave select signal output
	ASCLIN10_ATX	O4		Transmit output

(table continues...)

Table 37 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output
	ASCLIN26_ATX_F	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT118_F	O9		eGTM muxed output
	LETH0_P2_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.4 BGA292_COM port 03

Table 38 Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B1	P03.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN11_ARXH			Receive input
	CAN30_RXDE			CAN receive input node 0
	QSPI6_MRSTC			Master SPI data input
	P03.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	QSPI3_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MRST	O8		Slave SPI data output
	EGTM_TOUT271	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIIB_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRB_TXEN	O		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKB - registered*)
C2	P03.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN5_ARXG			Receive input
	QSPI6_SCLKC			Slave SPI clock inputs
	P03.1	O0		General-purpose output
	—	O1		Reserved
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CAN23_TXD	O7		CAN transmit output node 3
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT272	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
C1	P03.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDF			CAN receive input node 3
	QSPI6_MTSRA			Slave SPI data input
	P03.2	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT273	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D2	P03.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN19_ARXC			Receive input
	LETH0_P2_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKB)
	QSPI7_MRSTH			Master SPI data input
	P03.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_MRST	O7		Slave SPI data output
	QSPI6_SLSO4	O8		Master slave select output
	EGTM_TOUT274	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
D1	P03.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_CRSD			LETH PortX MII carrier sense
	ASCLIN8_ARXF			Receive input
	CAN11_RXDH			CAN receive input node 1
	QSPI6_SLSIA			Slave select input
	P03.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI3_SLSO0	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	ASCLIN19_ATX	O5		Transmit output
	CAN11_TXD	O6		CAN transmit output node 1
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI6_SLSO5	O8		Master slave select output
	EGTM_TOUT275	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E2	P03.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	P03.5	O0		General-purpose output
	—	O1		Reserved
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_MTSR	O7		Master SPI data output
	QSPI6_SLSO6	O8		Master slave select output

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT276	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E1	P03.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN43_RXDC			CAN receive input node 3
	ERAY1_RXDB2			Receive Channel B2
	ASCLIN23_ARXC			Receive input
	P03.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN19_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_SLSO9	O7		Master slave select output
	QSPI6_SLSO7	O8		Master slave select output
	EGTM_TOUT277	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
F2	P03.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P3_COLC			LETH PortX MII collision detection
	LETH0_P3_RXDC			LETH PortX TC14 interface receive data input
	QSPI7_MRSTC			Master SPI data input
	P03.7	O0		General-purpose output

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	CAN43_TXD	O2		CAN transmit output node 3
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT278	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E4	P03.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SENT0_SENT6D			Receive input channel 6
	P03.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN2_ATX	O3		Transmit output
	ASCLIN8_ATX	O4		Transmit output
	CAN23_TXD	O5		CAN transmit output node 3
	SENT0_SPC6	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT279	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKD)

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_RMIIB_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRB_TXD1	O		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKB - registered*)
F5	P03.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI6_SLSIC			Slave select input
	SENT0_SENT11D			Receive input channel 11
	CAN01_RXDG			CAN receive input node 1
	P03.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN8_ASCLK	O3		Shift clock output
	ASCLIN12_ATX	O4		Transmit output
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT280	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIIB_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKB)
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
	LETH0_P2_RMIIRB_TXD0	O		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKB - registered*)
F4	P03.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN12_ARXC			Receive input
	ASCLIN8_ARXG			Receive input
	P03.10	O0		General-purpose output

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT281	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
G5	P03.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SDAA			Serial Data Input 0
	QSPI7_MTSRC			Slave SPI data input
	QSPI3_SLSIC			Slave select input
	ASCLIN23_ARXD			Receive input
	P03.11	O0		General-purpose output
	—	O1		Reserved
	I2C2_SDA	O2		Serial Data Output
	ASCLIN8_ASLSO	O3		Slave select signal output
	CAN22_TXD	O4		CAN transmit output node 2
	CAN31_TXD	O5		CAN transmit output node 1
	ASCLIN26_ATX	O6		Transmit output
	QSPI7_MTSR	O7		Master SPI data output
	CAN01_TXD	O8		CAN transmit output node 1
	EGTM_TOUT282	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKB)

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIID_TXD2	O12		LETH PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G4	P03.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C2_SCLA			Serial Clock Input 0
	CAN22_RXDF			CAN receive input node 2
	P03.12	O0		General-purpose output
	—	O1		Reserved
	I2C2_SCL	O2		Serial Clock Output
	ASCLIN23_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_SCLK	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT283	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H5	P03.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDF			CAN receive input node 2
	ASCLIN26_ARXD			Receive input
	P03.13	O0		General-purpose output
	—	O1		Reserved
	CAN02_TXD	O2		CAN transmit output node 2
	—	O3		Reserved
	—	O4		Reserved

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT284	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H4	P03.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	LETH0_P2_MDIOD			LETH PortX MDIO interface data input
	LETH0_P2_EDD			LETH PortX TC14 interface energy detection input
	CAN01_RXDF			CAN receive input node 1
	QSPI3_MTSRD			Slave SPI data input
	P03.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX	O2		Transmit output
	ASCLIN12_ATX	O3		Transmit output
	ASCLIN9_ASCLK	O4		Shift clock output
	QSPI3_MTSR	O5		Master SPI data output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT285	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 38 (continued) Port 03 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
J5	P03.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN11_ARXG			Receive input
	LETH0_P2_RXDD			LETH PortX TC14 interface receive data input
	P03.15	O0		General-purpose output
	—	O1		Reserved
	ASCLIN7_ATX	O2		Transmit output
	CAN01_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT286	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIB_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKB)
	LETH0_P2_MIID_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P2_TXCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

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Table 39 Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A5	P10.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs

(table continues...)

Table 39 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCU_E_REQ2A			ERU channel 2 input A
	EGTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	LETH0_P2_MII_RXD2B			LETH PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKB)
	ASCLIN22_ARXC_F			Receive input
	P10.2	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI1_SCLK_F	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	ASCLIN2_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	QSPI7_SLSO2	O8		Master slave select output
	EGTM_TOUT104	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO1	O12		Master slave select output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E6	P10.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3A			ERU channel 3 input A
	ASCLIN2_ARXH_F			Receive input
	MSC0_SDI5			Upstream assynchronous input signal
	EGTM_CDTM0_DTM3_2			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1

(table continues...)

Table 39 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM2_5			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	EGTM_CDTM2_DTM3_3			Input mux of CDTM2_DTM3_AUXIN0/1
	LETH0_P2_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_RMII_CRSDVD			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_MII_RXDVD			Receive data valid and Carrier sense and receive data valid
	P10.3	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI1_MTSR_F	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	QSPI7_SCLK	O8		Master SPI clock output
	EGTM_TOUT105	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO15	O12		Master slave select output
	ASCLIN1_ASLSO	O13		Slave select signal output
	ASCLIN3_ASLSO	O14		Slave select signal output
	—	O15		Reserved
B5	P10.5	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	QSPI1_MRSTE			Master SPI data input
	CAN20_RXDA			CAN receive input node 0
	MSC0_INJ1			Injection signal from port
	ASCLIN22_ARXB_F			Receive input
	EGTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1
	QSPI5_MRSTE			Master SPI data input
	EGTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0

(table continues...)

Table 39 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	LETH0_P3_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P3_RXCLKC)
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX_F	O2		Transmit output
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	—	O5		Reserved
	ASCLIN22_ATX	O6		Transmit output
	—	O7		Reserved
	QSPI1_MRST	O8		Slave SPI data output
	EGTM_TOUT107	O9		eGTM muxed output
	QSPI5_MRST	O10		Slave SPI data output
	LETH0_P3_TXD	O11		LETH PortX TC14 interface transmit data output
	—	O12		Reserved
	ERAY0_TXDB	O13		Transmit Channel B
	ERAY1_TXDB	O14		Transmit Channel B
	—	O15		Reserved
A4	P10.6	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXD_F			Receive input
	QSPI3_MTSRB			Slave SPI data input
	ASCLIN7_ARXH			Receive input
	SENT1_SENT12B			Receive input channel 12
	ASCLIN23_ARXA_F			Receive input
	EGTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P3_MDIOF			LETH PortX MDIO interface data input
	LETH0_P3_EDF			LETH PortX TC14 interface energy detection input
	QSPI1_MRSTC_F			Master SPI data input
	EGTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	PMS_HWCFG5IN			HWCFG5 pin input

(table continues...)

Table 39 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P10.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK_F	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	QSPI1_MRST_F	O6		Slave SPI data output
	ERAY1_TXENB	O7		Transmit Enable Channel B
	—	O8		Reserved
	EGTM_TOUT108	O9		eGTM muxed output
	QSPI5_MTSR	O10		Master SPI data output
	—	O11		Reserved
	QSPI2_SLSO14	O12		Master slave select output
	CAN13_TXD	O13		CAN transmit output node 3
	ERAY0_TXENB	O14		Transmit Enable Channel B
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
A3	P10.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN2_ACTSA_F			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0B			ERU channel 0 input B
	ASCLIN23_ARXB			Receive input
	ERAY1_RXDB3			Receive Channel B3
	CAN10_RXDH			CAN receive input node 0
	CAN13_RXDH			CAN receive input node 3
	ASCLIN9_ARXG			Receive input
	ASCLIN20_ARXC_F			Receive input
	CANXL00_RXDE			CANXL receive input node 0
	QSPI7_MTSRD			Slave SPI data input
	EGTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	LETH0_P3_RXDF			LETH PortX TC14 interface receive data input

(table continues...)

Table 39 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_REFCLKB			LETH PortX RMII reference clock
	LETH0_P2_RXCLKB			LETH PortX MII receive clock
	LETH0_P2_REFCLKD			MII or RMII Clock from PAD
	LETH0_P2_RXCLKD			LETH PortX MII receive clock
	P10.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN23_ATX_F	O2		Transmit output
	QSPI3_MRST	O3		Slave SPI data output
	ASCLIN9_ATX	O4		Transmit output
	CAN20_TXD	O5		CAN transmit output node 0
	CAN12_TXD	O6		CAN transmit output node 2
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI7_MRST	O8		Slave SPI data output
	EGTM_TOUT109	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN0_ARTS	O12		Ready to send output
	QSPI2_SLSO13	O13		Master slave select output
	—	O14		Reserved
	ASCLIN20_ATX_F	O15		Transmit output
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B4	P10.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	CAN12_RXDB			CAN receive input node 2
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1B			ERU channel 1 input B
	QSPI1_SLSIC			Slave select input
	CAN20_RXDB			CAN receive input node 0
	SENT1_SENT14A			Receive input channel 14
	CAN02_RXDG			CAN receive input node 2
	ERAY1_RXDA3			Receive Channel A3
	QSPI7_MRSTG			Master SPI data input
	EGTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0

(table continues...)

Table 39 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	LETH0_P2_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD1D			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	P10.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ARTS_F	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	ASCLIN23_ATX_F	O4		Transmit output
	ASCLIN5_ASLSO	O5		Slave select signal output
	ASCLIN7_ASLSO	O6		Slave select signal output
	ASCLIN20_ATX_F	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT110	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.6 BGA292_COM port 13

Table 40 Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B7	P13.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN10_ARXC_F			Receive input
	ASCLIN21_ARXA_F			Receive input
	QSPI2_MRSTG_F			Master SPI data input
	CAN11_RXDG			CAN receive input node 1
	EGTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	P13.0	O0		General-purpose output

(table continues...)

Table 40 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN10_ATX_F	O2		Transmit output
	QSPI2_SCLKN_F	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
	—	O8		Reserved
	EGTM_TOUT91	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A7	P13.1	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD_F			Receive input
	EGTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	P13.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI2_SCLKP_F	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
	QSPI2_SCLK_F	O8		Master SPI clock output
	EGTM_TOUT92	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 40 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B6	P13.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SDAB			Serial Data Input 1
	CAN33_RXDA			CAN receive input node 3
	EGTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	P13.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASCLK_F	O2		Shift clock output
	QSPI2_MTSRN_F	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	ASCLIN21_ATX_F	O7		Transmit output
	QSPI2_MTSR_F	O8		Master SPI data output
	EGTM_TOUT93	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A6	P13.3	I	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN21_ARXB			Receive input
	EGTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN10_ASLSO_F	O2		Slave select signal output
	QSPI2_MTSRP_F	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	ASCLIN21_ATX_F	O6		Transmit output

(table continues...)

Table 40 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN33_TXD	O7		CAN transmit output node 3
	—	O8		Reserved
	EGTM_TOUT94	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.7 BGA292_COM port 14

Table 41 Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A9	P14.0	I	FAST / PU1 / VDDEXT / ES2	General-purpose input
	SENT1_SENT8D			Receive input channel 8
	CAN41_RXDB			CAN receive input node 1
	EGTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	LETH0_P2_REFCLKA			LETH PortX RMII reference clock
	LETH0_P2_RXCLKA			LETH PortX MII receive clock
	LETH0_P2_REFCLKC			MII or RMII Clock from PAD
	LETH0_P2_RXCLKC			LETH PortX MII receive clock
	P14.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT80	O9		eGTM muxed output

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P1_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O15		CANXL transmit output node 1
B9	P14.1	I	FAST / PU1 / VDDEXT / ES2	General-purpose input
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA_F			Receive input
	SENT0_SENT9D			Receive input channel 9
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3B			ERU channel 3 input B
	LETH0_P0_RXDB			LETH PortX TC14 interface receive data input
	CANXL00_RXDB			CANXL receive input node 0
	EGTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	PMS_PINAWKP			PINA (P14.1) pin input
	LETH0_P2_MII_RMII_RXD0A			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	CAN41_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT81	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D9	P14.2	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	LETH0_P2_MII_RXERA			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKA)
	LETH0_P2_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P2_RXCLKC)
	LETH0_P1_RXDD			LETH PortX TC14 interface receive data input
	CANXL01_RXDD			CANXL receive input node 1
	EGTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved
	GETH0_P0_PPS0B	O8		GETH Port0 Pulse Per Second (output A or B)
	EGTM_TOUT82	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P0_PPS	O13		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A8	P14.3	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream assynchronous input signal
	SCU_E_REQ1A			ERU channel 1 input A
	LETH0_P1_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	PMS_HWCFG3IN			HWCFG3 pin input
	LETH0_P2_MII_RMII_RXD1A			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P0_PPS0A	O8		GETH Port0 Pulse Per Second (output A or B)
	EGTM_TOUT83	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O15		CANXL transmit output node 3
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E9	P14.4	I	SLOW / PU2 / VDDEXT / ES	General-purpose input
	EGTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_1			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_1			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	PMS_HWCFG6IN			HWCFG6 pin input
	LETH0_P1_RXDA			LETH PortX TC14 interface receive data input
	CANXL01_RXDA			CANXL receive input node 1
	P14.4	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN0_ARTS_F	O3		Ready to send output
	QSPI2_SLSO4	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P1_PPS1A	O8		GETH Port1 Pulse Per Second (output A or B)
	EGTM_TOUT84	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)
	LETH0_P3_MIIC_TXD3	O13		LETH PortX MII transmit data bit 3 (to be used with LETH0_P3_TXCLKC)
	LETH0_P3_MDC	O14		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B8	P14.5	I	FAST / PU2 /	General-purpose input
	QSPI5_MRSTB			Master SPI data input

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM4_1		VDDEXT / ES	Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P2_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX_F	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	QSPI2_SLSO4_F	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	ERAY1_TXDB	O7		Transmit Channel B
	—	O8		Reserved
	EGTM_TOUT85	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O15		CANXL transmit output node 3
E8	P14.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI5_MTSRB			Slave SPI data input
	LETH0_P2_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOC			LETH PortX MDIO interface data input
	LETH0_P2_MII_RXD2C			LETH PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	P14.6	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI5_MTSR	O2		Master SPI data output
	QSPI2_SLSO2_F	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	ASCLIN0_ASLSO	O5		Slave select signal output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	ERAY1_TXENB	O7		Transmit Enable Channel B
	—	O8		Reserved
	EGTM_TOUT86	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D8	P14.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDB0			Receive Channel B0
	ERAY1_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input
	ASCLIN20_ARXA			Receive input
	QSPI7_MTSRA			Slave SPI data input
	LETH0_P2_RXDC			LETH PortX TC14 interface receive data input
	CANXL02_RXDC			CANXL receive input node 2
	EGTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	P14.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ARTS_F	O2		Ready to send output
	QSPI2_SLSO4_F	O3		Master slave select output
	ASCLIN9_ATX	O4		Transmit output

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN20_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT87	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	LETH0_P2_RMIIRA_TXEN	O		LETH PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA - registered*)
E7	P14.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	ERAY1_RXDA0			Receive Channel A0
	QSPI7_MRSTA			Master SPI data input
	LETH0_P0_RXDA			LETH PortX TC14 interface receive data input
	CANXL00_RXDA			CANXL receive input node 0
	EGTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	LETH0_P2_TXCLKA			PortX MII transmit clock
	LETH0_P2_TXCLKC			PortX MII transmit clock
	P14.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO_F	O3		Slave select signal output
	—	O4		Reserved

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN20_ATX	O7		Transmit output
	GETH0_P1_PPS1B	O8		GETH Port1 Pulse Per Second (output A or B)
	EGTM_TOUT88	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D7	P14.9	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN0_ACTSA			Clear to send input
	QSPI2_MRSTFN_F			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	ASCLIN20_ARXB			Receive input
	LETH0_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOA			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	P14.9	O0		General-purpose output
	—	O1		Reserved
	CAN23_TXD	O2		CAN transmit output node 3
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	ERAY1_TXENA	O7		Transmit Enable Channel A
	—	O8		Reserved
	EGTM_TOUT89	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIIA_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
	LETH0_P2_RMIIRA_TXD1	O		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA - registered*)
D6	P14.10	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN23_RXDA			CAN receive input node 3
	QSPI2_MRSTFP_F			Master SPI data input (LVDS P line)
	EGTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	P14.10	O0		General-purpose output
	—	O1		Reserved
	QSPI5_SCLK	O2		Master SPI clock output
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	ERAY1_TXDA	O7		Transmit Channel A
	LETH0_P2_RMIIA_TXD0	O8		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA)
	EGTM_TOUT90	O9		eGTM muxed output
	LETH0_P2_MIIA_TXD0	O10		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKC)
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL02_TXD	O15		CANXL transmit output node 2

(table continues...)

Table 41 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_RMIIRA_TXD0	O		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA - registered*)

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Table 42 Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D12	P15.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SDMMC0_DAT7_IN			Read data in
	EGTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	LETH0_P3_REFCLKA			RMII Clock from PAD
	LETH0_P3_RXCLKA			LETH PortX MII receive clock
	LETH0_P3_REFCLKC			RMII Clock from PAD
	LETH0_P3_RXCLKC			LETH PortX MII receive clock
	P15.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	ASCLIN1_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT71	O9		eGTM muxed output
	—	O10		Reserved
	CANXL00_TXD	O11		CANXL transmit output node 0
	—	O12		Reserved
	LETH0_P3_TXD	O13		LETH PortX TC14 interface transmit data output
	CANXL03_TXD	O14		CANXL transmit output node 3
	—	O15		Reserved
	SDMMC0_DAT7	O		Write data out
B11	P15.1	I	FAST / PU1 /	General-purpose input
	CAN02_RXDA			CAN receive input node 2

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ARXA_F		VDDEXT / ES	Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7B			ERU channel 7 input B
	LETH0_P0_RXDE			LETH PortX TC14 interface receive data input
	LETH0_P3_RXDB			LETH PortX TC14 interface receive data input
	CANXL03_RXDB			CANXL receive input node 3
	EGTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	LETH0_P3_MII_RXDVA			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_RMII_CRSDVA			Receive data valid and Carrier sense and receive data valid
	LETH0_P3_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid
	P15.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	SDMMC0_CLK	O7		Card clock
	—	O8		Reserved
	EGTM_TOUT72	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E12	P15.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	SENT0_SENT5D			Receive input channel 5
	QSPI2_MRSTE			Master SPI data input

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	XSPI0_RXD3B			Receive data
	LETH0_P3_TXCLKA			PortX MII transmit clock
	LETH0_P3_TXCLKC			PortX MII transmit clock
	P15.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SLSO0	O3		Master slave select output
	ASCLIN1_ATX_F	O4		Transmit output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK	O6		Shift clock output
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT73	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB3	O		Transmit data
B10	P15.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	SDMMC0_CMD_IN			Command in
	EGTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	LETH0_P2_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P2_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid
	P15.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SCLK	O3		Master SPI clock output

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT74	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXER	O12		LETH PortX MII transmit error (to be used with LETH0_P3_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_CMD	O		Command out
D11	P15.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0A			ERU channel 0 input A
	SENT1_SENT5D			Receive input channel 5
	CAN42_RXDB			CAN receive input node 2
	QSPI7_MRSTF_F			Master SPI data input
	LETH0_P3_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P3_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	P15.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	ASCLIN19_ATX_F	O4		Transmit output
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	QSPI7_MTSR_F	O7		Master SPI data output

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT75	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P3_TXCLKC)
	LETH0_P3_RMIIA_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P3_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
A10	P15.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN1_ARXB_F			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4D			ERU channel 4 input D
	EGTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	P15.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	CAN42_TXD	O4		CAN transmit output node 2
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT76	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P3_TXCLKC)

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P3_RMIIA_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P3_REFCLKA)
	LETH0_P3_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
E11	P15.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MTSRB			Slave SPI data input
	ASCLIN19_ARXA_F			Receive input
	EGTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	LETH0_P3_MII_RMII_RXD1A			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P3_RXCLKA or LETH0_P3_REFCLKA)
	LETH0_P3_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P3_RXCLKC or LETH0_P3_REFCLKC)
	P15.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	QSPI5_SLSO3	O4		Master slave select output
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT77	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
D10	P15.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	ASCLIN19_ARXB_F			Receive input

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN43_RXDB			CAN receive input node 3
	QSPI7_MRSTE_F			Master SPI data input
	EGTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	P15.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	ASCLIN19_ATX_F	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	QSPI7_SLSO10_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT78	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P3_MIIA_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P3_TXCLKA)
	LETH0_P3_MIIC_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P3_TXCLKC)
	LETH0_P3_RMIIA_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P3_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
E10	P15.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5A			ERU channel 5 input A
	GETH0_P0_COLB			Port0 MII Collision detect
	LETH0_P3_RXDG			LETH PortX TC14 interface receive data input
	EGTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	LETH0_P3_MII_RMII_RXD0A			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P3_RXCLKA or LETH0_P3_REFCLKA)
	LETH0_P3_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P3_RXCLKC or LETH0_P3_REFCLKC)

(table continues...)

Table 42 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P15.8	O0		General-purpose output
	—	O1		Reserved
	CAN43_TXD	O2		CAN transmit output node 3
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_SLSO11_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT79	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P3_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

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Table 43 Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B17	P16.0	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RGMII_GREFCLK			Port0 RGMII Gigabit Reference Clock input
	GETH0_P0_TXCLKC			Port0 Transmit Clock Input for MII
	LETH0_P0_TXCLKC			PortX MII transmit clock
	GETH0_P0_RXD1D			Port0 MII and RMII receive data bit 1 (to be used with GETH0_P0_RXCLKD or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD1D			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKD or LETH0_P0_REFCLKD)
	EGTM_TIM0_IN1_11			Mux input channel 1 of TIM module 0
	EGTM_TIM0_IN5_10			Mux input channel 5 of TIM module 0

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P16.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI1_SLSO3	O4		Master slave select output
	CAN13_TXD	O5		CAN transmit output node 3
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT121	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_CLKA_INV	O		Clock out inverted
A17	P16.1	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	QSPI7_SCLKB_F			Slave SPI clock inputs
	CAN13_RXDF			CAN receive input node 3
	GETH0_P0_RGMII_RCTL			Port0 RGMII Receive Control
	SCU_E_REQ1G			ERU channel 1 input G
	GETH0_P0_CRSDVC			Port0 RMII Carrier Sense and Receive Data Valid (P0_CRSDVC must only be used with P0_REFCLKD)
	GETH0_P0_RXDVC			Port0 MII Receive Data Valid
	LETH0_P0_MII_RXDVC			Receive data valid and Carrier sense and receive data valid
	LETH0_P0_RMII_CRSDVC			Receive data valid and Carrier sense and receive data valid
	P16.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN0_ATX_F	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT97	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_CLKA	O		Clock out
B16	P16.2	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RXCLKD			Port0 MII Receive Clock
	GETH0_P0_RGMII_RXCLK			Port0 RGMII Receive Clock
	GETH0_P0_REFCLKD			Port0 Reference Clock input for RMII
	LETH0_P0_REFCLKC			RMII Clock from PAD
	LETH0_P0_RXCLKC			LETH PortX MII receive clock
	LETH0_P0_REFCLKD			MII or RMII Clock from PAD
	LETH0_P0_RXCLKD			LETH PortX MII receive clock
	ASCLIN0_ARXG_F			Receive input
	EGTM_TIM1_IN6_8			Mux input channel 6 of TIM module 1
	EGTM_TIM1_IN7_7			Mux input channel 7 of TIM module 1
	XSPI0_RWDSA			Data strobe
	P16.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI7_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT96	O9		eGTM muxed output

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_DMA	O		Data mask
A16	P16.3	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RXD1B			Port0 MII and RMII receive data bit 1 (to be used with GETH0_P0_RXCLKB or GETH0_P0_REFCLKB)
	GETH0_P0_RGMII_RXD1			Port0 RGMII Receive data
	LETH0_P0_MII_RMII_RXD1C			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKC or LETH0_P0_REFCLKC)
	LETH0_P0_TXCLKD			PortX MII transmit clock
	EGTM_TIM0_IN7_9			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN5_9			Mux input channel 5 of TIM module 1
	XSPI0_RXD1A			Receive data
	P16.3	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	ASCLIN5_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT95	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	XSPI0_TXDA1	O		Transmit data
D15	P16.4	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	GETH0_P0_RXD0B			Port0 MII and RMII receive data bit 0 (to be used with GETH0_P0_RXCLKB or GETH0_P0_REFCLKB)
	GETH0_P0_RGMII_RXD0			Port0 RGMII Receive data
	QSPI3_MRSTF			Master SPI data input
	LETH0_P0_MII_RMII_RXD0C			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKC or LETH0_P0_REFCLKC)
	GETH0_P0_RXD0D			Port0 MII and RMII receive data bit 0 (to be used with GETH0_P0_RXCLKD or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD0D			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKD or LETH0_P0_REFCLKD)
	EGTM_TIM0_IN6_10			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN1_10			Mux input channel 1 of TIM module 1
	P16.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	QSPI7_SLSO8_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT120	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	QSPI3_SLSO14	O12		Master slave select output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_CSA1_N	O		Chip Select 1
B15	P16.5	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	ASCLIN5_ARXE			Receive input

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_RXD2B			Port0 MII receive data bit 2 (to be used with GETH0_P0_RXCLKB)
	GETH0_P0_RGMII_RXD2			Port0 RGMII Receive data
	GETH0_P0_RXD2D			Port0 MII receive data bit 2 (to be used with GETH0_P0_RXCLKD)
	LETH0_P0_MII_RXD2C			LETH PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD2D			LETH PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKD)
	EGTM_CDTM1_DTM0_1			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_1			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_1			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_1			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM1_IN0_11			Mux input channel 0 of TIM module 1
	EGTM_TIM1_IN4_10			Mux input channel 4 of TIM module 1
	XSPI0_RXD2A			Receive data
	P16.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	CAN20_TXD	O6		CAN transmit output node 0
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT119	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA2	O		Transmit data

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B13	P16.6	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN03_RXDG			CAN receive input node 3
	ASCLIN1_ARXH			Receive input
	QSPI7_SLSIA_F			Slave select input
	XSPI0_RXD3A			Receive data
	P16.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P0_MII_TXD0	O8		Port0 MII Transmit data (to be used with GETH0_P0_TXCLKC)
	EGTM_TOUT99	O9		eGTM muxed output
	GETH0_P0_RMIIC_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKC)
	LETH0_P0_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
	XSPI0_TXDA3	O		Transmit data
	GETH0_P0_RGMII_TXD0	O		Port0 RGMII Transmit data
A15	P16.7	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	QSPI7_MTSRB_F			Slave SPI data input
	GETH0_P0_RXD3B			Port0 MII receive data bit 3 (to be used with GETH0_P0_RXCLKB)
	GETH0_P0_RGMII_RXD3			Port0 RGMII Receive data
	GETH0_P0_RXD3D			Port0 MII receive data bit 3 (to be used with GETH0_P0_RXCLKD)

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD3D			LETH PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKD)
	XSPI0_RXD0A			Receive data
	P16.7	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT98	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA0	O		Transmit data
B14	P16.8	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN11_RXDE			CAN receive input node 1
	EGTM_TIM1_IN6_9			Mux input channel 6 of TIM module 1
	EGTM_TIM1_IN7_9			Mux input channel 7 of TIM module 1
	XSPI0_RXD4A			Receive data
	P16.8	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_MTSR_F	O6		Master SPI data output
	—	O7		Reserved
	GETH0_P0_MII_TXD1	O8		Port0 MII Transmit data
	EGTM_TOUT123	O9		eGTM muxed output
	GETH0_P0_RMIIC_TXD1	O10		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKC)
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDA4	O		Transmit data
	GETH0_P0_RGMII_TXD1	O		Port0 RGMII Transmit data
A12	P16.9	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN12_RXDE			CAN receive input node 2
	I2C0_SCLE			Serial Clock Input 4
	QSPI3_MRSTE			Master SPI data input
	EGTM_TIM1_IN7_8			Mux input channel 7 of TIM module 1
	XSPI0_RXD5A			Receive data
	P16.9	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	LETH0_P0_MIIC_TXD2	O5		LETH PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKC)
	QSPI7_SCLK_F	O6		Master SPI clock output
	LETH0_P0_MIID_TXD2	O7		LETH PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKD)
	GETH0_P0_MII_TXD2	O8		Port0 MII Transmit data
	EGTM_TOUT124	O9		eGTM muxed output

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_RMIIC_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKC)
	I2C0_SCL	O14		Serial Clock Output
	—	O15		Reserved
	XSPI0_TXDA5	O		Transmit data
	GETH0_P0_RGMII_TXD2	O		Port0 RGMII Transmit data
B12	P16.10	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	QSPI1_SLSIB			Slave select input
	I2C0_SDAE			Serial Data Input 4
	GETH0_P0_CRSDVB			Port0 RMII Carrier Sense and Receive Data Valid (P0_CRSDVB must only be used with P0_REFCLKB)
	GETH0_P0_RXDVB			Port0 MII Receive Data Valid
	GETH0_P0_CRSC			Port0 MII Carrier Sense
	LETH0_P0_MII_RXDVD			Receive data valid and Carrier sense and receive data valid
	LETH0_P0_RMII_CRSDVD			Receive data valid and Carrier sense and receive data valid
	XSPI0_RXD6A			Receive data
	P16.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI7_SLSO5_F	O6		Master slave select output
	LETH0_P0_MIIC_TXD3	O7		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKC)
	GETH0_P0_MII_TXD3	O8		Port0 MII Transmit data
	EGTM_TOUT129	O9		eGTM muxed output
	LETH0_P0_MIID_TXD3	O10		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKD)

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	QSPI3_MRST	O12		Slave SPI data output
	—	O13		Reserved
	I2C0_SDA	O14		Serial Data Output
	—	O15		Reserved
	XSPI0_TXDA6	O		Transmit data
	GETH0_P0_RGMII_TXD3	O		Port0 RGMII Transmit data
E13	P16.11	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	CAN30_RXDC			CAN receive input node 0
	LETH0_P0_MDIOD			LETH PortX MDIO interface data input
	I2C1_SDAE			Serial Data Input 4
	LETH0_P0_EDD			LETH PortX TC14 interface energy detection input
	QSPI3_MRSTD			Master SPI data input
	P16.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN0_ASLSO	O6		Slave select signal output
	GETH0_P0_MDC	O7		Port0 MDIO Clock
	GETH0_P1_MDC	O8		Port1 MDIO Clock
	EGTM_TOUT128	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	QSPI3_MTSR	O12		Master SPI data output
	—	O13		Reserved
	I2C1_SDA	O14		Serial Data Output
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
A11	P16.12	I	HSFAST / PU1 /	General-purpose input
	I2C2_SDAD			Serial Data Input 3

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_MRSTD_F		VDDHSIF / ES	Master SPI data input
	QSPI3_SLSID			Slave select input
	LETH0_P0_MII_RXERD			LETH PortX MII receive error (to be used with LETH0_P0_RXCLKD)
	EGTM_TIM1_IN5_10			Mux input channel 5 of TIM module 1
	XSPI0_RXD7A			Receive data
	P16.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	ASCLIN0_ASLSO	O6		Slave select signal output
	LETH0_P0_MIIC_TXER	O7		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKC)
	GETH0_P0_TXER	O8		Port0 MII Transmit Error
	EGTM_TOUT122	O9		eGTM muxed output
	LETH0_P0_MIID_TXER	O10		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKD)
	GETH0_P0_RMIIC_TXEN	O11		GETH PortX RMII transmit enable (to be used with GETH0_P0_REFCLKD)
	QSPI3_SLSO13	O12		Master slave select output
	—	O13		Reserved
	I2C2_SDA	O14		Serial Data Output
	—	O15		Reserved
	XSPI0_TXDA7	O		Transmit data
	GETH0_P0_RGMII_TXCLK	O		Port0 RGMII Transmit Clock Output
E15	P16.13	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	I2C2_SCLD			Serial Clock Input 3
	CAN20_RXDG			CAN receive input node 0
	QSPI3_MTSRE			Slave SPI data input
	EGTM_TIM1_IN1_11			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN4_11			Mux input channel 4 of TIM module 1
	P16.13	O0		General-purpose output

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH0_P0_MII_TXEN	O6		Port0 MII Transmit Enable
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT100	O9		eGTM muxed output
	GETH0_P0_RMIIC_TXEN	O10		GETH PortX RMII transmit enable (to be used with GETH0_P0_REFCLKD)
	LETH0_P0_MIIC_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKC)
	LETH0_P0_MIID_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKD)
	LETH0_P0_RMIIC_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P0_REFCLKC)
	I2C2_SCL	O14		Serial Clock Output
	—	O15		Reserved
	XSPI0_CSA0_N	O		Chip Select 0
	GETH0_P0_RGMII_TCTL	O		Port0 RGMII Transmit Control
E14	P16.14	I	HSFAST / PU1 / VDDHSIF / ES	General-purpose input
	I2C1_SCLE			Serial Clock Input 4
	GETH0_PX_MDIOB			PortX MDIO input
	QSPI3_SCLKD			Slave SPI clock inputs
	P16.14	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	EGTM_ECLK2	O4		CGM generated clock
	CAN03_TXD	O5		CAN transmit output node 3
	CLOCK_EXTCLK1	O6		External clock output 1
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 43 (continued) Port 16 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT101	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MDC	O11		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	QSPI3_SCLK	O12		Master SPI clock output
	—	O13		Reserved
	I2C1_SCL	O14		Serial Clock Output
	—	O15		Reserved
	GETH0_PX_MDIO1	O		PortX MDIO output

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Table 44 Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K19	P20.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN03_RXDC			CAN receive input node 3
	CAN21_RXDC			CAN receive input node 1
	CBS_TGI0			Trigger input
	SCU_E_REQ6A			ERU channel 6 input A
	GETH0_P1_RXERC			Port1 MII Receive Error
	SENT1_SENT1D			Receive input channel 1
	LETH0_P0_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	EGTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CLOCK_CLKA_SYSCLK			System clock input
	P20.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX_F	O2		Transmit output
	ASCLIN3_ASCLK_F	O3		Shift clock output
	SENT1_SPC1	O4		Transmit output
	—	O5		Reserved

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	—	O7		Reserved
	GETH0_P0_MII_TXD2	O8		Port0 MII Transmit data
	EGTM_TOUT59	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD2	O11		LETH PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_MDC	O12		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
	—	O13		Reserved
	—	O14		Reserved
	$\overline{\text{XSPI0\_CSB1\_N}}$	O15		chip select
	CBS_TGO0	O		Trigger output
	HSCT0_SYSCLK_OUT	O		sys clock output
F19	P20.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CBS_TGI1			Trigger input
	CAN40_RXDB			CAN receive input node 0
	GETH0_P0_CRSD			Port0 MII Carrier Sense
	EGTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	LETH0_P0_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	P20.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT60	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO1	O		Trigger output
F20	P20.2	I	S / PU / VDDEXT	General-purpose input
	$\overline{\text{TESTMODE}}$			Testmode Enable Input
	PMS_TESTMODEIN			TESTMODE pin input
E20	P20.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN3_ARXC_F			Receive input
	SENT0_SENT3D			Receive input channel 3
	EGTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	XSPI0_RXD0B			Receive data
	GETH0_P0_TXCLKD			Port0 Transmit Clock Input for MII
	LETH0_P0_TXCLKB			PortX MII transmit clock
	P20.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX_F	O2		Transmit output
	QSPI0_SLSO9_F	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	CAN21_TXD	O6		CAN transmit output node 1
	—	O7		Reserved
	SENT0_SPC3	O8		Transmit output
	EGTM_TOUT61	O9		eGTM muxed output
	LETH0_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	XSPI0_TXDB0	O		Transmit data
F17	P20.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	SENT1_SENT3D			Receive input channel 3
	CAN32_RXDB			CAN receive input node 2
	EGTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	XSPI0_RXD1B			Receive data
	P20.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8_F	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	GETH0_P0_TXER	O8		Port0 MII Transmit Error
	EGTM_TOUT62	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXER	O11		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O13		LETH PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB1	O		Transmit data
E19	P20.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	SDMMC0_DAT0_IN			Read data in

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SENT0D			Receive input channel 0
	EGTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	EGTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	P20.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	GETH0_P0_MII_TXD3	O8		Port0 MII Transmit data
	EGTM_TOUT63	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD3	O11		LETH PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT0	O		Write data out
D20	P20.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SDMMC0_DAT1_IN			Read data in
	LETH0_P0_CRSD			LETH PortX MII carrier sense
	EGTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GETH0_P0_RXDVD			Port0 MII Receive Data Valid
	GETH0_P0_CRSDVD			Port0 RMII Carrier Sense and Receive Data Valid (P0_CRSDVD must only be used with P0_REFCLKD)
	LETH0_P0_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P0_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	P20.8	O0		General-purpose output

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0_F	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT64	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT1	O		Write data out
E17	P20.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7A			ERU channel 7 input A
	ADC_TRIG62			Triggers from PORTS to ADC
	LETH0_P0_COLD			LETH PortX MII collision detection
	EGTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	XSPI0_RXD2B			Receive data
	P20.9	O0		General-purpose output
	—	O1		Reserved
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI0_SLSO1_F	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GETH0_P0_RMIIB_TXD1	O7		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P0_REFCLKB)
	GETH0_P0_MII_TXD1	O8		Port0 MII Transmit data
	EGTM_TOUT65	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O12		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB2	O		Transmit data
D19	P20.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	SDMMC0_DAT2_IN			Read data in
	EGTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI0_SLSO6_F	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	ASCLIN1_ASCLK	O6		Shift clock output
	GETH0_P0_RMIIB_TXD0	O7		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P0_REFCLKB)
	GETH0_P0_MII_TXD0	O8		Port0 MII Transmit data
	EGTM_TOUT66	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O12		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH0_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	SDMMC0_DAT2	O		Write data out
C20	P20.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SCLKA			Slave SPI clock inputs
	SDMMC0_DAT3_IN			Read data in
	ASCLIN18_ARXD			Receive input
	EGTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	GETH0_P0_RXD1C			Port0 MII and RMII receive data bit 1 (to be used with GETH0_P0_RXCLKC or GETH0_P0_REFCLKD)
	LETH0_P0_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	P20.11	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT67	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT3	O		Write data out
C19	P20.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MRSTA_F			Master SPI data input
	SDMMC0_DAT4_IN			Read data in
	EGTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	GETH0_P0_RXD0C			Port0 MII and RMII receive data bit 0 (to be used with GETH0_P0_RXCLKC or GETH0_P0_REFCLKD)

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MII_RMII_RXD0B			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	P20.12	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_MRST	O3		Slave SPI data output
	QSPI0_MTSR_F	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT68	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SDMMC0_DAT4	O		Write data out
B20	P20.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_SLSIA			Slave select input
	SDMMC0_DAT5_IN			Read data in
	ASCLIN9_ARXH			Receive input
	ASCLIN18_ARXE			Receive input
	GETH0_P0_RXD2C			Port0 MII receive data bit 2 (to be used with GETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD2B			LETH PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	P20.13	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_SLSO2_F	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI0_SCLK_F	O5		Master SPI clock output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT69	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CLKB	O15		clock output
	SDMMC0_DAT5	O		Write data out
A18	P20.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI0_MTSRA			Slave SPI data input
	SDMMC0_DAT6_IN			Read data in
	ASCLIN27_ARXB_F			Receive input
	QSPI4_MRSTH			Master SPI data input
	GETH0_P0_RXD3C			Port0 MII receive data bit 3 (to be used with GETH0_P0_RXCLKC)
	LETH0_P0_MII_RXD3B			LETH PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKB)
	EGTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	P20.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI0_MTSR_F	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT70	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 44 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSB0_N	O15		chip select
	SDMMC0_DAT6	O		Write data out

3.3.11 BGA292_COM port 21

Table 45 Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
M16	P21.0	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI4_MRSTDN_F			Master SPI data input (LVDS N line)
	DMU_FDEST			FDEST for NVM
	ASCLIN11_ARXC_F			Receive input
	HSCT1_RXDN			Rx data
	QSPI0_SCLKEN			Slave SPI clock inputs (LVDS N line)
	QSPI4_MRSTE			Master SPI data input
	ASCLIN17_ARXB			Receive input
	ASCLIN18_ARXF			Receive input
	EGTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI0_SCLKD			Slave SPI clock inputs
	P21.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ATX_F	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT51	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	CSCU_CSRM1	O		Pin Output Value
L16	P21.1	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI4_MRSTDP_F			Master SPI data input (LVDS P line)
	ASCLIN11_ARXD_F			Receive input
	HSCT1_RXDP			Rx data
	QSPI0_SCLKEP			Slave SPI clock inputs (LVDS P line)
	ASCLIN18_ARXA_F			Receive input
	EGTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPI0_SCLKF			Slave SPI clock inputs
	P21.1	O0		General-purpose output
	—	O1		Reserved
	CAN40_TXD	O2		CAN transmit output node 0
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT52	O9		eGTM muxed output
	LETH0_P0_MIIB_TXER	O10		LETH PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O12		LETH PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CSCU_CSRM2	O		Pin Output Value
M17	P21.2	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SMU_EXT_EMERGENCYSTOP_REQ			Emergency Stop External Request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN_F			Master SPI data input (LVDS N line)
	ASCLIN11_ARXE_F			Receive input
	QSPI0_MTSRDN			Slave SPI data input (LVDS N line)
	SENT0_SENT2D			Receive input channel 2
	EGTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	QSPI0_MTSRE			Slave SPI data input
	QSPI4_MTSRC			Slave SPI data input
	ASCLIN18_ARXG			Receive input
	P21.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC2	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	GETH0_P1_MDC	O7		Port1 MDIO Clock
	GETH0_P0_MDC	O8		Port0 MDIO Clock
	EGTM_TOUT53	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
L17	P21.3	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP_F			Master SPI data input (LVDS P line)
	GETH0_PX_MDIOD			PortX MDIO input
	QSPI0_MTSRDP			Slave SPI data input (LVDS P line)
	SENT1_SENT2D			Receive input channel 2
	EGTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	QSPI0_MTSRF			Slave SPI data input
	P21.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ASCLK_F	O2		Shift clock output
	ASCLIN18_ATX_F	O3		Transmit output
	SENT1_SPC2	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT54	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	GETH0_PX_MDIO3	O		PortX MDIO output
K17	P21.4	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	SENT0_SENT0D			Receive input channel 0
	ASCLIN18_ARXB_F			Receive input
	EGTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GETH0_P0_REFCLKB			Port0 Reference Clock input for RMII
	GETH0_P0_RXCLKB			Port0 MII Receive Clock
	LETH0_P0_REFCLKB			RMII Clock from PAD
	LETH0_P0_RXCLKB			LETH PortX MII receive clock
	P21.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN11_ASLSO_F	O2		Slave select signal output
	ASCLIN18_ATX_F	O3		Transmit output
	SENT0_SPC0	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTN	O8		Slave SPI inverted data output
	EGTM_TOUT55	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDN	O		Tx data
J17	P21.5	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	ASCLIN11_ARXF_F			Receive input
	SENT0_SENT1D			Receive input channel 1
	ASCLIN18_ARXC_F			Receive input
	EGTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	P21.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX_F	O3		Transmit output
	SENT0_SPC1	O4		Transmit output

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTP	O8		Slave SPI data output
	EGTM_TOUT56	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXEN	O11		LETH PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	GETH0_P0_MII_TXEN	O12		Port0 MII Transmit Enable
	GETH0_P0_RMIIB_TXEN	O13		GETH PortX RMII transmit enable (to be used with GETH0_P0_REFCLKB)
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDP	O		Tx data
H17	P21.6	I	FAST / PD3 / PU2 / VDDEXT / ES	General-purpose input
	CAN33_RXDB			CAN receive input node 3
	ASCLIN3_ARXF_F			Receive input
	CBS_TGI2			Trigger input
	TDI			PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	QSPI0_SLSIC			Slave select input
	GETH0_P0_COLC			Port0 MII Collision detect
	LETH0_P0_COLC			LETH PortX MII collision detection
	EGTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	P21.6	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT57	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO2	O		Trigger output
	DAP3	I/O		DAP:DAP3 Data I/O
	DAPE1	I/O		DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)
H16	P21.7	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	CBS_TGI3			Trigger input
	GETH0_P0_RXERB			Port0 MII Receive Error
	LETH0_P0_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P0_RXCLKC)
	EGTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	P21.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	ASCLIN3_ASCLK	O3		Shift clock output
	CAN33_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT58	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 45 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP:DAP2 Data I/O
	DAPE2	I/O		DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
	TDO	O		JTAG Module Data Output

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Table 46 Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
N17	P22.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	QSPI5_MRSTC			Master SPI data input
	LETH0_P1_MII_RXDVB			Receive data valid and Carrier sense and receive data valid
	GETH0_P1_CRSDVB			Port1 RMII Carrier Sense and Receive Data Valid (P1_CRSDVB must only be used with P1_REFCLKB)
	GETH0_P1_RXDVB			Port1 MII Receive Data Valid
	GETH0_P1_CRSB			Port1 MII Carrier Sense
	LETH0_P1_RMII_CRSDVB			Receive data valid and Carrier sense and receive data valid
	LETH0_P1_CRSB			LETH PortX MII carrier sense
	EGTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	P22.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR_F	O3		Master SPI data output
	QSPI4_SCLKN_F	O4		Master SPI clock output (LVDS N line)
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output

(table continues...)

Table 46 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT47	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N16	P22.1	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_MRSTB_F			Master SPI data input
	ASCLIN7_ARXE			Receive input
	GETH0_P0_RXERD			Port0 MII Receive Error
	GETH0_P1_RXERA			Port1 MII Receive Error
	LETH0_P1_MII_RXERA			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GETH0_P1_REFCLKB			Port1 RMII Reference Clock input
	GETH0_P1_RXCLKB			Port1 MII Receive Clock
	LETH0_P1_REFCLKB			RMII Clock from PAD
	LETH0_P1_RXCLKB			LETH PortX MII receive clock
	P22.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST	O3		Slave SPI data output
	QSPI4_SCLKP_F	O4		Master SPI clock output (LVDS P line)
	—	O5		Reserved
	QSPI5_SLSO9	O6		Master slave select output
	ASCLIN7_ATX	O7		Transmit output
	QSPI4_SLSO9	O8		Master slave select output
	EGTM_TOUT48	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 46 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P17	P22.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_SLSIB			Slave select input
	CAN41_RXDA			CAN receive input node 1
	GETH0_P1_COLA			Port1 MII Collision detect
	LETH0_P1_COLA			LETH PortX MII collision detection
	LETH0_P1_MII_RXERC			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	P22.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3	O3		Master slave select output
	QSPI4_MTSRN_F	O4		Master SPI data output (LVDS N line)
	—	O5		Reserved
	QSPI5_MTSR	O6		Master SPI data output
	QSPI4_MTSR_F	O7		Master SPI data output
	GETH0_P1_MII_TXEN	O8		Port1 MII Transmit Enable
	EGTM_TOUT49	O9		eGTM muxed output
	GETH0_P1_RMIIA_TXEN	O10		GETH PortX RMII transmit enable (to be used with GETH0_P1_REFCLKA)
	GETH0_P1_RMIIB_TXEN	O11		GETH PortX RMII transmit enable (to be used with GETH0_P1_REFCLKB)
	LETH0_P1_MIIA_TXEN	O12		LETH PortX MII transmit enable (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXEN	O13		LETH PortX MII transmit enable (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXEN	O14		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXEN	O15		LETH PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB)

(table continues...)

Table 46 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	HSCT1_TXDN	O		Tx data
P16	P22.3	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	QSPI4_SCLKB			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	GETH0_P1_COLB			Port1 MII Collision detect
	GETH0_P1_RXD0B			Port1 MII and RMII receive data bit 0 (to be used with GETH0_P1_RXCLKB or GETH0_P1_REFCLKB)
	LETH0_P1_COLC			LETH PortX MII collision detection
	LETH0_P1_MII_RMII_RXD0B			LETH PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GETH0_P1_REFCLKC			Port1 RMII Reference Clock input
	GETH0_P1_RXCLKC			Port1 MII Receive Clock
	LETH0_P1_REFCLKC			RMII Clock from PAD
	LETH0_P1_RXCLKC			LETH PortX MII receive clock
	P22.3	O0		General-purpose output
	—	O1		Reserved
	QSPI5_SCLK	O2		Master SPI clock output
	QSPI4_SCLK_F	O3		Master SPI clock output
	QSPI4_MTSRP_F	O4		Master SPI data output (LVDS P line)
	—	O5		Reserved
	CAN41_TXD	O6		CAN transmit output node 1
	ASCLIN7_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT50	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT1_TXDP	O		Tx data

3.3.13 BGA292_COM port 23

Table 47 Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
T17	P23.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN6_ARXF_F			Receive input
	SCU_E_REQ6F			ERU channel 6 input F
	PCIE0_PERSTA_N			PERST# input
	ADC_TRIG61			Triggers from PORTS to ADC
	QSPI0_MRSTD			Master SPI data input
	LETH0_P1_RXDG			LETH PortX TC14 interface receive data input
	GETH0_P1_RXD1B			Port1 MII and RMII receive data bit 1 (to be used with GETH0_P1_RXCLKB or GETH0_P1_REFCLKB)
	LETH0_P1_MII_RMII_RXD1B			LETH PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	P23.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6	O3		Master slave select output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	CLOCK_EXTCLK0	O6		External clock output 0
	ASCLIN6_ASCLK_F	O7		Shift clock output
	QSPI6_MTSR_F	O8		Master SPI data output
	EGTM_TOUT42	O9		eGTM muxed output
	EGTM_ECLK0	O10		CGM generated clock
	ASCLIN16_ATX_F	O11		Transmit output
	QSPI6_SCLK_F	O12		Master SPI clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
R17	P23.4	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 47 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN27_ARXA_F		VDDEXT / ES	Receive input
	PCIE0_WAKE_INA_N			WAKE# input
	QSPI6_MRSTD_F			Master SPI data input
	EGTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	P23.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ASLSO_F	O2		Slave select signal output
	QSPI4_SLSO5_F	O3		Master slave select output
	GETH0_P1_MII_TXD1	O4		Port1 MII Transmit data
	—	O5		Reserved
	ASCLIN27_ATX_F	O6		Transmit output
	GETH0_P1_RMIIA_TXD1	O7		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P1_REFCLKA)
	QSPI6_SLSO1_F	O8		Master slave select output
	EGTM_TOUT45	O9		eGTM muxed output
	GETH0_P1_RMIIB_TXD1	O10		GETH PortX RMII transmit data bit 1 (to be used with GETH0_P1_REFCLKB)
	LETH0_P1_MIIA_TXD1	O11		LETH PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD1	O12		LETH PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXD1	O13		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXD1	O14		LETH PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB)
	QSPI6_MTSR_F	O15		Master SPI data output
	PCIE0_WAKE_N	O		WAKE# output
R16	P23.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	ASCLIN16_ARXA_F			Receive input
	PCIE0_CLKREQ_INA_N			CLKREQ# input
	GETH0_P1_RXD3C			Port1 MII receive data bit 3 (to be used with GETH0_P1_RXCLKC)
	LETH0_P1_MII_RXD3C			LETH PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKC)

(table continues...)

Table 47 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	P23.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX_F	O2		Transmit output
	QSPI4_SLSO4_F	O3		Master slave select output
	GETH0_P1_MII_TXD0	O4		Port1 MII Transmit data
	—	O5		Reserved
	CAN22_TXD	O6		CAN transmit output node 2
	GETH0_P1_RMIIA_TXD0	O7		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P1_REFCLKA)
	QSPI6_SLSO2_F	O8		Master slave select output
	EGTM_TOUT46	O9		eGTM muxed output
	GETH0_P1_RMIIB_TXD0	O10		GETH PortX RMII transmit data bit 0 (to be used with GETH0_P1_REFCLKB)
	LETH0_P1_MIIA_TXD0	O11		LETH PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKA)
	LETH0_P1_MIIB_TXD0	O12		LETH PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_RMIIA_TXD0	O13		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RMIIB_TXD0	O14		LETH PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output
	$\overline{\text{PCIE0\_CLKREQ\_N}}$	O		CLKREQ# output

3.3.14 BGA292_COM port 32

Table 48 Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
W18	P32.2	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input
	CAN21_RXDD			CAN receive input node 1

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SMU_FSPIN2			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	UART_RXDH	I#		Receive input H
	WCAN_RXDF			Wake-up input F
	T0D			T0 capture input D
	T21EXG			T21 interrupt input G
	EXINT7			Interrupt 7 input
	P32.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT38	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP2	O		FSP Output Signal - Generated by SMU
W17	P32.4	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	ASCLIN1_ACTSB			Clear to send input
	ASCLIN15_ARXA_F			Receive input
	I2C0_SCLD			Serial Clock Input 3
	EGTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	SSC_MRSTD	I#		Master SPI data input D
	T21EXA			T21 interrupt input A
	T2CCU1_0A			T2 capture 1 input 0A
	EXINT8A			Interrupt 8 input A
	EXINT12A			Interrupt 12 input A
	I2CSCLA			Serial clock input A
	P32.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	CAN03_TXD	O3		CAN transmit output node 3
	—	O4		Reserved
	—	O5		Reserved
	CLOCK_EXTCLK1	O6		External clock output 1
	CAN21_TXD	O7		CAN transmit output node 1
	I2C0_SCL	O8		Serial Clock Output
	EGTM_TOUT40	O9		eGTM muxed output
	EGTM_ECLK1	O10		CGM generated clock
	—	O11		Reserved
	ASCLIN25_ATX_F	O12		Transmit output

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.1	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_0	O#6		T2 PWM channel 10
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DCDCSYNCO	O		DC-DC synchronization output
T15	P32.5	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	SENT0_SENT5C			Receive input channel 5
	ASCLIN17_ARXF			Receive input
	SMU_FSPIN3			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	SSC_MTSRD	I#		Slave SPI data input D
	PINRSTC			Reset input C
	T20EXO			T20 interrupt input O
	T2CCU1_1A			T2 capture 1 input 1A
	EXINT9A			Interrupt 9 input A
	EXINT13A			Interrupt 13 input A
	P32.5	O0		General-purpose output

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	SENT0_SPC5	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT140	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP3	O		FSP Output Signal - Generated by SMU

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U15	P32.6	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT1_SENT5C			Receive input channel 5
	I2C0_SDAD			Serial Data Input 3
	UART_RXDI	I#		Receive input I
	T1D			T1 capture input D
	T21A			T21 capture input A
	T2CCU1_2A			T2 capture 1 input 2A
	EXINT10A			Interrupt 10 input A
	EXINT14A			Interrupt 14 input A
	I2CSDAA			Serial data input A
	P32.6	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	SENT1_SPC5	O3		Transmit output
	ASCLIN17_ATX	O4		Transmit output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	I2C0_SDA	O8		Serial Data Output
	EGTM_TOUT141	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_PPS	O12		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO4	O		Trigger output
U16	P32.7	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CBS_TGI5			Trigger input
	CAN22_RXDB			CAN receive input node 2
	SENT0_SENT6C			Receive input channel 6
	ASCLIN15_ARXB_F			Receive input
	GETH0_P1_COLC			Port1 MII Collision detect
	GETH0_P1_RXERB			Port1 MII Receive Error
	LETH0_P1_MII_RXERB			LETH PortX MII receive error (to be used with LETH0_P1_RXCLKB)
	WCAN_RXDH	I#		Wake-up input H
	T20EXH			T20 interrupt input H
	T2CCU1_3A			T2 capture 1 input 3A
	EXINT11A			Interrupt 11 input A
	EXINT15A			Interrupt 15 input A
	P32.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN6_ATX	O2		Transmit output
	SENT0_SPC6	O3		Transmit output

(table continues...)

Table 48 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN15_ATX_F	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT142	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_3	O#6		T2 PWM channel 13
	PMSRTC32_OUT	O#7		RTC oscillator output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO5	O		Trigger output

3.3.15 BGA292_COM port 33

Table 49 Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
W10	P33.0	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT9B			Receive input channel 9
	EGTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_3			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_3			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	T21EXB	I#		T20 interrupt input B
	T2CCU0_0A			T2 capture 0 input 0A
	EXINT3A			Interrupt 3 input A
	EXINT12B			Interrupt 12 input B
	ADCOMPCH0			Analog input channel 0
	P33.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ATX_F	O2		Transmit output
	SENT1_SPC9	O3		Transmit output
	ASCLIN15_ATX_F	O4		Transmit output
	ADC_EMUXCTRL03	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT22	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y10	P33.1	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5_RX0C			RXD inputs (receive data) channel 0
	SENT0_SENT9B			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	EGTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	UART_RXDK	I#		Receive input K
	SSC_SCLKD			Slave SPI clock input D
	T0A			T0 capture input A
	T20EXA			T2 interrupt input A
	T2CCU0_1A			T2 capture 0 input 1A
	EXINT4A			Interrupt 4 input A
	EXINT13B			Interrupt 13 input B
	ADCOMPCH1			Analog input channel 1
	P33.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	SENT0_SPC9	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT23	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.1	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W11	P33.2	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT8B			Receive input channel 8
	ASCLIN14_ARXC_F			Receive input
	EGTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	WCAN_RXDE	I#		Wake-up input E
	DAP0_1			DAP0 input

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T21B			T21 capture input B
	T2CCU0_2A			T2 capture 0 input 2A
	EXINT5A			Interrupt 5 input A
	EXINT14B			Interrupt 14 input B
	ADCOMPCH2			Analog input channel 2
	P33.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN14_ATX_F	O7		Transmit output
	SENT1_SPC8	O8		Transmit output
	EGTM_TOUT24	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y11	P33.3	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT0_SENT8B			Receive input channel 8
	ASCLIN14_ARXA_F			Receive input
	EGTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	UART_RXDP	I#		Receive input P
	T20A			T20 capture input A
	T2CCU0_3A			T2 capture 0 input 3A
	EXINT6A			Interrupt 6 input A
	EXINT15B			Interrupt 15 input B
	ADCOMPCH3			Analog input channel 3
	P33.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN5_ASCLK_F	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN14_ATX_F	O7		Transmit output
	SENT0_SPC8	O8		Transmit output
	EGTM_TOUT25	O9		eGTM muxed output
	ASCLIN8_ATX	O10		Transmit output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.3	O#0		General-purpose output

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	DAP1_1	I/O		DAP1 input
	SPD_1	I/O		Single pin DAP1
W12	P33.4	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT1_SENT7B			Receive input channel 7
	ASCLIN5_ARXB_F			Receive input
	ASCLIN14_ARXB_F			Receive input
	ASCLIN25_ARXA_F			Receive input
	EGTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_1			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_1			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	UART_RXDC	I#		Receive input C
	WCAN_RXDP			Wake-up input P
	T1B			T1 capture input B
	T2CCU0_3D			T2 capture 0 input 3D
	EXINT0A			Interrupt 0 input A

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT6D			Interrupt 6 input D
	EXINT12C			Interrupt 12 input C
	ADCOMPCH4			Analog input channel 4
	P33.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	CAN13_TXD	O7		CAN transmit output node 3
	SENT1_SPC7	O8		Transmit output
	EGTM_TOUT26	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN25_ATX_F	O12		Transmit output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.4	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#14		Reserved
	—	O#15		Reserved
Y12	P33.5	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	PSI5S0_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	SENT1_SENT2C			Receive input channel 2
	CAN13_RXDB			CAN receive input node 3
	QSPI4_MRSTG			Master SPI data input
	EGTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	WCAN_RXDD	I#		Wake-up input D
	SSC_MRSTA			Master SPI data input A
	T0B			T0 capture input B
	T20EXB			T20 interrupt input B
	EXINT1A			Interrupt 1 input A
	EXINT13C			Interrupt 13 input C
	ADCOMPCH5			Analog input channel 5
	P33.5	O0		General-purpose output
	—	O1		Reserved
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	ASCLIN5_ASLSO_F	O7		Slave select signal output
	—	O8		Reserved
	EGTM_TOUT27	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P0.5	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W13	P33.6	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT0_SENT12B			Receive input channel 12
	ASCLIN8_ARXD			Receive input
	EGTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_2			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_2			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	UART_RXDL	I#		Receive input L
	SSC_MTSRA			Slave SPI data input A
	DAP0_0			DAP0 input
	T2CCU1_0B			T2 capture 1 input 0B
	EXINT2A			Interrupt 2 input A
	EXINT8B			Interrupt 8 input B
	ADCOMPCH6			Analog input channel 6
	P33.6	O0		General-purpose output

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	PSI5S0_TX	O7		TX data output
	SENT0_SPC12	O8		Transmit output
	EGTM_TOUT28	O9		eGTM muxed output
	QSPI4_MTSR	O10		Master SPI data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.6	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	SSC_MTSR	O#2		Master SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y13	P33.7	I	SLOW / PU1 /	General-purpose input
	CAN00_RXDE			CAN receive input node 0

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PSI5S0_RXD		VDDEVRSB / ES5	RX data input
	SCU_E_REQ4A			ERU channel 4 input A
	SENT1_SENT11B			Receive input channel 11
	ADC_TRIG60			Triggers from PORTS to ADC
	EGTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	WCAN_RXDB	I#		Wake-up input B
	SSC_SCLKA			Slave SPI clock input A
	T20B			T20 capture input B
	T21EXH			T21 interrupt input H
	T2CCU1_1B			T2 capture 1 input 1B
	EXINT0B			Interrupt 0 input B
	EXINT9B			Interrupt 9 input B
	ADCOMPCH7			Analog input channel 7
	P33.7	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	ADC_EMUXCTRL13	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	QSPI5_SLSO10	O7		Master slave select output
	SENT1_SPC11	O8		Transmit output
	EGTM_TOUT29	O9		eGTM muxed output
	QSPI4_SCLK	O10		Master SPI clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.7	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	DAP1_0	I/O		DAP1 input
	SPD_0	I/O		Single pin DAP0
W14	P33.8	I	FAST / HighZ / VDDEVRSB	General-purpose input
	ASCLIN2_ARXE			Receive input
	SMU_FSPIN0			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	UART_RXDF	I#		Receive input F
	WCAN_RXDO			Wake-up input O
	T21EXN			T21 interrupt input N
	T2CCU1_3D			T2 capture 1 input 3D
	EXINT1B			Interrupt 1 input B
	EXINT11D			Interrupt 11 input D
	I2CSDAD			Serial clock input D
	P33.8	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	QSPI5_SLSO11_F	O7		Master slave select output
	QSPI6_SLSO13	O8		Master slave select output
	EGTM_TOUT30	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.0	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP0	O		FSP Output Signal - Generated by SMU
Y14	P33.9	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	XTAL3			XTAL3.RTC Oscillator
	EGTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	T1A	I#		T1 capture input A
	T20EXC			T2 interrupt input C

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU0_0B			T2 capture 0 input 0B
	EXINT3B			Interrupt 3 input B
	EXINT14C			Interrupt 14 input C
	I2CSCLD			Serial clock input D
	P33.9	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO1	O3		Master slave select output
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ATX	O6		Transmit output
	QSPI5_SLSO12	O7		Master slave select output
	QSPI6_SLSO10	O8		Master slave select output
	EGTM_TOUT31	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.1	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	—	O#6		Reserved
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W15	P33.10	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	EGTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	UART_RXDA	I#		Receive input A
	WCAN_RXDA			Wake-up input A
	RTC32_IN			RTC oscillator input
	T20EXP			T20 interrupt input P
	T21CLK32K			T21 external input
	EXINT2B			Interrupt 2 input B
	EXINT15C			Interrupt 15 input C
	P33.10	O0		General-purpose output
	—	O1		Reserved
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S0_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	QSPI5_SLSO13	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT32	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P1.2	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	XTAL4	O		XTAL4. RTC Oscillator
Y15	P33.11	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_SCLKA			Slave SPI clock inputs
	SMM_ESR2_PORT_IN			ESR2 pad data from bitslice
	QSPI5_SCLKF			Slave SPI clock inputs
	EGTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	PMS_ESR2WKP			ESR2 pin input
	SSC_SCLKB	I#		Slave SPI clock input B
	PINRSTA			Reset input A
	T20C			T20 capture input C
	T2CCU0_1B			T2 capture 0 input 1B
	T2CCU1_2B			T2 capture 1 input 2B
	EXINT4B			Interrupt 4 input B
	EXINT10B			Interrupt 10 input B
	P33.11	O0		General-purpose output
	—	O1		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT33	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	PMS_RTCOUT	O12		RTC output for P33.11
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.3	O#0		General-purpose output
	—	O#1		Reserved
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_2	O#6		T2 PWM channel 12
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_ESR2PORST	O		ESR2 reset output. For details please refer to the PMS/SMM chapter.

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
W16	P33.12	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	SMU_FSPIN1			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	PMS_PINCWKP			PINC (P33.12) pin input
	UART_RXDG	I#		Receive input G
	WCAN_RXDG			Wake-up input G
	SSC_MTSRB			Slave SPI data input B
	T1C			T1 capture input C
	T21C			T21 capture input C
	T2CCU0_2B			T2 capture 0 input 2B
	T2CCU1_3B			T2 capture 1 input 3B
	EXINT5B			Interrupt 5 input B
	EXINT11B			Interrupt 11 input B
	P33.12	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	QSPI5_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT34	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_3	O#6		T2 PWM channel 13
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP1	O		FSP Output Signal - Generated by SMU
Y16	P33.13	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	ASCLIN1_ARXF			Receive input
	QSPI4_MRSTA			Master SPI data input
	CAN22_RXDA			CAN receive input node 2
	QSPI5_MRSTD_F			Master SPI data input
	ASCLIN16_ARXF			Receive input
	EGTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	PMS_PINBWKP			PINB (P33.13) pin input
	UART_RXDB	I#		Receive input B
	WCAN_RXDC			Wake-up input C
	SSC_MRSTB			Master SPI data input B
	T0C			T0 capture input C
	T20EXD			T20 interrupt input D
	T2CCU0_3B			T2 capture 0 input 3B
	EXINT0C			Interrupt 0 input C
	EXINT6B			Interrupt 6 input B
	ADCOMPCH8			Analog input channel 8
	P33.13	O0		General-purpose output

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MRST	O3		Slave SPI data output
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT35	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.5	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
T14	P33.14	I	FAST / PU1 /	General-purpose input
	QSPI2_SCLKD			Slave SPI clock inputs

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CBS_TGI6		VDDEVRSB / ES5	Trigger input
	CAN31_RXDB			CAN receive input node 1
	QSPI5_MRSTF			Master SPI data input
	EGTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	SSC_SCLKC	I#		Slave SPI clock input C
	EXTNMI			NMI input
	T21EXC			T21 interrupt input C
	EXINT1C			Interrupt 1 input C
	ADCOMPCH9			Analog input channel 9
	P33.14	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_MRST	O7		Slave SPI data output
	—	O8		Reserved
	EGTM_TOUT143	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.6	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO6	O		Trigger output
U14	P33.15	I	FAST / PU1 / VDDEVRSB / ES5	General-purpose input
	CBS_TGI7			Trigger input
	QSPI5_SLSIB			Slave select input
	ASCLIN15_ARXC			Receive input
	SENT1_SENT14D			Receive input channel 14
	QSPI4_MTSRD			Slave SPI data input
	EGTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	UART_RXDE	I#		Receive input E
	PINRSTB			Reset input B
	T20EXE			T20 interrupt input E
	T2CCU0_0C			T2 capture 0 input 0C
	T2CCU1_0C			T2 capture 1 input 0C
	EXINT2C			Interrupt 2 input C
	EXINT3C			Interrupt 3 input C
	EXINT8C			Interrupt 8 input C
	ADCOMPCH10			Analog input channel 10
	P33.15	O0		General-purpose output
	—	O1		Reserved
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 49 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SPC14	O8		Transmit output
	EGTM_TOUT144	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.7	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO7	O		Trigger output

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Table 50 Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U11	P34.1	I	SLOW / PU1 / VDDEVRSB / ES5	General-purpose input
	SENT0_SENT12D			Receive input channel 12
	$\overline{\text{PCIE0\_PERSTB\_N}}$			PERST# input

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN25_ARXB_F			Receive input
	EGTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	UART_RXDD	I#		Receive input D
	T21EXD			T21 interrupt input D
	T2CCU0_1C			T2 capture 0 input 1C
	T2CCU1_1C			T2 capture 1 input 1C
	EXINT4C			Interrupt 4 input C
	EXINT9C			Interrupt 9 input C
	ADCOMPCH11			Analog input channel 11
	P34.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	SENT0_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT146	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.0	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG0	O		PMS debugging power mode K
T12	P34.2	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	CAN20_RXDC			CAN receive input node 0
	SENT0_SENT14B			Receive input channel 14
	I2C1_SDAD			Serial Data Input 3
	EGTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	WCAN_RXDI	I#		Wake-up input I
	T20EXF			T20 interrupt input F
	T2CCU0_2C			T2 capture 0 input 2C
	EXINT5C			Interrupt 5 input C
	ADCOMPCH12			Analog input channel 12
	I2CSDAB			Serial data input B
	P34.2	O0		General-purpose output
	—	O1		Reserved
	ASCLIN16_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT147	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.1	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG1	O		PMS debugging power mode K
U12	P34.3	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	CAN43_RXDA			CAN receive input node 3
	ASCLIN4_ARXE			Receive input
	SENT1_SENT14B			Receive input channel 14
	I2C1_SCLD			Serial Clock Input 3
	EGTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	PINRSTD	I#		Reset input D
	T21EXE			T21 interrupt input E
	T2CCU0_3C			T2 capture 0 input 3C
	EXINT0D			Interrupt 0 input D
	EXINT6C			Interrupt 6 input C

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADCOMPCH13			Analog input channel 13
	I2CSCLB			Serial clock input B
	P34.3	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN4_ATX	O3		Transmit output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output
	EGTM_TOUT148	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.2	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_3	O#6		T2 PWM channel 13
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
	PMS_DEBUG2	O		PMS debugging power mode K
T13	P34.4	I	SLOW / PU1 / VDDEVRSB / ES	General-purpose input
	QSPI2_MRSTD			Master SPI data input
	SENT1_SENT13B			Receive input channel 13
	ASCLIN16_ARXE			Receive input
	PCIE0_CLKREQ_INB_N			CLKREQ# input
	EGTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	UART_RXDJ	I#		Receive input J
	SSC_MRSTC			Master SPI data input C
	T20EXG			T20 interrupt input P
	T2CCU1_2C			T2 capture 1 input 2C
	EXINT1D			Interrupt 1 input D
	EXINT10C			Interrupt 10 input C
	ADCOMPCH14			Analog input channel 14
	P34.4	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT149	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional Receive pin O

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	$\overline{\text{PCIE0\_CLKREQ\_N}}$	O		CLKREQ# output
	PMS_DEBUG3	O		PMS debugging power mode K
U13	P34.5	I	FAST / PU1 / VDDEVRSB / ES	General-purpose input
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	QSPI4_MRSTF			Master SPI data input
	SENT0_SENT13C			Receive input channel 13
	$\overline{\text{PCIE0\_WAKE\_INB\_N}}$			WAKE# input
	EGTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	WCAN_RXDJ	I#		Wake-up input J
	SSC_MTSRC			Slave SPI data input C
	T21EXF			T21 interrupt input F
	T2CCU1_3C			T2 capture 1 input 3C
	EXINT2D			Interrupt 2 input D
	EXINT11C			Interrupt 11 input C
	ADCOMPCH15			Analog input channel 15
	P34.5	O0		General-purpose output
	—	O1		Reserved
	ASCLIN8_ATX	O2		Transmit output

(table continues...)

Table 50 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN43_TXD	O3		CAN transmit output node 3
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	SENT0_SPC13	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT150	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	$\overline{\text{PCIE0\_WAKE\_N}}$	O		WAKE# output
	PMS_DEBUG4	O		PMS debugging power mode K

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Table 51 Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
T10	AN0	I	D / HighZ / VDDM	Analog Input 0
	ADC_TMADC0CH0			Analog Input for TMADC0 Channel 0
U10	AN1	I	D / HighZ / VDDM	Analog Input 1
	ADC_TMADC0CH1			Analog Input for TMADC0 Channel 1
W9	AN2	I	D / HighZ / VDDM	Analog Input 2
	ADC_TMADC0CH2			Analog Input for TMADC0 Channel 2
U9	AN3	I	D / HighZ / VDDM	Analog Input 3
	ADC_TMADC0CH3			Analog Input for TMADC0 Channel 3
T9	AN4	I	D / HighZ / VDDM	Analog Input 4
	ADC_TMADC0CH4			Analog Input for TMADC0 Channel 4
	ADC_TMADC1CH0			Analog Input for TMADC1 Channel 0
Y9	AN5	I	D / HighZ / VDDM	Analog Input 5
	ADC_TMADC0CH5			Analog Input for TMADC0 Channel 5
	ADC_TMADC1CH1			Analog Input for TMADC1 Channel 1
T8	AN6	I	D / HighZ / VDDM	Analog Input 6
	ADC_TMADC0CH6			Analog Input for TMADC0 Channel 6
	ADC_TMADC1CH2			Analog Input for TMADC1 Channel 2
U8	AN7	I	D / HighZ / VDDM	Analog Input 7
	ADC_TMADC0CH7			Analog Input for TMADC0 Channel 7
	ADC_TMADC1CH3			Analog Input for TMADC1 Channel 3
W8	AN8	I	D / HighZ / VDDM	Analog Input 8
	ADC_TMADC0CH8			Analog Input for TMADC0 Channel 8
U7	AN9	I	D / HighZ / VDDM	Analog Input 9
	ADC_TMADC0CH9			Analog Input for TMADC0 Channel 9
Y8	AN10	I	D / HighZ / VDDM	Analog Input 10
	ADC_TMADC0CH10			Analog Input for TMADC0 Channel 10
W7	AN11	I	D / HighZ / VDDM	Analog Input 11
	ADC_TMADC0CH11			Analog Input for TMADC0 Channel 11
T7	AN12	I	D / HighZ / VDDM	Analog Input 12
	ADC_TMADC0CH12			Analog Input for TMADC0 Channel 12
W6	AN13	I	D / HighZ / VDDM	Analog Input 13
	ADC_TMADC0CH13			Analog Input for TMADC0 Channel 13

(table continues...)

Table 51 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
U6	AN14	I	D / HighZ / VDDM	Analog Input 14
	ADC_TMADC0CH14			Analog Input for TMADC0 Channel 14
T6	AN15	I	D / HighZ / VDDM	Analog Input 15
	ADC_TMADC0CH15			Analog Input for TMADC0 Channel 15
W5	AN16	I	D / HighZ / VDDM	Analog Input 16
	ADC_TMADC1CH4			Analog Input for TMADC1 Channel 4
U5	AN17/P40_10	I	S / PU1 / VDDM	Analog Input 17
	ADC_TMADC1CH5			Analog Input for TMADC1 Channel 5
	SENT0_SENT5A			Receive input channel 5
W4	AN18/P40_11	I	S / PU1 / VDDM	Analog Input 18
	ADC_TMADC1CH6			Analog Input for TMADC1 Channel 6
	SENT1_SENT5A			Receive input channel 5
W3	AN19/P40_12	I	S / PU1 / VDDM	Analog Input 19
	ADC_TMADC1CH7			Analog Input for TMADC1 Channel 7
	SENT0_SENT6A			Receive input channel 6
Y3	AN20	I	D / HighZ / VDDM	Analog Input 20
	ADC_TMADC1CH8			Analog Input for TMADC1 Channel 8
Y2	AN21	I	D / HighZ / VDDM	Analog Input 21
	ADC_TMADC1CH9			Analog Input for TMADC1 Channel 9
T5	AN22	I	D / HighZ / VDDM	Analog Input 22
	ADC_TMADC1CH10			Analog Input for TMADC1 Channel 10
R5	AN23	I	D / HighZ / VDDM	Analog Input 23
	ADC_TMADC1CH11			Analog Input for TMADC1 Channel 11
W2	AN24/P40_0	I	S / PU1 / VDDM	Analog Input 24
	ADC_TMADC1CH12			Analog Input for TMADC1 Channel 12
	SENT0_SENT0A			Receive input channel 0
W1	AN25/P40_1	I	S / PU1 / VDDM	Analog Input 25
	ADC_TMADC1CH13			Analog Input for TMADC1 Channel 13
	SENT1_SENT0A			Receive input channel 0
V2	AN26/P40_2	I	S / PU1 / VDDM	Analog Input 26
	ADC_TMADC1CH14			Analog Input for TMADC1 Channel 14
	SENT0_SENT1A			Receive input channel 1

(table continues...)

Table 51 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
V1	AN27/P40_3	I	S / PU1 / VDDM	Analog Input 27
	ADC_TMADC1CH15			Analog Input for TMADC1 Channel 15
	SENT1_SENT1A			Receive input channel 1
U2	AN28/P40_13	I	S / PU1 / VDDM	Analog Input 28
	ADC_TMADC3CH0			Analog Input for TMADC3 Channel 0
	SENT1_SENT6A			Receive input channel 6
U1	AN29/P40_14	I	S / PU1 / VDDM	Analog Input 29
	ADC_TMADC3CH1			Analog Input for TMADC3 Channel 1
	SENT0_SENT7A			Receive input channel 7
T4	AN30	I	D / HighZ / VDDM	Analog Input 30
	ADC_TMADC3CH2			Analog Input for TMADC3 Channel 2
R4	AN31	I	D / HighZ / VDDM	Analog Input 31
	ADC_TMADC3CH3			Analog Input for TMADC3 Channel 3

3.3.18 BGA292_COM special

Table 52 Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
U19	PHY0_RXN	I	PHY / VDDPHPHY0	(Ball name)
	SGMII0_RXN	I		Receive data (N line)
	PCIE0_RXN	I		Receive data (N line)
R19	PHY0_TXN	O	PHY / VDDPHPHY0	(Ball name)
	PCIE0_TXN	O		Transmit data (N line)
	SGMII0_TXN	O		Transmit data (N line)
U20	PHY0_RXP	I	PHY / VDDPHPHY0	(Ball name)
	SGMII0_RXP	I		Receive data (P line)
	PCIE0_RXP	I		Receive data (P line)
R20	PHY0_TXP	O	PHY / VDDPHPHY0	(Ball name)
	PCIE0_TXP	O		Transmit data (P line)
	SGMII0_TXP	O		Transmit data (P line)
J20	PHY1_TXP	O	PHY / VDDPHPHY1	(Ball name)
	SGBT_TXP0	O		Transmit data (P line)
	SGMII1_TXP	O		Transmit data (P line)

(table continues...)

Table 52 (continued) Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
G20	PHY1_RXP	I	PHY / VDDPHPHY1	(Ball name)
	SGMII1_RXP	I		Receive data (P line)
J19	PHY1_TXN	O	PHY / VDDPHPHY1	(Ball name)
	SGBT_TXN0	O		Transmit data (N line)
	SGMII1_TXN	O		Transmit data (N line)
G19	PHY1_RXN	I	PHY / VDDPHPHY1	(Ball name)
	SGMII1_RXN	I		Receive data (N line)

3.3.19 BGA292_COM system

Table 53 System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
N19	PHYx_RESREF	I/O	—	Reference resistor
	SGMII0_RESREF	I/O		Reference resistor
	SGMII1_RESREF	I/O		Reference resistor
	PCIE0_RESREF	I/O		Reference resistor
	SGBT_RESREF	I/O		Reference resistor
P20	PCIE0REFCLKP	I	PHY / VDDPHPHY0	Reference clock (P line)
P19	PCIE0REFCLKN	I	PHY / VDDPHPHY0	Reference clock (N line)
M19	XTAL2	O	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output
M20	XTAL1	I	—	XTAL1. Main Oscillator/PLL/Clock generator input
J16	TCK	I/O	—	Signal with hybrid_probe
	DAP0	I		DAP:DAP0 Clock Input
L19	TRST	I/O	—	Signal with hybrid_probe
	DAPE0	I		DAPE: DAPE0 Data I/O DAPE: DAPE0 Data I/O (PD Devices: VSS)
K16	TMS	I/O	—	Signal with hybrid_probe
	DAP1	I/O		DAP:DAP1 Data I/O

(table continues...)

Table 53 (continued) System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
G16	ESR1	I/O	FAST / PU1 / VDDEXT	ESR1 pad data
	SMM_ESR1_PORT_IN	I		ESR1 pad data from bitslice
	PMS_ESR1WKP	I		ESR1 pin input
F16	ESR0	I/O	FAST / OD / VDDEXT	ESR0 pad data
	SMM_ESR0_PORT_IN	I		ESR0 pad data from bitslice
	PMS_ESR0WKP	I		ESR0 pin input
G17	PORST	I/O	—	Power On Reset Input. Additional strong PD in case of power fail.

3.3.20 BGA292_COM supply

Table 54 Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
U4	NC1_U4	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
Y1	NC1_Y1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
A1	VSSEXT	I	—	has to be connected to VSSEXT
B2	VSSEXT	I	—	External Vss
Y7	VAGND1	I	—	Negative Analog Reference Voltage 1
T2	VAGND2	I	—	Negative Analog Reference Voltage 1
Y6	VAREF1	I	—	Positive Analog Reference Voltage 1
T1	VAREF2	I	—	Positive Analog Reference Voltage 2
G13, G8, H12, H14, H7, H9, J13, J8, M13, M8, N12, N14, N7, N9, P8	VDD	I	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
T11	VDDEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
A2, B18, B3, D16, D5, V19, W20	VDDEXT	I	—	External Power Supply (5V / 3.3V)
Y19	VDDEXTDC	I	—	External DCDC Supply (6.5V...5.5V / 5V / 3.3V)
N20	VDDEXTOSC	I	—	External Power Supply for Oscillator (shall be supplied with same level as used for VDDEXT)
A19	VDDEXT_SENSE	I/O	—	External Power Supply (5V / 3.3V)

(table continues...)

Table 54 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
A13, D13	VDDHSIF	I	—	hs interface supply (3.3V/1.8V)
Y5	VDDM	I	—	External Power Supply (5V / 3.3V)
V20	VDDPHPHY0	I	—	PHY0 External Power Supply (1.8V)
K20	VDDPHPHY1	I	—	PHY1 External Power Supply (1.8V)
T20	VDDPHY0	I	—	PHY0 Digital Core Power Supply (0.9V / 0.95V / 1V)
H20	VDDPHY1	I	—	PHY1 Digital Core Power Supply (0.9V / 0.95V / 1V)
P13	VDD_SENSE	I/O	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
Y17	VGATE1N	O	—	DCDC N ch MOSFET gate driver output
Y18	VGATE1P	O	—	DCDC P ch MOSFET gate driver output
G10, G11, G12, G9, H10, H11, J10, J11, J14, J7, K10, K11, K12, K13, K14, K7, K8, K9, L10, L11, L12, L13, L14, L7, L8, L9, M10, M11, M14, M7, N10, N11, P10, P11, P9	VSS	I	—	Digital Ground
B19, D17, D4, E16, E5, T16, U17	VSSEXT	I	—	External Vss
W19, Y20	VSSEXTDC	I	—	DCDC Ground
L20	VSSEXTOSC	I	—	Oscillator Ground
A20	VSSEXT_SENSE	I/O	—	External Vss
A14, D14	VSSHSIF	I	—	High Speed Interface Digital Ground
Y4	VSSM	I	—	External Vss
H19, T19	VSSPHY	I	—	PHY Digital Ground
P12	VSS_SENSE	I/O	—	Digital Ground

3.4 Pad Sequence

Related information

Logic symbols for package variants on page 31
BGA436_COM package variant pin configuration on page 32

BGA292_COM package variant pin configuration on page 245
Pad Sequence on page 384
Legend on page 405

3.4.1 Sequence of pads in pad frame

Table 55 Pad Sequence

Number	Pad name	Pad type	Comment
1	COMPARATOR_VGPIO_tr	—	
2	VSSEXT_TL_HEAT	—	Supply Voltage
3	VDDEXT_50_TL	—	Supply Voltage
4	VSSEXT	—	
5	VSSEXT_TL	—	Supply Voltage
6	P02.12	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
7	PADS_BUF_P04	—	
8	P03.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
9	P03.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
10	P03.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
11	P03.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
12	VDDEXT_50_TL_HEAT	—	Supply Voltage
13	P03.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
14	P03.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
15	P03.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
16	VDDEXT_50_TL_HEAT	—	Supply Voltage
17	P03.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
18	P03.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
19	P03.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
20	PADS_BUF_WKPCLR_3	—	
21	VSSEXT_TL_HEAT	—	Supply Voltage
22	P03.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
23	P03.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
24	VDDEXT_50_TL	—	Supply Voltage
25	P03.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
26	P03.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
27	PADS_BUF_P03	—	
28	P04.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
29	P04.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
30	VSSEXT_TL_HEAT	—	Supply Voltage
31	P04.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
32	P03.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
33	P04.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
34	P04.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
35	ANARES_TGATE_6	—	
36	P03.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
37	P04.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
38	VDDEXT_50_TL_HEAT	—	Supply Voltage
39	ANARES_TGATE_5	—	
40	P04.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
41	P04.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
42	P04.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
43	VSSEXT_TL	—	Supply Voltage
44	P04.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
45	P02.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
46	P02.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
47	P02.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
48	OTP	VDDEXT	
49	VDDEXT_50_TL_HEAT	—	Supply Voltage
50	P02.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
51	P02.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
52	P02.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
53	VSSEXT_TL_HEAT	—	Supply Voltage
54	P02.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
55	VDDEXT_50_TL	—	Supply Voltage
56	P02.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
57	P02.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
58	P02.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
59	VDD_V	—	Supply Voltage
60	VSS_V	—	Supply Voltage
61	PADS_BUF_WKPCLR_2	—	
62	P02.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
63	P02.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
64	VSSEXT_TL	—	Supply Voltage
65	PADS_BUF_P02	—	
66	P02.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
67	VDDEXT_50_TL	—	Supply Voltage
68	P02.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
69	P02.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
70	P01.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
71	VSSEXT_TL_HEAT	—	Supply Voltage
72	P01.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
73	P01.9	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
74	P01.2	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
75	PADS_BUF_P01	—	
76	VDDEXT_50_TL_HEAT	—	Supply Voltage
77	P01.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
78	P01.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
79	P01.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
80	P01.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
81	P01.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
82	VSSEXT_TL	—	Supply Voltage
83	P00.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
84	P01.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
85	P00.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
86	VDDEXT_50_TL_HEAT	—	Supply Voltage
87	P01.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
88	VSSEXT_TL	—	Supply Voltage

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
89	P00.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
90	P00.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
91	P01.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
92	PADS_BUF_P00	—	
93	VDDEXT_50_TL	—	Supply Voltage
94	P01.4	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
95	P01.5	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
96	P01.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
97	TERMINATOR5V	—	
98	BANDGAP_VGPIO	—	
99	TERMINATOR5V	—	
100	P01.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
101	VSSEXT_TL_HEAT	—	Supply Voltage
102	PADS_BUF_WKPCLR_1	—	
103	VDDEXT_50_TL	—	Supply Voltage
104	TERMINATOR5V	—	
105	breaker	—	
106	VSSM_CONVIF0	—	Supply Voltage
107	VDDM_50_CONVIF0	—	Supply Voltage
108	term_lvds	—	
109	AN0	D / HighZ / VDDM	Analog Input 0
110	AN1	D / HighZ / VDDM	Analog Input 1
111	AN6	D / HighZ / VDDM	Analog Input 6
112	AN3	D / HighZ / VDDM	Analog Input 3
113	AN12	D / HighZ / VDDM	Analog Input 12
114	AN7	D / HighZ / VDDM	Analog Input 7
115	AN4	D / HighZ / VDDM	Analog Input 4
116	AN2	D / HighZ / VDDM	Analog Input 2
117	VSSM_CONVPAD	—	Supply Voltage
118	VSSM_CONVPAD	—	Supply Voltage
119	AN5	D / HighZ / VDDM	Analog Input 5

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
120	VAGND1	Vx	Supply Voltage
121	AN8	D / HighZ / VDDM	Analog Input 8
122	AN10	D / HighZ / VDDM	Analog Input 10
123	AN9	D / HighZ / VDDM	Analog Input 9
124	VAREF1	Vx	Supply Voltage
125	AN14	D / HighZ / VDDM	Analog Input 14
126	AN11	D / HighZ / VDDM	Analog Input 11
127	AN13	D / HighZ / VDDM	Analog Input 13
128	AN16	D / HighZ / VDDM	Analog Input 16
129	VDDM_50_CONVPAD	—	Supply Voltage
130	AN18/P40_11	S / PU1 / VDDM	Analog Input 18
131	AN15	D / HighZ / VDDM	Analog Input 15
132	AN20	D / HighZ / VDDM	Analog Input 20
133	AN19/P40_12	S / PU1 / VDDM	Analog Input 19
134	AN21	D / HighZ / VDDM	Analog Input 21
135	AN17/P40_10	S / PU1 / VDDM	Analog Input 17
136	AN33/P40_5	S / PU1 / VDDM	Analog Input 33
137	AN35	D / HighZ / VDDM	Analog Input 35
138	AN24/P40_0	S / PU1 / VDDM	Analog Input 24
139	AN25/P40_1	S / PU1 / VDDM	Analog Input 25
140	AN32/P40_4	S / PU1 / VDDM	Analog Input 32
141	VSSM_CONVPAD	—	Supply Voltage
142	VSSM_CONVPAD	—	Supply Voltage
143	comparator	—	
144	comparator	—	
145	VSSM_CONVPAD	—	Supply Voltage
146	VSSM_CONVPAD	—	Supply Voltage
147	VAREF2	Vx	Supply Voltage
148	AN39/P40_9	S / PU1 / VDDM	Analog Input 39
149	AN26/P40_2	S / PU1 / VDDM	Analog Input 26
150	AN27/P40_3	S / PU1 / VDDM	Analog Input 27
151	VAGND2	Vx	Supply Voltage
152	AN37/P40_7	S / PU1 / VDDM	Analog Input 37

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
153	VSSM_CONVPAD	—	Supply Voltage
154	AN34	D / HighZ / VDDM	Analog Input 34
155	AN36/P40_6	S / PU1 / VDDM	Analog Input 36
156	AN42	D / HighZ / VDDM	Analog Input 42
157	VDDM_50_CONVPAD	—	Supply Voltage
158	AN28/P40_13	S / PU1 / VDDM	Analog Input 28
159	AN30	D / HighZ / VDDM	Analog Input 30
160	AN29/P40_14	S / PU1 / VDDM	Analog Input 29
161	AN22	D / HighZ / VDDM	Analog Input 22
162	AN40	D / HighZ / VDDM	Analog Input 40
163	AN38/P40_8	S / PU1 / VDDM	Analog Input 38
164	VSSM_CONVPAD	—	Supply Voltage
165	AN43	D / HighZ / VDDM	Analog Input 43
166	AN41	D / HighZ / VDDM	Analog Input 41
167	AN31	D / HighZ / VDDM	Analog Input 31
168	AN23	D / HighZ / VDDM	Analog Input 23
169	term_lvds	—	
170	breaker	—	
171	VSSEXT_CONVE	—	Supply Voltage
172	P00.11	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
173	P00.12	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
174	P00.7	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
175	VDDEXT_50_CONVE	—	Supply Voltage
176	P00.9	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
177	P00.4	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
178	P00.5	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
179	P00.2	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
180	P00.3	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
181	P00.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
182	P00.10	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
183	P00.8	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
184	P00.6	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
185	term_lvds	—	
186	breaker	—	
187	DIODE	—	
188	DIODE_TCP	—	
189	TREFE_L	—	
190	TPROTBS	—	
191	TERMINATOR5V	—	
192	ANARES_TGATE_5V	—	
193	TGRPROT2CORE_5V	—	
194	P35.1	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
195	P35.2	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
196	VSSEVRSB_PAD	—	Supply Voltage
197	P35.0	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
198	P35.5	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
199	P35.3	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
200	VDDEVRSB_50_PAD	—	Supply Voltage
201	P35.4	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
202	P33.3	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
203	P33.1	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
204	VSSEVRSB_PAD	—	Supply Voltage
205	P33.11	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
206	P33.2	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
207	P33.0	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
208	P33.5	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
209	P34.4	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
210	P34.1	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
211	VDDEVRSB_50_PAD	—	Supply Voltage
212	P34.2	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
213	P33.7	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
214	P33.6	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
215	P34.3	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
216	VSSEVRSB_PAD	—	Supply Voltage
217	P33.14	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
218	PADS_BUF_P34	—	
219	P33.9	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
220	P33.10	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
221	PADS_BUF_P33	—	
222	P33.15	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
223	P34.5	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
224	VDDEVRSB_50_PAD	—	Supply Voltage
225	P32.5	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
226	P33.12	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
227	P32.6	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
228	P33.8	FAST / HighZ / VDDEVRSB	General-purpose I/O
229	P33.4	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
230	P33.13	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
231	VSSEVRSB_PAD	—	Supply Voltage
232	P32.4	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
233	PADS_BUF_P32	—	
234	P32.2	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
235	P32.7	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
236	VDDEVRSB_50_PAD	—	Supply Voltage
237	VSS_H	—	Supply Voltage
238	VDDPMS1_H	—	Supply Voltage
239	VDDEVRSB_50_TL	—	Supply Voltage
240	VSSQ_TL	—	Supply Voltage
241	VDDEVRSB_50_TL	—	Supply Voltage

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
242	VSSEVRSB_TL	—	Supply Voltage
243	TGRPROT2CORE	—	
244	TGRPROTBS	—	
245	TERMINATOR5V	—	
246	DIODE_TCP	—	
247	Tpp7ve	—	
248	VDDEXTDC_70_TL_SENSE	—	Supply Voltage
249	Tpp7v	—	
250	VDDEXTDC_70_TL	—	Supply Voltage
251	VDDEXTDC_70_TL	—	Supply Voltage
252	VDDEXTDC_70_TL	—	Supply Voltage
253	CTRL1V3P0	—	DCDC P ch.MOSFET gate driver output External Pass Device gate control for EVRC
254	CTRL1V3P2	—	
255	CTRL1V3P1	—	DCDC P ch.MOSFET gate driver output External Pass Device gate control for EVRC
256	Tpp7v	—	
257	CTRL1V3N2	—	DCDC N ch.MOSFET gate driver output SMPS mode: analog output. External Pass Device gate control for EVRC
258	CTRL1V3N1	—	DCDC N ch.MOSFET gate driver output SMPS mode: analog output. External Pass Device gate control for EVRC
259	CTRL1V3N0	—	DCDC N ch.MOSFET gate driver output SMPS mode: analog output. External Pass Device gate control for EVRC
260	VSSEXTDC_TL	—	Supply Voltage
261	VSSEXTDC_TL	—	Supply Voltage
262	VSSEXTDC_TL	—	Supply Voltage
263	Dgtpp	—	
264	VSS_H	—	Supply Voltage
265	PMS_testmode	—	
266	VSSEXT_TL_HEAT_H	—	Supply Voltage
267	P31.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
268	P31.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
269	P30.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
270	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
271	P30.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
272	TERMINATOR5V	—	
273	BANDGAP_HGPIO	—	
274	TERMINATOR5V	—	
275	P30.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
276	P30.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
277	P30.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
278	P30.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
279	P30.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
280	P30.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
281	P30.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
282	PADS_BUF_WKPCLR_0	—	
283	P30.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
284	P30.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
285	VSS_H	—	Supply Voltage
286	VDD_H	—	Supply Voltage
287	P30.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
288	VSSEXT_TL_HEAT_H	—	Supply Voltage
289	P30.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
290	P30.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
291	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
292	P30.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
293	PADS_BUF_P30	—	
294	P30.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
295	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
296	VSSEXT_TL_HEAT_H	—	Supply Voltage
297	COMPARATOR_HGPIO_lb	—	
298	CRACK_SENSOR_1	—	

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
299	COMPARATOR_VGPIO_bl	—	
300	VDDEXT_50_TL	—	Supply Voltage
301	VSSEXT_TL	—	Supply Voltage
302	TOXMON	—	
303	VDDEXT_50_TL	—	Supply Voltage
304	VSSEXT_TL	—	Supply Voltage
305	P23.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
306	P23.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
307	VDDEXT_50_TL_HEAT	—	Supply Voltage
308	P23.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
309	PADS_BUF_P23	—	
310	P23.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
311	P23.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
312	P23.7	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
313	VSSEXT_TL_HEAT	—	Supply Voltage
314	P23.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
315	P23.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
316	COMPARATOR_VLVDS_bl	—	
317	VDDEXT_50_TL	—	Supply Voltage
318	P22.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
319	VSSEXT_TL_HEAT	—	Supply Voltage
320	VDDEXT_50_TL_HEAT	—	Supply Voltage
321	PADS_BUF_P22	—	
322	P22.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
323	P22.2	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
324	P22.3	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
325	P22.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
326	P22.0	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
327	P22.1	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
328	P22.7	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
329	VDDEXT_50_TL	—	Supply Voltage
330	VSSEXT_TL_HEAT	—	Supply Voltage
331	P22.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
332	VDDEXT_50_TL_HEAT	—	Supply Voltage
333	VSS_V	—	Supply Voltage
334	VDD_V	—	Supply Voltage
335	P22.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
336	VSSEXT_TL_HEAT	—	Supply Voltage
337	PADS_BUF_P25	—	
338	P22.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
339	VDDEXT_50_TL_HEAT	—	Supply Voltage
340	P22.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
341	P25.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
342	TERMINATOR5V	—	
343	PHY2_RXN	PHY / VDDPHPHY2	Receive data (N line)
344	PCIE1REFCLKP	PHY / VDDPHPHY2	Reference clock (P line)
345	PHY2_TXN	PHY / VDDPHPHY2	Transmit data (N line)
346	PHY2_RXP	PHY / VDDPHPHY2	Receive data (P line)
347	PCIE1REFCLKN	PHY / VDDPHPHY2	Reference clock (N line)
348	PHY2_TXP	PHY / VDDPHPHY2	Transmit data (P line)
349	VSSPHY2_TL	—	Supply Voltage
350	VDDPHY2_10_TL	—	Supply Voltage
351	VDDPHPHY2_18_TL	—	Supply Voltage
352	PHYx_RESREF2	PHY	Reference resistor
353	PHY0_RXN	PHY / VDDPHPHY0	Receive data (N line)
354	PCIE0REFCLKP	PHY / VDDPHPHY0	Reference clock (P line)
355	PHY0_TXN	PHY / VDDPHPHY0	Transmit data (N line)
356	PHY0_RXP	PHY / VDDPHPHY0	Receive data (P line)
357	PCIE0REFCLKN	PHY / VDDPHPHY0	Reference clock (N line)

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
358	PHY0_TXP	PHY / VDDPHPHY0	Transmit data (P line)
359	VSSPHY0_TL	—	Supply Voltage
360	VDDPHY0_10_TL	—	Supply Voltage
361	VDDPHPHY0_18_TL	—	Supply Voltage
362	PHYx_RESREF0	PHY	Reference resistor
363	XTAL2	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
364	XTAL1	XTAL / VDDEXTOSC	XTAL1. Main Oscillator/PLL/Clock generator input XTAL1. Main Oscillator/PLL/Clock Generator Input.
365	VSS_OSC	—	Supply Voltage
366	VDDEXTOSC_50_TL	—	Supply Voltage
367	PHY1_TXP	PHY / VDDPHPHY1	Transmit data (P line)
368	PHY1_RXP	PHY / VDDPHPHY1	Receive data (P line)
369	PHY1_TXN	PHY / VDDPHPHY1	Transmit data (N line)
370	PHY1_RXN	PHY / VDDPHPHY1	Receive data (N line)
371	VSSPHY1_TL	—	Supply Voltage
372	VDDPHPHY1_18_TL	—	Supply Voltage
373	VDDPHY1_10_TL	—	Supply Voltage
374	PHYx_RESREF1	PHY	Reference resistor
375	TERMINATOR5V	—	
376	VDDEXT_50_TL_HEAT	—	Supply Voltage
377	TCK	FAST / PD3 / VDDEXT	
378	PADS_BUF_P21	—	
379	TRST	FAST / PU2 / VDDEXT	
380	VSSEXT_TL_HEAT	—	Supply Voltage
381	BANDGAP_VLVDS	—	
382	TERMINATOR5V	—	
383	TMS	FAST / PD2 / VDDEXT	
384	P21.2	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
385	P21.3	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
386	P21.7	FAST / PU2 / VDDEXT / ES	General-purpose I/O
387	P21.4	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
388	P21.5	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
389	P21.6	FAST / PD3 / PU2 / VDDEXT / ES	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
390	VSSEXT_TL_HEAT	—	Supply Voltage
391	VDDEXT_50_TL_HEAT	—	Supply Voltage
392	P21.0	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
393	P21.1	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
394	P20.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
395	P20.2	S / PU / VDDEXT	General-purpose I/O This pin is latched at power on reset release to enter test mode.
396	COMPARATOR_VLVDS_br	—	
397	PADS_BUF_P20	—	
398	P20.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
399	VDDEXT_50_TL_HEAT	—	Supply Voltage
400	P20.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
401	P20.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
402	VSS_V	—	Supply Voltage
403	VDD_V	—	Supply Voltage

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
404	ESR1	FAST / PU1 / VDDEXT	ESR1: External System Request Reset 1. Default NMI function (Configuration options see also SMM / SCU chapter for details). EVR Wakeup Source. Behavior after power-on can be different. See also SMM chapter: External service request interface. Behavior for system and application reset differs to the warm power-on reset behavior and is in that case always pull-up.
405	ESR0	FAST / OD / VDDEXT	ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter Reset Control Unit and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
406	PORST	PORST / PD / VDDEXT	Power On Reset Input. Additional strong PD in case of power fail.
407	P20.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
408	VSSEXT_TL_HEAT	—	Supply Voltage
409	P20.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
410	P20.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
411	VDDEXT_50_TL_HEAT	—	Supply Voltage
412	P20.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
413	P20.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
414	P20.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
415	VDDEXT_50_TL_HEAT	—	Supply Voltage
416	VSSEXT_TL_HEAT	—	Supply Voltage
417	P20.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
418	VDDEXT_50_TL_UNLOADED	—	Supply Voltage
419	P20.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
420	VSSEXT_TL_UNLOADED	—	Supply Voltage

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
421	VDDEXT_50_TL_HEAT	—	Supply Voltage
422	VDDEXT_50_TL	—	Supply Voltage
423	VSSEXT_TL_HEAT	—	Supply Voltage
424	VSSEXT_TL_HEAT	—	Supply Voltage
425	COMPARATOR_VGPIO_br	—	
426	COMPARATOR_HGPIO_rb	—	
427	TERMINATOR5V	—	
428	DIODE	—	
429	Bridge_port16	—	
430	P16.1	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
431	P16.0	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
432	VDDHSIF_33_TL	—	Supply Voltage
433	P16_SPARE	VDDHSIF	
434	VDD_33_H	—	Supply Voltage
435	VSS_33_H	—	Supply Voltage
436	P16.3	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
437	P16.2	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
438	VSSHSIF_TL	—	Supply Voltage
439	P16.5	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
440	P16.4	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
441	VDDHSIF_33_TL	—	Supply Voltage
442	P16.8	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
443	TRIMANA	—	
444	P16.6	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
445	VSSHSIF_TL	—	Supply Voltage
446	VDD_33_H	—	Supply Voltage
447	VSS_33_H	—	Supply Voltage
448	P16.7	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
449	VDDHSIF_33_TL	—	Supply Voltage
450	P16.9	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
451	P16.10	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
452	VSSHSIF_TL	—	Supply Voltage
453	P16.12	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
454	P16.13	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
455	VDDHSIF_33_TL	—	Supply Voltage
456	P16.11	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
457	P16.14	HSFAST / PU1 / VDDHSIF / ES	General-purpose I/O
458	VSSHSIF_TL	—	Supply Voltage
459	Bridge_port16	—	
460	DIODE	—	
461	TERMINATOR5V	—	
462	PADS_BUF_P16_ENPS	—	
463	PADS_BUF_P16_TRIST	—	
464	ANARES_TGATE_1	—	
465	ANARES_TGATE_2	—	
466	P15.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
467	P15.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
468	P15.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
469	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
470	ANARES_TGATE_3	—	
471	ANARES_TGATE_4	—	
472	P15.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
473	P15.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
474	VSSEXT_TL_HEAT_H	—	Supply Voltage
475	P15.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
476	COMPARATOR_HLVDS_rb	—	
477	P15.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
478	P15.11	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
479	P15.10	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
480	P15.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
481	P15.13	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
482	P15.12	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
483	P15.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
484	PADS_BUF_WKPCLR_5	—	
485	P15.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
486	P15.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
487	PADS_BUF_P14	—	
488	P14.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
489	VSSEXT_TL_HEAT_H	—	Supply Voltage
490	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
491	P14.12	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
492	P14.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
493	P13.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
494	P13.8	FAST / PU2 / VDDEXT / ES	General-purpose I/O
495	P14.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
496	P14.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
497	P14.0	FAST / PU1 / VDDEXT / ES2	General-purpose I/O
498	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
499	P14.1	FAST / PU1 / VDDEXT / ES2	General-purpose I/O
500	P14.3	SLOW / PU2 / VDDEXT / ES	General-purpose I/O
501	PADS_BUF_P15	—	
502	P13.5	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
503	P13.4	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
504	VSSEXT_TL_HEAT_H	—	Supply Voltage
505	P13.7	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
506	P13.6	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
507	P14.2	SLOW / PU2 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
508	P14.4	SLOW / PU2 / VDDEXT / ES	General-purpose I/O
509	VDDEXT_50_TL	—	Supply Voltage
510	BANDGAP_HLVDS	—	
511	TERMINATOR5V	—	
512	P14.5	FAST / PU2 / VDDEXT / ES	General-purpose I/O
513	P14.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
514	P14.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
515	VDD_H	—	Supply Voltage
516	VSS_H	—	Supply Voltage
517	P14.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
518	VSSEXT_TL_HEAT_H	—	Supply Voltage
519	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
520	P13.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
521	P13.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
522	P13.13	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
523	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
524	P13.12	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
525	P14.10	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
526	P14.9	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
527	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
528	VSSEXT_TL_HEAT_H	—	Supply Voltage
529	P13.1	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
530	P13.0	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
531	VSSEXT_TL_HEAT_H	—	Supply Voltage
532	P13.3	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
533	P13.2	LVDS_TX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
534	PADS_BUF_P13	—	

(table continues...)

Table 55 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
535	P13.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
536	PADS_BUF_WKPCLR_4	—	
537	VDDEXT_50_TL	—	Supply Voltage
538	COMPARATOR_HLVDS_rt	—	
539	P13.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
540	P10.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
541	P10.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
542	P10.5	SLOW / PU2 / VDDEXT / ES	General-purpose I/O
543	VSSEXT_TL_HEAT_H	—	Supply Voltage
544	P10.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
545	P10.9	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
546	P10.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
547	P10.13	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
548	PADS_BUF_P10	—	
549	P10.6	FAST / PU2 / VDDEXT / ES	General-purpose I/O
550	P10.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
551	VDDEXT_50_TL_HEAT_H	—	Supply Voltage
552	P10.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
553	P10.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
554	P10.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
555	P10.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
556	P10.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
557	P10.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
558	VSSEXT_TL	—	Supply Voltage
559	VDDEXT_50_TL	—	Supply Voltage
560	COMPARATOR_HGPIO_rt	—	

3.5 Legend

Column'Ctrl.'

- I = Input (for GPIO port lines with Pn_DRVCFG bit field Selection MODE = $0XXXX_B$)
- O = Output (for GPIO port lines the ´O´ represents in most cases the port HWOUT function)
- O0 = Output with Pn_DRVCFG bit field selection MODE = $1X0000_B$
- O1 = Output with Pn_DRVCFG bit field selection MODE = $1X0001_B$ (ALT1)
- O2 = Output with Pn_DRVCFG bit field selection MODE = $1X0010_B$ (ALT2)
- O3 = Output with Pn_DRVCFG bit field selection MODE = $1X0011_B$ (ALT3)
- O4 = Output with Pn_DRVCFG bit field selection MODE = $1X0100_B$ (ALT4)
- O5 = Output with Pn_DRVCFG bit field selection MODE = $1X0101_B$ (ALT5)
- O6 = Output with Pn_DRVCFG bit field selection MODE = $1X0110_B$ (ALT6)
- O7 = Output with Pn_DRVCFG bit field selection MODE = $1X0111_B$ (ALT7)
- O8 = Output with Pn_DRVCFG bit field selection MODE = $1X1000_B$ (ALT8)
- O9 = Output with Pn_DRVCFG bit field selection MODE = $1X1001_B$ (ALT9)
- O10 = Output with Pn_DRVCFG bit field selection MODE = $1X1010_B$ (ALT10)
- O11 = Output with Pn_DRVCFG bit field selection MODE = $1X1011_B$ (ALT11)
- O12 = Output with Pn_DRVCFG bit field selection MODE = $1X1100_B$ (ALT12)
- O13 = Output with Pn_DRVCFG bit field selection MODE = $1X1101_B$ (ALT13)
- O14 = Output with Pn_DRVCFG bit field selection MODE = $1X1110_B$ (ALT14)
- O15 = Output with Pn_DRVCFG bit field selection MODE = $1X1111_B$ (ALT15)
- I# and O# mark SCR peripheral mappings

Column 'Buffer type'

- FAST = Pad class FAST (5V/3.3V)
- HSFAST = Pad class HSFAST (3.3V/1.8V)
- SLOW = Pad class SLOW (5V/3.3V)
- LVDS_TX = Pad class LVDS Transmit
- LVDS_RX = Pad class LVDS Receive
- S = Pad class S (Analog Input overlayed with General Purpose Input)
- D = Pad class D (Analog Input)
- Porst = Porst input Pad
- XTAL1 = XTAL1 input Pad
- XTAL2 = XTAL2 output Pad
- PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
- PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0). The default state of GPIOs (Px.y) during and after PORST active is controlled through HWCFG6 (P14.4). See PMS, HWCFG[6]
- PU2 = with pull-up device connected during startup and reset, HighZ in Standby mode
- PU3 = with pull-up device connected during startup and reset, HighZ in Standby mode, after reset Pad Level transitions from AL to TTL
- PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
- PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0). The default state of GPIOs (Px.y) during and after PORST active is controlled through HWCFG6 (P14.4). See PMS, HWCFG[6].
- PD2 = with pull-down device connected during startup and reset, HighZ in Standby mode
- PD3 = with pull-down device connected during startup and reset, HighZ in Standby mode, after reset Pad Level transitions from AL to TTL
- OD = open drain during reset ($\overline{\text{PORST}}$ = 0)

- ES = Supports Emergency Stop
- ES1 = ES. ES is controlled by Pn_PCSRSEL register.
- ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message
- ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI
- ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode
- ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR
- ES6 = ES. On LVDS TX pads the ES affects the pads only in CMOS mode, not in LVDS mode. Thus, only when LPCRx.TX_EN selects the CMOS Mode, the output is switched off in the ES event

Related information

Logic symbols for package variants on page 31
BGA436_COM package variant pin configuration on page 32
BGA292_COM package variant pin configuration on page 245
Pad Sequence on page 384

4 Electrical characteristics

4.1 Parameter interpretation

The parameters listed in this section represent both the characteristics of the device and its requirements on the system. To aid the interpretation of the parameters when evaluating them for a design, they are marked with a two-letter abbreviation in the 'Symbol' column.

- **CC**
  - Controller Characteristics which are a distinctive feature of the device and must be taken into account for a system design
- **SR**
  - System Requirements which must be provided by the microcontroller system in which the device is designed in to

4.2 Absolute maximum ratings

Note: *Stresses above the values listed under 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*

4.2.1 Absolute maximum ratings

Table 56 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} *SR*	-65	-	150	°C	Up to 65 h at T_J = 150°C
Maximum Junction Temperature	T_J *SR*	-40	-	160[1]	°C	
Voltage at $V_{DDEXTDC}$ EVRC supply pin with respect to $V_{SSEXTDC}$	$V_{DDEXTDC}$ *SR*	-0.7	-	7.5	V	Up to 2.8 h; EVRC in reset (no switching)
Voltage at V_{DDM}, V_{DDEXT}, V_{DDFLEX} and $V_{DDEVRSB}$ power supply pins with respect to V_{SSEXT}	V_{PADIO} *SR*	-0.7	-	6.5	V	Up to 2.8 h
		-0.7	-	5.7	V	Up to 72 h
Voltage at V_{DD} and V_{DDPHYx} power supply pins with respect to V_{SS}[2][3]	V_{DD} *SR*	-0.7	-	1.2	V	Up to 2.8 h
		-0.7	-	1.14	V	Up to 72 h
Voltage at V_{DDHSIF} power supply pins with respect to V_{SSHSIF}	V_{DDHSIF} *SR*	-0.7	-	4.43	V	Up to 2.8 h
		-0.7	-	3.76	V	Up to 72 h
Voltage at $V_{DDPHPHYx}$ power supply pins with respect to V_{SS}	$V_{DDPHPHYx}$ *SR*	-0.7	-	2.4	V	Up to 2.8 h
		-0.7	-	2.0	V	Up to 72 h
Voltage on all analog and class S input pins with respect to V_{SS}[4]	V_{IN} *SR*	-0.7	-	6.5	V	Up to 2.8 h
Voltage on V_{DDHSIF} (Port 16) input pins with respect to V_{SSHSIF}[4]	V_{IN} *SR*	-0.7	-	4.43	V	Up to 2.8 h
Voltage on V_{DDPHYx} (HSPHY) input pins with respect to V_{SSPHY}[4]						
Voltage on all other input pins with respect to V_{SS}.[4]	V_{IN} *SR*	-0.7	-	6.5	V	Up to 2.8 h
Input current on any pin during overload condition [5]	I_{IN} *SR*	-10	-	10	mA	Up to 2.8 h

(table continues...)

Table 56 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Absolute maximum sum of all input circuit currents during overload condition for all ports[5]	ΣI_{INx} *SR*	-100	-	100	mA	

1) Continuous operation of the device at Tj absolute max. is prohibited. Duration must comply with the temperature profiles approved by Infineon
2) Valid for cumulated overshoots of up to 2.8 h
3) Due to EVRC output voltage oscillation during switch off phase, V_{DD} can drop down to -0.7 V. For VDD an input level down up to -0.7 V during switch off phase will not cause any damage or reliability issues.
4) Voltages below V_{IN} (Min) have no impact to the device reliability as long as the times and currents defined in section Pin reliability in overload for the affected pad(s) are not violated.
5) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device

4.3 Pin reliability in overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- Allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined, the allowed time includes example temperature profiles. The number of hours in example temperature profiles are examples only, and the applicable numbers are defined by the customer profiles accepted by Infineon.

  Operating conditions are met for

  - pad supply levels
  - temperature

If a pin current is out of the operating conditions but within the overload parameters, then the parameters functionality of this pin as stated in the operating conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Related information

Operating conditions on page 413
Example temperature profiles on page 419

4.3.1 Overload characteristics

Table 57 Overload characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	Except LVDS. Port 16 pins are limited to 60 h over lifetime
		-15[1]	-	15[1]	mA	Except LVDS and Port 16 pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-5	-	5	mA	Limited to 60 h over lifetime
		-3	-	3	mA	
Absolute sum of all analog input currents for analog inputs during overload conditon	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	V_{SS} - 2	-	V_{DDIO} + 2[2]	V	Limited to 60 h over lifetime; valid for non LVDS and analog pads

(table continues...)

Table 57 (continued) Overload characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	I_{OUT} *CC*	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong
Overload coupling factor for digital inputs, negative	K_{OVDN} *CC*	-	-	$3*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbour fast pads; -5 mA < I_{IN} < 0 mA
		-	-	$1*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbour slow pads; -5 mA < I_{IN} < 0 mA
		-	-	0.87		Overload injected on LVDS RX pad and affecting neighbour LVDS pads
		-	-	0.55		Overload injected on LVDS TX pad and affecting neighbour LVDS pads
Overload coupling factor for digital inputs, positive	K_{OVDP} *CC*	-	-	$1.5*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbour GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbour LVDS pads
		-	-	$5*10^{-3}$		Overload injected on LVDS TX pad and affecting neighbour LVDS pads
Overload coupling factor for analog inputs, negative[3]	K_{OVAN} *CC*	-	-	$1*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; -5 mA < I_{IN} < 0 mA
		-	-	$1*10^{-5}$		else -5 mA < I_{IN} < 0 mA
Overload coupling factor for analog inputs, positive[3] [4]	K_{OVAP} *CC*	-	-	$2*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; 0 mA < I_{IN} < 5 mA
		-	-	$2*10^{-5}$		else 0 mA < I_{IN} < 5 mA

1) Reduced TMADC / DSADC (if feature available) result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.
2) VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB
3) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures. The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.

4) In case of overload condition on analog inputs, the V_{DDEXT}/V_{DDM} supply must not float.

4.4 Operating conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC4DxAA-step COM.

Digital supply voltages applied to the TC4DxAA-step COM must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise stated in the Note / Test Condition column.

Related information

Pin reliability in overload on page 410

4.4.1 Clock operating conditions

Table 58 Clock operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
System PLL and Peripheral PLL clocks						
PLL0 output frequency from SYS PLL	f_{PLL0} *SR*	25	-	500	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} *SR*	25	-	160	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} *SR*	50	-	200	MHz	
PLL3 output frequency from PER PLL	f_{PLL3} *SR*	50	-	400[1)]	MHz	
PLL-PPU output frequency						
System clocks - CPU						
CPU frequency (All CPUs)	f_{CPUx} *SR*	25[2)]	-	500	MHz	
CPU-CS frequency	f_{CPU_CS} *SR*	25[2)]	-	500	MHz	
PPU frequency						
System clocks						
SRI frequency	f_{SRI} *SR*	25[2)]	-	500	MHz	
SPB frequency	f_{SPB} *SR*	25[2)]	-	100	MHz	
TPB frequency	f_{TPB} *SR*	-	-	250	MHz	
COMPB frequency	f_{COMPB} *SR*	25[2)]	-	100	MHz	
FSI frequency	f_{FSI} *SR*	25[3)]	-	100	MHz	
eGTM frequency	f_{eGTM} *SR*	-	-	500	MHz	
STM frequency	f_{STM} *SR*	-	-	500	MHz	
GETH frequency	f_{GETH} *CC*	150	-	250	MHz	
LETH frequency						
MCANH frequency	f_{MCANH} *SR*	f_{MCAN}	-	250	MHz	

(table continues...)

Table 58 (continued) Clock operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CANXL host frequency	f_{CANXLH} *SR*	f_{CANXL}	-	250	MHz	
Peripheral clocks						
TMADC frequency	f_{ADC} *SR*	-	160[4]	-	MHz	
ERAY frequency	f_{ERAY} *SR*	-	80	-	MHz	
ASCLIN frequency	$f_{ASCLINx}$ *SR*	-	-	200	MHz	
CAN frequency	f_{MCAN} *SR*	-	-	160	MHz	
CANXL frequency	f_{CANXL} *SR*	-	-	160	MHz	
LETH frequency						
MSC frequency	f_{MSC} *SR*	-	-	200	MHz	
I2C frequency	f_{I2C} *SR*	-	-	100	MHz	
QSPI frequency	f_{QSPI} *SR*	-	-	200	MHz	
xSPI frequency[5]	f_{XSPI} *SR*	-	-	200[6]	MHz	
SGBT frequency	f_{SGBT} *SR*	-	20	25	MHz	
External clock inputs						
PCIe external reference clock frequency	$f_{PCIEREFCLK}$ *SR*	-	100	-	MHz	

1) 400 MHz is the maximum PLL3 operating frequency for test operations only. It is strongly recommended that applications use the PLL3 output frequency of 200 MHz.
2) In case of operation with the *f* (MIN) value the ratio of *f* (MIN) / f_{SRI} and *f*(MIN) / f_{SPB} shall be 1/1
3) For FSI frequency f_{FSI} < 100 MHz the bank sleep feature shall not be used to ensure a proper shutdown operation of the NVM in case of a reset. Operation at f_{FSI} (Min) prolongs data memory and SOTA program memory write times significantly.
4) The proper functionality of the module can only be ensured for the typical clock frequency setting.
5) The appropriate baud rate divider in CCU and XSPI for the maximum supported data rate in each device must be selected for both fast (via HSPHY, if applicable) and slow (via GPIO) XSPI interfaces
6) The max. frequency setting is also valid for the clock named f_{XSPISL}.

Related information

Supply operating conditions on page 415
Limitation of supply voltage over time on page 417
Temperature operating conditions on page 418
Example temperature profiles on page 419

4.4.2 Supply operating conditions

Table 59 Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for EVRC DCDC regulator and MOSFET gate driver	$V_{DDEXTDC}$ *SR*	4.95[1]	-	7	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode with EVRC active.
		2.97[1]	-	5.5	V	HWCFG [2:1] = [00, 01 or 10]. Low-voltage $V_{DDEXTDC}$ modes.
External supply voltage for IO supply pins	V_{DDEXT} *SR*	4.5	5.0	5.5[2]	V	Nominal 5 V Pad / Port Pin supply range. 5 V pad parameters are valid. 5 V NVM programming range
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid; a running NVM command sequence (e.g. program or erase) shall be suspended or aborted
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid. 3.3 V NVM programming range
External supply voltage for main XTAL/Oscillator[3]	$V_{DDEXTOSC}$ *SR*	4.5	5.0	5.5[2]	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid. 5V NVM programming range
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid. 3.3 V NVM programming range
External supply voltage for PMS, standby domains, standby pins and SCR	$V_{DDEVRSB}$ *SR*	4.5[4]	5	5.5[2]	V	
		2.97[4]	3.3	3.63	V	

(table continues...)

Table 59 (continued) Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for ADC modules and ANx analog and class S input pins with respect to VSSM	V_{DDM} *SR*	4.5	5.0	5.5[2)]	V	Nominal ADC supply voltage range. ADC 5 V parameters are valid
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. Degraded ADC parameters are valid (see TMADC 5V chapter)
		2.97	3.3	3.63	V	Nominal ADC supply voltage range. Degraded ADC parameters are valid (see TMADC 5V chapter)
External supply voltage for xSPI Interface, Ethernet RGMII module and other Port 16 functions	V_{DDHSIF} *SR*	2.97	3.3	3.63[5)]	V	
		1.66	1.8	1.98	V	High performance case
External supply voltage for HSPHY module[6)]						
Supply Voltage for core logic (V_{DD}) at unloaded supply pin.[8)]	V_{DD} *SR*	0.943[9)]	1.025	1.128[10)]	V	V_{DD} (VID_CON.VDDNOM) setpoint value for slow and typical devices. V_{DD} setpoint value, if no voltage scaling possible (e.g. in case of fixed external supply voltage)
		0.897[9)]	0.975	1.073[10)]	V	V_{DD} (VID_CON.VDDNOM) setpoint value for fast devices
Supply Voltage for HSPHY core logic (V_{DDPHYx}) at unloaded supply pin						
Core ground supply	V_{SS} *SR*	0	-	-	V	
Analog ground supply V_{SSM}	V_{SSM} *CC*	-0.1	0	0.1	V	
Minimum external voltage to ensure defined pad states for $V_{DDEVRSB}$ supplied pins	V_{DDPPSB} *CC*	1.3[11)]	-	-	V	Default pad pull-up or tristate is ensured at respective $V_{DDEVRSB}$ supply level

(table continues...)

Table 59 (continued) Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum external voltage to ensure defined pad states for V_{DDEXT} supplied pins	V_{DDPPA} *CC*	1.3[11]	-	-	V	Default pad pull-up or tristate is ensured at respective V_{DDEXT} supply level

1) $V_{DDEXTDC}$ supply voltage is allowed to drop down to 2.8 V during device start-up cranking phase.
2) Voltage overshoot up to 6.5 V is permissible, provided that the duration is less than 2 h cumulated. ADC accuracy is reduced and leakage current is increased. The voltage life time profile limitations need to be considered.
3) $V_{DDEXTOSC}$ has to be connected to V_{DDEXT} on PCB
4) $V_{DDEVRSB}$ supply voltage is allowed to drop down to 2.76 V during device start-up and operation mode transitions, and to 2.6 V during standby modes.
5) Voltage overshoot up to 4.29 V is permissible, provided that the duration is less than 2 h cumulated.
6) If at least one HSPHYx module is used, all VDDPHPHYx and VDDPHYx supply rails in the device shall be supplied complying to operating range limits.
7) Voltage overshoot up to 2.4 V is permissible, provided that the duration is less than 2 h cumulated.
8) The V_{DD} voltage on the loaded VDD ball would be higher than that on the internal sense point indicated by the unloaded VDD_SENSE pin with respect to unloaded VSS_SENSE ball. The difference is attributed to the static and dynamic core voltage drop on the power distribution network. The loaded V_{DD} voltage is indicated by VDDPAD monitor and unloaded V_{DD} internal voltage is indicated by the VDD monitor respectively. It is expected that the external regulator static + dynamic voltage undershoot at unloaded VDD_SENSE point is limited to V_{DD} (Typ) - 6% as is documented in the max pattern current consumption use case to have adequate headroom for voltage monitoring and margin towards reset (VDDPRIUV limit).
9) For VDD VDDPRIUV (MIN) ≤ VDD < VDD (MIN) core logic operation is validated for patterns without additional load jumps to ensure device start-up. Analog performance of ADCs or HSPHYx are not being guaranteed. Operation at rated frequency is ensured in production test down to VDD VDDPRIUV reset limit at VDD sense point.
10) Voltage overshoot up to 1.2 V is permissible, provided that the duration is less than 2 h cumulated. ADC accuracy is reduced and leakage current is increased. The voltage life time profile limitations need to be considered.
11) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when V_{DDEXT} or $V_{DDEVRSB}$ has reached this level.

Related information

Clock operating conditions on page 413
Limitation of supply voltage over time on page 417
Temperature operating conditions on page 418
Example temperature profiles on page 419

4.4.3 Limitation of supply voltage over time

The maximum operation voltage for $V_{DDEXT/DDM}$ supply rails is limited over the complete lifetime.

***Note**: The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 60 Example voltage profile 1

$V_{DDEXT/DDM}$	Duration [h]
5.4 V < $V_{DDEXT/DDM}$ ≤ 5.5 V	≤ 5% of lifetime
5.15 V < $V_{DDEXT/DDM}$ ≤ 5.4 V	≤ 15% of lifetime
4.85 V < $V_{DDEXT/DDM}$ ≤ 5.15 V	≤ 60% of lifetime
4.6 V < $V_{DDEXT/DDM}$ ≤ 4.85 V	≤ 15% of lifetime

(table continues...)

Table 60 (continued) Example voltage profile 1

$V_{DDEXT/DDM}$	Duration [h]
4.5 V < $V_{DDEXT/DDM}$ ≤ 4.6 V	≤ 5% of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

***Note**: The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 61 Example voltage profile 2

V_{DD}	Duration [h]
$V_{DD, typ}$ - 3 % of $V_{DD, typ}$< V_{DD} ≤ $V_{DD, typ}$ + 3 % of $V_{DD, typ}$	≤ 90% of lifetime
Operating $V_{DD, min}$ < V_{DD} ≤ $V_{DD, typ}$ - 3 % of $V_{DD, typ}$ AND $V_{DD, typ}$ + 3 % of $V_{DD, typ}$ < V_{DD} ≤ Operating $V_{DD, max}$	≤ 10% of lifetime
Operating $V_{DD, max}$ < V_{DD} ≤ Absolute maximum $V_{DD, max}$	as documented in absolute maximum ratings section.

Related information

Clock operating conditions on page 413
Supply operating conditions on page 415
Temperature operating conditions on page 418
Example temperature profiles on page 419

4.4.4 Temperature operating conditions

Table 62 Temperature operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A *SR*	-40	-	105	°C	valid for all SAA products
		-40	-	125	°C	valid for all SAK products
Junction Temperature	T_J *SR*	-40	-	145[1)]	°C	valid for all SAA and SAK products

1) Operation is allowed up to T_J (Max) = 150°C provided DTS accuracy is included and duration of operation is limited by temperature and voltage lifetime profiles.

Related information

Clock operating conditions on page 413
Supply operating conditions on page 415
Limitation of supply voltage over time on page 417
Example temperature profiles on page 419

4.4.5 Example temperature profiles

***Note**: The following temperature profile is an example. Application specific temperature profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 63 Example temperature profile

T_J	Duration [h]	Comment
≤ 150°C	≤ 100	Device in RUN mode
≤ 145°C	≤ 400	Device in RUN mode
≤ 140°C	≤ 600	Device in RUN mode
≤ 115°C	≤ 5200	Device in RUN mode
≤ 105°C	≤ 23500	Device in RUN mode
≤ 90°C	≤ 18000	Device in RUN mode
≤ 85°C	≤ 12500	Device in RUN mode
≤ 20°C	≤ 3100	Device in RUN mode
	≤ 63400	Total operational lifetime

Table 64 Example inactive lifetime temperature profile

T_J	Duration [h]	Comment
≤ 20°C	≤ 68000	Device in Standby 0 mode or is switched off
≤ 20°C	≤ 43800	Device is switched off
	≤ 111800	Total inactive lifetime

Related information

Clock operating conditions on page 413
Supply operating conditions on page 415
Limitation of supply voltage over time on page 417
Temperature operating conditions on page 418
Pin reliability in overload on page 410

4.5 Switchable pad characteristics

The pad classes Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.1 ¬ PORST Pad characteristics

Table 65 ¬ PORST Pad characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PORST pad output current[1]	I_{PORST} CC	13	-	-	mA	V_{DDEXT} = 2.97 V; V_{PORST} = 0.9 V
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} CC	263	-	-	ns	Without additional PORST Digtial Filter active (PORSTDF = 0)
Input high voltage level	V_{IH} SR	1.4	-	-	V	V_{DDEXT} = 2.97 V
		2.0	-	-	V	TTL; V_{DDEXT} = 4.5 V
Input low voltage level	V_{IL} SR	-	-	0.5	V	V_{DDEXT} = 2.97 V
		-	-	0.8	V	TTL; V_{DDEXT} = 4.5 V
Input hysteresis[2]	HYS CC	0.026 * V_{DDEXT}	-	-	V	None of the neighbour pads are used as output
Pull-down current[3] [1]	I_{PDL} CC	|15|	-	-	µA	V_{IL}; V_{DDEXT} = 2.97 V
		-	-	|130|	µA	V_{IH}; TTL
Input leakage current	I_{OZ} CC	-900	-	900	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDEXT}) < V_{IN} < (0.9 * V_{DDEXT})
		-950	-	950	nA	$T_J \le T_J$ (Max); else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added

1) It is recommended that PORST pin shall be externally pulled high with a pull-up resistor in the range 1.4 kΩ up to 6.4 kΩ.
2) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

5 V switchable pad characteristics on page 421
3.3 V switchable pad characteristics on page 427
1.8 V switchable pad characteristics on page 439
Class D characteristics on page 441
ADC reference pads characteristics on page 442
Driver mode selection for slow and fast pads on page 443

4.5.2 5 V switchable pad characteristics

The pad classes Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

Related information

¬ PORST Pad characteristics on page 420
3.3 V switchable pad characteristics on page 427
1.8 V switchable pad characteristics on page 439
Class D characteristics on page 441
ADC reference pads characteristics on page 442
Driver mode selection for slow and fast pads on page 443

4.5.2.1 Fast 5V GPIO characteristics

Table 66 Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} *CC*	100	225	295	Ohm	Driver = medium; $I_{OH\,/\,OL}$ = 2 mA
		31	55	80	Ohm	Driver = strong; $I_{OH\,/\,OL}$ = 8 mA
Rise / Fall time[1)]	t_{RF} *CC*	1.6	-	3.2	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}
		4+0.55* C_L	4+0.75* C_L	12+1.0* C_L	ns	Driver = medium; $C_L \le 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		1.0+0.18 *C_L	2.5+0.27 *C_L	5.0+0.37 *C_L	ns	Driver = strong, edge = medium; $C_L \le 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		0.5+0.08 *C_L	0.5+0.11 *C_L	1.0+0.17 *C_L	ns	Driver = strong, edge = sharp; $C_L \le 200$ pF; measured from 10 % to 90 % of V_{DDIO}
Asymmetry of sending[2)]	t_{TX_ASYM} *CC*	-1	-	1	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.44 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL

(table continues...)

Table 66 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input low threshold variation	V_{ILD} *SR*	-95	-	95	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[3)]	*HYS CC*	0.09 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.06 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		210[4)]	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[5)]	I_{PUH} *CC*	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Equivalent resistance to pull-up device	R_{PUH} *CC*	30	-	42	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; Automotive level
		56	-	78	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; TTL level
Pull-down current[6)]	I_{PDL} *CC*	|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
		-	-	|130|	µA	V_{IH}; AL or TTL
Equivalent resistance to pull-down device	R_{PDL} *CC*	43	-	58	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; Automotive level
		18	-	25	kOhm	$0.1*V_{DDIO} \le V_{IN} \le V_{DDIO}$; TTL level

(table continues...)

Table 66 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-3000	-	3000	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})
		-3700	-	3700	nA	$T_J \le T_J$ (Max); else
		-2400	-	2400	nA	$T_J \le T_J$ (Max); (0.1 * $V_{DDEXT/DDEXTHS}$) < V_{IN} < (0.9 * $V_{DDEXT/DDEXTHS}$); LVDS_RX / Fast pad type
		-10100	-	10100	nA	$T_J \le T_J$ (Max); LVDS_RX / Fast pad type; else
		-3300	-	3300	nA	$T_J \le T_J$ (Max); (0.1 * $V_{DDEXT/DDEXTHS}$) < V_{IN} < (0.9 * $V_{DDEXT/DDEXTHS}$); LVDS_TX / Fast pad type
		-4300	-	4300	nA	$T_J \le T_J$ (Max); LVDS_TX / Fast pad type; else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) This parameter defines the difference of the output signal delay parameter for rising and falling edge
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) For Pin P01.14 the Min value is 165 mV.
5) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
6) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Slow 5V GPIO characteristics on page 424
Class S 5V characteristics on page 425

4.5.2.2 Slow 5V GPIO characteristics

Table 67 Slow 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} *CC*	100	225	295	Ohm	Driver = medium; $I_{OH\,/\,OL}$ = 2 mA
Rise / Fall time[1)]	t_{RF} *CC*	4+0.55* C_L	4+0.75* C_L	12+1*C_L	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		1.5+0.25 *C_L	2.5+0.40 *C_L	7+0.55* C_L	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
Asymmetry of sending[2)]	t_{TX_ASYM} *CC*	-1.3	-	1.3	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.44 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-100	-	100	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[3)]	*HYS CC*	0.09 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.058 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		210	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[4)]	I_{PUH} *CC*	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current[5)]	I_{PDL} *CC*	|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
		-	-	|130|	µA	V_{IH}; AL or TTL

(table continues...)

Table 67 (continued) Slow 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} *CC*	-1200	-	1200	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO}); no analog input
		-1500	-	1500	nA	$T_J \le T_J$ (Max); no analog input; else
		-2000	-	2000	nA	$T_J \le T_J$ (Max); (0.1 * $V_{DDEXT/DDFLEX}$) < V_{IN} < (0.9 * $V_{DDEXT/DDFLEX}$); $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-2400[6]	-	2400[6]	nA	$T_J \le T_J$ (Max); $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) This parameter defines the difference of the output signal delay parameter for rising and falling edge
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.
6) For ($V_{IN} > V_{DDM}$) or ($V_{IN} < V_{SSM}$) leakage is doubled.

Related information

Fast 5V GPIO characteristics on page 421
Class S 5V characteristics on page 425

4.5.2.3 Class S 5V characteristics

Table 68 Class S 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL

(table continues...)

Table 68 (continued) Class S 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} *SR*	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDM} = constant; AL
Input hysteresis[1]	*HYS CC*	0.09 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; AL
		0.06 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		290	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[2]	I_{PUH} *CC*	|30|	-	-	µA	V_{IH}; AL and TTL
		-	-	|130|	µA	V_{IL}; AL and TTL
Pull-down current[3]	I_{PDL} *CC*	|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
		-	-	|130|	µA	V_{IH}; AL and TTL
Input leakage current	I_{OZ} *CC*	-800	-	800	nA	$T_J \le T_J$ (Max); PDD option available
		-300	-	300	nA	$T_J \le T_J$ (Max); else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Fast 5V GPIO characteristics on page 421
Slow 5V GPIO characteristics on page 424

4.5.3 3.3 V switchable pad characteristics

Pad classes as Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

Related information

¬ PORST Pad characteristics on page 420
5 V switchable pad characteristics on page 421
1.8 V switchable pad characteristics on page 439
Class D characteristics on page 441
ADC reference pads characteristics on page 442
Driver mode selection for slow and fast pads on page 443

4.5.3.1 HSFast 3.3V GPIO characteristics

Table 69 HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} *CC*	125	225	320	Ohm	P16_PCSRSEL.PCSRx = 0; Driver = medium; $I_{OH\,/\,OL}$ = 2 mA
		31	55	80	Ohm	P16_PCSRSEL.PCSRx = 0; Driver = strong; $I_{OH\,/\,OL}$ = 8 mA

(table continues...)

Table 69 (continued) HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pad output impedance	*Z CC*	22.5	30	41.0	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$
		24.75	33	44.50	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $001_{(2)}$
		28.5	38	49.5	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $010_{(2)}$
		32.25	43	55.50	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $011_{(2)}$
		37.5	50	64.0	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $100_{(2)}$
		45	60	75	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $101_{(2)}$
		75	100	125	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $110_{(2)}$
		112.5	150	187.5	Ohm	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $111_{(2)}$

(table continues...)

Table 69 (continued) HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise / Fall time[1)]	t_{RF} CC	1.6	-	4.5	ns	P16_PCSRSEL.PCSRx = 0; C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDHSIF}
		2+0.57* C_L	5.5+0.75 *C_L	10+1.25 *C_L	ns	P16_PCSRSEL.PCSRx = 0; Driver = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDHSIF}
		1.5+0.18 *C_L	1.5+0.28 *C_L	8+0.4*C_L	ns	P16_PCSRSEL.PCSRx = 0; Driver = strong, edge = medium; measured from 10 % to 90 % of V_{DDHSIF}
		0.75+0.08*C_L	0.75+0.11*C_L	2.5+0.21 *C_L	ns	P16_PCSRSEL.PCSRx = 0; Driver = strong, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDHSIF}
		-	-	5	ns	P16_PCSRSEL.PCSRx = 0; C_L = 25 pF; driver = strong, edge = sharp; measured from 0.8 V to 2.0 V
		-	-	4.85	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $111_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	5.10	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $111_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V [2)]
		-	-	3.20	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $110_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	3.40	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $110_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V

(table continues...)

Table 69 (continued) HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
						2)
		-	-	2.00	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $101_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	2.20	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $101_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V 2)
		-	-	1.75	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $100_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	1.90	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $100_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V 2)
		-	-	1.50	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $011_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	1.65	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $011_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V 2)
		-	-	1.30	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $010_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	1.44	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $010_{(2)}$; C_L = 15 pF; measured

(table continues...)

Table 69 (continued) HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
						from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V 2)
		-	-	1.10	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $001_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	1.20	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $001_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V 2)
		-	-	0.96	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.97 V
		-	-	1.0	ns	P16_PCSRSEL.PCSRx = 1; PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 2.7 V 2)
Asymmetry of sending	t_{TX_ASYM} *CC*	-0.4	-	0.4	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input frequency	f_{IN} *CC*	-	-	160	MHz	AL and TTL configuration
		-	-	200	MHz	xSPI modes and RGMII mode configuration
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDHSIF}	-	-	V	AL
		2.0	-	-	V	TTL
		1.89	-	-	V	xSPI modes and RGMII mode
Input low voltage level	V_{IL} *SR*	-	-	0.42 * V_{DDHSIF}	V	AL
		-	-	0.8	V	TTL
		-	-	1.08	V	xSPI modes and RGMII mode

(table continues...)

Table 69 (continued) HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input low threshold variation	V_{ILD} *SR*	-44	-	44	mV	Max. variation of 1 ms; V_{DDHSIF} = constant; AL
Input hysteresis[3)]	*HYS CC*	0.055 * V_{DDHSIF}	-	-	V	None of the neighbour pads are used as output; AL
		0.085 * V_{DDHSIF}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[4)]	I_{PUH} *CC*	|19|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		|20|	-	-	µA	V_{IH}; AL configuration in xSPI modes and RGMII mode
		|13|	-	-	µA	V_{IH}; TTL configuration in xSPI modes and RGMII mode
		-	-	|80|	µA	V_{IL}; AL and TTL
		-	-	|100|	µA	V_{IL}; AL configuration in xSPI modes and RGMII mode
		-	-	|70|	µA	V_{IL}; TTL configuration in xSPI modes and RGMII mode
Pull-down current[5)]	I_{PDL} *CC*	|19|	-	-	µA	V_{IL}; AL and TTL
		|17|	-	-	µA	V_{IL}; AL configuration in xSPI modes and RGMII mode
		|34|	-	-	uA	V_{IL}; TTL configuration in xSPI modes and RGMII mode
		-	-	|115|	µA	V_{IH}; TTL
		-	-	|60|	µA	V_{IH}; AL configuration in xSPI modes and RGMII mode
		-	-	|110|	uA	V_{IH}; TTL configuration in xSPI modes and RGMII mode
Input leakage current	I_{OZ} *CC*	-3000	-	3000	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDHSIF}) < V_{IN} < (0.9 * V_{DDHSIF})
		-4000	-	4000	nA	$T_J \le T_J$ (Max); else

(table continues...)

Table 69 (continued) HSFast 3.3V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pin capacitance	C_{IO} *CC*	-	2	3.5	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) Supply voltage of V_{DDHSIF} (Min) = 2.7 V corresponds to a NOR Flash use case with V_{DDHSIF} (Typ) = 3.0 V
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

Fast 3.3V GPIO characteristics on page 433
Slow 3.3V GPIO characteristics on page 436
Class S 3.3V characteristics on page 437

4.5.3.2 Fast 3.3V GPIO characteristics

Table 70 Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} *CC*	125	225	320	Ohm	Driver = medium; $I_{OH\,/\,OL}$ = 2 mA
		31	55	80	Ohm	Driver = strong; $I_{OH\,/\,OL}$ = 8 mA

(table continues...)

Table 70 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise / Fall time[1)]	t_{RF} *CC*	1.6	-	4.5	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}
		2+0.57* C_L	5.5+0.75 *C_L	10+1.25 *C_L	ns	Driver = medium; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		1.5+0.18 *C_L	1.5+0.28 *C_L	8+0.43* C_L	ns	Driver = strong, edge = medium; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		0.75+0.08*C_L	0.75+0.11*C_L	2.5+0.21 *C_L	ns	Driver = strong, edge = sharp; C_L ≤ 200 pF; measured from 10 % to 90 % of V_{DDIO}
		-	-	5	ns	C_L = 25 pF; driver = strong, edge = sharp; measured from 0.8 V to 2.0 V (RMII)
Asymmetry of sending[2)]	t_{TX_ASYM} *CC*	-1	-	1	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.42 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[3)]	*HYS CC*	0.055 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.081 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL

(table continues...)

Table 70 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up current[4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL
Pull-down current[5]	I_{PDL} CC	|19|	-	-	µA	V_{IL}; AL and TTL
		-	-	|105|	µA	V_{IH}; AL
		-	-	|115|	µA	V_{IH}; TTL
Input leakage current	I_{OZ} CC	-2000	-	2000	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})
		-2100	-	2100	nA	$T_J \le T_J$ (Max); else
		-1500	-	1500	nA	$T_J \le T_J$ (Max); (0.1 * $V_{DDEXT/DDEXTHS}$) < V_{IN} < (0.9 * $V_{DDEXT/DDEXTHS}$); LVDS_RX / Fast pad type
		-5700	-	5700	nA	$T_J \le T_J$ (Max); LVDS_RX / Fast pad type; else
		-2000	-	2000	nA	$T_J \le T_J$ (Max); (0.1 * $V_{DDEXT/DDEXTHS}$) < V_{IN} < (0.9 * $V_{DDEXT/DDEXTHS}$); LVDS_TX / Fast pad type
		-2500	-	2500	nA	$T_J \le T_J$ (Max); LVDS_TX / Fast pad type; else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) This parameter defines the difference of the output signal delay parameter for rising and falling edge
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise
4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

HSFast 3.3V GPIO characteristics on page 427
Slow 3.3V GPIO characteristics on page 436
Class S 3.3V characteristics on page 437

4.5.3.3 Slow 3.3V GPIO characteristics

Table 71 Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} *CC*	125	225	320	Ohm	Driver = medium; $I_{OH\,/\,OL}$ = 2 mA
Rise / Fall time[1)]	t_{RF} *CC*	2+0.57* C_L	5.5+0.75 *C_L	10+1.25 *C_L	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		2+0.30* C_L	3.5+0.50 *C_L	5+0.70* C_L	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
Asymmetry of sending[2)]	t_{TX_ASYM} *CC*	-1.3	-	1.3	ns	C_L = 15 pF; valid for all data rates excluding clock tolerance
Input frequency	f_{IN} *CC*	-	-	160	MHz	
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.42 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDIO} = constant; AL
Input hysteresis[3)]	*HYS CC*	0.055 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.081 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current[4)]	I_{PUH} *CC*	|17|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL

(table continues...)

Table 71 (continued) Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-down current[5]	I_{PDL} CC	|19|	-	-	µA	V_{IL}; AL and TTL
		-	-	|105|	µA	V_{IH}; AL
		-	-	|115|	µA	V_{IH}; TTL
Input leakage current	I_{OZ} CC	-750	-	750	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO}); no analog input
		-1100	-	1100	nA	$T_J \le T_J$ (Max); no analog input; else
		-1200	-	1200	nA	$T_J \le T_J$ (Max); (0.1 * $V_{DDEXT/DDFLEX}$) < V_{IN} < (0.9 * $V_{DDEXT/DDFLEX}$); $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-1400[6]	-	1400[6]	nA	$T_J \le T_J$ (Max); $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
2) This parameter defines the difference of the output signal delay parameter for rising and falling edge
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.
6) For ($V_{IN} > V_{DDM}$) or ($V_{IN} < V_{SSM}$) leakage is doubled.

Related information

HSFast 3.3V GPIO characteristics on page 427
Fast 3.3V GPIO characteristics on page 433
Class S 3.3V characteristics on page 437

4.5.3.4 Class S 3.3V characteristics

Table 72 Class S 3.3V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	

(table continues...)

Table 72 (continued) Class S 3.3V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} *SR*	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} *SR*	-70	-	70	mV	Max. variation of 1 ms; V_{DDM} = constant; AL
Input hysteresis[1]	*HYS CC*	0.055 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; AL
		0.085 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
Pull-up current[2]	I_{PUH} *CC*	|17|	-	-	µA	V_{IH}; AL
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL
Pull-down current[3]	I_{PDL} *CC*	|19|	-	-	µA	V_{IL}; AL and TTL
		-	-	|105|	µA	V_{IH}; AL
		-	-	|115|	µA	V_{IH}; TTL
Input leakage current	I_{OZ} *CC*	-600	-	600	nA	$T_J \le T_J$ (Max); PDD option available
		-300	-	300	nA	$T_J \le T_J$ (Max); else
Pin capacitance	C_{IO} *CC*	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} *CC*	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

HSFast 3.3V GPIO characteristics on page 427
Fast 3.3V GPIO characteristics on page 433
Slow 3.3V GPIO characteristics on page 436

4.5.4 1.8 V switchable pad characteristics

Related information

¬ PORST Pad characteristics on page 420
5 V switchable pad characteristics on page 421
3.3 V switchable pad characteristics on page 427
Class D characteristics on page 441
ADC reference pads characteristics on page 442
Driver mode selection for slow and fast pads on page 443

4.5.4.1 HSFast 1.8V GPIO characteristics

Table 73 HSFast 1.8V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pad output impedance	*Z CC*	22.5	30	39.1	Ohm	PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$
		24.75	33	42.80	Ohm	PADCFG.DRVCFG.PD [2:0] = $001_{(2)}$
		28.5	38	47.5	Ohm	PADCFG.DRVCFG.PD [2:0] = $010_{(2)}$
		32.25	43	53.75	Ohm	PADCFG.DRVCFG.PD [2:0] = $011_{(2)}$
		37.5	50	62.5	Ohm	PADCFG.DRVCFG.PD [2:0] = $100_{(2)}$
		45	60	75	Ohm	PADCFG.DRVCFG.PD [2:0] = $101_{(2)}$
		75	100	125	Ohm	PADCFG.DRVCFG.PD [2:0] = $110_{(2)}$
		112.5	150	206	Ohm	PADCFG.DRVCFG.PD [2:0] = $111_{(2)}$

(table continues...)

Table 73 (continued) HSFast 1.8V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise / Fall time	t_{RF} *CC*	-	-	1.82	ns	PADCFG.DRVCFG.PD [2:0] = $101_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	2.76	ns	PADCFG.DRVCFG.PD [2:0] = $110_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	4.55	ns	PADCFG.DRVCFG.PD [2:0] = $111_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	1.70	ns	PADCFG.DRVCFG.PD [2:0] = $100_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	1.36	ns	PADCFG.DRVCFG.PD [2:0] = $011_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	1.20	ns	PADCFG.DRVCFG.PD [2:0] = $010_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	1.10	ns	PADCFG.DRVCFG.PD [2:0] = $001_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
		-	-	0.91	ns	PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$; C_L = 15 pF; measured from 0.2 * V_{DDHSIF} to 0.8 * V_{DDHSIF}; V_{DDHSIF} = 1.7 V
Asymmetry of sending	t_{TX_ASYM} *CC*	-1	-	1	ns	
Input frequency	f_{IN} *CC*	-	-	200	MHz	xSPI modes and RGMII mode configuration
Input high voltage level	V_{IH} *SR*	0.7 * V_{DDHSIF}	-	V_{DDHSIF} + 0.3	V	
Input low voltage level	V_{IL} *SR*	- 0.3	-	0.3 * V_{DDHSIF}	V	

(table continues...)

Table 73 (continued) HSFast 1.8V GPIO characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up current	I_{PUH} CC	|10|	-	-	µA	V_{IH}; AL configuration in xSPI modes and RGMII mode
		|5|	-	-	µA	V_{IH}; TTL configuration in xSPI modes and RGMII mode
		-	-	|50|	µA	V_{IL}; AL configuration in xSPI modes and RGMII mode
		-	-	|35|	µA	V_{IL}; TTL configuration in xSPI modes and RGMII mode
Pull-down current	I_{PDL} CC	|8|	-	-	µA	V_{IL}; AL configuration in xSPI modes and RGMII mode
		|16|	-	-	µA	V_{IL}; TTL configuration in xSPI modes and RGMII mode
		-	-	|40|	µA	V_{IH}; AL configuration in xSPI modes and RGMII mode
		-	-	|80|	µA	V_{IH}; TTL configuration in xSPI modes and RGMII mode
Input leakage current	I_{OZ} CC	-3000	-	3000	nA	$T_J \le T_J$ (Max); (0.1 * V_{DDHSIF}) < V_{IN} < (0.9 * V_{DDHSIF})
		-4000	-	4000	nA	$T_J \le T_J$ (Max); else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

4.5.5 Class D characteristics

Table 74 Class D characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-800	-	800	nA	$T_J \le T_J$ (Max); PDD option available
		-600	-	600	nA	$T_J \le T_J$ (Max) ; valid for AN9, AN10, AN34, AN35
		-80	-	80	nA	$T_J \le T_J$ (Max); else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added

Related information

¬ PORST Pad characteristics on page 420
5 V switchable pad characteristics on page 421
3.3 V switchable pad characteristics on page 427
1.8 V switchable pad characteristics on page 439
ADC reference pads characteristics on page 442
Driver mode selection for slow and fast pads on page 443

4.5.6 ADC reference pads characteristics

Table 75 ADC reference pads characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} *CC*	-4[1)]	-	4[1)]	µA	$T_J \le T_J$ (Max); $V_{AREF} \le V_{DDM}$; used for TMADC; valid for BGA436 & BGA292
		-14[1)]	-	14[1)]	µA	$T_J \le T_J$ (Max); $V_{AREF} \le V_{DDM}$ + 50 mV; used for TMADC; valid for BGA436 & BGA292

1) Limit is valid for VAREF2 pin.

Related information

¬ PORST Pad characteristics on page 420
5 V switchable pad characteristics on page 421
3.3 V switchable pad characteristics on page 427
1.8 V switchable pad characteristics on page 439
Class D characteristics on page 441
Driver mode selection for slow and fast pads on page 443

4.5.7 Driver mode selection for slow and fast pads

Table 76 Driver mode selection for Slow pads

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium edge (m)

Table 77 Driver mode selection for Fast pads or HSFast pads

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium edge (m)
X	1	1	Speed grade 4	Reserved. ***Note**: Do not use this combination!*

Table 78 Driver mode selection for HSFast pads valid for RGMII and xSPI configuration (applicable if PCSRSEL bitfield of the corresponding port slice is set to one)

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
0	0	0	Impedance setting 0	Output impedance value see datasheet HSFast pad type specification
0	0	1	Impedance setting 1	Output impedance value see datasheet HSFast pad type specification
0	1	0	Impedance setting 2	Output impedance value see datasheet HSFast pad type specification
0	1	1	Impedance setting 3	Output impedance value see datasheet HSFast pad type specification
1	0	0	Impedance setting 4	Output impedance value see datasheet HSFast pad type specification
1	0	1	Impedance setting 5	Output impedance value see datasheet HSFast pad type specification
1	1	0	Impedance setting 6	Output impedance value see datasheet HSFast pad type specification
1	1	1	Impedance setting 7	Output impedance value see datasheet HSFast pad type specification

Related information

¬ PORST Pad characteristics on page 420
5 V switchable pad characteristics on page 421
3.3 V switchable pad characteristics on page 427
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4.6 High performance LVDS pad characteristic

This LVDS pad type is used for the high speed chip to chip communication interface of the new TC4DxAA-step COM. It is composed out of an LVDS pad and a fast pad.

C_L = 2.5 pF for all LVDS parameters.

***Note**:* *Driver ground potential difference is defined as driver-receiver potential difference, that can result in a voltage shift when comparing the driver output voltage level and the receiver input voltage level of a transmitted signal.*

***Note**:* *R_T in table 'LVDS - IEEE standard LVDS general purpose Link (GPL)' is as termination resistor of the receiver according to figure 3-5 in IEEE Std 1596.3-1996 and is represented in either by R_{IN} or by $R_T = 100\Omega$ but not both.*

***Note**:* *Default after start-up = CMOS function*

4.6.1 LVDS - IEEE standard LVDS general purpose link (GPL)

Table 79 LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Driver dc characteristics						
Output voltage high	V_{oh} *CC*	-	-	1475	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 00 and 01
		-	-	1500	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 10 and 11
Output voltage low	V_{ol} *CC*	925	-	-	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 00 and 01
		900	-	-	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 10 and 11
Output differential voltage	V_{od} *CC*	380	-	500	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 11; Multi slave operation
		240	-	330	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 00
		280	-	370	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 01
		320	-	410	mV	R_T = 100 Ohm ± 1%; LPCRx.VDIFFADJ = 10
Output differential voltage in Sleep Mode[1)]	V_{ODSM} *CC*	-5	-	20	mV	R_T = 100 Ohm ± 20%; LPCRx.VDIFFADJ = xx
Output offset (Common mode) voltage	V_{os} *CC*	1125	-	1275	mV	R_T = 100 Ohm ± 1%

(table continues...)

Table 79 (continued) LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output impedance	R_o *CC*	40	-	140	Ohm	
Delta output impedance	dR_o *SR*	-	-	10	%	
Change in V_{OD} between 0 and 1	dV_{od} *CC*	-	-	25	mV	R_T = 100 Ohm ± 1%
Change in V_{OS} between 0 and 1	dV_{os} *CC*	-	-	25	mV	R_T = 100 Ohm ± 1%
Driver ac characteristics						
Duty cycle	t_{duty} *CC*	45	-	55	%	
Fall time (20% - 80%)	t_{fall20} *CC*	-	-	0.75[2)]	ns	Z_L = 100 Ohm ± 20% at 2 pF external load
Rise time (20% - 80%)	t_{rise20} *CC*	-	-	0.75[3)]	ns	Z_L = 100 Ohm ± 20% at 2 pF external load
Receiver dc characteristics						
Input voltage range	V_i *SR*	0	-	1600	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ± 10%
		0	-	2000	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ± 20%
Input differential threshold	V_{idth} *SR*	-100	-	100	mV	Driver ground potential difference < 925 mV
Receiver differential input impedance	R_{in} *CC*	80	-	120	Ohm	V_I ≤ 2400 mV
Receiver ac characteristics						
Pad setup time	t_{SET_LVDS} *CC*	-	10	13	µs	

1) Common Mode voltage of TX is maintained
2) t_{fall20} = 0.75 ns + (C_L - 2)[pF]*20 ps. C_L defines the external load.
3) t_{rise20} = 0.75 ns + (C_L - 2)[pF]*20 ps. C_L defines the external load.

Related information

LVDS pad input model on page 446

4.6.2 LVDS pad input model

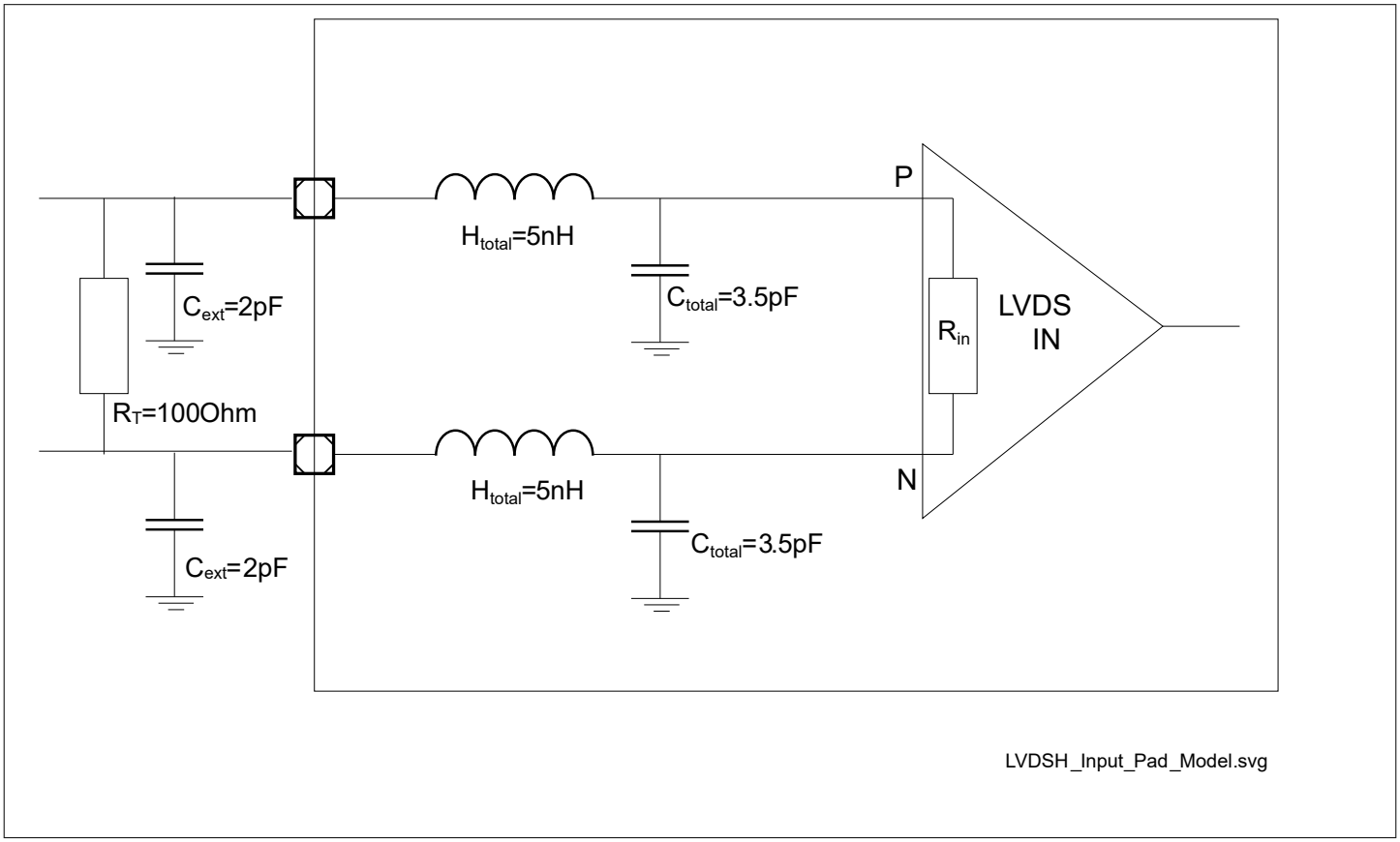


Figure 3 LVDS pad input model

Related information

LVDS - IEEE standard LVDS general purpose link (GPL) on page 444

4.7 TMADC characteristics

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of (V_{AREF} - V_{AGND}) ≥ 4.5 V.

If the reference voltage range is below 4.5 V, for example 3.3 V, the accuracy parameter values increase by a factor of 1.1 / k, where k = 3.3 V / 4.5 V. If TUE is specified with ±4 LSB_{12} at 4.5 V the corresponding value at 3.3 V will be: 4 LSB_{12} × (1.1 × 4.5 V / 3.3 V) = 6 LSB_{12} → ±6 LSB_{12}.

***Note**: Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).*

***Note**: Digital functions overlapping analog inputs influence accuracy.*

***Note**: The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and EN_{RMS} = 1.0 the additional peak-peak noise error is ±(4 × 1.0) = 8 LSB_{12}.*

4.7.1 TMADC 5V characteristics

Table 80 TMADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC internal regulator characteristics						
TMADC IVR output voltage	V_{DDK} *CC*	-	2.4	-	V	
Deviation of IVR output voltage V_{DDK}	dV_{DDK} *CC*	-2.0	-	2.0	%	Based on device-specific value
TMADC reference voltage characteristics						
Analog reference voltage	V_{AREF} *SR*	V_{DDM} - 0.1	V_{DDM}	V_{DDM} + 0.05[1)]	V	2.97 V ≤ V_{DDM} ≤ 5.5 V
Negative reference voltage[2)]	V_{AGND} *SR*	V_{SSM} - 0.05	V_{SSM}	V_{SSM} + 0.05	V	V_{SSM} and V_{AGND} are connected together
Reference input charge consumption per conversion (from V_{AREF})[3)]	Q_{CONV} *CC*	-	-	10	pC	
TMADC accuracy						
Total Unadjusted Error[4) 5) 6) 7) 8)]	*TUE CC*	-4	-	4	LSB	12-bit resolution DC input; 4.5 V ≤ V_{DDM} ≤ 5.5 V
Integral Non-linearity[4) 5) 8)]	EA_{INL} *CC*	-3	-	3	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
Differential Non-linearity[4) 5) 9) 8)]	EA_{DNL} *CC*	-1	-	2	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
Gain error[4) 5) 8)]	EA_{GAIN} *CC*	-4	-	4	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
Offset[4) 5) 6) 8)]	EA_{OFF} *CC*	-4	-	4	LSB	4.5 V ≤ V_{DDM} ≤ 5.5 V
RMS Noise[4) 5) 6) 10) 11) 12) 7)]	EN_{RMS} *CC*	-	0.5	1	LSB	12bit resolution DC input

(table continues...)

Table 80 (continued) TMADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC input characteristics						
Analog input voltage range	V_{AIN} *SR*	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Analog input charge consumption[13)]	Q_{AINS} *CC*	-	-	3.0	pC	
TMADC timing						
Converter reference clock[14)]	f_{ADCI} *SR*	-	-	80	MHz	4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	40	MHz	2.97 V ≤ V_{DDM} < 4.5 V
Conversion time (excluding sample and hold time)	t_{CONV} *CC*	16	-	16	cycles	Measured between two conversion start-points, thus these numbers are valid for pipelined conversions [15)]
Sampling time	t_{mstc} *SR*	50	-	-	ns	Valid for the continous conversion mode; 4.5 V ≤ V_{DDM} ≤ 5.5 V
		100	-	-	ns	Valid for the continous conversion mode; 2.97 V ≤ V_{DDM} < 4.5 V
		100	-	-	ns	Valid for a single conversion; 4.5 V ≤ V_{DDM} ≤ 5.5 V
		200	-	-	ns	Valid for a single conversion; 2.97 V ≤ V_{DDM} < 4.5 V
Sampling time monitor channel	t_{mmstc} *SR*	1	-	-	µs	
Calibration time	t_{CAL} *CC*	-	-	3	ms	Valid for power up calibration and recalibration; 4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	6	ms	Valid for power up calibration and recalibration; 2.97 V ≤ V_{DDM} < 4.5 V
Hold Time for pending Sample	t_{HOLD} *SR*	-	-	3	µs	4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	6	µs	2.97 V ≤ V_{DDM} < 4.5 V

(table continues...)

Table 80 (continued) TMADC 5V characteristics

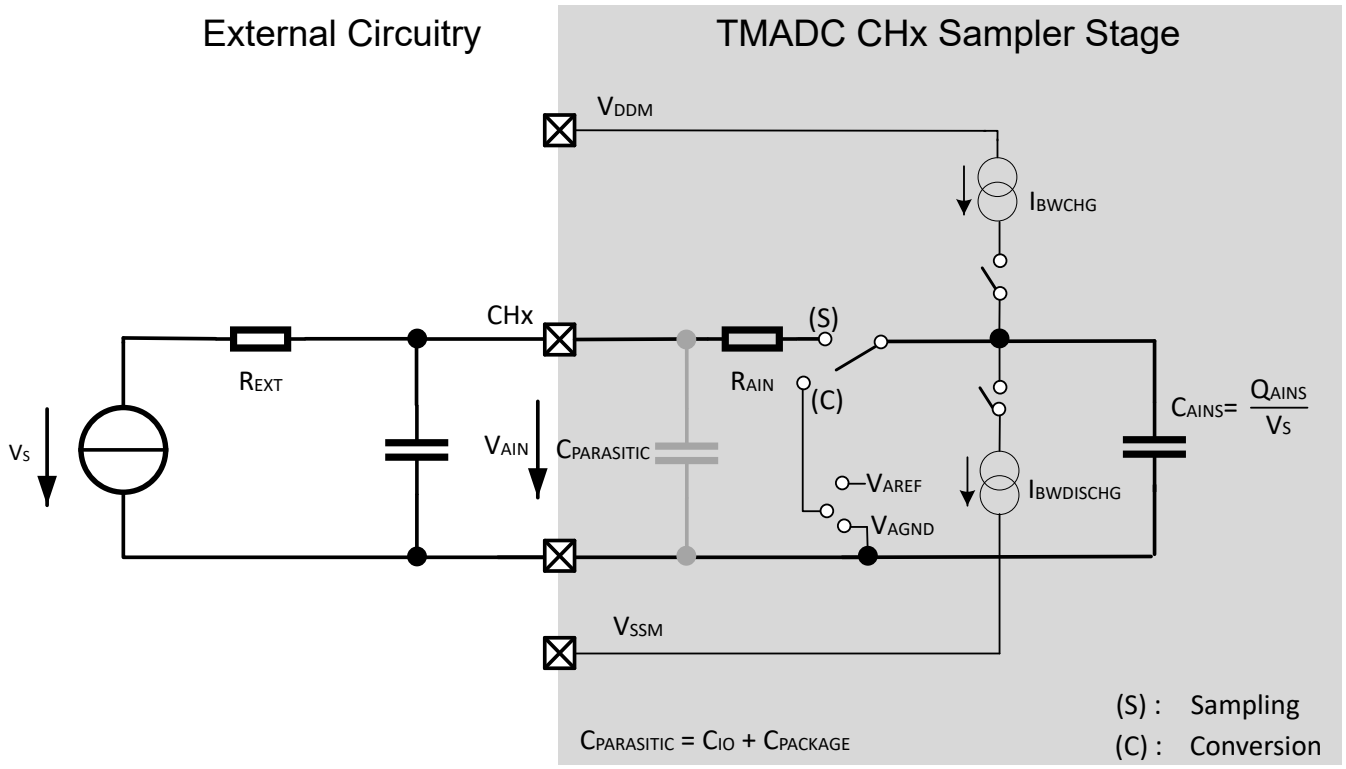
Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Wakeup time	t_{WUDIS} *CC*	-	-	8	µs	From module disable state (MODCFG.RUN set from zero to one); 4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	-	15	µs	From module disable state (MODCFG.RUN set from zero to one); 2.97 V ≤ V_{DDM} < 4.5 V
TMADC diagnosis characteristics						
Converter diagnostics voltage accuracy	dV_{CSD} *CC*	-1	-	1	%	Referred to V_{DDM}
Resistance of the pull-down test device[16]	R_{PDD} *CC*	-	-	0.3	kOhm	Measured at pad input voltage V_{IN} = V_{DDM} / 2
Broken wire detection charge current	I_{BWCHG} *CC*	5	10	15	µA	
Broken wire detection discharge current	$I_{BWDISCHG}$ *CC*	5	10	15	µA	

1) For V_{DDM} = 5.5 V the valid Max. value is 5.5 V
2) VAGND shall be directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball)
3) Parameter is valid for the typical value of V_{AREF}-V_{AGND}. If a reduced V_{AREF}-V_{AGND} voltage is used this parameter will decrease linearly.
4) This parameter is valid for V_{AREF}-V_{AGND} equal or higher than the typical value * 0.9. If a reduced V_{AREF}-V_{AGND} voltage is used this parameter can increase. If V_{AREF}-V_{AGND} is reduced with the factor k (k is the quotient build out of the reduced reference voltage and the 4.5 V), the parameter will increase with 1.1/k. e.g., k = 3.3 V/4.5 V = 0.73 → 1.1/k = 1.5 → 1.5 * TUE: 6 LSB at 3.3 V reference
5) This parameter is only guaranteed with a maximum supply voltage ripple on VDDM / VSSM of 20 mVpp in a frequency band from 1 kHz to 10 MHz. Supply voltage ripples above 10 MHz must be smaller than 5 mV. This must be guaranteed by high quality power supply sources and proper blocking capacitors
6) This parameter is valid for analog inputs within Pads not sharing digital functions. Parameter for analog inputs sharing digital functions (pad type Slow and Fast) will increase by 3 LSB
7) Resulting worst case combined error is arithmetic combination of *TUE* and user-defined distribution of EN_{RMS}
8) Start-up calibration is a prerequisite to achieve TMADC accuracy specification. It needs to be repeated when channel to SAR-core mapping is changed. Refer to user manual TMADC chapter "Module start-up calibration" for details.
9) Monotonic characteristic, no missing codes (after calibration)
10) Valid only for BGA Packages. For other packages the parameter might increase
11) Only valid if VAGND is directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball)
12) The value is derived from a 1 sigma distribution
13) The specified value does not include the pin leakage current I_{OZ}. I_{OZ} has to be added to get the total current value.
14) This is the operating frequency of TMADC selectable by the bit 'TMADC supply level' (SUPLLEV.TMADCSUP)
15) f_{ADCI} clock cycles
16) Enabling of the pull down test device is only allowed in PWM operation with a duty cycle of ≤ 50% and a frequency of 1 kHz

Related information

TMADC input structure figure on page 450

4.7.2 TMADC input structure figure



Q_{AINS} : Analog input charge

R_{AIN} : Analog input switch resistance → $(t_{mstc(Min)}/C_{AINS})/10$, where $t_{mstc(Min)}$ is either 50ns (5V) or 100ns (3.3V)

I_{BWCHG} : Broken wire detection charge current

$I_{BWDISCHG}$: Broken wire detection discharge current

Figure 4 Equivalent Circuitry for Analog Inputs

Related information

TMADC 5V characteristics on page 447

4.8 External clock sources

OSC_XTAL is used to provide an accurate clock source for the device. It enables the connection of an external 20 MHz to 50 MHz crystals outside of the device. Ceramic resonators are also supported.

The purpose of the RTC 32 kHz oscillator is to offer a precise and power saving clock option for the device in its lower power modes like Sleep and Standby.

***Note**: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

4.8.1 OSC_XTAL characteristics

Table 81 OSC_XTAL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Oscillator frequency[1)]	f_{OSC} *SR*	20	-	50	MHz	External clock mode selected, if shaper is not bypassed
		20	-	50	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} *CC*	-	-	3[2)]	ms	Valid for above specified f_{OSC} range and 8 pF load capacitance
Input voltage at XTAL1	V_{IX} *SR*	-0.3	-	2.4	V	External crystal mode
		-0.5	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed
Input high voltage at XTAL1	V_{IHBX} *SR*	3.15	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; $V_{DDEXTOSC}$ = 5 V
		2.08	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; $V_{DDEXTOSC}$ = 3.3 V
Input low voltage at XTAL1	V_{ILBX} *SR*	-0.5	-	0.5	V	
Input amplitude (peak to peak) at XTAL1	V_{PPX} *SR*	1.0	-	3.0	V	External crystal mode; valid for 20 MHz ≤ f_{OSC} ≤ 50 MHz
		2.5	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; valid for 20 MHz ≤ f_{OSC} ≤ 50 MHz
Input current at XTAL1	I_{IX1} *CC*	-70	-	70	µA	DC input voltage sweep from 0V < V_{IN} < $V_{DDEXTOSC}$; T_J = T_J (Max)
Duty cycle at XTAL1	DC_{X1} *SR*	35	-	65	%	External clock mode, if shaper is not bypassed; V_{XTAL1} = 0.5*V_{PPX}

(table continues...)

Table 81 (continued) OSC_XTAL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Absolute RMS jitter at XTAL1	J_{ABSX1} *SR*	-	-	28	ps	External clock mode, if shaper is not bypassed;10 KHz to f_{OSC} / 2
Slew rate at XTAL1	SR_{XTAL1} *SR*	0.3	-	-	V/ns	External clock mode, if shaper is not bypassed; Maximum 30% difference between rising and falling slew rate
Internal load capacitor	C_{L0} *CC*	1.30	1.40	1.55	pF	Enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} *CC*	2.6	2.75	2.9	pF	Enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} *CC*	6.9	7.3	7.5	pF	Enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} *CC*	10.6	10.8	11.0	pF	Enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} *CC*	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} *CC*	3.5	4	5	pF	

1) SGMII protocol operation via HSPHY is only possible with 25MHz or 40 MHz
2) This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decreases

Related information

RTC 32 kHz oscillator characteristics on page 452

4.8.2 RTC 32 kHz oscillator characteristics

Table 82 RTC 32 kHz oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Operating input frequency of external crystal	f_{OSC} *CC*	-	32.768	-	kHz	The range depends on external crystal accuracy
Start-up time	T_{SU} *CC*	-	-	5	s	
Input high voltage at XTAL3	V_{IHBX} *CC*	-	-	$V_{DDEVRSB}$ + 0.5	V	
Input low voltage at XTAL3	V_{ILBX} *CC*	-0.5	-	-	V	
Oscillation amplitude at XTAL PADIN	V_{PP} *CC*	0.3	0.5	$V_{DDEVRSB}$	V	

(table continues...)

Table 82 (continued) RTC 32 kHz oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input hysteresis for shaper	V_{HYS} *CC*	-	50	-	mV	RTC_CON0.HYSEN = 1
Oscillator bias current	I_{bias} *CC*	0.2	0.6	0.8	µA	Lowest gain setting: RTC_CON0.GAINSEL = 00
		1	1.2	1.6	µA	Highest gain setting: RTC_CON0.GAINSEL = 11
Total current consumption of RTC	I_{RTC} *CC*	-	3	6	µA	

Related information

OSC_XTAL characteristics on page 451

4.9 Internal clock sources

The TC4DxAA-step COM provides two fully integrated clock options:

- Back-up clock
- Standby clock

The 100 MHz clock source is a precise on-chip clock. After start-up, the 100 MHz clock source has a lower accuracy (see f_{BACKUT}) and the clock source is later trimmed by the start-up software (see f_{BACKT} parameter).

The Standby clock source is used during standby mode. Its accuracy is specified by the f_{SB} and f_{SBT} parameters. This clock source is trimmed after start-up.

4.9.1 Back-up oscillator characteristics

Table 83 Back-up oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Back-up clock frequency before trimming	f_{BACKUT} *CC*	70	100	130	MHz	V_{DDEXT}, $V_{DDEVRSB}$ ≥ 2.97 V
Back-up clock frequency after trimming	f_{BACKT} *CC*	98	100	102	MHz	V_{DDEXT}, $V_{DDEVRSB}$ ≥ 2.97 V
Back-up clock fine trim LSB	$f_{BACKLSBFT}$ *CC*	18	-	40	kHz	

Related information

Standby oscillator characteristics on page 454

4.9.2 Standby oscillator characteristics

Table 84 Standby oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Standby clock before trimming	f_{SB} *CC*	30	70	110	kHz	V_{DDEXT}, $V_{DDEVRSB}$ ≥ 2.97 V
Standby clock after trimming	f_{SBT} *CC*	62	70	75	kHz	V_{DDEXT}, $V_{DDEVRSB}$ ≥ 2.97 V
Standby clock fine trim LSB	$f_{SBLSBFT}$ *CC*	1.82	2.03	2.24	kHz	LPOSCGAIN=0

Related information

Back-up oscillator characteristics on page 454

4.10 System Phase Locked Loop (SYS_PLL) characteristics

The following characteristics are valid for the System Phase Locked Loop (SYS_PLL). In order to achieve the specified performance of the module following constrains need to be considered:

***Note**:* *The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.*

***Note**:* *The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

4.10.1 System PLL characteristics

Table 85 System PLL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} *CC*	20	-	50	MHz	
Modulation Amplitude	*MA CC*	0	-	2	%	
Peak Period jitter[1)]	*DP CC*	-150	-	150	ps	Without modulation (PLL output frequency); valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; peak is equal to 5 sigma RMS jitter at DCO output
Peak accumulated jitter	D_{PP} *CC*	-5	-	5	ns	Without modulation (PLL output frequency); valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
Total long term jitter	J_{TOT} *CC*	-	-	11.5	ns	Including modulation (PLL output frequency); MA 1.25%; valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over at least 1000 output clock observances
DCO frequency range	f_{DCO} *CC*	400	-	1000	MHz	
PLL lock-in time	t_L *CC*	4	-	100	µs	

1) Scaling division on the measurement to be applied: sqrt (f_{DCO} / $f_{Aquired}$), at maximum 16

4.11 Peripheral Phase Locked Loop (PER_PLL) characteristics

The following characteristics are valid for the Peripheral Phase Locked Loop (PER_PLL). In order to achieve the specified performance of the module following constrains need to be considered:

***Note**: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.*

***Note**: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

4.11.1 Peripheral PLL characteristics

Table 86 Peripheral PLL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DCO input frequency range	f_{REF} *CC*	20	-	50	MHz	
Peak Period jitter[1)]	*DP CC*	-150	-	150	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; peak is equal to 5 sigma RMS valid at DCO output
Peak accumulated jitter	D_{PPI} *CC*	-700	-	700	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
Peak accumulated jitter at SYSCLK pin	D_{PP} *CC*	-1000	-	1000	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
RMS accumulated jitter	D_{RMS} *CC*	-150	-	150	ps	Valid for f_{REF} = 20 MHz and f_{DCO} = 800 MHz; measured over 100 µs (over at least 6k samples)
Absolute RMS jitter (PLL out)	J_{ABS20} *CC*	-92	-	92	ps	Valid for f_{REF} = 20 MHz; f_{DCO} = 800 MHz; integration range from 10 kHz to about f_{DCO} divided by 2
DCO frequency range	f_{DCO} *CC*	400	-	800	MHz	
PLL lock-in time	t_L *CC*	4	-	100	µs	

1) Scaling division on the measurement to be applied: sqrt (f_{DCO} / $f_{Aquired}$), at maximum 16

4.12 Power supply topology and power supply characteristics

4.12.1 Power supply topology

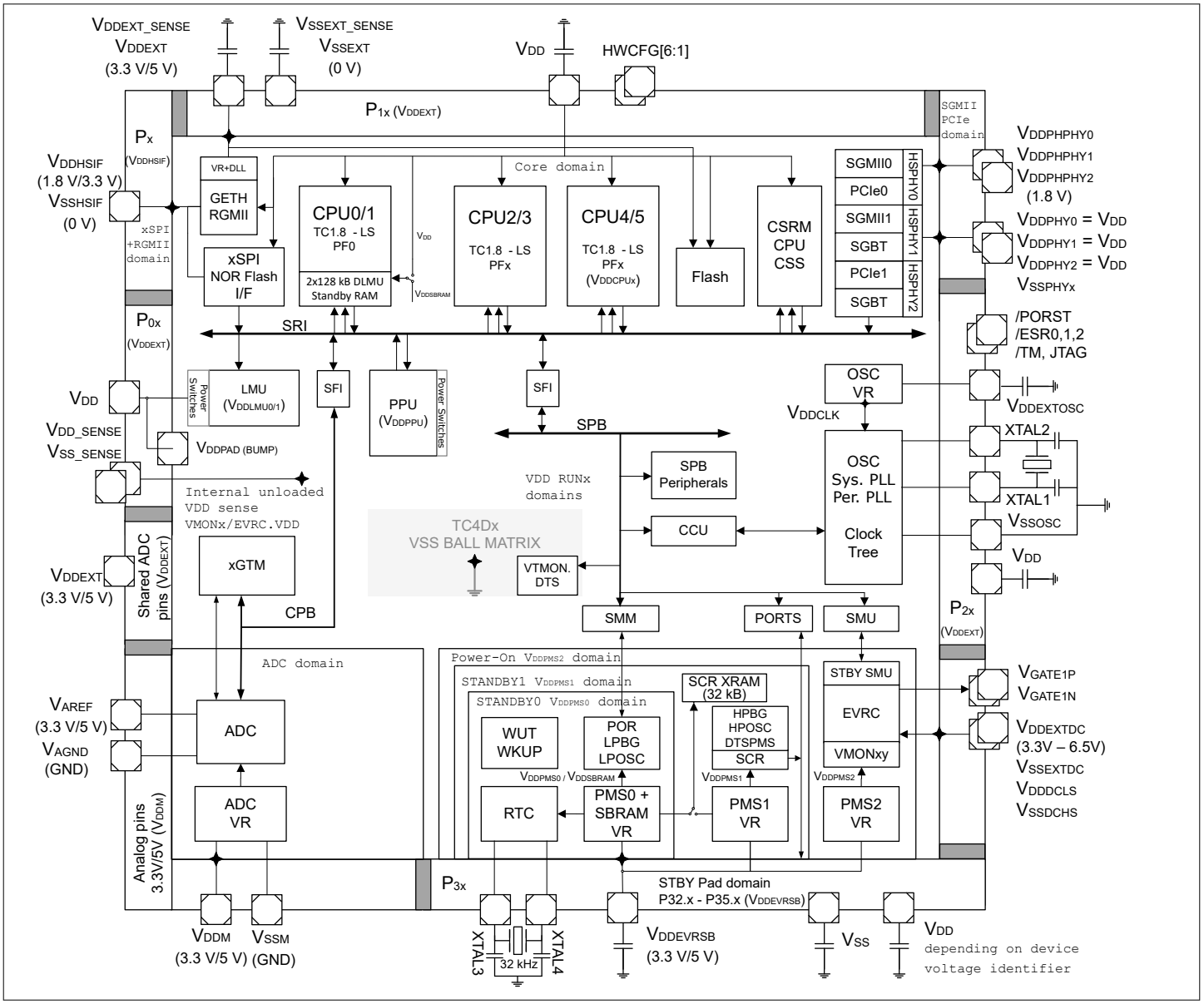


Figure 5 Power Supply Topology

Related information

Supply ramp-up and ramp-down behavior on page 458
LVD reset characteristics on page 459
Line Transients on page 460

4.12.2 Supply ramp-up and ramp-down behavior

This section presents the behavior of the supply rails during ramp-up, ramp-down, and dynamic operational phases.

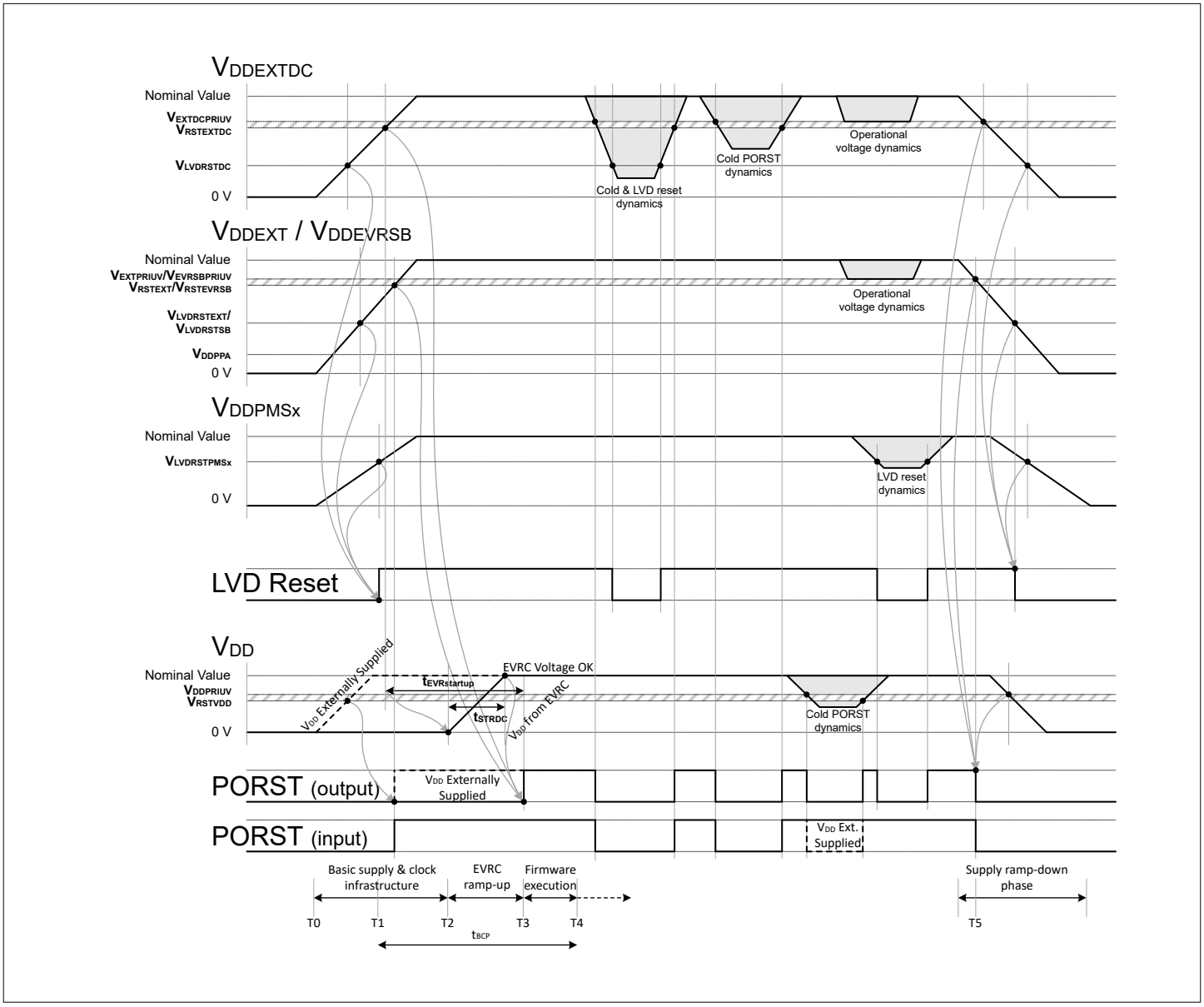


Figure 6 Supply ramp-up and ramp-down behavior

- The start-up slew rates for the supply rails shall comply to the respective data sheet parameters dV_{xx}/dt. The slope is defined as the maximum tangential slope between 0% to 100% voltage level. The actual waveform may not represent the specification
- In case of an external regulator for the V_{DD} supply rail, it is ensured that the load jumps to the external regulator (from the V_{DD} rail) are limited during the start-up phase to the dI_{DDDYN_STRT} data sheet parameter
- PORST is active or asserted when either PORST (input) or PORST (output) is active or asserted
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold (V_{RSTxx} parameter in the datasheet)
- PORST (output) active means that the microcontroller asserts the reset internally and drives the PORST pin low, propagating the reset to external devices. The PORST (output) is asserted by the MCU when at least one supply domain violates its primary under-voltage reset threshold. The PORST (output) is de-asserted by the microcontroller when all relevant supplies (with VMONP_VxxRST.RESETOFF = 0) are above their primary reset thresholds and the basic supply and clock infrastructure is available

The power sequence as shown in the figure above is enumerated as follows:

- T0 is the begin of the supply ramp-up from the external regulator
- T1 is the point in time when LVD reset is released. The LVD resets are released when $V_{DDEXTDC}$, V_{DDEXT}, $V_{DDEVRSB}$, and V_{DDPMSx} are above their LVD reset levels (denoted as $V_{LVDRSTxx}$)
- T0 up to T2 refers to the period in time when basic supply and clock infrastructure components are made available as the external supply ramps up. The band-gap and internal clock sources are started. The supply mode is evaluated based on the *HWCFG* pins. These events are initiated after LVD reset release at T1
- T2 refers to the point in time where a soft start of the EVRC is initiated. PORST (input) does not have any effect on the EVRC output and the regulator continues to generate the respective voltage though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the t_{STRDC} time (data sheet parameter) to avoid overshoots
- T3 refers to the point in time when all supplies are above their primary reset thresholds, denoted as V_{RSTxx}. There are two parameters denoting the primary reset threshold, respectively V_{RSTxx} (which is the untrimmed threshold) and $V_{xxPRIUV}$ (which is the trimmed threshold). Their values are located closely to each other and are indicated therefore as a thin hashed region in the figure above. During the supply ramp-up phase, the untrimmed threshold V_{RSTxx} is used for the first PORST release. After the firmware execution phase, the trimmed threshold $V_{xxPRIUV}$ is used for the PORST assertions. Subsequent reset releases occur at the untrimmed threshold V_{RSTxx}, since the primary voltage monitors reset thresholds VMONP_VxxRST.RESETTRIM are being reset to the V_{RSTxx} values also after a cold PORST (see the "Cold PORST" reset values of the VMONP_VxxRST registers)
- The supply start-up phase is completed when the regulator outputs are stable and operational and all voltages have ramped up. Consequently cold PORST reset is released when all voltages on the primary monitors are above their minimum operational limits (V_{RSTxx}/$V_{xxPRIUV}$)
- T4 refers to the point in time when the firmware execution is completed and the user code execution starts, with CPU0 running at the f_{BACKT} clock frequency. The time between T1 and T4 is documented as t_{BCP} (cold power on reset boot time, datasheet parameter)
- T5 refers to the point in time during the supply ramp-down phase when at least one of the supplies (either externally provided or internally generated) drops below its respective primary under-voltage reset threshold $V_{xxPRIUV}$

Related information

Power supply topology on page 457
LVD reset characteristics on page 459
Line Transients on page 460

4.12.3 LVD reset characteristics

Table 87 LVD reset characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDEXT} LVDANA reset undervoltage detector compartor threshold	$V_{LVDRSTEXT}$ *CC*	2.5	-	2.77	V	Supply ramp-down and undershoots
		2.53	-	2.8	V	Supply ramp-up
$V_{DDEVRSB}$ LVDANA reset undervoltage detector compartor threshold	$V_{LVDRSTSB}$ *CC*	2.26	-	2.5	V	Supply ramp-down and undershoots
		2.21	-	2.53	V	Supply ramp-up
$V_{DDEXTDC}$ LVDANA reset undervoltage detector compartor threshold	$V_{LVDRSTDC}$ *CC*	2.5	-	2.77	V	Supply ramp-down and undershoots
		2.53	-	2.8	V	Supply ramp-up

(table continues...)

Table 87 (continued) LVD reset characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPMS0} LVDPMSx undervoltage detector compartor threshold	$V_{LVDRSTPMS0}$ *CC*	0.75	0.785	0.82	V	Supply ramp-down and undershoots
		0.75	0.785	0.82	V	Supply ramp-up
V_{DDPMS1}, V_{DDPMS2} and $V_{DDSBRAM}$ LVDPMSx undervoltage detector compartor threshold	$V_{LVDRSTPMS1}$ *CC*	0.75	0.785	0.82	V	Supply ramp-down and undershoots
		0.75	0.785	0.82	V	Supply ramp-up
L_{VDx} reset assertion.response time on under voltage for V_{DDEXT} , $V_{DDEVRSB}$, $V_{DDEXTDC}$ and V_{DDPMSx} detectors	t_{LVD} *CC*	-	1	3	µs	LVD assertion
Input high voltage level for HWCFG pins on LVDANA reset release	V_{IH_HWCFG} *SR*	0.7*V_{DDIO} [1]	-	-	V	V_{DDIO} = $V_{LVDRSTEXT}$ [1]
Input low voltage level for HWCFG pins on LVDANA reset release	V_{IL_HWCFG} *SR*	-	-	0.44*V_{DDIO} [1]	V	V_{DDIO} = $V_{LVDRSTEXT}$ [1]

1) V_{DDIO} corresponding to the supply voltage of the IO supply domains V_{DDEXT} or $V_{DDEXTHS}$

Related information

Power supply topology on page 457
Supply ramp-up and ramp-down behavior on page 458
Line Transients on page 460

4.12.4 Line Transients

Table 88 Line Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External VDDEXT and VDDEVRSB supply ramp-up and ramp-down slope[1) 2)]	dV_{DDEXT}/dt *SR*	8.3E-06	1	100	V/ms	
External VDDM supply ramp-up and ramp-down slope[1) 2)]	dV_{DDM}/dt *SR*	8.3E-06	1	100	V/ms	
External VDD supply ramp-up and ramp-down slope[1) 2)]	dV_{DD}/dt *SR*	8.3E-06[2)]	1	50	V/ms	
$V_{DDEXTDC}$ voltage during cranking	$V_{DDEXTDC\ CRANKING}$ *SR*	2.97	-	7	V	Up to 2.8 h; EVRC in reset (no switching); Cold PORST is not triggered

(table continues...)

Table 88 (continued) Line Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEXTDC}$ voltage during standby	$V_{DDEXTDC\ STANDBY}$ *SR*	0.0	-	7	V	Up to 2.8 h; EVRC in reset (no switching); Higher standby current if VDDEXTDC is kept supplied
V_{DDEXT} voltage during cranking	$V_{DDEXT\ CRANKING}$ *SR*	2.97	-	5.5	V	Cold PORST is not triggered
V_{DDEXT} voltage during standby	$V_{DDEXT\ STANDBY}$ *SR*	0.0	-	5.5	V	Higher standby current if V_{DDEXT} is kept supplied
$V_{DDEVRSB}$ voltage during cranking	$V_{DDEVRSB\ CRANKING}$ *SR*	2.97	-	5.5	V	Cold PORST is not triggered
$V_{DDEVRSB}$ voltage during standby	$V_{DDEVRSB\ STANDBY}$ *SR*	2.6	-	5.5	V	

1) The device is robust against residual voltage ramp-up starting between [0 up to minimal operational voltage] for V_{DDEXT}, $V_{DDEVRSB}$, $V_{DDEXTDC}$, V_{DDHSIF} (if applicable), V_{DDM} and V_{DD}.
2) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

Related information

Power supply topology on page 457
Supply ramp-up and ramp-down behavior on page 458
LVD reset characteristics on page 459

4.13 PMS characteristics

The PMS is comprised of 3 power domain partitions PMS0, PMS1, and PMS2, to support the low power STANDBY0 and STANDBY1 modes. Each of the domains has its own voltage regulator:

- VDDPMS0 is used for the PMS0 domain
- VDDPMS1 is used for the PMS1/PMS2 domains

The EVRC SMPS regulator is also included in the PMS. Its purpose is to provide the main VDD core voltage.

The entire power supply topology can be found in chapter 'Power Supply Topology'.

Related information

Power supply topology and power supply characteristics on page 457

4.13.1 VDDPMS0 and VDDSBRAM regulator characteristics

Table 89 VDDPMS0 and VDDSBRAM regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEVRSB}$ voltage range during start-up and operation mode transitions	$V_{DDEVRSBIN}$ *SR*	2.76	-	6.5	V	
VDDPMS0 regulator output voltage Static accuracy without dynamic load/line regulation - untrimmed	$V_{DDPMS0UT}$ *CC*	0.88	0.95	1	V	
VDDPMS0 regulator output voltage range including load/ line regulation and aging	V_{DDPMS0} *CC*	0.88	0.95	1	V	
VDDPMS0 maximum output load current	$I_{DDPMS0MAX}$ *SR*	-	-	1	mA	
VDDPMS0 and VDDSBRAM regulator line transient response	dV_{DDPMS0}/dV_{IN} *CC*	-15	-	15	mV	dV/dT = 50 V/ms; dV < I 2.97-5.5 V I; C_L = 1 nF (C_L is an on-chip load capacitor)
Input VDDEVRSB voltage range during standby operation	$V_{DDEVRSBINSTBY}$ *SR*	2.6	-	-	V	

Related information

VDDPMS1 regulator characteristics on page 463
EVRC SMPS characteristics on page 464
EVRC SMPS external components on page 467

4.13.2 VDDPMS1 regulator characteristics

Table 90 VDDPMS1 regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDPMS1 regulator output voltage static accuracy without dynamic load/line regulation - untrimmed	$V_{DDPMS1UT}$ *CC*	0.936	0.98	1.024	V	
VDDPMS1 regulator output voltage static accuracy without dynamic load/line regulation - trimmed	$V_{DDPMS1T}$ *CC*	0.93	0.95	0.97	V	Standby mode at 70 kHz
		0.96	0.98	1	V	Standby mode and operation at 100 MHz
VDDPMS1 regulator output voltage range including load/ line regulation and aging	V_{DDPMS1} *CC*	0.91	0.95	0.97	V	Standby mode at 70 kHz
		0.94	0.98	1.00	V	Standby mode and operation at 100 MHz
VDDPMS1 maximum output load current	$I_{DDPMS1MAX}$ *SR*	-	-	15	mA	
VDDPMS1 regulator load transient response	dV_{DDPMS1}/dI_{OUT} *CC*	-60	-	60	mV	dI < ±3 mA; t_r = 0.01 µs; t_f = 0.01 µs; T_{settle} = 20 µs; C_L = 1.5 nF (C_L is an on-chip load capacitor); VDDPMS1 regulator in high current sink mode
Maximum load step limitation of VDDPMS1 regulator	dI_{DDPMS1}/dI_{OUT} *SR*	-	-	4	mA	SW limits load jumps
VDDPMS1 regulator line transient response	dV_{DDPMS1}/dV_{IN} *CC*	-15	-	15	mV	dV/dT = 50 V/ms; dV < I 2.97-5.5 V I

Related information

VDDPMS0 and VDDSBRAM regulator characteristics on page 462
EVRC SMPS characteristics on page 464
EVRC SMPS external components on page 467

4.13.3 EVRC SMPS characteristics

Table 91 EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEXTDC}$ Voltage range during start-up[1]	$V_{INEXTDCSTRT}$ *SR*	2.6[2]	-	6.5	V	$V_{DDEXTDC}$ = 3.3 V/5 V nominal voltage, EVRC in reset (no switching). Operation between 5.5 V and 6.5 V is limited to max. 2.8 h
		3.5	-	7.5	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode, EVRC in reset (no switching). Operation between 7.0 V and 7.5 V is limited to max. 2.8 h
Input $V_{DDEXTDC}$ voltage range during operation mode	$V_{INEXTDC}$ *SR*	2.97	-	5.5	V	$V_{DDEXTDC}$ = 3.3 V/5 V nominal voltage
		4.95	-	7.0	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode
Input $V_{DDEXTDC}$ and $V_{DDEVRSB}$ peak to peak Voltage Ripple during start-up and operation, at the external regulator output	$V_{INRIPPLE}$ *SR*	-	0.1	0.3	V	100 kHz < f_{ripple} < 3 MHz; square/sinusoidal ripple may be assumed
SMPS regulator output voltage range including load/line regulation and aging - trimmed	V_{DDDC} *CC*	0.983	1.025	1.087	V	$I_{DDSLEEP} \le I_{DDDC} \le I_{DDDCMAX}$; V_{ID} = slow + typical samples; for load transients $\|dI\|$ < 250 mA
		0.936	0.975	1.034	V	$I_{DDSLEEP} \le I_{DDDC} \le I_{DDDCMAX}$; V_{ID} = fast samples; for load transients $\|dI\|$ < 250 mA
SMPS regulator static voltage output accuracy without dynamic load/line regulation - trimmed	V_{DDDCT} *CC*	1.004	1.025	1.046	V	$I_{DDSLEEP} \le I_{DDDC} \le I_{DDDCMAX}$; V_{ID} = slow + typical samples; Voltage at V_{DD_SENSE} (EVRC feedback)
		0.955	0.975	0.995	V	$I_{DDSLEEP} \le I_{DDDC} \le I_{DDDCMAX}$; V_{ID} = fast samples; Voltage at V_{DD_SENSE} (EVRC feedback)
SMPS regulator static voltage output accuracy without dynamic load/line regulation - untrimmed	V_{DDDCUT} *CC*	0.975	1.025	1.075	V	$I_{DD\_LEAK} \le I_{DDDC} \le I_{DDDCSTRT}$

(table continues...)

Table 91 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable switching frequency after trimming	f_{DCDC} *SR*	-	0.8	-	MHz	$I_{DDDC} \leq I_{DDDCMAX}$ (HE case); start-up frequency switches from 444 kHz in open loop operation to f_{DCDC} in closed loop operation
		-	0.45	-	MHz	$I_{DDDC} \leq I_{DDDCMAX}$ (HE case); start-up frequency switches from 444 kHz in open loop operation to f_{DCDC} in closed loop operation
Start-up time	t_{STRDC} *CC*	0.2	-	1.5	ms	SMPS start-up mode; it is defined as the EVRC ramp-up time from 0V until V_{DD} nominal voltage reached, on condition that all other PORST requirements were released before; $I_{DDDC} = I_{DDDCSTRT}$
Switching frequency modulation spread	ΔT_{DCSPR} *SR*	-	10	-	ns	Modulation spread of the switching frequency, expressed as time period instead of frequency
Maximum ripple at I_{MAX}	ΔV_{DDDC} *CC*	-	-	14	mV	$I_{DDDCSTRT} \leq I_{DDDC} \leq I_{DDDCMAX}$; ΔV_{DDDC} = (peak-to-peak ripple / 2)
Current consumption of SMPS regulator at minimum load	I_{DCNL} *CC*	-	-	30	mA	f_{DCDC} = 0.8 MHz; I_{DDDC} = 10 mA; T_J = 25°C; current drawn from the $V_{DDEXTDC}$ rail
Standby/Quiescent current consumption of SMPS regulator	I_{DCSTBY} *CC*	-	10	-	µA	EVRC off in standby mode; current drawn from the $V_{DDEXTDC}$ rail; $V_{DDEXTDC}$ LV case (3.3 V/5 V); $V_{DDEXTDC}$ = 3.3 V/5 V ± 10%; $T_J \leq$ 25°C
		-	20	-	uA	EVRC off in standby mode; current drawn from the $V_{DDEXTDC}$ rail; $V_{DDEXTDC}$ LV case (3.3 V/5 V); $V_{DDEXTDC}$ = 3.3 V/5 V ± 10%; 25°C < $T_J \leq T_J$(Max)
		-	2.6	-	mA	EVRC off in standby mode; current drawn from the $V_{DDEXTDC}$ rail; $V_{DDEXTDC}$ HV case (6.5 V); $V_{DDEXTDC}$ remains supplied at 6.5 V

(table continues...)

Table 91 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SMPS regulator peak efficiency	n_{DC} *SR*	-	85	-	%	V_{IN} = 3.3 V; f_{DCDC} = 0.45 MHz
		-	85	-	%	V_{IN} = 3.3 V; f_{DCDC} = 0.8 MHz
Maximum output current	$I_{DDDCMAX}$ *CC*	-	-	6.5	A	HE case, RUN Mode[2)]
Load current during SMPS regulator start-up	$I_{DDDCSTRT}$ *CC*	0.15	-	3.5	A	HE, PORST asserted
SMPS regulator line transient response	dV_{DDDCT} / dV_{IN} *CC*	-6	-	6	%	Expressed as % of V_{DDDC} nominal value; dV/dt = 120 V/ms; $\|dV\| < \|V_{INEXTDCSTRT}$ (Min) - $V_{INEXTDCSTRT}$ (Max)$\|$; does not include EVRC ripple.
		-1	-	1	%	Expressed as % of V_{DDDC} nominal value; dV/dt = 1 V/ms; $\|dV\| < \|V_{INEXTDCSTRT}$ (Min) - $V_{INEXTDCSTRT}$ (Max)$\|$; does not include EVRC ripple.
SMPS regulator load transient response before trimming	dV_{DDDCUT} / dI_{OUT} *CC*	-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $\|dI\| < dI_{DDDYN\_STRT}$; $I_{DDDC} = I_{DDDCSTRT}$; t_r = 0.1 µs; t_f = 0.1 µs; V_{DDDC} untrimmed; T_{settle} = 20 µs; HE components; includes EVRC ripple
		-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $\|dI\| < \|dI_{DDDYN\_LBIST}\|$; $I_{DDDC} = I_{DDDCSTRT}$; EVRC bandgap and clock trimmed but operated with default coefficients; HE components; includes EVRC ripple
Input Synchronisation frequency	$f_{DCDCSYNC}$ *SR*	0.42	0.45	0.49	MHz	f_{DCDC} = 0.45 MHz HE case
		0.72	0.8	0.9	MHz	f_{DCDC} = 0.8 MHz HE case
Feedback ADC resolution for voltage scaling	dV_{FBADC} *SR*	-	2.83	-	mV	Used for scaling of VDD target value in EVRC_CON0 register. Feedback ADC nominal range < 1.446 V

1) Voltage range dependent on used MOSFETs (see chapter PMS in User Manual)
2) LCDCDC standalone lower limit. The minimum startup voltage of LCDCDC also depends on LVD reset threshold and Primary undervoltage thresholds of VDDEVRSB, VDDEXT, VDDEXTDC

Related information

VDDPMS0 and VDDSBRAM regulator characteristics on page 462

VDDPMS1 regulator characteristics on page 463
EVRC SMPS external components on page 467

4.13.4 EVRC SMPS external components

Table 92 EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External output capacitor value	C_{OUT} *SR*	42.9	66	89.1	µF	$I_{DDDC} \le I_{DDDCMAX}$; f_{DCDC} = 0.8 MHz; 2 x 33 µF connected in parallel
		71.5	110	148.5	µF	$I_{DDDC} \le I_{DDDCMAX}$; f_{DCDC} = 0.45 MHz; 5 x 22 µF or (2 x 47 µF + 1 x 15 µF) connected in parallel
External output capacitor ESR	C_{OUT_ESR} *SR*	-	-	100	Ohm	f = 10 Hz
		-	-	20	mOhm	f ≥ 0.5 MHz ; f ≤ 10 MHz
External input capacitor values (Buffer + Decoupling)[1]	C_{IN} *SR*	14.3 + 0.065	22 + 0.1[2]	29.7 + 0.135	µF	$I_{DDDC} \le I_{DDDCMAX}$; f_{DCDC} = 0.45 MHz
		14.3 + 0.065	22 + 0.1[2]	29.7 + 0.135	µF	$I_{DDDC} \le I_{DDDCMAX}$; f_{DCDC} = 0.8 MHz
External input capacitor ESR	C_{IN_ESR} *SR*	-	-	20	mOhm	f ≥ 0.5 MHz; f ≤ 10 MHz
		-	-	100	Ohm	f = 100 Hz
External inductor value	L_{DC} *SR*	1.54	2.2	2.86	µH	f_{DCDC} = 0.8 MHz
		1.54	2.2	2.86	µH	f_{DCDC} = 0.45 MHz
External inductor DCR	L_{DC_DCR} *SR*	-	-	0.02	Ohm	Max. value depending on output current
External Inductor Saturation Current Margin	ΔI_{SAT} *SR*	400	-	-	mA	The saturation current of the coil must be larger than I_{DDDC} + ΔI_{SAT}
P + N-channel MOSFET Gate threshold voltage	V_{GSTH} *SR*	-	1	-	V	NMOS
		-	-1	-	V	PMOS

(table continues...)

Table 92 (continued) EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SMPS regulator load transient response after trimming	dV_{DDDCT}/dI_{OUT} CC	-3	-	9	%	Expressed as % of V_{DDDC} nominal value; -1200 mA < dI < 0 mA; negative value specifies the max. undershoot after the overshoot; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; t_f = 0.1 µs; T_{settle} = 50 µs; application reset load drop; includes EVRC ripple 3)
		-4.5	-	5	%	Expressed as % of V_{DDDC} nominal value; -700 mA < dI < 700 mA; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; tr = 0.1 µs; t_f = 0.1 µs; two consecutive load transients in the same direction (one transient of max. ±700mA followed by a transient of max. ±400mA), separated by a time of 20µs; 2 x CPU + PPU load jump; includes EVRC ripple; Input Synchronization enabled
		-4	-	5	%	Expressed as % of V_{DDDC} nominal value; -700 mA < dI < 700 mA; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; tr = 0.1 µs; t_f = 0.1 µs; two consecutive load transients in the same direction (one transient of max. ±700mA followed by a transient of max. ±400mA), separated by a time of 20µs; 2 x CPU + PPU load jump; includes EVRC ripple; Input Synchronization disabled
		-2.0	-	4.0	%	Expressed as % of V_{DDDC} nominal value; -250 mA < dI < 250 mA; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; t_r = 0.1 µs; t_f = 0.1 µs; T_{settle} = 20 µs; 2 x CPU load jump; includes EVRC ripple

(table continues...)

Table 92 (continued) EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
						3)
		-3.5	-	16.5	%	Expressed as % of V_{DDDC} nominal value; -1.6A < dI < 0mA; negative value specifies the max. undershoot after the overshoot; I_{DD} (Freerun) ≤ I_{DDDC} ≤ $I_{DDDCMAX}$; t_f = 0.1µs; T_{settle} = 100µs; cold or warm PORST load drop; includes EVRC ripple 3)

1) The "+" means that both (Buffer and Decoupling) Capacitors have to be connected in parallel close to the external power stage. The smaller one (Decoupling Capacitor) needs to be placed as close as possible to the source connection of the PMOS.
2) Additional external components maybe required depending on EMI/EMC requirements
3) T_{settle} is the time after which the V_{DD} output voltage returns to within ±1.5% of the static EVRC output voltage value without any load transient.

Related information

VDDPMS0 and VDDSBRAM regulator characteristics on page 462
VDDPMS1 regulator characteristics on page 463
EVRC SMPS characteristics on page 464

4.14 System mode dependent and reset timing characteristics

4.14.1 System state timings

Table 93 System state timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
STANDBY0 entry transition time from STANDBY1_70k mode on SCR events	t_{STBY10} *CC*	-	-	50	µs	
STANDBY0 exit transition time to STANDBY1 _70k mode on wake-up events	t_{STBY01} *CC*	-	-	150	µs	
Standby RAM supply switch activation time during Run mode on V_{DDEXT} or V_{DD} primary undervoltage event	$t_{STBYRAM}$ *CC*	-	-	1	µs	dLMU Standby RAM supply switched
STANDBY1 entry transition time from RUN mode on V_{DDEXT} or V_{DD} undervoltage event	$t_{RxSTBY1}$ *CC*	-	1	10	µs	Current consumption $I_{STANDBY1}$ reached
STANDBY1 transition time to disable Bandgap and ADCOMP	$t_{ADC100M}$ *CC*	-	-	10	µs	SCR ADCOMP and HPBG disable, with SCU_PMS1IVRCON.SINKCTRLEN=0
STANDBY1 transition time to enable Bandgap and ADCOMP	$t_{100MADC}$ *CC*	-	-	50	µs	SCR ADCOMP_CON.EN_REQ request until ADCOMP_RESHSTAT.EN_STAT set to 1. ADCOMP SUCAL not considered, with SCU_PMS1IVRCON.SINKCTRLEN=0
STANDBY1 transition time to disable back-up clock	$t_{100M70k}$ *CC*	-	-	110	µs	SCR f_{SBT} clock request via SCU_CLK.DIV_REQ to switch off f_{BACKT} clock, with SCU_PMS1IVRCON.SINKCTRLEN=0
STANDBY1 transition time to enable back-up clock	$t_{70k100M}$ *SR*	-	-	170	µs	SCR f_{BACKT} clock request via SCU_CLK.DIV_REQ until SCU_CLK.DIV_STAT is updated

(table continues...)

Table 93 (continued) System state timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum HWCFG hold time after LVDANA reset release during start-up	t_{HWCFG} *SR*	200	-	400	µs	HWCFG latch after start-up for EVRC configuration. V_{DDEXT}, $V_{DDEVRSB}$ and $V_{DDEXTDC}$ above LVD detector levels. R_{HWCFG} = 4.7 kOhm ± 50%, V_{IL} = see V_{IL_HWCFG}, V_{IH} = see V_{IH_HWCFG}.
Power domain supply switch-off transition time after taken request	t_{PDDIS} *CC*	-	-	200	µs	Load jump sequencing of 25 mA / 5 µs as default reset value. PD_CON0.CLKPPU = [000, 001, 010, 011 or 100]
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ *SR*	360	-	-	µs	Valid for all primary voltage monitors to ensure proper reset shutdown sequencing.
MBIST execution time extending the boot time	t_{MBIST} *CC*	-	-	6	ms	Key-on MBIST (4N-DT, f_{SRI}=100 MHz) and consecutive initialization. Configuration details incl. SRAM-grouping described in UM, VMT-chapter.
		-	25	-	ms	Key-off MBIST (4N-DT, f_{SRI} = MAX). Configuration details incl. SRAM-grouping described in UM, VMT-chapter.
LBIST execution time	t_{LBIST} *CC*	-	-	50	ms	Key-off LBIST; Time per LBIST-Cluster; Reset time excluded
		-	-	6	ms	Key-on LBIST; Reset time excluded
Timing-Window available for placement of external Tool-Requests via COMDATA/ Cerberus	t_{WINDOW} *CC*	800	-	-	µs	In case of DXCPL used, shortened SPD-0-bitwidth in Activation sequence required.
Transitioning time to permanent reset	t_{WCST} *CC*	-	-	43	ms	Time is a sum of t_{BCP} (incl. EVR ramp-up) + t_{BCP} (w/o EVR ramp-up) + 2 * (FW fault handling time + $t_{CPU0WDT}$ + t_{RTC} + $t_{WARMRSTSEQ}$)

Related information

Reset timings on page 472
Power, pad and reset timing figure on page 474

4.14.2 Reset timings

Table 94 Reset timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Cold Power on Reset Boot Time [1]	t_{BCP} *CC*	-	-	3.3	ms	Firmware execution time after PORST release without EVRC ramp-up; RAM initialization, LBIST execution and CSRM boot time is not included [2]
		-	3	5.5	ms	dV_{DDEXT}/dT = 1 V/ms; V_{DDEXT} > $V_{LVDRST5}$; boot time after Cold PORST including EVRC ramp-up, PBIST and Firmware execution time; RAM initialization and CSRM boot time are not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary VMONP monitors	t_{EVRPOR} *CC*	10 [3]	-	-	µs	
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} *SR*	-	1 [4]	-	ms	
EVRC ramp-up time till cold PORST reset release	$t_{EVRstartup}$ *CC*	-	1	2	ms	It is defined from the $V_{EXTDCPRIUV}$ reset threshold crossing until cold PORST reset release. dV/dT=1 V/ms; EVRC active
Application Reset Boot Time	t_{BAR} *CC*	-	-	450	µs	operating with max. frequencies, with valid BMHD header; Warm Reset Sequencing Delay Time not included
System Reset Boot Time [2]	t_{BSR} *CC*	-	-	2	ms	w/o SWAP, with valid BMHD header
Warm PORST reset boot time [2]	t_{BWP} *CC*	-	-	2.5	ms	Start from internal NVM with configured BMHD. Time does not include RAM initialization, Foreground CSRM-Boot, ABM and LBIST-Runtime
Warm Reset Sequencing Delay Time	$t_{WARMRSTSEQ}$ *CC*	-	-	300	µs	

(table continues...)

Table 94 (continued) Reset timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ *CC*	600	-	1200	ns	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} *SR*	16 / f_{SPB}	-	-	ns	HWCFG latch after warm resets
HWCFG pins setup time to ESR0 rising edge	t_{HDS} *SR*	0	-	-	ns	HWCFG latch after warm resets
Ports inactive after ESR0 reset active	t_{PI} *CC*	-	-	8 / f_{SPB}	ns	
Ports inactive after PORST reset active	t_{PIP} *CC*	-	-	250	ns	
Hold time from PORST rising edge	t_{POH} *SR*	360	-	-	ns	
Setup time to PORST rising edge	t_{POS} *SR*	0	-	-	ns	
SCR reset boot time [2]	$t_{SCRBOOT}$ *CC*	-	-	60	µs	On user mode entry at 100 MHz, Standby exit, WDT (System) double bit ECC reset and soft reset

1) RAM initialization in SSW of PMEM, DMEM, PTAG, DTAG and DLMU RAMs add 1000 µs in addition.
2) From release of PORST by PMS
3) Cold PORST reset is driven by µC and maintained in an extended voltage range between V_{DDPPA} limit and absolute maximum rating voltage limits.
4) The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on V_{DDEXT}, V_{DDHSIF} (if applicable) and V_{DD} rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The t_{POA} additional time is recommended for a robust start-up and not a mandatory requirement.

Related information

System state timings on page 470
Power, pad and reset timing figure on page 474

4.14.3 Power, pad and reset timing figure

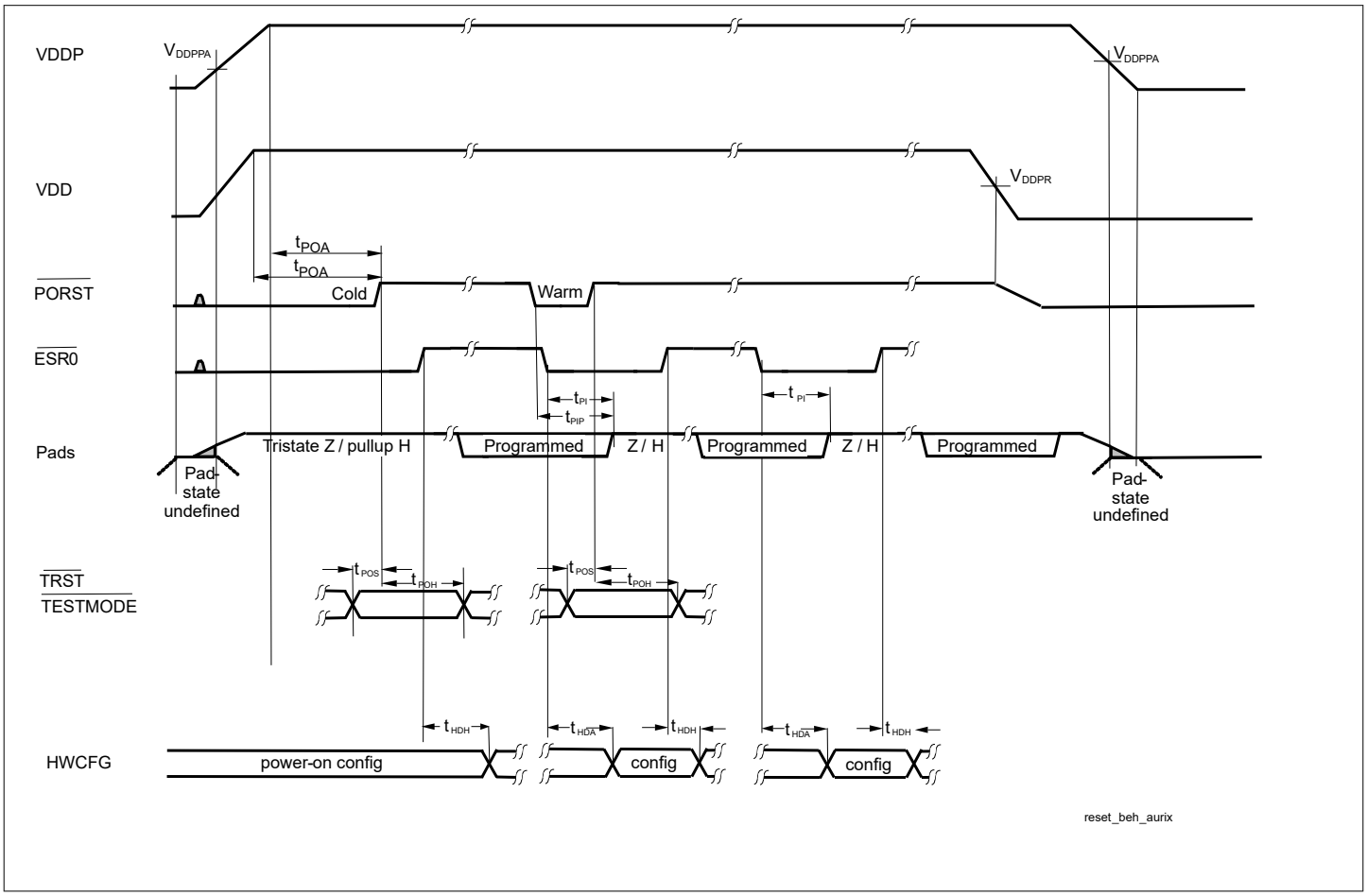


Figure 7 Power, pad and reset timing

Related information

System state timings on page 470
Reset timings on page 472

4.15 PMS voltage monitoring characteristics

The supply rails monitored by primary and secondary voltage monitors are measured by primary and secondary monitor ADCs. Four ADC topologies are used for this purpose:

- Tracking High Voltage ADC (TRKHV)
- Tracking Core ADC (TRKCORE)
- SAR High Voltage ADC (SARHV)
- SAR Core ADC (SARCORE)

The characteristics of this ADCs can be found in the following sub-chapter.

4.15.1 Primary and secondary voltage monitor ADC characteristics

Table 95 Primary and secondary voltage monitor ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Core tracking ADC characteristics						
Core tracking ADC least significant bit	$V_{TRKCORELSB}$ *CC*	-	2.830	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
Core tracking ADC measurement latency	$t_{TRKCORE}$ *CC*	-	-	21	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
High-voltage tracking ADC characteristics						
High-voltage tracking ADC least significant bit	$V_{TRKHVLSB}$ *CC*	-	11.32	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
High-voltage tracking ADC measurement latency	t_{TRKHV} *CC*	-	-	41	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
Core SAR ADC characteristics						
Core SAR ADC measurement latency	$t_{SARCORE}$ *CC*	-	420	430	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used; after firmware boot
Core SAR ADC least significant bit	$V_{SARCORELSB}$ *CC*	-	0.586	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
High-voltage SAR ADC characteristics						
High-voltage SAR ADC least significant bit	$V_{SARHVLSB}$ *CC*	-	2.830	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
High-voltage SAR ADC measurement latency	t_{SARHV} *CC*	-	-	450	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used

Related information

Primary voltage monitors on page 475
Secondary voltage monitors on page 481

4.15.2 Primary voltage monitors

Related information

Primary and secondary voltage monitor ADC characteristics on page 475
Secondary voltage monitors on page 481

4.15.2.1 Primary voltage monitors parameters overview

Table 96 Primary voltage monitors parameters

Voltage rail	VMONP LSB datasheet parameter	Primary under-voltage reset threshold after trimming - datasheet parameter	Effect of primary under-voltage reset threshold violation[1]
V_{DD}	$V_{TRKCORELSB}$	$V_{DDPRIUV}$	Cold PORST
V_{DDEXT}	$V_{TRKHVLSB}$	$V_{EXTPRIUV}$	Cold PORST
($V_{DDEXTDC}$- V_{SSDCHS})	$V_{TRKHVLSB}$	$V_{DCHSPRIUV}$	Cold PORST only if *HWCFG[2:1]* = 11_B
$V_{DDEXTDC}$	$V_{TRKHVLSB}$	$V_{EXTDCPRIUV}$	Only when EVRC is enabled, a power state transition corresponding to an EVRC failure is triggered. The primary monitor triggers not only a cold PORST, but a deeper power state where the EVRC regulator is disabled, until the supply raises above the reset release threshold.
V_{DDDCLS}	$V_{TRKHVLSB}$	$V_{DCLSPRIUV}$	Cold PORST only if *HWCFG[2:1]* = 11_B
$V_{DDEVRSB}$	$V_{SARHVLSB}$	$V_{EVRSBPRIUV}$	Cold PORST
V_{DDM}	$V_{SARHVLSB}$	$V_{DDMPRIUV}$	Cold PORST
$V_{DDPHPHYx}$	$V_{SARHVLSB}$	$V_{PHPHYPRIUV}$	Cold PORST
V_{DDHSIF}	$V_{SARHVLSB}$	$V_{HSIFPRIUV}$	Cold PORST
V_{DDPAD}	$V_{SARCORELSB}$	$V_{DDPADPRIUV}$	Cold PORST
V_{DDPPU}	$V_{SARCORELSB}$	$V_{DDPPUPRIUV}$	Cold PORST
V_{DDLMUx}	$V_{SARCORELSB}$	$V_{DDLMUPRIUV}$	Cold PORST
V_{DDPHYx}	$V_{SARCORELSB}$	$V_{DDPHYPRIUV}$	Cold PORST

1) Only if the respective VMONP_VxxRST.RESETOFF bit is set to zero.

4.15.2.2 Primary voltage monitors characteristics

Table 97 Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Non-configurable cold PORST thresholds						
$V_{DDEXTDC}$ primary undervoltage reset threshold before trimming [1]	$V_{RSTEXTDC}$ *CC*	2.6	-	3	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]

(table continues...)

Table 97 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDEXT} primary undervoltage reset threshold before trimming [1]	V_{RSTEXT} CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
$V_{DDEVRSB}$ primary undervoltage reset threshold before trimming[1]	$V_{RSTEVRSB}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
V_{DDM} primary undervoltage reset threshold before trimming [1]	V_{RSTDDM} CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
$V_{DDEXTDC}$ - V_{SSDCHS} primary undervoltage reset threshold before trimming; Only for PBIST[1]	$V_{RSTDCHS}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis only in $V_{DDEXTDC}$ HV Mode [2]
V_{DDDCLS} primary undervoltage reset threshold before trimming; Only for PBIST[1]	$V_{RSTDCLS}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis only in $V_{DDEXTDC}$ HV Mode [2]
V_{DD} primary undervoltage reset threshold before trimming	V_{RSTVDD} CC	-	-	0.894	V	By last cold PORST release on supply ramp-up including voltage hysteresis [2]
Configurable cold PORST thresholds						
$V_{DDEXTDC}$ primary undervoltage reset threshold after trimming[1]	$V_{EXTDCPRIUV}$ CC	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; 3.3 V ≤ $V_{DDEXTDC}$ ≤ 5 V mode [2]
		3.528	3.600	3.672	V	Default cold PORST PRIUV threshold = 0x13E; RESETHYS = 0x0; $V_{DDEXTDC}$ high-voltage mode [2]

(table continues...)

Table 97 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
($V_{DDEXTDC}$ - V_{SSDCHS}) primary undervoltage reset threshold after trimming.[1]	$V_{DCHSPRIUV}$ *CC*	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xx; RESETHYS = 0xFE; $V_{DDEXTDC}$ high-voltage mode [2]
V_{DDDCLS} primary undervoltage reset threshold after trimming[1]	$V_{DCLSPRIUV}$ *CC*	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; $V_{DDEXTDC}$ high-voltage mode [2]
V_{DDEXT} primary undervoltage reset threshold after trimming[1]	$V_{EXTPRIUV}$ *CC*	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; V_{DDEXT} = 3.3 V mode [2]
		4.27	4.358	4.446	V	Configurable cold PORST PRIUV threshold = 0x181; RESETHYS = 0x0; V_{DDEXT} = 5 V mode [2]
$V_{DDEVRSB}$ primary undervoltage reset threshold after trimming[1]	$V_{EVRSBPRIUV}$ *CC*	2.82	2.878	2.936	V	Default cold PORST PRIUV threshold = 0x3F9; RESETHYS = 0x0; V_{DDEXT} = 3.3 V mode [2]
		4.276	4.364	4.452	V	Configurable cold PORST PRIUV threshold = 0x606; RESETHYS = 0x0; V_{DDEXT} = 5 V mode [2]
V_{DDEXT}, $V_{DDEVRSB}$, and V_{DDM} primary undervoltage monitor threshold during supply ramp-down (dV_{IO}/dt)	$V_{EXTPRIUVMIN}$ *CC*	2.76	-	-	V	Valid for dV_{IO} / dt = 50 V / ms; with one single ADC input used; for $V_{DDEVRSB}$ and V_{DDM} with a maximum spike filter setting of 0
V_{DDEXT} undervoltage monitor threshold for 5V Flash programming and erase operation	$V_{EXTLVLFL}$ *CC*	4.35	4.4	4.5	V	No cold PORST generation. Only alarm signal to Flash

(table continues...)

Table 97 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDM} primary undervoltage reset threshold after trimming[1]	$V_{DDMPRIUV}$ *CC*	2.820	2.878	2.936	V	Default cold PORST PRIUV threshold = 0x3F9; RESETHYS = 0x0; V_{DDM} = 3.3 V mode [2]
		4.276	4.364	4.452	V	Configurable cold PORST PRIUV threshold = 0x606; RESETHYS = 0x0; V_{DDM} = 5 V mode [2]
V_{DDHSIF} primary undervoltage reset threshold after trimming[1]	$V_{HSIFPRIUV}$ *CC*	2.820	2.878	2.936	V	Optional configurable cold PORST PRIUV threshold = 0x3F9; RESETHYS = 0x0; V_{DDHSIF} = 3.3 V mode [2]
		1.577	1.610	1.643	V	Optional default cold PORST PRIUV threshold = 0x239; RESETHYS = 0x0; V_{DDHSIF} = 1.8 V mode [2]
$V_{DDPHPHYx}$ primary undervoltage reset threshold after trimming[1]	$V_{PHPHYPRIUV}$ *CC*	1.539	1.571	1.603	V	Optional configurable cold PORST PRIUV threshold = 0x22B; RESETHYS = 0x0 [2]
V_{DDPHYx} primary undervoltage reset threshold after trimming	$V_{DDPHYPRIUV}$ *CC*	0.852	0.870	0.888	V	Optional default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V [2]
		0.896	0.915	0.934	V	Optional configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2]

(table continues...)

Table 97 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DD} primary undervoltage reset threshold after trimming	$V_{DDPRIUV}$ *CC*	0.875[3]	0.886	0.897	V	Default cold PORST PRIUV threshold = 0x139; RESETHYS = 0x0; Valid for devices with V_{DD} = 0.975 V [2]
		0.919	0.931	0.943	V	Configurable cold PORST PRIUV threshold = 0x149; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2]
V_{DD} power domain cold reset level accuracy after trimming, for power-switched power domains (CPUx, PPU, LMU)	$V_{DDPDCLDUV}$ *CC*	0.754	0.770	0.786	V	Default power domain cold reset threshold = 0x110; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V
		0.798	0.815	0.832	V	Configurable power domain cold reset threshold = 0x120; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V
V_{DDPPU} primary undervoltage reset threshold after trimming	$V_{DDPPUPRIUV}$ *CC*	0.852	0.870	0.888	V	Optional default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V [2]
		0.896	0.915	0.934	V	Optional configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2]
V_{DDLMU} primary undervoltage reset threshold after trimming	$V_{DDLMUPRIUV}$ *CC*	0.896[3]	0.915	0.934	V	Optional configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2]
		0.852	0.870	0.888	V	Optional default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975V [2]

(table continues...)

Table 97 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPAD} primary undervoltage reset threshold after trimming[4]	$V_{DDPADPRIUV}$ *CC*	0.852	0.870	0.888	V	Default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V [2]
		0.896	0.915	0.934	V	Configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V [2]
V_{DDEXT} and $V_{DDEVRSB}$ PBIST primary overvoltage monitor threshold	V_{PBIST5} *CC*	5.498	-	-	V	
V_{DD} PBIST primary overvoltage monitor threshold	V_{PBISTC} *CC*	1.128	1.200	1.272	V	

1) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. All voltages are measured on pins/dedicated sense pins (VDDxx_SENSE) if available
2) Static voltage with supply slope less than or equal to 1 kV/s assumed as measurement condition.
3) V_{RSTxx} parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as $V_{xxPRIUV}$ parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.
4) The reset release on supply ramp-up is delayed by a time duration 20-40 µs after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. In case the 3.3 V supply is provided externally, the internal drop will cause a reset at a higher voltage of 3.0 V at the VDDHSIF pin.

4.15.3 Secondary voltage monitors

Related information

Primary and secondary voltage monitor ADC characteristics on page 475
Primary voltage monitors on page 475

4.15.3.1 Secondary voltage monitors parameters overview

Table 98 Secondary voltage monitors parameters

Voltage rail	VMONS LSB datasheet parameter	Secondary voltage monitor accuracy after trimming - datasheet parameter	Effects of secondary voltage monitoring thresholds violation[1]
$V_{DDEVRSB}$	$V_{SARHVLSB}$	$V_{DDEVRSBMON}$	UV, OV alarm
V_{DDEXT}	$V_{SARHVLSB}$	$V_{DDEXTMON}$	UV, OV alarm
V_{DDM}	$V_{SARHVLSB}$	V_{DDMMON}	UV, OV alarm

(table continues...)

Table 98 (continued) Secondary voltage monitors parameters

Voltage rail	VMONS LSB datasheet parameter	Secondary voltage monitor accuracy after trimming - datasheet parameter	Effects of secondary voltage monitoring thresholds violation[1)]
V_{DDFLEX}	$V_{SARHVLSB}$	$V_{DDFLEXMON}$	UV, OV alarm
V_{DD}	$V_{SARCORELSB}$	V_{DDMON}	UV, OV alarm
V_{DDPMS0}	$V_{SARCORELSB}$	$V_{DDPMS0MON}$	UV, OV alarm
$V_{DDPMS1,2}$	$V_{SARCORELSB}$	$V_{DDPMS2MON}$	UV, OV alarm
$V_{DDSBRAM}$	$V_{SARCORELSB}$	$V_{DDPMS0MON}$	UV, OV alarm
V_{DDPAD}	$V_{SARCORELSB}$	$V_{DDPADMON}$	UV, OV alarm
$V_{DDPHPHYx}$	$V_{SARHVLSB}$	$V_{DDPHPHYxMON}$	UV, OV alarm
V_{DDHSIF}	$V_{SARHVLSB}$	$V_{DDHSIFMON}$	UV, OV alarm
V_{DDPHYx}	$V_{SARCORELSB}$	$V_{DDPHYxMON}$	UV, OV alarm
V_{DDPPU}	$V_{SARCORELSB}$	$V_{DDPPUMON}$	UV, OV alarm
V_{DDLMUx}	$V_{SARCORELSB}$	$V_{DDLMUMON}$	UV, OV alarm
$V_{DDEXTDC}$	$V_{TRKHVLSB}$	$V_{DDEXTDCMON}$	UV, OV alarm

1) Only if the corresponding VMONS_VxxCON.UVMOD, respectively VMONS_VxxCON.OVMOD, are not zero.

4.15.3.2 Secondary voltage monitors characteristics

Table 99 Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEXTDC}$ secondary supply monitor accuracy after trimming	$V_{DDEXTDCMONCC}$	2.906	2.966	3.026	V	$V_{DDEXTDC}$ = 3.3 V mode; xxVAL monitoring threshold = 2.966 V = 0x106 (UV); FILTER = 0 1)
		5.734	5.852	5.970	V	$V_{DDEXTDC}$ high-voltage mode; xxVAL monitoring threshold = 5.852 V = 0x205 (UV); FILTER = 0 1)
		5.391	5.502	5.613	V	$V_{DDEXTDC}$ = 5 V mode; xxVAL monitoring threshold = 5.502 V = 0x1E6 (OV); FILTER = 0 1)
		6.856	6.996	7.136	V	$V_{DDEXTDC}$ high-voltage mode; xxVAL monitoring threshold = 6.996 V = 0x26A (OV); FILTER = 0 1)
		3.561	3.634	3.707	V	$V_{DDEXTDC}$ = 3.3 V mode; xxVAL monitoring threshold = 3.634 V = 0x141 (OV); FILTER = 0 1)
		4.414	4.505	4.596	V	$V_{DDEXTDC}$ = 5 V mode; xxVAL monitoring threshold = 4.505 V = 0x18D (UV); FILTER = 0 1)

(table continues...)

Table 99 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDEXT} secondary supply monitor accuracy after trimming	$V_{DDEXTMON}$ *CC*	4.410	4.500	4.590	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 *1)*
		5.389	5.499	5.609	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 5.499 V = 0x797 (OV); FILTER = 0 *1)*
		2.909	2.969	3.029	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 *1)*
		3.558	3.631	3.704	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 *1)*
$V_{DDEVRSB}$ secondary supply monitor accuracy after trimming	$V_{DDEVRSBMON}$ *CC*	2.909	2.969	3.029	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 *1)*
		4.410	4.500	4.590	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 *1)*
		3.558	3.631	3.704	V	V_{DDEXT} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 *1)*
		5.389	5.499	5.609	V	V_{DDEXT} = 5 V mode; xxVAL monitoring threshold = 5.499 V = 0x797 (OV); FILTER = 0 *1)*

(table continues...)

Table 99 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDM} secondary supply monitor accuracy after trimming	V_{DDMMON} *CC*	2.909	2.969	3.029	V	V_{DDM} = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 *1)*
		3.558	3.631	3.704	V	V_{DDM} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 *1)*
		5.389	5.499	5.609	V	V_{DDM} = 5 V mode; xxVAL monitoring threshold = 5.499V = 0x797(OV); FILTER = 0 *1)*
		4.410	4.500	4.590	V	V_{DDM} = 5 V mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 *1)*
V_{DDHSIF} secondary supply monitor accuracy after trimming	$V_{DDHSIFMON}$ *CC*	1.627	1.661	1.695	V	V_{DDHSIF} = 1.8 V mode; xxVAL monitoring threshold = 1.661 V = 0x24B(UV); FILTER = 0 *1)*
		1.941	1.981	2.021	V	V_{DDHSIF} = 1.8 V mode; xxVAL monitoring threshold = 1.981 V = 0x2BC(OV); FILTER = 0 *1)*
		2.909	2.969	3.029	V	V_{DDHSIF} = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419(UV); FILTER = 0 *1)*
		3.558	3.631	3.704	V	V_{DDHSIF} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503(OV); FILTER = 0 *1)*
$V_{DDPHPHYx}$ secondary supply monitor accuracy after trimming	$V_{DDPHPHYxMON}$ *CC*	1.586	1.619	1.652	V	xxVAL monitoring threshold = 1.619 V = 0x23C(UV); FILTER = 0 *1)*
		1.941	1.981	2.021	V	xxVAL monitoring threshold = 1.981 V = 0x2BC(OV); FILTER = 0 *1)*

(table continues...)

Table 99 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPHYx} secondary supply monitor accuracy after trimming	$V_{DDPHYxMON}$ *CC*	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 *1)*
		1.084	1.107	1.130	V	xxVAL monitoring threshold = 1.107 V = 0x761(OV); FILTER = 0 *1)*
V_{DD} secondary supply monitor accuracy after trimming *2)*	V_{DDMON} *CC*	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 *1)*
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 *1)*
V_{DDLMU} secondary supply monitor accuracy after trimming	$V_{DDLMUMON}$ *CC*	0.879	0.897	0.915	V	xxVAL monitoring threshold =0.897 V = 0x5FB(UV); FILTER = 0 *1)*
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 *1)*
V_{DDPPU} secondary supply monitor accuracy after trimming	$V_{DDPPUMON}$ *CC*	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 *1)*
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 *1)*
V_{DDPMS0} and $V_{DDSBRAM}$ secondary supply monitor accuracy after trimming *3)*	$V_{DDPMS0MON}$ *CC*	0.768	0.785	0.801	V	xxVAL monitoring threshold = 0.785 V = 0x53B(UV); FILTER = 0 *1)*
		1.079	1.102	1.125	V	xxVAL monitoring threshold = 1.102 V = 0x759(OV); FILTER = 0 *1)*
V_{DDPMS1} and V_{DDPMS2} secondary supply monitor accuracy after trimming *3)*	$V_{DDPMS2MON}$ *CC*	0.778	0.794	0.810	V	xxVAL monitoring threshold = 0.794 V = 0x54B(UV); FILTER = 0 *1)*
		1.129	1.153	1.177	V	xxVAL monitoring threshold = 1.153 V = 0x7B0(OV); FILTER = 0 *1)*

(table continues...)

Table 99 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPAD} secondary supply monitor accuracy after trimming	$V_{DDPADMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 1)
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 1)

1) Static voltage with supply slope less than or equal to 1 kV/s assumed as measurement condition.
2) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. All voltages are measured on pins
3) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.

4.16 Stand-by Controller (SCR)

4.16.1 SCR SAR ADC characteristics

Table 100 SCR SAR ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption on VDDEVRSB supply	$I_{\_VDDEVRSB}$ CC	-	0.7	1.25	mA	when ADC is turned on
Nominal SCR ADC Least Significant Bit Voltage	V_{LSB} CC	-	2.8302	-	mV	11 bit resolution. 5.7962V full range; BACKUP OSC and HPBG trimmed
Wake up Time at Digital Startup	t_{WUADC} CC	436	436	436	cycles	cycle time = 2 / f_{BACKT}
Startup Calibration Time	t_{SCAL} CC	1477	1477	1477	cycles	cycle time = 2 / f_{BACKT}
Sampling Time	t_{SMV} CC	80	-	-	ns	
Conversion Time	t_{convMV} CC	18	18	18	cycles	cycle time = 2 / f_{BACKT}
Integral Non-Linearity	E_{INL} CC	-4	-	4	LSB	HPBG, BACKUP OSC trimmed, ADC calibrated, excluding noise
Differential Non - Linearity	E_{DNL} CC	-1	-	3	LSB	HPBG, BACKUP OSC trimmed, ADC calibrated, excluding noise
Offset Error	E_{OFFSET} CC	-4	-	4	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise

(table continues...)

Table 100 (continued) SCR SAR ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Gain Error	E_{GAIN} CC	-11	-	11	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise
Total Unadjusted Error	E_{TUE} CC	-12	-	12	LSB	0V ≤ V_{IN} ≤ 5.5V; HPBG, BACKUP OSC trimmed and ADC calibrated; excluding noise
RMS Noise	EN_{RMS} CC	-	2	3	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated
Input charge consumption per conversion[1)]	Q_{AIN} CC	-	-	2.5	pC	V_{ain} = $V_{DDEVRSB}$ = 5.5 V
Total Unadjusted Error	E_{TUE} CC	-8	-	8	LSB	0V ≤ VIN ≤ 3.63V; HPBG, BACKUP OSC trimmed and ADC calibrated; excluding noise

1) pad leakage current is not considered and has to be added to the ADC input current

4.17 Temperature sensor characteristics

The temperature monitoring of the TC4DxAA-step COM consists of:

- VTMON DTS
- PMS DTS

The VTMON DTS modules (VTMON.DTS[0:x]) are multiple on-chip temperature sensors at different locations across the microcontroller.

The PMS DTS is a temperature sensor dedicated for the PMS.

4.17.1 VTMON DTS characteristics

Table 101 VTMON DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DTS measurement time for each conversion	t_M *CC*	-	-	2	ms	Measured between consecutive conversions
Temperature difference between DTS instances excluding accuracy	ΔT *CC*	-3	-	3	°C	Based on Real and Max pattern distribution and thermal simulations
Inherent DTS accuracy over temperature range	T_{NL} *CC*	-1	-	1	°C	Total accuracy is defined by T_{ACC}, the sum of T_{CALACC} and T_{NL}
Calibration reference accuracy	T_{CALACC} *CC*	-2	-	2	°C	Calibration points at T_J = -40°C and T_J = 127°C
Total DTS accuracy after calibration and trimming	T_{ACC} *CC*	-3	-	3	°C	$T_{ACC} = T_{CALACC} + T_{NL}$; valid for all VTMON.DTS[0:x] instances
Extended Operating temperature range only for DTS	T_{SR} *SR*	-45	-	ABS T_J (Max)	°C	Junction temperature
Thermal runaway and shutdown monitoring range[1) 2)]	T_{TSD} *CC*	-	-	ABS T_J (Max)	°C	Alarm to SMU to trigger reset

1) The operating temperature range of the device is defined and limited by the operating temperature range definition within the chapter "Operating conditions". It is not allowed to operate the device in the thermal runaway and thermal shutdown range.
2) User has to ensure that the range is adapted according to the specified operating conditions valid for its application.

Related information

PMS DTS characteristics on page 490

4.17.2 PMS DTS characteristics

Table 102 PMS DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DTS measurement time for each conversion	t_M *CC*	-	-	2	ms	Measured between consecutive conversions
Inherent DTS accuracy over temperature range	T_{NL} *CC*	-1	-	1	°C	Total accuracy is defined by TACC, the sum of T_{CALACC} and T_{NL}
Calibration reference accuracy	T_{CALACC} *CC*	-2	-	2	°C	Calibration points at T_J = -40°C and T_J = 127°C
Total DTS accuracy after calibration and trimming	T_{ACC} *CC*	-3	-	3	°C	$T_{ACC} = T_{CALACC} + T_{NL}$
Extended Operating temperature range only for DTS	T_{SR} *SR*	-45	-	165	°C	Junction temperature

Related information

VTMON DTS characteristics on page 489

4.18 Current consumption characteristics

The total power supply current defined here consists of leakage and switching components.

Application relevant values are typically lower than those given in the following tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

4.18.1 Definition of TC4Dx COM application use cases

The power pattern definition for all functional blocks is described in this section.

Table 103 Power pattern conditions

Functional block	Com	Sensor fusion	Max	FreeRUN one CPU
Supply Voltage	VDDEXT, VDDEXTDC, VDDEVRSB = 3.3V+ 2% VDD (TYP) + 2% VDDHSIF (TYP) + 2% VDDPHPHYx and VDDPHYx are not supplied VDD Voltage Scaling active EVRC disabled	VDDEXT, VDDEXTDC, VDDEVRSB = 3.3V+ 2% VDD, VDDPHYx (TYP) + 2% VDDHSIF, VDDPHPHYx (TYP) + 2% VDD Voltage Scaling active EVRC disabled	VDDEXT, VDDEXTDC, VDDEVRSB = 3.3V+ 6% VDD, VDDPHYx (TYP) + 6% VDDHSIF, VDDPHPHYx (TYP) + 6% VDD Voltage Scaling active EVRC disabled	VDDEXT, VDDEXTDC, VDDEVRSB = 3.3V+ 2% VDD, VDDPHYx (TYP) + 2% VDDHSIF, VDDPHPHYx (TYP) + 2% VDD Voltage Scaling active EVRC disabled
Temperature	TJ = 145°C	TJ = 145°C	TJ = 145°C	TJ = 145°C
PACKAGE	COM	COM	COM	COM
PORTS	minimal pattern activity	minimal pattern activity	minimal pattern activity	minimal pattern activity
SMM	RUN1 mode	RUN1 mode	RUN1 mode	RUN1 mode
CLOCK	XTAL = 25 MHz fSYS_PLL_DCO = 1000 MHz fPLL0 = 500 MHz	XTAL = 25 MHz fSYS_PLL_DCO = 1000 MHz fPLL0 = 500 MHz	XTAL = 25 MHz fSYS_PLL_DCO = 1000 MHz fPLL0 = 500 MHz	XTAL = 25 MHz fSYS_PLL_DCO = 1000 MHz fPLL0 = 500 MHz
Bus Interface	fSRI = fFSI2 = 500 MHz, fSPB = fFSI = 100 MHz	fSRI = fFSI2 = fCSS = 500 MHz fSPB = fFSI = 100 MHz	fSRI = fFSI2 = 500 MHz, fSPB = fFSI = 100 MHz	fSRI = fFSI2 = 500 MHz, fSPB = fFSI = 100 MHz
CPU0	CPU active @ 500 MHz and is managing the whole power pattern across modules	CPU active @ 500 MHz and is managing the whole power pattern across modules	CPU active @ 500 MHz and is managing the whole power pattern across modules	CPU active @ 500 MHz executing power pattern
CPU1	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 1.2 IPC max pattern	CPU inactive

(table continues...)

Table 103 (continued) Power pattern conditions

Functional block	Com	Sensor fusion	Max	FreeRUN one CPU
CPU2	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 1.2 IPC max pattern	CPU inactive
CPU3	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 1.2 IPC max pattern	CPU inactive
CPU4	CPU active @ 500 MHz and is managing the whole power pattern across modules	CPU active @ 500 MHz and is managing the whole power pattern across modules	CPU active @ 500 MHz and is managing the whole power pattern across modules	CPU inactive
CPU5	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 0.6 IPC realistic pattern	CPU active @ 500 MHz executing 1.2 IPC max pattern	CPU inactive
DMA0	DMA Real pattern	DMA Real pattern	DMA Max pattern	inactive
DMA1	inactive	DMA Real pattern	DMA Max pattern	inactive
IR	enabled	enabled	enabled	inactive
LMU	LMU off	LMU0 to LMU4 DMA max pattern. All other LMU modules inactive	DMA data transfer between all LMU units as per DMA Max pattern.	inactive

(table continues...)

Table 103 (continued) Power pattern conditions

Functional block	Com	Sensor fusion	Max	FreeRUN one CPU
NVM	Read activity from all Flash modules with 50% dutycycle. Periodic Data Flash write • Assumptions for the 2x data banks: - 50% of the time in Read mode. - Every 1ms write 128B of data into each of the data banks. - Rest of the time is Read-idle. • Assumptions for the 2x program banks: - 50% of the time in Read mode. - Rest of the time is Read-idle.	Read activity from all Flash modules with 50% dutycycle. Periodic Data Flash write • Assumptions for the 2x data banks: - 50% of the time in Read mode. - Every 1ms write 128B of data into each of the data banks. - Rest of the time is Read-idle. • Assumptions for the 2x program banks: - 50% of the time in Read mode. - Rest of the time is Read-idle.	Read activity from all Flash modules with 100% dutycycle. Periodic Data Flash write • Max power pattern: - Only read from NVM. 100% duty cycle for reading, continuous reading. - All 4 banks are in read mode for 100% of the time.	inactive
CSRM				
CSS				

(table continues...)

Table 103 (continued) Power pattern conditions

Functional block	Com	Sensor fusion	Max	FreeRUN one CPU
PPU				
GETH	RGMII active @ 1Gbit/s	SGMII1 active @2.5 Gbit/s GETH Controller @ 250 MHz	SGMII1 active @5 Gbit/s GETH Controller @ 250 MHz	inactive
ETH	RGMII active @1 Gbit/s MII inactive 2x RMII active (LETH)	RGMII inactive MII inactive RMII inactive	RGMII inactive MII inactive RMII inactive	inactive
HSPHY				
PCIe	PCIe0 off PCIe1 off	1xPCIe0 active @8 Gbit/s PCIe Controller @ 250 MHz	1x PCIe1 active @8 Gbit/s PCIe Controller @ 250 MHz	inactive
HSSL	inactive	inactive	active	inactive
xSPI	inactive	active fxSPI = 200 MHz DDR, xSPI400 mode	active fxSPI = 200 MHz DDR, xSPI400 mode	inactive
DRE	LETH2GETH - RMII 100M(MAC1), RMII 100M(GMAC1)	CAN2MEM	GETH2CAN - SGMII0 1Gbit/s	inactive
SDMMC	inactive	inactive	active	inactive
CAN	4 modules active fCAN = 160 MHz	4 modules active fCAN = 160 MHz	5 modules active fCAN = 160 MHz	inactive
CAN XL	inactive	inactive	1 module (w/ 4 nodes) active f_{CANXLH} = 250 MHz f_{CANXL} = 160 MHz	inactive
ERAY	inactive	ERAY0 active fERAY = 80 MHz	ERAY0 and ERAY1 active fERAY = 80 MHz	inactive
LETH				
ASCLIN	4 modules active fASCLINF/S = 200/160 MHz	8 modules active fASCLINF/S = 200/160 MHz	28 modules active fASCLINF/S = 200/160 MHz	inactive

(table continues...)

Table 103 (continued) Power pattern conditions

Functional block	Com	Sensor fusion	Max	FreeRUN one CPU
SENT	inactive	inactive	2 modules active	inactive
PSI5	inactive	inactive	2 modules active	inactive
PSI5S	inactive	inactive	1 module active	inactive
MSC	inactive	inactive	1 modules active	inactive
QSPI	4 modules active fQSPI = 200 MHz	6 modules active fQSPI = 200 MHz	8 modules active fQSPI = 200 MHz	inactive
I2C	2 modules active fI2C = 66.6 MHz	2 modules active fI2C = 66.6 MHz	3 modules active fI2C = 66.6 MHz	inactive
GST	not available	not available	not available	not available
VTMON	All DTS instances active	All DTS instances active	All DTS instances active	inactive
Logic TEST	inactive	inactive	inactive	inactive
VMT	inactive	inactive	inactive	inactive
SCR	inactive	inactive	inactive	inactive
PMS, SCU	default reset state	default reset state	default reset state	default reset state
WTU	Respective CPU units active	Respective CPU units active	Respective CPU units active	Respective CPU units active
SMU	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled
FCE	default reset state	default reset state	FCE active	default reset state
eGTM	3TIM + 3TOM+ 3ATOM active f eGTM = 500 MHz	3TIM + 3TOM+ 3ATOM active f eGTM = 500 MHz	3 TIM + 3 TOM + 3 ATOM active f eGTM = 500 MHz	inactive
GPT12	not available	not available	not available	not available
ADC.TMADC	2 modules active f TMADC = 160 MHz	4 modules active f TMADC = 160 MHz	4 modules active f TMADC = 160 MHz	inactive
ADC.CDSP	inactive	inactive	2 modules active fCDSP = 160 MHz	inactive
DEBUG	inactive	inactive	inactive	inactive
SGBT & TRACE	inactive	inactive	inactive	inactive

***Note**: Modules which are inactive are clock-gated by setting respective module clock control register CLC.DISS = 0x1.*

Related information

Current consumption and power dissipation overview in RUN mode on page 496
Respective supply rail currents in RUN mode on page 498
Current consumption in SLEEP and STANDBY modes on page 500

Load Transients on page 502

4.18.2 Current consumption and power dissipation overview in RUN mode

Table 104 Current consumption and power dissipation overview in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sum of all currents at VDDEXTDC rail with DC-DC EVRC regulator active	$I_{DDTOTDC}$ *CC*	-	-	1900[1)]	mA	Com power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC}$ = 3.3V; V_{DDEXT} (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDHSIF} (Typ) + 2%; $V_{DDPHPHYx}$ (Typ) + 2%; V_{DD} (Typ) + 2%; V_{DDPHYx} (Typ) + 2%
		-	-	2200[1)]	mA	Sensor fusion power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC}$ = 3.3V; V_{DDEXT} (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDHSIF} (Typ) + 2%; $V_{DDPHPHYx}$ (Typ) + 2%; V_{DD} (Typ) + 2%; V_{DDPHYX} (Typ) + 2%
		-	-	2700[1)]	mA	Max power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC}$ = 3.3V; V_{DDEXT} (Typ) + 6%; V_{DDM} (Typ) + 6%; $V_{DDEVRSB}$ (Typ) + 6%; V_{DDHSIF} (Typ) + 6%; $V_{DDPHPHYx}$ (Typ) + 6%; V_{DD} (Typ) + 6%; V_{DDPHYx} (Typ) + 6%

(table continues...)

Table 104 (continued) Current consumption and power dissipation overview in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum power dissipation	*PD SR*	-	-	4700	mW	Com power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC}$ = 3.3V; V_{DDEXT} (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDHSIF} (Typ) + 2%; $V_{DDPHPHYx}$ (Typ) + 2%; V_{DD} (Typ) + 2%; V_{DDPHYx} (Typ) + 2%
		-	-	5700	mW	Sensor fusion power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC}$ = 3.3V; V_{DDEXT} (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDHSIF} (Typ) + 2%; $V_{DDPHPHYx}$ (Typ) + 2%; V_{DD} (Typ) + 2%; V_{DDPHYX} (Typ) + 2%
		-	-	6700	mW	Max power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC}$ = 3.3V; V_{DDEXT} (Typ) + 6%; V_{DDM} (Typ) + 6%; $V_{DDEVRSB}$ (Typ) + 6%; V_{DDHSIF} (Typ) + 6%; $V_{DDPHPHYx}$ (Typ) + 6%; V_{DD} (Typ) + 6%; V_{DDPHYx} (Typ) + 6%

1) $I_{DDEXTDC} = I_{DCNL}$ (EVRC) (Max) + I_{DDEXT} (Max) + I_{DDM} (Max) + $I_{DDEVRSB}$ (Max) + I_{DDHSIF} (Max) + $I_{DDPHPHYx}$ (Max) + [((I_{DD} (Max) + I_{DDPHYx} (Max)) * V_{DD}) / ($V_{DDEXTDC}$ * 72% Efficiency)]

Related information

Definition of TC4Dx COM application use cases on page 491
Respective supply rail currents in RUN mode on page 498
Current consumption in SLEEP and STANDBY modes on page 500
Load Transients on page 502

4.18.3 Respective supply rail currents in RUN mode

Table 105 Respective supply rail currents in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD supply rail currents						
Sum of I_{DD} core supply currents (incl. I_{DD_LEAK}+ I_{DD_DYN})	I_{DD} *CC*	-	-	3650	mA	Freerun power pattern with CPU0 (@max IPC) active; T_J = T_J (Max); V_{DD} (Typ) + 2%
		-	-	4340	mA	Com power pattern; T_J = T_J (Max); V_{DD} (Typ) + 2%
		-	-	5000	mA	Sensor fusion power pattern; T_J = T_J (Max); V_{DD} (Typ) + 2%
		-	-	5300	mA	Max power pattern; T_J = T_J (Max); V_{DD} (Typ) + 6%
VDDEVRSB supply rail currents						
$I_{DDEVRSB}$ supply current (incl. leakage)	$I_{DDEVRSB}$ *CC*	-	-	30	mA	Freerun power pattern; T_J = T_J (Max); $V_{DDEVRSB}$ (Typ) + 2%
		-	-	30	mA	Com power pattern; T_J = T_J (Max); $V_{DDEVRSB}$ (Typ) + 2%
		-	-	34	mA	Max power pattern with SCR; T_J = T_J (Max); $V_{DDEVRSB}$ (Typ) + 6%
VDDEXT supply rail currents						
I_{DDEXT} supply current (incl. leakage and $I_{IEXTLVDS}$)	I_{DDEXT} *CC*	-	-	50[1)]	mA	Com power pattern; T_J = T_J (Max); V_{DDEXT} (Typ) + 2%
		-	-	50	mA	Sensor fusion power pattern; T_J = T_J (Max); V_{DDEXT} (Typ) + 2%
		-	-	60	mA	Max power pattern; T_J = T_J (Max); V_{DDEXT} (Typ) + 6%
VDDFLEX / VDDHSIF (if applicable) supply rail currents						
I_{DDHSIF} supply current (incl. leakage)	I_{DDHSIF} *CC*	-	-	0.45	mA	Freerun power pattern; T_J = T_J (Max); V_{DDHSIF} (Typ) + 2%; Pads in tristate
		-	-	40	mA	Com power pattern; T_J = T_J (Max); V_{DDHSIF} (Typ) + 2%
		-	-	40	mA	Sensor fusion power pattern; T_J = T_J (Max); V_{DDHSIF} (Typ) + 2%
		-	-	80	mA	Max power pattern; T_J = T_J (Max); V_{DDHSIF} (Typ) + 6%

(table continues...)

Table 105 (continued) Respective supply rail currents in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDM supply rail currents						
I_{DDM} supply current (incl. leakage)	I_{DDM} *CC*	-	-	25	mA	Com power pattern; $T_J = T_J$ (Max); V_{DDM} (Typ) + 2%
		-	-	25	mA	Sensor fusion power pattern; $T_J = T_J$ (Max); V_{DDM} (Typ) + 2%
VDDPHPHYx supply rail currents						
$I_{DDPHPHYx}$ supply current (incl. leakage)	$I_{DDPHPHYx}$ *CC*	-	-	3	mA	Freerun power pattern; $T_J = T_J$ (Max); $V_{DDPHPHY}$ (Typ) + 2%; HSPHY disabled
		-	-	3	mA	Com power pattern; $T_J = T_J$ (Max); $V_{DDPHPHYx}$ (Typ) + 2%
		-	-	65	mA	Sensor fusion power pattern; $T_J = T_J$ (Max); $V_{DDPHPHYx}$ (Typ) + 2%
		-	-	90	mA	Max power pattern; $T_J = T_J$ (Max); $V_{DDPHPHYx}$ (Typ) + 6%
VDDPHYx supply rail currents						
I_{DDPHYx} supply current (incl. I_{DDPHYx_LEAK} + I_{DDPHYx_DYN})	I_{DDPHYx} *CC*	-	-	60	mA	Freerun power pattern; $T_J = T_J$ (Max); V_{DDPHY} (Typ) + 2%
		-	-	10	mA	Com power pattern; $T_J = T_J$ (Max); V_{DDPHYx} (Typ) + 2%
		-	-	160	mA	Sensor fusion power pattern; $T_J = T_J$ (Max); V_{DDPHYx} (Typ) + 2%
		-	-	220	mA	Max power pattern; $T_J = T_J$ (Max); V_{DDPHYx} (Typ) + 6%

1) Value is without pad activity

Related information

Definition of TC4Dx COM application use cases on page 491
Current consumption and power dissipation overview in RUN mode on page 496
Current consumption in SLEEP and STANDBY modes on page 500
Load Transients on page 502

4.18.4 Current consumption in SLEEP and STANDBY modes

Table 106 Current consumption in SLEEP and STANDBY modes

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SLEEP mode current consumption						
∑ Sum of all IDD core supply currents in SLEEP mode	I_{SLEEP} *CC*	-	-	100	mA	All CPUs in idle; All peripherals in SLEEP mode; SCR inactive; $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25°C; $V_{DDEXTDC}$ = 5 V; V_{DDEXT} (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DD} = 0.9 V.
∑ Sum of all currents in STANDBY0 mode drawn at VDDEVRSB, VDDEXT, VDDM, VAREF and VDDEXTDC rail	$I_{STANDBY2}$ *CC*	-	115	130	µA	64kB Standby RAM (CPU0 dLMU) supplied; 32kB SCR XRAM not supplied; T_J = 25°C; f_{SCR} = 70 kHz; All rails VDDEVRSB, VDDEXT, VDDM, VAREF and VDDEXTDC rails are supplied with $V_{DDEVRSB}$ (Typ) + 2%.
STANDBY0 mode current consumption without memory retention						
VDDPMS0 Standby domain current in STANDBY0 mode at VDDEVRSB rail	$I_{STBYPMS0}$ *CC*	-	35	-	µA	Standby RAM (dLMU) not supplied; 32kB SCR XRAM not supplied; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDPMS0} + 4%;
STANDBY0 current consumption with memory retention (dLMU)						
VDDPMS0 Standby domain current in STANDBY0 mode at VDDEVRSB rail	$I_{STBYPMS0}$ *CC*	-	50	-	µA	64kB Standby RAM (CPU0 dLMU) supplied; 32kB SCR XRAM not supplied; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDPMS0} + 4%
		-	90[1)]	-	uA	Standby RAM (dLMU) not supplied; 32kB SCR XRAM supplied; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDPMS0} + 4%

(table continues...)

Table 106 (continued) Current consumption in SLEEP and STANDBY modes

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
STANDBY1 mode current consumption						
VDDPMS1 Standby domain current in STANDBY1 mode at VDDEVRSB rail	$I_{STBYPMS1}$ *CC*	-	215	-	µA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 70 kHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%
		-	3.7	-	mA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 1.25 MHz; T_J = 25°C; $V_{DDEVRSB}$ (Typ) + 2%; dI_{SCR}/dt < ±500 uA
		-	7.8	-	mA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 20 MHz; T_J = 85°C; $V_{DDEVRSB}$ (Typ) + 2%; HPOSC and ADCOMP active; dI_{SCR}/dt < ±1 mA
		-	12.8	-	mA	Standby RAM (dLMU) not supplied; SCR active; f_{SCR} = 100 MHz; T_J = 150°C; $V_{DDEVRSB}$ (Typ) + 2%; HPOSC and ADCOMP active; dI_{SCR}/dt < ±3 mA

1) In order not to increase result readings, during Standby Current measurements the GPIOs in VDDEVRSB domain (P32., P33., P34., P35.) shall be defined as follows: All these port pins shall be configured as Inputs and externally connected to GND; TRISTATE shall be enabled

Related information

Definition of TC4Dx COM application use cases on page 491
Current consumption and power dissipation overview in RUN mode on page 496
Respective supply rail currents in RUN mode on page 498
Load Transients on page 502

4.18.5 Load Transients

Table 107 Load Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IDD core dynamic current load jump during LBIST	dI_{DDDYN_LBIST} *CC*	-600	-	800	mA	Key-on LBIST; t_r = 50 µs; t_f = 20 µs; T_{DWELL} > 20us; external regulator untrimmed; EVRC bandgap and clock trimmed but operated with default coefficients; V_{DD} (Typ) - 5%
		-600	-	800	mA	Key-off LBIST; t_r = 50 µs; t_f = 20 µs; T_{DWELL} > 20 µs; external regulator untrimmed; EVRC bandgap and clock trimmed but operated with default coefficients; V_{DD} (Typ) - 3%
IDD core dynamic current load jump during start-up (e.g.: Supply ramp-up, Clock ramp-up, Firmware execution, Processor unit activation, PORST deassertion)	dI_{DDDYN_STRT} *CC*	-270	-	270	mA	t_r = 0.02 µs; t_f = 0.02 µs; T_{DWELL} = 100 µs; regulator untrimmed; V_{DD} (Typ) - 3%; I_{DD} > I_{SLEEP}

Related information

Definition of TC4Dx COM application use cases on page 491
Current consumption and power dissipation overview in RUN mode on page 496
Respective supply rail currents in RUN mode on page 498
Current consumption in SLEEP and STANDBY modes on page 500

4.19 AC characteristics

All AC parameters are specified for the complete operating range defined in Chapter 4.4 unless otherwise noted.
Unless otherwise noted, the timings are defined with the following guidelines:

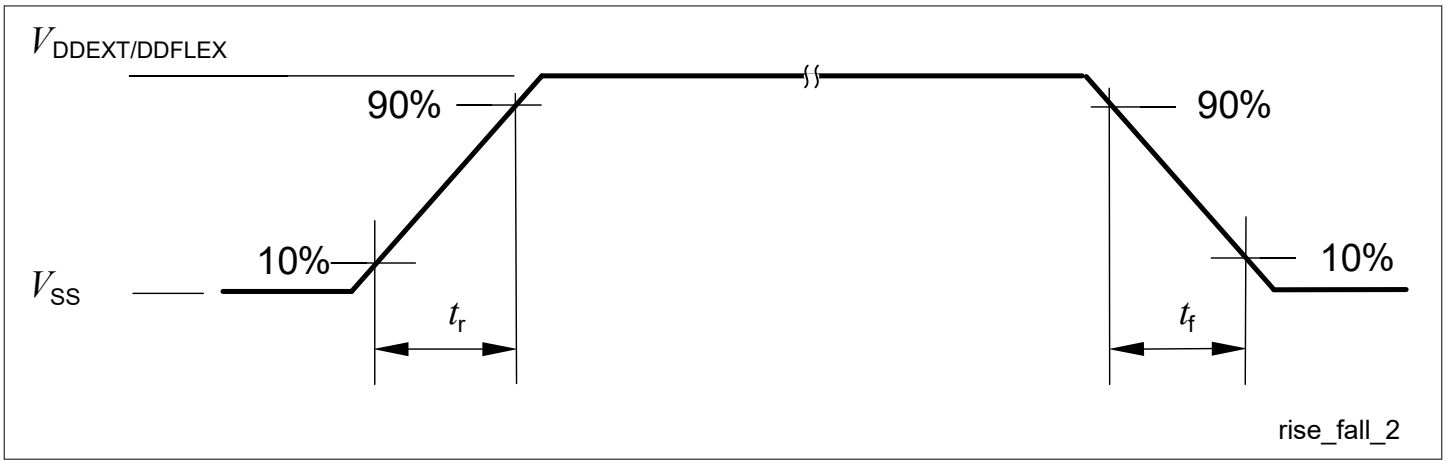


Figure 8 Definition of rise and fall times

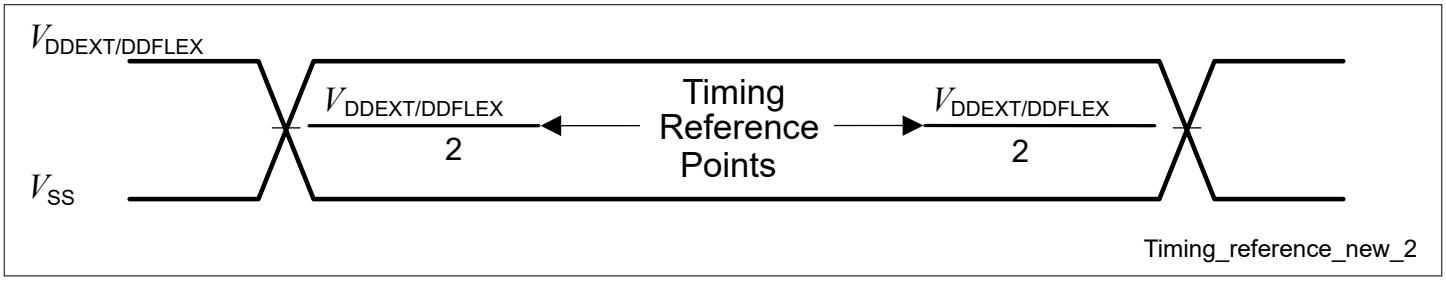


Figure 9 Time Reference Point Definition

4.20 ASCLIN SPI Master timing characteristics

This section defines the timing characteristics for the ASCLIN module in the TC4DxAA-step COM. The specified timing values are split in two sets:

- Speed graded signals with extension _F
- Signals belonging to a defined set of ports grouped to a segment:

Table 108 Segment definition

Segment	Ports	Module
0	Port01, Port02, Port03, Port04	ASCLIN8, ASCLIN9, ASCLIN26
1	Port10, Port13, Port14	ASCLIN0, ASCLIN2, ASCLIN7, ASCLIN10, ASCLIN20, ASCLIN21, ASCLIN22, ASCLIN23
2	Port31, Port32, Port33, Port34, Port35	ASCLIN5, ASCLIN14, ASCLIN15, ASCLIN25
3	Port21, Port22, Port23, Port25, Port30	ASCLIN4, ASCLIN6, ASCLIN11, ASCLIN16, ASCLIN17, ASCLIN18, ASCLIN27
4	Port15, Port16, Port20	ASCLIN1, ASCLIN3, ASCLIN19
5	Port00, Port40	ASCLIN12, ASCLIN13, ASCLIN24

4.20.1 ASCLIN Master Mode timing for strong sharp (ss) output pads

Table 109 ASCLIN Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} *SR*	20	-	-	ns	C_L = 25 pF
Deviation from ideal duty cycle	t_{500} *CC*	-2	-	2	ns	C_L = 25 pF; valid for signals marked with suffix _F and signals mapped to port slices within a segment
MTSR delay from ASCLKO shifting edge	t_{51} *CC*	-3.5	-	3.5	ns	C_L = 25 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.5	-	4.5	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment

(table continues...)

Table 109 (continued) ASCLIN Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASLSOn delay from the first ASCLKO edge	t_{510} *CC*	-3	-	3.5	ns	C_L = 25 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.5	-	3.5	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
MRST setup to ASCLKO latching edge	t_{52} *SR*	25	-	-	ns	C_L = 25 pF
MRST hold from ASCLKO latching edge	t_{53} *SR*	-2	-	-	ns	C_L = 25 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.5	-	-	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment

Related information

ASCLIN Master Mode timing for strong medium (sm) output pads on page 505
ASCLIN Master Mode timing for medium (m) output pads on page 506
ASCLIN SPI Master timing figures on page 507

4.20.2 ASCLIN Master Mode timing for strong medium (sm) output pads

Table 110 ASCLIN Master Mode timing for strong medium (sm) output pads

Note: The following timing parameters are valid for the preferred mappings (with suffix _F) and mappings to port slices of the same segments of the ASCLIN module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} *SR*	50	-	-	ns	C_L = 50 pF

(table continues...)

Table 110 (continued) ASCLIN Master Mode timing for strong medium (sm) output pads

Note: The following timing parameters are valid for the preferred mappings (with suffix _F) and mappings to port slices of the same segments of the ASCLIN module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Deviation from ideal duty cycle	t_{500} *CC*	-5	-	5	ns	C_L = 50 pF
MTSR delay from ASCLKO shifting edge	t_{51} *CC*	-7	-	7	ns	C_L = 50 pF; Valid for all mappings on port slices within a segment except mappings shared with port 16
		-9.5	-	7	ns	C_L = 50 pF; Valid for mappings on port slices within segment 4 between port16 and port15 / port20
ASLSOn delay from the first ASCLKO edge	t_{510} *CC*	-7	-	7	ns	C_L = 50 pF
MRST setup to ASCLKO latching edge	t_{52} *SR*	35	-	-	ns	C_L = 50 pF
MRST hold from ASCLKO latching edge	t_{53} *SR*	-5	-	-	ns	C_L = 50 pF

Related information

ASCLIN Master Mode timing for strong sharp (ss) output pads on page 504
ASCLIN Master Mode timing for medium (m) output pads on page 506
ASCLIN SPI Master timing figures on page 507

4.20.3 ASCLIN Master Mode timing for medium (m) output pads

Table 111 ASCLIN Master Mode timing for medium (m) output pads

Note: The following timing parameters are valid for all mappings of the ASCLIN module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} *SR*	160	-	-	ns	C_L = 50 pF
Deviation from ideal duty cycle	t_{500} *CC*	-10	-	10	ns	C_L = 50 pF
MTSR delay from ASCLKO shifting edge	t_{51} *CC*	-20	-	20	ns	C_L = 50 pF
ASLSOn delay from the first ASCLKO edge	t_{510} *CC*	-20	-	20	ns	C_L = 50 pF
MRST setup to ASCLKO latching edge	t_{52} *SR*	80	-	-	ns	C_L = 50 pF
MRST hold from ASCLKO latching edge	t_{53} *SR*	-15	-	-	ns	C_L = 50 pF

Related information

ASCLIN Master Mode timing for strong sharp (ss) output pads on page 504
ASCLIN Master Mode timing for strong medium (sm) output pads on page 505
ASCLIN SPI Master timing figures on page 507

4.20.4 ASCLIN SPI Master timing figures

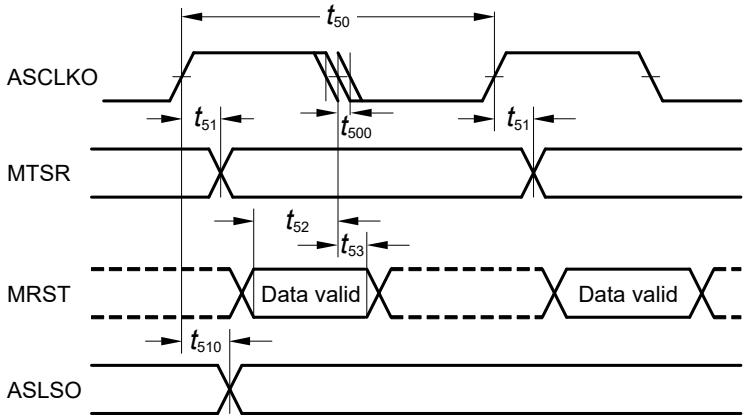


Figure 10 ASCLIN SPI Master Timing

Related information

ASCLIN Master Mode timing for strong sharp (ss) output pads on page 504
ASCLIN Master Mode timing for strong medium (sm) output pads on page 505
ASCLIN Master Mode timing for medium (m) output pads on page 506

4.21 Inter-IC (I2C) interface timing characteristics

The I2C module of the TC4DxAA-step COM supports following operating modes:

- Standard mode for speeds up to 100 kbits/s
- Fast mode for speeds up to 400 kbits/s
- High Speed mode for speeds up to 3.4 Mbits/s

***Note**: All I2C timing values are SR for Master Mode and CC for Slave Mode.*

4.21.1 I2C standard mode timing

Table 112 I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Capacitive load for each bus line	C_b *SR*	-	-	400	pF	
Bus free time between a STOP and START condition	t_{10}	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

(table continues...)

Table 112 (continued) I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Set-up time for STOP condition	t_9	4	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

Related information

I2C fast mode timing on page 509
I2C high speed mode timing on page 510
I2C standard and fast mode timing figures on page 511

4.21.2 I2C fast mode timing

Table 113 I2C fast mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1* C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Capacitive load for each bus line	C_b *SR*	-	-	400	pF	
Bus free time between a STOP and START condition	t_{10}	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1* C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

(table continues...)

Table 113 (continued) I2C fast mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Set-up time for (repeated) START condition	t_8	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

Related information

I2C standard mode timing on page 508
I2C high speed mode timing on page 510
I2C standard and fast mode timing figures on page 511

4.21.3 I2C high speed mode timing

Table 114 I2C high speed mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b *SR*	-	-	400	pF	
Fall time of SCL	t_{11}	10[1)]	-	40[1)]	ns	Bus line load C_b = 100 pF
Fall time of SDA	t_{12}	10[1)]	-	80[1)]	ns	Bus line load C_b = 100 pF
Rise time of SCL	t_{13}	10[1)]	-	40[1)]	ns	Bus line load C_b = 100 pF
Rise time of SDA	t_{14}	10[1)]	-	80[1)]	ns	Bus line load C_b = 100 pF
Data hold time	t_3	0[1)]	-	70[1)]	ns	Bus line load C_b = 100 pF
Data set-up time	t_4	10[1)]	-	-	ns	Bus line load C_b = 100 pF
Low period of SCL clock	t_5	160[1)]	-	-	ns	Bus line load C_b = 100 pF
High period of SCL clock	t_6	60[1)]	-	-	ns	Bus line load C_b = 100 pF
Hold time for the (repeated) START condition	t_7	160[1)]	-	-	ns	Bus line load C_b = 100 pF
Set-up time for (repeated) START condition	t_8	160[1)]	-	-	ns	Bus line load C_b = 100 pF
Set-up time for STOP condition	t_9	160[1)]	-	-	ns	Bus line load C_b = 100 pF

1) Values are defined for C_b = 100 pF, for the Timing of C_b = 400 pF see the I2C Standard.

Related information

I2C standard mode timing on page 508
I2C fast mode timing on page 509
I2C standard and fast mode timing figures on page 511

4.21.4 I2C standard and fast mode timing figures

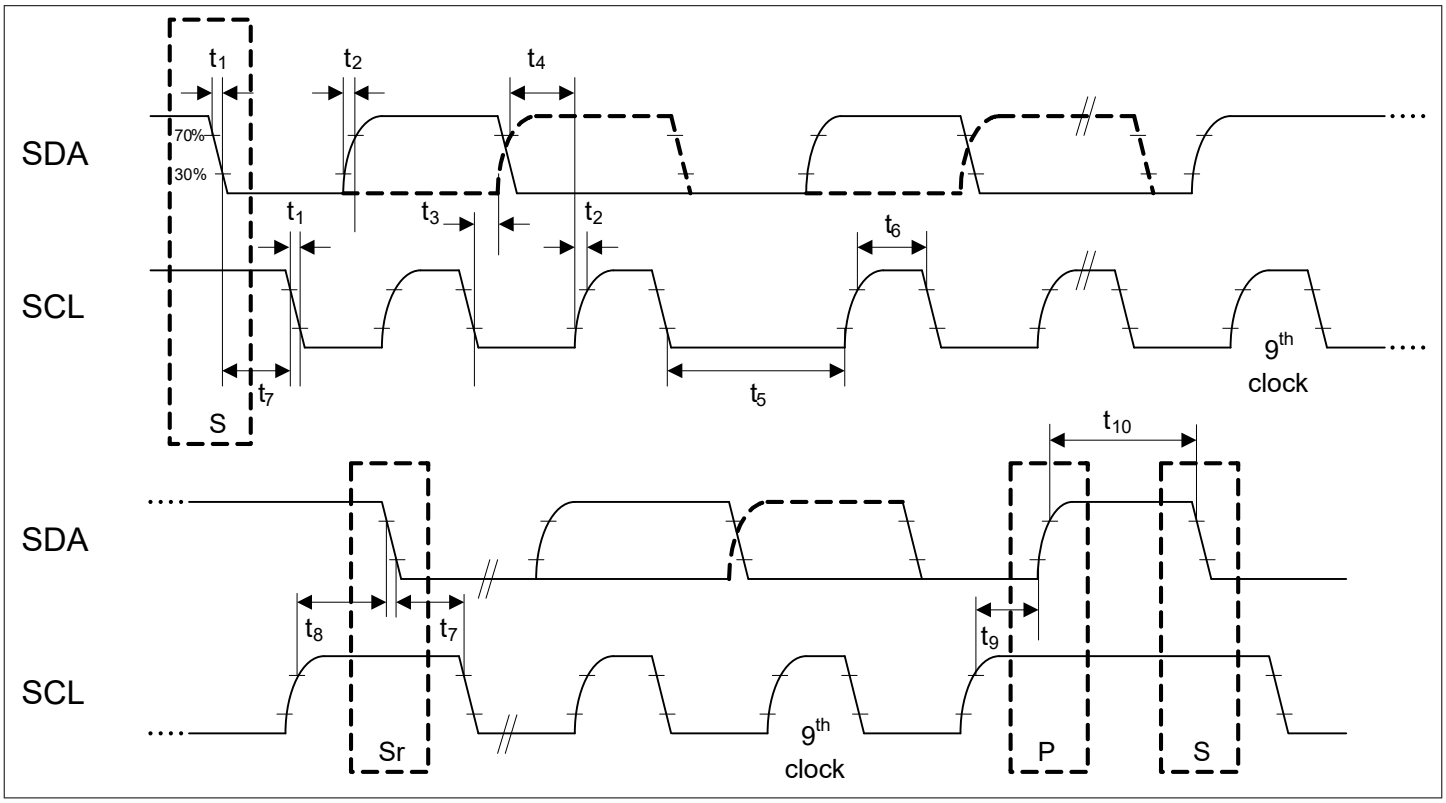


Figure 11 I2C standard and fast mode timing

Related information

I2C standard mode timing on page 508
I2C fast mode timing on page 509
I2C high speed mode timing on page 510

4.22 CAN characteristics

4.22.1 CAN internal receive delay for all pads

Table 115 CAN internal receive delay for all pads

The RX delay is the time measured from pad input to input of the CAN RXD input buffer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX delay	t_{RXD} *CC*	-	-	15 + (2*(1/f_{MCAN}))	ns	

4.22.2 CAN internal transmit delay for HSFast output pads

Table 116 CAN internal transmit delay for HSFast output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	16	ns	HSFast 3.3V GPIO - PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$; $C_L \leq 10$ pF
		-	-	22	ns	HSFast 1.8V GPIO - PADCFG.DRVCFG.PD [2:0] = $000_{(2)}$; $C_L \leq 10$ pF

4.22.3 CAN internal transmit delay for strong sharp (ss) output pads

Table 117 CAN internal transmit delay for strong sharp (ss) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	13.60	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	15.85	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF

4.22.4 CAN internal transmit delay for medium (m) output pads

Table 118 CAN internal transmit delay for medium (m) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	33.25	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF
		-	-	33.25	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF

4.22.5 CAN internal transmit delay for strong medium (sm) output pads

Table 119 CAN internal transmit delay for strong medium (sm) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	19.75	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	19.25	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF

4.23 CAN XL characteristics

4.23.1 CANXL internal receive delay for all pads

Table 120 CANXL internal receive delay for all pads

The RX delay is the time measured from pad input to input of the CANXL RXD input buffer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX delay	t_{RXD} *CC*	-	-	15 + (2*(1/f_{CANXL}))	ns	

4.23.2 CANXL internal transmit delay for strong sharp (ss) output pads

Table 121 CANXL internal transmit delay for strong sharp (ss) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	16.10	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	18	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF

4.23.3 CANXL internal transmit delay for medium (m) output pads

Table 122 CANXL internal transmit delay for medium (m) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	35.75	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF
		-	-	36.25	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq$ 10 pF

4.23.4 CANXL internal transmit delay for strong medium (sm) output pads

Table 123 CANXL internal transmit delay for strong medium (sm) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	t_{intern_TXD} *CC*	-	-	21.90	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq$ 10 pF
		-	-	25.40	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq$ 10 pF

4.24 E-Ray characteristics

The timing characteristics of following sub-chapter are valid for the driver setting = strong and edge configuration = sharp of the output drivers with a load capacitance of C_L = 25 pF.

4.24.1 Transmit characteristics

Table 124 Transmit characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25}$ *CC*	-	-	9	ns	C_L = 25 pF
Fall time of TxEN	$t_{dCCTxENFall25}$ *CC*	-	-	9	ns	C_L = 25 pF
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25}$ *CC*	-	-	9	ns	20% - 80%; C_L = 25 pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01}$ *CC*	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10}$ *CC*	-	-	25	ns	
Asymmetry of sending	t_{tx_asym} *CC*	-2.45	-	2.45	ns	C_L = 25 pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01}$ *CC*	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10}$ *CC*	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	t_{txd_sum} *CC*	-	-	9	ns	

Related information

Receive characteristics on page 516

4.24.2 Receive characteristics

Table 125 Receive characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept25}$ *SR*	-30.5	-	43.0	ns	C_L = 25 pF
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept15}$ *SR*	-31.5	-	44.0	ns	C_L = 15 pF
Threshold for detecting logical high	$T_{uCCLogic1}$ *SR*	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}$ *SR*	30	-	65	%	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ *CC*	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ *CC*	-	-	10	ns	

Related information

Transmit characteristics on page 515

4.25 MSC 5V timing characteristics

The following sub-chapters include the 5V timing characteristics of the Microsecond Channel (MSC) module. For the specified timing values it is assumed that FCLPx, SOPx, and ENx pads have the same pad settings.

The below listed tables contain the clock period T_A. $T_A = 1/f_A$ where f_A is the input clock frequency of the MSC ABRA block (see also User Manual Chapter MSC).

In case the MSC ABRA block is bypassed T_A is defined as $T_A = 1/f_{MSC}$ where f_{MSC} is the input clock frequency without ABRA block up to 50 MHz (see User Manual Chapter MSC Baud rate configuration).

***Note**: Pad asymmetry (defined by parameter t_{TX_ASYM}) is already included in the timing characteristics that follow.*

***Note**: The following timing characteristics are only valid for MSC modules 0, 2 and 3.*

4.25.1 MSC clock/data timing for strong sharp (ss) 5V output pads

Table 126 MSC clock/data timing for strong sharp (ss) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	C_L = 50 pF
Deviation from ideal duty cycle	t_{400} CC	-2	-	2	ns	C_L = 50 pF
SOPx output delay	t_{44} CC	-4	-	3.5	ns	C_L = 50 pF
ENx output delay	t_{45} CC	-4	-	3.5	ns	C_L = 50 pF

Related information

MSC clock/data timing for strong medium (sm) 5V output pads on page 517
MSC clock/data timing for medium (m) 5V output pads on page 517
MSC clock/data timing for LVDS 5V output pads on page 518
Upstream interface timing on page 519
MSC clock/data timing figures on page 519

4.25.2 MSC clock/data timing for strong medium (sm) 5V output pads

Table 127 MSC clock/data timing for strong medium (sm) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	C_L = 50 pF
Deviation from ideal duty cycle	t_{400} CC	-5	-	5	ns	C_L = 50 pF
SOPx output delay	t_{44} CC	-7	-	7	ns	C_L = 50 pF
ENx output delay	t_{45} CC	-7	-	7	ns	C_L = 50 pF

Related information

MSC clock/data timing for strong sharp (ss) 5V output pads on page 517
MSC clock/data timing for medium (m) 5V output pads on page 517
MSC clock/data timing for LVDS 5V output pads on page 518
Upstream interface timing on page 519
MSC clock/data timing figures on page 519

4.25.3 MSC clock/data timing for medium (m) 5V output pads

Table 128 MSC clock/data timing for medium (m) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	C_L = 50 pF
Deviation from ideal duty cycle	t_{400} CC	-10	-	10	ns	C_L = 50 pF

(table continues...)

Table 128 (continued) MSC clock/data timing for medium (m) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SOPx output delay	t_{44} CC	-20	-	20	ns	C_L = 50 pF
ENx output delay	t_{45} CC	-20	-	20	ns	C_L = 50 pF

Related information

MSC clock/data timing for strong sharp (ss) 5V output pads on page 517
MSC clock/data timing for strong medium (sm) 5V output pads on page 517
MSC clock/data timing for LVDS 5V output pads on page 518
Upstream interface timing on page 519
MSC clock/data timing figures on page 519

4.25.4 MSC clock/data timing for LVDS 5V output pads

Table 129 MSC clock/data timing for LVDS 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A 1) 2) 3)	-	-	ns	LVDS; C_L = 50 pF
Deviation from ideal duty cycle	t_{400} CC	-1 1)	-	1 1)	ns	LVDS; 0 < C_L < 50 pF
SOPx output delay	t_{44} CC	-3 1)	-	3 1)	ns	C_L = 50 pF
ENx output delay	t_{45} CC	-4 1)	-	5 1)	ns	ss; C_L = 50 pF; ABRA block bypassed
		-4 1)	-	4 1)	ns	ss; C_L = 50 pF; ABRA block used
		-2 1)	-	10 1)	ns	sm; C_L = 50 pF
		-30 1)	-	30 1)	ns	m; C_L = 50 pF

1) The load (C_L=50pF) defined in the condition list is a load definition for the single end signal EN and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.
2) T_A depends on the clock source selected for baud rate generation in the ABRA block of the MSC.
3) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.

Related information

MSC clock/data timing for strong sharp (ss) 5V output pads on page 517
MSC clock/data timing for strong medium (sm) 5V output pads on page 517
MSC clock/data timing for medium (m) 5V output pads on page 517
Upstream interface timing on page 519
MSC clock/data timing figures on page 519

4.25.5 Upstream interface timing

Table 130 Upstream interface timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SDI bit time	t_{46} *SR*	8 * t_{MSC}	-	-	ns	
SDI rise time	t_{48} *SR*	-	-	200	ns	
SDI fall time	t_{49} *SR*	-	-	200	ns	

Related information

MSC clock/data timing for strong sharp (ss) 5V output pads on page 517
MSC clock/data timing for strong medium (sm) 5V output pads on page 517
MSC clock/data timing for medium (m) 5V output pads on page 517
MSC clock/data timing for LVDS 5V output pads on page 518
MSC clock/data timing figures on page 519

4.25.6 MSC clock/data timing figures

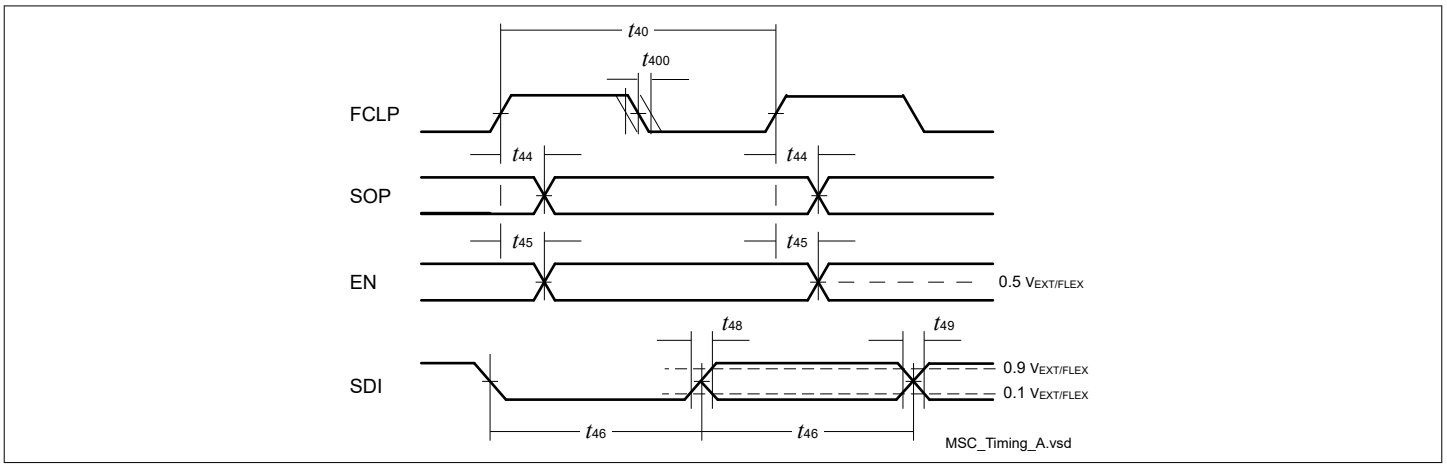


Figure 12 MSC clock/data timing

Related information

MSC clock/data timing for strong sharp (ss) 5V output pads on page 517
MSC clock/data timing for strong medium (sm) 5V output pads on page 517
MSC clock/data timing for medium (m) 5V output pads on page 517
MSC clock/data timing for LVDS 5V output pads on page 518
Upstream interface timing on page 519

4.26 QSPI timing characteristics, Master and Slave Mode

This section defines the timings for the QSPI in the TC4DxAA-step COM. For the specified timing values it is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings. The specified timing values are split in two sets:

- Speed graded signals with extension _F
- Signals belonging to a defined set of ports grouped to a segment:

Table 131 Segment definition

Segment	Ports	Module
0	Port01, Port02, Port03, Port04	QSPI3
1	Port10, Port13, Port14	QSPI1, QSPI2
2	Port31, Port32, Port33, Port34, Port35	QSPI5
3	Port21, Port22, Port23, Port25, Port30	QSPI4, QSPI6
4	Port15, Port16, Port20	QSPI0, QSPI7

4.26.1 QSPI Master Mode timing characteristics

***Note**: Pad asymmetry (defined by parameter t_{TX_ASYM}) is already included in the timing characteristics that follow.*

***Note**: The following timings are only valid when the same pad type with the same speed grade configuration are used for all output signals.*

4.26.1.1 QSPI Master Mode timing for strong sharp (ss) output pads

Table 132 QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	C_L = 25 pF
		20	-	-	ns	C_L = 25 pF; only valid for simplex mode
Deviation from the ideal duty cycle	t_{500} CC	-3.5	-	2.5	ns	C_L = 25 pF; timing parameter is valid for all other QSPI signals (apart _F) mapped to port slices within a segment
		-2	-	2	ns	C_L = 25 pF; timing parameter is only valid for the preferred QSPI module mappings (_F)

(table continues...)

Table 132 (continued) QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-4	-	5	ns	C_L = 25 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-5	-	5	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-4	-	5	ns	C_L = 25 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.5	-	5	ns	C_L = 25 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
MRST setup to SCLK latching edge	t_{52} *SR*	25[1) 2)]	-	-	ns	C_L = 25 pF
MRST hold from SCLK latching edge	t_{53} *SR*	-2[1) 2)]	-	-	ns	C_L = 25 pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

QSPI Master Mode timing for strong medium (sm) output pads on page 522
QSPI Master Mode timing for medium (m) output pads on page 523
QSPI Master Mode timing for LVDS output pads (clock/data) on page 524
QSPI Master Mode timing figures on page 525

4.26.1.2 QSPI Master Mode timing for strong medium (sm) output pads

Table 133 QSPI Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	50	-	-	ns	C_L = 50 pF
Deviation from the ideal duty cycle	t_{500} *CC*	-5	-	5	ns	C_L = 50 pF
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-7	-	7	ns	C_L = 50 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = medium. Signals mapped to those pads are marked with suffix _F
		-10	-	8.5	ns	C_L = 50 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-7	-	7	ns	C_L = 50 pF; valid for identical pad types of category Fast with configuration driver = strong and edge = medium. Signals mapped to those pads are marked with suffix _F
		-9.5	-	9	ns	C_L = 50 pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
MRST setup to SCLK latching edge	t_{52} *SR*	35[1) 2)]	-	-	ns	C_L = 50 pF
MRST hold from SCLK latching edge	t_{53} *SR*	-5[1) 2)]	-	-	ns	C_L = 50 pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 520
QSPI Master Mode timing for medium (m) output pads on page 523
QSPI Master Mode timing for LVDS output pads (clock/data) on page 524
QSPI Master Mode timing figures on page 525

4.26.1.3 QSPI Master Mode timing for medium (m) output pads

Table 134 QSPI Master Mode timing for medium (m) output pads

Note: The following timing parameters are valid for all mappings of the QSPI module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	160	-	-	ns	C_L = 50 pF
Deviation from the ideal duty cycle	t_{500} *CC*	-10	-	10	ns	C_L = 50 pF
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-20	-	20	ns	C_L = 50 pF
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-20	-	20	ns	C_L = 50 pF
MRST setup to SCLK latching edge	t_{52} *SR*	80[1) 2)]	-	-	ns	C_L = 50 pF
MRST hold from SCLK latching edge	t_{53} *SR*	-15[1) 2)]	-	-	ns	C_L = 50 pF; QSPI; valid for identical pad types of category Fast with configuration driver = medium and edge = medium
		-14[1) 2)]	-	-	ns	C_L = 50 pF; QSPI; valid for mixed pad types of category Fast, HSFast and Slow with identical configuration driver = medium, edge = medium
		-13[1) 2)]	-	-	ns	C_L = 50 pF; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 520
QSPI Master Mode timing for strong medium (sm) output pads on page 522
QSPI Master Mode timing for LVDS output pads (clock/data) on page 524
QSPI Master Mode timing figures on page 525

4.26.1.4 QSPI Master Mode timing for LVDS output pads (clock/data)

Table 135 QSPI Master Mode timing for LVDS output pads (clock/data)

Note: The following timing parameters are valid for the preferred mappings (with suffix _F) and mappings to port slices of the same segments of the QSPI module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} *CC*	50[1]	-	-	ns	C_L = 25 pF
		20[1]	-	-	ns	C_L = 25 pF; only valid for simplex mode
Deviation from the ideal duty cycle	t_{500} *CC*	-1[1]	-	1[1]	ns	C_L = 25 pF
MTSR delay from SCLKO shifting edge	t_{51} *CC*	-3[1]	-	4[1]	ns	C_L = 25 pF
SLSOn deviation from the ideal programmed position	t_{510} *CC*	-4[1]	-	7.5[1]	ns	C_L = 25 pF; driver strength ss
		-10[1]	-	13.5[1]	ns	C_L = 25 pF; driver strength sm
		-30[1]	-	30[1]	ns	C_L = 25 pF; driver strength m
MRST setup to SCLK latching edge	t_{52} *SR*	18[1]	-	-	ns	C_L = 25 pF; valid for LVDS Input pads only
MRST hold from SCLK latching edge	t_{53} *SR*	-1[1]	-	-	ns	C_L = 25 pF; valid for LVDS Input pads only

1) The load (C_L = 25 pF) defined in the condition list is a load definition for the single end signal SLSO and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 520
QSPI Master Mode timing for strong medium (sm) output pads on page 522
QSPI Master Mode timing for medium (m) output pads on page 523
QSPI Master Mode timing figures on page 525

4.26.1.5 QSPI Master Mode timing figures

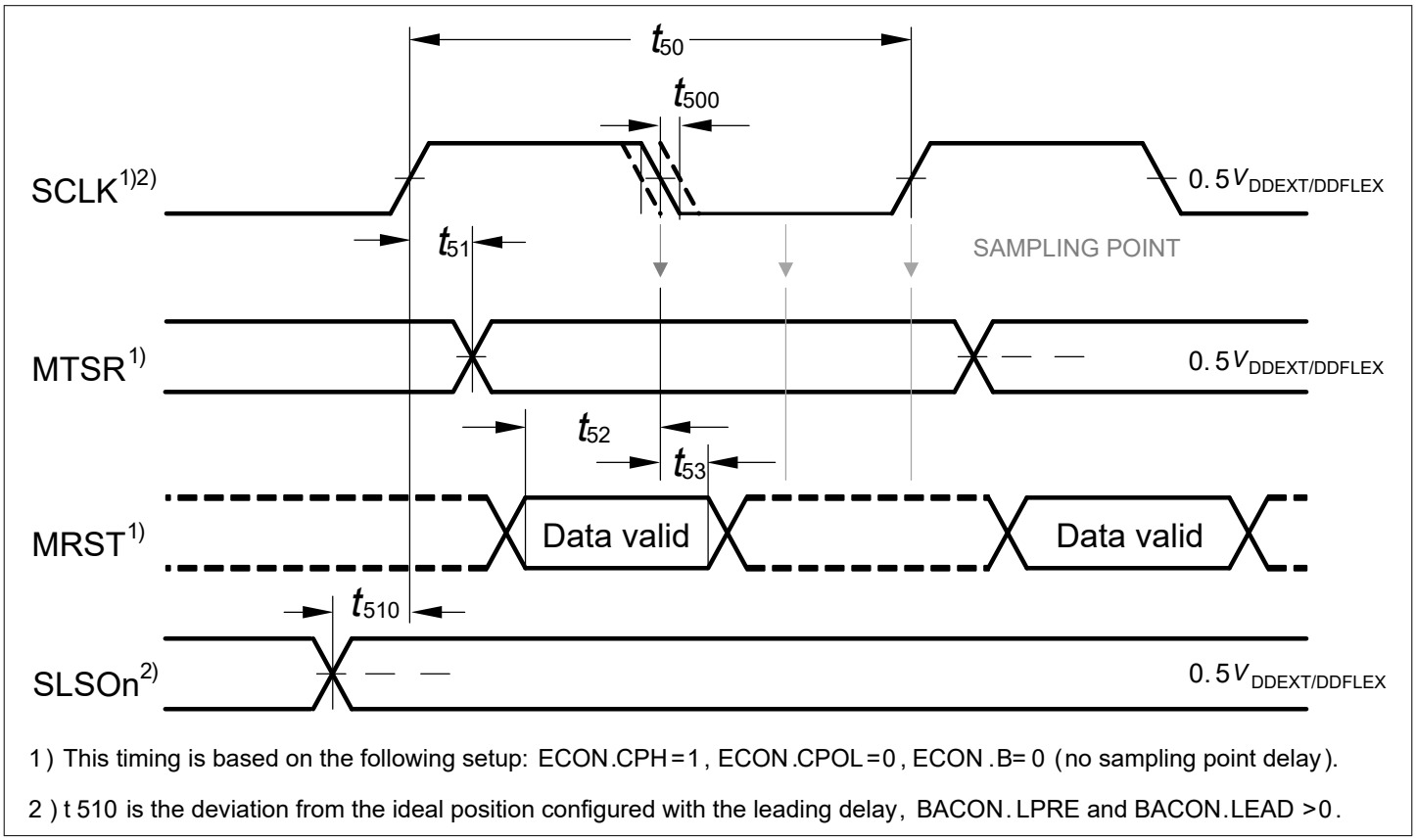


Figure 13 QSPI master mode timing

Related information

QSPI Master Mode timing for strong sharp (ss) output pads on page 520
QSPI Master Mode timing for strong medium (sm) output pads on page 522
QSPI Master Mode timing for medium (m) output pads on page 523
QSPI Master Mode timing for LVDS output pads (clock/data) on page 524

4.26.2 QSPI Slave Mode timing characteristics

4.26.2.1 QSPI Slave Mode timing

Table 136 QSPI Slave Mode timing

Note: The following timing parameters are valid for the preferred mappings (with suffix _F) and mappings to port slices of the same segments of the QSPI module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} *SR*	4 x T_{Max} 1)	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ *SR*	40	-	60	%	

(table continues...)

Table 136 (continued) QSPI Slave Mode timing

Note: The following timing parameters are valid for the preferred mappings (with suffix _F) and mappings to port slices of the same segments of the QSPI module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR setup to SCLK latching edge	t_{56} *SR*	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MTSR hold from SCLK latching edge	t_{57} *SR*	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} *SR*	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} *SR*	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} *CC*	5	-	35	ns	driver = strong, edge = medium; C_L = 50 pF
		2	-	24	ns	driver = strong, edge = sharp; C_L = 50 pF
		14	-	-	ns	medium driver; C_L = 50 pF; QSPI
		14	-	-	ns	medium driver; C_L = 50 pF; SCR SSC
		-	-	80	ns	medium driver; C_L = 50 pF

1) $T_{MAX} = 1/f_{QSPI}$ (Max)

Related information

QSPI Slave Mode timing figures on page 526

4.26.2.2 QSPI Slave Mode timing figures

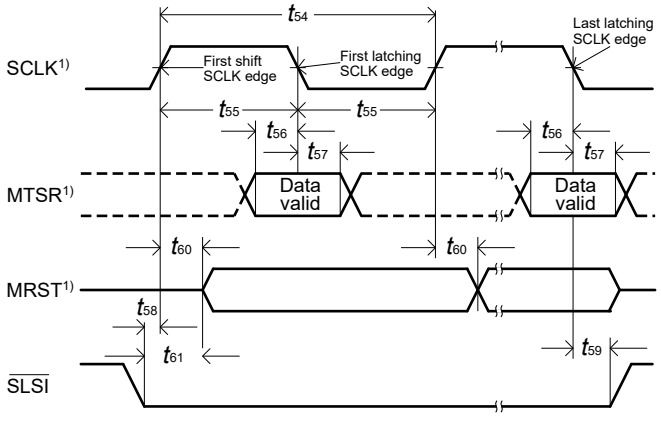


Figure 14 Slave mode timing

Related information

QSPI Slave Mode timing on page 525

4.27 SDMMC Interface timing characteristics

4.27.1 SDMMC timing

Table 137 SDMMC timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock period Data Transfer Mode	t_1 *CC*	20	-	-	ns	Push-pull; $C_L \leq 30$ pF; V_{DDEXT} = 3.3 V
Clock period Indentification Mode	t_2 *CC*	-	-	2500	ns	Open-drain; $C_L \leq 30$ pF; V_{DDEXT} = 3.3 V
Clock low time	t_3 *CC*	6.5	-	-	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V
Clock high time	t_4 *CC*	6.5	-	-	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V
Data output valid time before rising clock edge	t_5 *CC*	3	-	-	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V
Data output valid time after rising clock edge	t_6 *CC*	3	-	-	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V
Data input hold time	t_7 *SR*	2.5	-	-	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V; TTL levels
Data Input delay time	t_8 *SR*	-	-	13.7	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V; TTL levels
Data Input setup time	t_9 *SR*	5.2	-	-	ns	$C_L \leq 30$ pF; V_{DDEXT} = 3.3 V; TTL levels

Related information

SDMMC timing figure on page 528

4.27.2 SDMMC timing figure

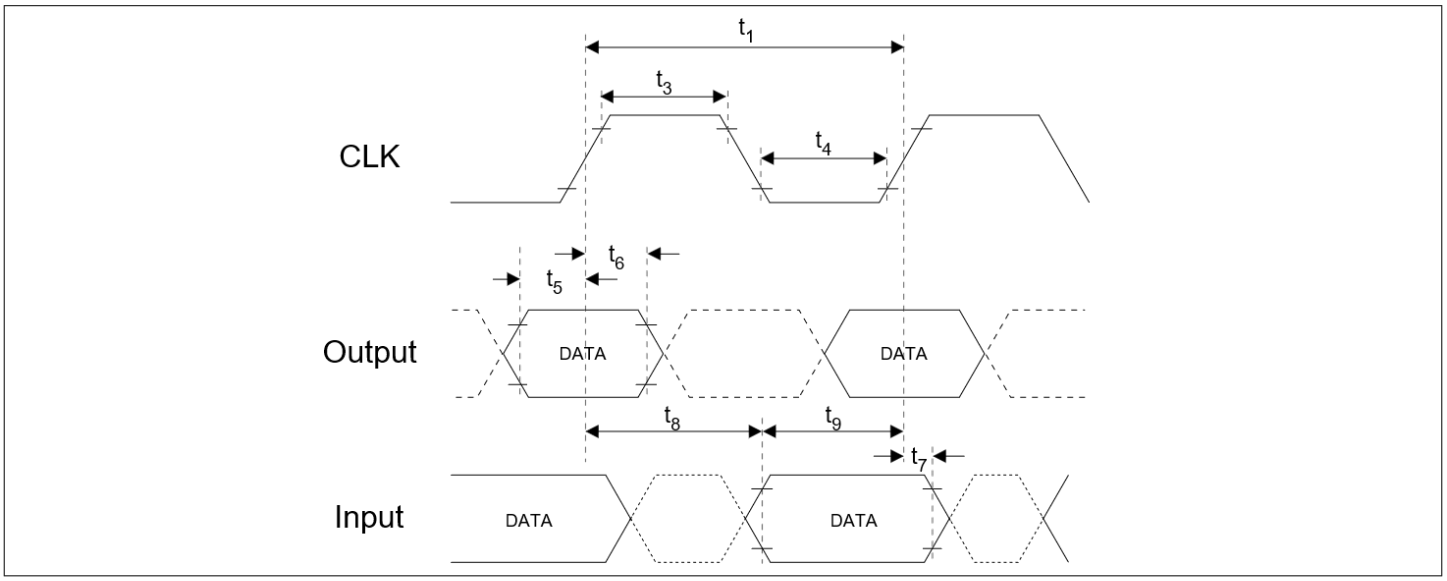


Figure 15 SDMMC Timing

Related information
SDMMC timing on page 527

4.28 HSCT characteristics

4.28.1 HSCT - Rx parasitics and loads

Table 138 HSCT - Rx parasitics and loads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Parasitic inductance budget	H_{total} *CC*	-	5	-	nH	
Capacitance total budget	C_{total} *CC*	-	3.5	5	pF	Total Budget for complete receiver including silicon, package, pins and bond wire

Related information
HSCT - Rx/Tx setup timing characteristics on page 528
HSCT characteristics on page 529

4.28.2 HSCT - Rx/Tx setup timing characteristics

Table 139 HSCT - Rx/Tx setup timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Disable time of the LVDS pad	$t_{LVDSDIS}$ *CC*	-	-	20	ns	

(table continues...)

Table 139 (continued) HSCT - Rx/Tx setup timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX o/p duty cycle	*DCrx CC*	40	-	60	%	
Wakeup time from Sleep Mode	t_{SWU} *CC*	-	-	250	ns	
RX start-up time	t_{rxi} *CC*	-	-	600	ns	Wake-up RX from power down.
TX start-up time	t_{tx} *CC*	-	-	280	ns	Wake-up TX from power down.

Related information

HSCT - Rx parasitics and loads on page 528
HSCT characteristics on page 529

4.28.3 HSCT characteristics

Table 140 HSCT characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Bit Error Rate based on 20 MHz reference clock at Slave PLL side	BER_{20} *CC*	-	-	10EXP-12		at 320 Mbps with 20 MHz Sysclk
Bit Error Rate based on 25 MHz reference clock at Slave PLL side	BER_{25} *CC*	-	-	10EXP-12		at 320 Mbps with 25 MHz Sysclk
Transition time from RX Disable to RX Low Speed Mode	t_{DISLS} *CC*	-	-	1000	ns	Transition time from RX Disable to RX Low Speed Mode
Transition time from RX High/Low Speed Mode to RX Medium Speed Mode	t_{HLSMS} *CC*	-	-	500	ns	Transition time from RX High/Low Speed Mode to RX Medium Speed Mode
Transition time from RX High/ Medium Speed Mode to RX Low Speed Mode	t_{HMSLS} *CC*	-	-	700	ns	Transition time from RX High/ Medium Speed Mode to RX Low Speed Mode
Transition time from TX High Speed Mode to TX Low Speed Mode	t_{HSLS} *CC*	-	-	800	ns	Transition time from TX High Speed Mode to TX Low Speed Mode
Transition time from TX Low Speed Mode to TX High Speed Mode	t_{LSHS} *CC*	-	-	500	ns	Transition time from TX Low Speed Mode to TX High Speed Mode
Transition time from RX Medium/Low Speed Mode to RX High Speed Mode	t_{MLSHS} *CC*	-	-	400	ns	Transition time from RX Medium/Low Speed Mode to RX High Speed Mode
HSCT physical layer power-on	t_{PON} *CC*	-	-	1.5	µs	HSCT physical layer power-on

Related information

HSCT - Rx parasitics and loads on page 528
HSCT - Rx/Tx setup timing characteristics on page 528

4.29 Ethernet Interface (ETH) timing characteristics

4.29.1 ETH definition of measurement reference points

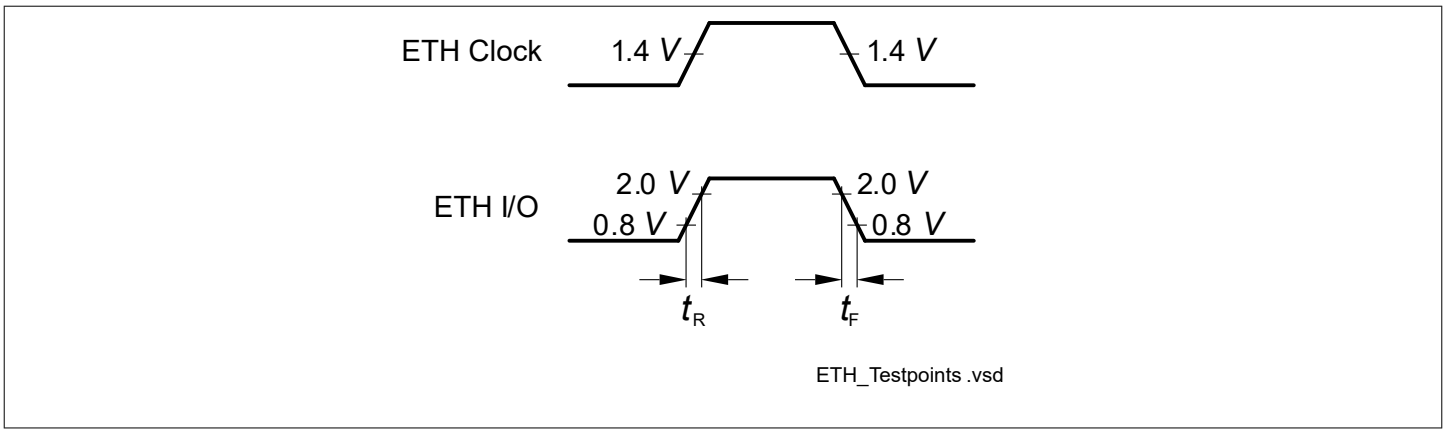


Figure 16 ETH Measurement Reference Points

4.29.2 ETH Management signal timing characteristics (ETH_MDC, ETH_MDIO)

The timing characteristics listed in the following sub-chapter are valid for the Ethernet (ETH) management signals MDC Management Data clock) and MDIO (Management Data Input/output).

4.29.2.1 ETH management signal timing valid for 3.3V

Table 141 ETH management signal timing valid for 3.3V

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 *CC*	80	-	-	ns	C_L = 25 pF
ETH_MDC high time	t_2 *CC*	16	-	-	ns	C_L = 25 pF
ETH_MDC low time	t_3 *CC*	16	-	-	ns	C_L = 25 pF
ETH_MDIO setup time (output)	t_4 *CC*	10	-	-	ns	C_L = 25 pF
ETH_MDIO hold time (output)	t_5 *CC*	10	-	-	ns	C_L = 25 pF
ETH_MDIO data valid (input)	t_6 *SR*	0	-	20	ns	C_L = 25 pF

Related information

ETH management signal timing figures on page 531

4.29.2.2 ETH management signal timing figures

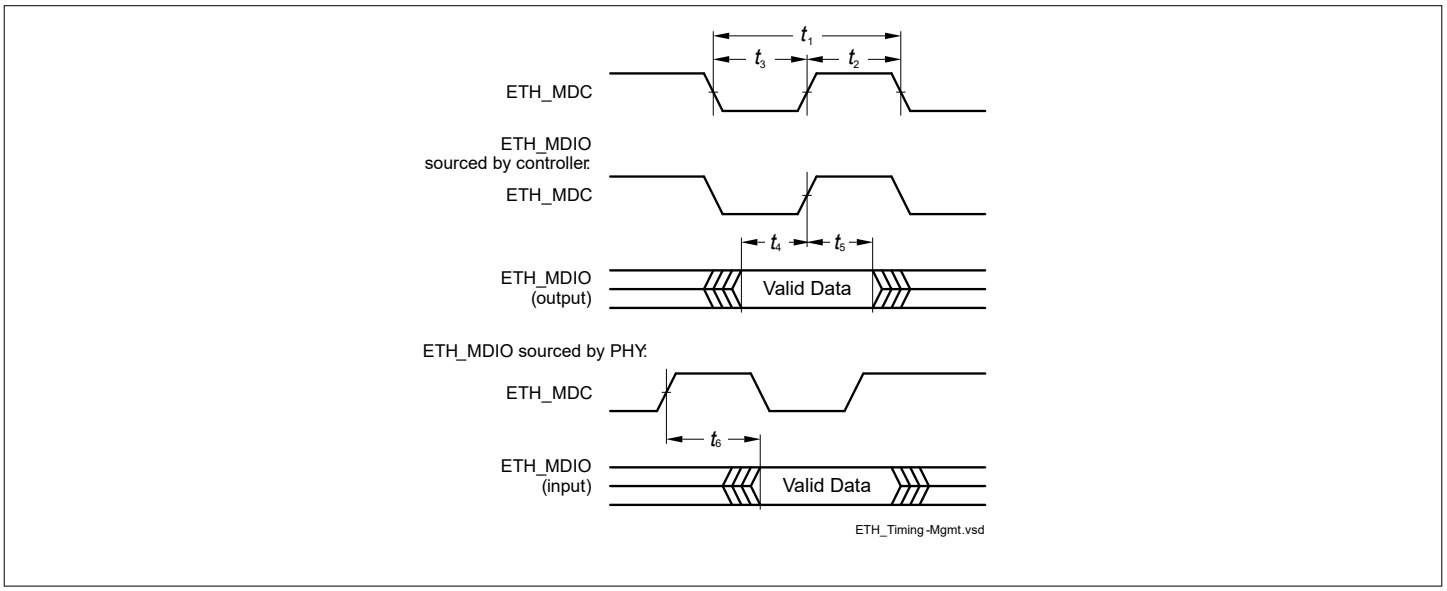


Figure 17 ETH management signal timing

Related information

ETH management signal timing valid for 3.3V on page 530

4.29.3 ETH 10BASE-T1S signal timing characteristics

In the following sub-chapter, the timing characteristics of the ETH 10BASE-T1S (Three Pin Interface) are listed.

4.29.3.1 ETH 10BASE-T1S signal timing

Table 142 ETH 10BASE-T1S signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transmit data '0' low duration	$t_{LowTXD0}$ *CC*	-	20	-	ns	C_L = 25 pF
Transmit data '0' high duration	$t_{HighTXD0}$ *CC*	-	60	-	ns	C_L = 25 pF
Transmit data '1' low or high duration	$t_{LowHighTXD1}$ *CC*	-	20	-	ns	C_L = 25 pF
RXD signal low pulse duration	t_{LowRXD} *SR*	12	-	-	ns	
		12	-	-	ns	
ED signal low pulse duration	t_{LowED} *SR*	21	-	-	ns	

4.29.3.2 ETH 10BASE-T1S signal timing figure

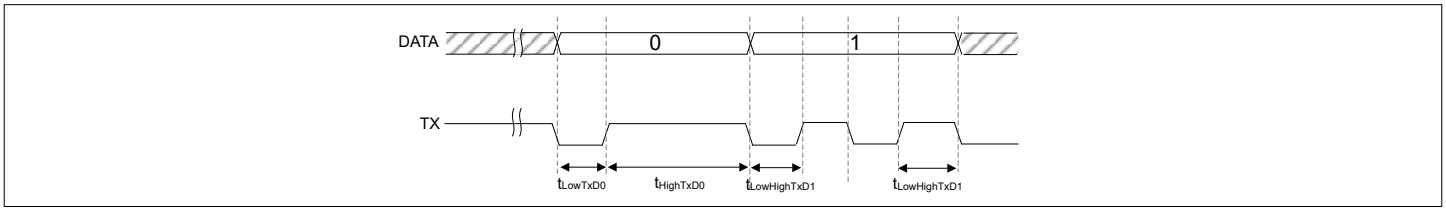


Figure 18 10BASE-T1S Signal Timing

4.29.4 ETH MII timing characteristics

In the following sub-chapter, the timing characteristics of the MII (Media Independent Interface) are listed. The following signal timings are valid for 3.3 V.

4.29.4.1 ETH MII signal timing

Table 143 ETH MII signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock period	t_7 *SR*	-	40	-	ns	C_L = 25 pF; baudrate = 100 Mbps
		-	400	-	ns	C_L = 25 pF; baudrate = 10 Mbps
Clock high time	t_8 *SR*	14	-	26	ns	C_L = 25 pF; baudrate = 100 Mbps
		140[1)]	-	260[2)]	ns	C_L = 25 pF; baudrate = 10 Mbps
Clock low time	t_9 *SR*	14	-	26	ns	C_L = 25 pF; baudrate = 100 Mbps
		140[1)]	-	260[2)]	ns	C_L = 25 pF; baudrate = 10 Mbps
Input setup time	t_{10} *SR*	10	-	-	ns	C_L = 25 pF
Input hold time	t_{11} *SR*	10	-	-	ns	C_L = 25 pF
Output valid time	t_{12} *CC*	0	-	25	ns	C_L = 25 pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

Related information

ETH MII signal timing figures on page 533

4.29.4.2 ETH MII signal timing figures

Ethernet media independent interface (ETH MII) signal timing.

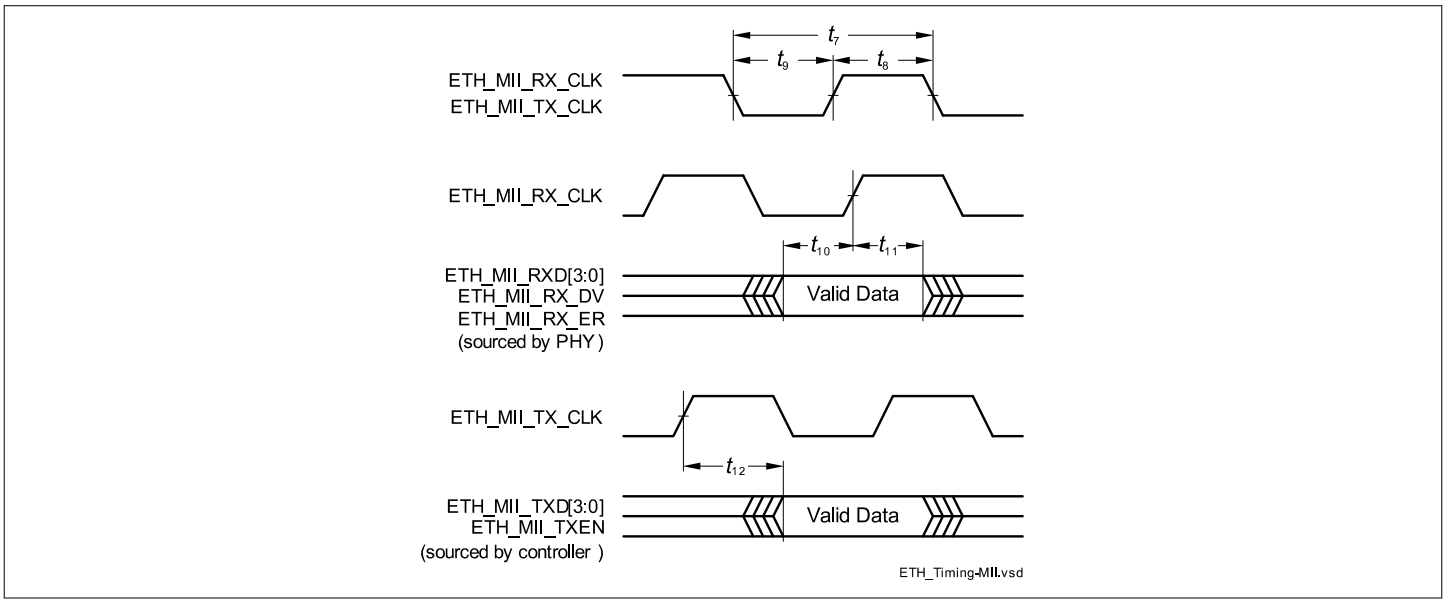


Figure 19 ETH MII signal timing

Related information

ETH MII signal timing on page 532

4.29.5 ETH RMII timing characteristics

The following sub-chapter contains the timing characteristics of the RMII (Reduced Media Independent Interface).

4.29.5.1 ETH RMII signal timing valid for 3.3V

Table 144 ETH RMII signal timing valid for 3.3V

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} *SR*	-	20	-	ns	50 ppm; C_L = 25 pF *1)*
ETH_RMII_REF_CL clock high time	t_{14} *SR*	7 *2)*	-	13 *3)*	ns	C_L = 25 pF *1)*
ETH_RMII_REF_CL clock low time	t_{15} *SR*	7 *2)*	-	13 *3)*	ns	C_L = 25 pF *1)*
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time	t_{16} *CC*	4	-	-	ns	C_L = 25 pF *1)*
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time	t_{17} *CC*	2	-	-	ns	C_L = 25 pF *1)*

(table continues...)

Table 144 (continued) ETH RMII signal timing valid for 3.3V

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18} CC	-	-	15.4	ns	C_L = 25 pF 1)

1) Maximum allowed capacitive load C_L for the RMII function on Port 20 in TC4Dx is 20 pF
2) Defined by 35% of clock period.
3) Defined by 65% of clock period.

Related information

ETH RMII signal timing figures on page 534

4.29.5.2 ETH RMII signal timing figures

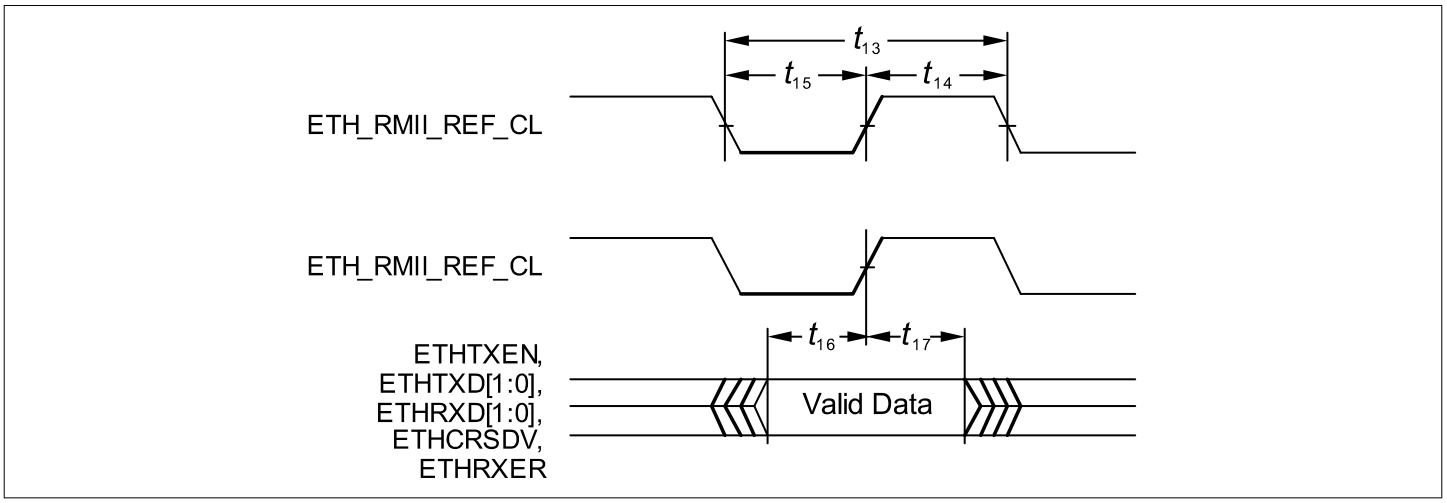


Figure 20 ETH RMII signal timing

Related information

ETH RMII signal timing valid for 3.3V on page 533

4.29.6 ETH RGMII timing characteristics

The following sub-chapter contains the RGMII (Reduced Gigabit Media Independent Interface) timing characteristics.

4.29.6.1 ETH RGMII signal timing valid for 3.3V

Table 145 ETH RGMII signal timing valid for 3.3V

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TX Clock period	t_{19} *CC*	360	400	440	ns	10 Mbps
		36	40	44	ns	100 Mbps
		7.2	8	8.8	ns	1 Gbps
Data to Clock Output skew[1)]	t_{20} *CC*	-500	0	500	ps	
Data to Clock input skew (at receiver)	t_{21} *SR*	1	1.8	2.6[2)]	ns	
Clock duty cycle	t_{duty} *CC*	40	50	60	%	10 / 100 Mbps
		45	50	55	%	1 Gbps
GREFCLK duty cycle	t_{duty_in} *SR*	45	-	55	%	
GREFCLK Input accuracy	*ACC SR*	-0.005	-	0.005	%	

1) Only valid when HSPHY_DLL_CFG.TXCFG = 0 (TX clock delay is 0)
2) For 10/100 Mbps the Max value is unspecified

Related information

ETH RGMII signal timing figures on page 535

4.29.6.2 ETH RGMII signal timing figures

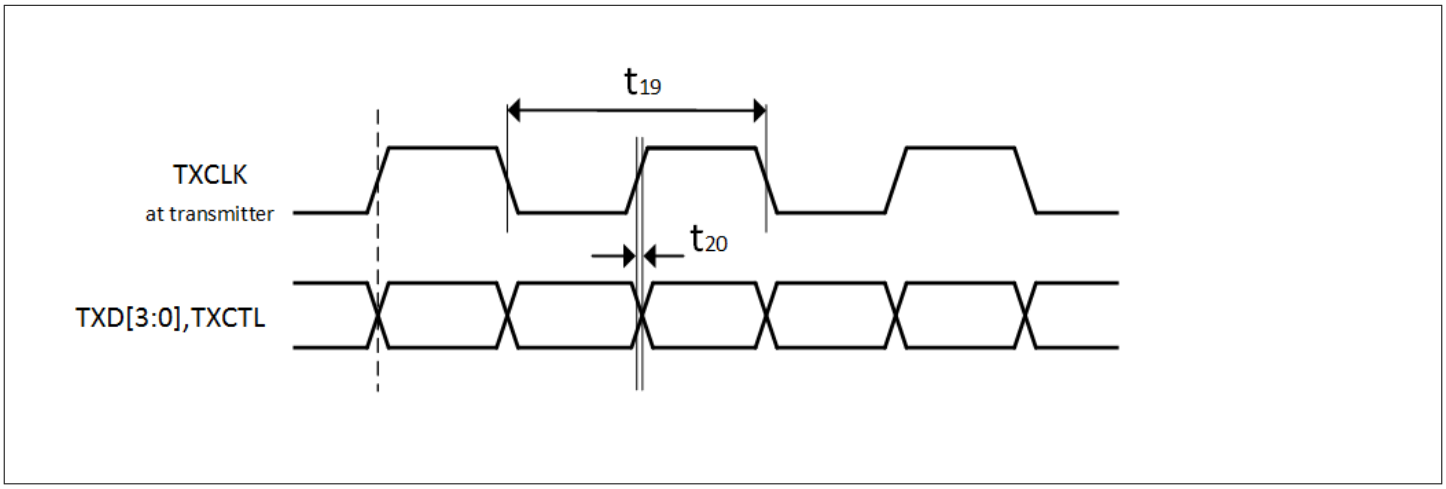


Figure 21 ETH RGMII TX Signal Timing (Delay on Destination (DoD))

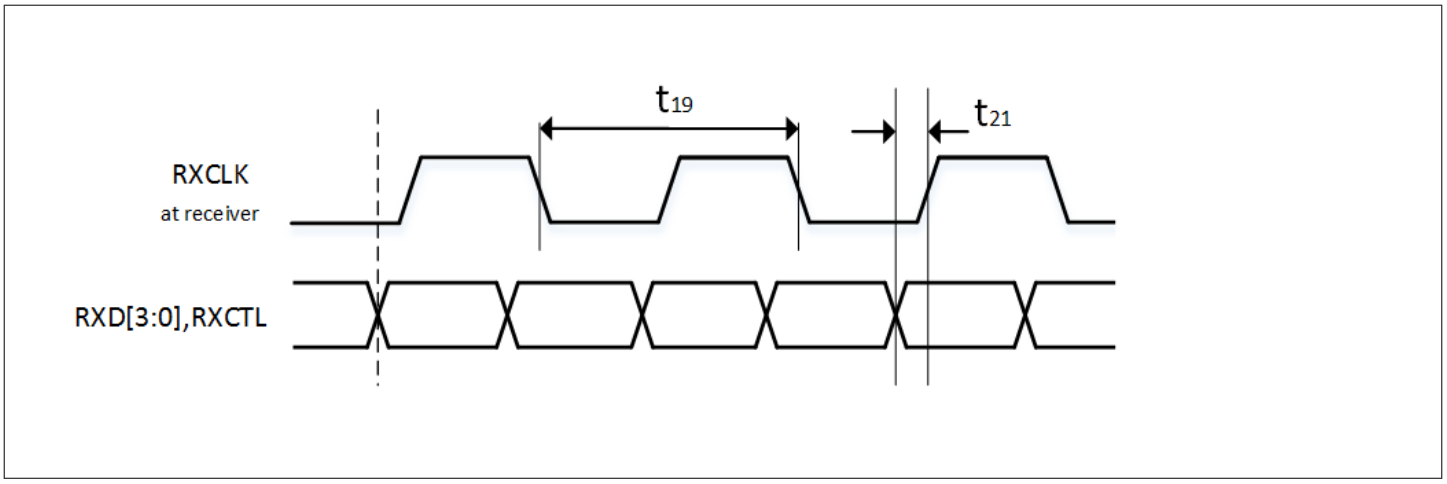


Figure 22 ETH RGMII RX Signal Timing (Delay on Source (DoS))

Related information
ETH RGMII signal timing valid for 3.3V on page 535

4.29.7 ETH SERDES characteristics

The following sub-chapters include the characteristics of the SGMII (Serial Gigabit Media Independent Interface).

***Note**: SGMII protocol operation via HSPHY is only possible with f_{OSC} = 25MHz or 40 MHz*

4.29.7.1 ETH SERDES transmitter characteristics

Table 146 ETH SERDES transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal DC characteristics						
Output DC high value	V_{oh} *CC*	-	-	1000	mV	
Output DC low value	V_{ol} *CC*	-350	-	-	mV	
Output current when shorted between P and N	I_{sab} *CC*	-	-	12	mA	
Differential signal characteristics						
Output Differential Voltage	$\|V_{od}\|$ *CC*	250	-	630	mV	
Change in Vod between "1" and "0"	$\Delta\|V_{od}\|$ *CC*	-	-	25	mV	
Output common mode voltage	V_{os} *CC*	250	-	650	mV	
Change in Vos between "1" and "0"	ΔV_{os} *CC*	-	-	25	mV	
TX Output impedance, differentially	R_o *CC*	80	-	120	Ohm	

(table continues...)

Table 146 (continued) ETH SERDES transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
AC characteristics						
TX AC min amplitude	TX_{A1} *CC*	200	-	-	mV	
TX AC max amplitude	TX_{A2} *CC*	-	-	700	mV	
AC characteristics - USXGMII 5.15625 Gbaud						
Unit Interval	*UI CC*	-	193.939 393	-	ps	Allowed variation from Typ value: ± 100 ppm
Max jitter value	TX_{X1} *CC*	-	-	0.14	UI	valid for a USXGMII line rate of 5.15625 Gbaud (for 64b/66b encoded protocols with a data rate of 5 Gbps)
Data eye measure point	TX_{X2} *CC*	-	-	0.39	UI	valid for a USXGMII line rate of 5.15625 Gbaud (for 64b/66b encoded protocols with a data rate of 5 Gbps)
Total jitter	J_T *CC*	-	-	0.28	UI	valid for an USXGMII line rate of 5.15625 Gbaud (for 64b/66b encoded protocols with a data rate of 5 Gbps)
AC characteristics - SGMII 3.125 Gbaud						
Unit Interval	*UI CC*	-	320	-	ps	Allowed variation from Typ value: ± 100 ppm
Max jitter value	TX_{X1} *CC*	-	-	0.175	UI	valid for a SGMII line rate of 3.125 Gbaud (for 8b/10b encoded protocols with a data rate of 2.5 Gbps)
Data eye measure point	TX_{X2} *CC*	-	-	0.39	UI	valid for a SGMII line rate of 3.125 Gbaud (for 8b/10b encoded protocols with a data rate of 2.5 Gbps)
Total jitter	J_T *CC*	-	-	0.35	UI	valid for an SGMII line rate of 3.125 Gbaud (for 8b/10b encoded protocols with a data rate of 2.5 Gbps)
AC characteristics - SGMII 1.25 Gbaud						
Unit Interval	*UI CC*	-	800	-	ps	Allowed variation from Typ value: ± 300 ppm

(table continues...)

Table 146 (continued) ETH SERDES transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Max jitter value	TX_{X1} *CC*	-	-	0.15	UI	valid for an SGMII line rate of 1.25 Gbaud (for 8b/10b encoded protocols with a data rate of 1 Gbps/100 Mbps)
Data eye measure point	TX_{X2} *CC*	-	-	0.39	UI	valid for an SGMII line rate of 1.25 Gbaud (for 8b/10b encoded protocols with a data rate of 1 Gbps/100 Mbps)
Total jitter	J_T *CC*	-	-	0.30	UI	valid for an SGMII line rate of 1.25 Gbaud (for 8b/10b encoded protocols with a data rate of 1 Gbps/100 Mbps)

Related information

ETH SERDES transmitter eye on page 538
ETH SERDES receiver characteristics on page 539
ETH SERDES receiver eye on page 539

4.29.7.2 ETH SERDES transmitter eye

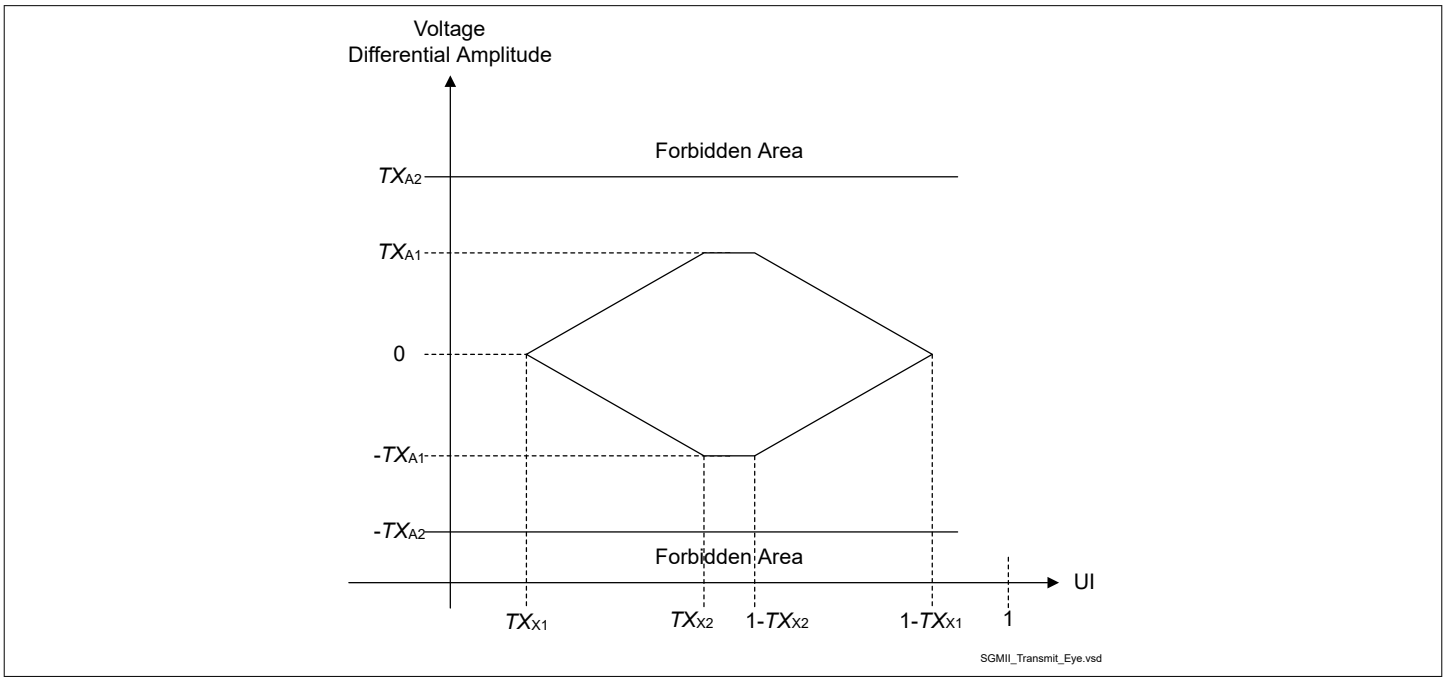


Figure 23 SERDES transmitter eye

Related information

ETH SERDES transmitter characteristics on page 536
ETH SERDES receiver characteristics on page 539

ETH SERDES receiver eye on page 539

4.29.7.3 ETH SERDES receiver characteristics

Table 147 ETH SERDES receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal DC characteristics						
Receiver input voltage range	V_i *CC*	0	-	1000	mV	
Differential signal characteristics						
Input differential impedance	R_{in} *CC*	80	-	120	Ohm	
AC characteristics						
RX AC min amplitude	RX_{A1} *CC*	100	-	-	mV	
RX AC max amplitude	RX_{A2} *CC*	-	-	700	mV	
Max jitter value	RX_{X1} *CC*	-	-	0.275	UI	Valid for all specified transmit line rates

Related information

ETH SERDES transmitter characteristics on page 536
ETH SERDES transmitter eye on page 538
ETH SERDES receiver eye on page 539

4.29.7.4 ETH SERDES receiver eye

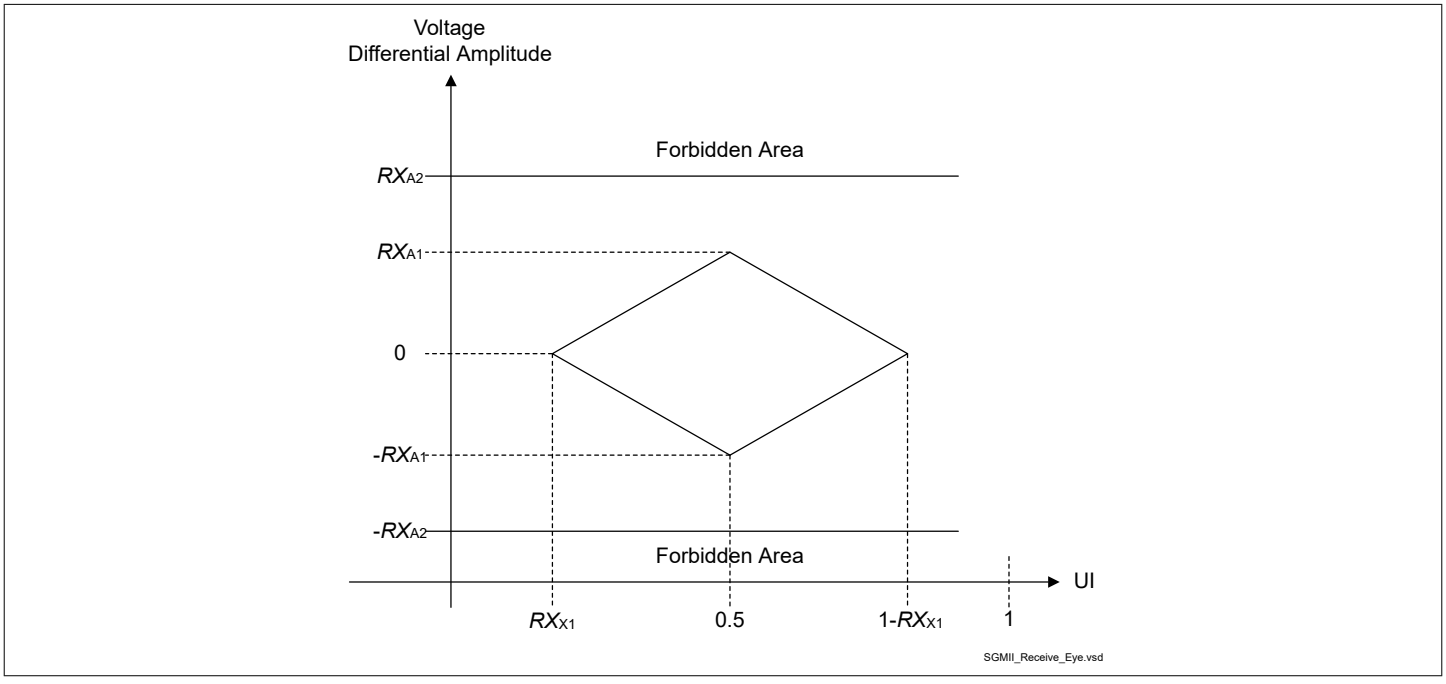


Figure 24 SERDES receiver eye

Related information

ETH SERDES transmitter characteristics on page 536
ETH SERDES transmitter eye on page 538
ETH SERDES receiver characteristics on page 539

4.30 PCIe characteristics

The PCIe module of the TC4DxAA-step COM supports following speed grades:

- up to 2.5 Gbps data rate - GEN1
- up to 5 Gbps data rate - GEN2
- up to 8 Gbps data rate - GEN3

The module characteristics relevant for all supported speed grades are listed in the following sub-chapters.

4.30.1 PCIe REFCLK characteristics

Related information

PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.1.1 PCIe REFCLK characteristics

Table 148 PCIe REFCLK characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input reference clock frequency range	$R_{efclkFREQ}$ *SR*	99.97	-	100.03	MHz	
Duty cycle	*Duty Cycle SR*	40	-	60	%	GEN1, GEN2, GEN3
Single ended rising Refclk edge rate versus falling Refclk edge rate	*Rise/Fall Matching SR*	-	20	-	%	GEN1, GEN2, GEN3
Rising edge rate	$T_{C\text{-}RISE}$ *SR*	0.6	-	4	V/ns	Differential; GEN1, GEN2, GEN3
Falling edge rate	$T_{C\text{-}FALL}$ *SR*	0.6	-	4	V/ns	Differential; GEN1, GEN2, GEN3
Cycle to cycle jitter	$T_{CC\text{-}JITTER}$ *SR*	-	-	150	ps	GEN1, GEN2, GEN3
Average clock period accuracy	$T_{PERIOD\text{-}AVG}$ *SR*	-300 ppm	-	2800 ppm		GEN1, GEN2, GEN3

(table continues...)

Table 148 (continued) PCIe REFCLK characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Absolute period, including spread-spectrum and jitter	$T_{PERIOD-ABS}$ *SR*	9.847	-	10.203	ns	GEN1, GEN2, GEN3
Time before VRB is allowed	T_{STABLE} *SR*	500	-	-	ps	Differential; GEN1, GEN2, GEN3
Differential input high voltage	V_{IH} *SR*	150	-	-	mV	Differential; GEN1, GEN2, GEN3
Differential input low voltage	V_{IL} *SR*	-	-	-150	mV	Differential; GEN1, GEN2, GEN3
Absolute maximum input voltage	V_{MAX} *SR*	-	-	1.15	V	GEN1, GEN2, GEN3
Absolute minimum input voltage	V_{MIN} *SR*	-0.3	-	-	V	GEN1, GEN2, GEN3
Absolute single-ended crossing point voltage	V_{CROSS} *SR*	250	-	550	mV	Single-ended; GEN1, GEN2, GEN3
Variation of VCROSS over all rising clock edges	$V_{CROSS-DELTA}$ *SR*	-	-	140	mV	Single-ended; GEN1, GEN2, GEN3
Ring back voltage margin	V_{RB} *SR*	-100	-	100	mV	Differential; GEN1, GEN2, GEN3
Clock source output DC impedance	Z_{C-DC} *SR*	40	-	60	Ohm	GEN1, GEN2, GEN3

Related information

PCIe REFCLK figures on page 542

4.30.1.2 PCIe REFCLK figures

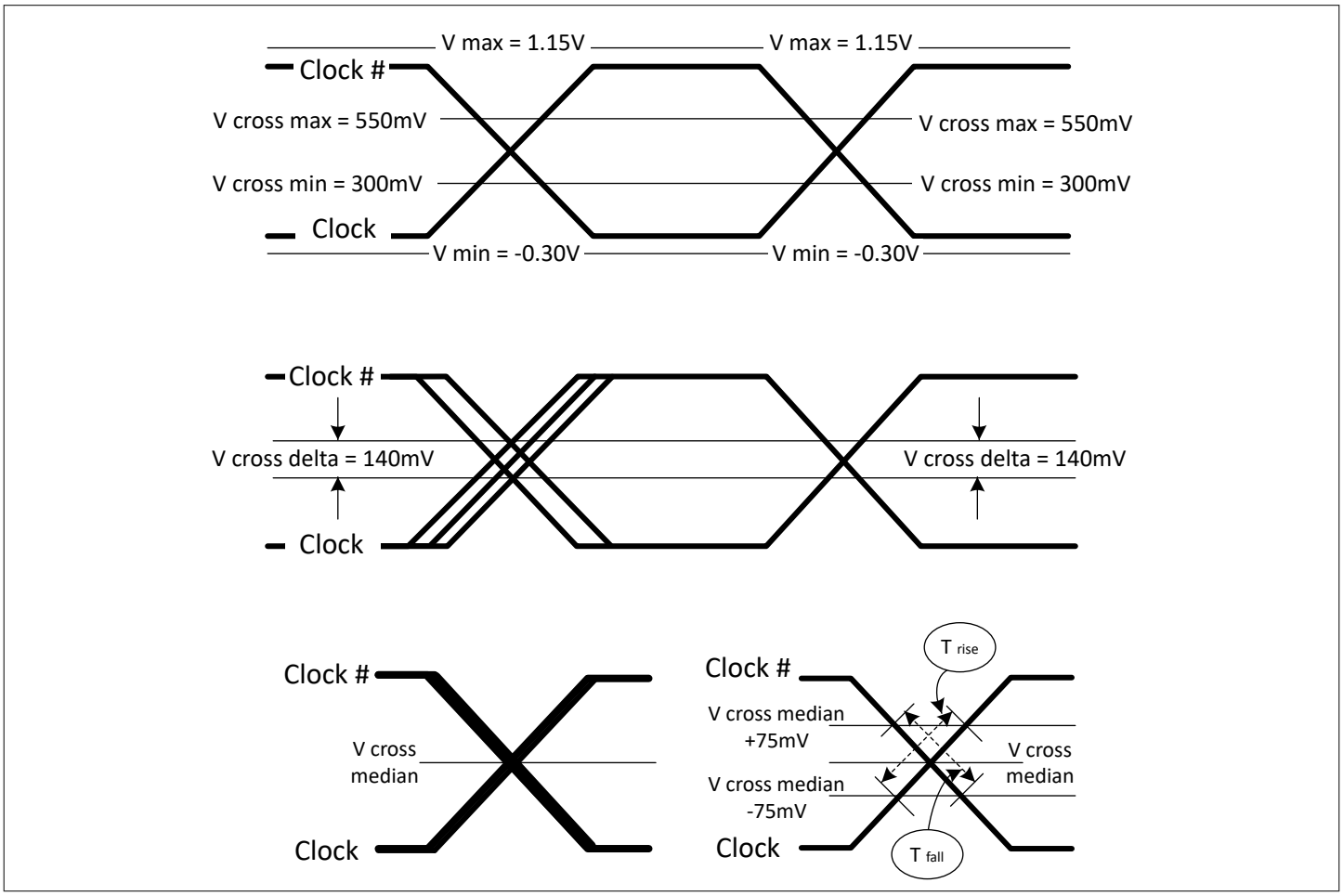


Figure 25 Differential Clock Single Ended Measurement for PCIe REFCLK

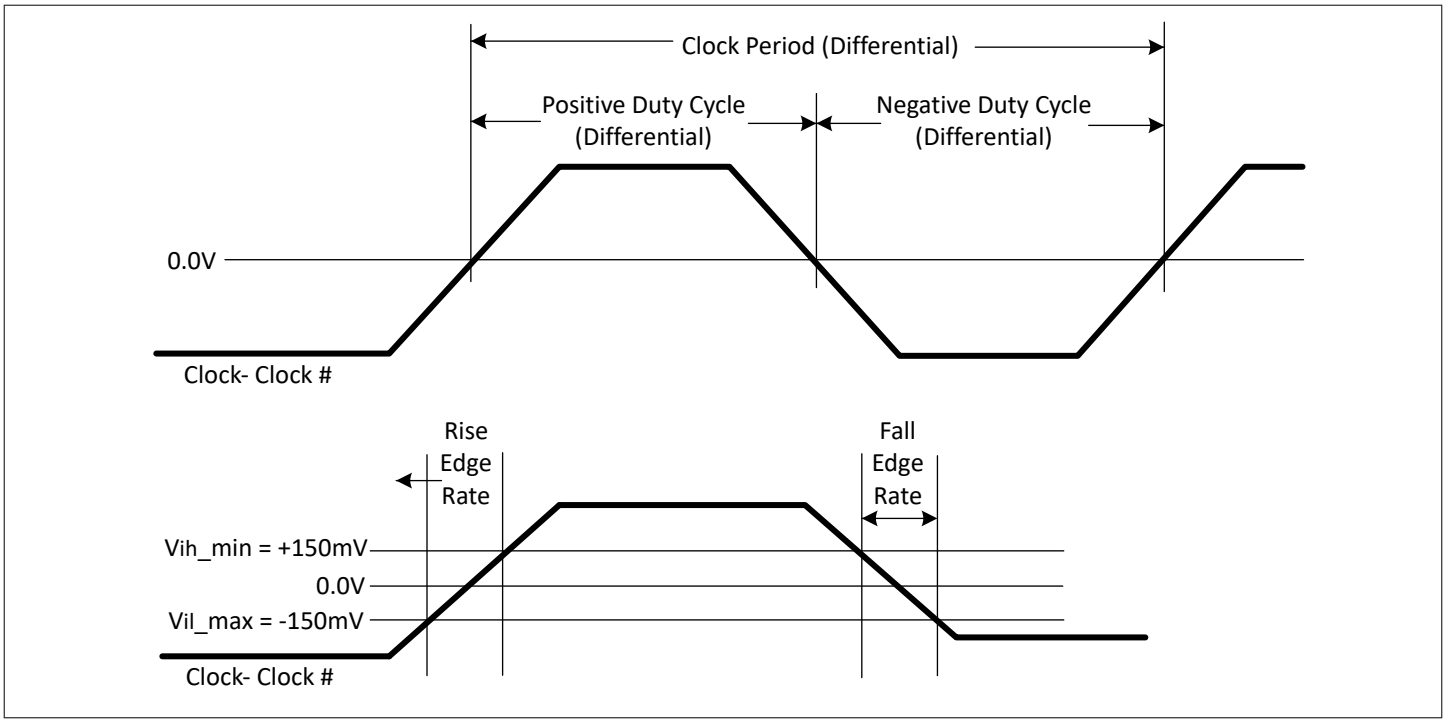


Figure 26 Differential Clock Differential Measurement for PCIe REFCLK

Related information

PCIe REFCLK characteristics on page 540

4.30.2 PCIe - GEN1 transmitter characteristics

Table 149 PCIe - GEN1 transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal dc characteristics						
DC Common mode voltage	$V_{TX\text{-}DC\text{-}CM}$ *CC*	0	-	1200	mV	
Differential signal characteristics						
Differential output voltage (peak-to-peak)	$V_{TX\text{-}DIFF\text{-}PP}$ *CC*	800	-	1200	mV	
Low power differential output voltage (peak-to-peak)	$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$ *CC*	400	-	1200	mV	
DC Differential TX impedance	$Z_{TX\text{-}DIFF\text{-}DC}$ *CC*	80	-	120	Ohm	
AC characteristics						
Unit Interval	*UI CC*	399.88	400	400.12	ps	
Minimum TX Eye Width	$T_{TX\text{-}EYE}$ *CC*	0.75	-	-	UI	

(table continues...)

Table 149 (continued) PCIe - GEN1 transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum time between the jitter median and maximum deviation from the median	$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ *CC*	-	-	0.125	UI	
Transmitter AC common mode peak voltage	$V_{TX\text{-}CM\text{-}AC\text{-}P}$ *CC*	-	-	20	mV	
AC coupling capacitor	C_{TX} *SR*	75	-	265	nF	

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.3 PCIe - GEN1 transmitter eye figure

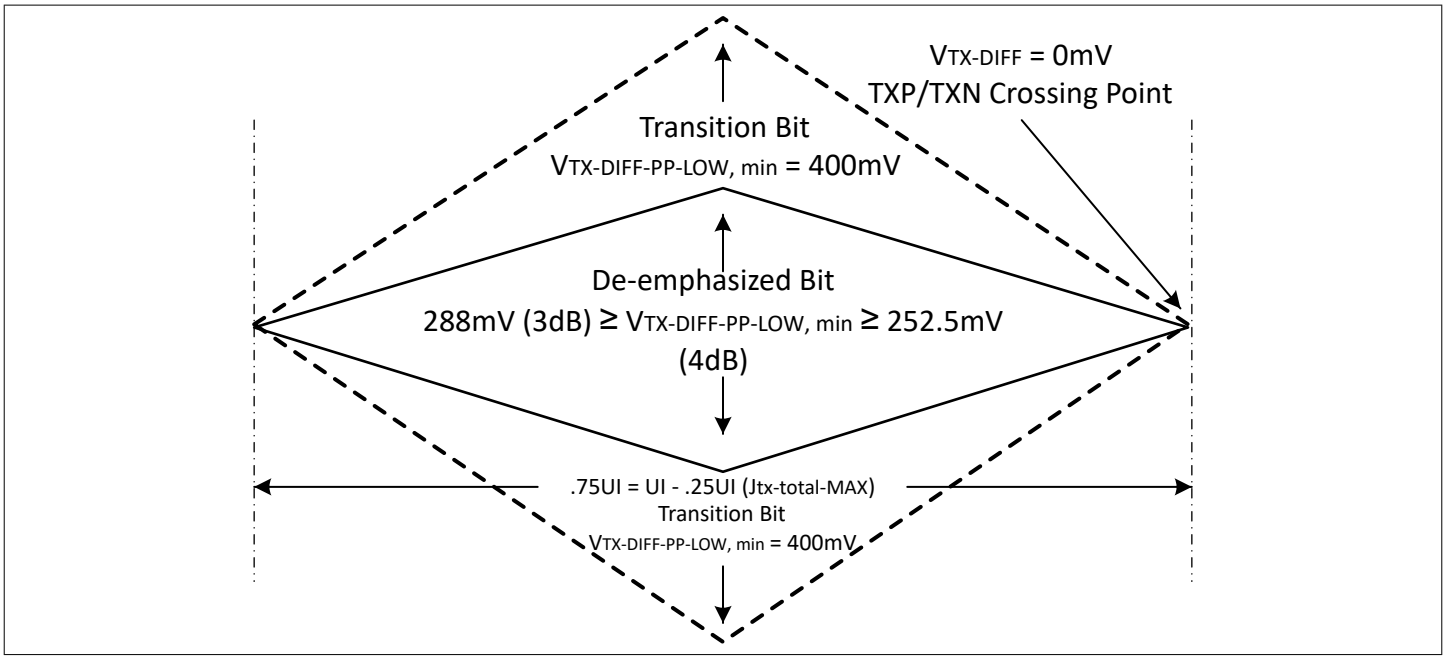


Figure 27 PCI Express Transmitter Eye - Illustrated on Example of GEN1

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN2 transmitter characteristics on page 545

PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.4 PCIe - GEN2 transmitter characteristics

Table 150 PCIe - GEN2 transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal dc characteristics						
DC Common mode voltage	$V_{TX\text{-}DC\text{-}CM}$ *CC*	0	-	1200	mV	
The amount of voltage change allowed during Receiver Detection	$V_{TX\text{-}RCV\text{-}DETECT}$ *CC*	-	-	600	mV	
Differential signal characteristics						
Differential output voltage (peak-to-peak)	$V_{TX\text{-}DIFF\text{-}PP}$ *CC*	800	-	1200	mV	
Low power differential output voltage (peak-to-peak)	$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$ *CC*	400	-	1200	mV	
DC Differential TX impedance	$Z_{TX\text{-}DIFF\text{-}DC}$ *CC*	-	-	120	Ohm	
AC characteristics						
Unit Interval	*UI CC*	199.94	200	200.06	ps	
Minimum TX Eye Width	$T_{TX\text{-}EYE}$ *CC*	0.75	-	-	UI	
10 KHz to 1.5 MHz RMS jitter	$T_{rx\text{-}lf\text{-}rms}$ *CC*	-	-	3	ps	RMS value
Tx deterministic jitter > 1.5 MHz	$T_{tx\text{-}hf\text{-}dj\text{-}dd}$ *CC*	-	-	0.15	UI	
Transmitter AC common mode peak-to-peak voltage	$V_{TX\text{-}CM\text{-}AC\text{-}PP}$ *CC*	-	-	100	mVPP	0.03 - 500 MHz
AC coupling capacitor	C_{TX} *SR*	75	-	265	nF	

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.5 PCIe - GEN3 transmitter characteristics

Table 151 PCIe - GEN3 transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal dc characteristics						
DC Common mode voltage	$V_{TX\text{-}DC\text{-}CM}$ *CC*	0	-	1200	mV	
Differential signal characteristics						
Full swing Tx voltage with no TxEq	$V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ *CC*	800	-	1300	mV	
Reduced swing Tx voltage with no TxEq	$V_{TX\text{-}RS\text{-}NO\text{-}EQ}$ *CC*	-	-	650	mV	
Min swing during EIEOS for full swing	$V_{TX\text{-}EIEOS\text{-}FS}$ *CC*	250	-	-	mVPP	
Min swing during EIEOS for reduced swing	$V_{TX\text{-}EIEOS\text{-}RS}$ *CC*	232	-	-	mVPP	
Tx boost ratio for full swing	$V_{TX\text{-}BOOST\text{-}FS}$ *CC*	8.0	-	-	dB	
Tx boost ratio for reduced swing	$V_{TX\text{-}BOOST\text{-}RS}$ *CC*	2.5	-	-	dB	
DC Differential TX impedance	$Z_{TX\text{-}DIFF\text{-}DC}$ *CC*	-	-	120	Ohm	
AC characteristics						
Unit Interval	*UI CC*	124.9625	125	125.0375	ps	
Tx uncorrelated total jitter	$T_{TX\text{-}UTJ}$ *CC*	-	-	31.25	ps PP	
Deterministic DjDD uncorrelated Pulse Width Jitter (PWJ)	$T_{TX\text{-}UPW\text{-}DJDD}$ *CC*	-	-	10	ps PP	
Tx uncorrelated deterministic jitter	$T_{TX\text{-}UDJDD}$ *CC*	-	-	12	ps PP	
Total uncorrelated Pulse Width Jitter (PWJ)	$T_{TX\text{-}UPW\text{-}TJ}$ *CC*	-	-	24	ps PP	
Data dependent jitter	$T_{TX\text{-}DDJ}$ *CC*	-	-	18	ps PP	
Transmitter AC common mode peak-to-peak voltage	$V_{TX\text{-}CM\text{-}AC\text{-}PP}$ *CC*	-	-	50	mVPP	0.03 - 500 MHz
AC coupling capacitor	C_{TX} *SR*	176	-	265	nF	

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544

PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.6 PCIe - GEN1 receiver characteristics

Table 152 PCIe - GEN1 receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal dc characteristics						
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$ *CC*	65	-	175	mV	
Receiver single ended impedance (DC)	$Z_{RX\text{-}DC}$ *CC*	40	-	60	Ohm	
Differential signal characteristics						
Differential input voltage (peak-to-peak)	$V_{RX\text{-}DIFF\text{-}PP}$ *CC*	175	-	1200	mV	
Differential input impedance (DC)	$Z_{RX\text{-}DIFF\text{-}DC}$ *CC*	80	-	120	Ohm	
AC characteristics						
Unit Interval	*UI CC*	399.88	400	400.12	ps	
Minimum Receiver Eye Width (jitter tolerance)	$T_{RX\text{-}EYE}$ *CC*	0.4	-	-	UI	
Receiver AC common mode peak voltage	$V_{RX\text{-}CM\text{-}AC\text{-}P}$ *CC*	-	-	150	mV	
Timing characteristics						
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERTIME}$ *CC*	-	-	10	ms	

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.7 PCIe - GEN1 receiver eye figure

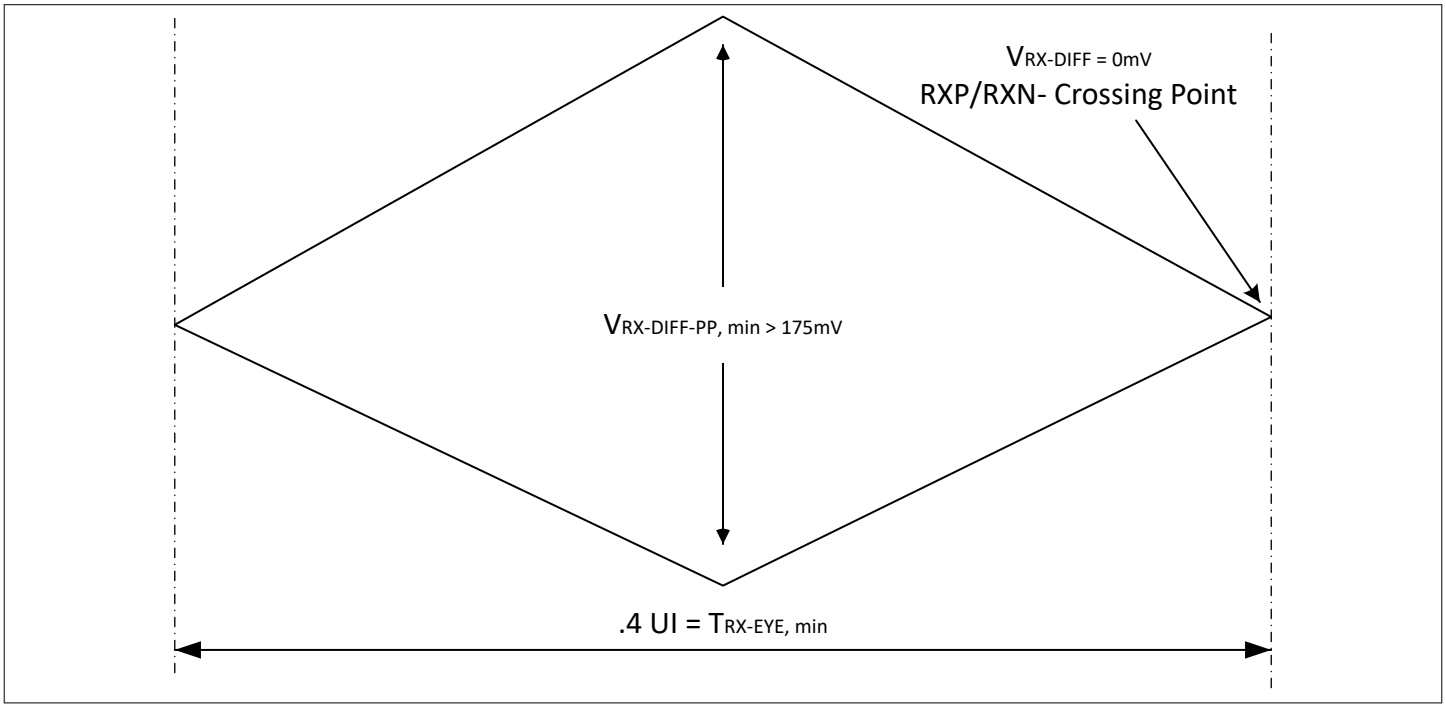


Figure 28 PCI Express Receiver Eye - Illustrated on Example of GEN1

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN2 receiver characteristics on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.8 PCIe - GEN2 receiver characteristics

Table 153 PCIe - GEN2 receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal dc characteristics						
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$ *CC*	65	-	175	mV	
Receiver single ended impedance (DC)	$Z_{RX\text{-}DC}$ *CC*	40	-	60	Ohm	

(table continues...)

Table 153 (continued) PCIe - GEN2 receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Differential signal characteristics						
Differential input voltage (peak-to-peak)	$V_{RX\text{-}DIFF\text{-}PP}$ *CC*	100	-	1200	mV	
AC characteristics						
Unit Interval	*UI CC*	199.94	200	200.06	ps	
Minimum Receiver instantaneous Eye Width	$T_{RX\text{-}MIN\text{-}PULSE}$ *CC*	0.6	-	-	UI	
Max Rx inherent timing error	$T_{RX\text{-}TJ\text{-}DC}$ *CC*	-	-	0.34	UI	
Receiver AC common mode peak voltage	$V_{RX\text{-}CM\text{-}AC\text{-}P}$ *CC*	-	-	150	mV	
Timing characteristics						
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERTIME}$ *CC*	-	-	10	ms	

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN3 receiver characteristics on page 549

4.30.9 PCIe - GEN3 receiver characteristics

Table 154 PCIe - GEN3 receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal dc characteristics						
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$ *CC*	65	-	175	mV	
AC characteristics						
Unit Interval	*UI CC*	124.9625	125	125.0375	ps	
Receiver AC common mode peak voltage	$V_{RX\text{-}CM\text{-}AC\text{-}P}$ *CC*	-	-	125	mV	EH ≥ 100 mVPP

(table continues...)

Table 154 (continued) PCIe - GEN3 receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Timing characteristics						
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$ *CC*	-	-	10	ms	

Related information

PCIe REFCLK characteristics on page 540
PCIe - GEN1 transmitter characteristics on page 543
PCIe - GEN1 transmitter eye figure on page 544
PCIe - GEN2 transmitter characteristics on page 545
PCIe - GEN3 transmitter characteristics on page 546
PCIe - GEN1 receiver characteristics on page 547
PCIe - GEN1 receiver eye figure on page 548
PCIe - GEN2 receiver characteristics on page 548

4.31 FSP timing characteristics

Table 155 FSP timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Skew between FSP0 and FSP1, respectively between FSP2 and FSP3	$t_{FSPSKEW}$ *CC*	-6	-	6	ns	C_L = 50 pF, driver = strong, edge = sharp
		-8	-	8	ns	C_L = 50 pF, driver = strong, edge = medium
		-12	-	12	ns	C_L = 50 pF, driver = medium

4.32 Flash characteristics

Table 156 Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector	t_{SECTOR_ERP} *CC*	-	-	0.2[1)]	s	cycle count: ≤ 1000
Program Flash Erase Time per logical sector range	t_{RANGE_ERP} *CC*	-	-	0.4[1)]	s	cycle count: ≤ 1000; range: ≤ 32 consecutive logical sectors (≤ 512 KB)

(table continues...)

Table 156 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Program Flash Program Time with 4x64 bit Program Operation per Page (32 Byte)	$t_{PRG\_P64\_P}$ *CC*	-	-	90[1)]	µs	32 Byte
Program Flash Program Time with 256 bit Program Operation per Page (32 Byte)	$t_{PRG\_P256\_P}$ *CC*	-	-	70[1)]	µs	32 Byte
Program Flash Program Time with 4x64 bit Program Operation in Burst Mode (512 Byte)	$t_{PRG\_P64\_B}$ *CC*	-	-	530[1)]	µs	512 Byte
Program Flash Program Time with 256 bit Program Operation in Burst Mode (512 Byte)	$t_{PRG\_P256\_B}$ *CC*	-	-	220[1)]	µs	512 Byte
Program Flash Program Time with 256 bit Program Operation in Burst Mode for 2 MB	$t_{PRG\_P256\_B\_2MB}$ *CC*	-	-	1[1)]	s	Derived value for documentation purpose
Write Page Once adder	t_{ADD} *CC*	-	-	15[1)]	µs	Adder to Program Time when using Write Page Once
Program Flash abort to read latency	t_{ABORTP} *CC*	-	-	120[1)]	µs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Program time per Page (8 Byte)	$t_{PRG\_D\_P}$ *CC*	-	-	150[1)]	µs	8 Byte
Data Flash Program time in Burst Mode (32 Byte)	$t_{PRG\_D\_B}$ *CC*	-	-	200[1)]	µs	32 Byte
Data Flash abort to read latency	t_{ABORTD} *CC*	-	-	120[1)]	µs	
Wait time after margin change	$t_{FL\_MarginDel}$ *CC*	-	-	5	µs	
Program Flash Endurance per Logical Sector[2)]	N_{E_P} *CC*	-	-	1000	cycles	
Number of Erase Operations per Program Flash Bank	N_{ERP} *CC*	-	-	32000	cycles	
Program Flash Retention Time, Sector	t_{RET} *CC*	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU} *CC*	20	-	-	years	Max. 200 erase/program cycles per UCB

(table continues...)

Table 156 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Data Flash access delay	t_{DF} *CC*	-	-	50	ns	
Program Flash access delay	t_{PF} *CC*	-	-	15	ns	
Number of erase operations on DF0 over lifetime	N_{ERD0S} *CC*	-	-	2000000 [3]	cycles	
Number of erase operations on DF1 over lifetime	N_{ERD1S} *CC*	-	-	2000000 [3]	cycles	
Data Flash Endurance per CSRMx sector [4]	N_{E_CSRM} *CC*	-	-	250000 [5]	cycles	Retention time and T_J as mentioned in "Temperature operating conditions" chapter
DataFlash Endurance per EEPROMx sector [6]	N_{E_EEPROM} *CC*	-	-	250000 [5]	cycles	Retention time and T_J in "Temperature operating conditions" chapter
Program Flash Maximum Number of Overwrite Operations on the same Page	$N_{P\_PAGE\_OVERWR}$ *CC*	-	-	2	cycles	After the initial prog each page of a wordline may be overwritten 2 additional times before next erase; in addition parameter N_P_LOGSEC_BL_PROG must be met
Data Flash Maximum Number of Overwrite Operations on the same Page	$N_{D\_PAGE\_OVERWR}$ *CC*	-	-	2	cycles	After the initial prog each page of a wordline may be overwritten 2 additional times before next erase; in addition parameter N_D_LOGSEC_BL_PROG must be met
Program Flash Logical Sector: Number of Program Operations on the same Bitline Address	$N_{P\_LOGSEC\_BL\_PROG}$ *CC*	0	16	24	cycles	valid within a Logical Sector: 16 = # Wordlines per Log Sec; 24 considers 8 additional overwrites on the same bitline address
Data Flash Logical Sector: Number of Program Operations on the same Bitline Address	$N_{D\_LOGSEC\_BL\_PROG}$ *CC*	0	4	8	cycles	valid within a Logical Sector: 4 = # Wordlines per Log Sec; 8 considers 4 additional overwrites on the same bitline address
User Content Count execution time per word-line	t_{CVWL} *CC*	-	-	150 [1]	µs	

(table continues...)

Table 156 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Data Flash Erase Time per logical sector	t_{SECTOR_ERDM} *CC*	-	-	0.15[1) 7)]	s	cycle count: ≤ max allowed cycles defined by parameters NE_EEPROM and NE_CSRM
Data Flash Erase Time per logical sector range	t_{RANGE_ERDM} *CC*	-	-	0.5[1) 7)]	s	cycle count: ≤ max allowed cycles defined by parameters NE_EEPROM and NE_CSRM; range: ≤ 128 consecutive logical sectors (≤ 256 KB)
DataFlash Erase Time per logical sector of quasi static data and per UCB	$t_{SECTOR\_ERDM\_LC\_UCB}$ *CC*	-	-	200[1)]	ms	cycle count: ≤ 1.000 (EEPROM quasi static data or UCB)
DataFlash Erase Time per logical sector range of quasi static data	$t_{RANGE\_ERDM\_LC}$ *CC*	-	-	500[1)]	ms	cycle count: ≤ 1.000 (EEPROM quasi static data or UCB)
Data Flash Erase Verify time per page	$t_{VER\_PAGE\_DS}$ *CC*	-	-	15[1)]	µs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page	$t_{VER\_PAGE\_P}$ *CC*	-	-	15[1)]	µs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector	$t_{VER\_SEC\_DS}$ *CC*	-	-	180[1)]	µs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector	$t_{VER\_SEC\_P}$ *CC*	-	-	360[1)]	µs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline	$t_{VER\_WL\_DS}$ *CC*	-	-	50[1)]	µs	
Program Flash Erase Verify time per wordline	$t_{VER\_WL\_P}$ *CC*	-	-	30[1)]	µs	
Bank Sleep command execution time[8)]	t_{BANK_SLEEP} *CC*	-	-	40	µs	
Bank Wake-Up command execution time[9)]	t_{BANK_WAKEUP} *CC*	-	-	100	µs	
Bank Wake-Up command execution time (When NVM is in Deep Sleep)[9)]	t_{NVM_WAKEUP} *CC*	-	-	130	µs	
Program Flash Replace Logical Sector command execution time[10)]	t_{RLS_PF} *CC*	-	-	120	µs	

(table continues...)

Table 156 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Data Flash Replace Logical Sector command execution time[10]	t_{RLS_DF} *CC*	-	-	120	µs	

1) Only valid for $f_{FSI} \geq 100$ MHz
2) Replace Logical Sector command must be used if a sector fails during an erase or a program operation. FAR will be accepted only when the Replace Logical Sector command also fails, or when the result of the Count Free Redundant Sectors command is 0 for the fail-affected PFlash bank (HOST and CSRM). For more details see "Error handling" chapter in the User Manual.
3) Allows segmentation of addressable memory into 8 logical sectors.
4) If a sector fails during an erase or a program operation, it is suggested to use the Replace Logical Sector command. If the Replace Logical Sector command is used, FAR will be accepted only when the command also fails, or when the result of the Count Free Redundant Sectors command is 0 for the CSRM DFlash bank. For more details see "Error handling" chapter in the User Manual. If the Replace Logical Sector command is not used to repair the failing sector, then it is the user´s responsibility to implement a wordline skipping algorithm that is able to prevent the use of the failing wordlines, otherwise FAR will not be accepted.
5) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.
6) If a sector fails during an erase or a program operation, it is suggested to use the Replace Logical Sector command. If the Replace Logical Sector command is used, FAR will be accepted only when the command also fails, or when the result of the Count Free Redundant Sectors command is 0 for the HOST DFlash bank. For more details see "Error handling" chapter in the User Manual. If the Replace Logical Sector command is not used to repair the failing sector, then it is the user´s responsibility to implement a wordline skipping algorithm that is able to prevent the use of the failing wordlines, otherwise FAR will not be accepted.
7) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
8) Value is measured from the moment when DMU acknowledges the command request to the moment when the status flags of all selected banks are set in the sleep register (HOST and CSRM)
9) Value is measured from the moment when DMU acknowledges the command request to the moment when the status flags of all selected banks are cleared in the sleep register (HOST and CSRM)
10) Value is measured from the moment when DMU acknowledges the command request to the moment when command execution is completed.

4.33 xSPI timing characteristics

4.33.1 xSPI Clock to Data output timings

Table 157 xSPI Clock to Data output timings

xSPI Load Definition

The specified load of CL = 15 pF in the table below corresponds to the use case with one connected slave. For further details see xSPI application note.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
xSPI200						
Cycle time data transfer mode	t_{period} *CC*	10	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF [1]

(table continues...)

Table 157 (continued) xSPI Clock to Data output timings

xSPI Load Definition

The specified load of CL = 15 pF in the table below corresponds to the use case with one connected slave. For further details see xSPI application note.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Duty cycle distortion [2]	t_{CKDCD} CC	-	-	0.5	ns	Timing valid for xSPI200 interface; C_L = 15 pF [1]
Minimum pulse width[2]	t_{CKMPW} CC	4.5	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF [1]
Output Setup Time[3] [4]	t_{oSUddr} CC	1.1	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF [1]
Output hold time[3] [4]	t_{oHddr} CC	1.1	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF [1]
xSPI266						
Cycle time data transfer mode	t_{period} CC	7.5	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF [1]
Duty cycle distortion [2]	t_{CKDCD} CC	-	-	0.375	ns	Timing valid for xSPI266 interface; C_L = 15 pF [1]
Minimum pulse width[2]	t_{CKMPW} CC	3.375	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF [1]
Output Setup Time[3] [4]	t_{oSUddr} CC	0.9	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF [1]
Output hold time[3] [4]	t_{oHddr} CC	0.9	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF [1]
xSPI333						
Cycle time data transfer mode	t_{period} CC	6	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF [1]
Duty cycle distortion [2]	t_{CKDCD} CC	-	-	0.3	ns	Timing valid for xSPI333 interface; C_L = 15 pF [1]

(table continues...)

Table 157 (continued) xSPI Clock to Data output timings

xSPI Load Definition

The specified load of CL = 15 pF in the table below corresponds to the use case with one connected slave. For further details see xSPI application note.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum pulse width[2]	t_{CKMPW} CC	2.7	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF [1]
Output Setup Time[3] [4]	t_{oSUddr} CC	0.7	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF [1]
Output hold time[3] [4]	t_{oHddr} CC	0.7	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF [1]
xSPI400						
Cycle time data transfer mode	t_{period} CC	5	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF [1]
Duty cycle distortion [2]	t_{CKDCD} CC	-	-	0.25	ns	Timing valid for xSPI400 interface; C_L = 15 pF [1]
Minimum pulse width[2]	t_{CKMPW} CC	2.25	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF [1]
Output Setup Time[3] [4]	t_{oSUddr} CC	0.6	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF [1]
Output hold time[3] [4]	t_{oHddr} CC	0.6	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF [1]

1) The specified load corresponds to the use case with one connected slave. For further details see xSPI application note.
2) Timing is measured at 50% of the output level
3) Timing is measured between 30% and 70% of the output level
4) The corresponding timing parameter is valid for the DLL setting DLL_CFG.TXCFG = 9 which corresponds to a phase shift of 90 ° between clock and data

Related information

xSPI Clock to Data timing figure on page 557
xSPI Clock to CS output timings on page 558
xSPI Clock to CS timing figure on page 559
xSPI Data Strobe input timings on page 560
xSPI data strobe to data input timing figure on page 561

xSPI SDR timing without data strobe on page 562
xSPI SDR without data strobe timing figure on page 564

4.33.2 xSPI Clock to Data timing figure

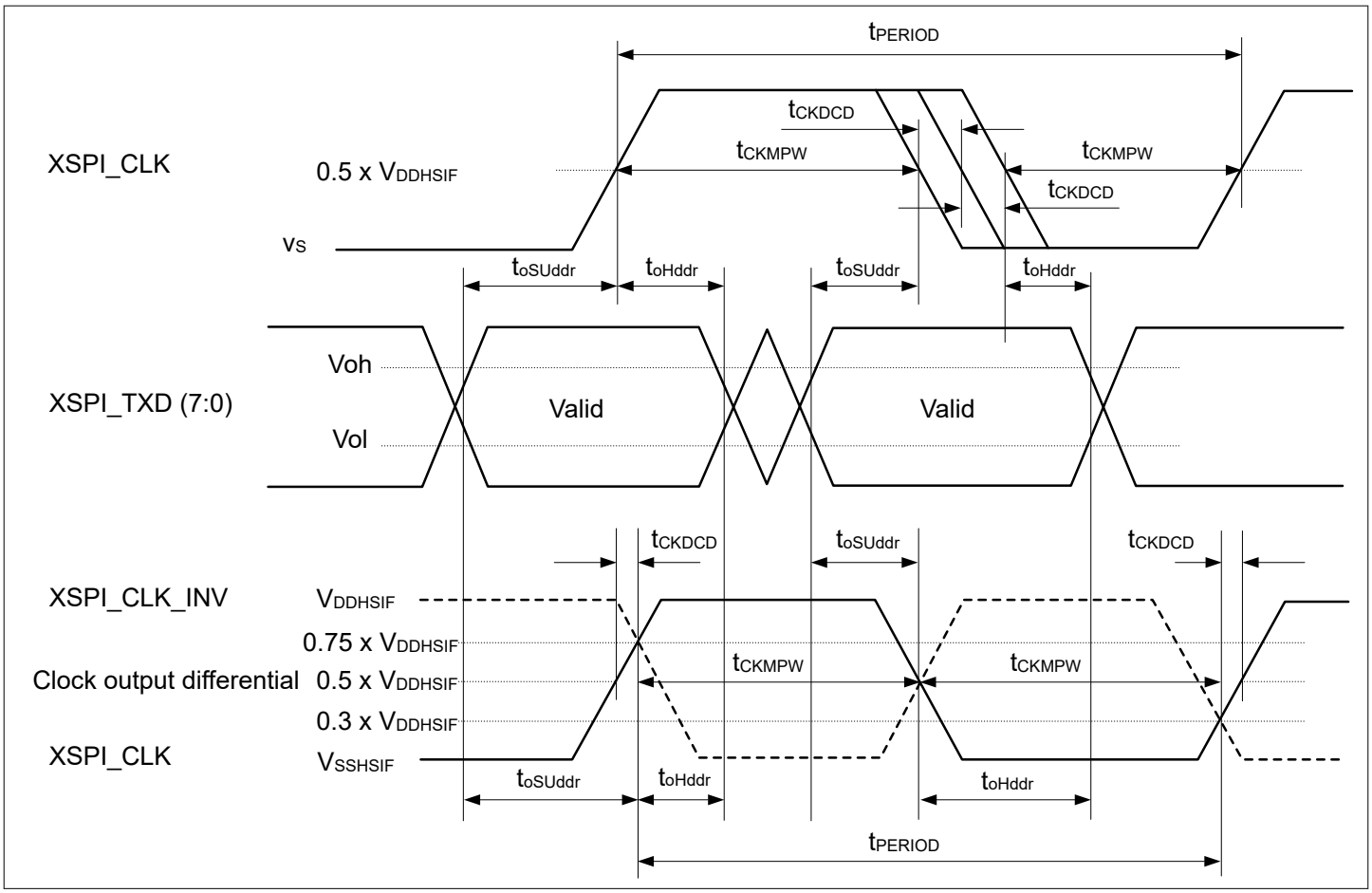


Figure 29 Clock to Data Output Timing

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to CS output timings on page 558
xSPI Clock to CS timing figure on page 559
xSPI Data Strobe input timings on page 560
xSPI data strobe to data input timing figure on page 561
xSPI SDR timing without data strobe on page 562
xSPI SDR without data strobe timing figure on page 564

4.33.3 xSPI Clock to CS output timings

Table 158 xSPI Clock to CS output timings

xSPI Load Definition

The specified load of CL = 15 pF in the table below corresponds to the use case with one connected slave. For further details see xSPI application note.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
xSPI200						
Clock low to CS Low	t_{CKLCSL} CC	8.5	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF
Clock low to CS high	t_{CKLCSH} CC	8.5	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF
CS low to Clock high	t_{CSLCKH} CC	8.5	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF
CS high to Clock high	t_{CSHCKH} CC	8.5	-	-	ns	Timing valid for xSPI200 interface; C_L = 15 pF
xSPI266						
Clock low to CS Low	t_{CKLCSL} CC	6.5	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF
Clock low to CS high	t_{CKLCSH} CC	6.5	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF
CS low to Clock high	t_{CSLCKH} CC	6.5	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF
CS high to Clock high	t_{CSHCKH} CC	6.5	-	-	ns	Timing valid for xSPI266 interface; C_L = 15 pF
xSPI333						
Clock low to CS Low	t_{CKLCSL} CC	5.3	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF
Clock low to CS high	t_{CKLCSH} CC	5.3	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF
CS low to Clock high	t_{CSLCKH} CC	5.3	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF
CS high to Clock high	t_{CSHCKH} CC	5.3	-	-	ns	Timing valid for xSPI333 interface; C_L = 15 pF
xSPI400						
Clock low to CS Low	t_{CKLCSL} CC	4.5	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF
Clock low to CS high	t_{CKLCSH} CC	4.5	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF

(table continues...)

Table 158 (continued) xSPI Clock to CS output timings

xSPI Load Definition

The specified load of CL = 15 pF in the table below corresponds to the use case with one connected slave. For further details see xSPI application note.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CS low to Clock high	t_{CSLCKH} *CC*	4.5	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF
CS high to Clock high	t_{CSHCKH} *CC*	4.5	-	-	ns	Timing valid for xSPI400 interface; C_L = 15 pF

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to Data timing figure on page 557
xSPI Clock to CS timing figure on page 559
xSPI Data Strobe input timings on page 560
xSPI data strobe to data input timing figure on page 561
xSPI SDR timing without data strobe on page 562
xSPI SDR without data strobe timing figure on page 564

4.33.4 xSPI Clock to CS timing figure

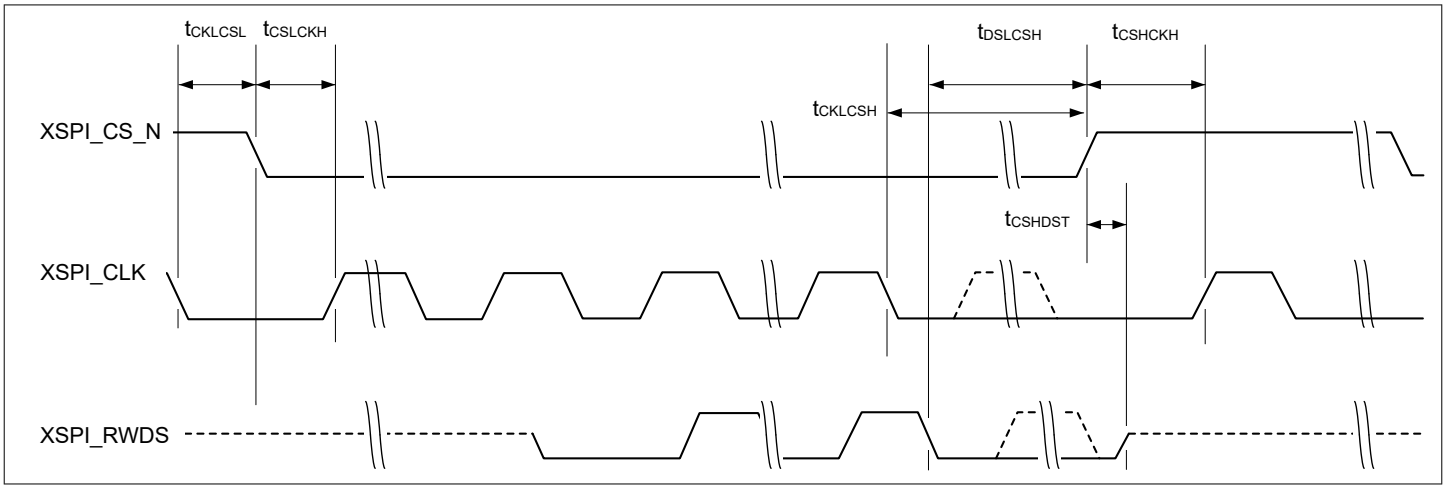


Figure 30 Clock to Chip Select Timing (incl. data strobe)

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to Data timing figure on page 557
xSPI Clock to CS output timings on page 558
xSPI Data Strobe input timings on page 560
xSPI data strobe to data input timing figure on page 561
xSPI SDR timing without data strobe on page 562
xSPI SDR without data strobe timing figure on page 564

4.33.5 xSPI Data Strobe input timings

Table 159 xSPI Data Strobe input timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
xSPI200						
Cycle time data transfer mode	t_{period} *SR*	10	-	-	ns	Timing valid for xSPI200 interface
Duty cycle distortion	t_{DSDCD} *SR*	-	-	0.4	ns	Timing valid for xSPI200 interface
Minimum pulse width	t_{DSMPW} *SR*	4.1	-	-	ns	Timing valid for xSPI200 interface
Input Skew[1)]	t_{RQ} *SR*	-	-	0.9	ns	Timing valid for xSPI200 interface
Input hold skew[1)]	t_{RQH} *SR*	-	-	0.9	ns	Timing valid for xSPI200 interface
xSPI266						
Cycle time data transfer mode	t_{period} *SR*	7.5	-	-	ns	Timing valid for xSPI266 interface
Duty cycle distortion	t_{DSDCD} *SR*	-	-	0.3	ns	Timing valid for xSPI266 interface
Minimum pulse width	t_{DSMPW} *SR*	3.075	-	-	ns	Timing valid for xSPI266 interface
Input Skew[1)]	t_{RQ} *SR*	-	-	0.7	ns	Timing valid for xSPI266 interface
Input hold skew[1)]	t_{RQH} *SR*	-	-	0.7	ns	Timing valid for xSPI266 interface
xSPI333						
Cycle time data transfer mode	t_{period} *SR*	6	-	-	ns	Timing valid for xSPI333 interface
Duty cycle distortion	t_{DSDCD} *SR*	-	-	0.24	ns	Timing valid for xSPI333 interface
Minimum pulse width	t_{DSMPW} *SR*	2.46	-	-	ns	Timing valid for xSPI333 interface
Input Skew[1)]	t_{RQ} *SR*	-	-	0.58	ns	Timing valid for xSPI333 interface
Input hold skew[1)]	t_{RQH} *SR*	-	-	0.58	ns	Timing valid for xSPI333 interface
xSPI400						
Cycle time data transfer mode	t_{period} *SR*	5	-	-	ns	Timing valid for xSPI400 interface

(table continues...)

Table 159 (continued) xSPI Data Strobe input timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Duty cycle distortion	t_{DSDCD} *SR*	-	-	0.2	ns	Timing valid for xSPI400 interface
Minimum pulse width	t_{DSMPW} *SR*	2.05	-	-	ns	Timing valid for xSPI400 interface
Input Skew[1)]	t_{RQ} *SR*	-	-	0.5	ns	Timing valid for xSPI400 interface
Input hold skew[1)]	t_{RQH} *SR*	-	-	0.5	ns	Timing valid for xSPI400 interface

1) The corresponding timing parameter is valid for the DLL setting DLL_CFG.RXCFG = 8 which corresponds to a phase shift of 80 ° between clock and data

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to Data timing figure on page 557
xSPI Clock to CS output timings on page 558
xSPI Clock to CS timing figure on page 559
xSPI data strobe to data input timing figure on page 561
xSPI SDR timing without data strobe on page 562
xSPI SDR without data strobe timing figure on page 564

4.33.6 xSPI data strobe to data input timing figure

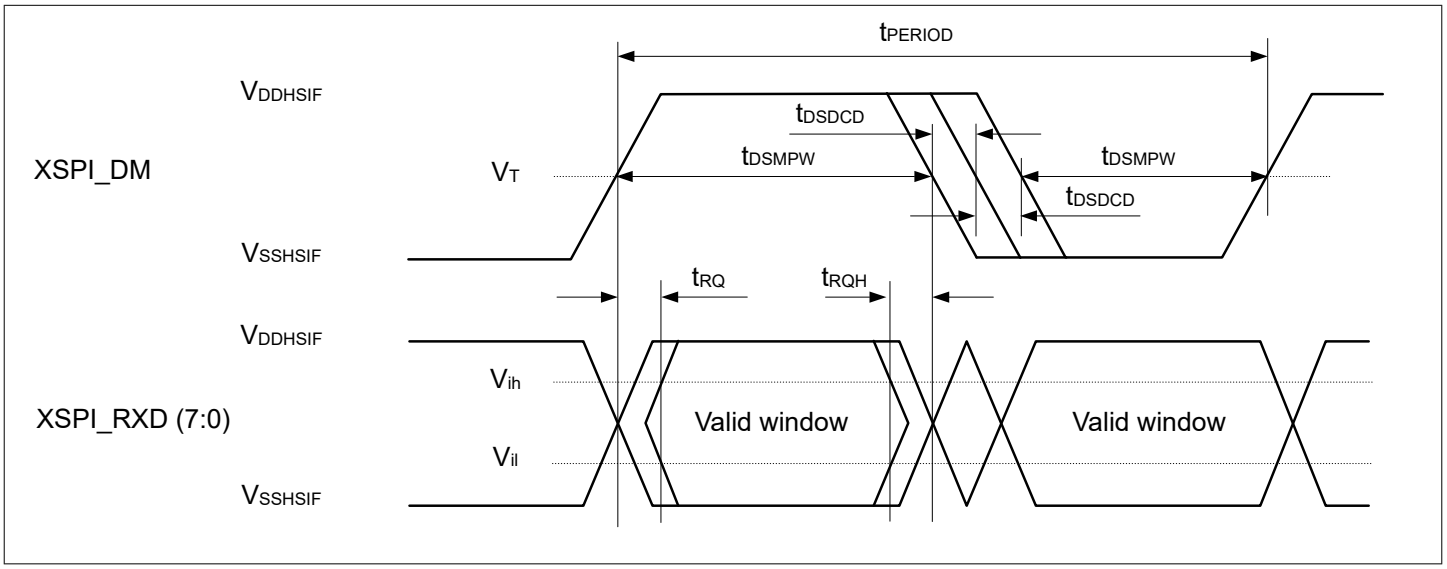


Figure 31 Data Strobe to Data Input Timing

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to Data timing figure on page 557

xSPI Clock to CS output timings on page 558
xSPI Clock to CS timing figure on page 559
xSPI Data Strobe input timings on page 560
xSPI SDR timing without data strobe on page 562
xSPI SDR without data strobe timing figure on page 564

4.33.7 xSPI SDR timing without data strobe

Table 160 xSPI SDR timing without data strobe

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transmit frequency in SDR mode	f_{TX_SDR} *CC*	-	-	133	MHz	Valid for Port 16; driver = xSPI400
		-	-	25	MHz	Valid for Port 11 (only available in STD package variant) and Port 20; driver = strong, edge = sharp
Receive frequency in SDR mode	f_{RX_SDR} *CC*	-	-	133	MHz	Valid for Port 16; V_{DDHSIF} = 3.3 V
		-	-	50	MHz	Valid for Port 16; V_{DDHSIF} = 1.8 V
		-	-	25	MHz	Valid for Port 11 (only available in STD package variant) and Port 20; V_{DDEXT} = 3.3 V

(table continues...)

Table 160 (continued) xSPI SDR timing without data strobe

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock low to input valid timing[1]	t_V *SR*	1	-	6	ns	Valid for Port 16; $f_{RX\_SDR} \leq 133$ MHz; $V_{DDHSIF} = 3.3$ V and $V_{DDHSIF} = 1.8$ V; Enable the loopback clock by setting the register CTRLR0.CLK_LOOP_EN and DLL_CFG.RXSAMPLESEL. Depending on the system load, the loopback clock can be shifted to align with the input data by setting the appropriate value in the register DLL_CFG.RXCFG [2]
		1	-	8	ns	Valid for Port 11 (only available in STD package variant) and Port 20; $f_{RX\_SDR} \leq 25$ MHz; $V_{DDEXT} =$ 3.3 V; depending on the system load the sample delay shall be adapted by setting the corresponding value inside register RX_SAMPLE_DELAY.RSD
		1	-	8	ns	Valid for Port 16; $f_{RX\_SDR} \leq 50$ MHz; $V_{DDEXT} = 1.8$ V; depending on the system load the sample delay shall be adapted by setting the corresponding value inside register RX_SAMPLE_DELAY.RSD
Output hold time[1]	t_{hosdr} *CC*	2.0	-	-	ns	
Output setup time[1]	t_{susdr} *CC*	2.0	-	-	ns	

1) Timing is measured at 50% of the output level
2) Without the loopback and sample delay included, it is possible to reach up to 83 MHz

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to Data timing figure on page 557
xSPI Clock to CS output timings on page 558
xSPI Clock to CS timing figure on page 559
xSPI Data Strobe input timings on page 560
xSPI data strobe to data input timing figure on page 561
xSPI SDR without data strobe timing figure on page 564

4.33.8 xSPI SDR without data strobe timing figure

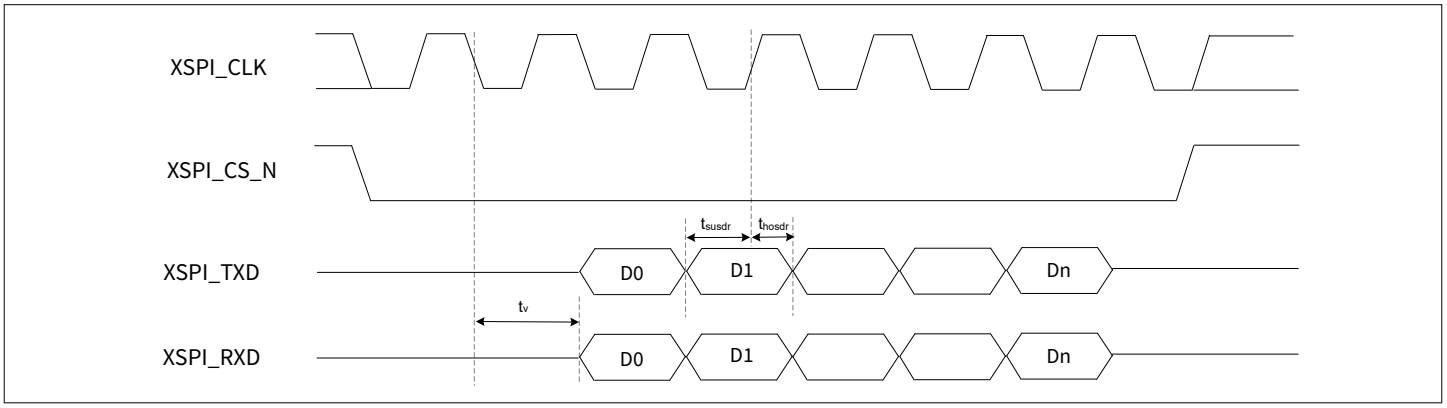


Figure 32 SDR without Data Strobe Timing

Related information

xSPI Clock to Data output timings on page 554
xSPI Clock to Data timing figure on page 557
xSPI Clock to CS output timings on page 558
xSPI Clock to CS timing figure on page 559
xSPI Data Strobe input timings on page 560
xSPI data strobe to data input timing figure on page 561
xSPI SDR timing without data strobe on page 562

4.34 DAP timing characteristics

The following characteristics are applicable for communication through the DAP debug interface.

4.34.1 DAP timing

Table 161 DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} *SR*	6.25	-	-	ns	
DAP0 high time	t_{12} *SR*	2	-	-	ns	
DAP0 low time	t_{13} *SR*	2	-	-	ns	
DAP0 clock rise time	t_{14} *SR*	-	-	1	ns	f = 160 MHz
		-	-	4	ns	f = 40 MHz
		-	-	2	ns	f = 80 MHz
DAP0 clock fall time	t_{15} *SR*	-	-	1	ns	f = 160 MHz
		-	-	4	ns	f = 40 MHz
		-	-	2	ns	f = 80 MHz
DAP1 setup to DAP0 rising edge[1)]	t_{16} *SR*	4	-	-	ns	f = 160 MHz or f = 80 MHz
		5	-	-	ns	f = 40 MHz
DAP1 hold after DAP0 rising edge	t_{17} *SR*	2	-	-	ns	
DAP1 valid per DAP0 clock period[1)]	t_{19} *CC*	4	-	-	ns	C_L = 20 pF; f = 160 MHz
		8	-	-	ns	C_L = 20 pF; f = 80 MHz
		10	-	-	ns	C_L = 50 pF; f = 40 MHz

1) Timing parameter and parameter value is also valid for the DAP2 and DAP3 lines

Related information

SCR DAP timing on page 565
DAP timing figures on page 566

4.34.2 SCR DAP timing

Table 162 SCR DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} *SR*	50	-	-	ns	
DAP0 high time	t_{12} *SR*	15	-	-	ns	
DAP0 low time	t_{13} *SR*	15	-	-	ns	

(table continues...)

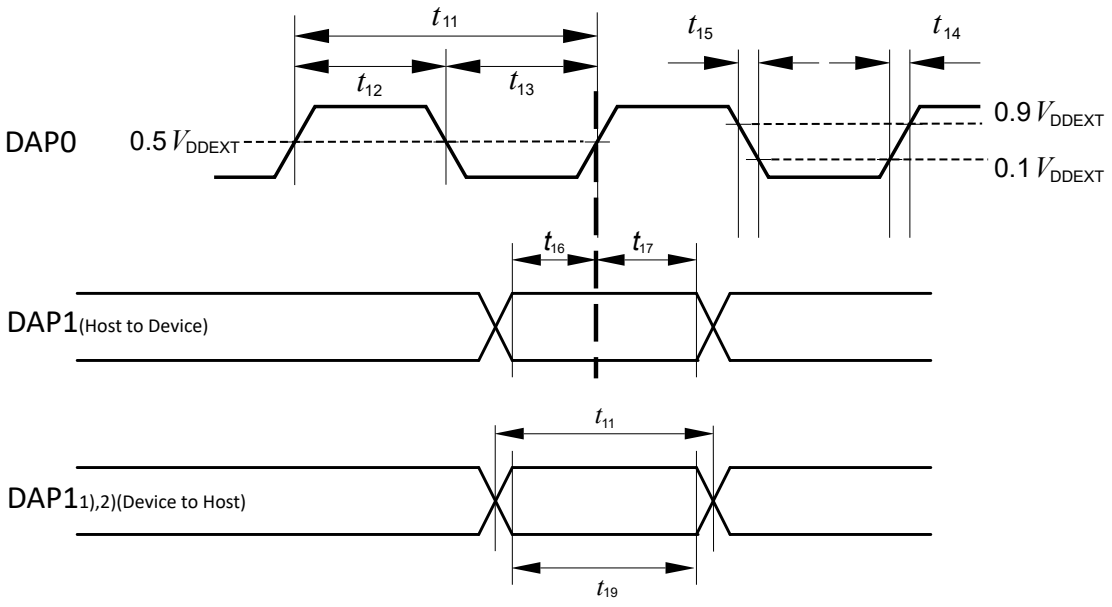
Table 162 (continued) SCR DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} *SR*	-	-	8	ns	*f* = 20 MHz
DAP0 clock fall time	t_{15} *SR*	-	-	8	ns	*f* = 20 MHz
DAP1 setup to DAP0 rising edge	t_{16} *SR*	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} *SR*	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} *CC*	30	-	-	ns	C_L = 20 pF; *f* = 20 MHz

Related information

DAP timing on page 565
DAP timing figures on page 566

4.34.3 DAP timing figures



1) The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

2) No explicit setup and hold times are given for DAP1 for the direction Device to Host. Only t11 and t19 are guaranteed and the tool may set the sample point freely.

Figure 33 DAP timing

Related information

DAP timing on page 565
SCR DAP timing on page 565

4.35 JTAG timing characteristics

The following characteristics are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

The explanation of the timing characteristics can be found in the 'JTAG timing figures' sub-chapter.

4.35.1 JTAG timing

Table 163 JTAG timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TCK clock period	t_1 *SR*	50	-	-	ns	
TCK high time	t_2 *SR*	10	-	-	ns	
TCK low time	t_3 *SR*	10	-	-	ns	
TCK clock rise time	t_4 *SR*	-	-	4	ns	
TCK clock fall time	t_5 *SR*	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 *SR*	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 *SR*	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 *CC*	3.0	-	-	ns	$C_L \leq 20$ pF
		-	-	26.5	ns	$C_L \leq 50$ pF
TDO hold after TCK falling edge	t_{18} *CC*	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 *CC*	-	-	28	ns	$C_L \leq 50$ pF
TDO valid output to high impedance from TCK falling edge	t_{10} *CC*	-	-	25	ns	$C_L \leq 50$ pF

Related information

JTAG timing figures on page 568

4.35.2 JTAG timing figures

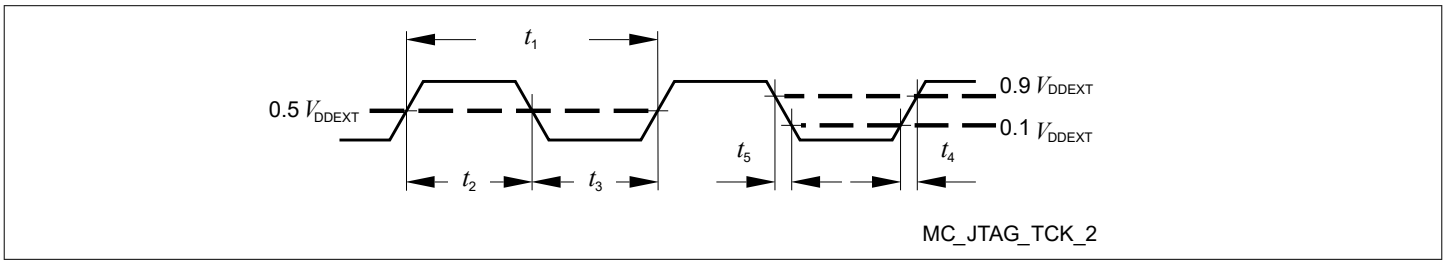


Figure 34 Test clock timing (TCK)

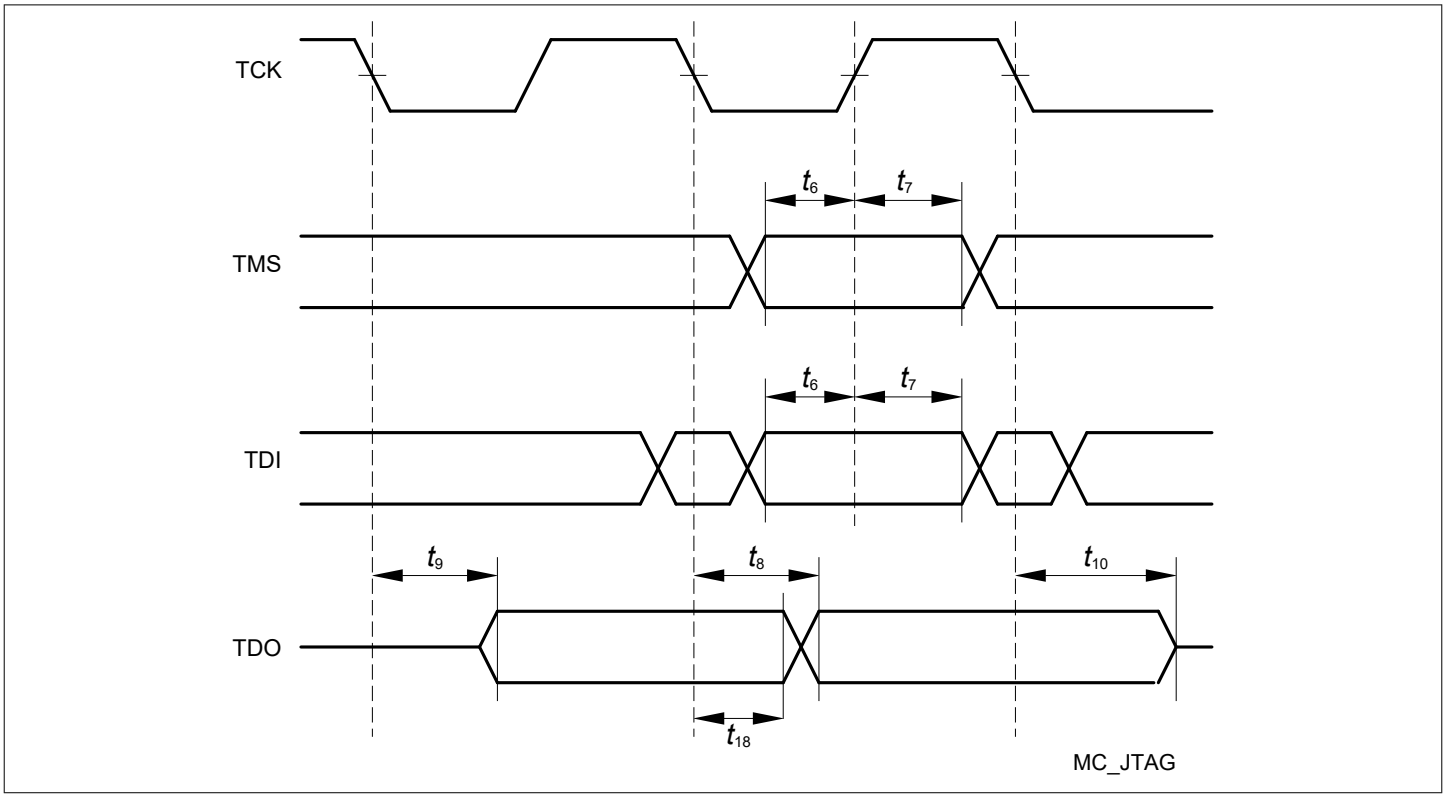


Figure 35 JTAG timing

Related information

JTAG timing on page 567

4.36 SGBT characteristics

SGBT is a trace interface dedicated for laboratory use only. Defined timing is only valid for laboratory conditions.

4.36.1 SGBT transmitter characteristics

Table 164 SGBT transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Differential signal characteristics						
Differential p-p voltage	*TX_V_{diff_pp} CC*	600	-	1200	mV	
Differential DC impedance	*TX_Z_{diff_dc} CC*	80	-	120	Ohm	
AC characteristics						
Rise time 20%-80%	*TX_T_{rise} CC*	30	-	-	ps	Measured at BGA pins by de-embedding the breakout channel (no additional de-embedding of the package is applied).
Fall time 20%-80%	*TX_T_{fall} CC*	30	-	-	ps	Measured at BGA pins by de-embedding the breakout channel (no additional de-embedding of the package is applied).
Differential skew	*TX_T_{skew} CC*	-	-	20	ps	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	20	ps	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	20	ps	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)
Deterministic jitter	*J_D CC*	-	-	0.15	UI	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	0.17	UI	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	0.17	UI	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)

(table continues...)

Table 164 (continued) SGBT transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total jitter	J_T *CC*	-	-	0.35	UI	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	0.35	UI	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	0.35	UI	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)
External AC coupling capacitance	*TX_*C_{ac_ext} *SR*	75	100	200	nF	
Timing characteristics						
Data rate	*TX_DR CC*	4999.5	5000	5000.5	Mbps	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		3999.6	4000	4000.4	Mbps	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		1999.8	2000	2000.2	Mbps	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)

4.37 External components

4.37.1 HSPHY external components

4.37.2 Buffering and decoupling capacitors

Table 166 Buffering and decoupling capacitors

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Capacitances on VDD pins / rail[1]	$C_{VDD\_EXTDEC\ SR}$	-50%	2x1000 +2x100 +2x47	+50%	nF	Capacitors placed on bottom PCB layer below center ball matrix.
Capacitances on VDDEXT pins / rail[1]	$C_{VDDEXT\_EXTBUF\ SR}$	-50%	4.7	50%	µF	
Capacitances on VDDEXT pins / rail[1]	$C_{VDDEXT\_EXTDEC\ SR}$	-50%	4 x 100	+50%	nF	
Capacitances on VDDEXT pins / rail[1]	$C_{VDDEXTOSC\_EXTDEC\ SR}$	-50%	100	+50%	nF	XTAL supply. Decoupling to local VSSOSC ground
Capacitances on VDDEVRSB pins / rail[1]	$C_{VDDEVRSB\_EXTDEC\ SR}$	-50%	100	+50%	nF	
Capacitances on VDDEXTDC pins / rail[1] [2]	$C_{VDDEXTDC\_EXTDEC\ SR}$	-50%	100	+50%	nF	VDDEXTDC is tied to VDDEXT and Capacitor is omitted if EVRC not used.
Capacitances on each VDDMx pins / rail[1]	$C_{VDDM\_EXTDEC\ SR}$	-50%	100	+50%	nF	
Filter on VAREFx pins / rail[1]	$C_{VAREF\_EXTFIL\ SR}$	-50%	2.2	+50%	µF	Additional Resistor depending on noise and usecase
Capacitances on each VDDPHPHYx pins / rail[1]	$C_{VDDPHPHYx\_EXTDEC\ SR}$	-50%	1000 + 100	+50%	nF	Bigger capacitor may be omitted if regulator capacitors present
Capacitances on each VDDPHYx pins / rail[1]	$C_{VDDPHYx\_EXTDEC\ SR}$	-50%	2200 + 100	+50%	nF	Capacitors for each HSPHY unit to ensure SGMII GETH (1Gbps) functionality. For PCIe interface, additional Ferrite is required.
Capacitances on VDDHSIF pins / rail[1]	$C_{VDDHSIF\_EXTDEC\ SR}$	-50%	1000 + 100	+50%	nF	Bigger capacitor required if xSPI is active.

1) The given capacitors serve as a reference example considering typical power pattern use cases and load jumps as documented in the datasheet. This is derived based on an example PCB implementation and regulator schematic scheme as shown in the figure and is verified only by simulation and validation and not characterization. The capacitances may not cover all extremities of use cases, all external regulators and components, therefore the implementation need to be additionally validated by the user together with the chosen regulators to ensure function. The tolerances of the capacitors need to be confirmed by the chosen capacitor vendor and adequate derating margins shall be applied for temperature, dc bias, lifetime and maximum continuous operation duration. Therefore Infineon cannot take liability on capacitor performance or tolerance, PCB implementations and external regulator schemes and this needs to be ensured by the user.

2) Component size 0402 can be used in order to realize a capacitor placement as close as possible to the ball/pin. Other capacitance values and component sizes are also possible.

4.38 Quality declarations

4.38.1 Quality parameters

Table 167 Quality parameters

Quality Parameters (Golden Reference)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	*MSL CC*	-	-	3		Conforming to JEDEC J-STD-020 for 260°C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} *SR*	-	-	250	V	for all balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} *SR*	-	-	1000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} *SR*	-	-	500	V	
Operation Lifetime	t_{OP} *CC*	-	-	24500	hour	see "Example temperature profile" as an example
Number of allowed power cycles	N_{PC} *SR*	-	-	$1.5*10^6$	cycles	

4.38.2 SRAM related fault tolerance

Table 168 SRAM related fault tolerance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum number of acceptable hard Single-Bit Errors[1)]	M_{SBE} *CC*	-	-	12		Total RAM considered SRAM_TOT = 12301 kB [1)]
Maximum number of Bitline-oriented Errors	M_{BLE} *CC*	-	-	2		

1) The parameter considers all RAMs being used by application except the ones specifically marked in the User Manual device specific VMT chapter with "Exclude from test" or part of G1*/G2_1*

5 Package information

Topics:

- PG-F2BGA-436
- PG-F2BGA-292
- PG-F2HBGA-436

You can find all of the Infineon packages, types of packing and package related information, on our internet pages: www.infineon.com/products.

5.1 PG-F2BGA-436

5.1.1 PG-F2BGA-436 outline

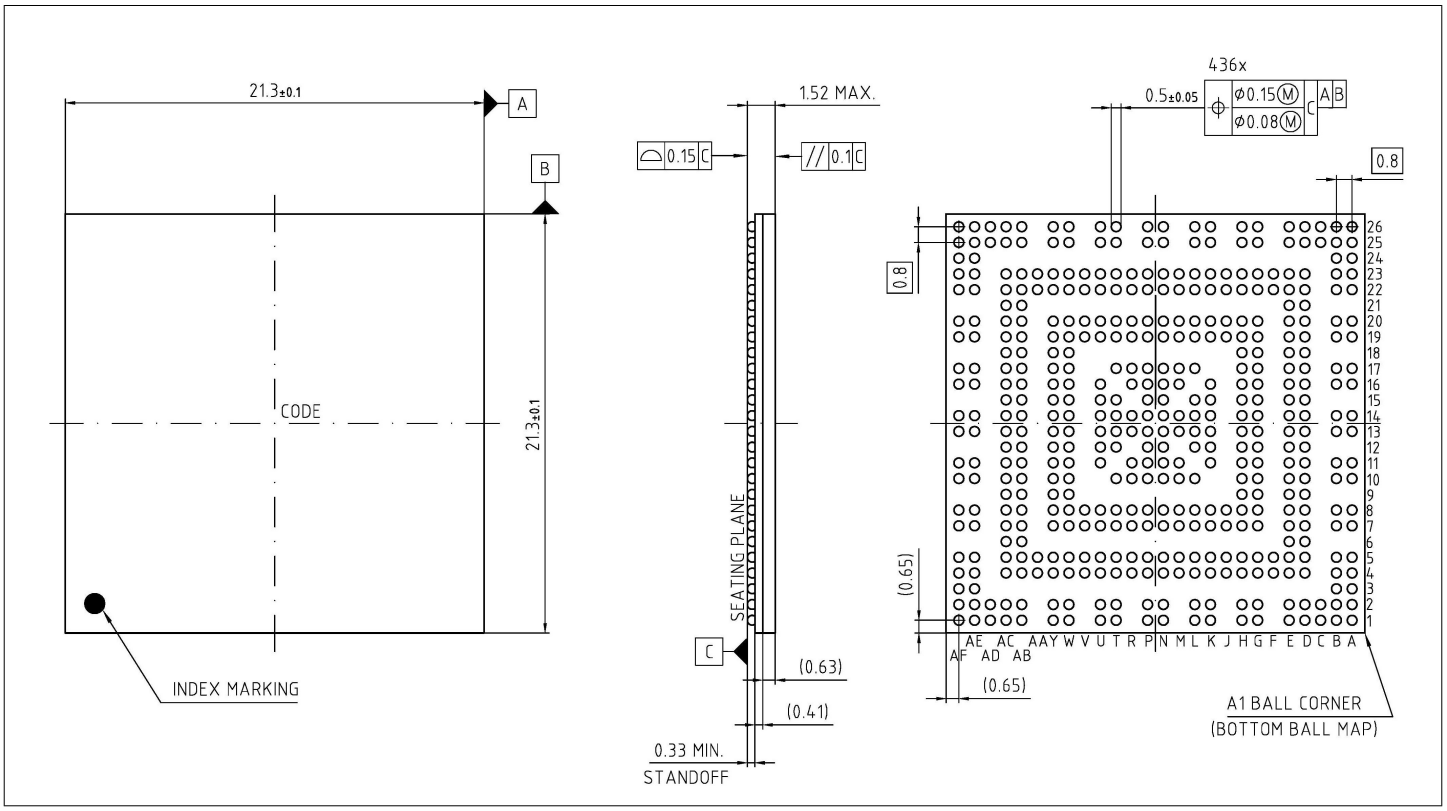


Figure 36 PG-F2BGA-436 Outline

5.1.2 PG-F2BGA-436 characteristics

Table 169 PG-F2BGA-436 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum Force applicable on package against top cooling TIM interface and mounting	P_{kgTopF} *SR*	-	100.0	-	N	

(table continues...)

Table 169 (continued) PG-F2BGA-436 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
JEDEC Top Thermal resistance with heat sink at top of uC (junction to case top)	$R_{th\text{-}JCT}$ *CC*	-	1.1[1)]	-	K/W	Com power pattern used.
JEDEC Bottom thermal resistance with heat sink at bottom of uC (junction to case bottom)	$R_{th\text{-}JCB}$ *CC*	-	3.0[1)]	-	K/W	Com power pattern used
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_ECU}$ *CC*	-	17	-	K/W	Standard cooling stack and PCB considered as described in UM. Com Power Pattern with reduced ambient temperature T_A = 85°C.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_uC}$ *CC*	-	8	-	K/W	Com Power Pattern with reduced ambient temperature T_A = 85°C.
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_ECU}$ *CC*	-	9.2	-	K/W	Top cooling stack and PCB considered as described in UM. TIM thickness = 1.16mm, TIM Conductivity = 2.6W/mK. Com power pattern used.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_uC}$ *CC*	-	3	-	K/W	Com power pattern used.
Max allowed Power Dissipation considering Package and Thermal boundary conditions	T_{PD} *SR*	-	-	4.5	W	Com Power pattern

1) All parameters are established using thermal simulations. The top and bottom thermal resistances between the case and the ambient (R_{TH_JCA}, R_{TH_JCA}) are to be combined with the thermal resistances between the junction and the case given above (R_{TH_JCT}, R_{TH_JCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TH_JA}). The thermal resistances between the case and the ambient (R_{TH_JCA}, R_{TH_JCA}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: ($T_J = T_A + R_{THJA}$ * PD), where the R_{THJA} is the total thermal resistance between the junction and the ambient. R_{TH_JCT} and R_{TH_JCB} case thermal resistances are measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1). R_{THJA} is established using reference ECU / PCB stacks and automotive boundary conditions as documented in the User Manual.

5.2 PG-F2BGA-292

5.2.1 PG-F2BGA-292 outline

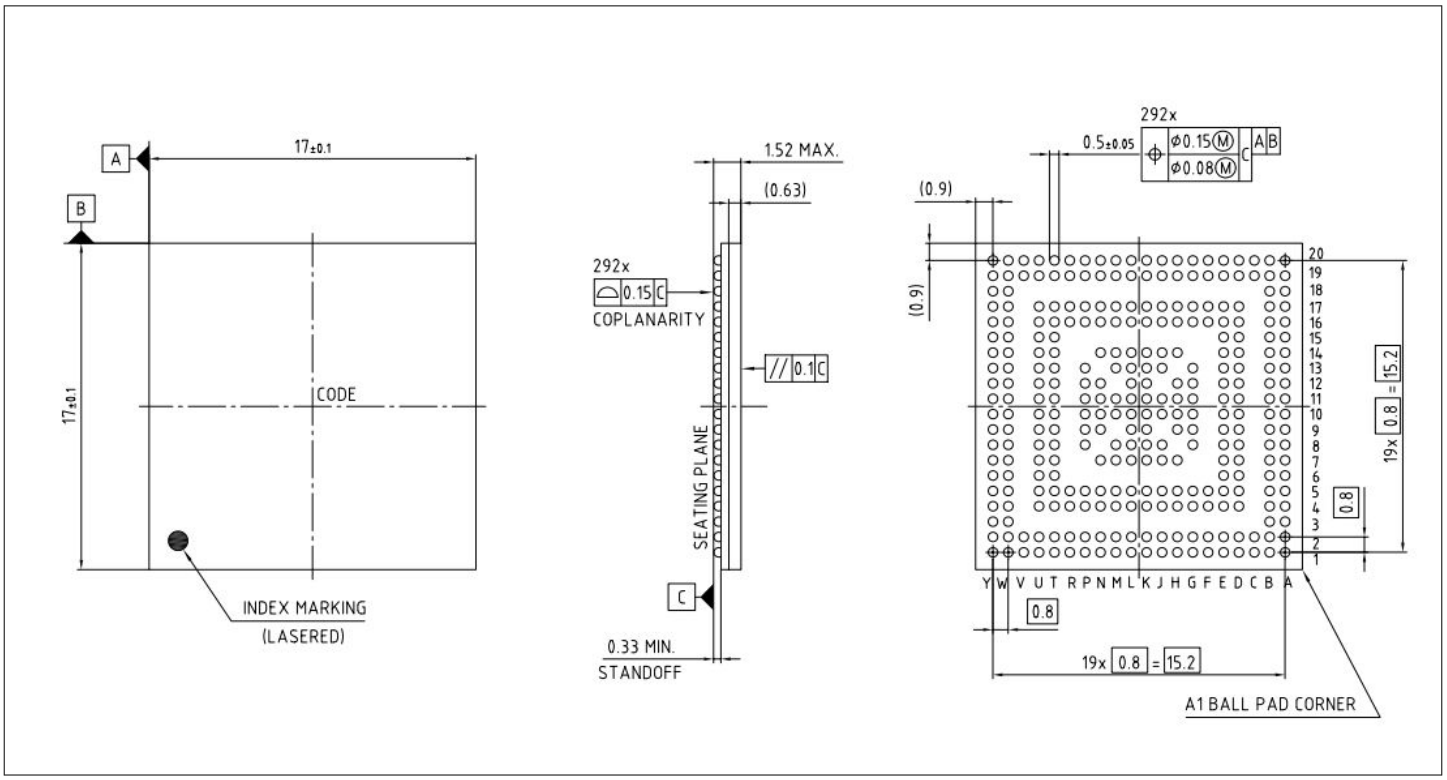


Figure 37 PG-F2BGA-292 Outline

5.2.2 PG-F2BGA-292 characteristics

Table 170 PG-F2BGA-292 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum Force applicable on package against top cooling TIM interface and mounting	P_{kgTopF} *SR*	-	65	-	N	
JEDEC Top Thermal resistance with heat sink at top of uC (junction to case top)	$R_{th\text{-}JCT}$ *CC*	-	1.1[1)]	-	K/W	Com power pattern used.
JEDEC Bottom thermal resistance with heat sink at bottom of uC (junction to case bottom)	$R_{th\text{-}JCB}$ *CC*	-	3.4[1)]	-	K/W	Com power pattern used.

(table continues...)

Table 170 (continued) PG-F2BGA-292 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_ECU}$ *CC*	-	17.5	-	K/W	Standard cooling stack and PCB considered as described in UM. Com Power Pattern with reduced ambient temperature T_A = 85°C.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_uC}$ *CC*	-	8.6	-	K/W	Com Power Pattern with reduced ambient temperature T_A = 85°C.
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_ECU}$ *CC*	-	9.2	-	K/W	Top cooling stack and PCB considered as described in UM. TIM thickness = 1.16mm, TIM Conductivity = 2.6W/mK. Com power pattern used.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_uC}$ *CC*	-	3	-	K/W	Com power pattern used.
Max allowed Power Dissipation considering Package and Thermal boundary conditions	T_{PD} *SR*	-	-	4.5	W	Com Power pattern

1) All parameters are established using thermal simulations. The top and bottom thermal resistances between the case and the ambient (RTH_JCA, RTH_JCA) are to be combined with the thermal resistances between the junction and the case given above (RTH_JCT, RTH_JCB), in order to calculate the total thermal resistance between the junction and the ambient (RTH_JA). The thermal resistances between the case and the ambient (RTH_JCA, RTH_JCA) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: (TJ = TA + RTHJA * PD), where the RTHJA is the total thermal resistance between the junction and the ambient. RTH_JCT and RTH_JCB case thermal resistances are measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1). RTHJA is established using reference ECU / PCB stacks and automotive boundary conditions as documented in the User Manual.

5.3 PG-F2HBGA-436

5.3.1 PG-F2HBGA-436 outline

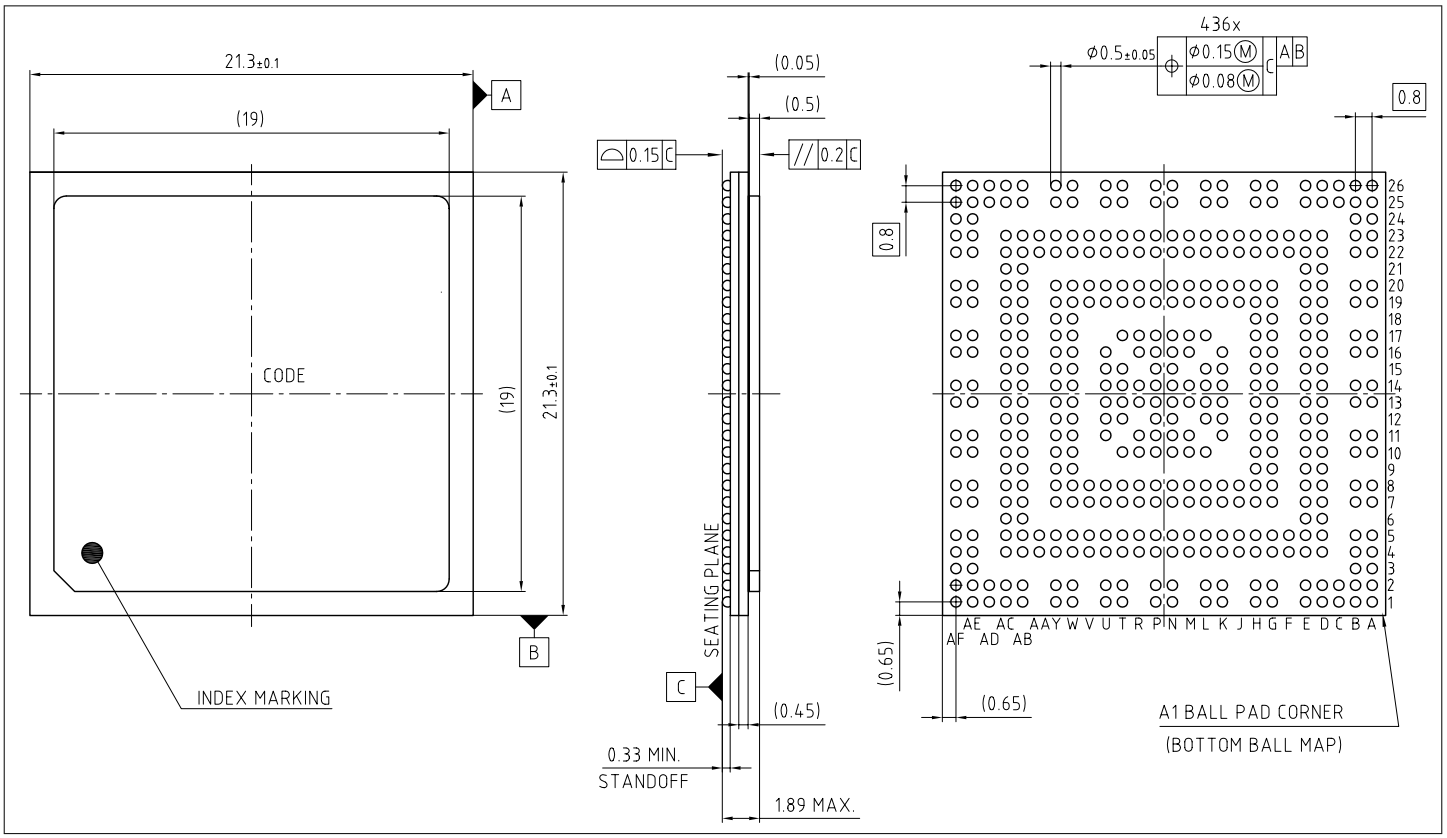


Figure 38 PG-F2HBGA-436 Outline

5.3.2 PG-F2HBGA-436 characteristics

Table 171 PG-F2HBGA-436 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum Force applicable on package against top cooling TIM interface and mounting	P_{kgTopF} *SR*	-	100.0	-	N	
JEDEC Top Thermal resistance with heat sink at top of uC (junction to case top)	$R_{th\text{-}JCT}$ *CC*	-	0.9[1)]	-	K/W	Com Power Pattern used.
JEDEC Bottom thermal resistance with heat sink at bottom of uC (junction to case bottom)	$R_{th\text{-}JCB}$ *CC*	-	2.3[1)]	-	K/W	Com Power Pattern used.

(table continues...)

Table 171 (continued) PG-F2HBGA-436 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_ECU}$ *CC*	-	16	-	K/W	Standard cooling stack and PCB considered as described in UM. Com Power Pattern with reduced ambient temperature Ta = 85°C.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Standard Cooling)	$R_{th\text{-}JA\_SC\_uC}$ *CC*	-	7	-	K/W	Com Power Pattern with reduced ambient temperature Ta = 85°C.
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_ECU}$ *CC*	-	7.2	-	K/W	Top cooling stack and PCB considered as described in UM. TIM thickness = 1.16mm, TIM Conductivity = 2.6W/mK. Max Power Pattern used.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Top Cooling)	$R_{th\text{-}JA\_TC\_uC}$ *CC*	-	1.5	-	K/W	Max Power Pattern used.
Max allowed Power Dissipation considering Package and Thermal boundary conditions	T_{PD} *SR*	-	-	6.6[2)]	W	Max Power Pattern

1) All parameters are established using thermal simulations. The top and bottom thermal resistances between the case and the ambient (R_{TH_JCA}, R_{TH_JCA}) are to be combined with the thermal resistances between the junction and the case given above (R_{TH_JCT}, R_{TH_JCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TH_JA}). The thermal resistances between the case and the ambient (R_{TH_JCA}, R_{TH_JCA}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: ($T_J = T_A + R_{THJA} * PD$), where the R_{THJA} is the total thermal resistance between the junction and the ambient. R_{TH_JCT} and R_{TH_JCB} case thermal resistances are measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1). R_{THJA} is established using reference ECU / PCB stacks and automotive boundary conditions as documented in the User Manual.

2) Maximum allowed Power Dissipation can be estimated for different temperatures using the following equation: TPD = (TPCBMax_ECU - TA_ECU) / (RthJA_x_ECU - PsiJB_x_uC CC).

6 History

	First public release

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