REF BGT60LTR11AIP M0

XENSIV™ 60 GHz radar reference board

Board version V1.0

About this document

Scope and purpose

This application note describes the function, circuitry, and performance of the 60 GHz radar BGT60LTR11AIP M0 reference board (REF_BGT60LTR11AIP_M0). The board provides supporting circuitry to the XENSIV™ BGT60LTR11AIP monolithic microwave integrated circuit (MMIC) with antenna-in-package (AIP).

This BGT60LTR11AIP M0 reference board offers a digital interface for configuration and transfer of the acquired radar data to an Arm® Cortex®-M0 based microcontroller.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems, working with Infineon's XENSIV™ 60 GHz radar sensors.

Related documents

Additional information can be found in the documentation provided with the Radar BGT60LTR11AIP tool available from the Infineon Developer Center (IDC), or from www.infineon.com/60GHz.

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1 Introduction

1.1 Overview

The BGT60LTR11AIP MMIC is a fully integrated microwave motion sensor including Antenna in Package (AIP), built-in motion and direction of motion detectors. This small-sized radar solution is a compelling, smart and cost-effective replacement for conventional passive infrared (PIR) sensors in low-power or battery-powered applications. The MMIC is designed to operate as a Doppler motion sensor in the 60 GHz ISM-band.

The MMIC supports multiple operation modes, including autonomous mode and SPI mode, which can be selected via the QS1 pin.

The MMIC has four quad-state (QS1-4) input pins that give the performance parameters flexibility even when it is running in autonomous mode. These pins are used for configuration of the MMIC as explained in section 4.

In SPI mode, a full flexibility regarding radar MMIC parameters configuration e.g., detection threshold, hold time and operation frequency, is offered by writing into the MMIC registers the wanted configuration, using an external microcontroller unit (MCU). In this mode, the integrated detectors also deliver digital outputs indicating motion and direction of motion. If further signal processing is needed, the radar raw data can be extracted and sampled from BGT60LTR11AIP MMIC and then used for developing customized algorithms for maximum performance. The BGT60LTR11AIP M0 reference board works in SPI mode.

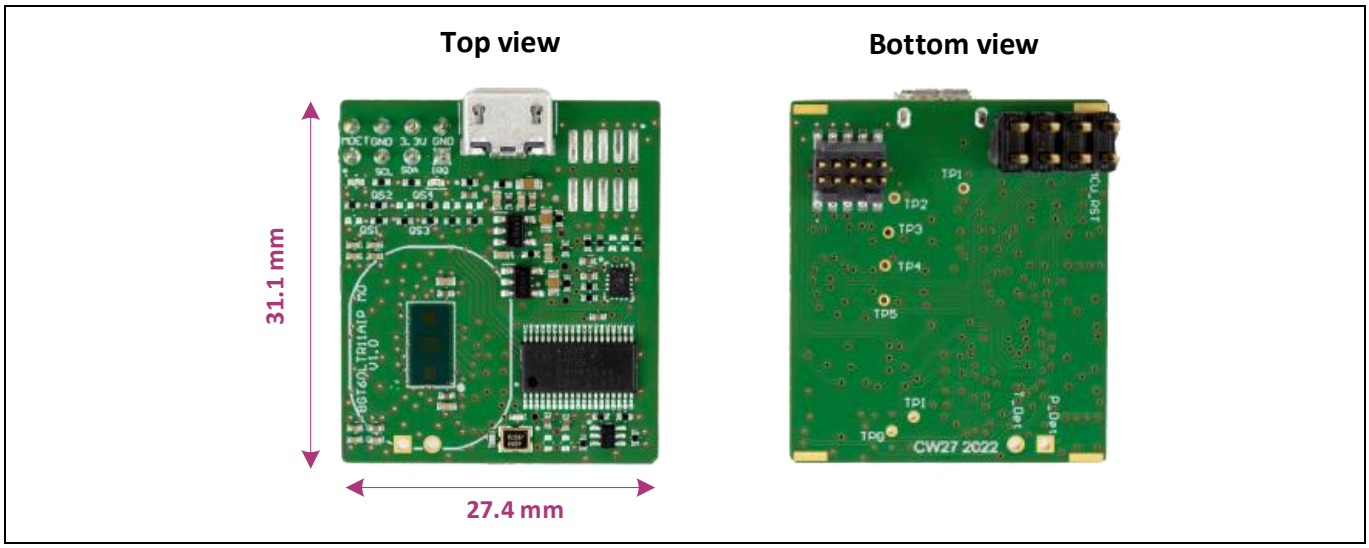


Figure 1 Top and bottom views of the BGT60LTR11AIP M0 reference board

1.2 Key features

The BGT60LTR11AIP M0 reference board is optimized for fast prototyping designs and system integrations as well as initial product feature evaluations. In addition, the sensor can be integrated into systems like laptops, tablets, TVs, speakers etc. to 'wake' them up based on motion (or direction of motion) detection, put them to sleep or auto-lock when no motion is detected for a defined amount of time. This way, it can be a smart power saving feature for these devices and might also eliminate the need for keyword-based activation of systems. Radar sensors offer the possibility to hide them inside the end product since they operate through non-metallic materials. Therefore, it enables a seamless integration of technology in our day-to-day lives.

Some key features of the BGT60LTR11AIP M0 reference board are as follows:

- Form factor of 31 mm x 28 mm
- Features an AIP MMIC of small size (6.7 mm x 3.3 mm x 0.56 mm), thereby eliminating antenna design complexity at the user end
- Detects motion and direction of movement (approaching or departing) for a human target
- Works standalone (autonomous mode) or also with SPI mode to interface with an external Cortex®-M0 microcontroller to do further signal processing
- Configurable settings like operation mode, detector threshold, hold time, operating frequency

2 System specifications

Table 1 lists the various parameters of the BGT60LTR11AIP M0 reference board.

Table 1 BGT60LTR11AIP M0 reference board specifications

Parameter	Unit	Min.	Typ.	Max.	Comments
System performance					
Maximum detection range	m		10	14	Typical motion detection range for human target at high sensitivity (in both E-plane and H-plane orientation)
Power supply					
Supply voltage	V		5.0		
Current consumption	mA		13		At 5V supplied via USB PRT = 500µs, pulse width = 5µs (LEDs off) (9.2mA M0 MCU + 3mA MMIC)
Antenna characteristics (measured)					
Antenna type			1 x 1		Antenna-in-Package (AIP)
Horizontal – 3 dB beam width (HPBW)	Degrees		80		At frequency = 61.25 GHz
Elevation – 3 dB beam width (HPBW)	Degrees		80		At frequency = 61.25 GHz

3 Hardware description

This section presents an overview of the board's hardware building blocks, such as BGT60LTR11AIP MMIC, microcontroller, power supply, crystal, and board interfaces.

3.1 Key features

The BGT60LTR11AIP M0 reference board is a PCB of 26 x 28 mm size as shown in Figure 2. Mounted on top of the PCB is a BGT60LTR11AIP, Infineon's 60 GHz radar sensor. The antennas are integrated into the chip package; therefore, the PCB can be manufactured using a standard FR4 laminate. The board can be powered up by using the USB port or the 3.3V pins. Two On semi LDOs are used for providing a clean supply to the components on the board. The board has an Arm® Cortex® M0 microcontroller, XMC1302-T038X0200 to apply different settings to the MMIC and also to perform further signal processing and algorithm implementations using the output signals of the MMIC. Communication between the MMIC and the MCU is mainly performed via a Serial Peripheral Interface (SPI). These signals need to be level shifted using a level shifter to interface with the SPI block of the MCU. BSD84N (Q1A) and SN74AVC4T245RSVR (U5) are used for level shifting. The MMIC uses a 38.4 MHz crystal (Y1 as an oscillator source with a stable reference clock. The Cortex Debug connector can be placed on the top side or the bottom side of the board and is used to connect an XMC™ Link (J-Link based debug probe). The connectors provide access to other important signals of the board. The board has two LEDs (D1 and D2) to output the results from the MCU. The block diagram of the board is shown in Figure 3.

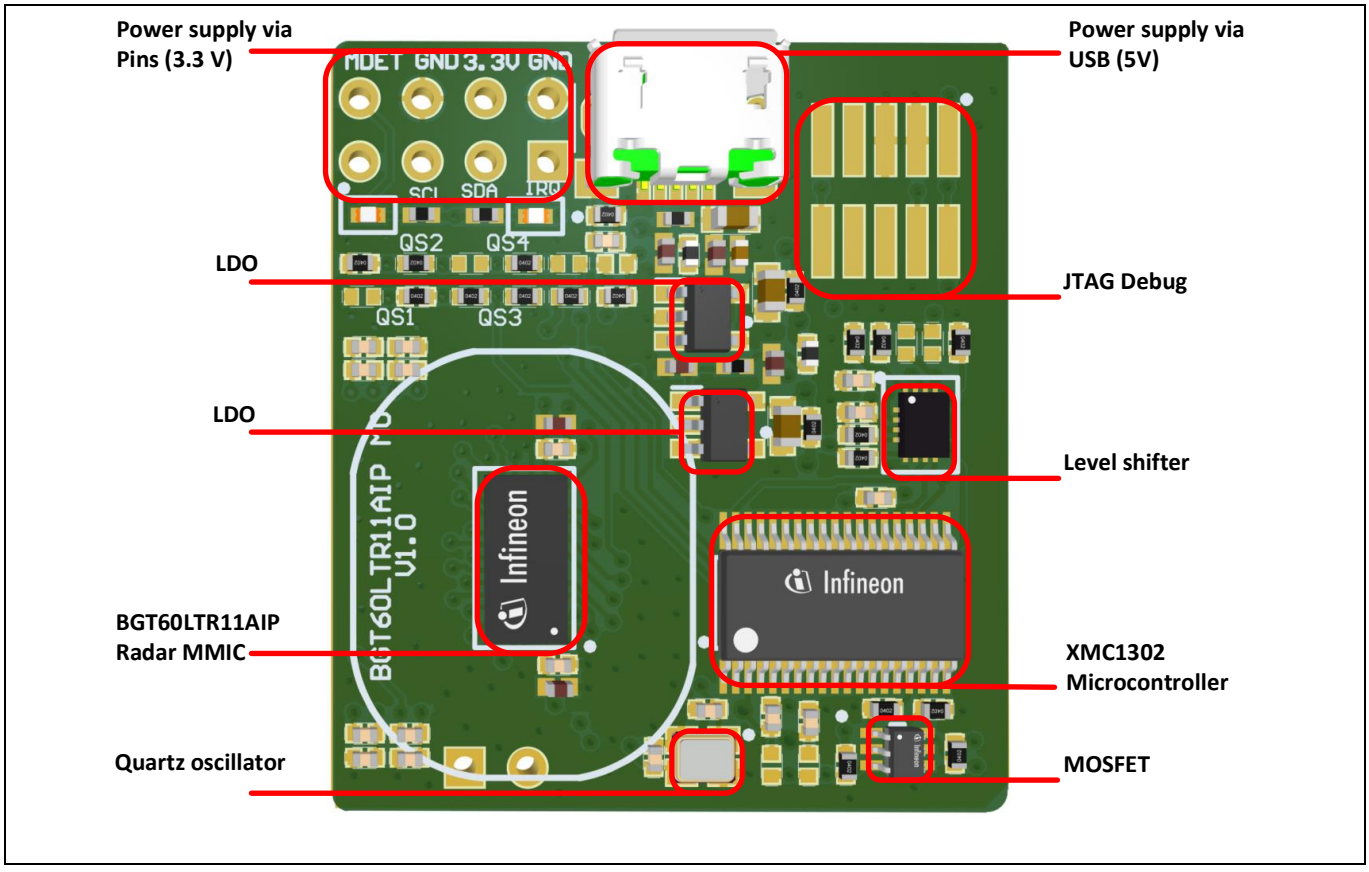


Figure 2 Components on the BGT60LTR11AIP M0 reference board

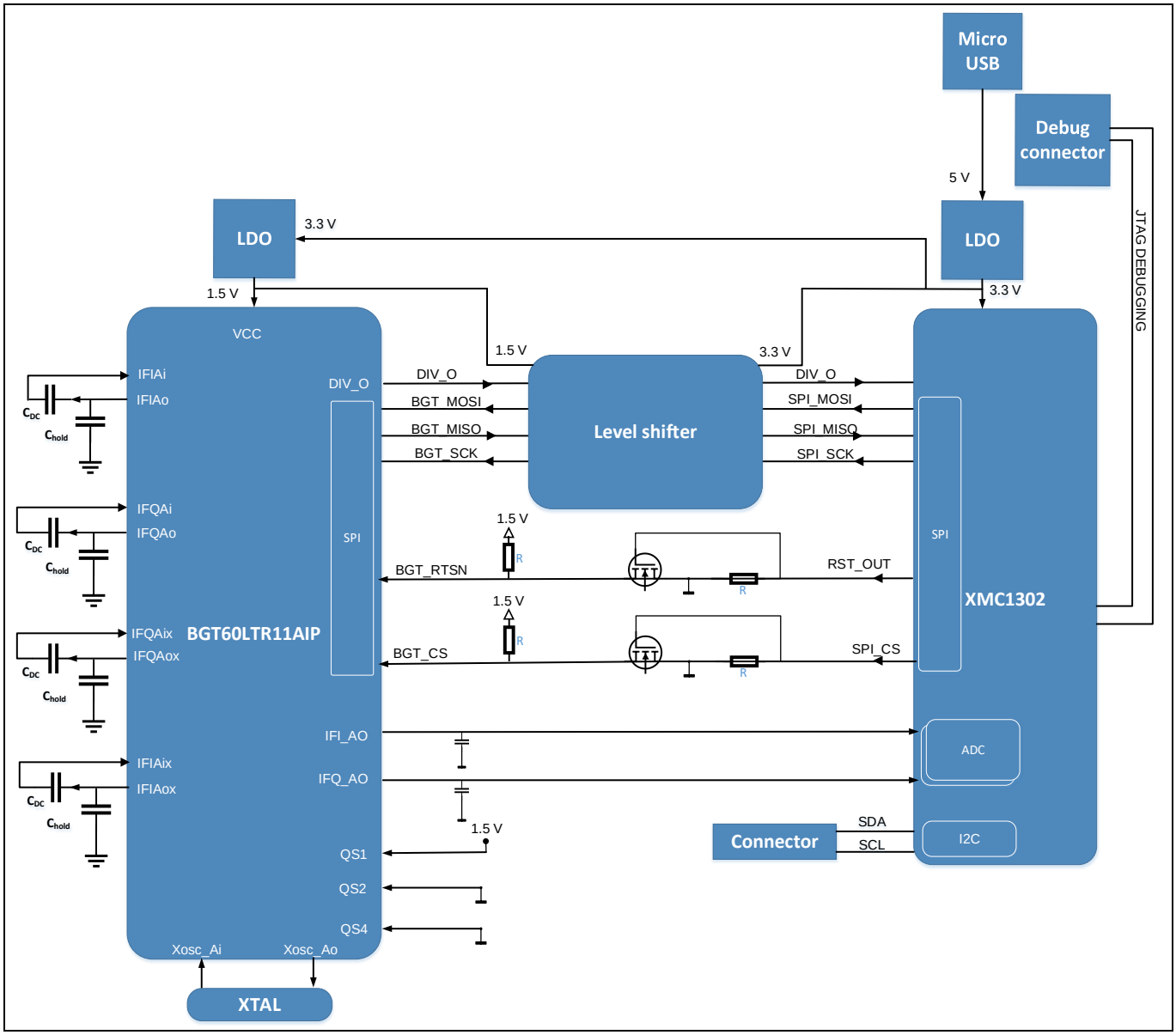


Figure 3 Block diagram of the BGT60LTR11AIP M0 reference board

3.2 BGT60LTR11AIP MMIC

The BGT60LTR11AIP MMIC (Figure 4) serves as the main element on the BGT60LTR11AIP M0 reference board. The MMIC has one transmit antenna and one receive antenna integrated into the package, shown in Figure 5. The package dimensions are 6.7 mm x 3.3 mm x 0.56 mm, as illustrated in Figure 6.

The MMIC has an integrated Voltage Controlled Oscillator (VCO) and Phase Locked Loop (PLL) for high-frequency signal generation. The transmit section consists of a Medium Power Amplifier (MPA) with configurable output power, which can be controlled via the SPI.

The chip features a low-noise quadrature receiver stage. The receiver uses a Low Noise Amplifier (LNA) in front of a quadrature homodyne down-conversion mixer to provide excellent receiver sensitivity. Derived from the internal VCO signal, an RC Poly-Phase Filter (PPF) generates quadrature LO signals for the quadrature mixer.

The Analog Base Band (ABB) unit consists of an integrated sample and hold circuit for low-power duty-cycled operation followed by an externally configurable high-pass filter, a Variable Gain Amplifier (VGA) stage and a low-pass filter.

The integrated target detector circuits in the MMIC indicate the detection of movement in front of the radar and the direction of movement with two digital signals (BGT_TARGET_DET and BGT_PHASE_DET). See section 3.9 for more details. The detector circuit offers a user-configurable hold-time for maximum flexibility.

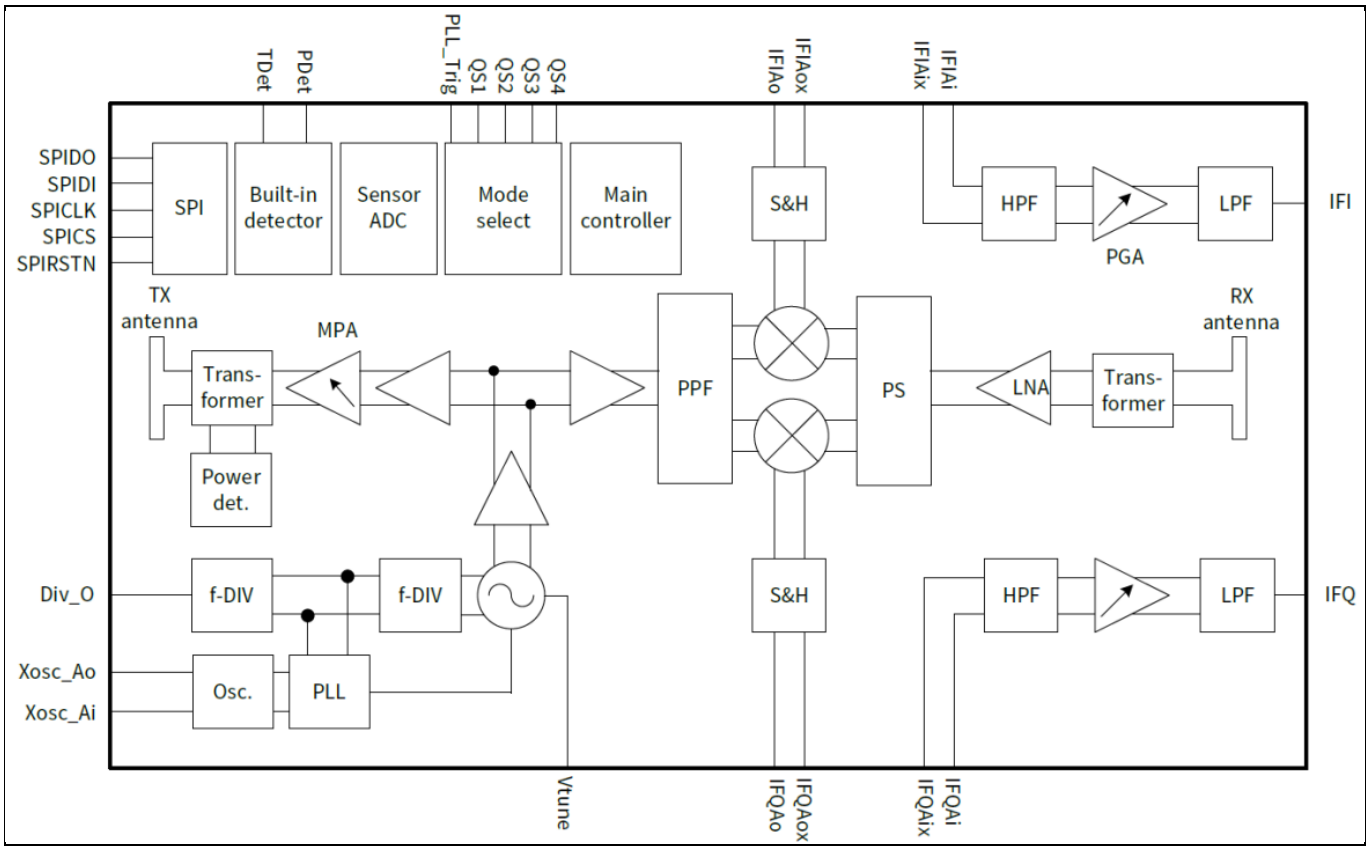


Figure 4 BGT60LTR11AIP MMIC block diagram

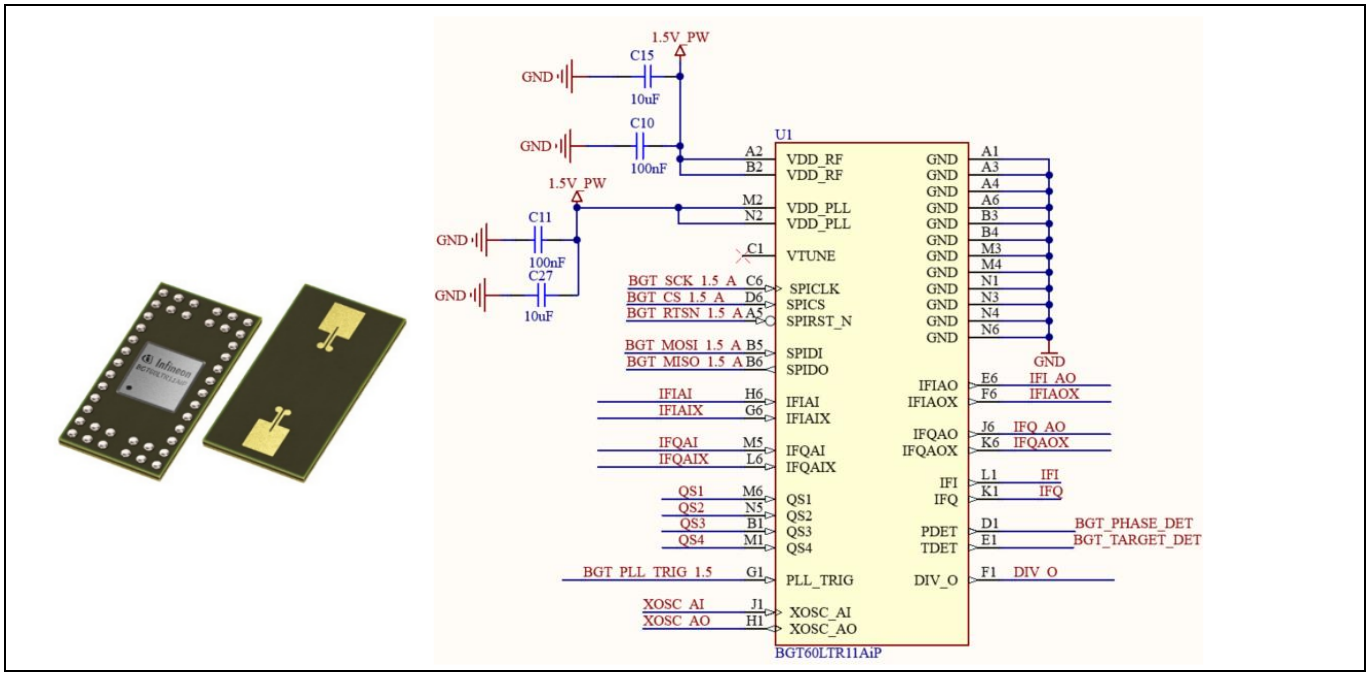


Figure 5 Package and pin-signal assignment of the BGT60LTR11AIP MMIC

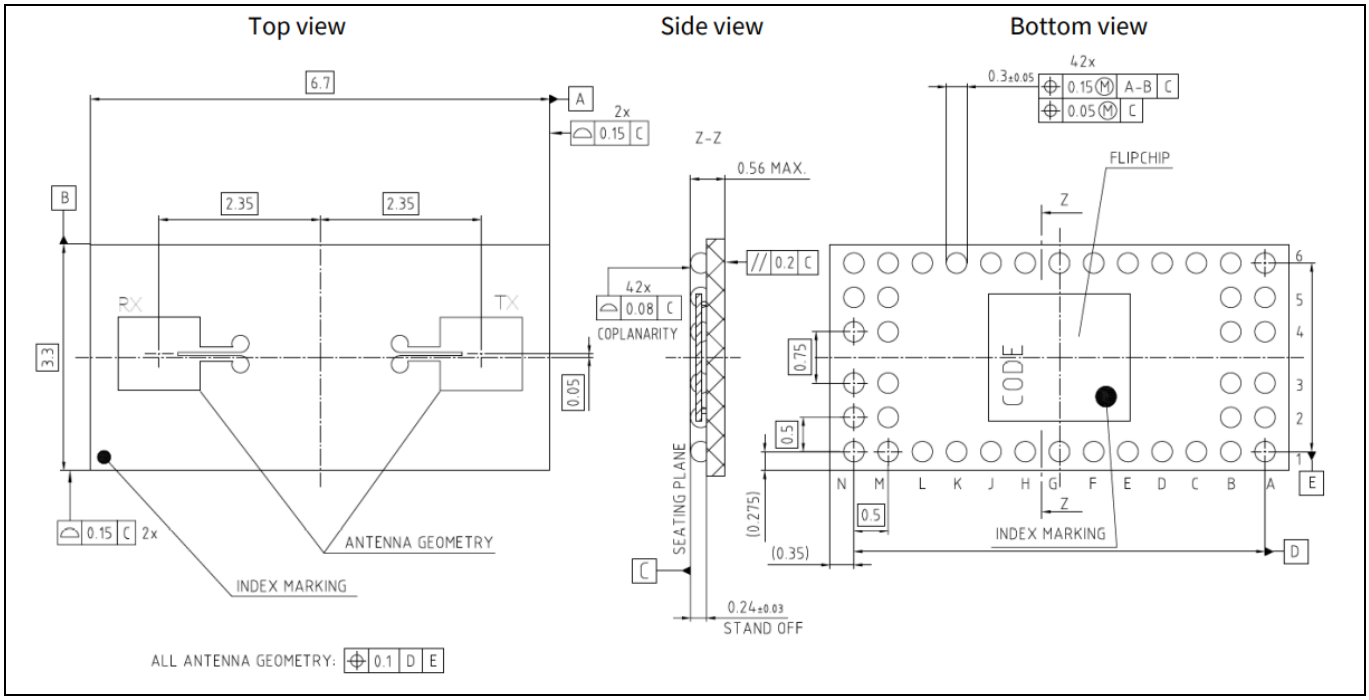


Figure 6 Top, side, and bottom views of the BGT60LTR11AIP MMIC package – all dimensions in mm

3.3 Microcontroller unit - XMC1302

The BGT60LTR11AIP M0 reference board uses an Arm® Cortex®-M0 microcontroller to allow flexibility to the users to do their own signal processing and algorithm implementations. Infineon's XMC™ 32-bit industrial microcontroller (XMC1302-T038X0200) is designed for system cost and efficiency for demanding industrial applications. It comes with the most advanced peripheral set in the industry. Fast and largely autonomous peripherals can be configured to support individual needs. Highlights include analog-mixed signal, timer/PWM and communication peripherals powered by an Arm® Cortex®-M0 core.

3.4 Sensor supply

Since radar sensors are very sensitive to supply voltage fluctuations or crosstalk between different supply domains, a low-noise power supply as well as properly decoupled supply rails are vital. Figure 7 depicts the schematics of the low-pass filters employed to decouple the supplies of the different power rails in the BGT60LTR11AIP M0 reference board . Two LDOs are used in cascaded implementation to create stable and clean supply voltages of 1.5V (for the MMIC), and 3.3V (for the MCU). R11 and R19 can be used to make accurate current consumption measurements at the output of both the LDOs. Test points TP2, TP3, TP4, and TP5 can be used for such measurements. One can choose between two different LDO packages. For this board, G1 and G2 are DNPs.

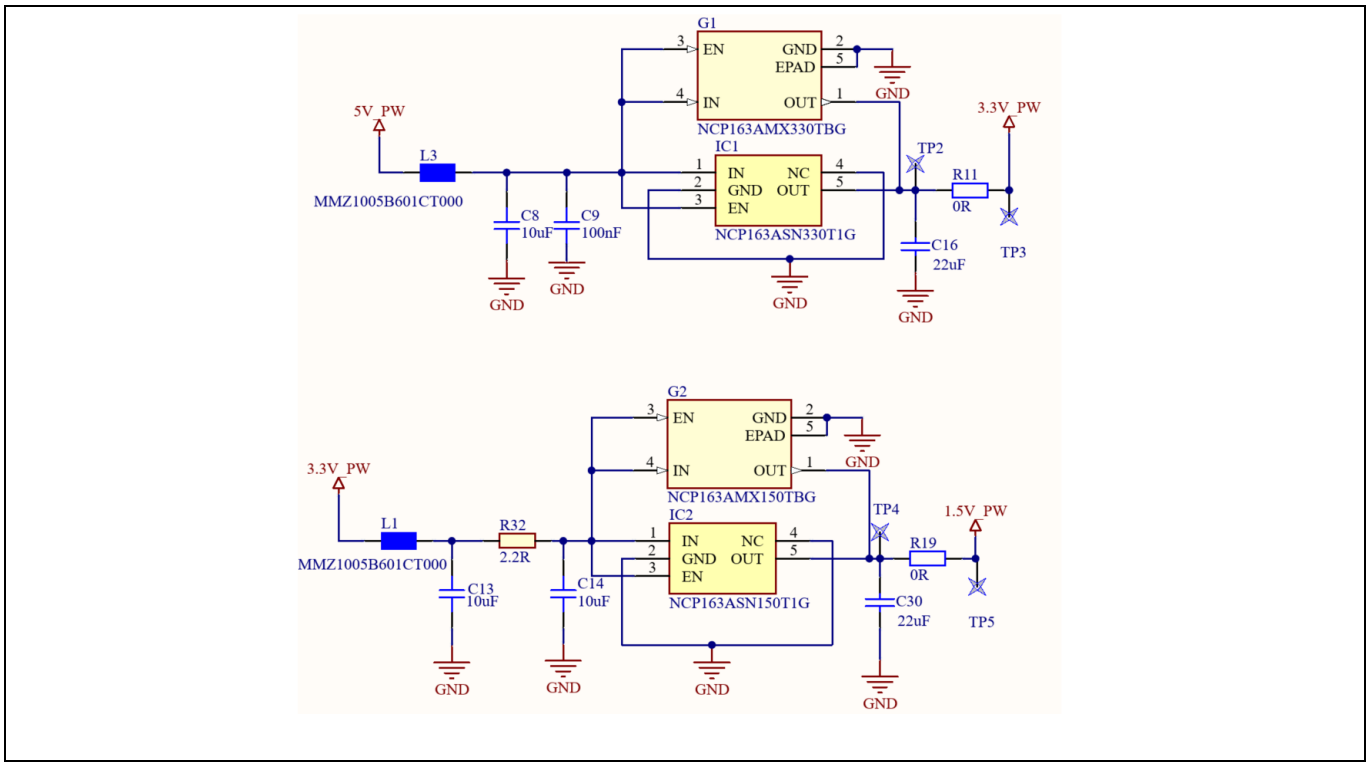


Figure 7 Schematics of the sensor supply and low-pass filters

3.5 Crystal

The MMIC requires an oscillator source with a stable reference clock providing low phase jitter and low phase noise. The oscillator is integrated inside the MMIC. This saves current consumption, as crystal oscillator consumes only a few milliamperes (mA) and runs continuously. The BGT60LTR11AIP M0 reference board uses a 38.4 MHz crystal oscillator, as shown in Figure 8.

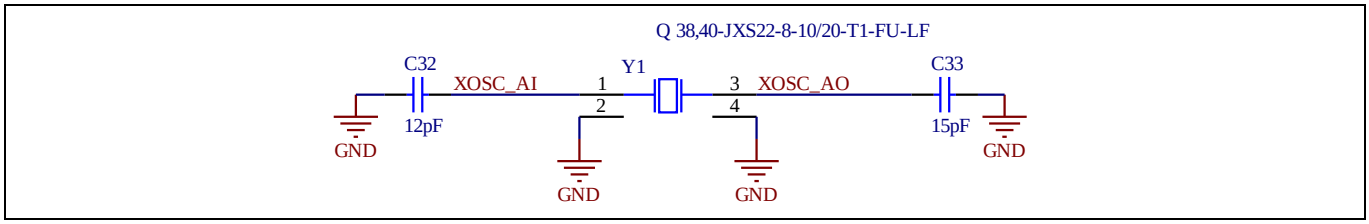


Figure 8 The crystal circuit on the BGT60LTR11AIP M0 reference board

3.6 External capacitors

The BGT60LTR11AIP MMIC is duty-cycled and performs a sample and hold (S&H) operation for lower power consumption. The S&H switches are integrated in chip at each differential IQ mixer output ports. They are controlled synchronously via the internal state machine. The capacitors between S&H and the high-pass filter (HPF) are external (Figure 9). C21, C22, C23 and C24 are 5.6 nF capacitors used as “hold” capacitors for the S&H circuitry. They can be configured for different pulse width settings, as shown in Table 2. C17, C18, C19 and C20 are the DC blocking (or High Pass) capacitors. They are 10 nF to get a high pass of 4 Hz (if internal high pass resistor, RHP = 4 MΩ). It is not recommended to use higher values as it will affect the Analog Base Band (ABB) settling time. The DC blocking capacitors are important because the mixer output has a different DC voltage than the internal ABB. In Figure 9, the external hold (Chold) and high-pass capacitors (CHP) are shown for all four branches in the differential IQ configuration.

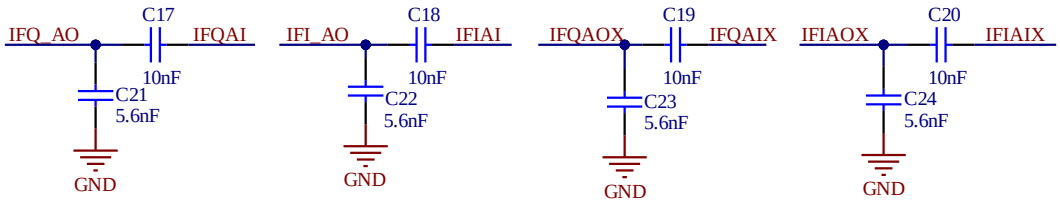


Figure 9 External capacitors

Table 2 Recommended hold capacitors (C21, C22, C23 and C24) for different pulse width

Pulse width (µs)	Hold capacitor value (nF)
3	4.7
4	5.6
5 (default)	5.6 (default)
10	15

Charging time of the hold capacitor (C_{hold}) is limited to the selected pulse width. Shorter pulse widths require smaller C_{hold} to get it ~ 90% charged during one pulse. Rise-time is controlled by the C_{hold} itself and the internal mixer output resistance (R_{mixer_out}) of 300 Ω in each branch.

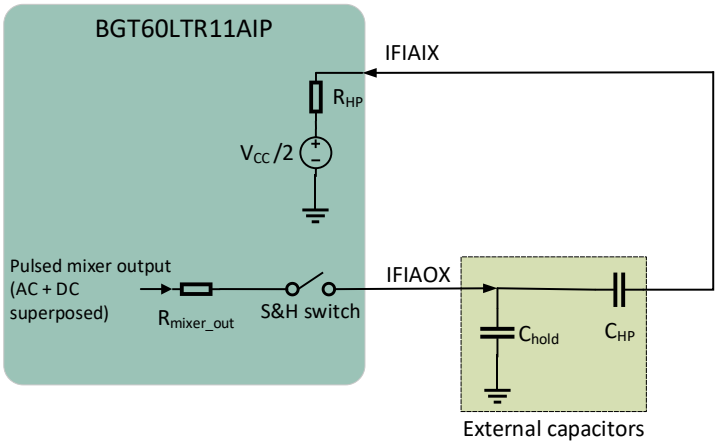


Figure 10 External capacitors for BGT60LTR11AIP

A longer pulse width can have a higher C_{hold} value. This leads to a reduced bandwidth (BW) of the RC fiter (R_{mixer_out} and C_{hold}). Consequently, there will be lower baseband noise because of reduced noise folding bandwidth.

For this RC structure, the low pass 3dB cutoff frequency ($f_{LP_{3dB}}$) can be calculated under following conditions:

t_{rise} = 10% / 90% = S&H ON time = 4µs

Pulse width = 5 µs

R_{mixer_out} = 300 Ω

$$f_{LP_{3dB}} = \frac{0.35}{t_{rise}} = \frac{0.35}{4\mu s} = 87.5\ kHz$$

Or based on the formula:

$$f_{LP_{3dB}} = \frac{1}{2\pi \times R_{mixer\_out} \times C_{hold}}$$

$C_{hold} = 6.1\ nF$
$\rightarrow 5.6\ nF$ (closest E12 series value)

The high-pass 3dB cutoff frequency ($f_{HP_{3dB}}$) can be calculated under following conditions:

C_{HP} = 10nF

R_{HP} = 4MΩ

$$f_{HP_{3dB}} = \frac{1}{2\pi \times R_{HP} \times C_{HP}} = \frac{1}{2\pi \times 4M\Omega \times 10nF} = 4\ Hz$$

3.7 Connectors

The BGT60LTR11AIP M0 reference board has a Cortex Debug (10-pin) connector, J2 to easily allow debugging the XMC1302 and give user flexibility for their own implementations. The P2 and P3 connectors provide access to other important signals of the board such as the I²C signals (SCL and SDA) and the outputs of the internal detectors of the MMIC (BGT_PHASE DET and BGT_TARGET_DET).

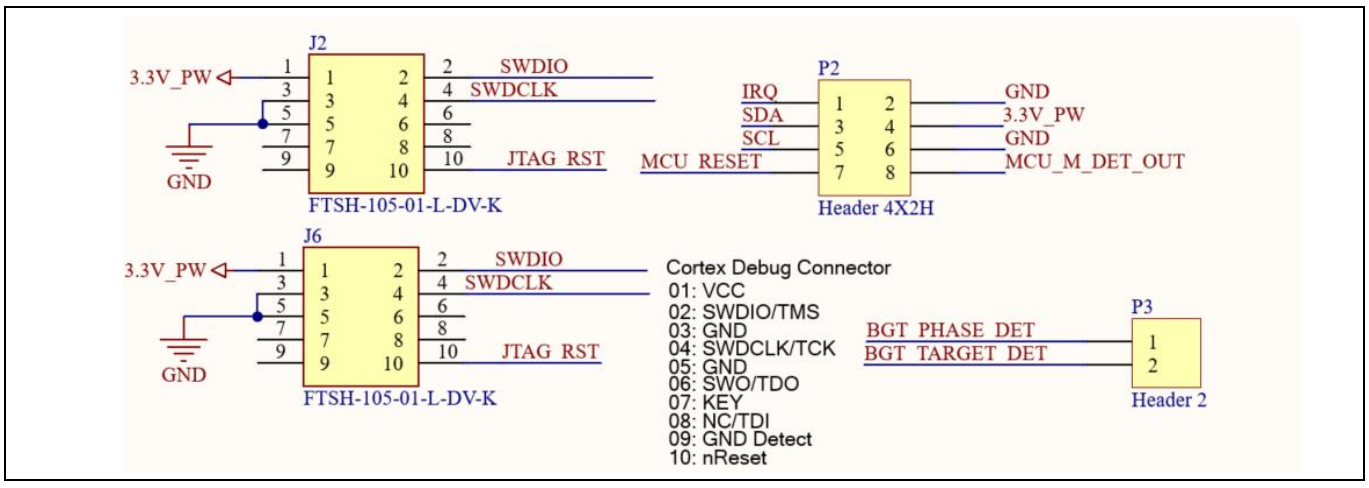


Figure 11 Connectors on the BGT60LTR11AIP M0 reference board, and their pinouts

3.8 LEDs

The board also has two LEDs, D1 and D2 as shown in Table 3 and Figure 12.

Table 3 LEDs on BGT60LTR11AIP M0 reference board

LED	Purpose
D1	User green LED connected to the I/O P1.2 of the XMC1302 MCU.
D2	User red LED connected to the I/O P1.1 of the XMC1302 MCU. By default, connected to MCU_M_DET_OUT signal to indicate the detection status of FFT Peak Algorithm running on MCU.

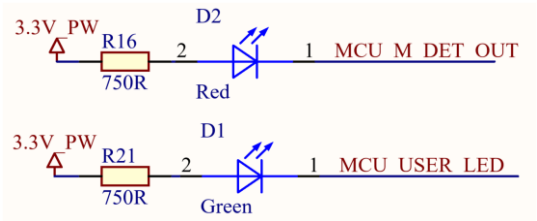


Figure 12 Connections of the LEDs

3.9 Level shifters

The outputs from MMIC are at the voltage level of 1.5 V. They are level-shifted to the voltage level of 3.3V by using the circuit shown in Figure 13.

BGT_MISO_1.5_A and IRQ signals at 1.5V are converted to SPI_MISO and BGT_DIV_TRIG_IN at 3.3V to interface with the MCU. SPI_SCK, SPI_MOSI, SPI_CS and BGT_RST_OUT are outputs of the MCU and are converted to corresponding 1.5V signals for the MMIC.

BGT_CS_1.5_A and BGT_RTSN_1.5_A should be pulled up with 10kΩ resistors for the correct operation of the MMIC.

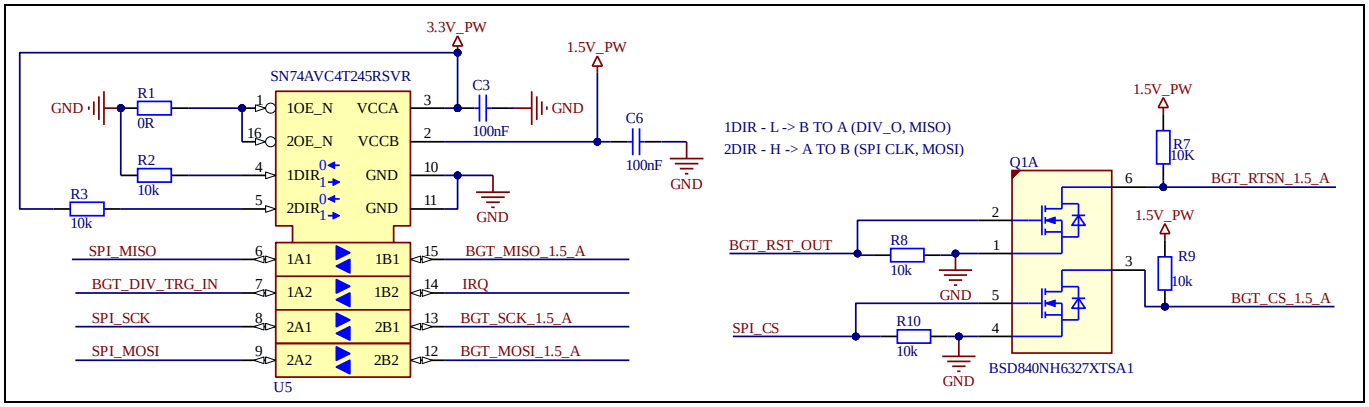


Figure 13 Connections of the level shifter

3.10 MMIC quad state inputs

The radar MMIC can be configured in both operation modes. In autonomous mode, the sensor configuration parameters are set via QS pins and external resistors. In SPI mode, the connection to a microcontroller allows setting the sensor configuration parameters by writing in the internal registers through SPI.
The BGT60LTR11AIP MMIC has four quad-state inputs QS1-4. Figure 14 shows the default settings of these QS pins on the board can be used as a reference to configure the board with different settings. The board is by default configured in SPI mode (QS1) to interface with the MCU.

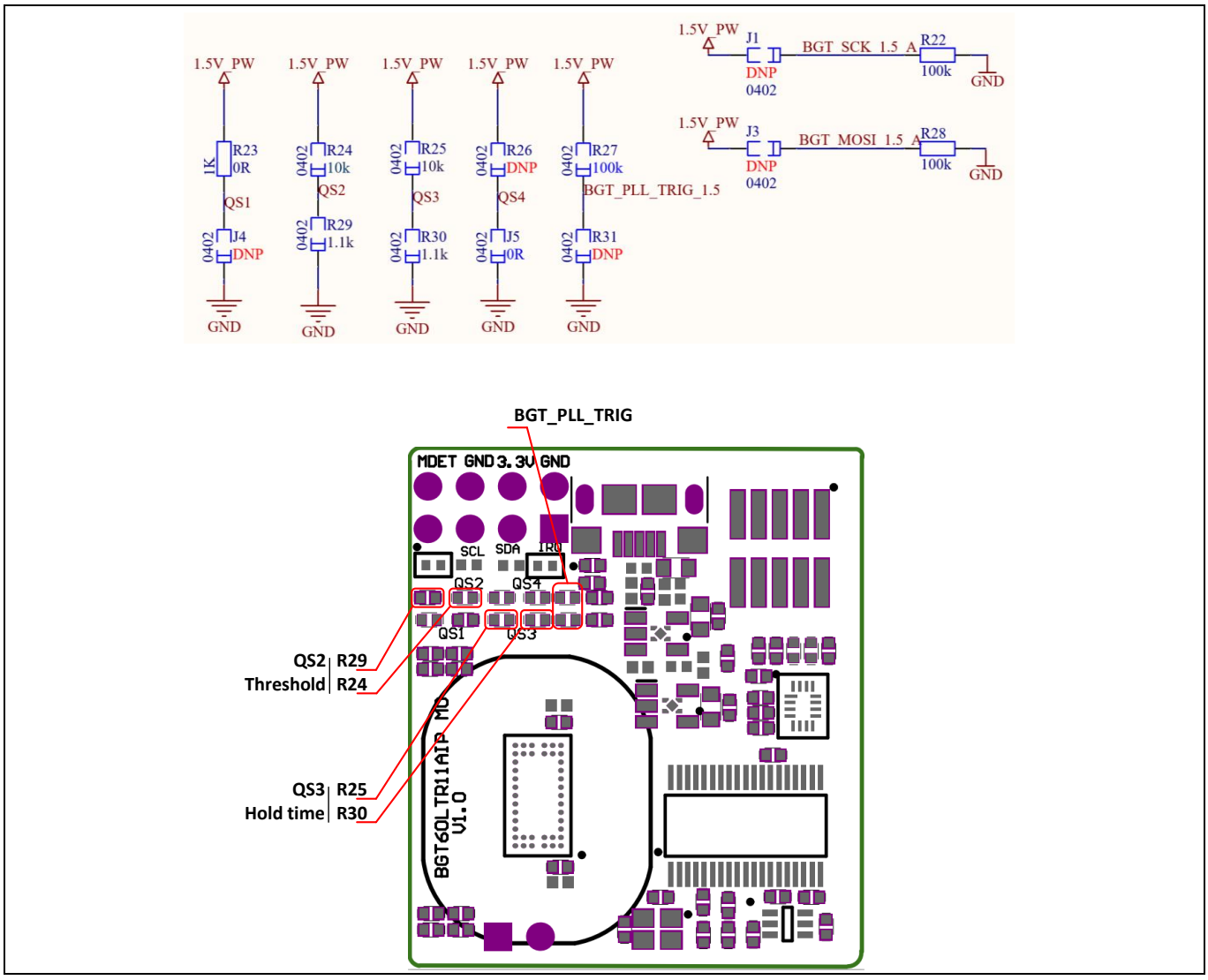
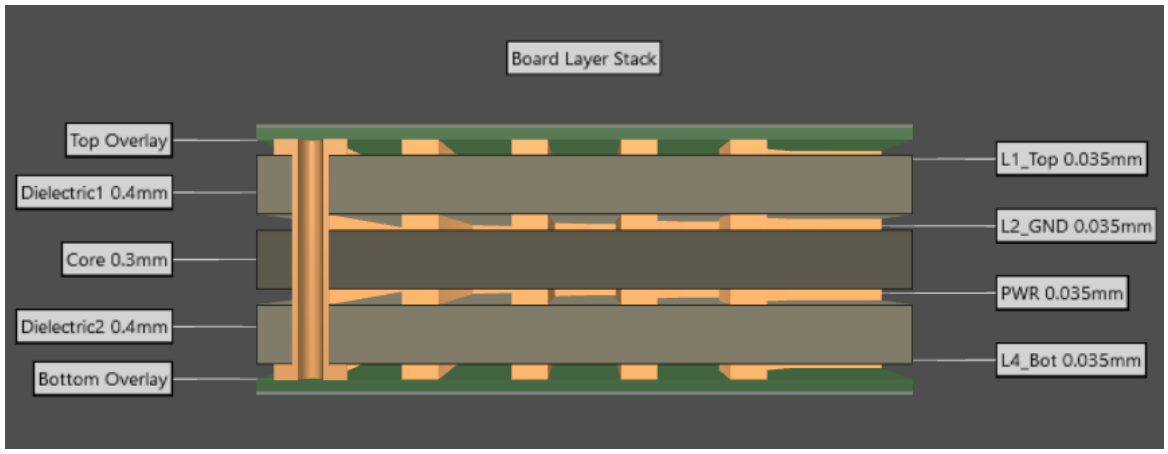


Figure 14 QS1 to QS4 schematic and layout connections

Note: The BGT60LTR11AIP M0 reference board only works in SPI mode. For autonomous mode, please refer to the BGT60LTR11AIP autonomous reference board (REF_BGT60LTR11AIP).

3.11 Layer-stack up and routing

The PCB is designed with a 4-layer stack up with standard FR4 material. Figure 15 shows the different layers and their thicknesses.



#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.02mm	3.5
1	L1_Top		Signal	1oz	0.035mm	
	Dielectric1	PP-006	Prepreg		0.4mm	4.1
2	L2_GND	CF-004	Signal	1oz	0.035mm	
	Core	FR-4	Core		0.3mm	4.2
3	PWR	CF-004	Signal	1oz	0.035mm	
	Dielectric2	PP-006	Prepreg		0.4mm	4.1
4	L4_Bot		Signal	1oz	0.035mm	
	Bottom Solder	Solder Resist	Solder Mask		0.02mm	3.5
	Bottom Overlay		Overlay			

Figure 15 QS1 to QS4 schematic and layout connections

In the routing on the PCB, the VTUNE pin on BGT60LTR11AIP MMIC should be left floating. Any components added to the line, or a long wire connected can result in spurs.

4 Radar MMIC settings configuration

In SPI mode, the radar sensor MMIC configuration parameters are, initially, set via QS pins and external resistors. With the FW running on a microcontroller allows overwriting or setting the sensor configuration parameters by writing in the internal registers through SPI.

4.1 Operation mode

The QS1 pin allows choosing the operation mode of the radar MMIC, as detailed in Table 4.

Table 4 QS1 settings

QS1	Operation mode of the MMIC	PCB configuration	
ground	Autonomous continuous wave (CW) mode	J4 = 0 Ω	R23 = DNP*
open	Autonomous pulsed mode	J4 = DNP*	R23 = DNP*
100 kΩ to V_{DD}	SPI mode with external 9.6 MHz clock enabled	J4 = DNP*	R23 = 100 kΩ
V_{DD} (default)	SPI mode	J4 = DNP*	R23 = 0 Ω

*DNP: Do Not Populate/Do Not Place

The BGT60LTR11AIP M0 reference board is originally configured for SPI mode applications.

4.2 Detector threshold

The internal detector threshold is the minimum signal strength that must be reached to trigger a detection event. The lower the threshold set, the higher the sensitivity and therefore also the detection range. In current FW running on the BGT60LTR11AIP M0 reference board, we also use two algorithms detection thresholds, that depend mainly on the defined algorithm, and not related to internal detector threshold.

4.3 Detector hold time

The internal detector hold time, is the time for which the internal detector outputs remain active after target detection.

In SPI operation mode, the user can set the internal detector hold time by writing to *hold* (Reg10[15:0]) bit fields of the MMIC SPI registers.

4.4 Operating frequency

In SPI operation mode, the user can set the device operation frequency by writing to *pll_fcw* (Reg5[11:0]) bit fields of the MMIC SPI registers. The BGT60LTR11AIP device operates in the frequency band from 61 GHz to 61.5 GHz.

4.5 Pulse repetition time

The Pulse Repetition Time (PRT) is the duty cycle repetition rate, which means the time until the next pulsing sequence starts in pulsed mode.

In SPI pulsed operation mode, the user can set the PRT value by writing to *dc_rep_rate* (Reg7[11:10]) bit fields of the MMIC SPI registers. The user can also enable the Adaptive Pulse Repetition Time (APRT) by writing to *aprt* (Reg2[6]) bit field of the MMIC SPI registers. The PRT multiplier factor, of 2, 4, 8 or 16, is also set by writing to *prt_mult* (Reg13[1:0]) bit fields.

5 Running radar algorithms

This section explains how to customize, build, Flash and debug radar applications built on generated DAVE™ code and run them on the 60 GHz radar BGT60LTR11AIP Cortex™-M0 based reference board.

With the BGT60LTR11AIP M0 reference board, Infineon offers two main algorithms to demonstrate the capabilities of the radar MMIC and to facilitate the development of user applications that can not only be used to detect motion and direction of movement but also mitigate interference when multiple radars are used.

Before using this reference board, as well as running the available algorithms, it is necessary to download the supporting software from Infineon.

5.1 Infineon Developer Center

In order to install and use Infineon plugins and tools, and be able to use the full functionalities of the 60 GHz radar, you must first download and install the Infineon developer Center (IDC). It is the one stop shop for engineers for downloading and design-in of all Infineon development tools, embedded software, services, and solutions.

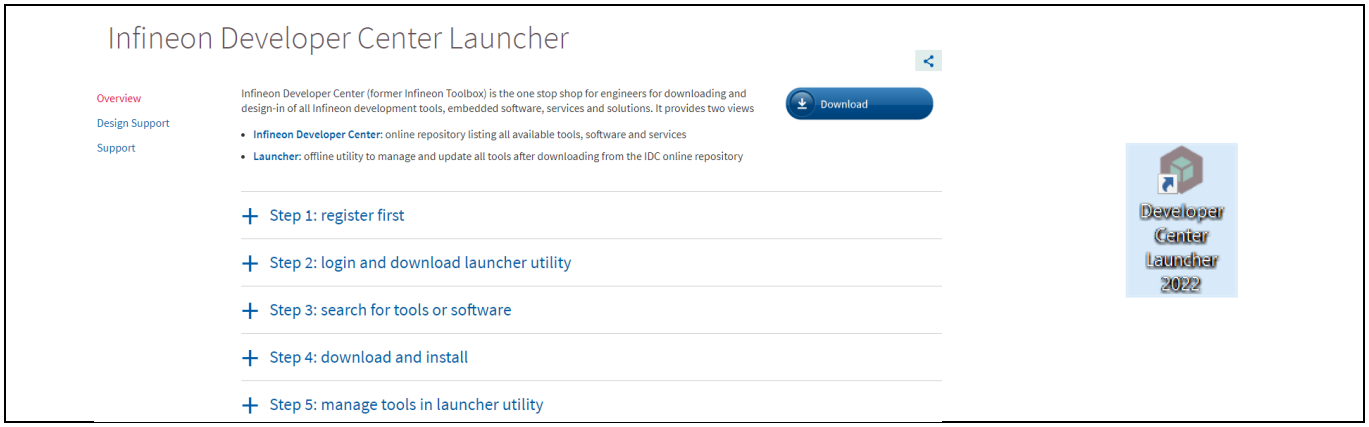


Figure 16 Download and run Infineon Developer Center launcher

5.2 XMC™ Flasher

The BGT60LTR11AIP M0 reference board firmware is already preloaded in the Flash memory on the XMC™ microcontroller. This section describes how to use the binary images provided to reprogram the firmware applications. In addition to XMC™ Flasher, DAVE™ IDE can also be used to modify, compile, and flash new firmware into the device, which is explained in section 7.1.3. The “Radar BGT60LTR11AIP” IDC package contains binary images (*.hex) of the applications provided in the subfolder **Binary**.

Figure 17 Connect the XMC™ Link Debug Probe

The XMC™ Flasher tool can be used for on-chip Flash programming to reprogram the radar board using a binary image, as follows:

- Connect the 60 GHz radar board to a PC with USB “type A to micro-B” cables through the embedded USB connector to power up the board. Two power supply options are available via USB (5V) or via one 3.3V pin.
- Connect the XMC™ Link debugger to your PC and connect the JTAG Debug connector to the board for flashing and debugging.
- Use (*.hex) binary with the XMC™ Flasher tool to reprogram the radar firmware:
  - Start the **XMC™ Flasher** tool in the Infineon Developer Center.

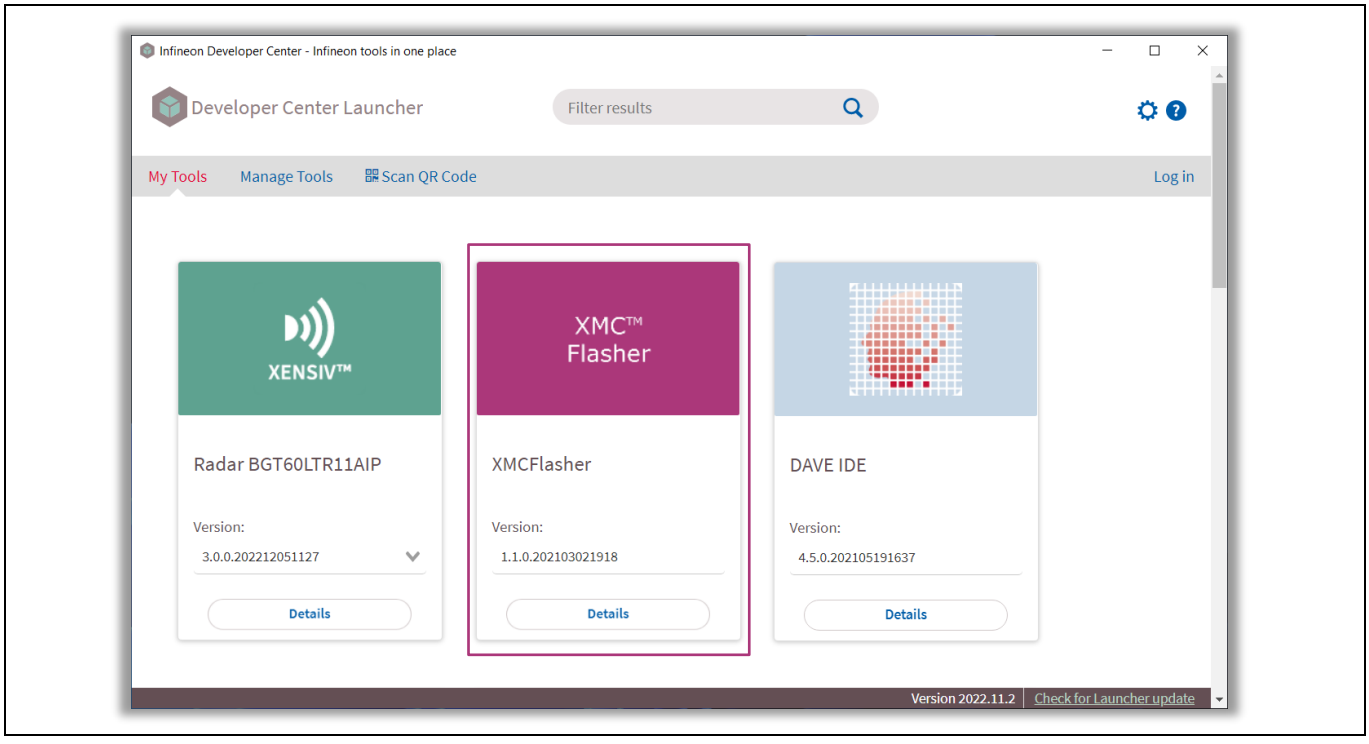


Figure 18 Start XMC™ Flasher tool via the Infineon Developer Center

  - Once started, click on the **Connect** button, then select the device name XMC1302-0200 and confirm with the **Ok** button.

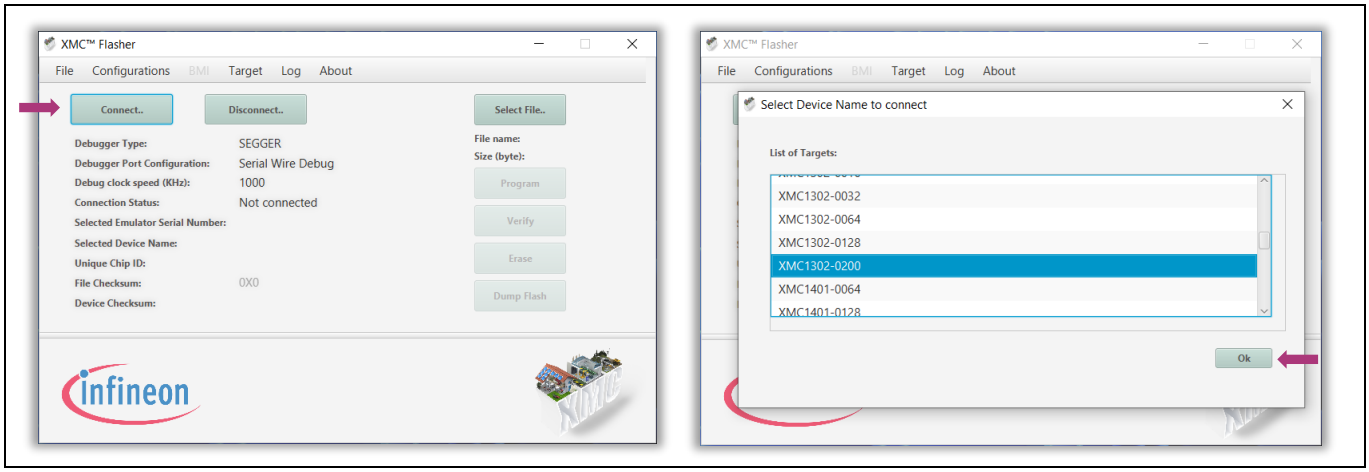


Figure 19 XMC™ Flasher device selection and connection

*Note: Please ensure that SEGGER J-Link drivers are installed before using the XMC™ Flasher tool. Otherwise, the default debugger type under XMC™ Flasher Target Interface Setup will be set to **DAP**, as shown in Figure 20a. Once installed, the user must change the debugger type to **SEGGER**, as shown in Figure 20b.*

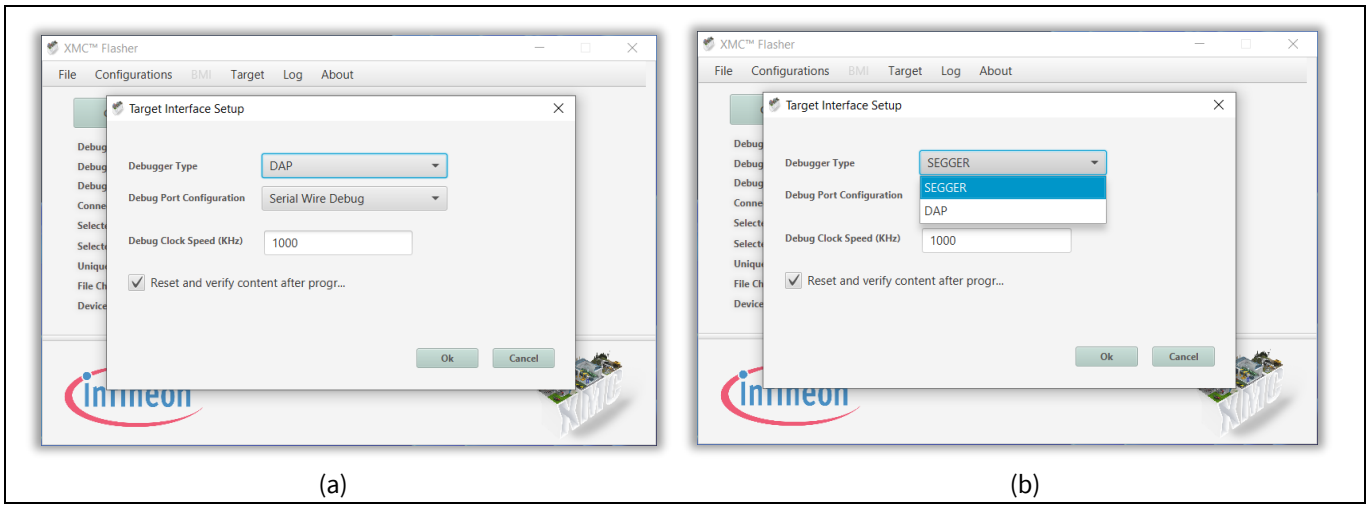


Figure 20 Change debugger type

- If the connection is established successfully, **Connection Status** turns to **Connected**. The **Unique Chip ID** is displayed as well.
- After connection is established, select the (*.hex) file by clicking on the **Select File…** button.

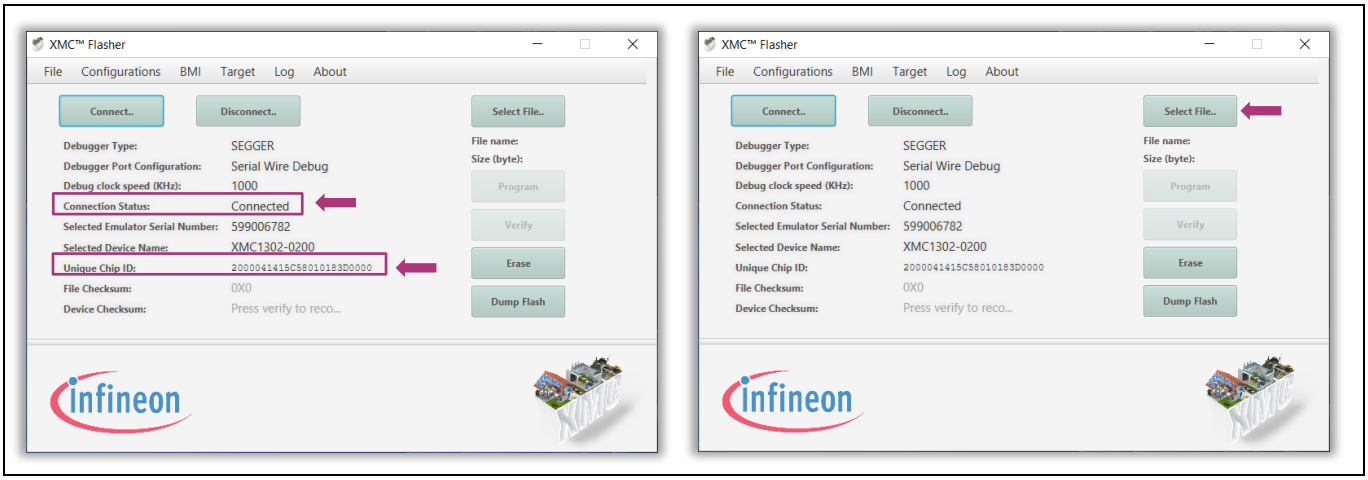


Figure 21 Binary image file selection

- Navigate to the **Binary** folder and select the (*.hex) file inside it (REF_BGT60LTR11AIP_M0_FW.hex), then click on **Open** in the dialog box.
- Successful selection of the (*.hex) file results in listing its filename below the **Select File…** button.

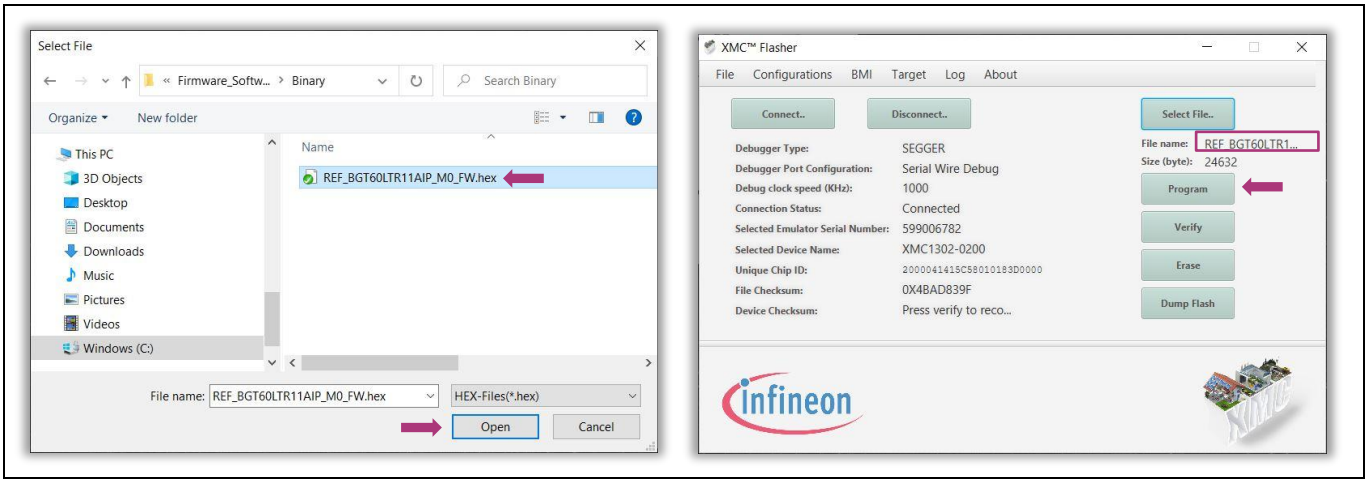


Figure 22 Binary image programming

- Click on the **Program** button, which opens the SEGGER progress window. It either verifies successful Flashing or shows an error message.
- If programming succeeds, the message **Programming is successful!** appears.

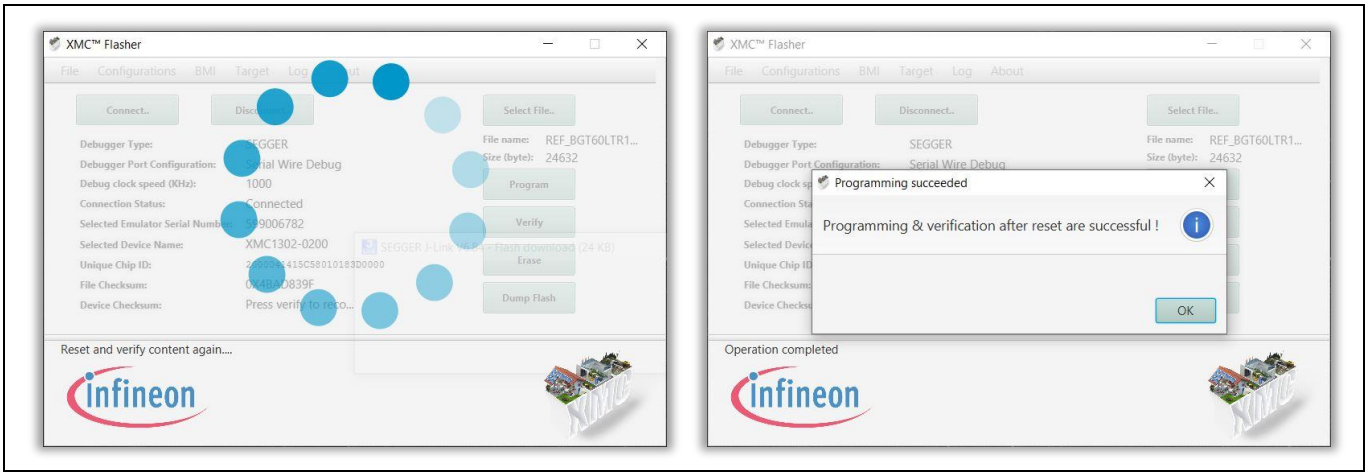


Figure 23 Programming successful

5.3 Graphical User Interface (GUI)

µC/Probe™ XMC™ from Micrium® is a free-of-charge data monitoring and visualization tool to modify and track real-time data on the XMC™ target microcontroller in a non-intrusive way.

It enables designing a graphical dashboard with a wide range of widgets to control or fine-tune your XMC™ application, and it includes an eight-channel digital oscilloscope to visualize real-time data, controlled by a dedicated code that runs on the XMC™ target.

µC/Probe™ XMC™ is simple to install on a Windows PC and can be easily connected via the J-Link onboard debugger integrated into most of the XMC™ kits.

The latest version of µC/Probe™ XMC™ v4.3.0.9 is available for download from Infineon website.

Note: The BGT60LTR11AIP M0 reference board is only supported by the Micrium-based GUI tool.

The software package comes with a GUI based on a µC/Probe™ project from Micrium, which helps the user process collected raw data.

Here below an example, on how to run this Micrium-based GUI project, for the Sense2GoL device:

- Go to the **/Firmware_Software/GUI** folder inside the locally installed package.
- Double-click the µC/Probe™ **REF_BGT60LTR11AIP_M0_GUI.wspx** project, to open the GUI.

The µC/Probe™ needs to be provided by the XMC™ compiling and linking process output file (ELF file). This file containing the name, data type and address of all firmware global variables is parsed by the µC/Probe™ project.

A precompiled .elf file is already available in a **/Firmware_Software/GUI** folder called **REF_BGT60LTR11AIP_M0_FW.elf**.

*Note: After building a project, object files and an application binary file (typically in ELF format) exist in the Debug folder in the Project Explorer view file tree. Please ensure you have imported the **.elf** file into your Micrium-based GUI project each time you modify and build your DAVE™ project.*

Once the GUI project has opened, the following steps need to be executed:

- Start the GUI by clicking on the **Run** button.

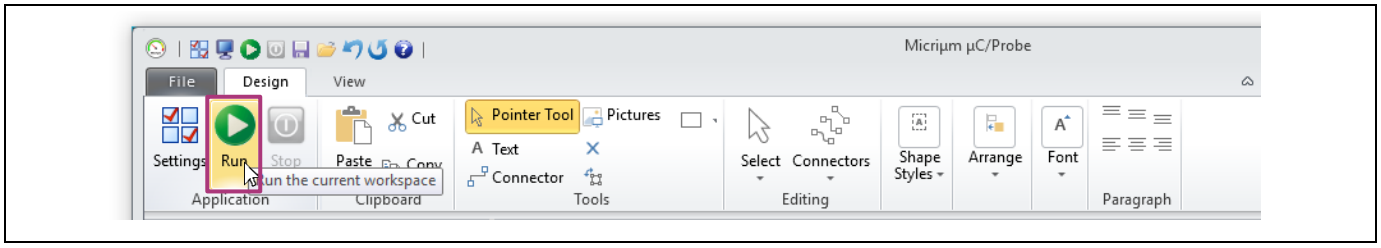


Figure 24 Run the REF_BGT60LTR11AIP_M0_GUI

- The GUI interface in Figure 25 should appear.

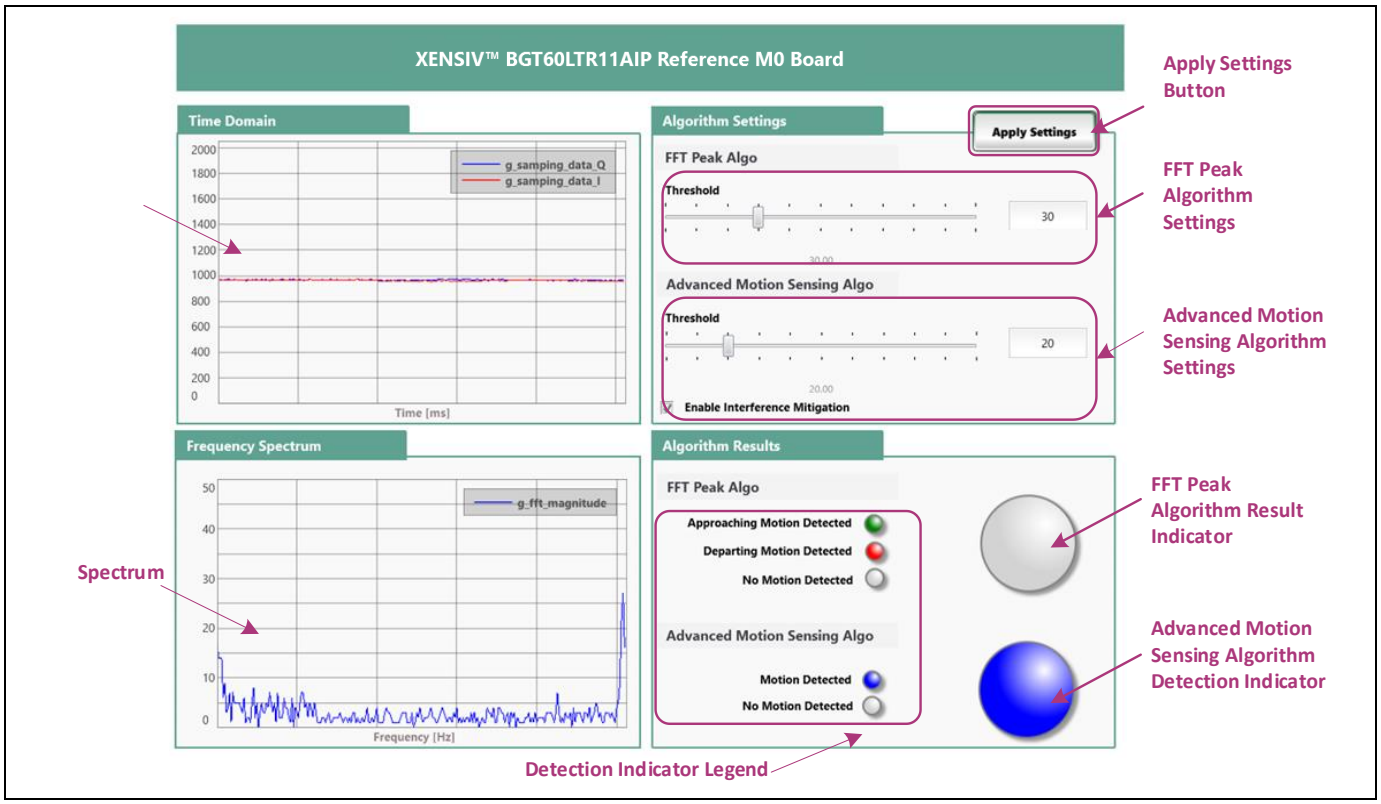


Figure 25 Data display on Micrium-based GUI

The radar should now detect movement and display the following data on the GUI:

- Time and frequency plots
- Algorithm settings (e.g., detection threshold, enable/disable interference mitigation)
- Algorithm results (e.g., detection status, direction of movement)

- If you change the any of the algorithm's parameters, press the **Apply Settings** button.

Figure 26 Apply Settings

6 Firmware description

6.1 DAVE™ IDE

DAVE™ (Digital Application Virtual Engineer), is a free-of-charge Eclipse-based Integrated Development Environment (IDE) using a GNU C-compiler that provides an extensive, configurable, and reusable code repository for an XMC™ industrial microcontroller powered by ARM® Cortex®-M processors.

It is a C/C++-language software development and code generation tool for XMC™ microcontroller applications using DAVE™ APPs to configure the MCU peripherals (ADC, DMA, CCU4…), which reduces development time and allows for quick porting of the firmware across XMC™-series MCUs.

DAVE™ v4.4.2 or higher should be installed. The latest version of DAVE™ IDE can be downloaded from the Infineon Developer Center (IDC).

6.2 Firmware project overview

The radar firmware is released as a ready-to-run DAVE™4 project, where source files are generated based on the DAVE™ APPs used, which are graphical-configurable application-oriented software components, used to enable quick reuse and customization. Figure 22 shows a top-level view of the project file structure.

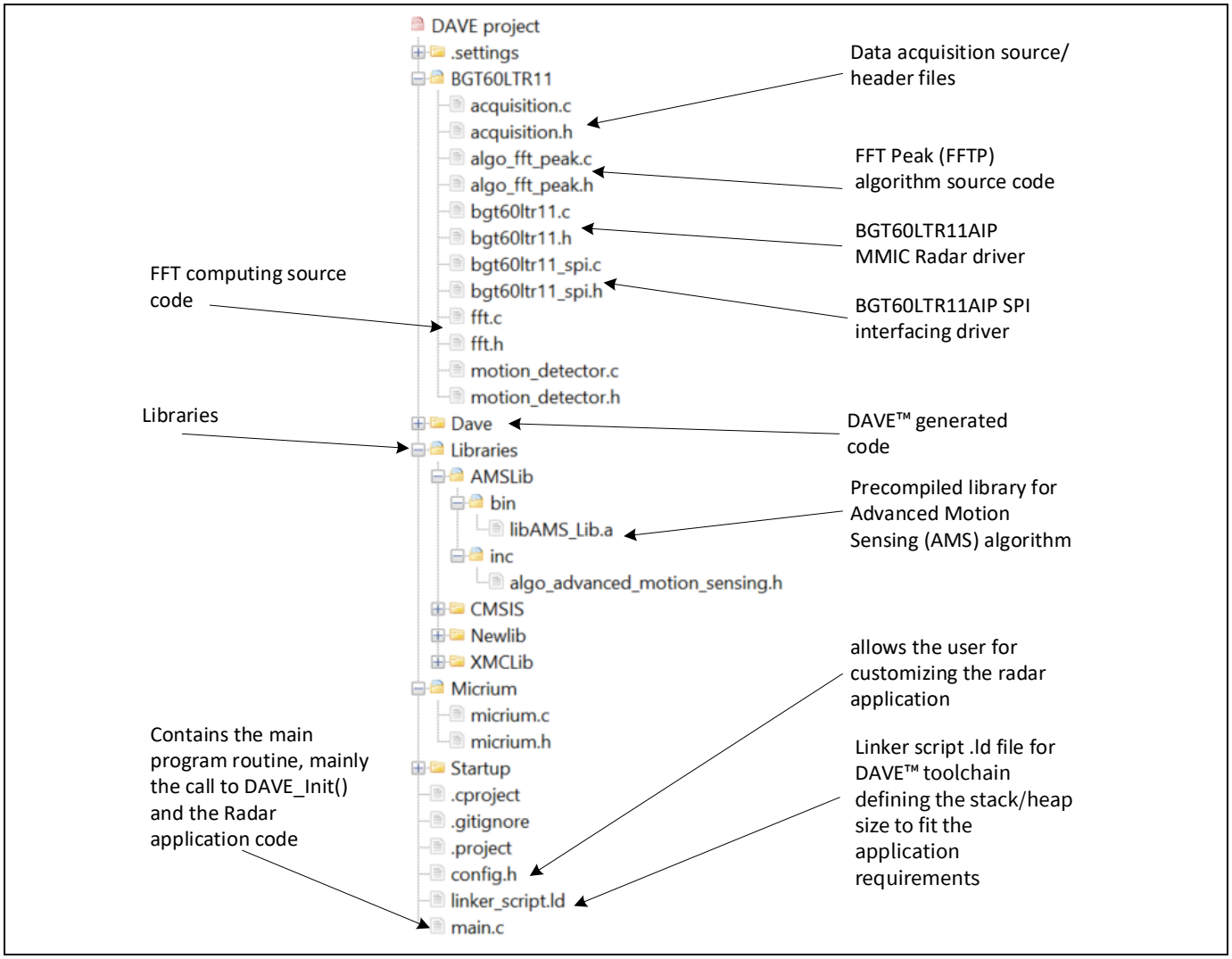


Figure 27 Package folder structure

6.3 Footprint

The purpose of the following sections is to provide the memory requirements for all the firmware modules, including devices' drivers, algorithms, and main radar applications. The aim is to have an estimation of fixed and customizable memory requirements in case of removal or addition of a module or feature. The footprint data are provided for the following environment:

- Board – REF_BGT60LTR11AIP_M0 (v1.0)
- Firmware – REF_BGT60LTR11AIP_M0_FW
- Toolchain – DAVE™ v4.4.2

After building a project, the build result is displayed in the console window, where the code size figures are listed. The values are organized according to memory areas, arranged by the linker file (*.ld) into the text, data and bss sections. Table 5 shows the build memory utilization for the radar firmware configurations, main modules, and algorithms. The information has been gathered by analyzing the corresponding (*.elf) file.

Table 5 Firmware footprint

DAVE project	Optimization	text[(1)] [byte]	data [byte]	bss[(2)] [byte]	Total [byte]
REF_BGT60LTR11AIP_M0_FW	Optimize (-O1)	24472	148	6428	31048 byte (0x7948)

(1) text: code.

(2) bss: statically allocated variables that are not explicitly initialized to any value.

6.4 Firmware customization and configuration

The configuration files allow for customizing the drivers (***config.h***) and algorithms (***algo_fft_peak.h/algo_advanced_motion_sensing.h)*** for the radar application. The following parameters can be configured by modifying the values of the related define statements, as described in Table 6.

Table 6 Define statements used for radar firmware configuration

Parameter	Description	Default	Valid range
General configurations			
FRAME_INTERVAL_TIME_MS	Time period between two consecutive frames (units in ms)	300	
SAMPLING_FREQ_HZ	Sampling frequency (units in Hz)	2000	
FFT Peak algorithm configurations			
THRESHOLD_FFT_PEAK	Minimum threshold value to trigger a detection event	30	[30 to ...]
BIN_NUMBER_START	Minimum bin number to consider for peak search	3	[0 to 255]
BIN_NUMBER_END	Maximum bin number to consider for peak search	253	[0 to 255]
Advanced Motion Sensing algorithm configurations			
THRESHOLD_AMS	Minimum threshold value to trigger a detection event	30	[30 to ...]

7 Simulation results

To analyze the sensor radiation characteristics, the radiation pattern of BGT60LTR11AIP M0 reference board is simulated along the H-plane and E-plane of the sensor.

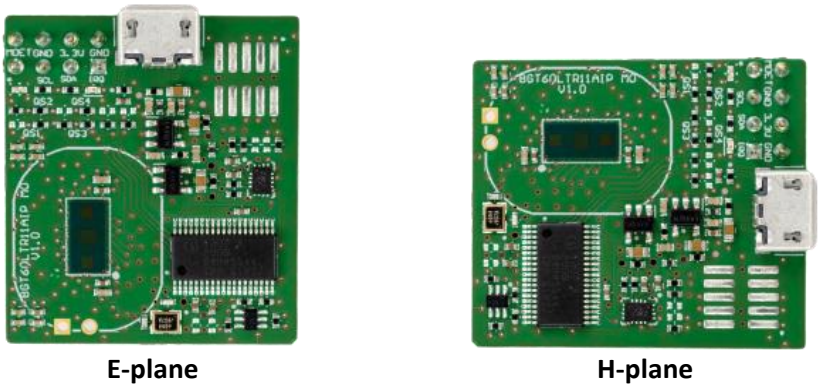
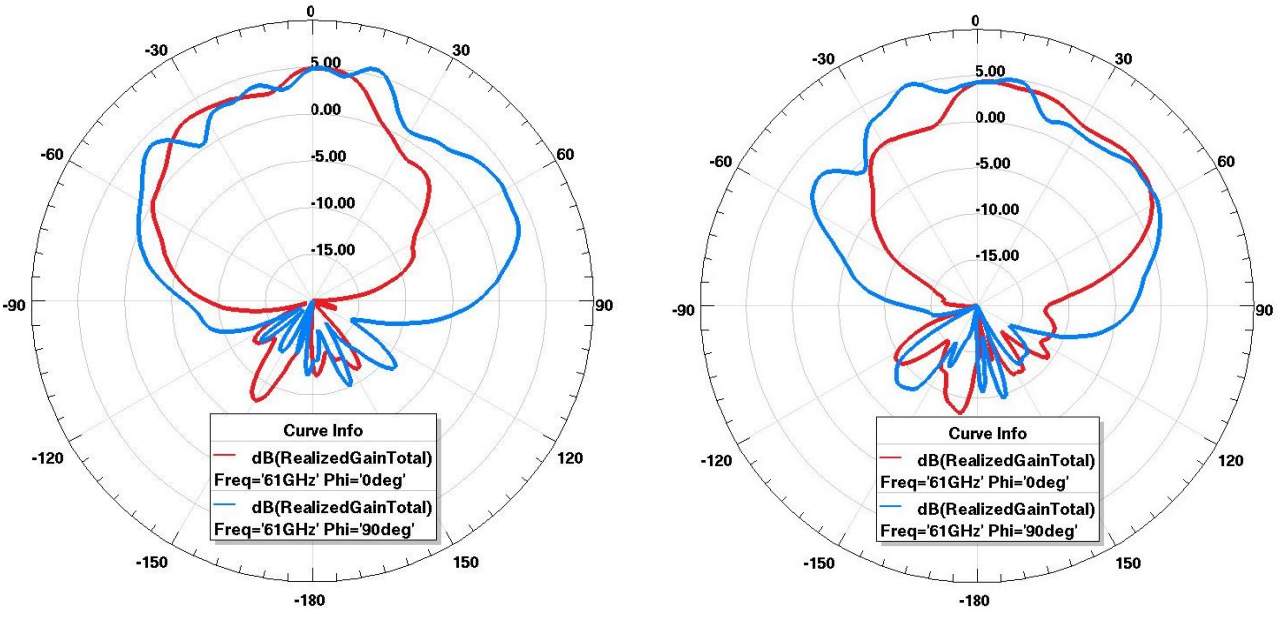


Figure 28 E-plane and H-plane orientations of the BGT60LTR11AIP M0 reference board

The realized gain of the transmitting antenna, in H-plane and E-plane at a frequency of 61 GHz, is shown in Figure 29a. The antenna characteristics of the receiving antenna in H-plane and E-plane at a frequency of 61 GHz, is illustrated in Figure 29b.



a) TX – H/E plane at f = 61 GHz b) RX – H/E plane at f = 61 GHz

Figure 29 Radiation pattern simulations of the BGT60LTR11AIP M0 reference board

8 Measurement results

8.1 FFT Peak algorithm

- **Scenario**
  Measure the max. detection range of a human target along the H-plane and E-plane of the sensor for different angles, with the default configuration, and with an algorithm set threshold value of 30, which can be selected from the Micrium-based GUI.
- **Height**: Board is placed at 1.2 m
- **Detection status**
  is driven from the FFT peak detection algorithm running on the embedded microcontroller of the BGT60LTR11AIP M0 reference board. Figure 30 shows the measurement results in H- and E-plane.

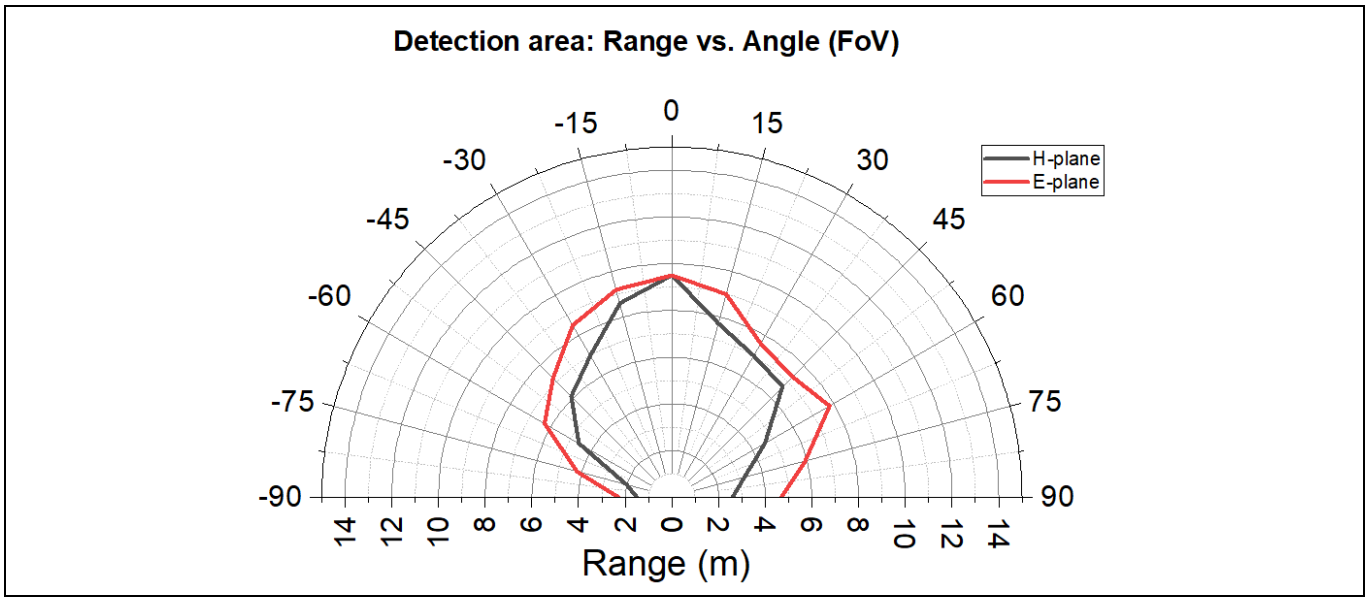


Figure 30 Detection area of FFT Peak algorithm

8.2 Advanced Motion Sensing algorithm

- **Scenario**
  Measure the max. detection range of a human target along the H-plane and E-plane of the sensor for different angles, with the default configuration, and with an algorithm set threshold value of 40, which can be selected from the Micrium-based GUI.
- **Interference mitigation**: Disabled
- **Height**: Board is placed at 1.2 m
- **Detection status**
  is driven from the advanced motion detection algorithm running on the embedded microcontroller of the BGT60LTR11AIP M0 reference board. Figure 30 shows the measurement results in H- and E-plane.

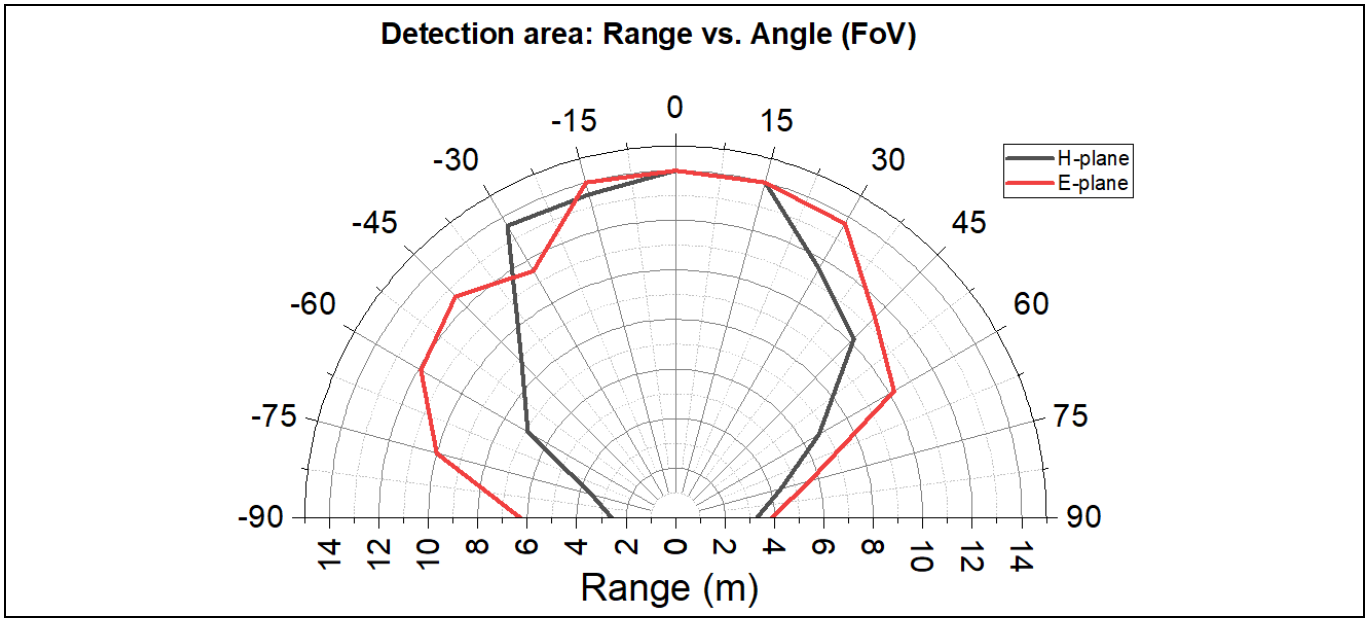


Figure 31 Detection area of Motion Sensing algorithm

References

[1] Infineon Technologies AG. BGT60LTR11AIP MMIC Datasheet

[2] Infineon Technologies AG. AN625: User's guide to BGT60LTR11AIP

Revision history

Document revision	Date	Description of changes
1.00	2023-02-14	Initial version

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