1ED21x7x Family Datasheet

650 V high-side gate driver with over current protection (OCP), multi-function RCIN/Fault/Enable (RFE) and integrated bootstrap diode (BSD)

Features

- Infineon thin-film-SOI-technology
- Maximum blocking voltage +650 V
- Output source/sink current +4 A/ -4 A
- Maximum supply voltage of 25 V
- Integrated ultra-fast, low $R_{DS(ON)}$ Bootstrap Diode
- Negative VS transient immunity of 100 V
- Detection of over current and under voltage supply
- Multi-function RCIN/Fault/Enable (RFE) with programmable fault clear time
- Less than 100 ns propagation delay
- DSO-8 package
- RoHS compliant

Product summary

V_{S_OFFSET}	= 650 V max.
$I_{O+/-}$ (typ.)	= +4 A / -4 A
t_{ON} / t_{OFF} (typ.)	= 55 ns / 55 ns
t_R / t_F (typ.)	= 12 ns / 12 ns

Package

PG-DSO-8

Potential applications

- Motor drives, general purpose inverters
- Forklift
- Light electric vehicles

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

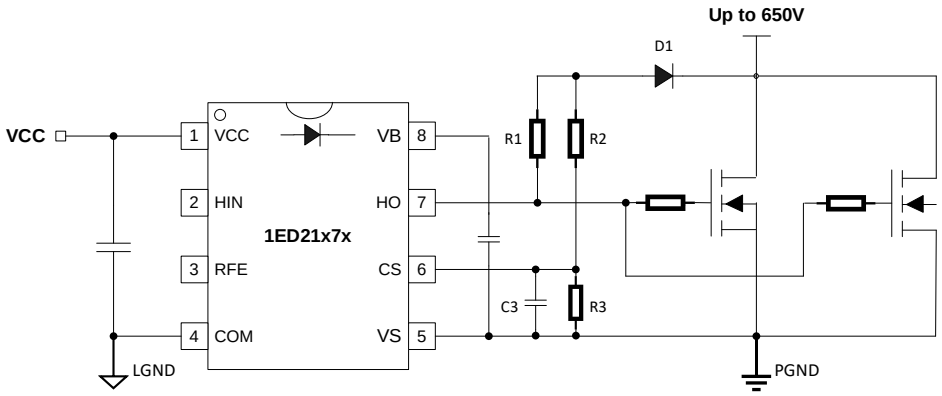
Ordering information

Table 1 Order information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
1ED2127S65F	PG-DSO-8	Tape and Reel	2500	1ED2127S65FXUMA1
1ED21271S65F	PG-DSO-8	Tape and Reel	2500	1ED21271S65FXUMA1
1ED2147S65F	PG-DSO-8	Tape and Reel	2500	1ED2147S65FXUMA1
1ED21471S65F	PG-DSO-8	Tape and Reel	2500	1ED21471S65FXUMA1

Description

The 1ED21x7x family are high voltage, high current and high speed gate drivers for Si / SiC power MOSFET and IGBT. The floating channel can be used to drive an Si / SiC power MOSFET or IGBT in the high-side or low-side configuration which operates up to 650 V, with output current of +/-4 A and propagation delay of less than 100 ns.
Based on Infineon's SOI-technology there is an excellent ruggedness and noise immunity with capability to maintain operational logic at negative transient voltages up to -100 V.
The over-current protection and under-voltage lockout circuity detects over-current / under-voltage in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred.



*Bootstrap diode is monolithically integrated.

Figure 1 Typical application diagram

Summary of feature comparison of the 1ED21x7x family:

Table 2 Members of 1ED21x7x family

Base part number	Target transistor	Typ. UVLO-Thresholds	Typ. CS Thresholds	Package
1ED2127S65F	IGBT / SiC MOSFET	10.0 V / 8.7 V	0.24 V	PG-DSO-8
1ED21271S65F	Si MOSFET	7.2 V / 6.8 V	1.78 V	PG-DSO-8
1ED2147S65F	Si MOSFET	7.2 V / 6.8 V	0.24 V	PG-DSO-8
1ED21471S65F	IGBT / SiC MOSFET	10.0 V / 8.7 V	1.78 V	PG-DSO-8

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1 Block diagram

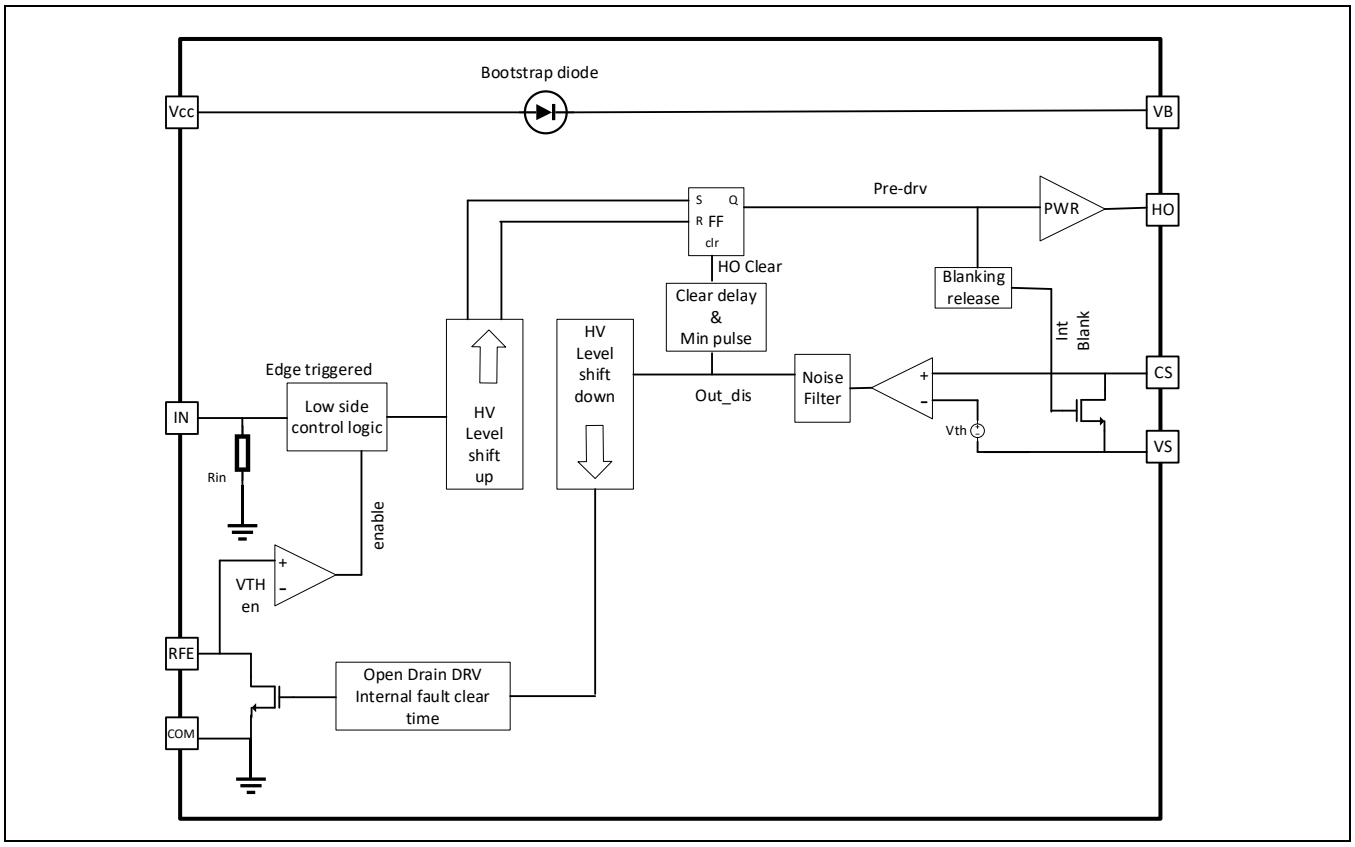


Figure 2 Functional block diagram for 1ED21x71 family

2 Pin configuration and functionality

2.1 Pin configuration

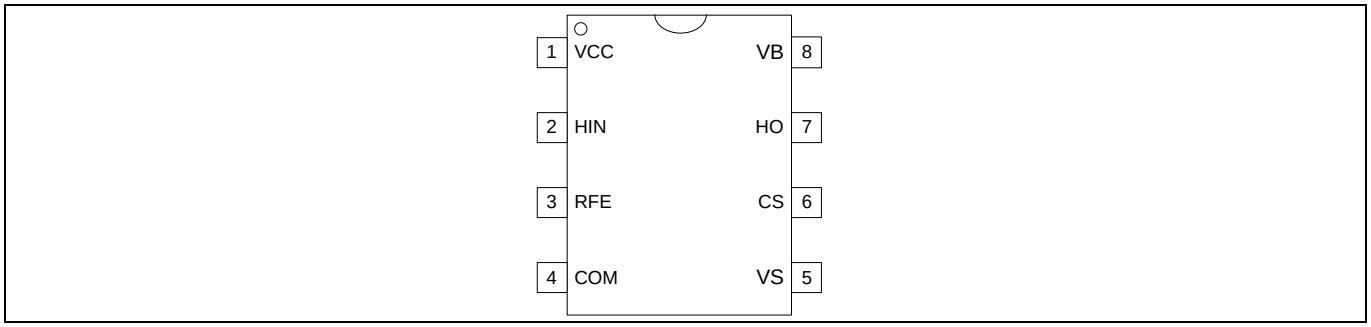


Figure 3 1ED21x7x family pin assignments (top view)

2.2 Pin functionality

Table 3 1ED21x7x family lead definitions

Pin no.	Name	Function
1	VCC	Low-side and logic supply voltage
2	HIN	High-side logic input, in phase with HO
3	RFE	Multi-function pin 1) for logic input to enable I/O functionality, 2) fault reporting of high-side over-current, and 3) programmable fault clear timer with external R/C components.
4	COM	Low-side gate drive return
5	VS	High-side negative power supply
6	CS	Current sense input for over current protection
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. All parameters are valid for T_A = 25°C. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 4 Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
High-side floating well supply voltage	V_B	-0.3	675	V
High-side floating well supply return voltage	V_S	-0.3	650	
High-side floating well supply voltage (V_B vs. V_S)	V_{BS}	-0.3	25	
Floating gate drive output voltage	V_{HO}	V_S - 0.3	V_B + 0.3	
Low side supply voltage	V_{CC}	-0.3	25	
Logic I/O voltage (HIN / RFE)	$V_{LOGIC IO}$	-0.3	6.5	
Floating CS Voltage	V_{CS}	V_S - 0.3	V_S + 6.5	
Allowable VS offset supply transient relative to COM	dV_S/dt	–	50	V/ns
Package power dissipation @ TA @+25°C	P_D	–	0.625	W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	–	200	°C/W
Junction temperature	T_J	–	150	°C
Storage temperature	T_S	-55	150	
Lead temperature (soldering, 10 seconds)	T_L	–	260	

3.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. All parameters are valid for T_A = 25 °C. The offset rating is tested with supplies of (V_{CC} – COM) = (V_B – V_S) = 15 V.

Table 5 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
High-side floating well supply voltage	V_B	V_S + $V_{BSUVLO+}$	672	V
High-side floating well supply offset voltage	V_S	0	650	
High-side floating well supply voltage (V_B vs. V_S)	V_{BS}	$V_{BSUVLO+}$	22	
Floating gate drive output voltage	V_{HO}	V_S	V_B	
Low-side supply voltage	V_{CC}	$V_{CCUVLO+}$	*22*	
Logic I/O voltage (HIN / RFE)	$V_{LOGIC IO}$	0	5	
Floating CS Voltage	V_{CS}	V_S	V_S + 5	
Ambient temperature	T_A	-40	125	°C

3.3 Static parameters

(V_{CC}– COM) = (V_B – V_S) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the input lead HIN. The V_O and I_O parameters are referenced to V_S and are applicable to the respective output leads HO. The V_{BSUV} parameters are referenced to V_S.

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
V_{BS} supply undervoltage positive going threshold	1ED2127 1ED21471	$V_{BSUVLO+}$	9.2	10.0	10.8	V	
	1ED21271 1ED2147		6.6	7.2	8.0		
V_{BS} supply undervoltage negative going threshold	1ED2127 1ED21471	$V_{BSUVLO-}$	8.0	8.7	9.4	V	
	1ED21271 1ED2147		6.2	6.8	7.4		
V_{CC} supply undervoltage positive going threshold	1ED2127 1ED21471	$V_{CCUVLO+}$	9.2	10.0	10.8	V	
	1ED21271 1ED2147		6.6	7.2	8.0		
V_{CC} supply undervoltage negative going threshold	1ED2127 1ED21471	$V_{CCUVLO-}$	8.0	8.7	9.4	V	
	1ED21271 1ED2147		6.2	6.8	7.4		
High-side floating well offset supply leakage		I_{LK}	-	-	5	µA	V_B = V_S = 650 V
V_{BS} quiescent supply current		I_{QBS}	-	270	350	µA	
V_{CC} quiescent supply current		I_{QCC}	-	270	400	µA	
High level output voltage drop		V_{OH}	-	0.46	-	V	I_O = 300 mA
Low level output voltage drop		V_{OL}	-	0.26	-	V	I_O = 300 mA
Peak output current turn-on		I_{O+}[1]	-	4	-	A	t_p<10 µs
Peak output current turn-off		I_{O-}[1]	-	4	-	A	t_p<10 µs
Logic “1” input voltage		V_{IH}	2.4	-	-	V	For HIN and RFE
RFE input positive going threshold		$V_{IH,RFE}$	-	2.1	-		
Logic “0” input voltage		V_{IL}	-	-	0.8		For HIN and RFE
Input bias current (Output = high)		$I_{LOGIC\ IN+}$	-	25	50	µA	V_{IN} = 4 V
Input bias current (Output = Low)		$I_{LOGIC\ IN-}$	-	-	1		V_{IN} = 0 V
Bootstrap diode forward voltage between V_{CC} and V_B		V_{FBSD}	0.6	0.91	1.1	V	I_F = 0.3 mA
Bootstrap diode forward current between V_{CC} and V_B		I_{FBSD}	40	71	-	mA	V_F = 4 V
Bootstrap diode resistance		R_{BSD}	-	35	50	Ω	V_{F1} = 4 V, V_{F2} = 5 V

[1] Parameter not subject to production test. Verified by characterisation.

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
CS input positive going threshold	1ED2127 1ED2147	V_{CSTH+}	220	240	260	mV	V_{HIN} = 4 V, HO on
	1ED21271 1ED21471		1.69	1.78	1.87	V	
CS input open drain Rdson		$R_{on, CS}$	-	20	-	Ω	I = 20 mA
RFE open drain Rdson		$R_{on, RFE}$	-	50	-	Ω	I = 2 mA

3.4 Dynamic parameters

(V_{CC}– COM) = (V_B – V_S) = 15 V, T_A = 25 °C and C_L = 2.2 nF unless otherwise specified.

Table 7 Dynamic parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Turn-on propagation delay	t_{ON}	-	55	80	ns	IN 50% rise to OUT 10% rise
Turn-off propagation delay	t_{OFF}	-	55	80		IN 50% fall to OUT 90% fall
Turn-on rise time	t_R	-	12	-	ns	OUT 10% to 90%
Turn-off fall time	t_F	-	12	-		OUT 90% to 10%
VBS UVLO glitches filter time	$t_{FIL, UVBS}$	-	1	-	µs	
CS shutdown propagation delay	t_{CS}	250	330	410	ns	V_{CS} > V_{CSTH+} to OUT 90% fall
CS to RFE propagation delay	t_{FLT}	-	450	800	ns	V_{CS} > V_{CSTH+} to RFE low
CS input filter	$t_{FIL, CS}$	135	170	-	ns	CS = 3.3 V for 1.8 V threshold CS = 1 V for 250 mV threshold
RFE low to shutdown propagation delay	t_{SD}	-	60	85	ns	V_{RFE} < $V_{IL,RFE}$ to OUT 90% fall
Fault clear time	t_{FLTC}	-	112	-	µs	V_{DD} = 3.3 V R_{FLTC} = 1 MΩ to V_{DD} C_{FLTC} = 75 pF to COM RFE: falling 1.65 V to rising 2.1 V
Internal Fault clear time	$t_{FLTC, INT}$	-	10	-	µs	V_{DD} = 3.3 V R_{FLTC} = 1 MΩ to V_{DD} No C_{FLTC} to COM RFE: falling 1.65 V to rising 0.33 V

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Internal CS Blanking Time	$t_{BL, INT}$	170	260	350	ns	HO rising to CS release

4 Application information and additional details

4.1 Si / SiC MOSFET and IGBT gate drive

The 1ED21x7x HVIC is designed to drive Si / SiC MOSFET or IGBT power devices. Figure 6Figure 4 and Figure 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch.

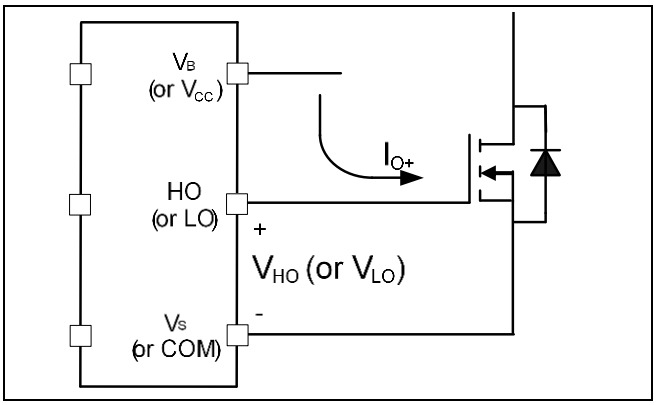


Figure 4 HVIC sourcing current

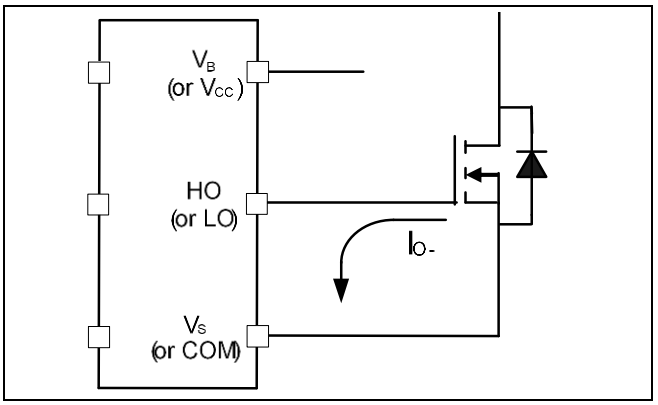


Figure 5 HVIC sinking current

4.2 Edge triggered input logic

The high side power output (HO) is specifically designed for pulse operation such as gate drive for IGBT and Si / SiC MOSFET devices. It is edge triggered by input pin (HIN). In particular, after an undervoltage condition of the VBS or VCC supply, a new turn-on signal (edge) is necessary to activate the high side output.

4.3 Over-current protection

The 1ED21x7x is equipped with an over-current protection feature (CS input pin). Once the HVIC detects an over-current event with de-sat detection circuit as shown in Figure 6, the output will be shutdown, and RFE is pulled to COM.

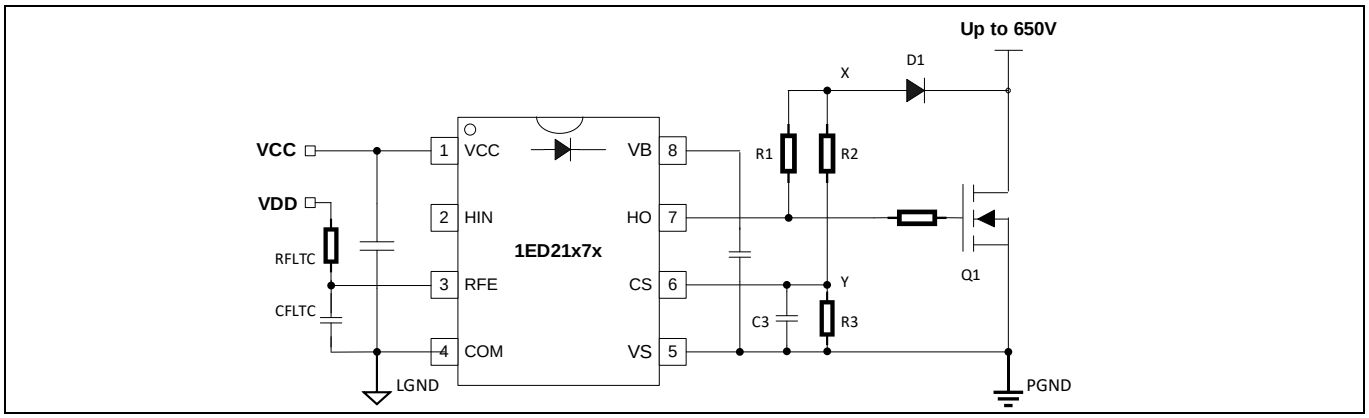


Figure 6 Over-current protection with de-sat detection circuit

The de-sat detection circuit can be used for both short circuit and over-current protection. The overall timing diagram is illustrated in Figure 7. For detailed explanation on this timing diagram, as well as instructions on how to select the resistor (R_1 / R_2 / R_3) and capacitor (C_3) values in de-sat detection circuit, please refer to "1ED21x7x family Application Note".

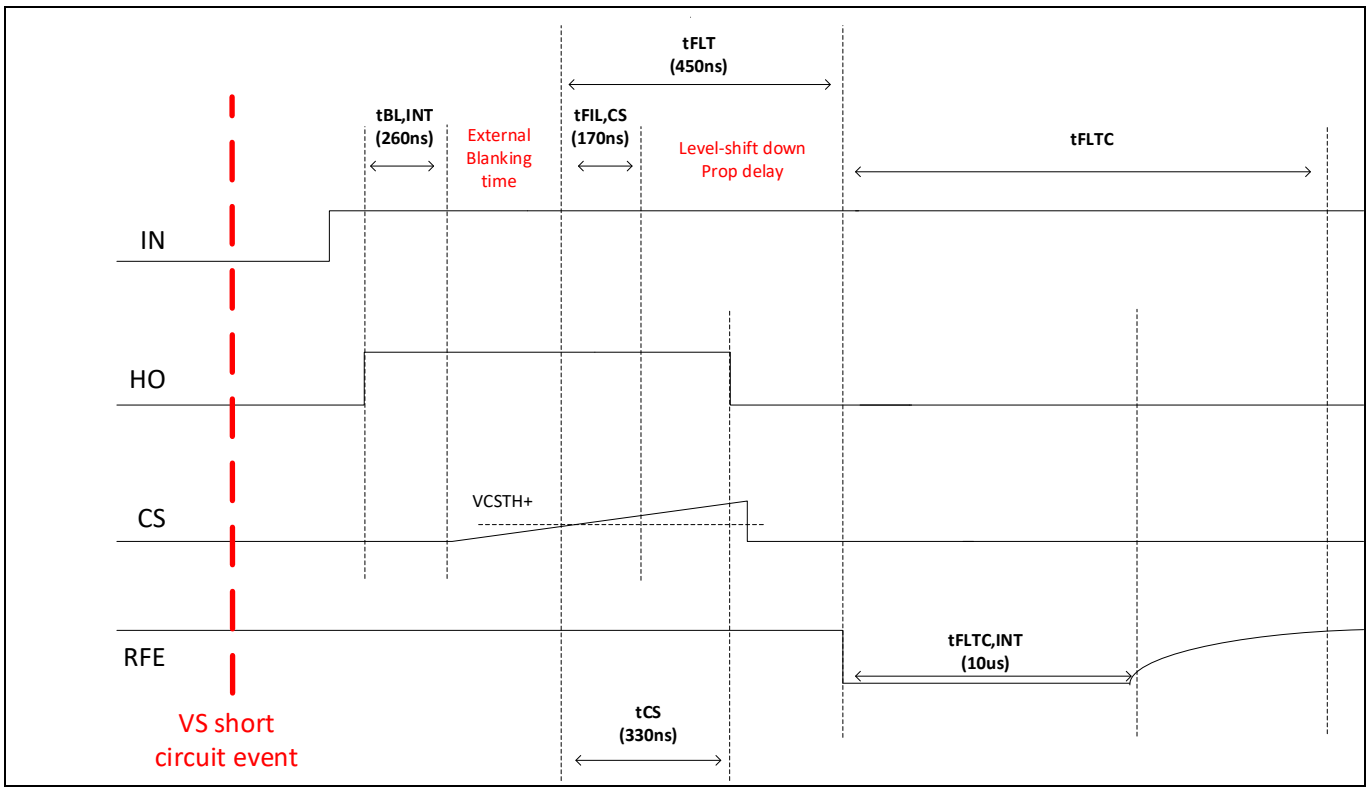


Figure 7 Over-current protection

4.4 Enable, Fault reporting and programmable fault clear timer

The 1ED21x7x provides an enable functionality that can be used to shutdown or enable the HVIC. In addition, it also provides an integrated fault reporting output along with an adjustable fault clear timer. In case of over-current, the fault condition will be triggered. Once the fault condition occurs, the RFE pin is internally pulled to COM and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed, plus 10us ($t_{FLTC,INT}$), After this, the voltage on RFE pin will start to rise, dictated by external pull-up voltage and R_{FLTC} / C_{FLTC} network, as shown in Figure 7.

The total length of the fault clear time period (t_{FLTC}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{FLTC} and C_{FLTC}. For detailed instructions on how to select the R_{FLTC} and C_{FLTC} values, please also refer to the application note.

4.5 Static logic function table

Table 8 provides the truth table for the 1ED21x7x. The first line shows that the UVLO for VCC has been tripped and the gate drive output has been disabled. UVCC is not latched in this case and when VCC is greater than VCCUV+, the driver is functional. However, HO will stay low until the HVIC input receives a new rising transition of HIN.

The second case shows that the UVLO for VBS has been tripped and the gate drive output has been disabled. After VBS exceeds the VBSUV+ threshold, HO will stay low until the HVIC input receives a new rising transition of HIN.

The third case shows the normal operation of the HVIC.

The fourth case illustrates that the CS trip threshold has been reached and that the gate drive outputs have been disabled. This condition is stored in the external RC network waiting for fault clear time.

The last case shows when the HVIC has received a disable command through the RFE input to shutdown; as a result, the gate drive output has been disabled.

Table 8 1ED21x7x truth table

Input				Output		Condition
VCC	VBS	CS	RFE (Enable)	RFE (Fault)	HO	
<	X	X	X	0	0	UVCC
15 V	<	X	X	0	0	UVBS
15 V	15 V	0	High	High	HIN	Normal operation
15 V	15 V	High	X	0	0	Over current
15 V	15 V	0	0	0	0	Disabled

4.6 Undervoltage lockout

1ED21x7x provides undervoltage lockout protection on both the VCC (logic and low-side circuitry) power supply and the VBS (high-side circuitry) power supply. Figure 8 is used to illustrate this concept; VCC (or VBS) is plotted over time and as the waveform crosses the UVLO threshold (VCCUV+/- or VBSUV+/-) the undervoltage protection is enabled or disabled.

Upon power-up, should the VCC voltage fail to reach the VCCUV+ threshold, the IC will not turn-on. Additionally, if the VCC voltage decreases below the VCCUV- threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high-side gate drive outputs.

Upon power-up, should the VBS voltage fail to reach the VBSUV threshold, the IC will not turn-on. Additionally, if the VBS voltage decreases below the VBSUV threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

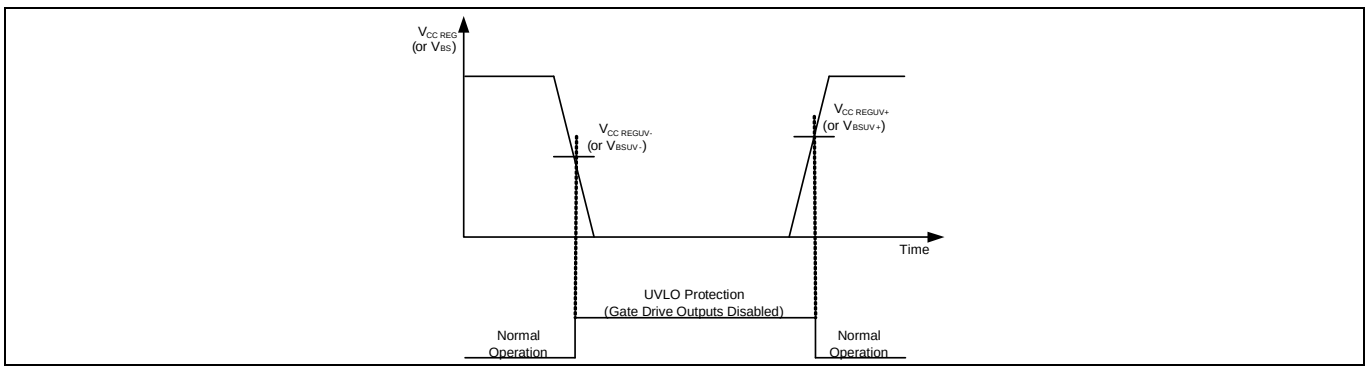


Figure 8 UVLO protection

4.7 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 1ED21x7x's robustness can be seen in Figure 18, where the 1ED21x7x's Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

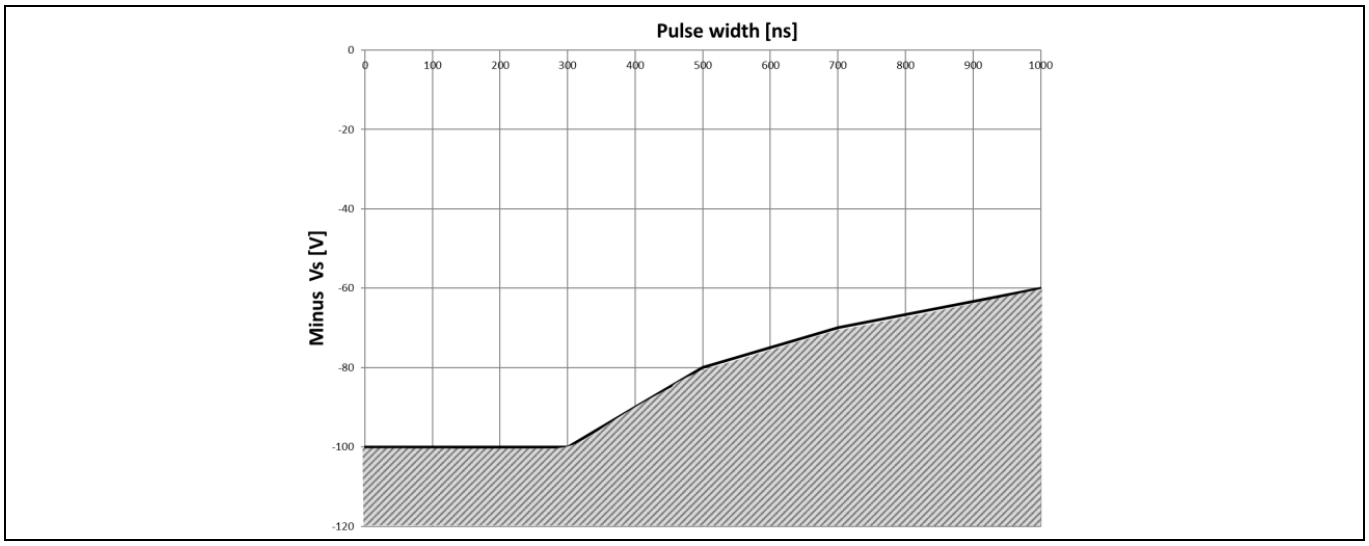


Figure 9 Negative VS transient SOA for 1ED21x7x @ V_{CC} = V_{BS} =15 V, T_A = 25°C

Even though the 1ED21x7x has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

5 Qualification information[1]

Table 9 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.
Moisture sensitivity level		MSL2, 260°C (per IPC/JEDEC J-STD-020E)
ESD	**Charged device model**	Class C3 (1.0 kV) (per ANSI/ESDA/JEDEC JS-002-2018)
	Human body model	Class 2 (2.0 kV) (per ANSI/ESDA/JEDEC JS-001-2017)
RoHS compliant		Yes

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

6 Related products

Table 10 Related products

Product	Description
Gate Driver ICs	
2ED2101(3/4)S06F	650 V high speed, high-side and low-side gate driver with typical 0.29 A source and 0.7 A sink currents in DSO-8 package for driving power MOSFETs and IGBTs.
6EDL04x065xR	EiceDRIVER™ 650 V 2nd generation 3 phase gate driver with a typical 0.165 A source and 0.375 A sink current in DSO-28 and TSSOP-25 package for IGBTs and MOSFETs.
Power Switches	
IKW40N65ET7	650 V, 40 A TRENCHSTOP™ IGBT7 discrete in TO-247 package with soft EC7 diode inside.
IPAN60R125PFD7S	600 V CoolMOS™ PFD7 superjunction MOSFET in TO-220 FullPAK narrow-lead package.
IMBG65R022M1H	650 V CoolSiC™ MOSFET in compact 7 pin SMD pacakge.
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

7 Package information

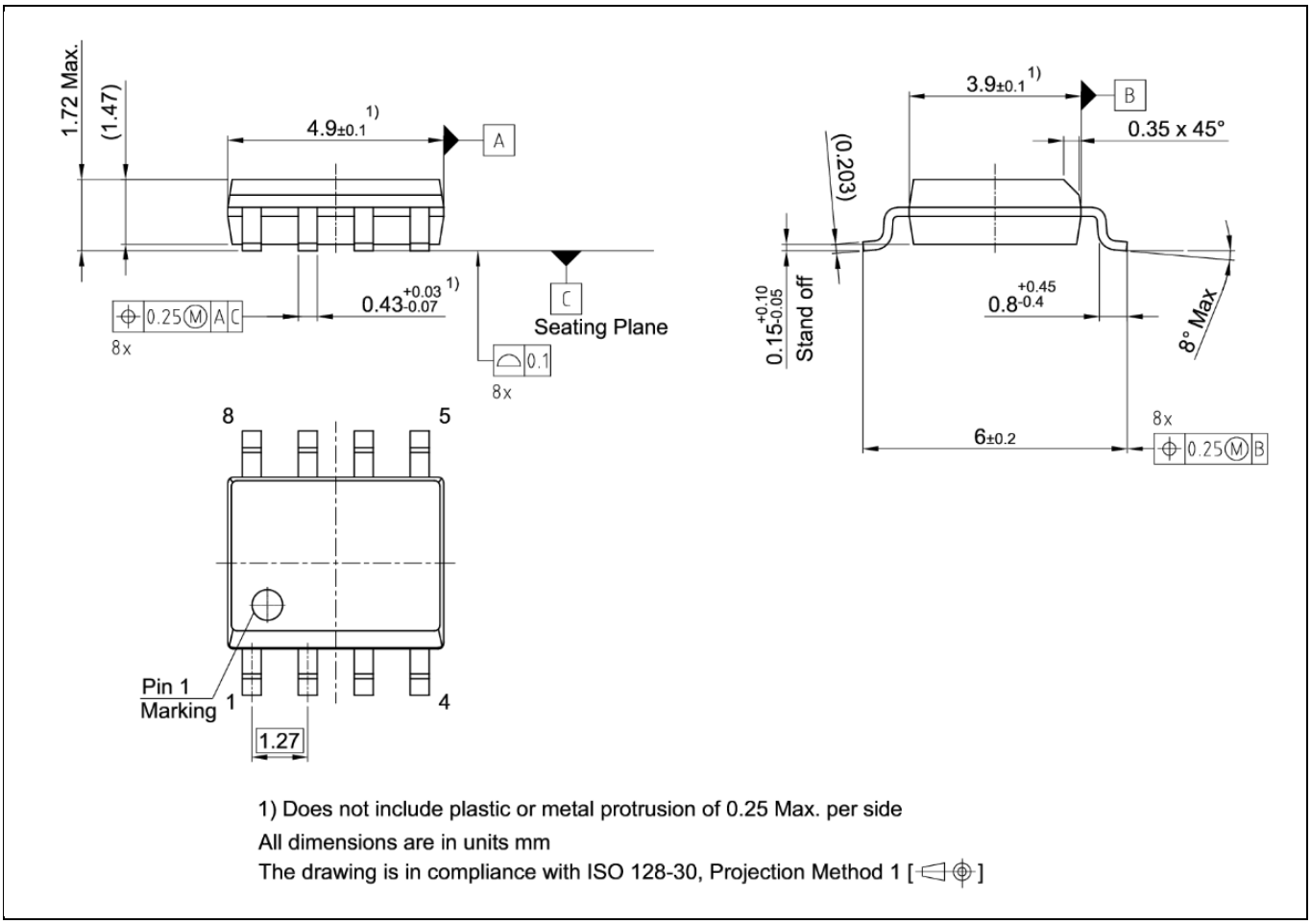
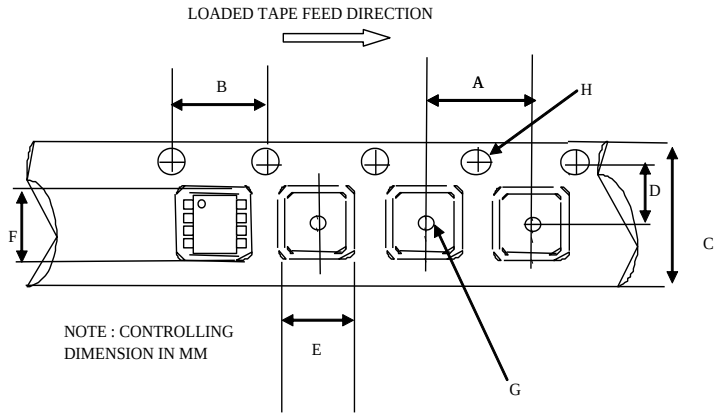
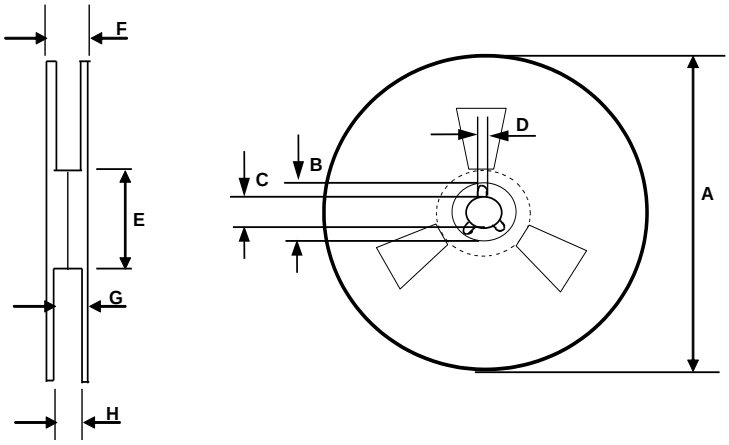


Figure 10 PG-DSO-8 Package drawing



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 11 PG-DSO-8 Tape and reel details

8 Part marking information

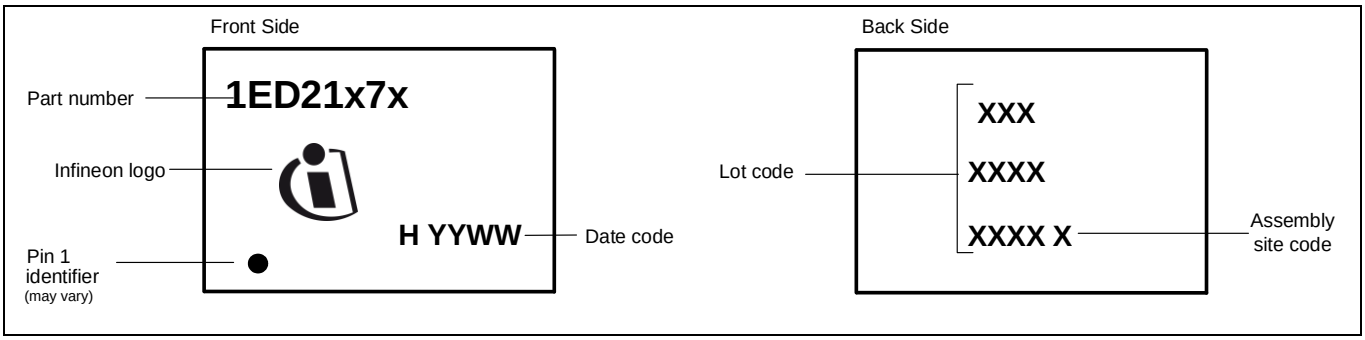


Figure 12 PG-DSO-8 marking information

9 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

9.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

10 Revision history

Document version	Date of release	Description of changes
2.0	2024-12-17	Final datasheet.

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