# BATTERY MONITORING IC


Rev.1.1_00

This IC is a battery monitoring IC developed using CMOS technology. Compared with conventional CMOS voltage detectors, this IC is ideal for the applications that require high-withstand voltage due to its maximum operation voltage as high as 24 V.
This IC is capable of confirming the voltage in stages since it detects four voltage values.
The S-82D9A Series has an EN pin, allowing for reduction of current consumption by using an external signal to turn off this IC.
The S-82D9B Series has a SENSE pin, and the SENSE pin and external components enable battery monitoring equal to or higher than the rated voltage of the IC.

## ■ Features

| | |
|---|---|
| • Detection voltage accuracy: | ±1.0% |
| • Hysteresis characteristics: | $V_{HYS1(S)}$ to $V_{HYS4(S)}$ = 0 mV, 50 mV, 300 mV, 400 mV, 500 mV |
| • Current consumption: | During operation: $I_{DD1}$ = 10 μA max.<br>During power-off: $I_{DD2}$ = 0.1 μA max. |
| • Operation voltage range: | $V_{DD}$ = 3.6 V to 24 V |
| • Detection voltage: | $V_{DET1(S)}$ to $V_{DET4(S)}$ = 7.5 V to 21.5 V (0.1 V step) |
| • Output form: | Nch open-drain output |
| • Output logic*1: | Full charge all on, Individual step voltage on |
| • SENSE pin power-off voltage: | $V_{SENSE}$ < 0.3 V (S-82D9B Series) |
| • Voltage detection pin: | S-82D9A Series: VDD pin<br>S-82D9B Series: SENSE pin |
| • Operation temperature range: | Ta = -40°C to +85°C |
| • Lead-free (Sn 100%), halogen-free | |

***1.** Full charge all on: The multiple output pins become $V_{SS}$ output depending on the input voltage.
When the input voltage is equal to or higher than each of the four detection voltage values, $V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{SS}$.
Individual step voltage on: According to the input voltage, only one output pin is a $V_{SS}$ output.
Set the detection voltage to $V_{DET1} > V_{DET2} > V_{DET3} > V_{DET4}$ and $V_{DETn} > V_{DETn+1} + V_{HYSn+1}$.
$V_{OUT1} = V_{SS}$ and $V_{OUT2} = V_{OUT3} = V_{OUT4}$ = High-Z when the input voltage is equal to or higher than detection voltage 1 ($V_{DET1}$).

## ■ Application

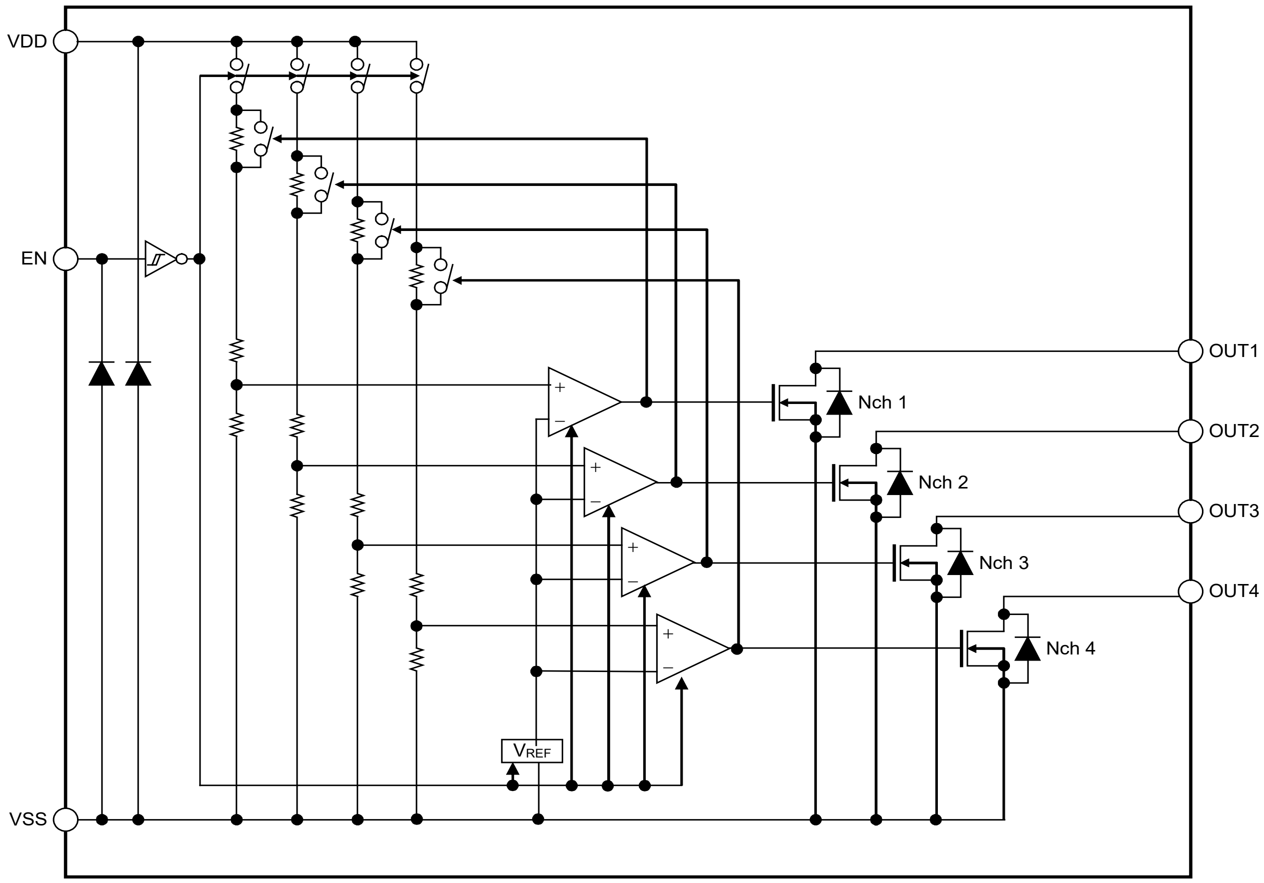
- Rechargeable lithium-ion battery pack

## ■ Package

- HTMSOP-8

## ■ Block Diagram

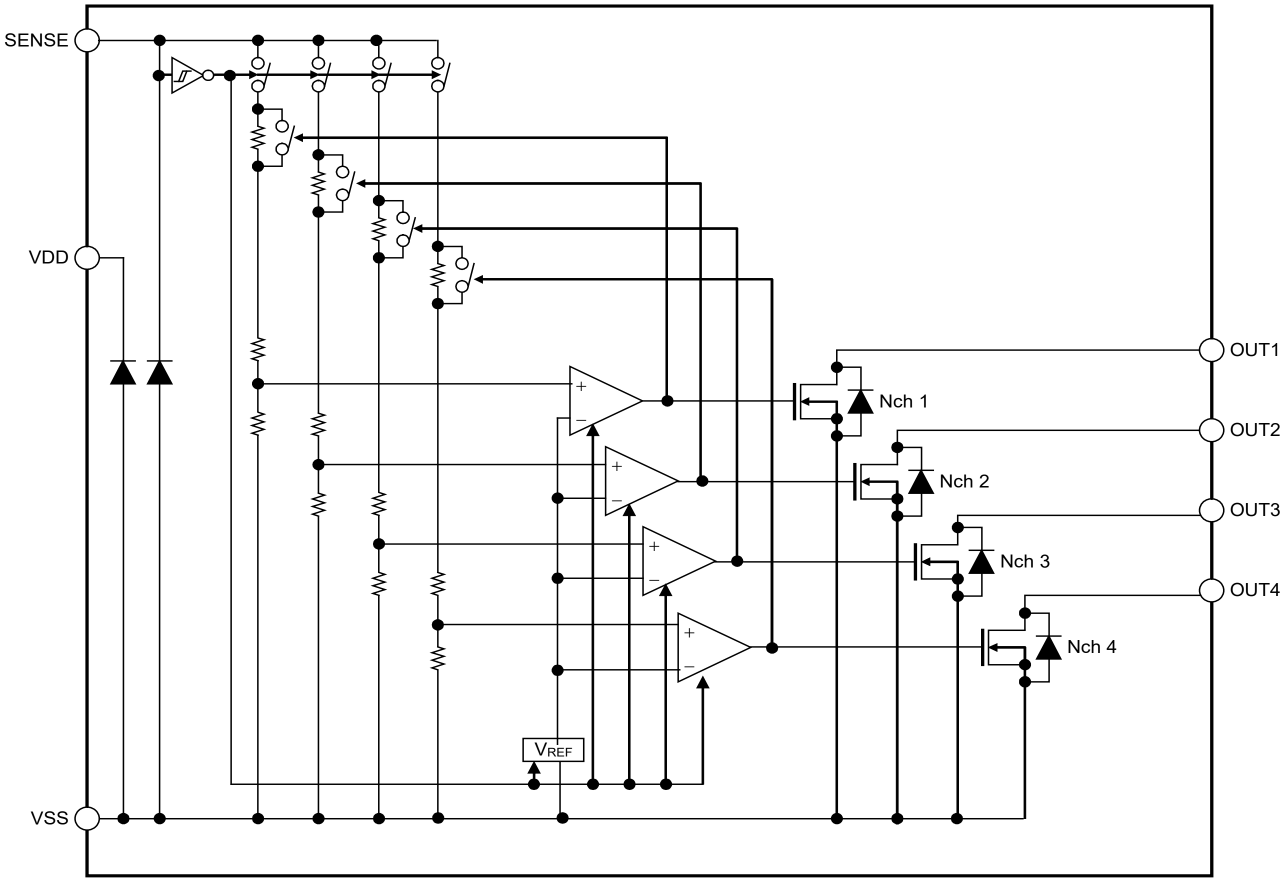
### 1. S-82D9A Series




**Remark** Diodes in the figure are parasitic diodes.

**Figure 1**

### 2. S-82D9B Series




**Remark** Diodes in the figure are parasitic diodes.

**Figure 2**

## ■ Product Name Structure

### 1. Product name

**S-82D9x xx - S8T1 U**

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications *1
S8T1: HTMSOP-8, Tape

Serial code *2
Sequentially set from AA to ZZ

Product type *3
A: EN pin function
B: SENSE pin function

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".
***3.** EN pin function: The EN pin can control the state of the IC.
SENSE pin function: The SENSE pin can monitor the battery voltage.

### 2. Package

**Table 1 Package Drawing Codes**

| Package Name | Dimension | Tape | Reel | Land |
|---|---|---|---|---|
| HTMSOP-8 | FP008-A-P-SD | FP008-A-C-SD | FP008-A-R-SD | FP008-A-L-SD |

## 3. Product name list

### 3. 1 S-82D9A Series

**Table 2 (1 / 2)**

| Product Name | Detection Voltage 1 [$V_{DET1(S)}$] | Detection Voltage 2 [$V_{DET2(S)}$] | Detection Voltage 3 [$V_{DET3(S)}$] | Detection Voltage 4 [$V_{DET4(S)}$] |
|---|---|---|---|---|
| S-82D9AAA-S8T1U | 21.5 V | 16.8 V | 12.1 V | 7.5 V |

**Table 2 (2 / 2)**

| Product Name | Hysteresis Width 1 [$V_{HYS1(S)}$] | Hysteresis Width 2 [$V_{HYS2(S)}$] | Hysteresis Width 3 [$V_{HYS3(S)}$] | Hysteresis Width 4 [$V_{HYS4(S)}$] | Output Logic*1 |
|---|---|---|---|---|---|
| S-82D9AAA-S8T1U | 500 mV | 500 mV | 500 mV | 500 mV | Full charge all on |

### 3. 2 S-82D9B Series

**Table 3 (1 / 2)**

| Product Name | Detection Voltage 1 [$V_{DET1(S)}$] | Detection Voltage 2 [$V_{DET2(S)}$] | Detection Voltage 3 [$V_{DET3(S)}$] | Detection Voltage 4 [$V_{DET4(S)}$] |
|---|---|---|---|---|
| S-82D9BAA-S8T1U | 21.5 V | 16.8 V | 12.1 V | 7.5 V |

**Table 3 (2 / 2)**

| Product Name | Hysteresis Width 1 [$V_{HYS1(S)}$] | Hysteresis Width 2 [$V_{HYS2(S)}$] | Hysteresis Width 3 [$V_{HYS3(S)}$] | Hysteresis Width 4 [$V_{HYS4(S)}$] | Output Logic*1 |
|---|---|---|---|---|---|
| S-82D9BAA-S8T1U | 500 mV | 500 mV | 500 mV | 500 mV | Full charge all on |

***1.** Output Logic: Full charge all on、Individual step voltage on

**Remark** Please contact our sales representatives for products other than the above.

## ■ Pin Configurations

### 1. HTMSOP-8

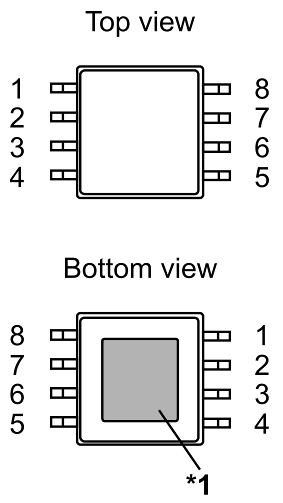



**Figure 3**

**Table 4 S-82D9A Series**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | OUT1 | Voltage detection output pin 1 |
| 2 | OUT2 | Voltage detection output pin 2 |
| 3 | OUT3 | Voltage detection output pin 3 |
| 4 | OUT4 | Voltage detection output pin 4 |
| 5 | NC*2 | No connection |
| 6 | VSS | GND pin |
| 7 | EN | EN signal input pin |
| 8 | VDD | Positive power supply input pin |

**Table 5 S-82D9B Series**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | OUT1 | Voltage detection output pin 1 |
| 2 | OUT2 | Voltage detection output pin 2 |
| 3 | OUT3 | Voltage detection output pin 3 |
| 4 | OUT4 | Voltage detection output pin 4 |
| 5 | NC*2 | No connection |
| 6 | VSS | GND pin |
| 7 | SENSE | Detection voltage input pin |
| 8 | VDD | Positive power supply input pin |

***1.** Connect the heat sink of backside at shadowed area to the board and set electric potential open or $V_{DD}$. However, do not use it as the function of electrode.
***2.** The NC pin is electrically open. The NC pin can be connected to VDD pin or VSS pin.

## ■ Absolute Maximum Ratings

**Table 6**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|
| Input voltage between VDD pin and VSS pin | $V_{DD}$ | $V_{SS}$ - 0.3 to $V_{SS}$ + 28 | V |
| EN pin input voltage (S-82D9A Series) | $V_{EN}$ | $V_{SS}$ - 0.3 to $V_{SS}$ + 28 | V |
| SENSE pin input voltage (S-82D9B Series) | $V_{SENSE}$ | $V_{SS}$ - 0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage n | $V_{OUTn}$ | $V_{SS}$ - 0.3 to $V_{SS}$ + 28 | V |
| Operation ambient temperature | $T_{opr}$ | -40 to +85 | °C |
| Storage temperature | $T_{stg}$ | -40 to +125 | °C |

**Caution** **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

**Remark** n = 1 to 4

## ■ Thermal Resistance Value

**Table 7**

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance[*1] | $\theta_{JA}$ | HTMSOP-8 | Board A | - | 159 | - | °C/W |
| | | | Board B | - | 113 | - | °C/W |
| | | | Board C | - | 39 | - | °C/W |
| | | | Board D | - | 40 | - | °C/W |
| | | | Board E | - | 30 | - | °C/W |

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

## ■ Electrical Characteristics

**Table 8**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|
| **Common** | | | | | | | |
| Detection voltage n[*1] | $V_{DETn}$ | - | $V_{DETn(S)}$ × 0.99 | $V_{DETn(S)}$ | $V_{DETn(S)}$ × 1.01 | V | 1 |
| Hysteresis width n[*2] | $V_{HYSn}$ | 300 mV ≤ $V_{HYSn(S)}$ ≤ 500 mV | $V_{HYSn(S)}$ × 0.8 | $V_{HYSn(S)}$ | $V_{HYSn(S)}$ × 1.2 | V | 1 |
| | | 0 V ≤ $V_{HYSn(S)}$ ≤ 50 mV | $V_{HYSn(S)}$ - 0.025 | $V_{HYSn(S)}$ | $V_{HYSn(S)}$ + 0.025 | V | 1 |
| Operation voltage range between VDD pin and VSS pin | $V_{DD}$ | Fixed output pin voltage | 3.6 | - | 24 | V | - |
| Current consumption during operation[*3] | $I_{DD1}$ | V1 = 23 V, V2 = 23 V | - | - | 10 | μA | 1 |
| Current consumption during power-off | $I_{DD2}$ | V1 = 23 V, V2 = 0 V | - | - | 0.1 | μA | 1 |
| Output sink current n | $I_{OUTn}$ | Full charge all on, V1 = 23 V, V2 = 23 V, V3 = 1 V | 10 | - | - | mA | 2 |
| | | Individual step voltage on V1 = V2 = $V_{DETn}$ + $V_{HYSn}$, V3 = 1 V | 10 | - | - | mA | 2 |
| Output leak current n | $I_{LEAKn}$ | V1 = 23 V, V2 = 0 V, V3 = 23 V | - | - | 0.1 | μA | 2 |
| **S-82D9A Series** | | | | | | | |
| EN pin input voltage "H" | $V_{SH}$ | V1 = 23 V | 1.5 | - | - | V | 1 |
| EN pin input voltage "H" | $V_{SL}$ | V1 = 23 V | - | - | 0.3 | V | 1 |
| **S-82D9B Series** | | | | | | | |
| SENSE pin current | $I_{SENSE}$ | V1 = 23 V, V2 = 23 V | - | - | 10 | μA | 1 |
| SENSE pin input voltage "H" | $V_{SH}$ | V1 = 23 V | 7 | - | - | V | 1 |
| SENSE pin input voltage "L" | $V_{SL}$ | V1 = 23 V | - | - | 0.3 | V | 1 |

***1.** $V_{DETn}$: Actual detection voltage value, $V_{DETn(S)}$: Set detection voltage
***2.** $V_{HYSn}$: Actual hysteresis width, $V_{HYSn(S)}$: Set hysteresis width
The relationship between $V_{DETn}$ and $V_{HYSn}$ is as follows.
$V_{DETn} < V_{DETn} + V_{HYSn}$
***3.** Current consumption = $I_{VDD}$ + $I_{EN}$ (S-82D9A Series)
Current consumption = $I_{VDD}$ + $I_{SENSE}$ (S-82D9B Series)

**Remark** n = 1 to 4

## ■ Test Circuits

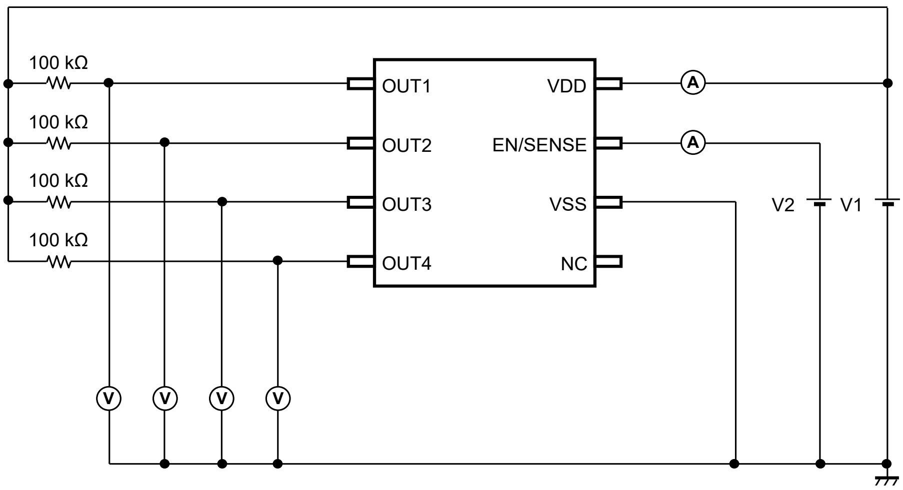



**Figure 4 Test Circuit 1**

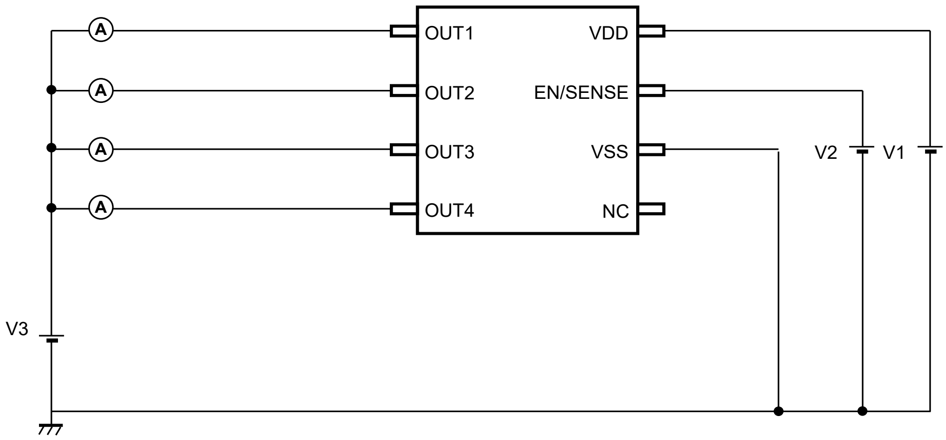



**Figure 5 Test Circuit 2**

## ■ Standard Circuit

### 1. S-82D9A Series

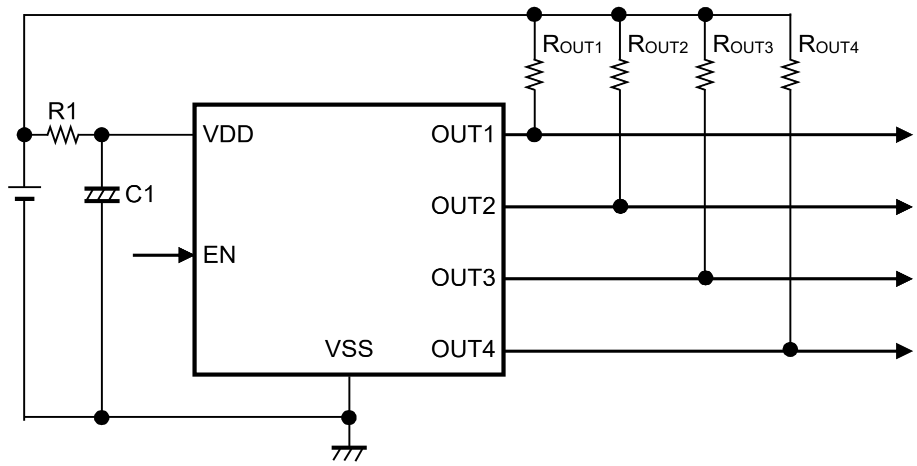



**Figure 6**

### 2. S-82D9B Series

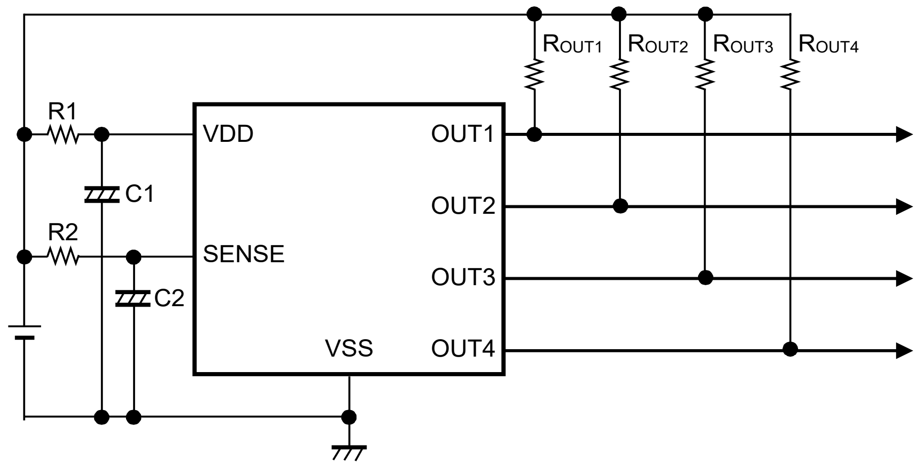



**Figure 7**

**Table 9 Constants for External Components**

| Symbol | Purpose | Typ. | Remark |
|---|---|---|---|
| R1, R2*1 | For power fluctuation | 470 Ω | Set the value as small as possible to prevent deterioration of the detection voltage. |
| C1, C2 | For power fluctuation | 0.1 μF | - |
| $R_{OUTn}$*2 | For output pin pull-up | 1 kΩ | Make sure the power dissipation of this IC is not exceeded. |

***1.** Set up R1, R2 as 100 kΩ or less to prevent oscillation.
***2.** Set up each of $R_{OUTn}$ as 620 Ω or more so that the power dissipation is not exceeded.

**Caution 1. The constants may be changed without notice.**
**2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**

**Remark** n = 1 to 4

## ■ Operation

### 1. Basic operation

#### 1. 1 S-82D9A Series

**1. 1. 1 When the power supply voltage ($V_{DD}$) decreases**

The OUTn pin becomes detection status if $V_{DD}$ is equal to or lower than the detection voltage ($V_{DETn}$).

**1. 1. 2 When the power supply voltage increases**

The OUTn pin becomes release status if $V_{DD}$ is equal to or higher than the release voltage ($V_{DETn}$ + $V_{HYSn}$).

**1. 1. 3 When $V_{DD}$ ≤ minimum operation voltage**

The OUTn pin voltage is indefinite.

#### 1. 2 S-82D9B Series

**1. 2. 1 When the SENSE pin voltage ($V_{SENSE}$) decreases**

The OUTn pin becomes detection status if $V_{SENSE}$ is equal to or lower than the detection voltage ($V_{DETn}$).

**1. 2. 2 When the SENSE pin voltage increases**

The OUTn pin becomes release status if $V_{SENSE}$ is equal to or higher than the release voltage ($V_{DETn}$ + $V_{HYSn}$).

**1. 2. 3 When $V_{SENSE}$ ≤ minimum operation voltage**

Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUTn pin is stable when $V_{DD}$ is minimum operation voltage or higher.

### 2. EN pin (S-82D9A Series)

This pin starts and stops this IC.
When $V_{EN}$ ≤ $V_{SL}$ is set, all internal circuits stop operating, and Nch transistor n (refer to **Figure 1** in "**■ Block Diagram**") is turned off, reducing current consumption significantly.
When not using the EN pin, connect it to the VDD pin.
Refer to the circuit diagram in **Figure 11** for the circuit connection example.

### 3. SENSE pin (S-82D9B Series)

This pin starts and stops this IC and monitors the battery voltage.
When $V_{SENSE}$ ≤ $V_{SL}$ is set, all internal circuits stop operating, and Nch transistor n (refer to **Figure 2** in **■ Block Diagram**") is turned off, reducing current consumption significantly.
Refer to the circuit diagram in **Figure 12** and **Figure 13** for the circuit connection example.

**Remark** n = 1 to 4

## ■ Timing Charts

### 1. S-82D9A Series (Full charge all on, $V_{EN} \geq V_{SH}$)

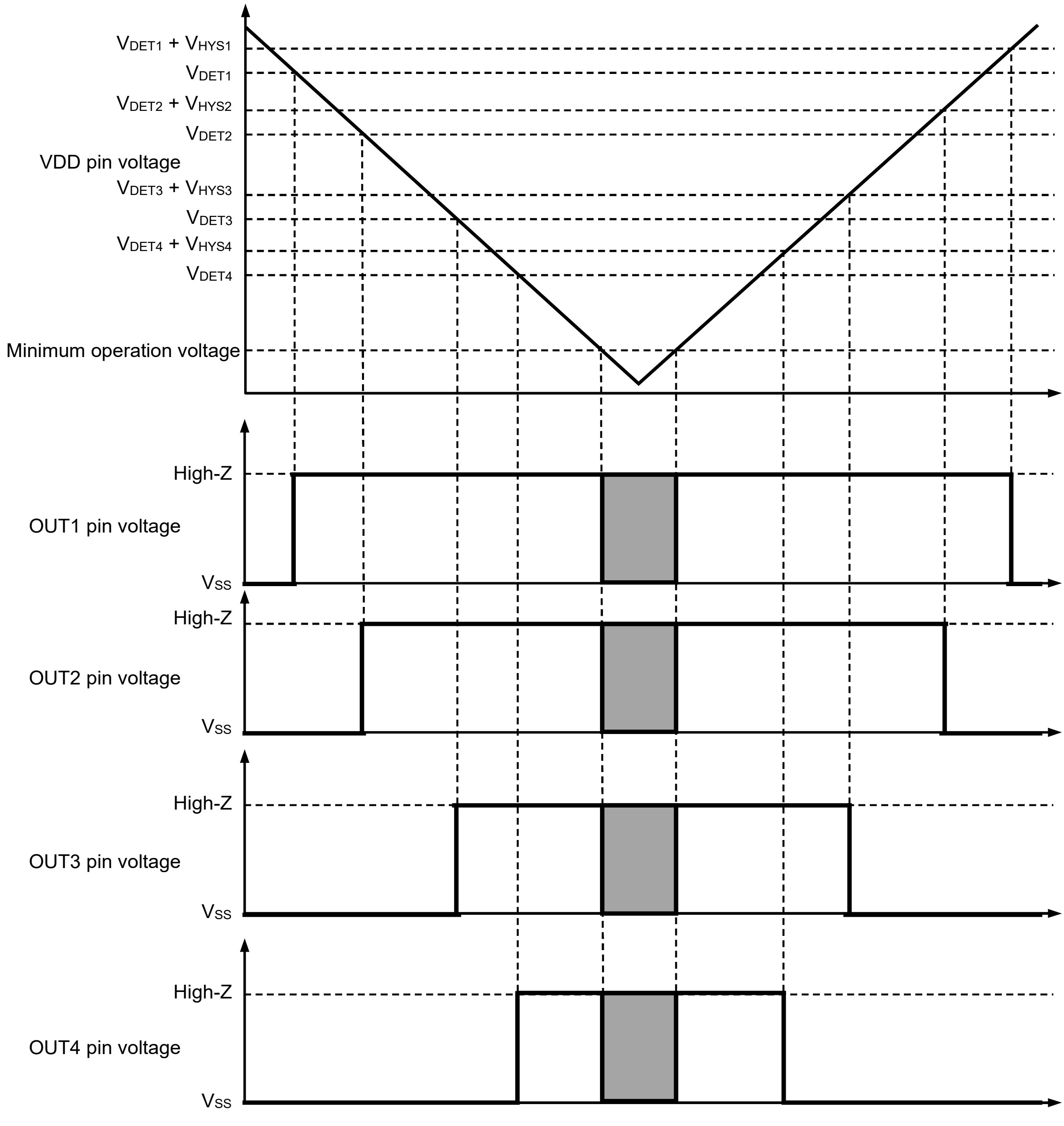



**Figure 8**

**Remark** When $V_{DD}$ is equal to or lower than the minimum operation voltage, the output voltage from the OUT1 pin to the OUT4 pin is indefinite in the shaded area.

2. S-82D9A Series (Individual step voltage on, $V_{EN} \geq V_{SH}$)

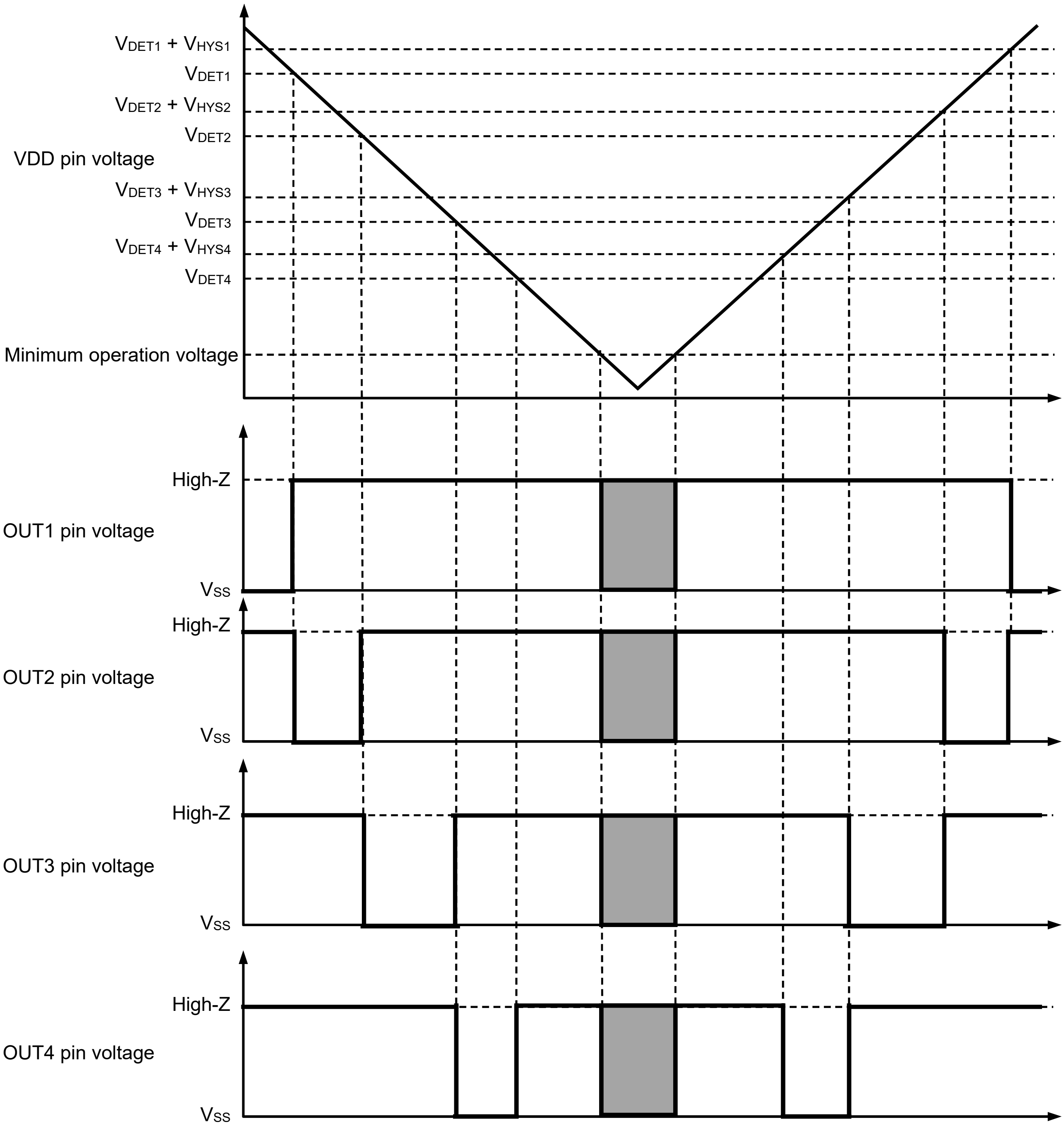



**Figure 9**

**Remark** When $V_{DD}$ is equal to or lower than the minimum operation voltage, the output voltage from the OUT1 pin to the OUT4 pin is indefinite in the shaded area.

### 3. S-82D9B Series (Full charge all on, $V_{SENSE} \geq V_{SH}$)

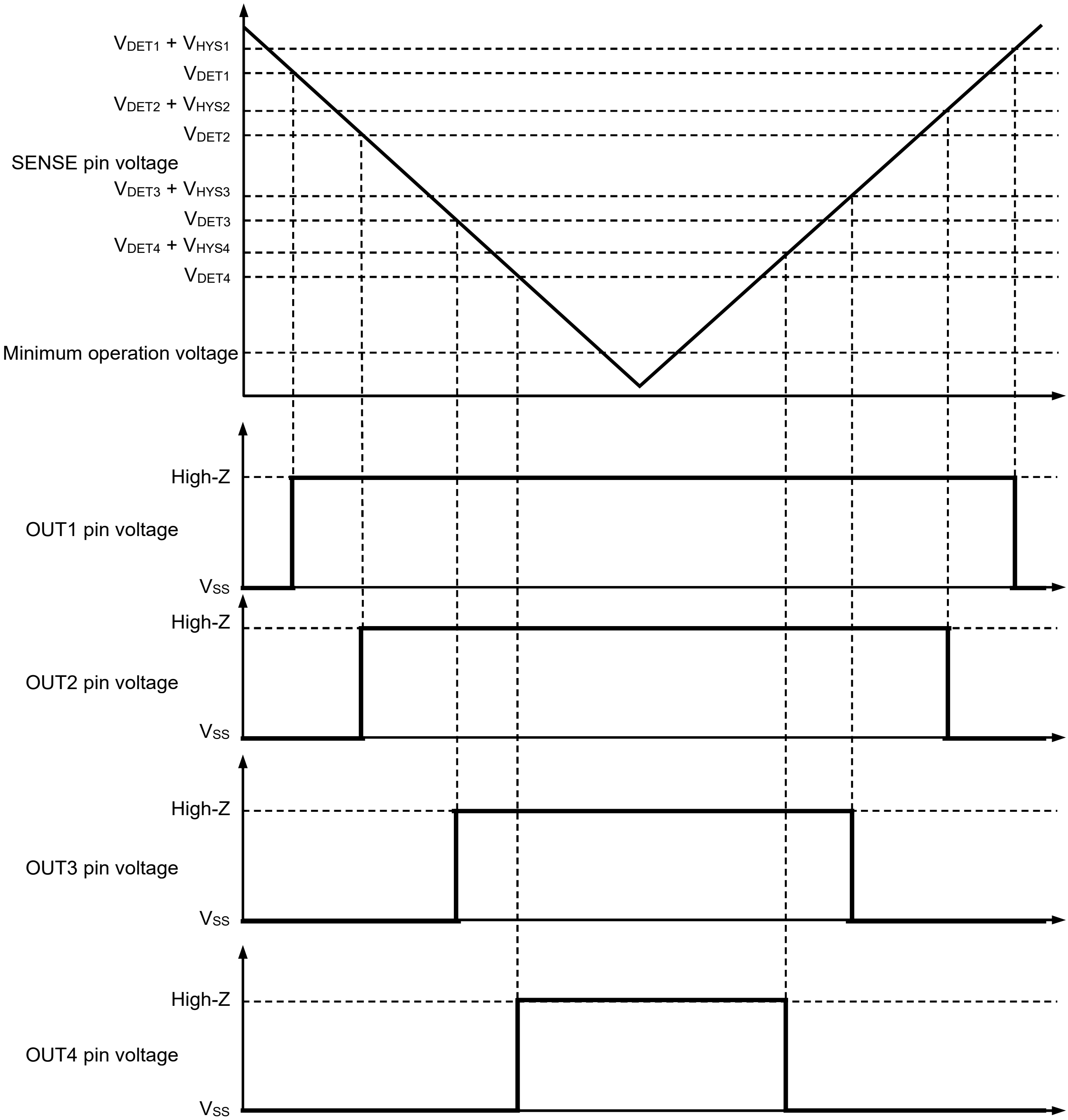



**Figure 10**

**Remark** Even if $V_{SENSE}$ is below the minimum operating voltage of the IC, the output voltage from the OUT1 pin to OUT4 pin are stable when $V_{DD}$ is minimum operation voltage or higher.

## ■ Application Circuits

### 1. LED battery level Indicator

#### 1. 1 S-82D9A Series

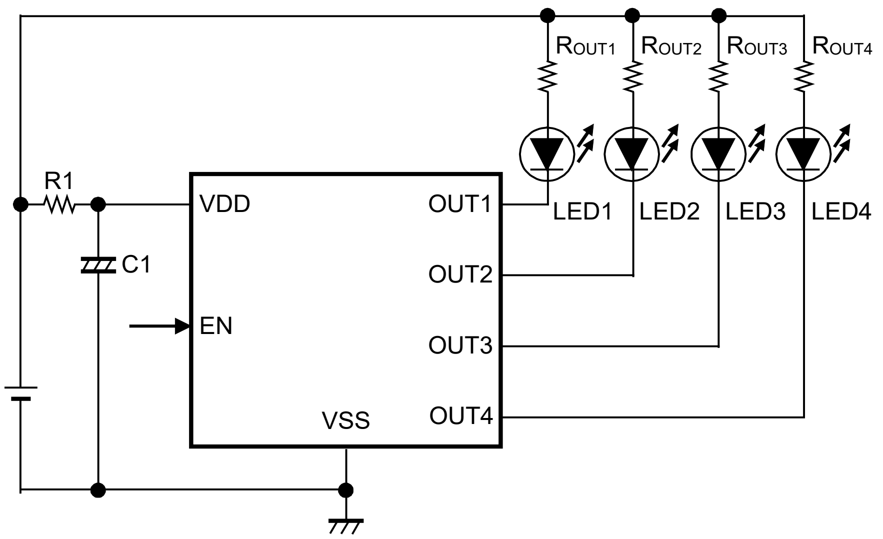



**Figure 11**

**Caution It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**

#### 1. 2 S-82D9B Series

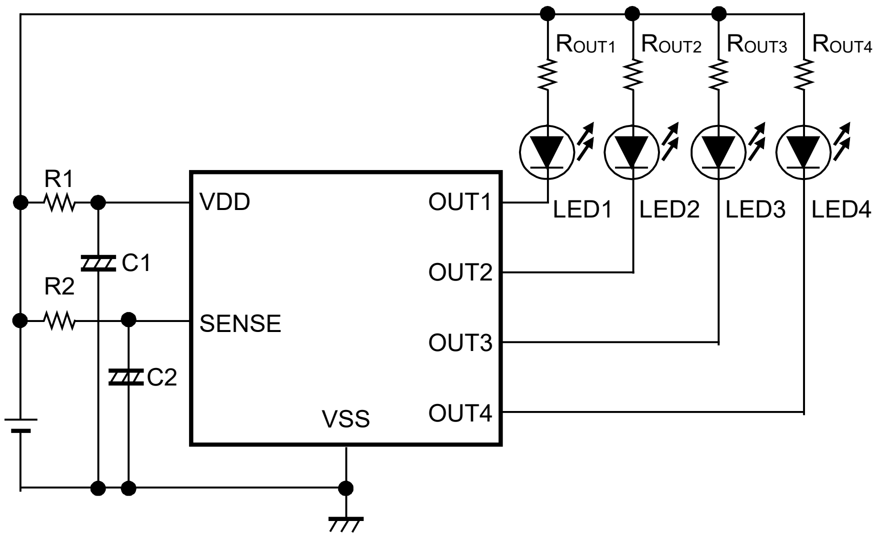



**Figure 12**

**Caution It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**

## 2. Change of detection voltage using S-82D9B Series

This IC can monitor battery voltage equal to or higher than the rated voltage of the IC by making the connection shown in **Figure 13.**

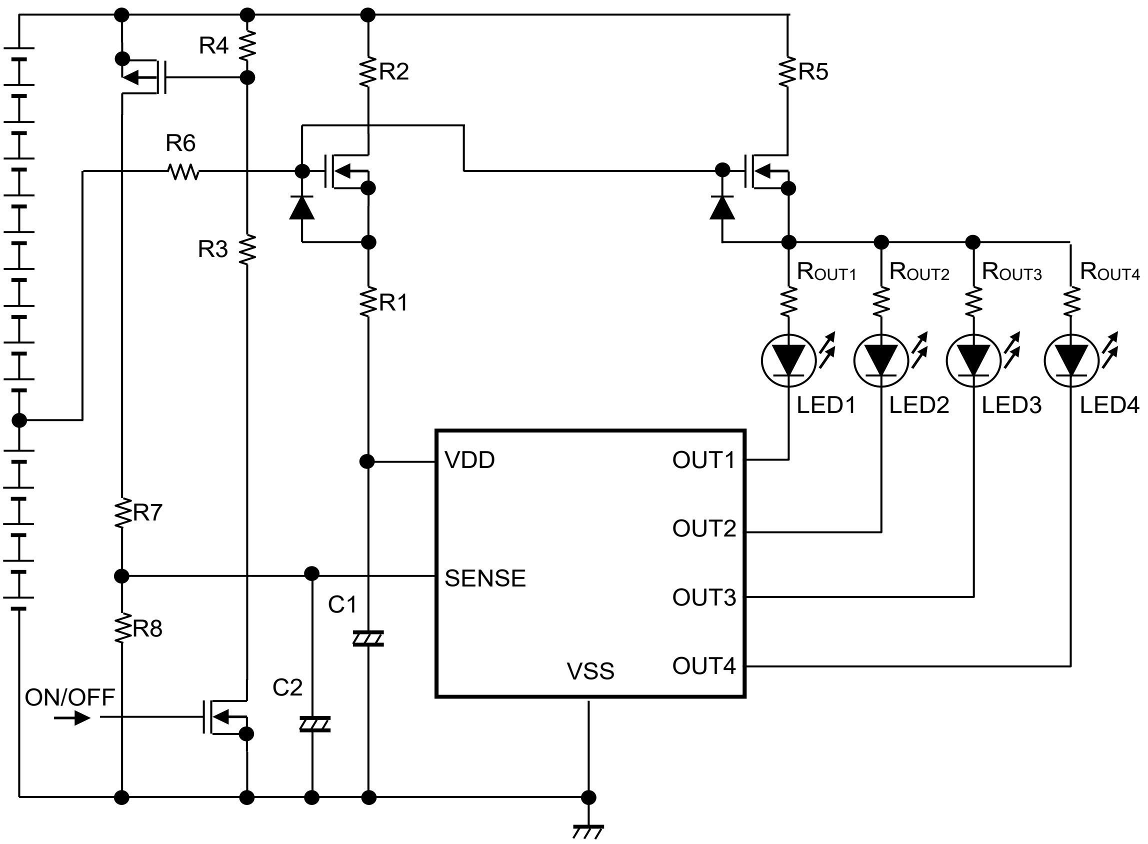



**Figure 13**

**Caution It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**

## ■ Precautions

- The application conditions for the input voltage, output voltage, and output pin pull-up resistance should not exceed the package power dissipation.

- Wiring patterns for the VDD pin, the VOUTn pin and the VSS pin should be designed so that the impedance is low.

- Note that the detection voltage may deviate due to the resistance component of output sink current and the VSS pin wiring.

- In applications where a resistor is connected to the input (refer to **Figure 11** in "**■ Application Circuit**"), the feed-through current which is generated when the output switches causes a voltage drop equal to feed-through current × input resistance. After the output switches, the feed-through current stops and its resultant voltage drop disappears, and the output switches. The feed-through current is then generated again, a voltage drop appears. Note that an oscillation may be generated for this reason.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

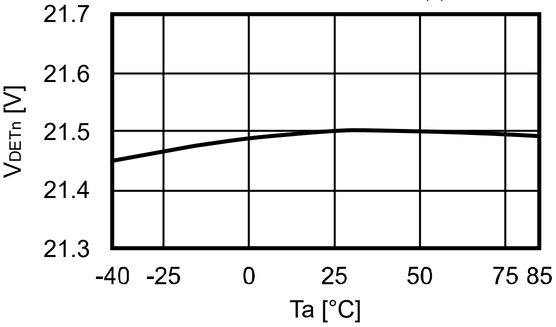
**Remark** n = 1 to 4

## ■ Characteristics (Typical Data)

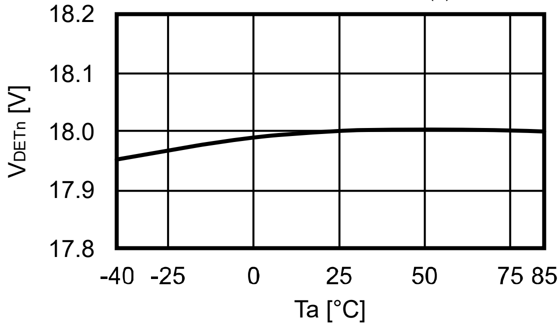
### 1. Detection voltage

#### 1. 1 $V_{DETn}$ vs. Ta

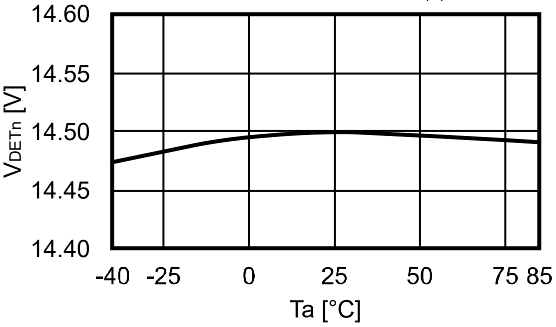
$V_{DETn(S)}$ = 21.5 V



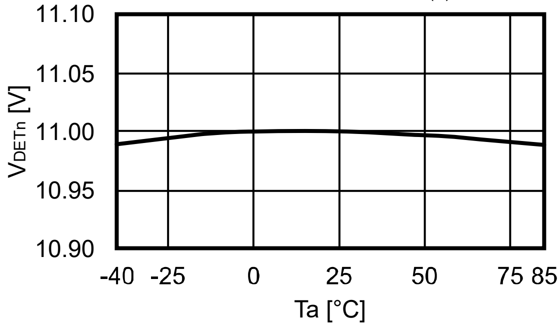

$V_{DETn(S)}$ = 18.0 V



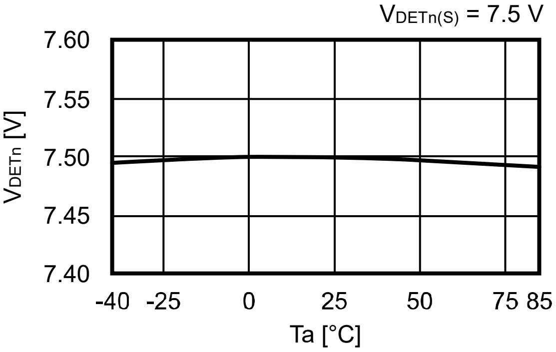

$V_{DETn(S)}$ = 14.5 V




$V_{DETn(S)}$ = 11.0 V



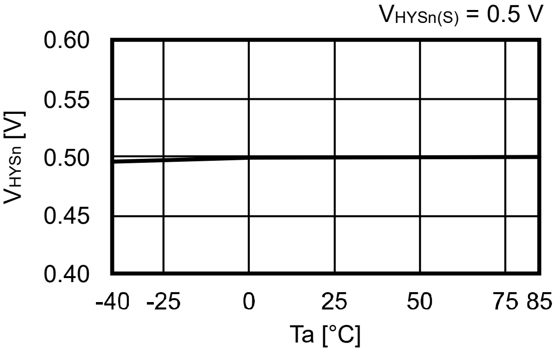

$V_{DETn(S)}$ = 7.5 V



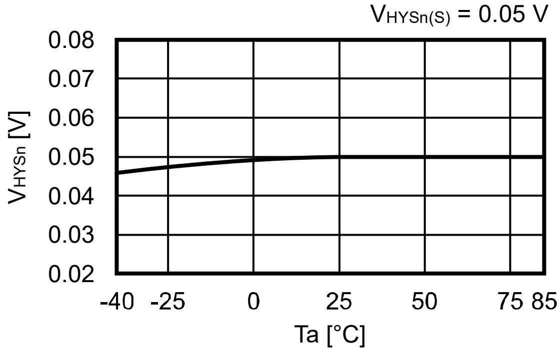

### 2. Hysteresis width

#### 2. 1 $V_{HYSn}$ vs. Ta

$V_{HYSn(S)}$ = 0.5 V



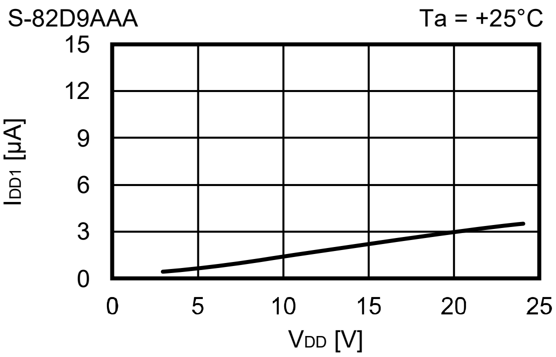

$V_{HYSn(S)}$ = 0.05 V



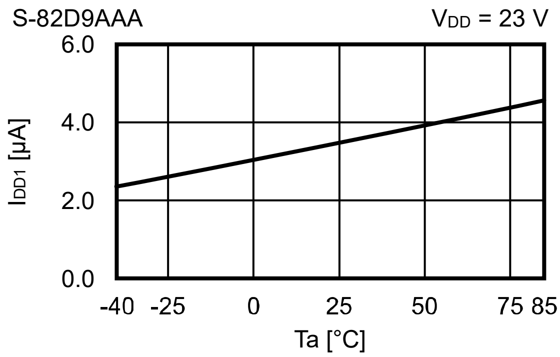

**Remark** n = 1 to 4

## 3. Current consumption

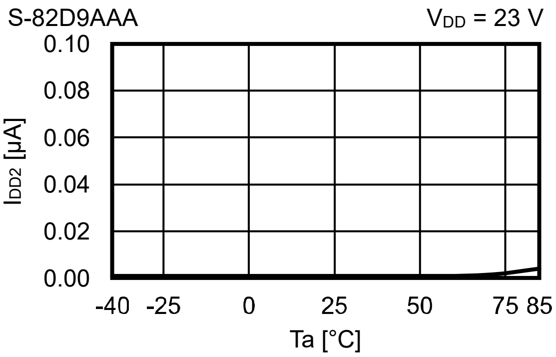
### 3. 1 $I_{DD1}$ vs. $V_{DD}$




### 3. 2 $I_{DD1}$ vs. Ta

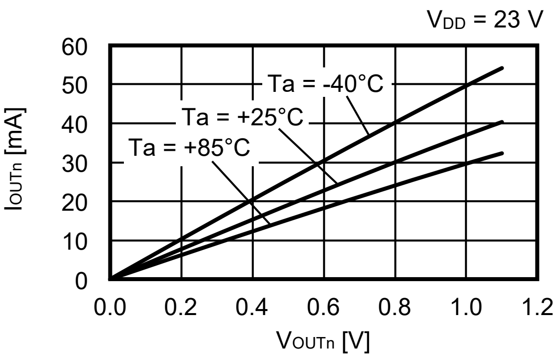



### 3. 3 $I_{DD2}$ vs. Ta

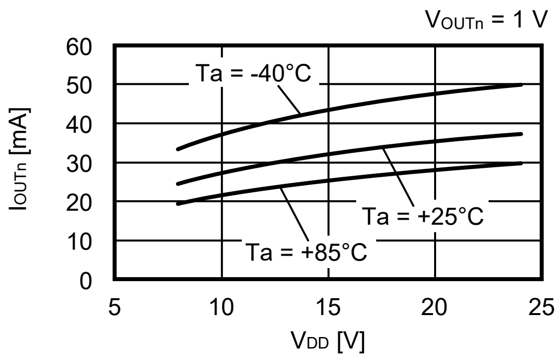



## 4. Output current

### 4. 1 $I_{OUTn}$ vs. $V_{OUTn}$



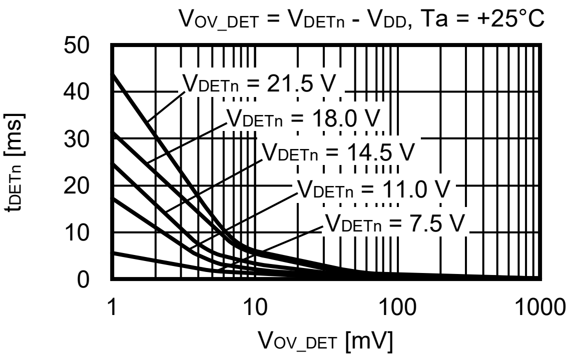

### 4. 2 $I_{OUTn}$ vs. $V_{DD}$



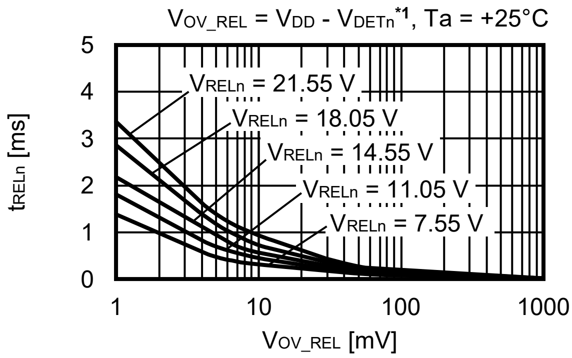

**Remark** n = 1 to 4

## 5. Response time

### 5. 1 $t_{DETn}$ vs. $V_{OV\_DET}$




### 5. 2 $t_{RELn}$ vs. $V_{OV\_REL}$




***1.** $V_{RELn} = V_{DETn} + V_{HYSn}$

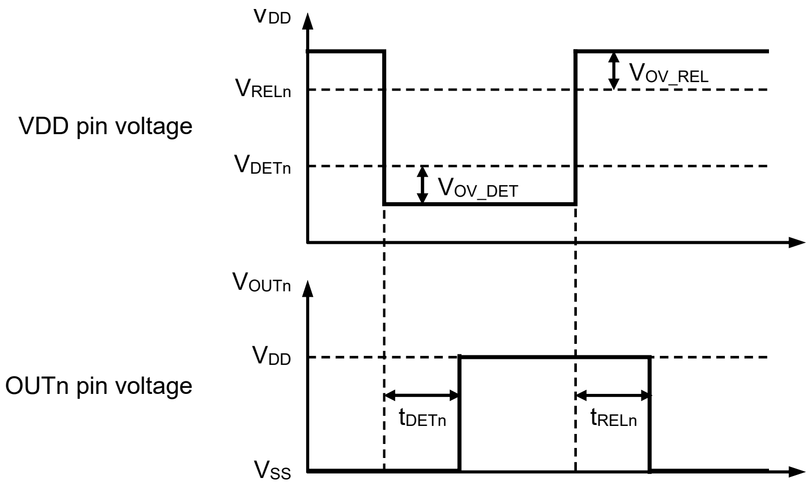
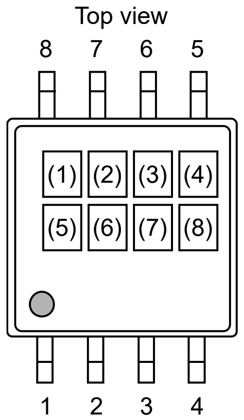



**Figure 14 Test Condition of Response Time**

**Remark 1.** Refer to "**Figure 4 Test Circuit 1**" for the test condition of the response time.
**2.** n = 1 to 4

## ■ Marking Specifications

### 1. HTMSOP-8




(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5): Blank
(6) to (8): Lot number

**Product name vs. Product code**

**1. 1 S-82D9A Series**

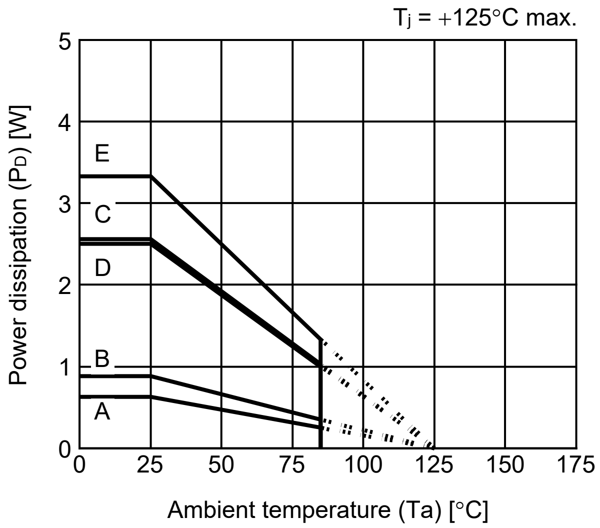
| Product Name | Product Code | | |
|---|---|---|---|
| | (2) | (3) | (4) |
| S-82D9AAA-S8T1U | 9 | Y | A |

**1. 2 S-82D9B Series**

| Product Name | Product Code | | |
|---|---|---|---|
| | (2) | (3) | (4) |
| S-82D9BAA-S8T1U | 9 | Y | C |

## ■ Power Dissipation

**HTMSOP-8**

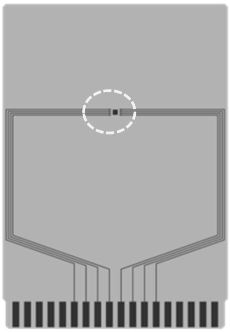



| Board | Power Dissipation ($P_D$) |
|---|---|
| A | 0.63 W |
| B | 0.88 W |
| C | 2.56 W |
| D | 2.50 W |
| E | 3.33 W |

# HTMSOP-8 Test Board

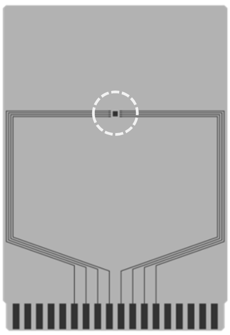
IC Mount Area

### (1) Board A



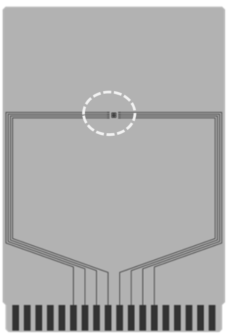
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

### (2) Board B

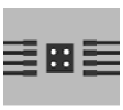


| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

### (3) Board C



| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | Number: 4<br>Diameter: 0.3 mm |



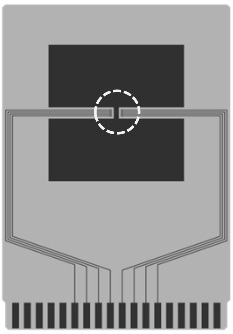
enlarged view

No. HTMSOP8-A-Board-SD-1.0

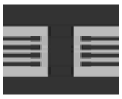
# HTMSOP-8 Test Board

IC Mount Area

**(4) Board D**

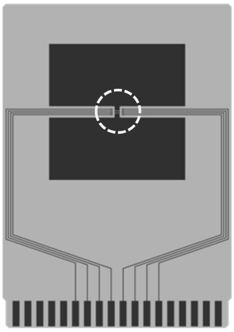


| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Pattern for heat radiation: 2000mm$^2$ t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

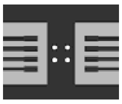


enlarged view

**(5) Board E**

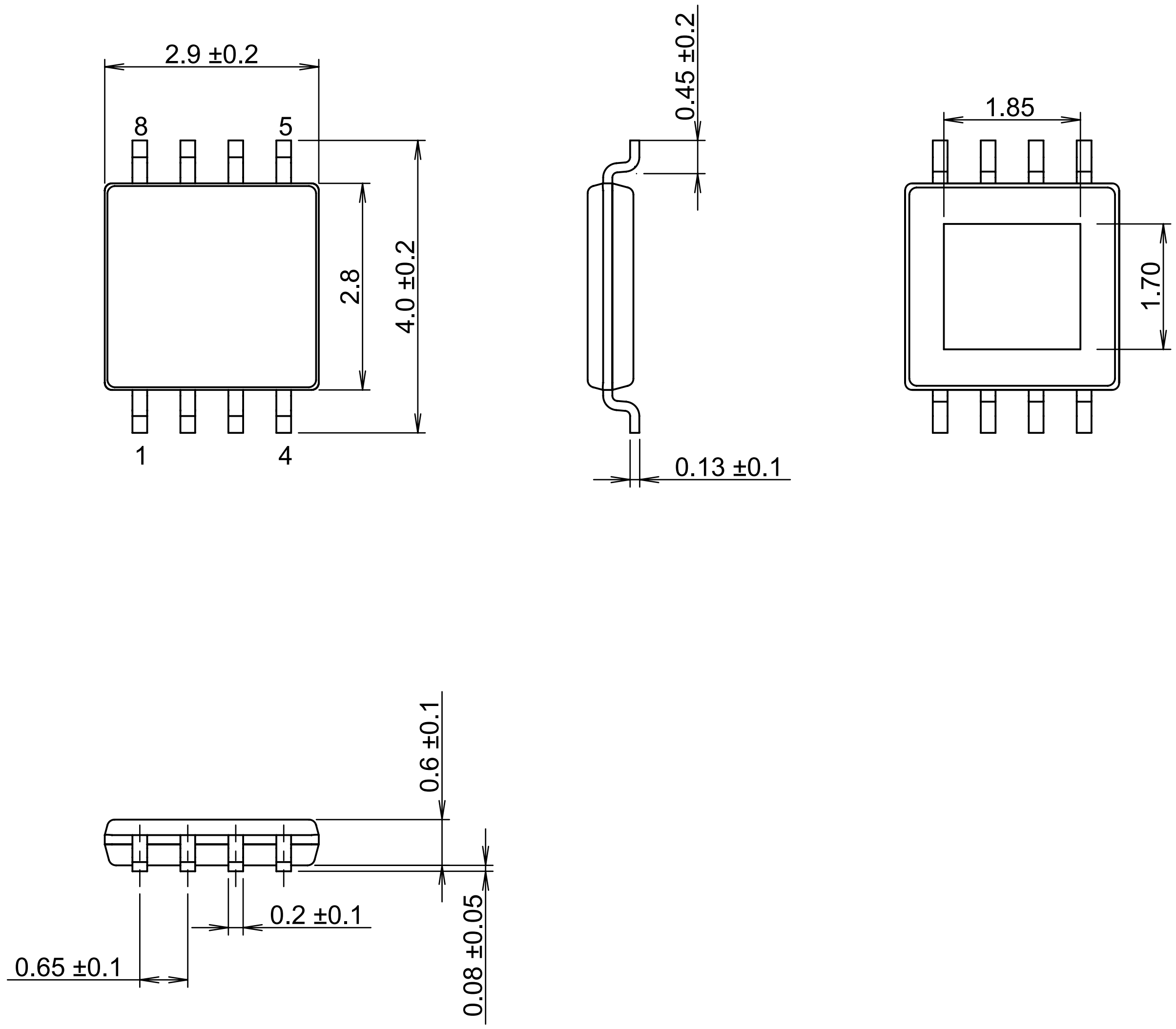


| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Pattern for heat radiation: 2000mm$^2$ t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | Number: 4<br>Diameter: 0.3 mm |



enlarged view

No. HTMSOP8-A-Board-SD-1.0




No. FP008-A-P-SD-2.0

| | |
|---|---|
| TITLE | HTMSOP8-A-PKG Dimensions |
| No. | FP008-A-P-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |

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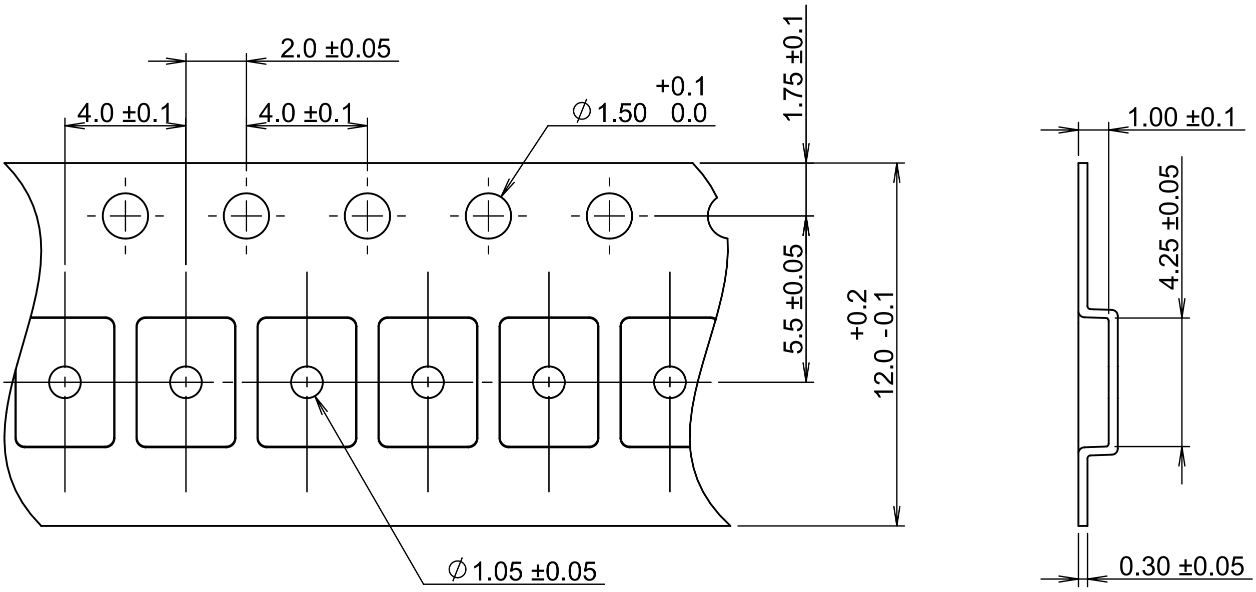


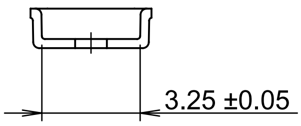


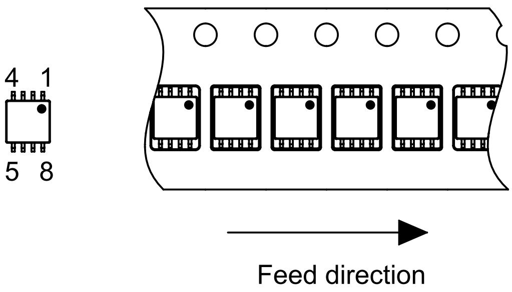


No. FP008-A-C-SD-1.0

| | |
|---|---|
| TITLE | HTMSOP8-A-Carrier Tape |
| No. | FP008-A-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |

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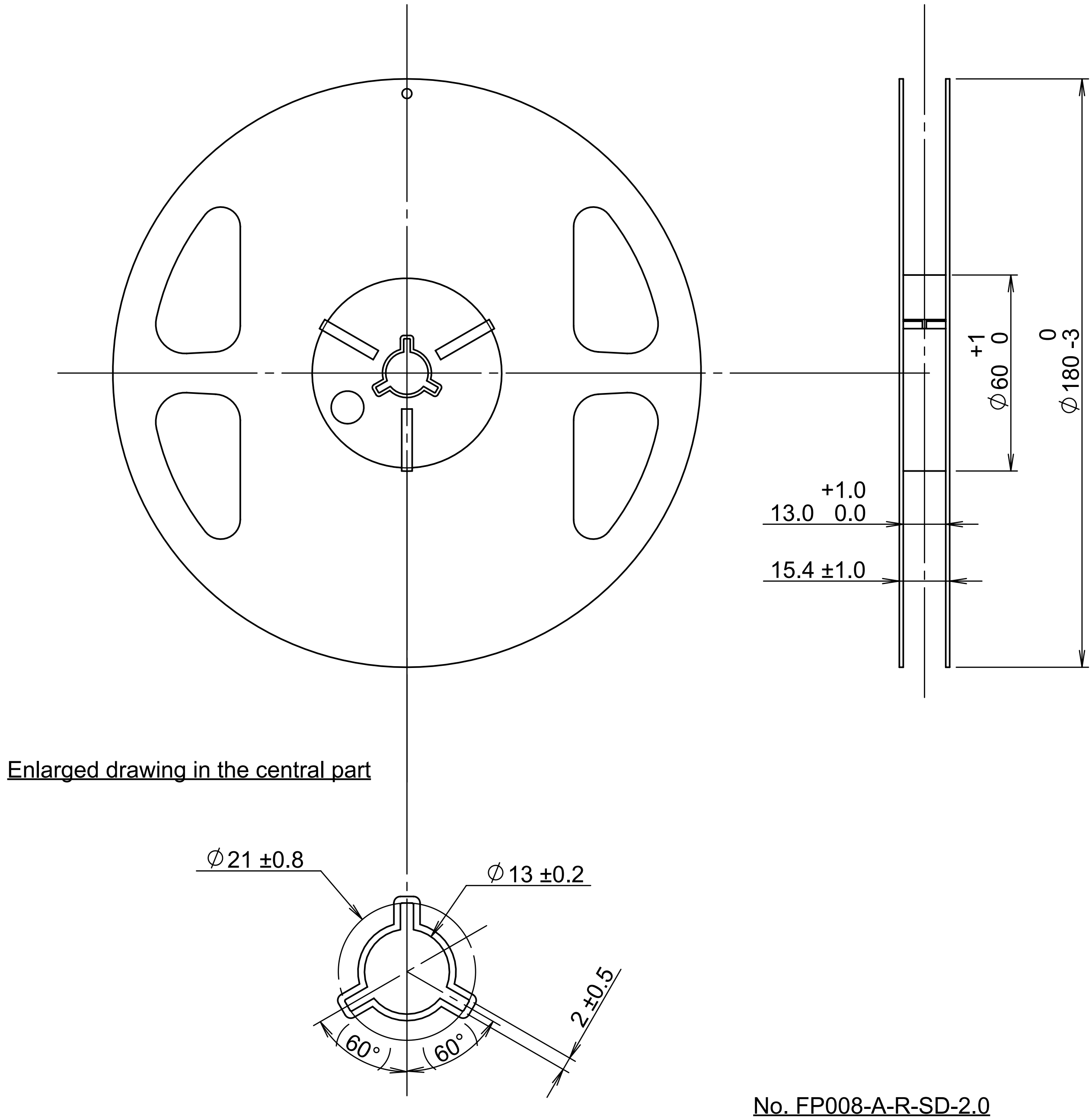
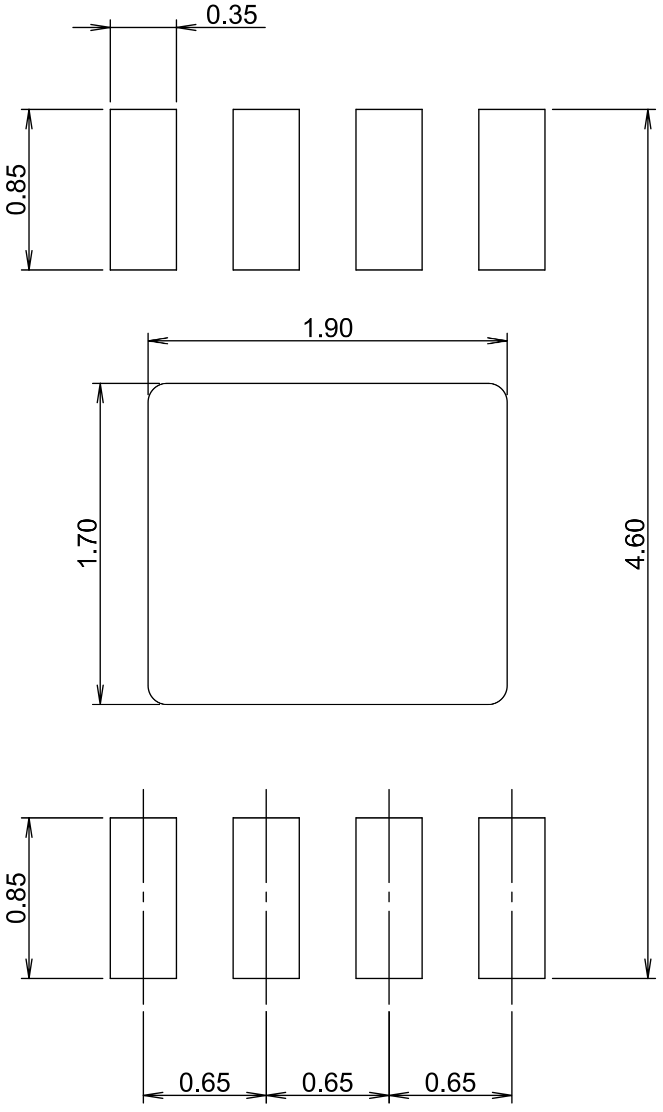



No. FP008-A-R-SD-2.0

| | | | |
|---|---|---|---|
| TITLE | HTMSOP8-A-Reel | | |
| No. | FP008-A-R-SD-2.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |

**ABLIC Inc.**




No. FP008-A-L-SD-2.0

| | |
|---|---|
| TITLE | HTMSOP8-A<br>-Land Recommendation |
| No. | FP008-A-L-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |

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