

This IC is high-side protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuit, delay circuit, and triple boost charge pump to drive an external charge / discharge FET. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.

By using an external overcurrent detection resistor, this IC realizes high-accuracy overcurrent protection with less effect from temperature change.

■ Features

- High-accuracy voltage detection circuit

| | | |
|--|---|-------------------|
| Overcharge detection voltage: | 3.500 V to 4.800 V (5 mV step) | Accuracy ±15 mV |
| Overcharge release voltage: | 3.100 V to 4.800 V ^{*1} | Accuracy ±50 mV |
| Overdischarge detection voltage: | 2.000 V to 3.000 V (10 mV step) | Accuracy ±50 mV |
| Overdischarge release voltage: | 2.000 V to 3.400 V ^{*2} | Accuracy ±75 mV |
| Discharge overcurrent 1 detection voltage: | -3 mV to -100 mV (0.25 mV step) | Accuracy ±0.75 mV |
| Discharge overcurrent 2 detection voltage: | -6 mV to -100 mV (0.5 mV step) | Accuracy ±2 mV |
| Load short-circuiting detection voltage: | -20 mV to -100 mV (1 mV step) | Accuracy ±4 mV |
| Charge overcurrent detection voltage: | 3 mV to 100 mV (0.25 mV step) | Accuracy ±0.75 mV |
| 0 V battery charge inhibition battery voltage: | 1.45 V to 2.00 V ^{*3} (50 mV step) | Accuracy ±50 mV |
- Overheat detection function: Available, unavailable
- High-accuracy temperature detection circuit with an external NTC thermistor
(Resistance: 100 kΩ ±1% or 470 kΩ ±1% at 25°C, B-constant: ±1%)

| | | |
|---------------------------------|---|---------------|
| Overheat detection temperature: | +65°C to +85°C (5°C step) | Accuracy ±3°C |
| Overheat release temperature: | +55°C to +80°C (5°C step) ^{*4} | Accuracy ±5°C |
- Internal charge pump: Triple boost (regulation voltage = V_{DD} + 4.2 V)
- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Discharge overcurrent control function

Release condition of discharge overcurrent status: Load disconnection, charger connection
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- Power-saving function: Available, unavailable
- PS pin internal resistance connection

| | |
|-------------------------|--------------------|
| In normal status: | Pull-up, pull-down |
| In power-saving status: | Pull-up, pull-down |
- PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)
- PS pin control logic: Active "H", active "L"
- High-withstand voltage: VM pin, CO pin and DO pin: absolute maximum rating 28 V
- Wide operation temperature range: Ta = -40°C to +85°C
- Low current consumption

| | |
|-----------------------|--------------------------------------|
| During operation: | 6.0 μA typ., 10 μA max. (Ta = +25°C) |
| During power-down: | 50 nA max. (Ta = +25°C) |
| During overdischarge: | 1.0 μA max. (Ta = +25°C) |
| During power-saving: | 50 nA max. (Ta = +25°C) |
- Lead-free, Sn100%, halogen-free^{*5}

- *1. Overcharge release voltage = Overcharge detection voltage - Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step)
- *2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step)
- *3. Overdischarge detection voltage - 0.25 V ≥ 0 V battery charge inhibition battery voltage
- *4. Overheat release temperature = Overheat detection temperature - 5°C or 10°C
- *5. Refer to "■ Product Name Structure" for details.

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Packages

- SNT-8A
- WLP-8V

■ **Block Diagram**

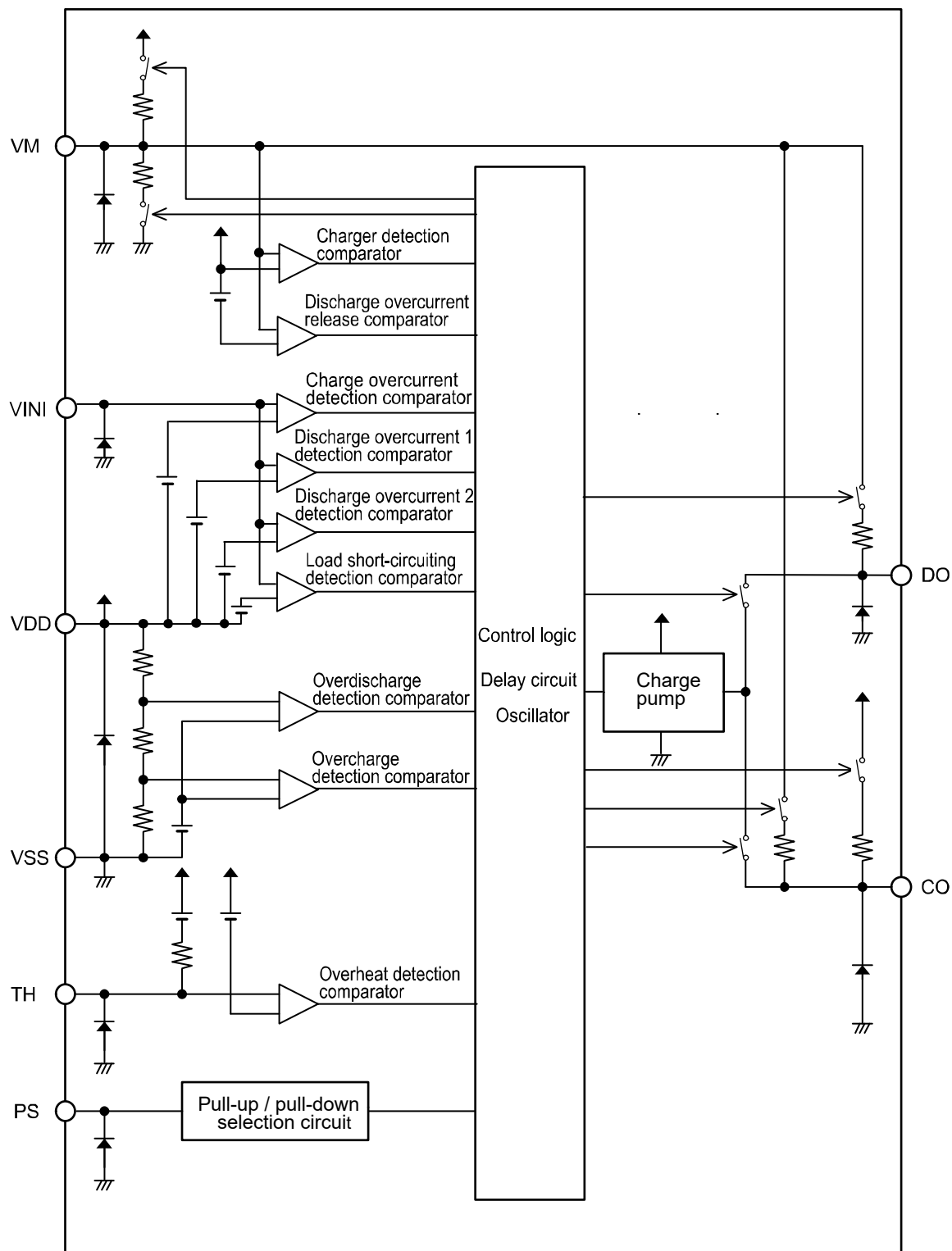
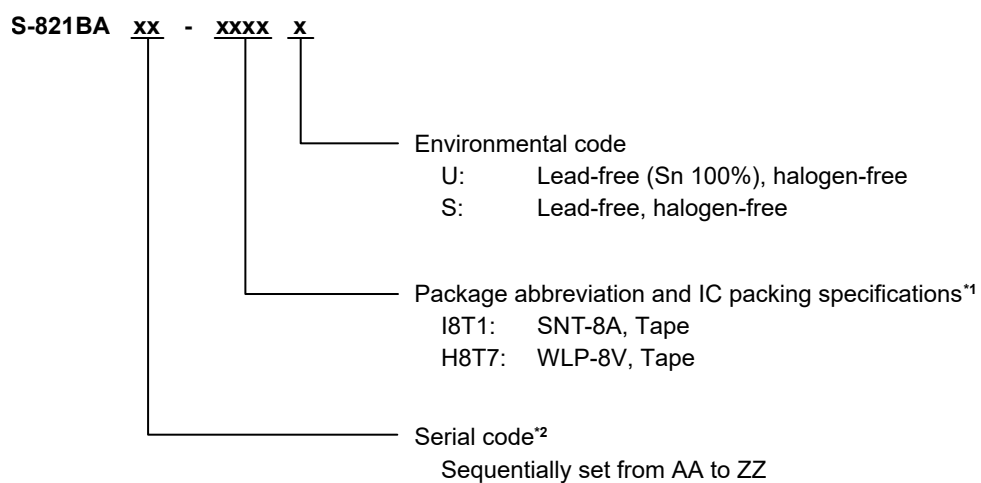


Figure 1

■ Product Name Structure

1. Product name



*1. Refer to the tape drawing.

*2. Refer to "3. Product name list".

2. Packages

Table 1 Package Drawing Codes

| Package Name | Dimension | Tape | Reel | Land |
|--------------|--------------|--------------|--------------|--------------|
| SNT-8A | PH008-A-P-SD | PH008-A-C-SD | PH008-A-R-SD | PH008-A-L-SD |
| WLP-8V | HV008-A-P-S2 | HV008-A-C-SD | HV008-A-R-SD | HV008-A-L-SD |

3. Product name list

3.1 WLP-8V

Table 2 (1 / 4)

| Product Name | Overcharge Detection Voltage [V _{CU}] | Overcharge Release Voltage [V _{CL}] | Overdischarge Detection Voltage [V _{DL}] | Overdischarge Release Voltage [V _{DU}] | Discharge Overcurrent 1 Detection Voltage [V _{DIOV1}] | Discharge Overcurrent 2 Detection Voltage [V _{DIOV2}] | Load Short- circuiting Detection Voltage [V _{SHORT}] | Charge Overcurrent Detection Voltage [V _{CIOV}] |
|-----------------|--|--|---|---|---|---|--|---|
| S-821BAAC-H8T7S | 4.590 V | 4.390 V | 2.500 V | 2.800 V | -5.8 mV | - | -20.5 mV | 20 mV |
| S-821BAAD-H8T7S | 4.620 V | 4.420 V | 2.300 V | 2.600 V | -5.8 mV | - | -20.5 mV | 20 mV |
| S-821BAAE-H8T7S | 4.540 V | 4.340 V | 2.500 V | 2.800 V | -7.5 mV | - | -25 mV | 14.5 mV |
| S-821BAAF-H8T7S | 4.590 V | 4.390 V | 2.300 V | 2.600 V | -7.5 mV | - | -25 mV | 14.5 mV |
| S-821BAAK-H8T7S | 4.625 V | 4.425 V | 2.500 V | 2.900 V | -5.6 mV | - | -22.5 mV | 18 mV |
| S-821BAAL-H8T7S | 4.660 V | 4.460 V | 2.300 V | 2.500 V | -5.6 mV | - | -26.25 mV | 18 mV |

Table 2 (2 / 4)

| Product Name | Delay Time Combination*1 | Release Condition of Discharge Overcurrent Status*2 | 0 V Battery Charge*3 | 0 V Battery Charge Inhibition Battery Voltage [V _{OINH}] | Power-down Function*4 |
|-----------------|-----------------------------|---|-------------------------|---|--------------------------|
| S-821BAAC-H8T7S | (1) | Load disconnection | Inhibited | 1.550 V | Unavailable |
| S-821BAAD-H8T7S | (2) | Load disconnection | Inhibited | 1.550 V | Unavailable |
| S-821BAAE-H8T7S | (1) | Load disconnection | Inhibited | 1.550 V | Unavailable |
| S-821BAAF-H8T7S | (2) | Load disconnection | Inhibited | 1.550 V | Unavailable |
| S-821BAAK-H8T7S | (3) | Load disconnection | Inhibited | 1.250 V | Available |
| S-821BAAL-H8T7S | (4) | Load disconnection | Inhibited | 1.250 V | Available |

Table 2 (3 / 4)

| Product Name | Overheat Detection Function*5 | Overheat Detection Temperature [T _{DET}] | Overheat Release Temperature [T _{REL}] | NTC Thermistor Resistance Value*6 [R _{NTC}] | B-constant*6 [B] |
|-----------------|----------------------------------|--|--|---|---------------------|
| S-821BAAC-H8T7S | Unavailable | - | - | - | - |
| S-821BAAD-H8T7S | Unavailable | - | - | - | - |
| S-821BAAE-H8T7S | Unavailable | - | - | - | - |
| S-821BAAF-H8T7S | Unavailable | - | - | - | - |
| S-821BAAK-H8T7S | Unavailable | - | - | - | - |
| S-821BAAL-H8T7S | Unavailable | - | - | - | - |

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S-821BA Series

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Table 2 (4 / 4)

| Product Name | Power-saving Function ^{*7} | PS Pin Control Logic ^{*8} | PS Pin Internal Resistance Connection ^{*9} | | PS Pin Internal Resistance ^{*10} [R _{PS}] | PS Pin Voltage "H" ^{*11} [V _{PSH}] | PS Pin Voltage "L" ^{*12} [V _{PSL}] |
|-----------------|-------------------------------------|------------------------------------|---|---------------------|---|--|--|
| | | | Normal Status | Power-saving Status | | | |
| S-821BAAC-H8T7S | Unavailable | - | - | - | - | - | - |
| S-821BAAD-H8T7S | Unavailable | - | - | - | - | - | - |
| S-821BAAE-H8T7S | Unavailable | - | - | - | - | - | - |
| S-821BAAF-H8T7S | Unavailable | - | - | - | - | - | - |
| S-821BAAK-H8T7S | Available | Active "H" | Pull-down | Pull-down | 5 MΩ | V _{SS} + 0.65 V | V _{SS} + 0.60 V |
| S-821BAAL-H8T7S | Available | Active "H" | Pull-down | Pull-down | 5 MΩ | V _{SS} + 0.65 V | V _{SS} + 0.60 V |

***1.** Refer to **Table 3** about the details of the delay time combinations.

***2.** Release condition of discharge overcurrent status: Load disconnection, charger connection.

***3.** 0 V battery charge: Enabled, inhibited.

***4.** Power-down function: Available, unavailable

***5.** Overheat detection function: Available, unavailable

***6.** Temperature detection accuracy varies with NTC thermistor specifications.

When an NTC thermistor listed in **Table 2 (3 / 4)** is connected, the detection temperature and accuracy can be achieved.

***7.** Power-saving function: Available, unavailable

***8.** PS pin control Logic: Active "H", active "L"

***9.** PS pin internal resistance connection: Pull-up, pull-down

***10.** PS pin internal resistance value: 1 MΩ to 10 MΩ (1 MΩ step)

***11.** PS pin voltage "H": V_{SS} + 0.65 V, V_{DD} - 0.90 V

***12.** PS pin voltage "L": V_{SS} + 0.60 V, V_{DD} - 0.90 V

Remark Please contact our sales representatives for products other than the above.

Caution Do not apply voltages exceeding the absolute maximum ratings shown in Table 7.

Table 3

| Delay Time Combination | Overcharge Detection Delay Time [t _{CU}] | Overdischarge Detection Delay Time [t _{DL}] | Discharge Overcurrent 1 Detection Delay Time [t _{DIOV1}] | Discharge Overcurrent 2 Detection Delay Time [t _{DIOV2}] | Load Short-circuiting Detection Delay Time [t _{SHORT}] | Charge Overcurrent Detection Delay Time [t _{CIOV}] | Overheat Detection Delay Time [t _{DET}] | Overheat Release Delay Time [t _{TREL}] | Power-saving Delay Time [t _{PS}] |
|------------------------|--|---|--|--|--|--|---|--|--|
| (1) | 512 ms | 64 ms | 128 ms | - | 280 μs | 32 ms | - | - | - |
| (2) | 1.0 s | 64 ms | 256 ms | - | 280 μs | 64 ms | - | - | - |
| (3) | 512 ms | 64 ms | 256 ms | - | 280 μs | 64 ms | - | - | 128 ms |
| (4) | 1.0 s | 64 ms | 512 ms | - | 280 μs | 128 ms | - | - | 256 ms |

Remark The delay times can be changed within the range listed in **Table 4**. For details, please contact our sales representatives.

Table 4

| Delay Time | Symbol | Selection Range | | | | | | Remark |
|--|--------------------|-----------------|--------|--------|--------|--------|--------|-------------------------------|
| Overcharge detection delay time | t _{CU} | 256 ms | 512 ms | 1.0 s | - | - | - | Select a value from the left. |
| Overdischarge detection delay time | t _{DL} | 32 ms | 64 ms | 128 ms | - | - | - | Select a value from the left. |
| Discharge overcurrent 1 detection delay time | t _{DIOV1} | 16 ms | 32 ms | 64 ms | 128 ms | 256 ms | 512 ms | Select a value from the left. |
| | | 1.0 s | 2.0 s | 3.0 s | 3.75 s | 4.0 s | - | |
| Discharge overcurrent 2 detection delay time | t _{DIOV2} | 16 ms | 32 ms | 64 ms | 128 ms | - | - | Select a value from the left. |
| Load short-circuiting detection delay time | t _{SHORT} | 280 μs | 530 μs | - | - | - | - | Select a value from the left. |
| Charge overcurrent detection delay time | t _{CIOV} | 16 ms | 32 ms | 64 ms | 128 ms | - | - | Select a value from the left. |
| Overheat detection delay time | t _{DET} | 256 ms | 512 ms | 1.0 s | - | - | - | Select a value from the left. |
| Overheat release delay time | t _{TREL} | 256 ms | - | - | - | - | - | Select a value from the left. |
| Power-saving delay time | t _{PS} | 16 ms | 32 ms | 64 ms | 128 ms | 256 ms | 512 ms | Select a value from the left. |

■ Pin Configuration

1. SNT-8A

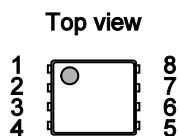


Figure 2

Table 5

| Pin No. | Symbol | Description |
|---------|--------|--|
| 1 | VDD | Input pin for positive power supply |
| 2 | CO | Connection pin of charge control FET gate (Charge pump output) |
| 3 | DO | Connection pin of discharge control FET gate (Charge pump output) |
| 4 | VM | Input pin for external positive voltage |
| 5 | VINI | Voltage detection pin between VINI pin and VDD pin (Overcurrent detection pin) |
| 6 | PS*1 | Input pin for power-saving |
| 7 | TH*2 | Thermistor connection pin |
| 8 | VSS | Input pin for negative power supply |

*1. If the power-saving function is unavailable, the PS pin must be left open.

*2. If the overheat detection function is unavailable, the TH pin must be connected to the VDD pin or the VSS pin.

2. WLP-8V

Bottom view

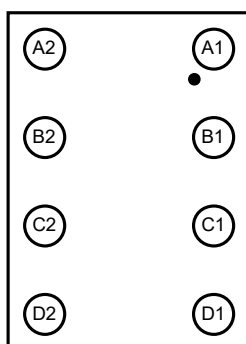


Figure 3

Table 6

| Pin No. | Symbol | Description |
|---------|--------|--|
| A1 | VSS | Input pin for negative power supply |
| A2 | VDD | Input pin for positive power supply |
| B1 | TH*2 | Thermistor connection pin |
| B2 | CO | Connection pin of charge control FET gate (Charge pump output) |
| C1 | PS*1 | Input pin for power-saving |
| C2 | DO | Connection pin of discharge control FET gate (Charge pump output) |
| D1 | VINI | Voltage detection pin between VINI pin and VDD pin (Overcurrent detection pin) |
| D2 | VM | Input pin for external positive voltage |

*1. If the power-saving function is unavailable, the PS pin must be left open.

*2. If the overheat detection function is unavailable, the TH pin must be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 7

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Applied Pin | Absolute Maximum Rating | Unit |
|---|-------------------|-------------|--|------|
| Input voltage between VDD pin and VSS pin | V _{DS} | VDD | V _{SS} - 0.3 to V _{SS} + 6.0 | V |
| VINI pin input voltage | V _{VINI} | VINI | V _{SS} - 0.3 to V _{DD} + 0.3 | V |
| VM pin input voltage | V _{VM} | VM | V _{SS} - 0.3 to V _{SS} + 28 | V |
| TH pin input voltage | V _{TH} | TH | V _{SS} - 0.3 to V _{DD} + 0.3 | V |
| PS pin input voltage | V _{PS} | PS | V _{SS} - 0.3 to V _{SS} + 6.0 | V |
| DO pin output voltage | V _{DO} | DO | V _{SS} - 0.3 to V _{SS} + 28 | V |
| CO pin output voltage | V _{CO} | CO | V _{SS} - 0.3 to V _{SS} + 28 | V |
| Operation ambient temperature | T _{opr} | - | -40 to +85 | °C |
| Storage temperature | T _{stg} | - | -55 to +125 | °C |

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 8

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|--|---------------|-----------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | θ_{JA} | SNT-8A | Board A | - | 211 | - | °C/W |
| | | | Board B | - | 173 | - | °C/W |
| | | | Board C | - | - | - | °C/W |
| | | | Board D | - | - | - | °C/W |
| | | | Board E | - | - | - | °C/W |

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

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■ Electrical Characteristics

1. Ta = +25°C

Table 9 (1 / 2)

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---------------------|---|---------------------------|------------------------|---------------------------|------|--------------|
| Detection Voltage | | | | | | | |
| Overcharge detection voltage | V _{CU} | - | V _{CU} - 0.015 | V _{CU} | V _{CU} + 0.015 | V | 1 |
| Overcharge release voltage | V _{CL} | V _{CL} ≠ V _{CU} | V _{CL} - 0.050 | V _{CL} | V _{CL} + 0.050 | V | 1 |
| | | V _{CL} = V _{CU} | V _{CL} - 0.020 | V _{CL} | V _{CL} + 0.015 | V | 1 |
| Overdischarge detection voltage | V _{DL} | - | V _{DL} - 0.050 | V _{DL} | V _{DL} + 0.050 | V | 2 |
| Overdischarge release voltage | V _{DU} | V _{DL} ≠ V _{DU} | V _{DU} - 0.075 | V _{DU} | V _{DU} + 0.075 | V | 2 |
| | | V _{DL} = V _{DU} | V _{DU} - 0.050 | V _{DU} | V _{DU} + 0.050 | V | 2 |
| Discharge overcurrent 1 detection voltage | V _{DIOV1} | - | V _{DIOV1} - 0.75 | V _{DIOV1} | V _{DIOV1} + 0.75 | mV | 2 |
| Discharge overcurrent 2 detection voltage | V _{DIOV2} | - | V _{DIOV2} - 2 | V _{DIOV2} | V _{DIOV2} + 2 | mV | 2 |
| Load short-circuiting detection voltage | V _{SHORT} | - | V _{SHORT} - 4 | V _{SHORT} | V _{SHORT} + 4 | mV | 2 |
| Load short-circuiting 2 detection voltage | V _{SHORT2} | - | V _{SS} + 0.3 | V _{SS} + 0.6 | V _{SS} + 1.0 | V | 2 |
| Charge overcurrent detection voltage | V _{CIOV} | - | V _{CIOV} - 0.75 | V _{CIOV} | V _{CIOV} + 0.75 | mV | 2 |
| Discharge overcurrent release voltage (Release condition of discharge overcurrent status "load disconnection") | V _{RIOV} | V _{DD} = 3.4 V | V _{DD} × 0.17 | V _{DD} × 0.20 | V _{DD} × 0.23 | V | 2 |
| Discharge overcurrent release voltage (Release condition of discharge overcurrent status "charger connection") | V _{DRIOV} | - | V _{DD} - 0.480 | V _{DD} - 0.4 | V _{DD} - 0.320 | V | 2 |
| PS pin voltage "H" | V _{PSH} | - | V _{PSH} - 0.4 | V _{PSH} | V _{PSH} + 0.4 | V | 1 |
| PS pin voltage "L" | V _{PSL} | - | V _{PSL} - 0.4 | V _{PSL} | V _{PSL} + 0.4 | V | 1 |
| Detection Temperature with an External NTC Thermistor | | | | | | | |
| Overheat detection temperature*1 | T _{DET} | - | T _{DET} - 3 | T _{DET} | T _{DET} + 3 | °C | 1 |
| Overheat release temperature*1 | T _{REL} | - | T _{REL} - 5 | T _{REL} | T _{REL} + 5 | °C | 1 |
| 0 V Battery Charge | | | | | | | |
| 0 V battery charge starting charger voltage | V _{0CHA} | 0 V battery charge enabled | 1.1 | - | - | V | 1 |
| 0 V battery charge inhibition battery voltage | V _{0INH} | 0 V battery charge inhibited (1.45 V ≤ V _{0INH} ≤ 2.00 V) | V _{0INH} - 0.05 | V _{0INH} | V _{0INH} + 0.05 | V | 1 |
| | | 0 V battery charge inhibited (V _{0INH} = 1.25 V) | V _{0INH} - 0.10 | V _{0INH} | V _{0INH} + 0.10 | V | 1 |
| Internal Resistance | | | | | | | |
| Resistance between VDD pin and VM pin | R _{VMD} | V _{DD} = 3.4 V, V _{VM} = 2.4 V | 5 | 15 | 30 | kΩ | 4 |
| Resistance between VM pin and VSS pin | R _{VMS} | V _{DD} = 1.8 V, V _{VM} = 1.8 V | 450 | 900 | 1800 | kΩ | 4 |
| Input Voltage | | | | | | | |
| Operation voltage between VDD pin and VSS pin | V _{DSOP1} | - | 1.5 | - | 6.0 | V | - |
| Operation voltage between VM pin and VSS pin | V _{DSOP2} | - | 1.5 | - | 28 | V | - |
| Input Current | | | | | | | |
| Current consumption during operation | I _{OPE} | V _{DD} = V _{VM} = 3.4 V | - | 6.0 | 10 | μA | 3 |
| Current consumption during power-down | I _{PDN} | V _{DD} = 1.5 V, V _{VM} = 0 V | - | - | 0.05 | μA | 3 |
| Current consumption during overdischarge | I _{OPEd} | V _{DD} = 1.5 V, V _{VM} = 0 V | - | - | 1.0 | μA | 3 |
| Current consumption during power-saving | I _{PS} | V _{DD} = 3.4 V, V _{VM} = 0 V | - | - | 0.05 | μA | 3 |

Table 9 (2 / 2)

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|--|--------------------|---|---------------------------|-----------------------|---------------------------|------|--------------|
| Output Voltage | | | | | | | |
| CO pin output voltage "H" | V _{COH} | V _{DD} = V _{VM} = 3.4 V, C _{CO} = 4.7 nF, I _{COU} T = 0 μA | V _{DD} + 4.0 | V _{DD} + 4.2 | V _{DD} + 4.4 | V | 2 |
| DO pin output voltage "H" | V _{DOH} | V _{DD} = V _{VM} = 3.4 V, C _{DO} = 4.7 nF, I _{DOU} T = 0 μA | V _{DD} + 4.0 | V _{DD} + 4.2 | V _{DD} + 4.4 | V | 2 |
| Output Resistance | | | | | | | |
| CO pin resistance "L" | R _{COL} | - | 1 | 2.5 | 5 | kΩ | 5 |
| DO pin resistance "L" | R _{DOL} | - | 1 | 2.5 | 5 | kΩ | 5 |
| Delay Time | | | | | | | |
| Overcharge detection delay time | t _{CU} | - | t _{CU} × 0.7 | t _{CU} | t _{CU} × 1.3 | - | 6 |
| Overdischarge detection delay time | t _{DL} | - | t _{DL} × 0.7 | t _{DL} | t _{DL} × 1.3 | - | 6 |
| Discharge overcurrent 1 detection delay time | t _{DIOV1} | - | t _{DIOV1} × 0.75 | t _{DIOV1} | t _{DIOV1} × 1.25 | - | 6 |
| Discharge overcurrent 2 detection delay time | t _{DIOV2} | - | t _{DIOV2} × 0.7 | t _{DIOV2} | t _{DIOV2} × 1.3 | - | 6 |
| Load short-circuiting detection delay time | t _{SHORT} | - | t _{SHORT} × 0.7 | t _{SHORT} | t _{SHORT} × 1.3 | - | 6 |
| Charge overcurrent detection delay time | t _{CIOV} | - | t _{CIOV} × 0.7 | t _{CIOV} | t _{CIOV} × 1.3 | - | 6 |
| Overheat detection delay time | t _{TDET} | - | t _{TDET} × 0.7 | t _{TDET} | t _{TDET} × 1.3 | - | 6 |
| Overheat release delay time | t _{TREL} | - | t _{TREL} × 0.6 | t _{TREL} | t _{TREL} × 1.4 | - | 6 |
| Power-saving delay time | t _{PS} | - | t _{PS} × 0.7 | t _{PS} | t _{PS} × 1.3 | - | 6 |

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

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2. Ta = -20°C to +60°C*1

Table 10 (1 / 2)

(Ta = -20°C to +60°C*1 unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---------------------|---|---------------------------|------------------------|---------------------------|------|--------------|
| Detection Voltage | | | | | | | |
| Overcharge detection voltage | V _{CU} | - | V _{CU} - 0.020 | V _{CU} | V _{CU} + 0.020 | V | 1 |
| Overcharge release voltage | V _{CL} | V _{CL} ≠ V _{CU} | V _{CL} - 0.065 | V _{CL} | V _{CL} + 0.057 | V | 1 |
| | | V _{CL} = V _{CU} | V _{CL} - 0.025 | V _{CL} | V _{CL} + 0.020 | V | 1 |
| Overdischarge detection voltage | V _{DL} | - | V _{DL} - 0.060 | V _{DL} | V _{DL} + 0.055 | V | 2 |
| Overdischarge release voltage | V _{DU} | V _{DL} ≠ V _{DU} | V _{DU} - 0.085 | V _{DU} | V _{DU} + 0.080 | V | 2 |
| | | V _{DL} = V _{DU} | V _{DU} - 0.060 | V _{DU} | V _{DU} + 0.055 | V | 2 |
| Discharge overcurrent 1 detection voltage | V _{DIOV1} | - | V _{DIOV1} - 1.25 | V _{DIOV1} | V _{DIOV1} + 1.25 | mV | 2 |
| Discharge overcurrent 2 detection voltage | V _{DIOV2} | - | V _{DIOV2} - 2 | V _{DIOV2} | V _{DIOV2} + 2 | mV | 2 |
| Load short-circuiting detection voltage | V _{SHORT} | - | V _{SHORT} - 4 | V _{SHORT} | V _{SHORT} + 4 | mV | 2 |
| Load short-circuiting 2 detection voltage | V _{SHORT2} | - | V _{SS} + 0.1 | V _{SS} + 0.6 | V _{SS} + 1.2 | V | 2 |
| Charge overcurrent detection voltage | V _{CIOV} | - | V _{CIOV} - 1.25 | V _{CIOV} | V _{CIOV} + 1.25 | mV | 2 |
| Discharge overcurrent release voltage (Release condition of discharge overcurrent status "load disconnection") | V _{RIOV} | V _{DD} = 3.4 V | V _{DD} × 0.17 | V _{DD} × 0.20 | V _{DD} × 0.23 | V | 2 |
| Discharge overcurrent release voltage (Release condition of discharge overcurrent status "charger connection") | V _{DRIOV} | - | V _{DD} - 0.550 | V _{DD} - 0.4 | V _{DD} - 0.250 | V | 2 |
| PS pin voltage "H" | V _{PSH} | - | V _{PSH} - 0.5 | V _{PSH} | V _{PSH} + 0.5 | V | 1 |
| PS pin voltage "L" | V _{PSL} | - | V _{PSL} - 0.5 | V _{PSL} | V _{PSL} + 0.5 | V | 1 |
| Detection Temperature with an External NTC Thermistor | | | | | | | |
| Overheat detection temperature*1 | T _{DET} | - | T _{DET} - 3 | T _{DET} | T _{DET} + 3 | °C | 1 |
| Overheat release temperature*1 | T _{REL} | - | T _{REL} - 5 | T _{REL} | T _{REL} + 5 | °C | 1 |
| 0 V Battery Charge | | | | | | | |
| 0 V battery charge starting charger voltage | V _{0CHA} | 0 V battery charge enabled | 1.5 | - | - | V | 1 |
| 0 V battery charge inhibition battery voltage | V _{0INH} | 0 V battery charge inhibited (1.45 V ≤ V _{0INH} ≤ 2.00 V) | V _{0INH} - 0.05 | V _{0INH} | V _{0INH} + 0.05 | V | 1 |
| | | 0 V battery charge inhibited (V _{0INH} = 1.25 V) | V _{0INH} - 0.10 | V _{0INH} | V _{0INH} + 0.10 | V | 1 |
| Internal Resistance | | | | | | | |
| Resistance between VDD pin and VM pin | R _{VMD} | V _{DD} = 3.4 V, V _{VM} = 2.4 V | 3 | 15 | 35 | kΩ | 4 |
| Resistance between VM pin and VSS pin | R _{VMS} | V _{DD} = 1.8 V, V _{VM} = 1.8 V | 300 | 900 | 2200 | kΩ | 4 |
| Input Voltage | | | | | | | |
| Operation voltage between VDD pin and VSS pin | V _{DSOP1} | - | 1.5 | - | 6.0 | V | - |
| Operation voltage between VM pin and VSS pin | V _{DSOP2} | - | 1.5 | - | 28 | V | - |
| Input Current | | | | | | | |
| Current consumption during operation | I _{OP} | V _{DD} = V _{VM} = 3.4 V | - | 6.0 | 12 | μA | 3 |
| Current consumption during power-down | I _{PDN} | V _{DD} = 1.5 V, V _{VM} = 0 V | - | - | 0.1 | μA | 3 |
| Current consumption during overdischarge | I _{OPED} | V _{DD} = 1.5 V, V _{VM} = 0 V | - | - | 1.1 | μA | 3 |
| Current consumption during power-saving | I _{PS} | V _{DD} = 3.4 V, V _{VM} = 0 V | - | - | 0.1 | μA | 3 |

Table 10 (2 / 2)

(Ta = -20°C to +60°C*1 unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|--|--------------------|---|---------------------------|-----------------------|---------------------------|------|--------------|
| Output Voltage | | | | | | | |
| CO pin output voltage "H" | V _{COH} | V _{DD} = V _{VM} = 3.4 V, C _{CO} = 4.7 nF, I _{COOUT} = 0 μA | V _{DD} + 4.0 | V _{DD} + 4.2 | V _{DD} + 4.4 | V | 2 |
| DO pin output voltage "H" | V _{DOH} | V _{DD} = V _{VM} = 3.4 V, C _{DO} = 4.7 nF, I _{DOOUT} = 0 μA | V _{DD} + 4.0 | V _{DD} + 4.2 | V _{DD} + 4.4 | V | 2 |
| Output Resistance | | | | | | | |
| CO pin resistance "L" | R _{COL} | - | 1 | 2.5 | 7.5 | kΩ | 5 |
| DO pin resistance "L" | R _{DOL} | - | 1 | 2.5 | 7.5 | kΩ | 5 |
| Delay Time | | | | | | | |
| Overcharge detection delay time | t _{CU} | - | t _{CU} × 0.6 | t _{CU} | t _{CU} × 1.4 | - | 6 |
| Overdischarge detection delay time | t _{DL} | - | t _{DL} × 0.6 | t _{DL} | t _{DL} × 1.4 | - | 6 |
| Discharge overcurrent 1 detection delay time | t _{DIOV1} | - | t _{DIOV1} × 0.65 | t _{DIOV1} | t _{DIOV1} × 1.35 | - | 6 |
| Discharge overcurrent 2 detection delay time | t _{DIOV2} | - | t _{DIOV2} × 0.6 | t _{DIOV2} | t _{DIOV2} × 1.4 | - | 6 |
| Load short-circuiting detection delay time | t _{SHORT} | - | t _{SHORT} × 0.6 | t _{SHORT} | t _{SHORT} × 1.4 | - | 6 |
| Charge overcurrent detection delay time | t _{CIOV} | - | t _{CIOV} × 0.6 | t _{CIOV} | t _{CIOV} × 1.4 | - | 6 |
| Overheat detection delay time | t _{TDET} | - | t _{TDET} × 0.6 | t _{TDET} | t _{TDET} × 1.4 | - | 6 |
| Overheat release delay time | t _{TREL} | - | t _{TREL} × 0.5 | t _{TREL} | t _{TREL} × 1.5 | - | 6 |
| Power-saving delay time | t _{PS} | - | t _{PS} × 0.6 | t _{PS} | t _{PS} × 1.4 | - | 6 |

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

BATTERY PROTECTION IC FOR 1-CELL PACK

S-821BA Series

Rev.1.2_00

3. Ta = -40°C to +85°C*1

Table 11 (1 / 2)

(Ta = -40°C to +85°C*1 unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---------------------|---|---------------------------|------------------------|---------------------------|------|--------------|
| Detection Voltage | | | | | | | |
| Overcharge detection voltage | V _{CU} | - | V _{CU} - 0.045 | V _{CU} | V _{CU} + 0.030 | V | 1 |
| Overcharge release voltage | V _{CL} | V _{CL} ≠ V _{CU} | V _{CL} - 0.080 | V _{CL} | V _{CL} + 0.060 | V | 1 |
| | | V _{CL} = V _{CU} | V _{CL} - 0.050 | V _{CL} | V _{CL} + 0.030 | V | 1 |
| Overdischarge detection voltage | V _{DL} | - | V _{DL} - 0.080 | V _{DL} | V _{DL} + 0.060 | V | 2 |
| Overdischarge release voltage | V _{DU} | V _{DL} ≠ V _{DU} | V _{DU} - 0.105 | V _{DU} | V _{DU} + 0.085 | V | 2 |
| | | V _{DL} = V _{DU} | V _{DU} - 0.080 | V _{DU} | V _{DU} + 0.060 | V | 2 |
| Discharge overcurrent 1 detection voltage | V _{DIOV1} | - | V _{DIOV1} - 1.25 | V _{DIOV1} | V _{DIOV1} + 1.25 | mV | 2 |
| Discharge overcurrent 2 detection voltage | V _{DIOV2} | - | V _{DIOV2} - 2 | V _{DIOV2} | V _{DIOV2} + 2 | mV | 2 |
| Load short-circuiting detection voltage | V _{SHORT} | - | V _{SHORT} - 4 | V _{SHORT} | V _{SHORT} + 4 | mV | 2 |
| Load short-circuiting 2 detection voltage | V _{SHORT2} | - | V _{SS} + 0.1 | V _{SS} + 0.6 | V _{SS} + 1.2 | V | 2 |
| Charge overcurrent detection voltage | V _{CIOV} | - | V _{CIOV} - 1.25 | V _{CIOV} | V _{CIOV} + 1.25 | mV | 2 |
| Discharge overcurrent release voltage (Release condition of discharge overcurrent status "load disconnection") | V _{RIOV} | V _{DD} = 3.4 V | V _{DD} × 0.17 | V _{DD} × 0.20 | V _{DD} × 0.23 | V | 2 |
| Discharge overcurrent release voltage (Release condition of discharge overcurrent status "charger connection") | V _{DRIOV} | - | V _{DD} - 0.600 | V _{DD} - 0.4 | V _{DD} - 0.200 | V | 2 |
| PS pin voltage "H" | V _{PSH} | - | V _{PSH} - 0.5 | V _{PSH} | V _{PSH} + 0.5 | V | 1 |
| PS pin voltage "L" | V _{PSL} | - | V _{PSL} - 0.5 | V _{PSL} | V _{PSL} + 0.5 | V | 1 |
| Detection Temperature with an External NTC Thermistor | | | | | | | |
| Overheat detection temperature*1 | T _{DET} | - | T _{DET} - 3 | T _{DET} | T _{DET} + 3 | °C | 1 |
| Overheat release temperature*1 | T _{REL} | - | T _{REL} - 5 | T _{REL} | T _{REL} + 5 | °C | 1 |
| 0 V Battery Charge | | | | | | | |
| 0 V battery charge starting charger voltage | V _{0CHA} | 0 V battery charge enabled | 1.5 | - | - | V | 1 |
| 0 V battery charge inhibition battery voltage | V _{0INH} | 0 V battery charge inhibited (1.45 V ≤ V _{0INH} ≤ 2.00 V) | V _{0INH} - 0.15 | V _{0INH} | V _{0INH} + 0.15 | V | 1 |
| | | 0 V battery charge inhibited (V _{0INH} = 1.25 V) | V _{0INH} - 0.20 | V _{0INH} | V _{0INH} + 0.20 | V | 1 |
| Internal Resistance | | | | | | | |
| Resistance between VDD pin and VM pin | R _{VMD} | V _{DD} = 3.4 V, V _{VM} = 2.4 V | 2 | 15 | 40 | kΩ | 4 |
| Resistance between VM pin and VSS pin | R _{VMS} | V _{DD} = 1.8 V, V _{VM} = 1.8 V | 200 | 900 | 2400 | kΩ | 4 |
| Input Voltage | | | | | | | |
| Operation voltage between VDD pin and VSS pin | V _{DSOP1} | - | 1.5 | - | 6.0 | V | - |
| Operation voltage between VM pin and VSS pin | V _{DSOP2} | - | 1.5 | - | 28 | V | - |
| Input Current | | | | | | | |
| Current consumption during operation | I _{OP} | V _{DD} = V _{VM} = 3.4 V | - | 6.0 | 14 | μA | 3 |
| Current consumption during power-down | I _{PDN} | V _{DD} = 1.5 V, V _{VM} = 0 V | - | - | 0.5 | μA | 3 |
| Current consumption during overdischarge | I _{OPED} | V _{DD} = 1.5 V, V _{VM} = 0 V | - | - | 1.2 | μA | 3 |
| Current consumption during power-saving | I _{PS} | V _{DD} = 3.4 V, V _{VM} = 0 V | - | - | 0.5 | μA | 3 |

Table 11 (2 / 2)

(Ta = -40°C to +85°C*1 unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|--|--------------------|---|--------------------------|-----------------------|--------------------------|------|--------------|
| Output Voltage | | | | | | | |
| CO pin output voltage "H" | V _{COH} | V _{DD} = V _{VM} = 3.4 V, C _{CO} = 4.7 nF, I _{COOUT} = 0 μA | V _{DD} + 4.0 | V _{DD} + 4.2 | V _{DD} + 4.4 | V | 2 |
| DO pin output voltage "H" | V _{DOH} | V _{DD} = V _{VM} = 3.4 V, C _{DO} = 4.7 nF, I _{DOOUT} = 0 μA | V _{DD} + 4.0 | V _{DD} + 4.2 | V _{DD} + 4.4 | V | 2 |
| Output Resistance | | | | | | | |
| CO pin resistance "L" | R _{COL} | - | 1 | 2.5 | 7.5 | kΩ | 5 |
| DO pin resistance "L" | R _{DOL} | - | 1 | 2.5 | 7.5 | kΩ | 5 |
| Delay Time | | | | | | | |
| Overcharge detection delay time | t _{CU} | - | t _{CU} × 0.4 | t _{CU} | t _{CU} × 1.6 | - | 6 |
| Overdischarge detection delay time | t _{DL} | - | t _{DL} × 0.4 | t _{DL} | t _{DL} × 1.6 | - | 6 |
| Discharge overcurrent 1 detection delay time | t _{DIOV1} | - | t _{DIOV1} × 0.4 | t _{DIOV1} | t _{DIOV1} × 1.6 | - | 6 |
| Discharge overcurrent 2 detection delay time | t _{DIOV2} | - | t _{DIOV2} × 0.4 | t _{DIOV2} | t _{DIOV2} × 1.6 | - | 6 |
| Load short-circuiting detection delay time | t _{SHORT} | - | t _{SHORT} × 0.4 | t _{SHORT} | t _{SHORT} × 1.6 | - | 6 |
| Charge overcurrent detection delay time | t _{CIOV} | - | t _{CIOV} × 0.4 | t _{CIOV} | t _{CIOV} × 1.6 | - | 6 |
| Overheat detection delay time | t _{TDET} | - | t _{TDET} × 0.4 | t _{TDET} | t _{TDET} × 1.6 | - | 6 |
| Overheat release delay time | t _{TREL} | - | t _{TREL} × 0.3 | t _{TREL} | t _{TREL} × 1.7 | - | 6 |
| Power-saving delay time | t _{PS} | - | t _{PS} × 0.4 | t _{PS} | t _{PS} × 1.6 | - | 6 |

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

- Caution**
1. Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{DD} and the DO pin level with respect to V_{VM} .
 2. Unless otherwise specified, V6 and SW3 should be as follows.
 - With power-saving function and Active "H": SW3 = ON, V6 = 0 V
 - With power-saving function and Active "L": SW3 = ON, V6 = V1
 - Without power-saving function: SW3 = OFF, or SW3 = ON and V6 = V1

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

1.1 $V_{CU} \neq V_{CL}$

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = 3.4 V, V2 = 0 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL} .

1.2 $V_{CU} = V_{CL}$

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = 3.4 V, V2 = 0 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when setting V2 = -0.5 V and when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL} .

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased after setting V1 = 3.4 V, V2 = V5 = 0 V.

Overdischarge release voltage (V_{DU}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when setting V2 = -0.01 V, V5 = 0 V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL} .

3. Discharge overcurrent 1 detection voltage, discharge overcurrent release voltage (Test circuit 2)

Discharge overcurrent 1 detection voltage (V_{DIOV1}) is defined as the voltage V5 at which delay time from when V5 is decreased after setting V1 = 3.4 V, V2 = -1.4 V, V5 = 0 V to when V_{DO} goes from "H" to "L" is discharge overcurrent detection 1 delay time (t_{DIOV1}).

Discharge overcurrent release voltage (V_{RIOV} or V_{DRIOV}) is defined as the voltage V1 + V2 at which V_{DO} goes from "L" to "H" when setting V2 = -3.4 V, V5 = 0 V and when the voltage V2 is then gradually increased.

When the voltage V2 exceeds V_{RIOV} , V_{DO} will go to "H" after 2.0 ms typ. and maintain "H" during load short-circuiting detection delay time (t_{SHORT}).

4. Discharge overcurrent 2 detection voltage (Test circuit 2)

Discharge overcurrent 2 detection voltage (V_{DIOV2}) is defined as the voltage V5 at which delay time from when V5 is decreased after setting V1 = 3.4 V, V2 = -1.4 V, V5 = 0 V to when V_{DO} goes from "H" to "L" is discharge overcurrent 2 detection delay time (t_{DIOV2}).

5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V5 at which delay time from when V5 is decreased after setting V1 = 3.4 V, V2 = -1.4 V, V5 = 0 V to when V_{DO} goes from "H" to "L" is t_{SHORT} .

6. Load short-circuiting 2 detection voltage
(Test circuit 2)

Load short-circuiting 2 detection voltage (V_{SHORT2}) is defined as the voltage $V1 + V2$ at which delay time from when $V2$ is decreased after setting $V1 = 3.4 \text{ V}$, $V2 = V5 = 0 \text{ V}$ to when V_{DO} goes from "H" to "L" is t_{SHORT} .

7. Charge overcurrent detection voltage
(Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage $V5$ at which delay time from when the voltage $V5$ is increased after setting $V1 = 3.4 \text{ V}$, $V2 = V5 = 0 \text{ V}$ to when V_{CO} goes from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}).

8. Overheat detection temperature, overheat release temperature
(Test Circuit 1)

8. 1 NTC thermistor resistance value ($R_{\text{NTC}} = 100 \text{ k}\Omega$ (25°C))

After setting $V1 = 3.4 \text{ V}$, $V2 = 0 \text{ V}$, $R2 = 100 \text{ k}\Omega$, decrease $R2$ gradually, and then substitute $R2$ when V_{CO} and V_{DO} go from "H" to "L" into equation (1).

Temperature T [$^\circ\text{C}$] obtained from the calculation result is defined as overheat detection temperature (T_{DET}).

After setting $V1 = 3.4 \text{ V}$, $V2 = 0 \text{ V}$, $R2 = 5 \text{ k}\Omega$, increase $R2$ gradually, and then substitute $R2$ when V_{CO} and V_{DO} go from "L" to "H" into equation (1).

Temperature T [$^\circ\text{C}$] obtained from the calculation result is defined as overheat release temperature (T_{REL}).

8. 2 NTC thermistor resistance value ($R_{\text{NTC}} = 470 \text{ k}\Omega$ (25°C))

After setting $V1 = 3.4 \text{ V}$, $V2 = 0 \text{ V}$, $R2 = 470 \text{ k}\Omega$, decrease $R2$ gradually, and then substitute $R2$ when V_{CO} and V_{DO} go from "H" to "L" into equation (1).

Temperature T [$^\circ\text{C}$] obtained from the calculation result is defined as overheat detection temperature (T_{DET}).

After setting $V1 = 3.4 \text{ V}$, $V2 = 0 \text{ V}$, $R2 = 25 \text{ k}\Omega$, increase $R2$ gradually, and then substitute $R2$ when V_{CO} and V_{DO} go from "L" to "H" into equation (1).

Temperature T [$^\circ\text{C}$] obtained from the calculation result is defined as overheat release temperature (T_{REL}).

$$T \text{ [}^\circ\text{C]} = \frac{1}{\frac{1}{B \text{ [K]} \times \log_e \left(\frac{R_2}{R_{\text{NTC}}} \right)} + \frac{1}{25 \text{ [}^\circ\text{C]} + 273.15}} - 273.15 \dots\dots\dots (1)$$

- Remark**
1. R_{NTC} : $100 \text{ k}\Omega$ or $470 \text{ k}\Omega$
 2. B : NTC thermistor B-constant

9. PS pin voltage "H", PS pin voltage "L"
(Test Circuit 1)

9. 1 PS pin control logic active "H"

The PS pin voltage "H" (V_{PSH}) is defined as the voltage $V6$ at which V_{CO} and V_{DO} go from "H" to "L" when the voltage $V6$ is gradually increased after setting $V1 = 3.4 \text{ V}$, $V2 = V6 = 0 \text{ V}$, $\text{SW3} = \text{ON}$.

After that, the PS pin voltage "L" (V_{PSL}) is defined as the voltage $V6$ at which V_{CO} and V_{DO} go from "L" to "H" after $V6$ is gradually decreased.

9. 2 PS pin control logic active "L"

The PS pin voltage "L" (V_{PSL}) is defined as the voltage $V6$ at which V_{CO} and V_{DO} go from "H" to "L" when the voltage $V6$ is gradually decreased after setting $V1 = V6 = 3.4 \text{ V}$, $V2 = 0 \text{ V}$, $\text{SW3} = \text{ON}$.

After that, the PS pin voltage "H" (V_{PSH}) is defined as the voltage $V6$ at which V_{CO} and V_{DO} go from "L" to "H" after $V6$ is gradually increased.

10. Current consumption during operation
(Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of $V1 = V2 = V5 = 3.4\text{ V}$.

11. Current consumption during power-down, current consumption during overdischarge
(Test circuit 3)**11. 1 With power-down function**

The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of $V1 = V5 = 1.5\text{ V}$, $V2 = 0\text{ V}$.

11. 2 Without power-down function

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set conditions of $V1 = V5 = 1.5\text{ V}$, $V2 = 0\text{ V}$.

12. Current consumption during power-saving
(Test circuit 3)**12. 1 PS pin control logic active "H"**

The current consumption during power-saving (I_{PS}) is I_{DD} under the set conditions of $V1 = V5 = V6 = 3.4\text{ V}$, $V2 = 0\text{ V}$, $SW3 = \text{ON}$.

12. 2 PS pin control logic active "L"

The current consumption during power-saving (I_{PS}) is I_{DD} under the set conditions of $V1 = V5 = 3.4\text{ V}$, $V2 = V6 = 0\text{ V}$, $SW3 = \text{ON}$.

13. Resistance between VDD pin and VM pin
(Test circuit 4)

R_{VMD} is the resistance between VDD pin and VM pin under the set conditions of $V1 = 3.4\text{ V}$, $V2 = V5 = 2.4\text{ V}$.

14. Resistance between VM pin and VSS pin
(Test circuit 4)

R_{VMS} is the resistance between VM pin and VSS pin under the set conditions of $V1 = V2 = V5 = 1.8\text{ V}$.

15. CO pin output voltage "H"
(Test circuit 2)

The CO pin output voltage "H" (V_{COH}) is the average voltage V_{CO} under the set conditions of $V1 = 3.4\text{ V}$, $V2 = V5 = 0\text{ V}$.

16. DO pin output voltage "H"
(Test circuit 2)

The DO pin output voltage "H" (V_{DOH}) is the average voltage V_{DO} under the set conditions of $V1 = 3.4\text{ V}$, $V2 = V5 = 0\text{ V}$.

17. CO pin resistance "L"
(Test circuit 5)

The CO pin resistance "L" (R_{COL}) is the resistance between VDD pin and CO pin under the set conditions of $V1 = V2 = V5 = 4.7\text{ V}$, $V3 = 5.1\text{ V}$, $SW1 = \text{ON}$, $SW2 = \text{OFF}$.

18. DO pin resistance "L"
(Test circuit 5)

The DO pin resistance "L" (R_{DOL}) is the resistance between VM pin and DO pin under the set conditions of $V1 = V2 = V5 = 1.8\text{ V}$, $V4 = 2.2\text{ V}$, $SW1 = \text{OFF}$, $SW2 = \text{ON}$.

19. Overcharge detection delay time
(Test circuit 6)

After setting $V1 = 3.4\text{ V}$, $V2 = V5 = 0\text{ V}$, the voltage $V1$ is increased. The time interval from when the voltage $V1$ exceeds V_{CU} until V_{CO} goes to "L" is the overcharge detection delay time (t_{CU}).

20. Overdischarge detection delay time
(Test circuit 6)

After setting $V1 = 3.4\text{ V}$, $V2 = V5 = 0\text{ V}$, the voltage $V1$ is decreased. The time interval from when the voltage $V1$ falls below V_{DL} until V_{DO} goes to "L" is the overdischarge detection delay time (t_{DL}).

21. Discharge overcurrent 1 detection delay time
(Test circuit 6)

After setting $V1 = 3.4\text{ V}$, $V2 = -1.4\text{ V}$, $V5 = 0\text{ V}$, the voltage $V5$ is decreased. The time interval from when the voltage $V5$ falls below V_{DIOV1} until V_{DO} goes to "L" is the discharge overcurrent 1 detection delay time (t_{DIOV1}).

22. Discharge overcurrent 2 detection delay time
(Test circuit 6)

After setting $V1 = 3.4\text{ V}$, $V2 = -1.4\text{ V}$, $V5 = 0\text{ V}$, the voltage $V5$ is decreased. The time interval from when the voltage $V5$ falls below V_{DIOV2} until V_{DO} goes to "L" is the discharge overcurrent 2 detection delay time (t_{DIOV2}).

23. Load short-circuiting detection delay time
(Test circuit 6)

After setting $V1 = 3.4\text{ V}$, $V2 = -1.4\text{ V}$, $V5 = 0\text{ V}$, the voltage $V5$ is decreased. The time interval from when the voltage $V5$ falls below V_{SHORT} until V_{DO} goes to "L" is the load short-circuiting detection delay time (t_{SHORT}).

24. Charge overcurrent detection delay time
(Test circuit 6)

After setting $V1 = 3.4\text{ V}$, $V2 = V5 = 0\text{ V}$, the voltage $V5$ is increased. The time interval from when the voltage $V5$ exceeds V_{CIOV} until V_{CO} goes to "L" is the charge overcurrent detection delay time (t_{CIOV}).

25. Overheat detection delay time, overheat release delay time (Test Circuit 6)

The overheat detection delay time (t_{DET}) is the time from when this IC enters awake mode until V_{CO} and V_{DO} go to "L" after the resistance R_2 decreases and falls below R_{TDET}^*1 under the set condition of $V_1 = 3.4 \text{ V}$, $V_2 = V_5 = 0 \text{ V}$.

The overheat release delay time (t_{REL}) is the time from when this IC enters awake mode until V_{CO} and V_{DO} go to "H" after the resistance R_2 increases.

$$R_{\text{TDET}} = R_{\text{NTC}} \bullet \exp \left\{ B [\text{K}] \left(\frac{1}{T_{\text{DET}} [^{\circ}\text{C}] + 273.15} - \frac{1}{25 [^{\circ}\text{C}] + 273.15} \right) \right\} \dots\dots\dots (2)$$

*1. R_{TDET} is calculated by the formula (2) using the overheat detection temperature (T_{DET}).

Remark 1. R_{NTC} : 100 k Ω or 470 k Ω
2. B: NTC thermistor B-constant

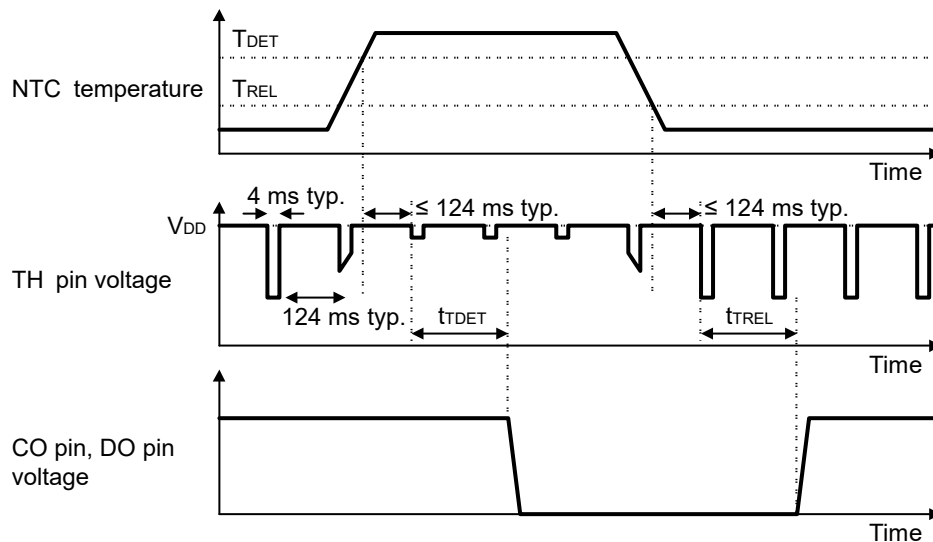


Figure 4

26. Power-saving delay time (Test Circuit 6)

26. 1 PS pin control logic active "H"

After setting $V_1 = 3.4 \text{ V}$, $V_2 = V_5 = V_6 = 0 \text{ V}$, $\text{SW3} = \text{ON}$, the voltage V_6 is increased. The time interval from when the voltage V_6 exceeds V_{PSH} until V_{CO} and V_{DO} go to "L" is the power-saving delay time (t_{PS}).

26. 2 PS pin control logic active "L"

After setting $V_1 = V_6 = 3.4 \text{ V}$, $V_2 = V_5 = 0 \text{ V}$, $\text{SW3} = \text{ON}$, the voltage V_6 is decreased. The time interval from when the voltage V_6 falls below V_{PSL} until V_{CO} and V_{DO} go to "L" is the power-saving delay time (t_{PS}).

27. 0 V battery charge starting charger voltage (0 V battery charge enabled) (Test circuit 1)

The 0 V battery charge starting charger voltage ($V_{0\text{CHA}}$) is defined as the voltage V_2 at which V_{CO} goes to "H" ($V_{\text{CO}} = V_{\text{VM}}$) when the voltage V_2 is gradually increased after setting $V_1 = V_2 = V_5 = 0 \text{ V}$.

28. 0 V battery charge inhibition battery voltage (0 V battery charge inhibited) (Test circuit 1)

The 0 V battery charge inhibition battery voltage ($V_{0\text{INH}}$) is defined as the voltage V_1 at which V_{CO} goes to "L" when the voltage V_1 is gradually decreased after setting $V_1 = V_5 = 1.8 \text{ V}$, $V_2 = 1.0 \text{ V}$, $V_5 = 0 \text{ V}$.

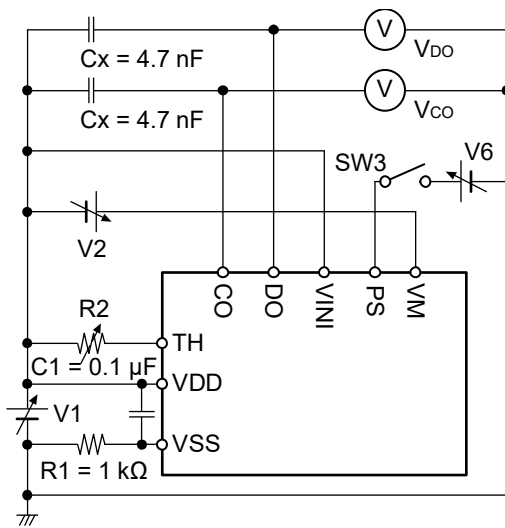


Figure 5 Test Circuit 1

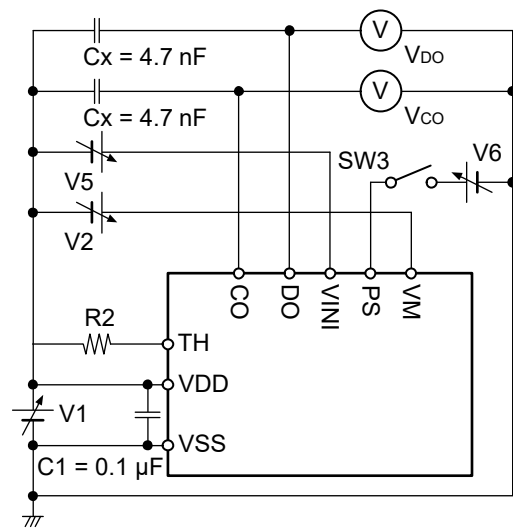


Figure 6 Test Circuit 2

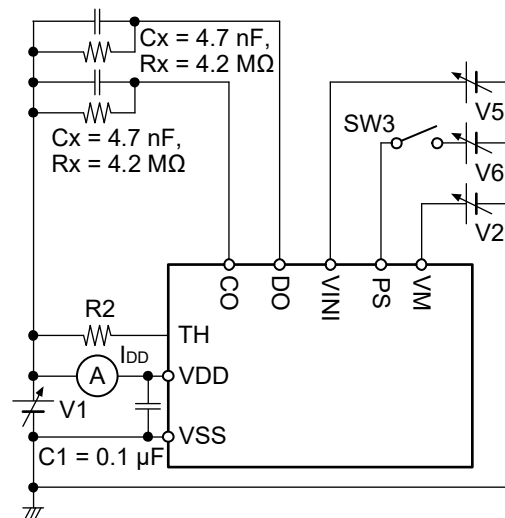


Figure 7 Test Circuit 3

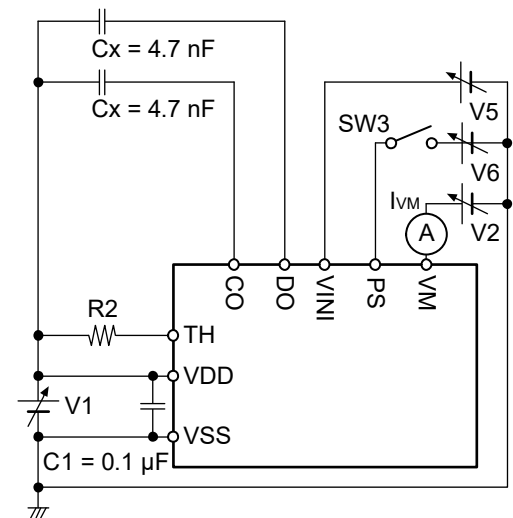


Figure 8 Test Circuit 4

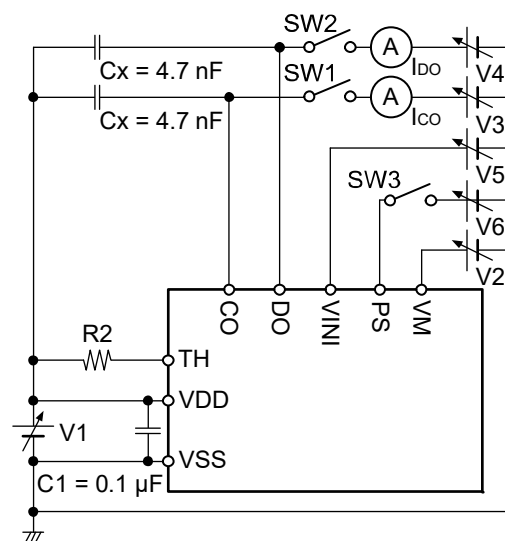


Figure 9 Test Circuit 5

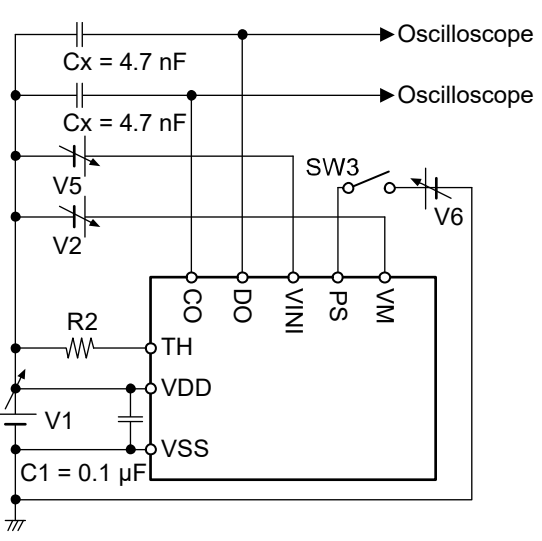


Figure 10 Test Circuit 6

■ Operation

Remark Refer to "■ Battery Protection IC Connection Example".

1. Normal status

This IC monitors the voltage of the battery connected between VDD pin and VSS pin and the voltage between VINI pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), and the VINI pin voltage is in the range from discharge overcurrent 1 detection voltage (V_{DIOV1}) to charge overcurrent detection voltage (V_{CIOV}), both charge and discharge control FETs are turned on. This status is called the normal status, and in this condition charging and discharging can be carried out freely.

The resistance between VDD pin and VM pin (R_{VMD}), and the resistance between VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

Caution After a battery is connected, there may be cases when discharging cannot be performed. In this case, this IC returns to the normal status by connecting a charger.

2. Overcharge status

2.1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the charge control FET is turned off and charging is stopped. This status is called the overcharge status.

The overcharge status is released in the following two cases.

- (1) In the case that the VM pin voltage is equal to or higher than $V_{DD} - 0.4 \text{ V typ.}$, this IC releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
- (2) In the case that the VM pin voltage is equal to or lower than $V_{DD} - 0.4 \text{ V typ.}$, this IC releases the overcharge status when the battery voltage falls below overcharge detection voltage (V_{CU}).

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage falls by the V_f voltage of the internal parasitic diode than the VDD pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or lower than $V_{DD} - 0.4 \text{ V typ.}$, this IC releases the overcharge status when the battery voltage is equal to or lower than V_{CU} .

Caution If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection does not function until the battery voltage falls below V_{CU} . Since an actual battery has an internal impedance of tens of m Ω , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection function.

2.2 $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for t_{CU} or longer, the charge control FET is turned off and charging is stopped. This status is called the overcharge status.

In the case that the VM pin voltage is equal to or lower than $V_{DD} - 0.4 \text{ V typ.}$ and the battery voltage falls below V_{CU} , this IC releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage falls by the V_f voltage of the internal parasitic diode than the VDD pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or lower than $V_{DD} - 0.4 \text{ V typ.}$, this IC releases the overcharge status when the battery voltage is equal to or lower than V_{CU} .

- Caution**
1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection does not function until the battery voltage falls below V_{CU} . Since an actual battery has an internal impedance of tens of m Ω , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection functions.
 2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below V_{CL} . The overcharge status is released when the discharge current flows and the VM pin voltage goes under $V_{DD} - 0.4 \text{ V typ.}$ by removing the charger.

3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the overdischarge status.

Under the overdischarge status, VSS pin and VM pin are shorted by R_{VMS} in this IC. The VM pin voltage is pulled down by R_{VMS} .

When connecting a charger in the overdischarge status, the battery voltage reaches V_{DL} or higher and this IC releases the overdischarge status if the VM pin voltage is above V_{DD} typ.

The battery voltage reaches the overdischarge release voltage (V_{DU}) or higher and this IC releases the overdischarge status if the VM pin voltage is not above V_{DD} typ.

R_{VMD} is not connected in the overdischarge status.

3.1 With power-down function

Under the overdischarge status, when the VM pin voltage is $V_{DD} - 0.8$ V typ. or lower, the power-down function works and the current consumption is reduced to the current consumption during power-down (I_{PDN}). By connecting a battery charger, the power-down function is released when the VM pin voltage is $V_{DD} - 0.8$ V typ. or higher.

- When a battery is not connected to a charger and the VM pin voltage $\leq V_{DD} - 0.8$ V typ., this IC maintains the overdischarge status even when the battery voltage reaches V_{DU} or higher.
- When a battery is connected to a charger and $V_{DD} - 0.8$ V typ. < the VM pin voltage < V_{DD} typ., the battery voltage reaches V_{DU} or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and V_{DD} typ. \leq the VM pin voltage, the battery voltage reaches V_{DL} or higher and this IC releases the overdischarge status.

3.2 Without power-down function

Under the overdischarge status, the power-down function does not work even when the VM pin voltage is $V_{DD} - 0.8$ V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage $\leq V_{DD} - 0.8$ V typ., the battery voltage reaches V_{DU} or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and $V_{DD} - 0.8$ V typ. < the VM pin voltage < V_{DD} typ., the battery voltage reaches V_{DU} or higher and this IC releases the overdischarge status.
- When a battery is connected to a charger and V_{DD} typ. \leq the VM pin voltage, the battery voltage reaches V_{DL} or higher and this IC releases the overdischarge status.

4. Discharge overcurrent status

(Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting, load short-circuiting 2)

4. 1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting

When a battery in the normal status is in the status where the overcurrent detection pins is equal to or lower than V_{DIOV1} because the discharge current is equal to or higher than the specified value and the status continues for the discharge overcurrent 1 detection delay time (t_{DIOV1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

4. 1. 1 Release condition of discharge overcurrent "load disconnection"

Under the discharge overcurrent status, VM pin and VDD pin are shorted by R_{VMD} in this IC. However, the VM pin voltage is the VSS pin voltage due to the load as long as the load is connected. When the load is disconnected, the VM pin voltage returns to the VDD pin voltage. When the VM pin voltage returns to discharge overcurrent release voltage (V_{RIOV}) or higher, this IC releases the discharge overcurrent status.

R_{VMS} is not connected in the discharge overcurrent status.

4. 1. 2 Release condition of discharge overcurrent "charger connection"

Under the discharge overcurrent status, the VM pin and VSS pin are shorted by R_{VMS} in this IC. When a battery is connected to a charger and the VM pin voltage returns to the discharge overcurrent release voltage (V_{DRIOV}) or higher, this IC releases the discharge overcurrent status.

R_{VMD} is not connected in the discharge overcurrent status.

4. 2 Load short-circuiting 2

When a battery in the normal status is in the status where a load causing discharge overcurrent is connected, and the VM pin voltage is equal to or lower than the load short-circuiting 2 detection voltage (V_{SHORT2}) and the status continues for the load short-circuiting detection delay time (t_{SHORT}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

This IC releases the discharge overcurrent status in the same way as in "4. 1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting".

5. Charge overcurrent status

When a battery in the normal status is in the status where the overcurrent detection pins is equal to or higher than V_{CIOV} because the charge current is equal to or higher than the specified value and the status continues for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.

This IC releases the charge overcurrent status when the discharge current flows and the VM pin voltage is $V_{DD} - 0.4$ V typ. or lower by removing the charger.

The charge overcurrent detection does not function in the overdischarge status.

6. Overheat protection status

Under the normal status and the overheat protection status, the overheat detection circuit operates intermittently every 128 ms typ., during which the awake mode period is 4 ms typ. When a battery in the normal status is in the status where the temperature of the NTC thermistor (T_{NTC}) rises above the overheat detection temperature (T_{DET}) and the status lasts for the overheat detection delay time (t_{DET}) or longer from the next awake mode start timing of the overheat detection circuit, this IC becomes the overheat protection status. This IC in the overheat protection status turns off both the charge control FET and the discharge control FET.

When T_{NTC} drops below the overheat release temperature (T_{REL}) and the condition continues for t_{TREL} or longer from the next awake mode start timing of the overheat detection circuit, this IC returns to the normal status.

Both R_{VMD} and R_{VMS} are not connected.

7. 0 V battery charge enabled

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB- pins by connecting a charger, the charge control FET gate is fixed to the VM pin voltage.

When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than V_{DL} , this IC returns to the normal status.

Caution 1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

2. The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL} .

8. 0 V battery charge inhibited

This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the VDD pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. It depends on the characteristics of the lithium-ion rechargeable battery to be used; therefore, please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

9. Power-saving status

9.1 PS pin control logic active "H"

When the PS pin voltage is equal to or higher than PS pin voltage "H" (V_{PSH}) and the status continues for the power-saving delay time (t_{PS}) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the power-saving status.

In the power-saving status, current consumption is reduced to the current consumption during power-saving (I_{PS}).

When PS pin voltage falls below PS pin voltage "L" (V_{PSL}), power-saving status is released.

9.2 PS pin control logic active "L"

When the PS pin voltage is equal to or lower than V_{PSL} and the status continues for t_{PS} or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the power-saving status.

In the power-saving status, current consumption is reduced to I_{PS} .

When the PS pin voltage is equal to or higher than V_{PSH} , power-saving status is released.

10. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV1} , t_{DIOV2} and t_{SHORT} start when V_{DIOV1} is detected. When V_{DIOV2} or V_{SHORT} is detected over t_{DIOV2} or t_{SHORT} after the detection of V_{DIOV1} , the discharge control FET is turned off within t_{DIOV2} or t_{SHORT} of each detection.

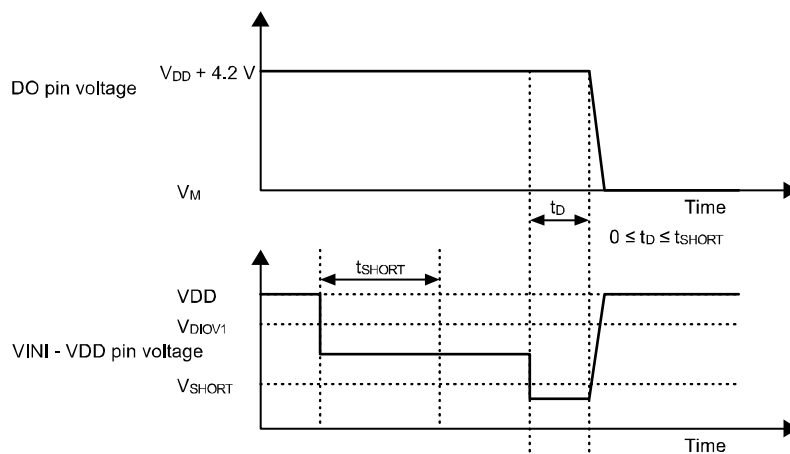
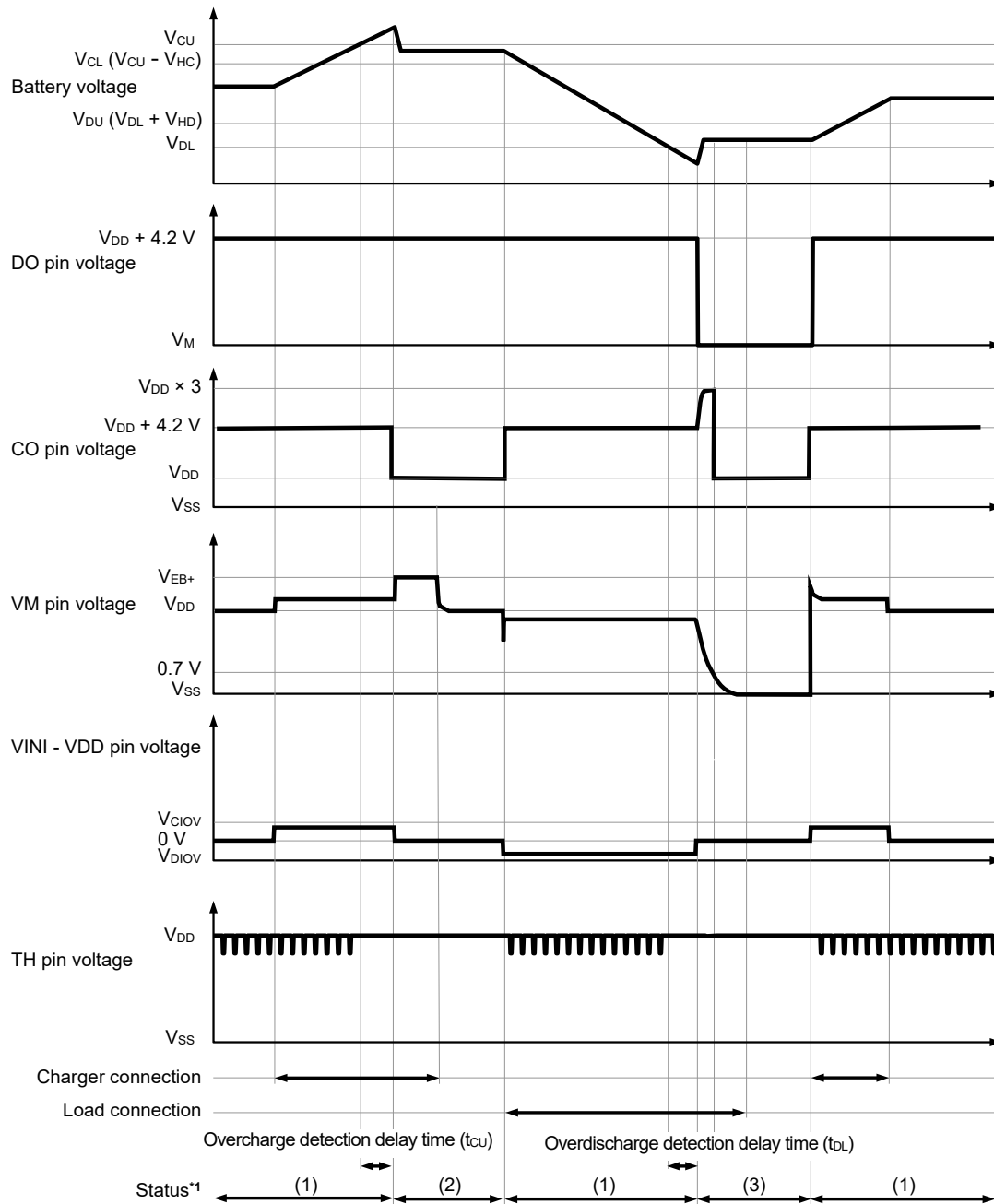


Figure 11

■ **Timing Charts**

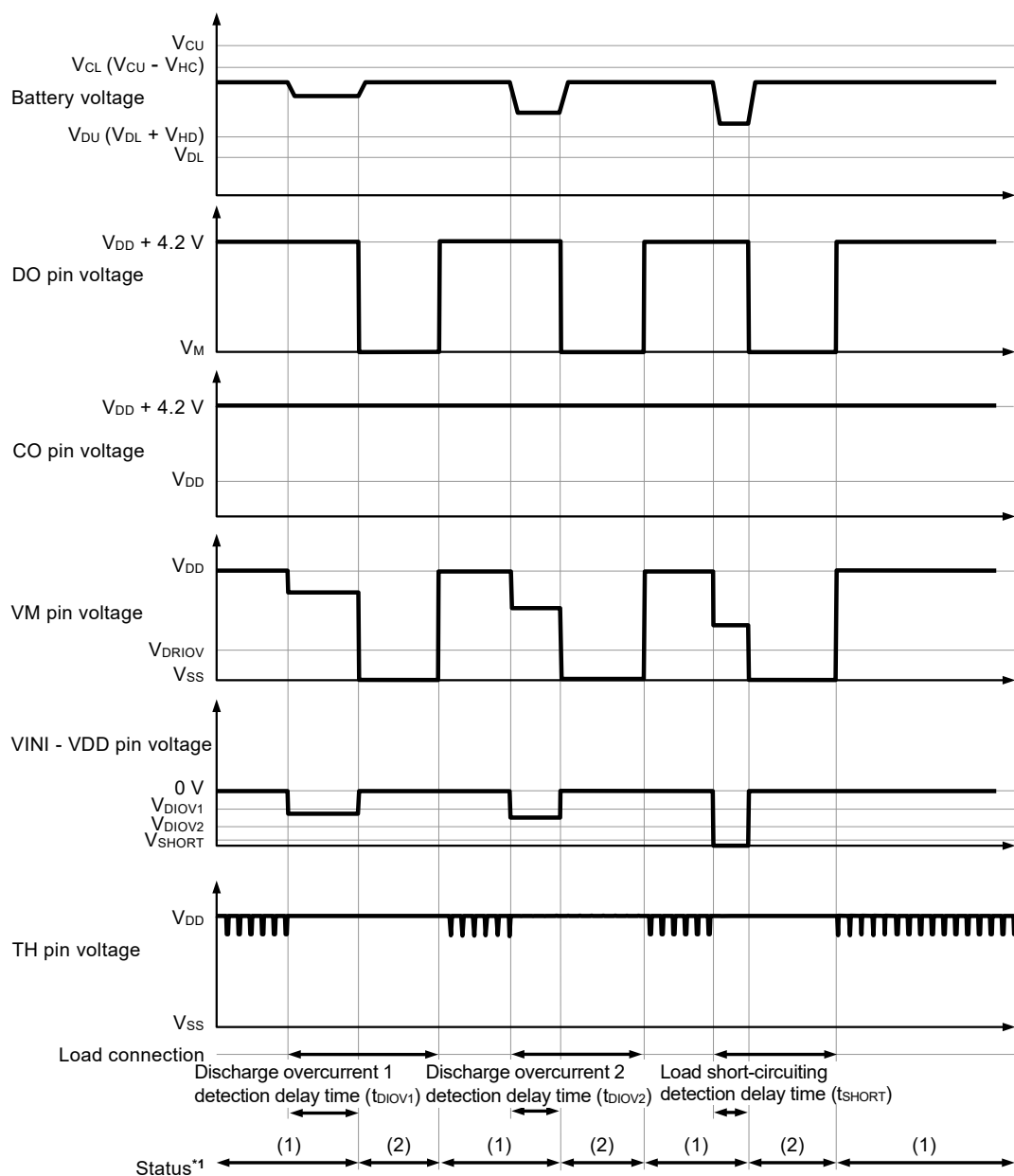
1. Overcharge detection, overdischarge detection



- *1. (1): Normal status
 (2): Overcharge status
 (3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 12

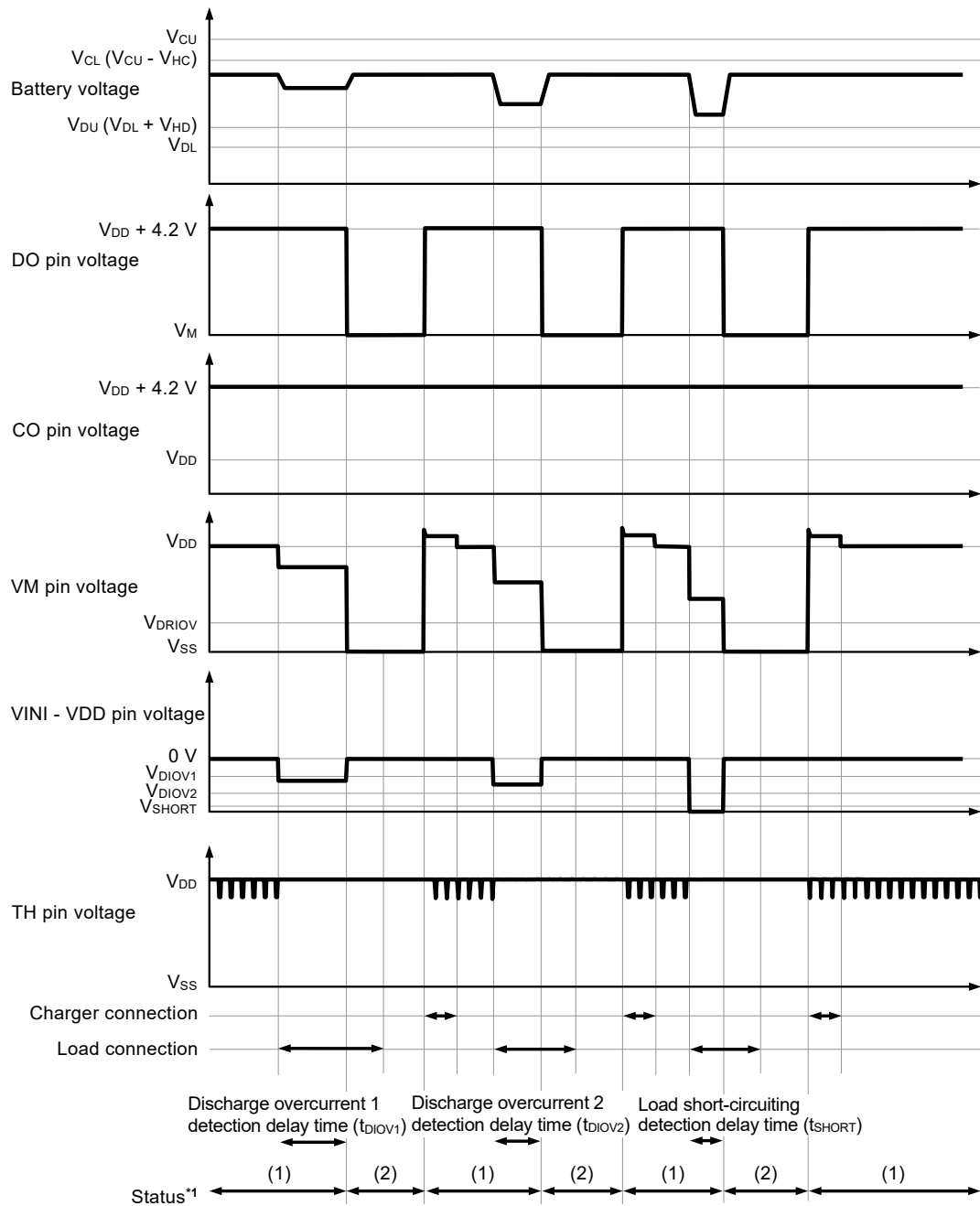
2. Discharge overcurrent detection**(Release condition of discharge overcurrent status "load disconnection")**

*1. (1): Normal status

(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.**Figure 13**

3. Discharge overcurrent detection
(Release condition of discharge overcurrent status "charger connection")

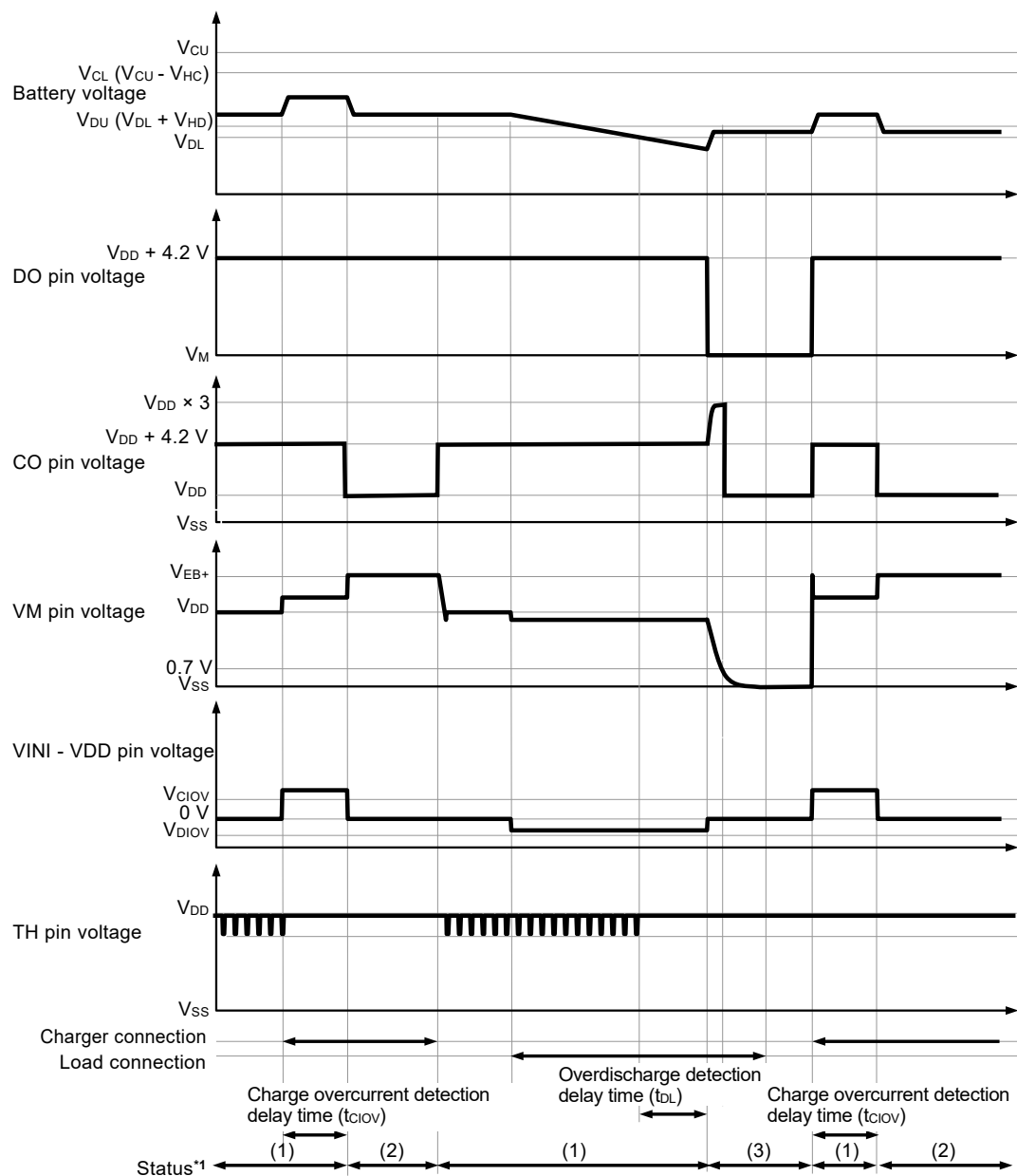


*1. (1): Normal status
 (2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 14

4. Charge overcurrent detection

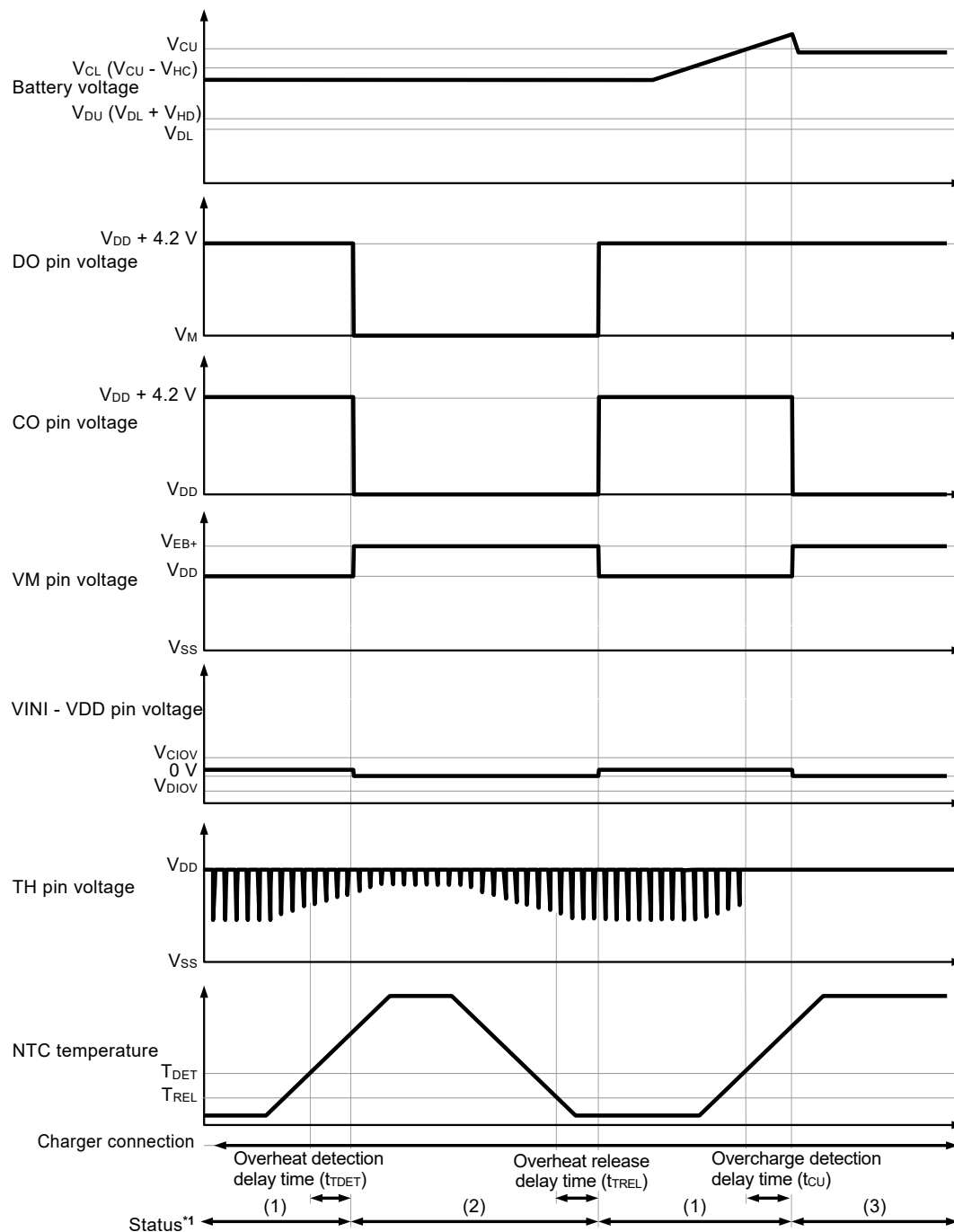


- *1. (1): Normal status
 (2): Charge overcurrent status
 (3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 15

5. Overheat detection

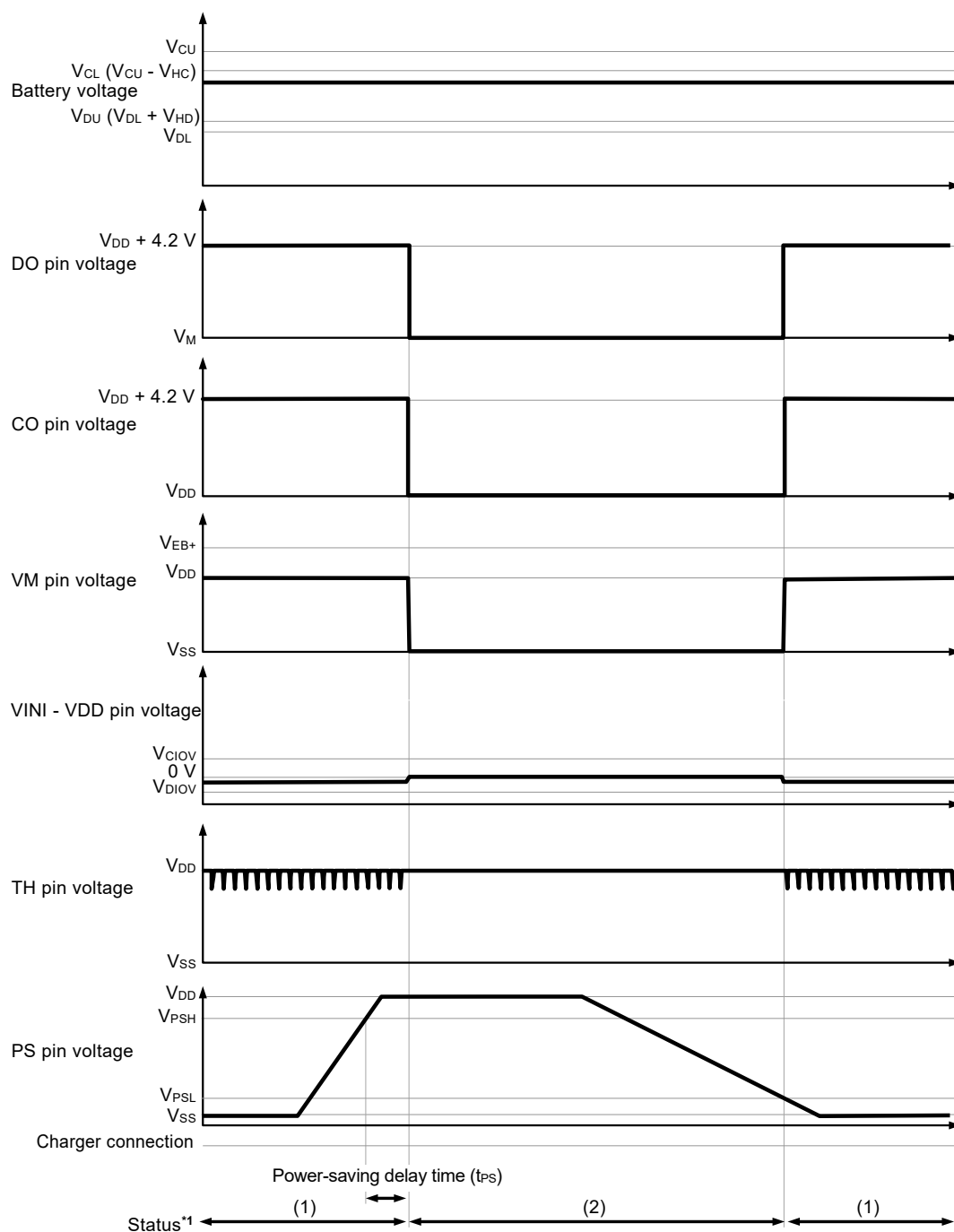


- *1. (1): Normal status
 (2): Overheat protection status
 (3): Overcharge status

Remark The charger is assumed to charge with a constant current.

Figure 16

6. Power-saving (PS pin control logic active "H")



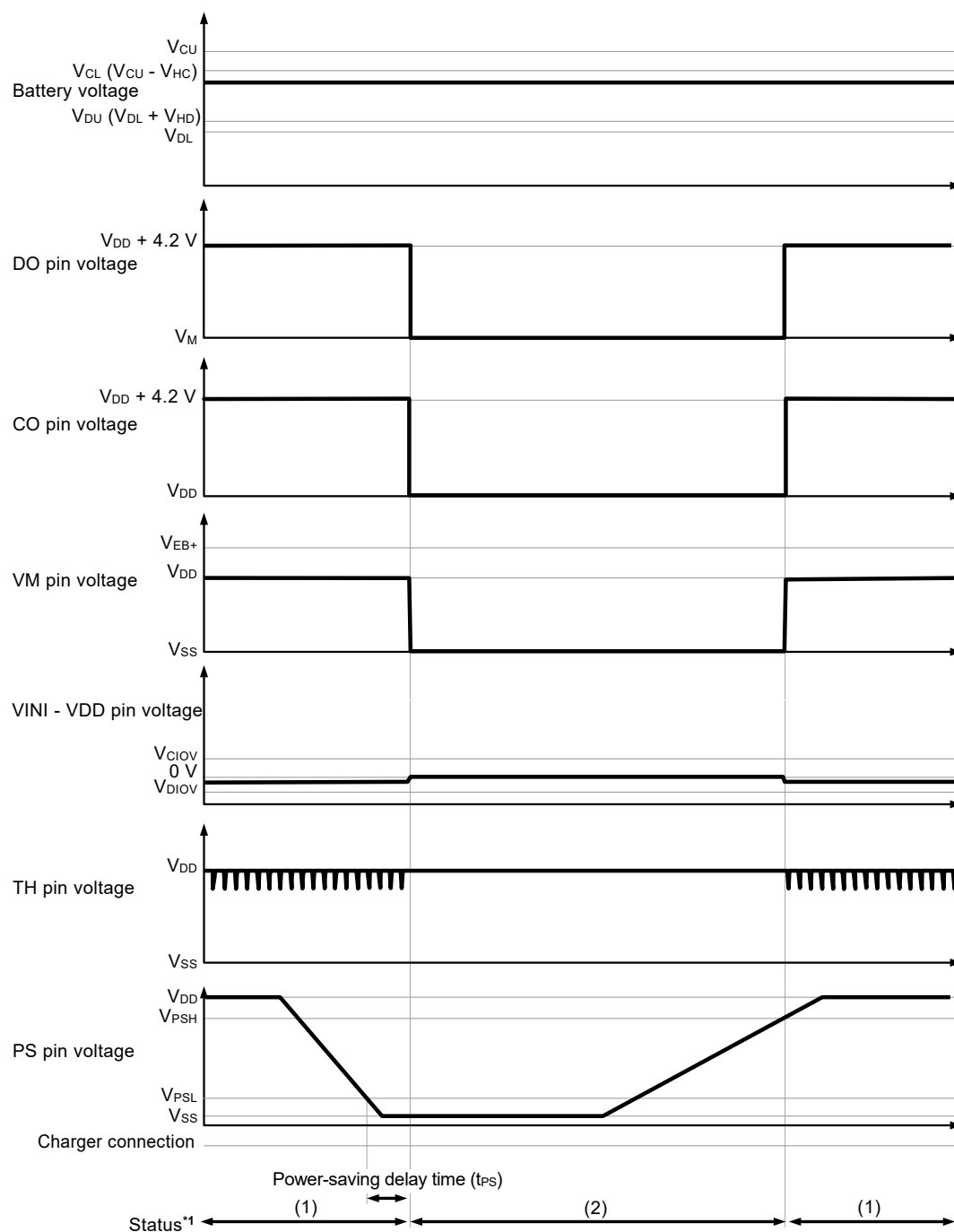
*1. (1) : Normal status

(2) : Power-saving status

Remark The charger is assumed to charge with a constant current.

Figure 17

7. Power-saving (PS pin control logic active "L")



*1. (1) : Normal status
 (2) : Power-saving status

Remark The charger is assumed to charge with a constant current.

Figure 18

■ Battery Protection IC Connection Example

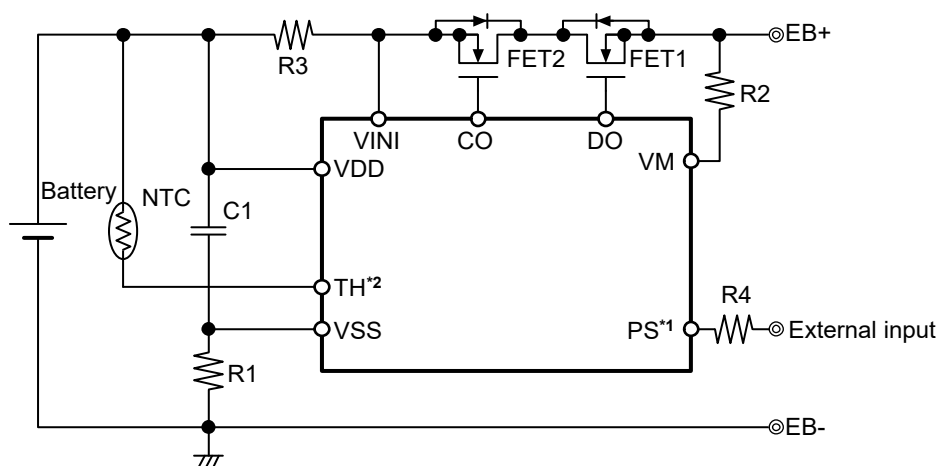


Figure 19

*1. If the power-saving function is unavailable, the PS pin must be left open.

*2. If the overheat detection function is unavailable, the TH pin must be connected to the VDD pin or the VSS pin.

Table 12 Constants for External Components

| Symbol | Part | Purpose | Min. | Typ. | Max. | Remark |
|--------|-------------------|--|--------|---------|--------|---|
| FET1 | N-channel MOS FET | Discharge control | - | - | - | Threshold voltage ≤ Overdischarge detection voltage*1 |
| FET2 | N-channel MOS FET | Charge control | - | - | - | Threshold voltage ≤ Overdischarge detection voltage*1 |
| R1*2 | Resistor | ESD protection, For power fluctuation | 1 kΩ | 1 kΩ | 1 kΩ | - |
| C1 | Capacitor | For power fluctuation | 0.1 μF | 0.1 μF | 0.1 μF | - |
| R2 | Resistor | ESD protection, Protection for reverse connection of a charger | 22 Ω | 22 Ω | 22 Ω | - |
| R3 | Resistor | Overcurrent detection | - | 0.75 mΩ | - | - |
| R4 | Resistor | ESD protection | - | 1 kΩ*3 | - | - |
| NTC*4 | NTC thermistor | Temperature sensing | 100 kΩ | 100 kΩ | 470 kΩ | - |

*1. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

*2. Accuracy of overcharge detection voltage is guaranteed by R1 = 1 kΩ. Connecting resistors with other values will worsen the accuracy.

*3. Current limiting resistance when a voltage of 6 V or higher is applied to the EB+ pin.

*4. Temperature detection accuracy varies with NTC thermistor specifications.

When an NTC thermistor listed in **Table 2 (3 / 4)** is connected, the detection temperature and accuracy can be achieved.

Caution 1. The constants may be changed without notice.

- It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

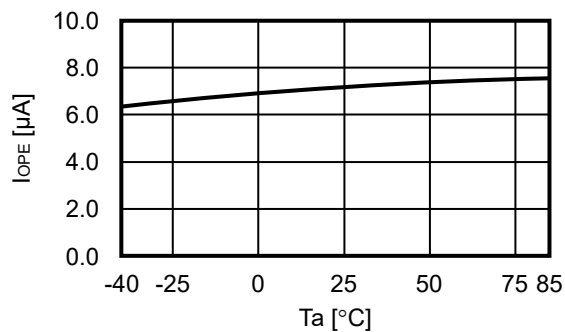
■ **Precautions**

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

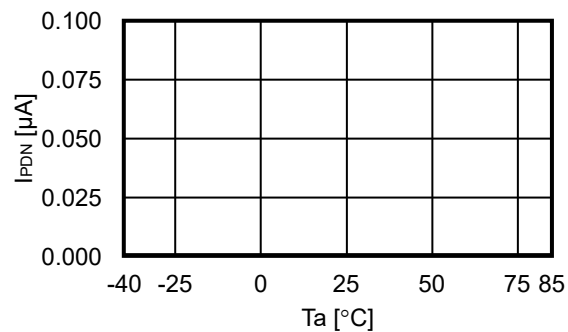
■ Characteristics (Typical Data)

1. Current consumption

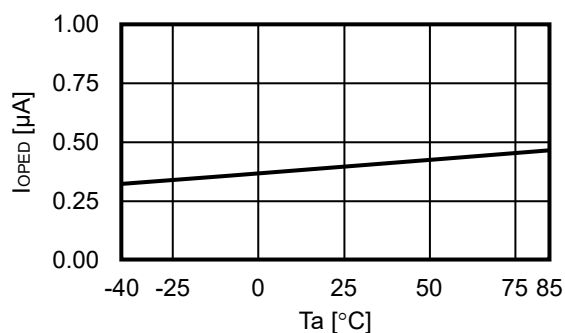
1. 1 I_{OPE} vs. T_a



1. 2 I_{PDN} vs. T_a

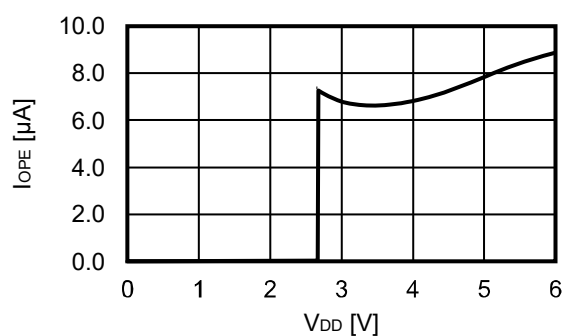


1. 3 I_{OPED} vs. T_a

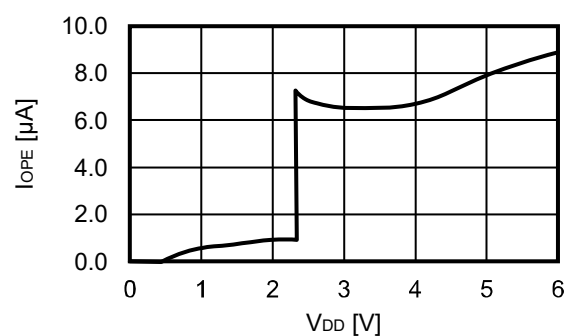


1. 4 I_{OPE} vs. V_{DD}

1. 4. 1 With power-down function

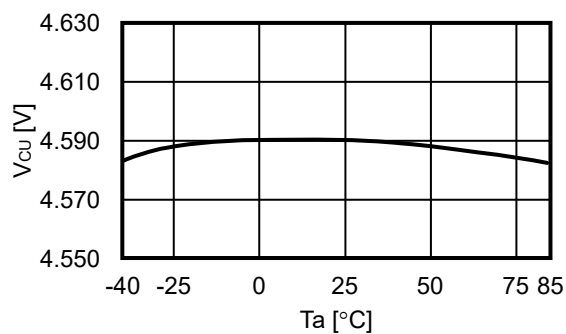


1. 4. 2 Without power-down function

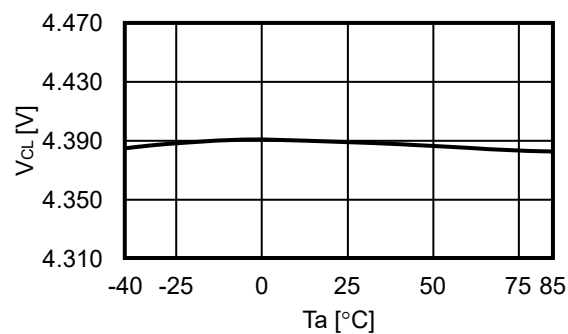


2. Detection voltage

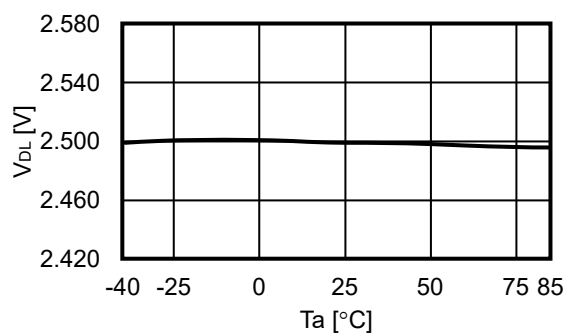
2. 1 V_{CU} vs. T_a



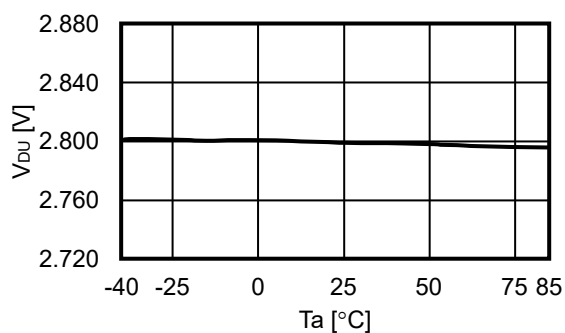
2. 2 V_{CL} vs. T_a



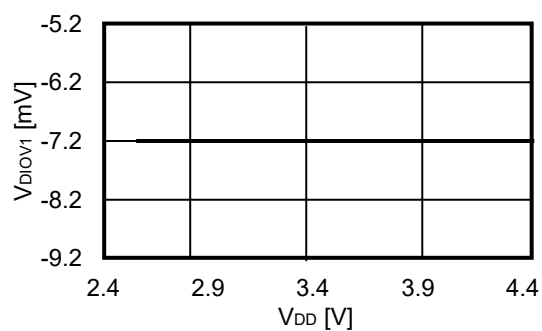
2. 3 V_{DL} vs. T_a



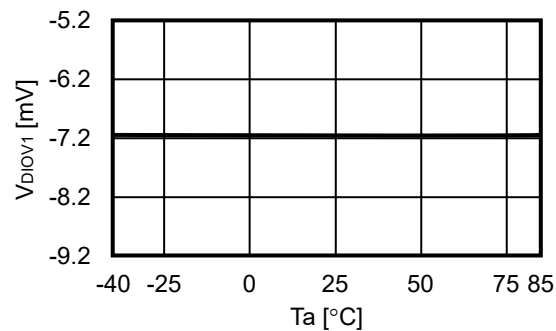
2. 4 V_{DU} vs. T_a



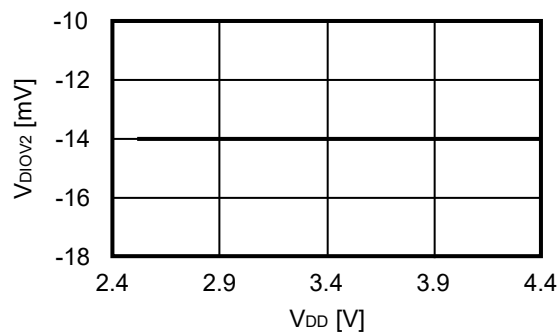
2. 5 V_{DIOV1} vs. V_{DD}



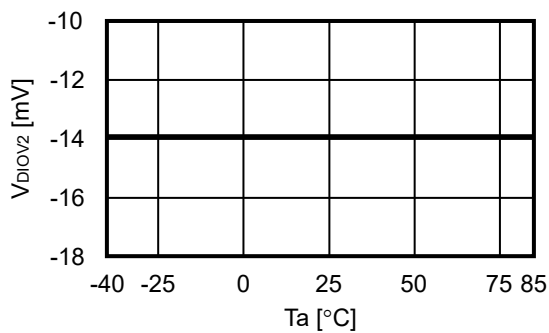
2. 6 V_{DIOV1} vs. T_a

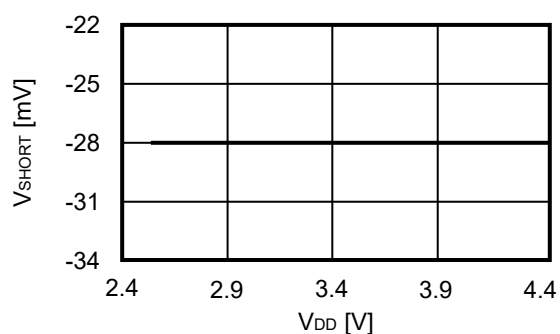
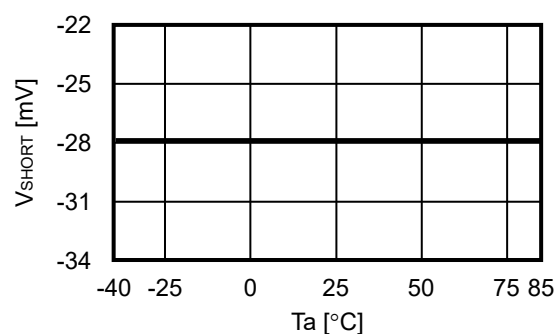
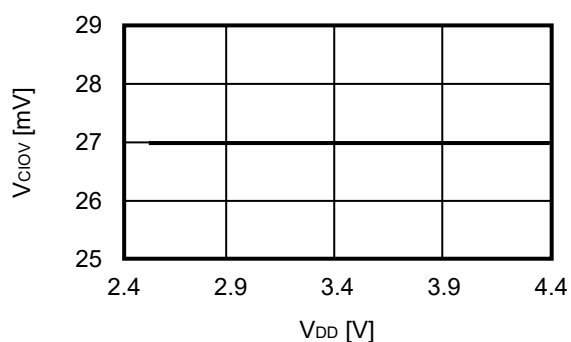
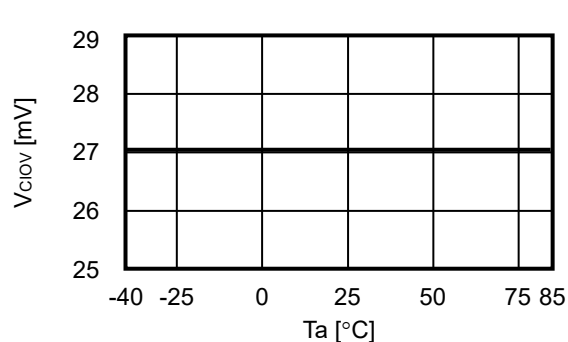
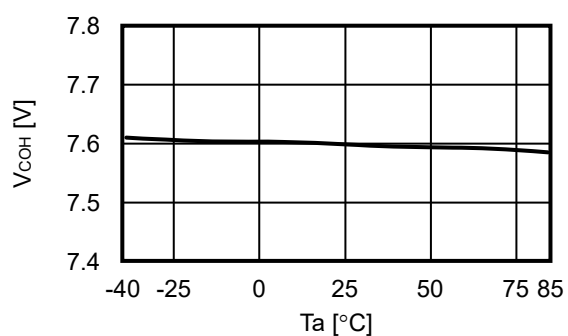
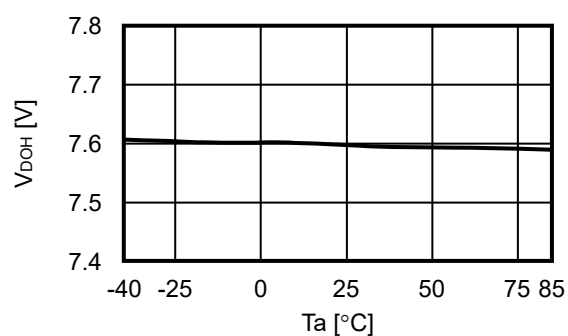


2. 7 V_{DIOV2} vs. V_{DD}



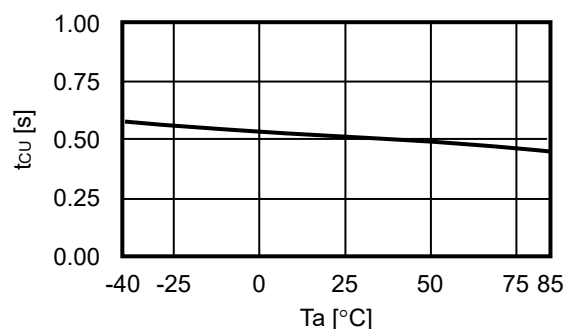
2. 8 V_{DIOV2} vs. T_a



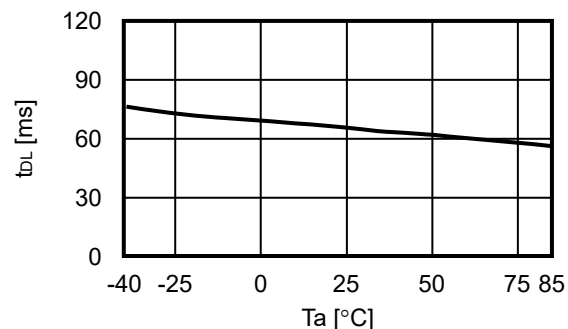
2. 9 V_{SHORT} vs. V_{DD} 2. 10 V_{SHORT} vs. T_a 2. 11 V_{CLOV} vs. V_{DD} 2. 12 V_{CLOV} vs. T_a 2. 13 V_{COH} vs. T_a 2. 14 V_{DOH} vs. T_a 

3. Delay time

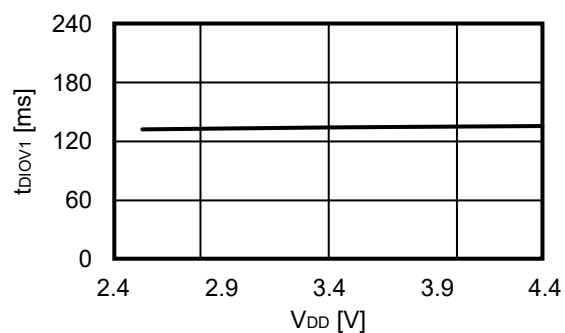
3. 1 t_{CU} vs. T_a



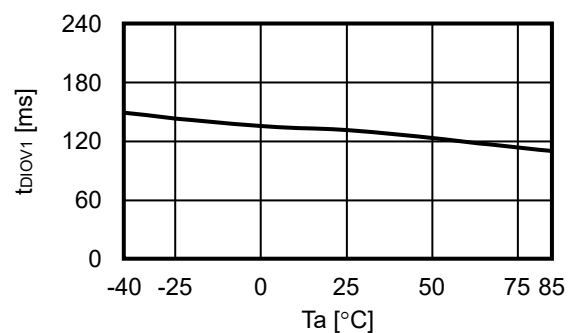
3. 2 t_{DL} vs. T_a



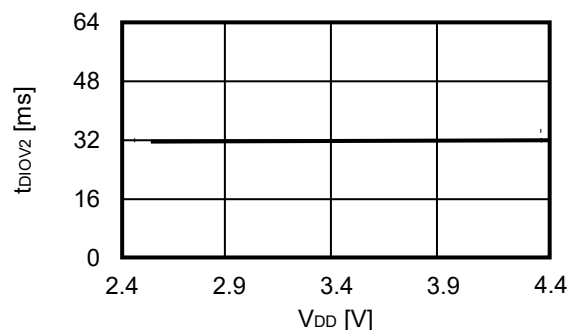
3. 3 t_{DIOV1} vs. V_{DD}



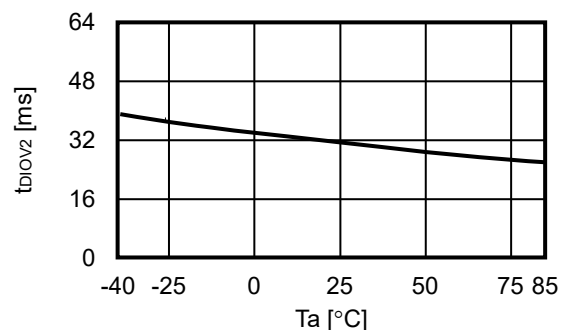
3. 4 t_{DIOV1} vs. T_a



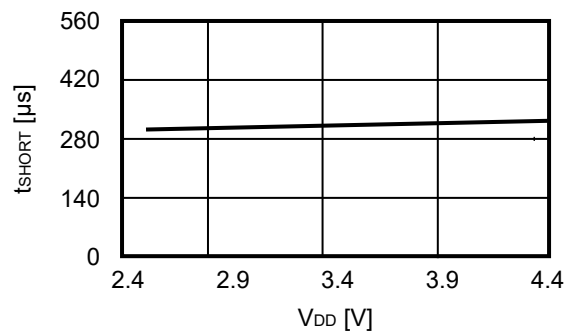
3. 5 t_{DIOV2} vs. V_{DD}



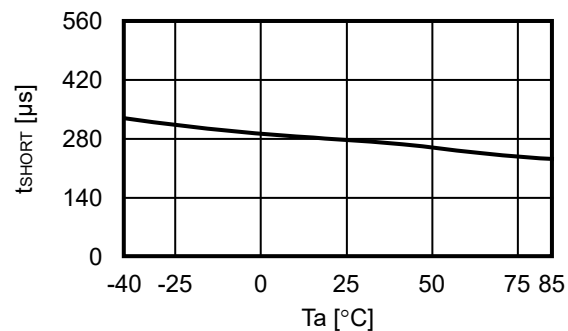
3. 6 t_{DIOV2} vs. T_a

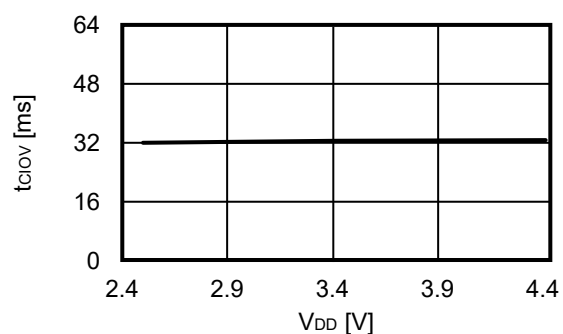
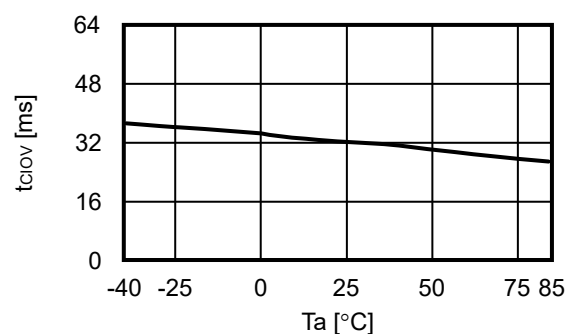


3. 7 t_{SHORT} vs. V_{DD}

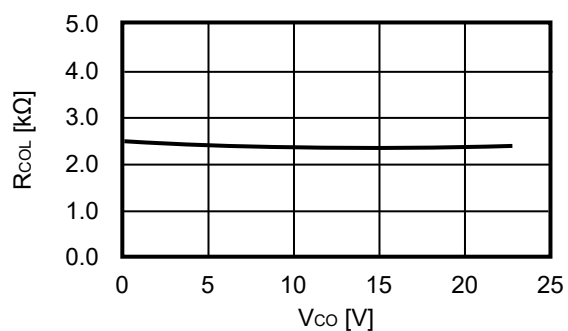
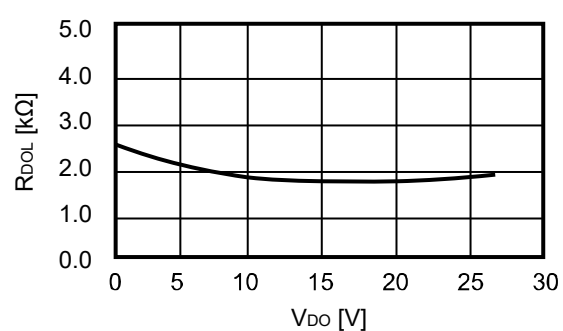


3. 8 t_{SHORT} vs. T_a



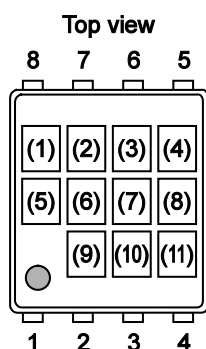
3. 9 t_{CIOV} vs. V_{DD} 3. 10 t_{CIOV} vs. T_a 

4. Output resistance

4. 1 R_{COL} vs. V_{CO} 4. 2 R_{DOL} vs. V_{DO} 

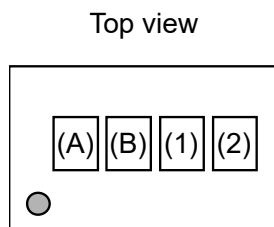
■ Marking Specifications

1. SNT-8A



(1), (5), (6) : Blank
 (2) to (4) : Product code
 (7) to (11) : Lot number

2. WLP-8V



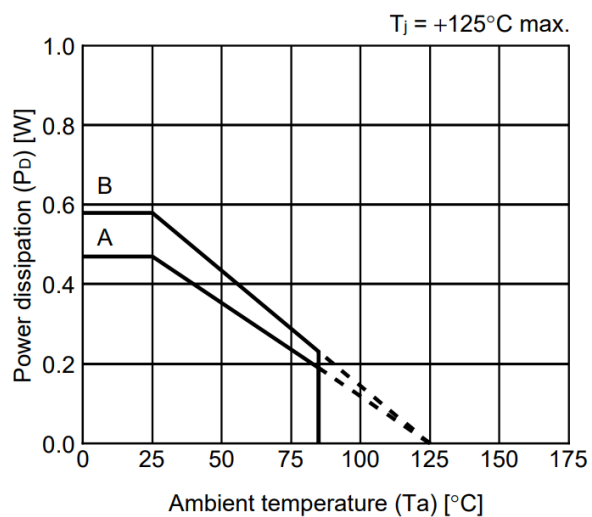
(A) : Product code (Refer to **Product name vs. Product code**)
 (B) : Blank
 (1), (2) : Lot number

Product Name vs. Product Code

| Product Name | Product Code |
|-----------------|--------------|
| | (A) |
| S-821BAAC-H8T7S | E |
| S-821BAAD-H8T7S | F |
| S-821BAAE-H8T7S | G |
| S-821BAAF-H8T7S | H |
| S-821BAAK-H8T7S | M |
| S-821BAAL-H8T7S | N |

■ Power Dissipation

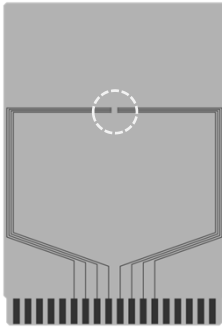
SNT-8A



| Board | Power Dissipation (P_D) |
|-------|-----------------------------|
| A | 0.47 W |
| B | 0.58 W |
| C | - |
| D | - |
| E | - |

SNT-8A Test Board

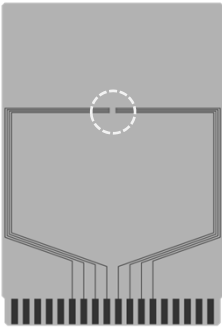
(1) Board A



 IC Mount Area

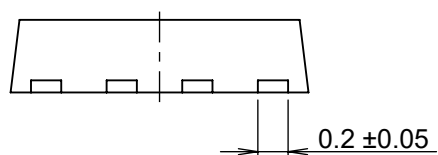
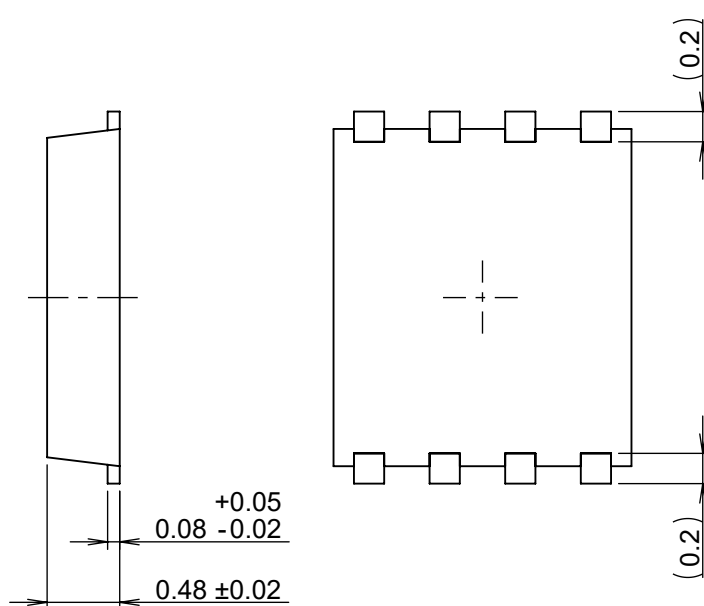
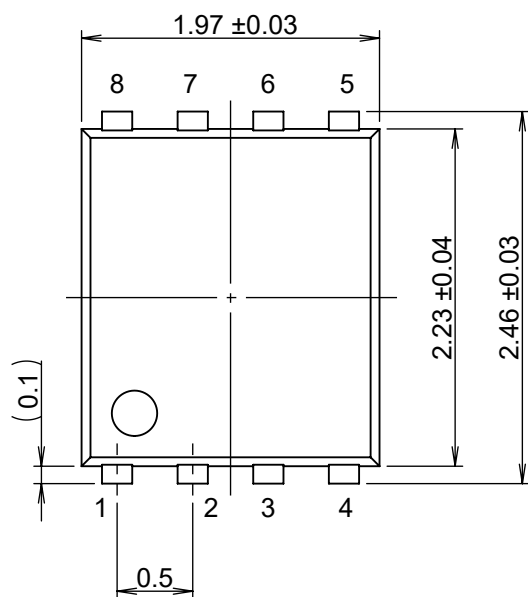
| Item | | Specification |
|-----------------------------|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

(2) Board B



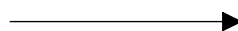
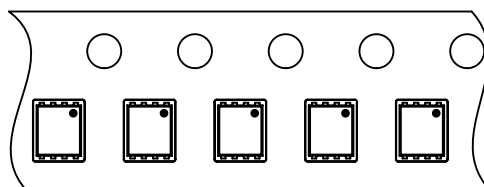
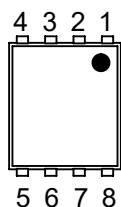
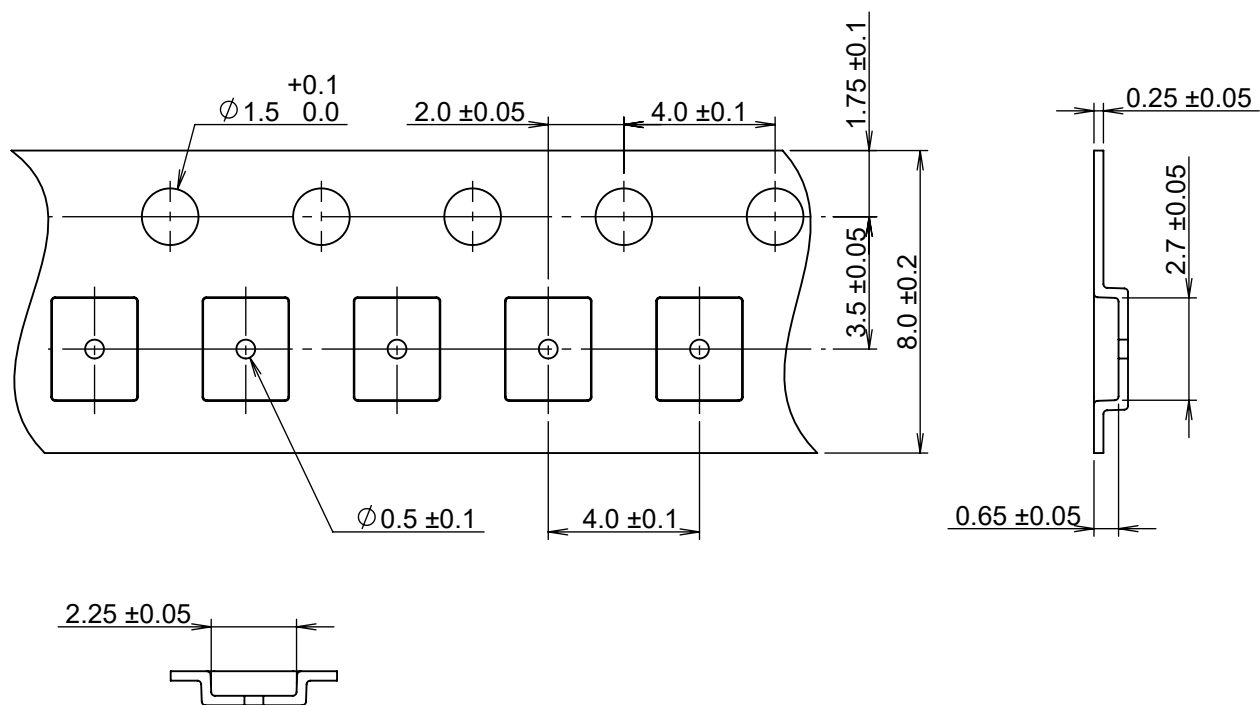
| Item | | Specification |
|-----------------------------|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

No. SNT8A-A-Board-SD-1.0



No. PH008-A-P-SD-2.1

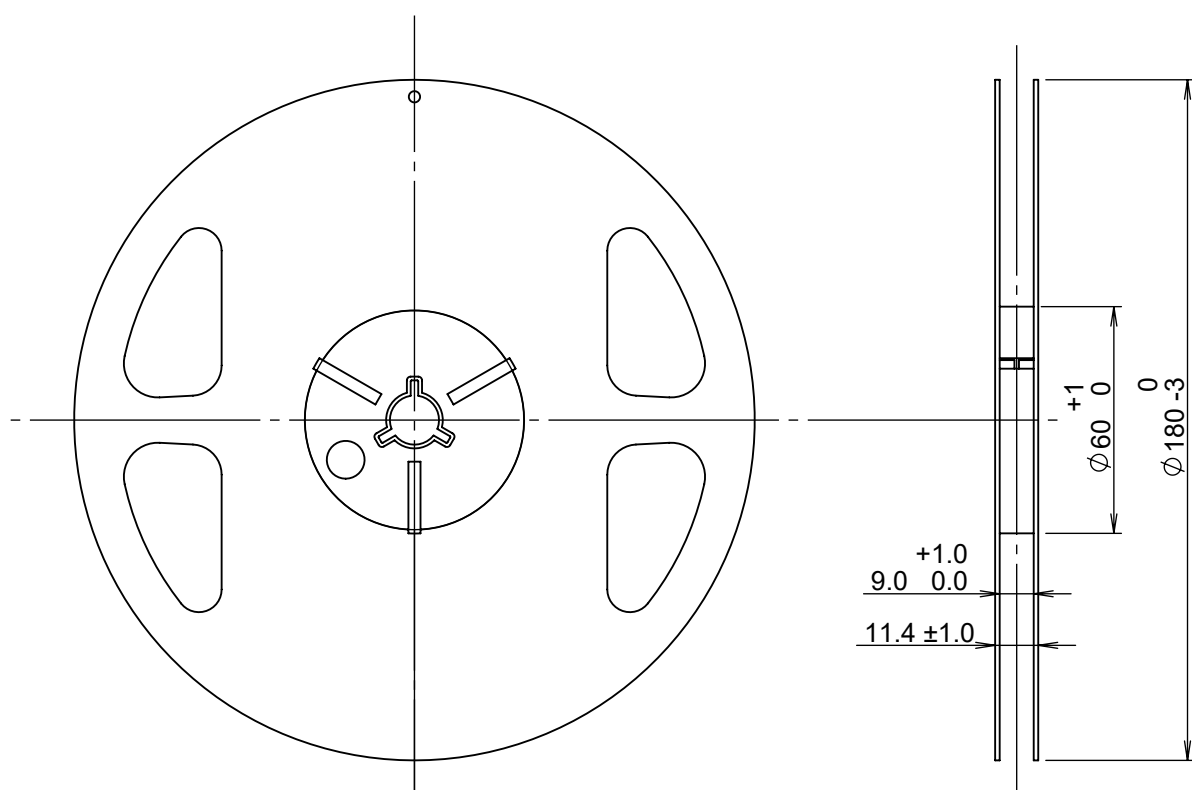
| | |
|------------|-------------------------|
| TITLE | SNT-8A-A-PKG Dimensions |
| No. | PH008-A-P-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |



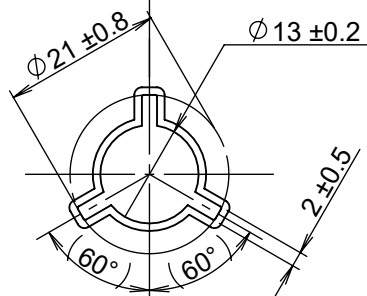
Feed direction

No. PH008-A-C-SD-2.0

| | |
|------------|-----------------------|
| TITLE | SNT-8A-A-Carrier Tape |
| No. | PH008-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |

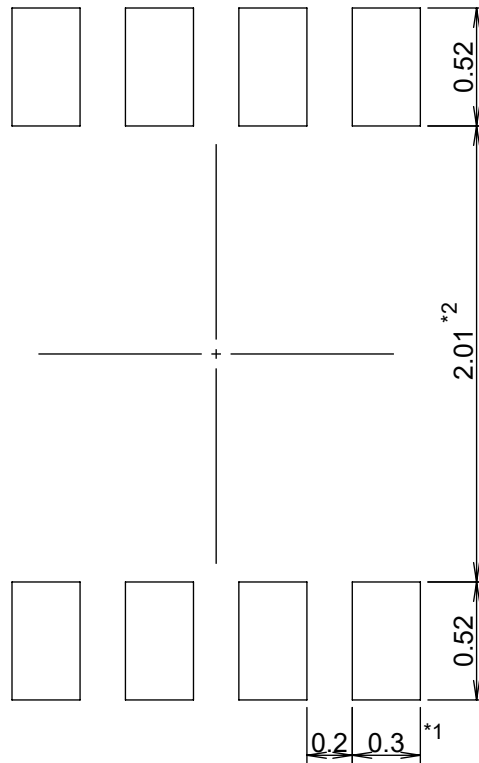


Enlarged drawing in the central part



No. PH008-A-R-SD-2.0

| | | | |
|------------|------------------|------|-------|
| TITLE | SNT-8A-A-Reel | | |
| No. | PH008-A-R-SD-2.0 | | |
| ANGLE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |



- *1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.).
 *2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm).

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
 2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
 3. マスク開口サイズと開口位置はランドパターンと合わせてください。
 4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

- *1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
 *2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06 mm).

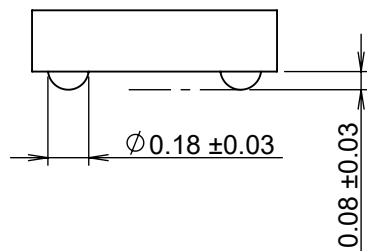
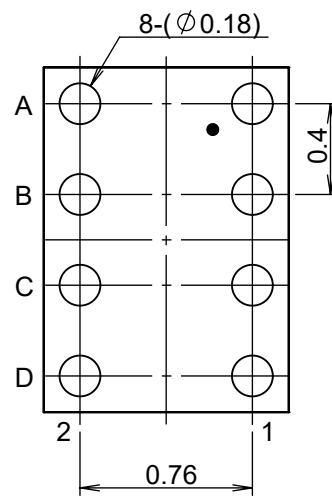
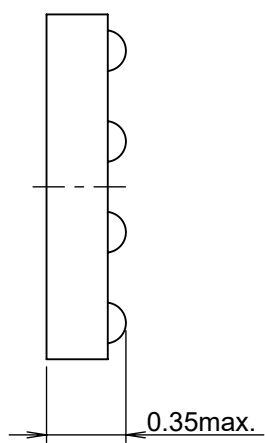
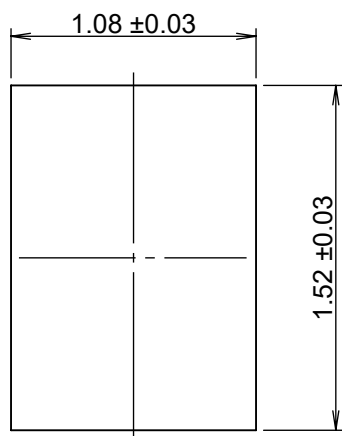
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

- *1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.).
 *2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
 2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在0.03 mm以下。
 3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
 4. 详细内容请参阅 "SNT封装的应用指南"。

No. PH008-A-L-SD-4.1

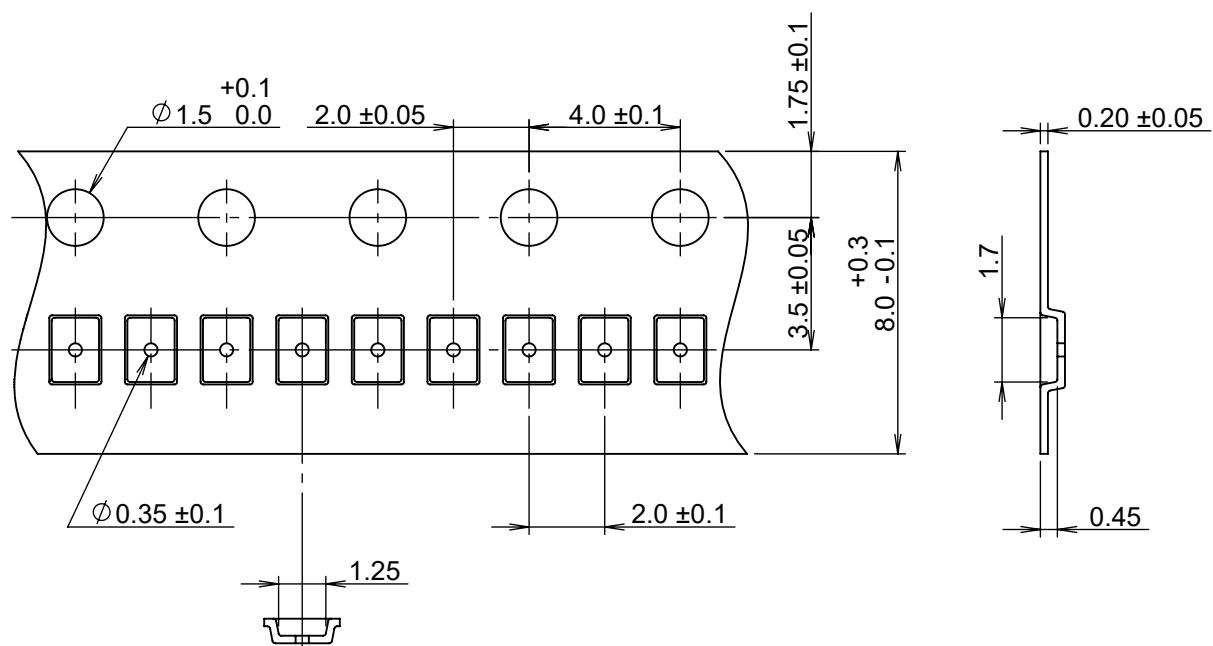
| | |
|------------|----------------------------------|
| TITLE | SNT-8A-A -Land Recommendation |
| No. | PH008-A-L-SD-4.1 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |



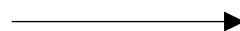
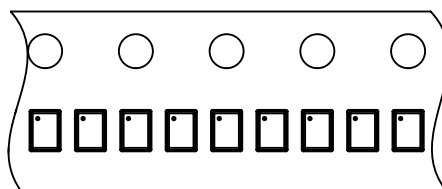
| Pin No. | Symbol |
|---------|--------|
| A1 | VSS |
| A2 | VDD |
| B1 | TH |
| B2 | CO |
| C1 | PS |
| C2 | DO |
| D1 | VINI |
| D2 | VM |

No. HV008-A-P-S2-1.0

| | |
|------------|---|
| TITLE | WLP-8V-A-PKG Dimensions (S-821A*, S-821B*) |
| No. | HV008-A-P-S2-1.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |



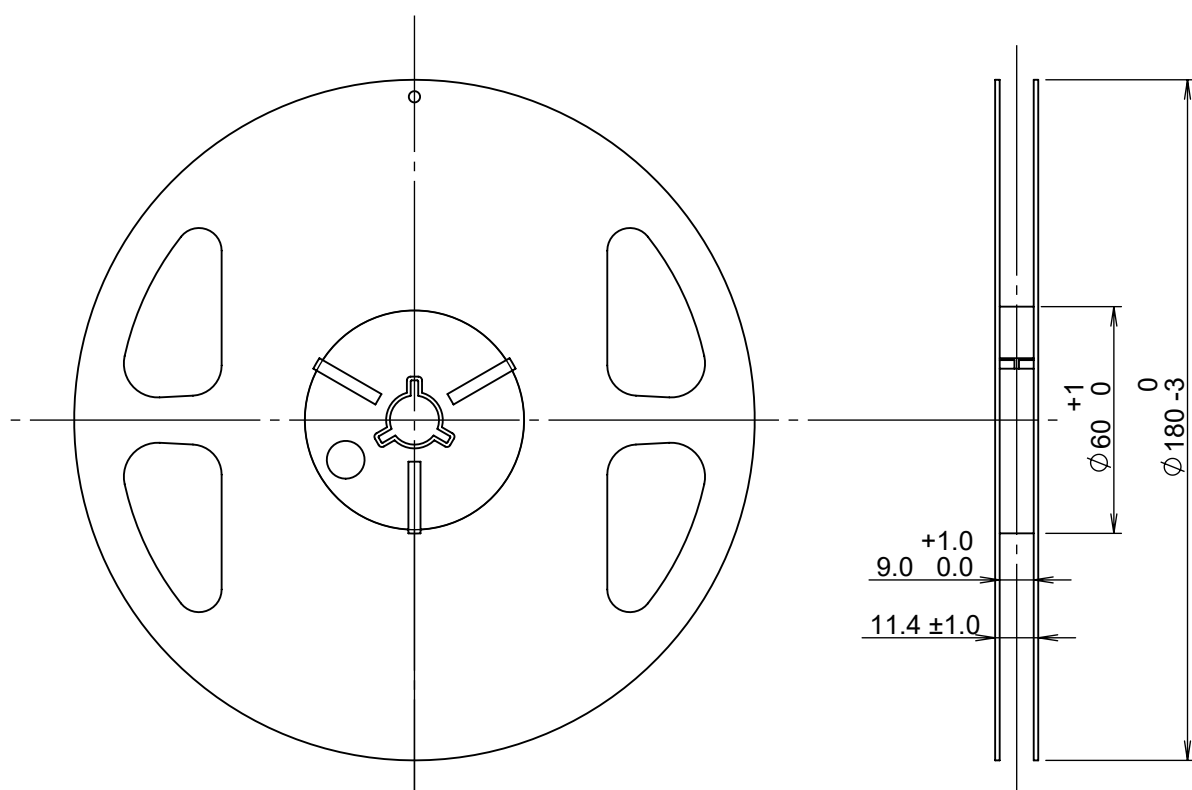
A1 A2
D1 D2



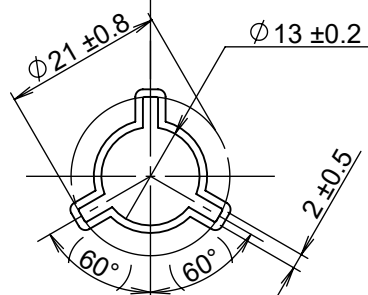
Feed direction

No. HV008-A-C-SD-1.0

| | |
|------------|-----------------------|
| TITLE | WLP-8V-A-Carrier Tape |
| No. | HV008-A-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |

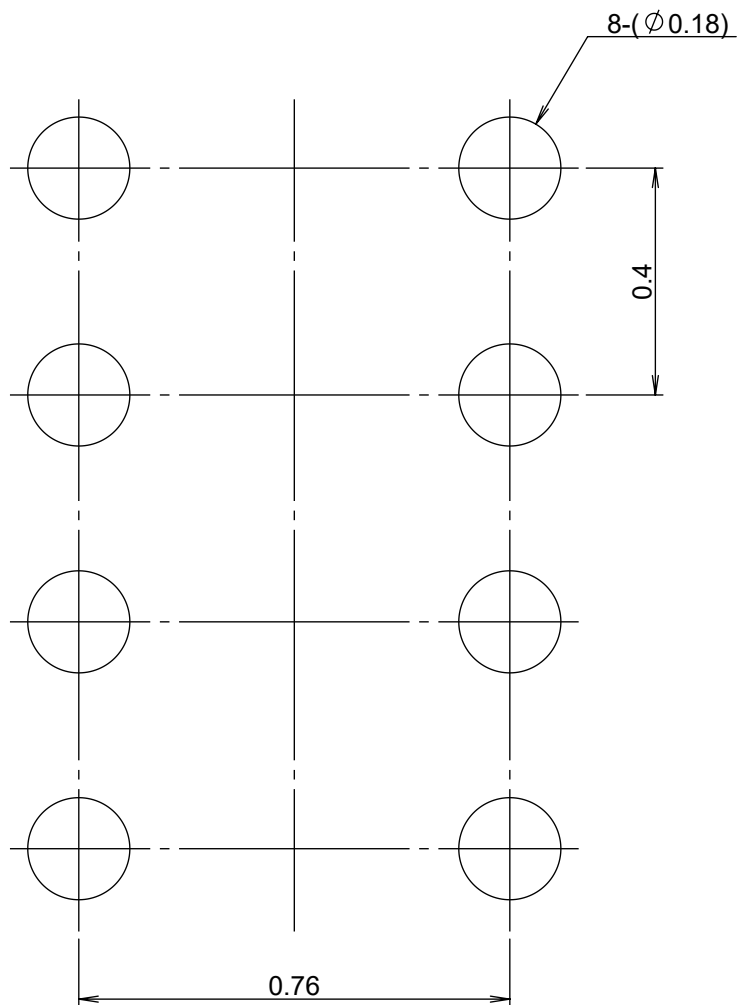


Enlarged drawing in the central part



No. HV008-A-R-SD-1.0

| | | | |
|------------|------------------|------|-------|
| TITLE | WLP-8V-A-Reel | | |
| No. | HV008-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 6,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |



No. HV008-A-L-SD-1.0

| | |
|------------|------------------------------|
| TITLE | WLP-8V-A-Land Recommendation |
| No. | HV008-A-L-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |

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2.4-2019.07

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