

This IC, developed using CMOS technology, is a high-accuracy voltage detector. The detection voltage and release voltage are fixed internally with an accuracy of  $\pm 1.5\%$ .

Since the detection response time is as fast as 6.8  $\mu\text{s}$  max., overvoltage abnormalities can be detected and notified quickly.

Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin voltage ( $V_{\text{SENSE}}$ ) falls to 0 V. The SENSE pin also has a built-in reverse connection protection circuit that reduces current in the SENSE pin during a reverse connection.

The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy is  $\pm 20\%$  ( $C_D = 3.3 \text{ nF}$ ). The output form is Nch open-drain output.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.

For more information regarding our FIT rate calculation, contact our sales representatives.

**Caution** This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

## ■ Features

- |   |   |  |
|---|---|--|
| • Detection voltage:  | 8.0 V to 24.0 V (0.05 V step)                                 |  |
| • Detection voltage accuracy:                                   | $\pm 1.5\%$   |  |
| • Hysteresis width selectable from "Available" / "Unavailable": |   | "Available": 2.3%, 5.0%, 9.0%<br>"Unavailable": 0% |
| • Detection response time:                                      | 6.8 $\mu\text{s}$ max.  |  |
| • Release delay time:   | 10 ms typ. ( $C_D = 3.3 \text{ nF}$ )                         |  |
| • Release delay time accuracy:                                  | $\pm 20\%$ ( $C_D = 3.3 \text{ nF}$ )                         |  |
| • Current consumption:  | 2.0 $\mu\text{A}$ typ.  |  |
| • Operation voltage range:                                      | 3.0 V to 36.0 V   |  |
| • Output form:  | Nch open-drain output   |  |
| • Built-in reverse connection protection circuit:               | Reduces current in the SENSE pin during a reverse connection. |  |
| • Operation temperature range:                                  | $T_a = -40^\circ\text{C}$ to $+125^\circ\text{C}$             |  |
| • Lead-free (Sn 100%), halogen-free                             |   |  |
| • Withstand 45 V load dump                                      |   |  |
| • AEC-Q100 qualified <sup>*1</sup>                              |   |  |

<sup>\*1</sup>. Contact our sales representatives for details.

## ■ Applications

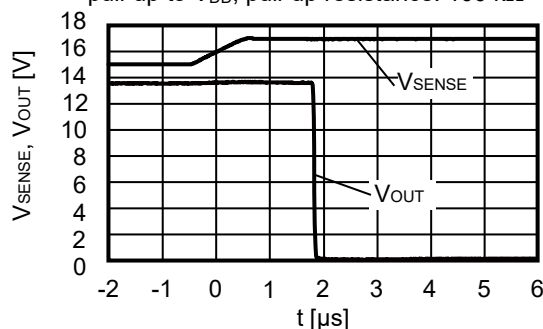
- Automotive battery voltage detection
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

## ■ Packages

- SOT-23-5
- HSNT-6(2025)

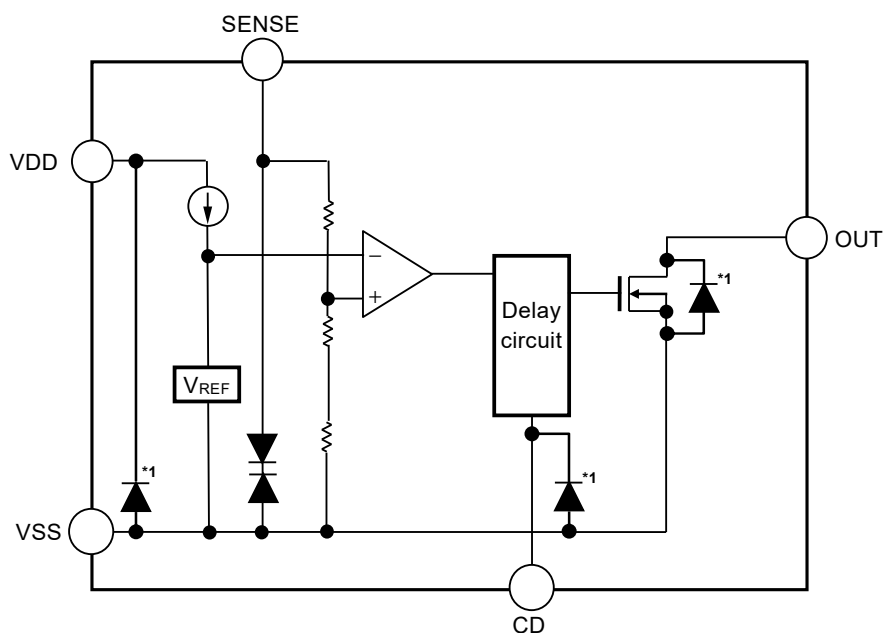
## ■ Detection response time

$V_{\text{DET(S)}} = 16.0 \text{ V}$ ,  $V_{\text{HYS}} = 5.0 \%$ ,  $V_{\text{DD}} = 13.5 \text{ V}$ ,  
 $V_{\text{SENSE}} = V_{\text{DET(S)}} - 1.0 \text{ V} \rightarrow V_{\text{DET(S)}} + 1.0 \text{ V}$ ,  
 pull-up to  $V_{\text{DD}}$ , pull-up resistance: 100 k $\Omega$



## ■ Block Diagrams

### 1. S-19116 Series L type

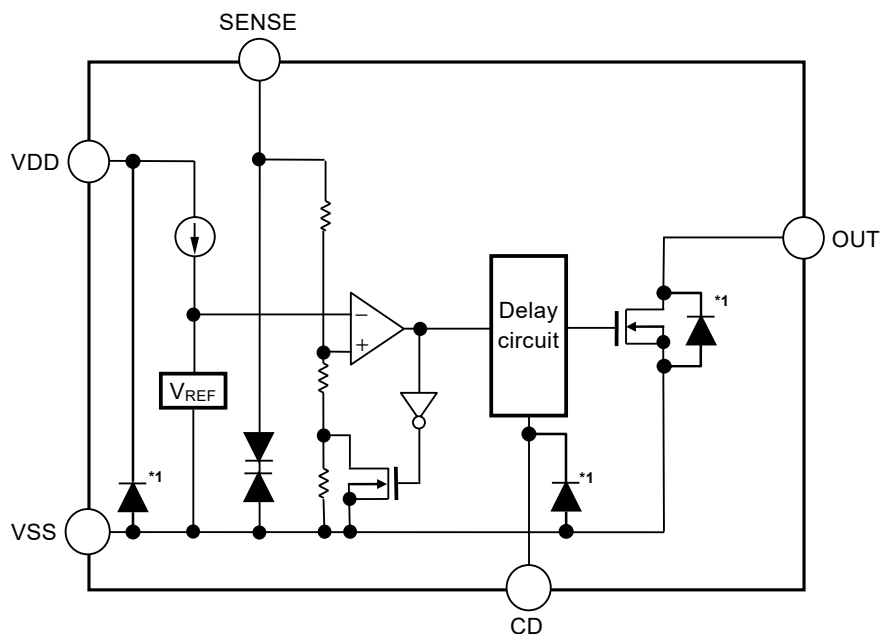


\*1. Parasitic diode

Figure 1

| Product Type | Hysteresis Width | Output Form           | Output Logic |
|--------------|------------------|-----------------------|--------------|
| L type       | 0%               | Nch open-drain output | Active "L"   |

## 2. S-19116 Series M / N / R type



\*1. Parasitic diode

Figure 2

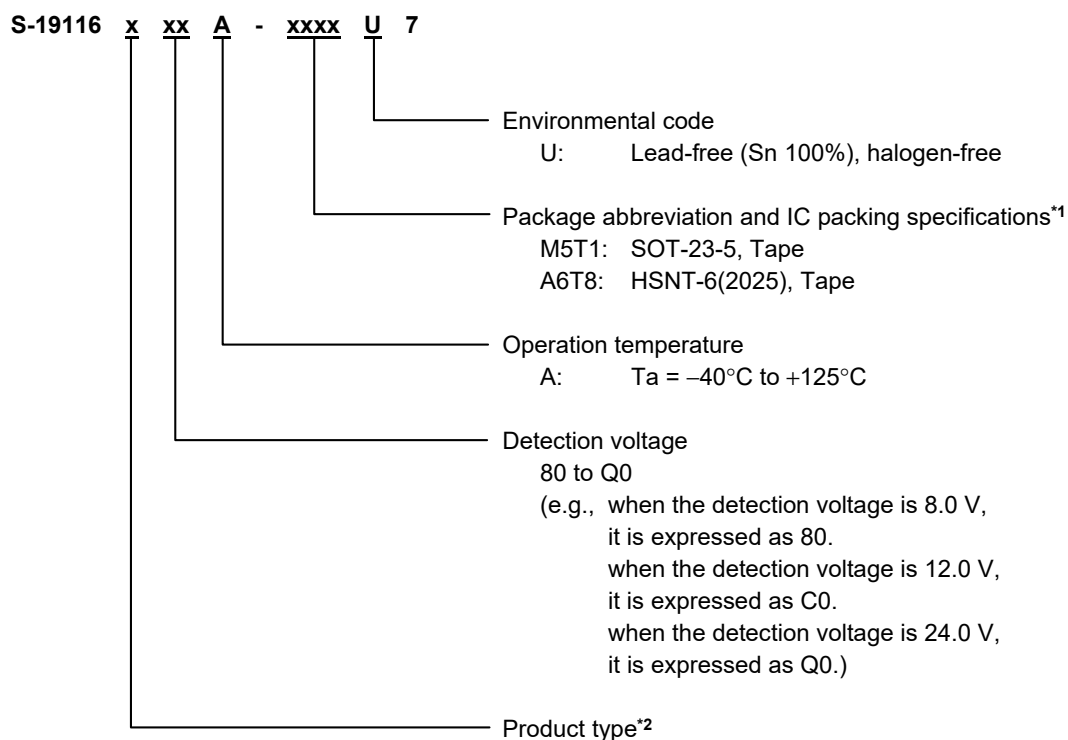
| Product Type | Hysteresis Width | Output Form           | Output Logic |
|--------------|------------------|-----------------------|--------------|
| M type       | 2.3%             | Nch open-drain output | Active "L"   |
| N type       | 5.0%             | Nch open-drain output | Active "L"   |
| R type       | 9.0%             | Nch open-drain output | Active "L"   |

## ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.  
 Contact our sales representatives for details of AEC-Q100 reliability specification.

## ■ Product Name Structure

### 1. Product name



\*1. Refer to the tape drawing.

\*2. Refer to "2. Function list of product types".

### 2. Function list of product types

Table 1

| Product Type | Hysteresis Width | Pin Output Form       | Output Logic |
|--------------|------------------|-----------------------|--------------|
| L type       | 0%               | Nch open-drain output | Active "L"   |
| M type       | 2.3%             | Nch open-drain output | Active "L"   |
| N type       | 5.0%             | Nch open-drain output | Active "L"   |
| R type       | 9.0%             | Nch open-drain output | Active "L"   |

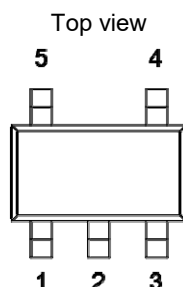
### 3. Packages

Table 2 Package Drawing Codes

| Package Name | Dimension    | Tape         | Reel         | Land          | Stencil Opening |
|--------------|--------------|--------------|--------------|---------------|-----------------|
| SOT-23-5     | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD | —             | —               |
| HSNT-6(2025) | PJ006-B-P-SD | PJ006-B-C-SD | PJ006-B-R-SD | PJ006-B-LM-SD | PJ006-B-LM-SD   |

## ■ Pin Configurations

### 1. SOT-23-5



**Figure 3**

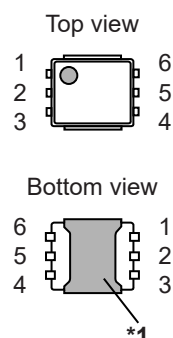
**Table 3**

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 1       | OUT    | Voltage detection output pin                               |
| 2       | VSS    | GND pin  |
| 3       | CD*1   | Connection pin for release delay time adjustment capacitor |
| 4       | SENSE  | Detection voltage input pin                                |
| 5       | VDD    | Voltage input pin  |

- \*1. Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

Moreover, the CD pin is available even when it is open.

### 2. HSNT-6(2025)



**Figure 4**

**Table 4**

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 1       | VDD    | Voltage input pin  |
| 2       | NC*2   | No connection  |
| 3       | SENSE  | Detection voltage input pin                                |
| 4       | CD*3   | Connection pin for release delay time adjustment capacitor |
| 5       | VSS    | GND pin  |
| 6       | OUT    | Voltage detection output pin                               |

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
- \*2. The NC pin is electrically open.  
The NC pin can be connected to the VDD pin or the VSS pin.
- \*3. Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.  
Moreover, the CD pin is available even when it is open.

## ■ Absolute Maximum Ratings

Table 5

(Ta = -40°C to +125°C unless otherwise specified)

| Item                          | Symbol             | Absolute Maximum Rating  | Unit |
|-------------------------------|--------------------|--|------|
| Power supply voltage          | V <sub>DD</sub>    | V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 45.0                        | V    |
| SENSE pin voltage             | V <sub>SENSE</sub> | V <sub>SS</sub> - 30.0 to V <sub>SS</sub> + 45.0                       | V    |
| CD pin input voltage          | V <sub>CD</sub>    | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
| Output voltage                | V <sub>OUT</sub>   | V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 45.0                        | V    |
| Output current                | I <sub>OUT</sub>   | 25   | mA   |
| Junction temperature          | T <sub>j</sub>     | -40 to +150  | °C   |
| Operation ambient temperature | T <sub>opr</sub>   | -40 to +125  | °C   |
| Storage temperature           | T <sub>stg</sub>   | -40 to +150  | °C   |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Thermal Resistance Value

Table 6

| Item                                     | Symbol        | Condition    |         | Min. | Typ. | Max. | Unit |
|--|---------------|--------------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | $\theta_{JA}$ | SOT-23-5     | Board A | —    | 192  | —    | °C/W |
|  |               |              | Board B | —    | 160  | —    | °C/W |
|  |               |              | Board C | —    | —    | —    | °C/W |
|  |               |              | Board D | —    | —    | —    | °C/W |
|  |               |              | Board E | —    | —    | —    | °C/W |
|  |               | HSNT-6(2025) | Board A | —    | 180  | —    | °C/W |
|  |               |              | Board B | —    | 128  | —    | °C/W |
|  |               |              | Board C | —    | 43   | —    | °C/W |
|  |               |              | Board D | —    | 44   | —    | °C/W |
|  |               |              | Board E | —    | 36   | —    | °C/W |

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

## ■ Electrical Characteristics

**Table 7**

(Ta = -40°C to +125°C unless otherwise specified)

| Item                           | Symbol             | Condition   | Min.                           | Typ.                        | Max.                           | Unit | Test Circuit |
|--------------------------------|--------------------|---|--------------------------------|-----------------------------|--------------------------------|------|--------------|
| Detection voltage*1            | V <sub>DET</sub>   | V <sub>DD</sub> = 13.5 V,<br>8.0 V ≤ V <sub>DET(S)</sub> ≤ 24.0 V   | V <sub>DET(S)</sub><br>× 0.985 | V <sub>DET(S)</sub>         | V <sub>DET(S)</sub><br>× 1.015 | V    | 1            |
| Hysteresis width*2             | V <sub>HYS</sub>   | L type<br>(V <sub>HYS</sub> = 0%)   | —                              | V <sub>DET</sub><br>× 0.00  | —                              | V    | 1            |
|                                |                    | M type<br>(V <sub>HYS</sub> = 2.3%)   | V <sub>DET</sub><br>× 0.013    | V <sub>DET</sub><br>× 0.023 | V <sub>DET</sub><br>× 0.033    | V    | 1            |
|                                |                    | N type<br>(V <sub>HYS</sub> = 5.0%)   | V <sub>DET</sub><br>× 0.04     | V <sub>DET</sub><br>× 0.05  | V <sub>DET</sub><br>× 0.06     | V    | 1            |
|                                |                    | R type<br>(V <sub>HYS</sub> = 9.0%)   | V <sub>DET</sub><br>× 0.08     | V <sub>DET</sub><br>× 0.09  | V <sub>DET</sub><br>× 0.10     | V    | 1            |
| Current consumption            | I <sub>SS1</sub>   | V <sub>DD</sub> = 13.5 V,<br>V <sub>SENSE</sub> = V <sub>REL(S)</sub> *3 - 1 V  | —                              | 2.0                         | 3.5                            | μA   | 2            |
| Operation voltage              | V <sub>DD</sub>    | —   | 3.0                            | —                           | 36.0                           | V    | —            |
| Output current                 | I <sub>OUT</sub>   | OUT pin Nch driver,<br>V <sub>DD</sub> = 3.0 V, V <sub>DS</sub> *4 = 0.1 V,<br>V <sub>SENSE</sub> = V <sub>DET(S)</sub> + 1 V | 0.60                           | —                           | —                              | mA   | 3            |
| Leakage current                | I <sub>LEAK</sub>  | OUT pin Nch driver,<br>V <sub>DD</sub> = 36 V, V <sub>OUT</sub> = 36 V,<br>V <sub>SENSE</sub> = V <sub>REL(S)</sub> *3 - 1 V  | —                              | —                           | 2.0                            | μA   | 3            |
| Detection response time*5      | t <sub>RESET</sub> | —   | —                              | —                           | 6.8                            | μs   | 4            |
| Release delay time*6           | t <sub>DELAY</sub> | C <sub>D</sub> = 3.3 nF   | 8.0                            | 10.0                        | 12.0                           | ms   | 4            |
| SENSE pin resistance           | R <sub>SENSE</sub> | —   | 13.7                           | 35.8                        | 83.3                           | MΩ   | 2            |
| CD pin discharge ON resistance | R <sub>CDD</sub>   | V <sub>DD</sub> = 3.0 V, V <sub>CD</sub> = 0.5 V  | 0.15                           | —                           | 1.00                           | kΩ   | —            |

\*1. V<sub>DET</sub>: Actual detection voltage value, V<sub>DET(S)</sub>: Set detection voltage value

\*2. The Release voltage (V<sub>REL</sub>) is as follows.

L type (hysteresis width "Unavailable"):

$$V_{REL} = V_{DET}$$

M / N / R type (hysteresis width "Available"):

$$V_{REL} = V_{DET} - V_{HYS}$$

\*3. V<sub>REL(S)</sub>: Set release voltage value

\*4. V<sub>DS</sub>: Drain-to-source voltage of the output transistor

\*5. The time period from when the pulse voltage of V<sub>DET(S)</sub> - 1.0 V → V<sub>DET(S)</sub> + 1.0 V is applied to the SENSE pin after V<sub>SENSE</sub> reaches the release voltage once, until V<sub>OUT</sub> reaches 50% of V<sub>DD</sub>.

\*6. The time period from when the pulse voltage of V<sub>REL(S)</sub> + 1.0 V → V<sub>REL(S)</sub> - 1.0 V is applied to the SENSE pin to when V<sub>OUT</sub> reaches 50% of V<sub>DD</sub>.

## ■ Test Circuits

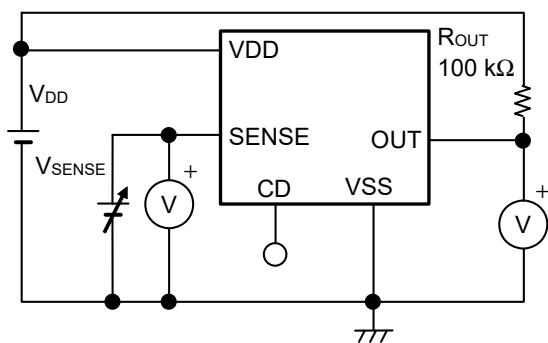


Figure 5 Test Circuit 1

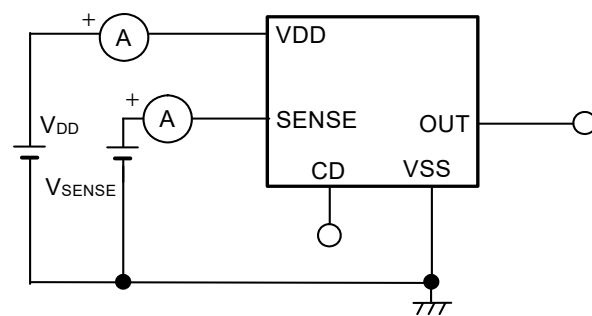


Figure 6 Test Circuit 2

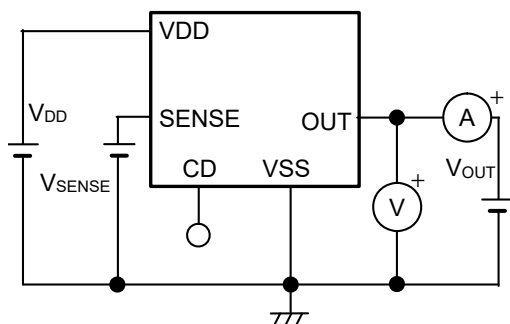


Figure 7 Test Circuit 3

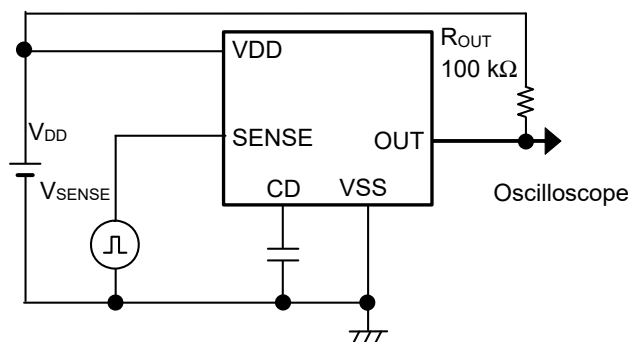
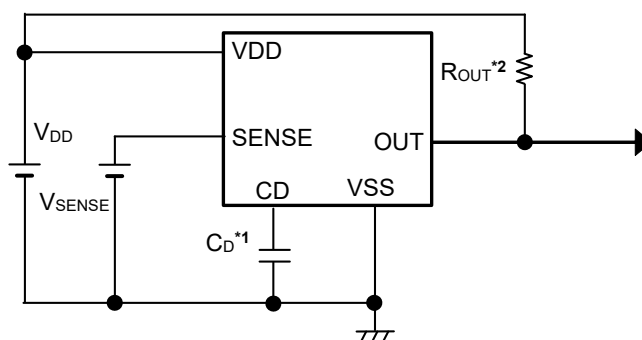


Figure 8 Test Circuit 4



## ■ Standard Circuit



- \*1.  $C_D$  is a release delay time adjustment capacitor. The  $C_D$  should be connected directly to the CD pin and the VSS pin.
- \*2.  $R_{OUT}$  is the external pull-up resistors for the output pin.

Figure 9

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

## ■ Selection of Release Delay Time Adjustment Capacitor ( $C_D$ )

In this IC, the release delay time adjustment capacitor ( $C_D$ ) is necessary between the CD pin and the VSS pin to adjust the release delay time ( $t_{DELAY}$ ) of the detector. Refer to "3. Delay circuit" in "■ Operation" for details.

**Caution** Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_D$ .

## ■ Explanation of Terms

### 1. Detection voltage ( $V_{DET}$ )

The detection voltage is a SENSE pin voltage at which the output voltage in **Figure 12** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum and the maximum is called the detection voltage range (Refer to "**Figure 10 Detection Voltage**").

Example: In  $V_{DET} = 10.0 \text{ V}$  product, the detection voltage is at any point in the range of  $9.85 \text{ V} \leq V_{DET} \leq 10.15 \text{ V}$ .  
 This means that some  $V_{DET} = 10.0 \text{ V}$  product has  $V_{DET} = 9.85 \text{ V}$  and some has  $V_{DET} = 10.15 \text{ V}$ .

### 2. Release voltage ( $V_{REL}$ )

The release voltage is a SENSE pin voltage at which the output voltage in **Figure 12** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum and the maximum is called the release voltage range (Refer to "**Figure 11 Release Voltage**").  
 The release voltage becomes the value differs from the detection voltage within the range shown below.

- M type: 1.3% to 3.3% (2.3% typ.)
- N type: 4% to 6% (5% typ.)
- R type: 8% to 10% (9% typ.)

Example: For R type,  $V_{DET} = 10.0 \text{ V}$  product, the release voltage is at any point in the range of  $8.865 \text{ V} \leq V_{REL} \leq 9.338 \text{ V}$  despite  $V_{REL} = 9.1 \text{ V}$  typ.

This means that some R type,  $V_{DET} = 10.0 \text{ V}$  product has  $V_{REL} = 8.865 \text{ V}$  and some has  $V_{REL} = 9.338 \text{ V}$ .

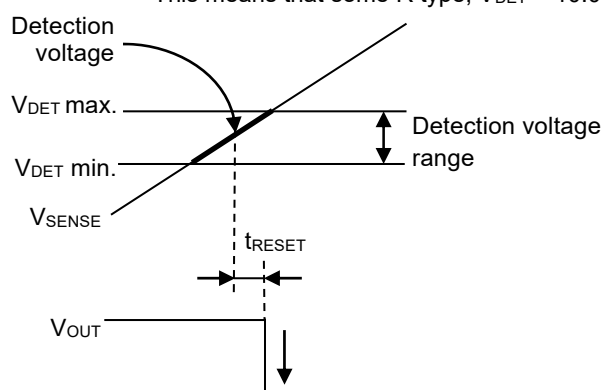


Figure 10 Detection Voltage

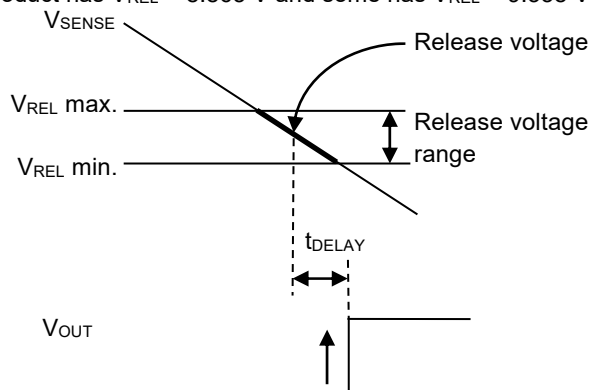


Figure 11 Release Voltage

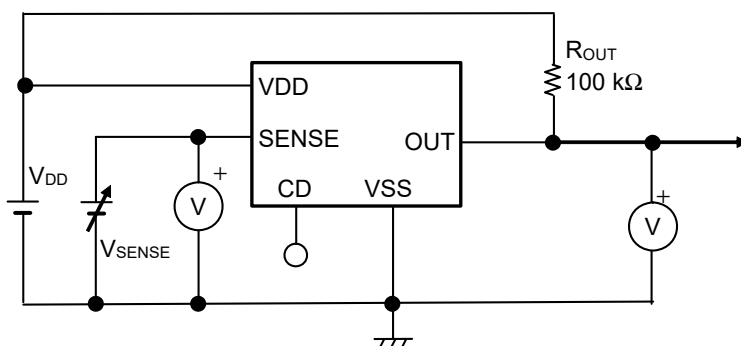


Figure 12 Test Circuit of Detection Voltage and Release Voltage

### 3. Hysteresis width ( $V_{HYS}$ )

The hysteresis width is the voltage difference between the detection voltage ( $V_{DET}$ ) and the release voltage ( $V_{REL}$ ). Voltage difference between  $V_{DET}$  and  $V_{REL}$  is the hysteresis width ( $V_{HYS}^{*1}$ ) of the OUT pin. Setting the hysteresis width between  $V_{DET}$  and  $V_{REL}$ , prevents malfunction caused by noise on the input voltage.

\*1. Refer to "1.2 S-19116 Series M / N / R type" in "■ Operation" for details.

### 4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

## ■ Operation

### 1. Basic operation

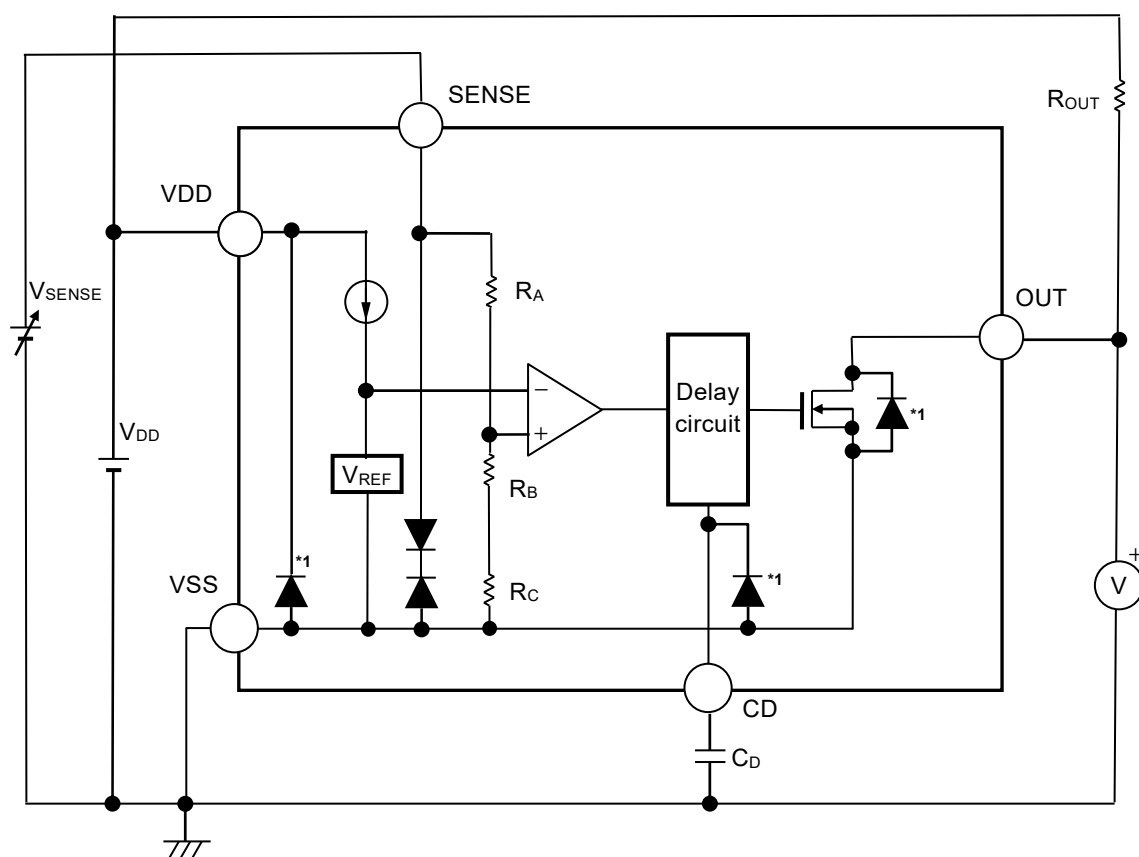
Figure 13 and Figure 15 show that the OUT pin being pulled up by resistors ( $R_{OUT}$ ) is an example of basic operation.

#### 1.1 S-19116 Series L type

- (1) When the power supply voltage ( $V_{DD}$ ) is the minimum operation voltage or higher, and the SENSE pin voltage ( $V_{SENSE}$ ) is lower than the detection voltage ( $V_{DET}$ ), the Nch transistor on the output side is turned off. And then  $V_{DD}$  ("H") is output from the OUT pin when the output is pulled up.

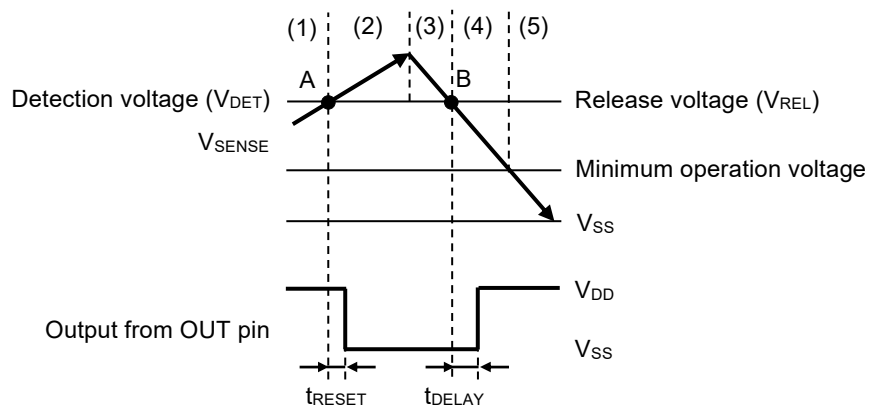
At this time, the input voltage to the comparator is  $\frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C}$ .

- (2) When  $V_{SENSE}$  increases to  $V_{DET}$  or higher (point A in Figure 14), the Nch transistor on the output side is turned on. And then  $V_{SS}$  ("L") is output from the OUT pin after the elapse of the detection response time ( $t_{RESET}$ ).
- (3) When  $V_{SENSE}$  decreases but is still equal to or higher than the release voltage ( $V_{REL}$ ),  $V_{SS}$  is output.
- (4) If  $V_{SENSE}$  decreases to  $V_{REL}$  or lower (point B in Figure 14), the Nch transistor on the output side is turned off. And then  $V_{DD}$  is output from the OUT pin after the elapse of the release delay time ( $t_{DELAY}$ ) when the output is pulled up.
- (5) Even if  $V_{SENSE}$  further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when  $V_{DD}$  is minimum operation voltage or higher.



\*1. Parasitic diode

Figure 13 Operation of S-19116 Series L type



**Remark** The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

**Figure 14 Timing Chart of S-19116 Series L Type**

## 1.2 S-19116 Series M / N / R type

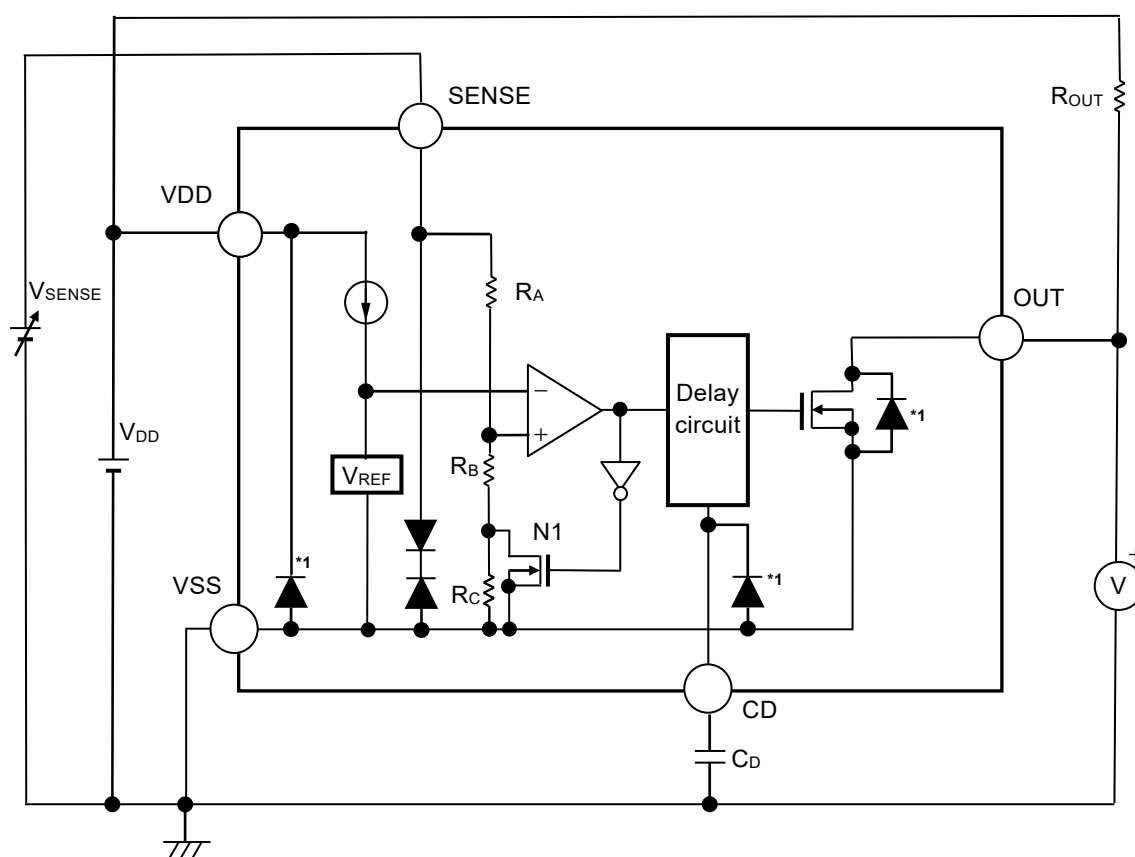
- (1) When the power supply voltage ( $V_{DD}$ ) is the minimum operation voltage or higher, and the SENSE pin voltage ( $V_{SENSE}$ ) is lower than the detection voltage ( $V_{DET}$ ), the Nch transistor on the output side is turned off. And then  $V_{DD}$  ("H") is output from the OUT pin when the output is pulled up.

Since the Nch transistor (N1) is turned on, the input voltage to the comparator is  $\frac{R_B \cdot V_{SENSE}}{R_A + R_B}$ .

- (2) Even if  $V_{SENSE}$  increases to the release voltage ( $V_{REL}$ ) or higher,  $V_{DD}$  is output when  $V_{SENSE}$  is lower than  $V_{DET}$ . When  $V_{SENSE}$  further increases to  $V_{DET}$  or higher (point A in **Figure 16**), the Nch transistor on the output side is turned on. And then  $V_{SS}$  ("L") is output from the OUT pin after the elapse of the detection response time ( $t_{RESET}$ ).

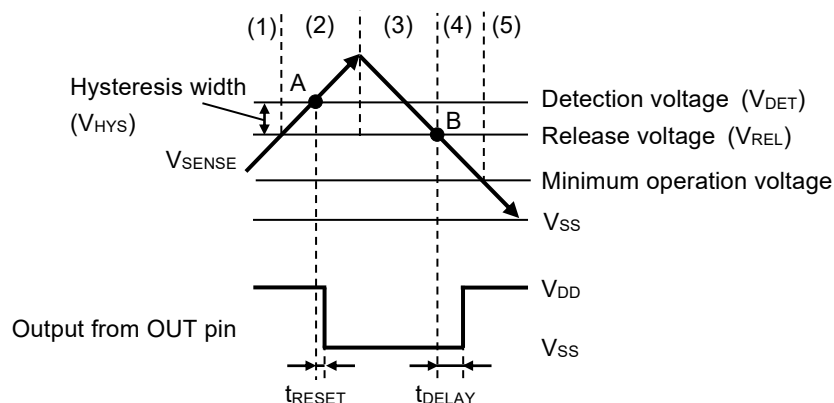
At this time, N1 is turned off, and the input voltage to the comparator is  $\frac{(R_B + R_C) \cdot V_{SENSE}}{R_A + R_B + R_C}$ .

- (3) Even if  $V_{SENSE}$  decreases to  $V_{DET}$  or lower,  $V_{SS}$  is output when  $V_{SENSE}$  is higher than  $V_{REL}$ .  
 (4) If  $V_{SENSE}$  decreases to  $V_{REL}$  or lower (point B in **Figure 16**), the Nch transistor on the output side is turned off. And then  $V_{DD}$  is output from the OUT pin after the elapse of the release delay time ( $t_{DELAY}$ ) when the output is pulled up.  
 (5) Even if  $V_{SENSE}$  further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when  $V_{DD}$  is minimum operation voltage or higher.



\*1. Parasitic diode

Figure 15 Operation of S-19116 Series M / N / R type



**Figure 16 Timing Chart of S-19116 Series M / N / R Type**

## 2. SENSE pin

The SENSE pin is the input pin for the detection voltage. The power supply VDD pin and SENSE pin, for voltage detection, are divided. Therefore, as long as a voltage is supplied to the VDD pin, the reset signal will be held even if the input voltage to the SENSE pin drops below the minimum operation voltage. Also, the SENSE pin of this IC has a built-in reverse connection protection circuit. Even when the SENSE pin voltage is less than the VSS pin voltage, the current flowing from the VSS pin to the SENSE pin is reduced to 0.05 mA typ.

### 2.1 Error when detection voltage is set externally

The detection voltage can be set externally by connecting a node that was resistance-divided by the resistor ( $R_A$ ) and the resistor ( $R_B$ ) to the SENSE pin as shown in **Figure 17**.

For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.

In this IC,  $R_A$  and  $R_B$  in **Figure 17** are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance ( $R_{SENSE}$ ) that will occur.

Although  $R_{SENSE}^{*1}$  in this IC is large to make the error small,  $R_A$  and  $R_B$  should be selected such that the error is within the allowable limits.

\*1. 13.7 MΩ min.

## 2.2 Selection of $R_A$ and $R_B$

In **Figure 17**, the relation between the external setting detection voltage ( $V_{DX}$ ) and the actual detection voltage ( $V_{DET}$ ) is ideally calculated by the equation below.

$$V_{DX} = V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \cdots \cdots (1)$$

However, in reality there is an error in the current flowing through  $R_{SENSE}$ .

When considering this error, the relation between  $V_{DX}$  and  $V_{DET}$  is calculated as follows.

$$\begin{aligned} V_{DX} &= V_{DET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\ &= V_{DET} \times \left(1 + \frac{R_A}{\frac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{DET} \cdots \cdots (2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as  $V_{DET} \times \frac{R_A}{R_{SENSE}}$ .

The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100 [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100 [\%] \cdots \cdots (3)$$

As seen in equation (3), the smaller the resistance values of  $R_A$  and  $R_B$  compared to  $R_{SENSE}$ , the smaller the error rate becomes.

Also, the relation between the external setting hysteresis width ( $V_{HX}$ ) and the hysteresis width ( $V_{HYS}$ ) is calculated by equation below. Error due to  $R_{SENSE}$  also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \cdots \cdots (4)$$

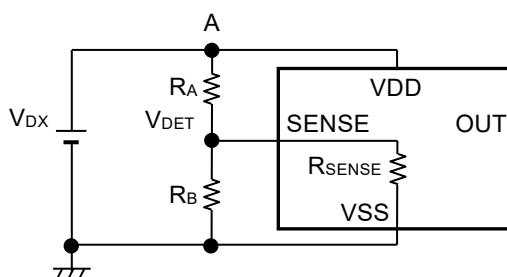


Figure 17 Detection Voltage External Setting Circuit

**Caution** If  $R_A$  and  $R_B$  are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.



### 3. Delay circuit

The delay circuit has a function that adjusts the release delay time ( $t_{\text{DELAY}}$ ) from when the SENSE pin voltage ( $V_{\text{SENSE}}$ ) descends the release voltage ( $V_{\text{REL}} = V_{\text{DET}} - V_{\text{HYS}}$ ) or lower to when the output from OUT pin inverts.

$t_{\text{DELAY}}$  is determined by the delay coefficient, the release delay time adjustment capacitor ( $C_D$ ) and the release delay time when the CD pin is open ( $t_{\text{DELAY0}}$ ). They are calculated by the equations below.

$$t_{\text{DELAY}} [\text{ms}] = \text{Delay coefficient} \times C_D [\text{nF}] + t_{\text{DELAY0}} [\text{ms}]$$

**Table 8**

| Operation Temperature | Delay Coefficient |      |      |
|-----------------------|-------------------|------|------|
|                       | Min.              | Typ. | Max. |
| Ta = -40°C to +125°C  | 2.76              | 3.00 | 3.28 |

**Table 9**

| Operation Temperature | Release Delay Time when CD Pin is Open<br>( $t_{\text{DELAY0}}$ ) |      |      |
|-----------------------|---|------|------|
|                       | Min.  | Typ. | Max. |
| Ta = -40°C to +125°C  | 0.01  | 0.04 | 0.23 |

- Caution 1.** Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
- There is no limit for the capacitance of  $C_D$  as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 350 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.
  - The above equations will not guarantee successful operation. Determine the capacitance of  $C_D$  through thorough evaluation including temperature characteristics in the actual usage conditions.

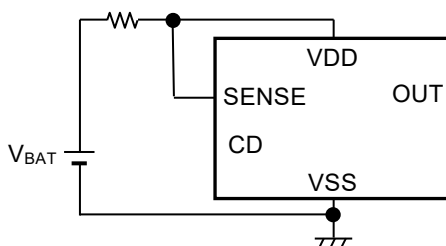
## ■ Usage Precautions

### 1. Feed-through current at the time of detection and release

In this IC, a feed-through current flows instantaneously at the time of detection and release. Therefore, if the input impedance is increased, oscillation may occur due to the voltage drop caused by the feed-through current.

When this IC is used in the configuration shown in **Figure 18**, the input impedance is recommended to be 1.0 kΩ or less.

Perform a sufficient evaluation including the temperature characteristics under the actual operating conditions.



**Figure 18**

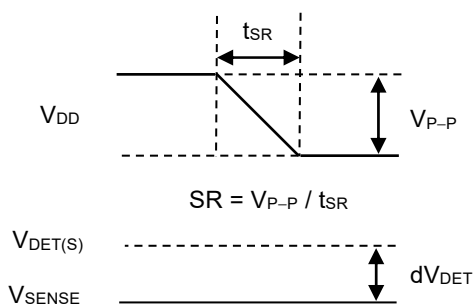
### 2. Power down (Reference)

As shown in **Figure 19**, when the VDD pin voltage ( $V_{DD}$ ) falls sharply in the state of  $V_{SENSE} < V_{DET}$ , the OUT pin may be detected. So be careful.

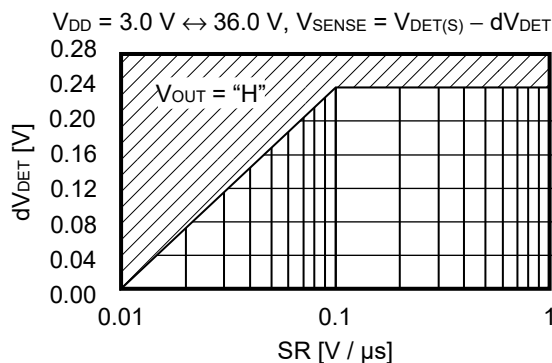
**Figure 20** shows the relationship between the  $dV_{DET}^{*1}$  that can hold the released state and the falling slew rate (SR) of  $V_{DD}$ .

Please perform a sufficient evaluation with the actual machine when using it.

\*1.  $dV_{DET}$ : Difference between  $V_{DET(S)}$  and  $V_{SENSE}$



**Figure 19**



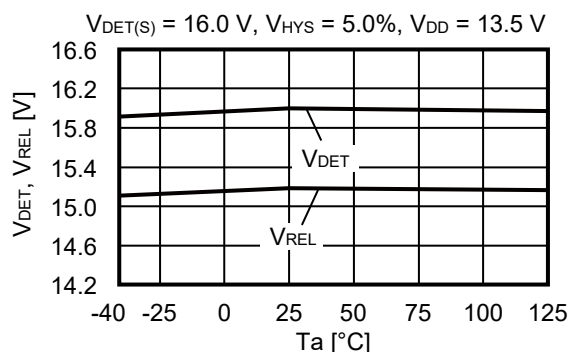
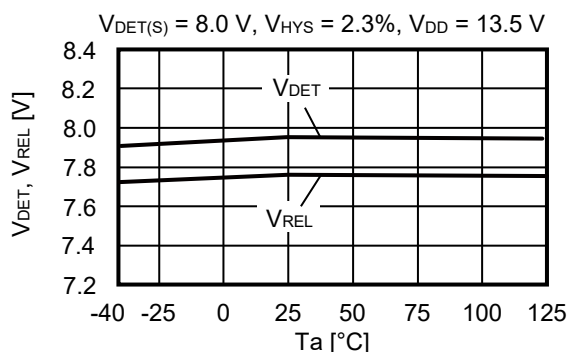
**Figure 20**

## ■ Precautions

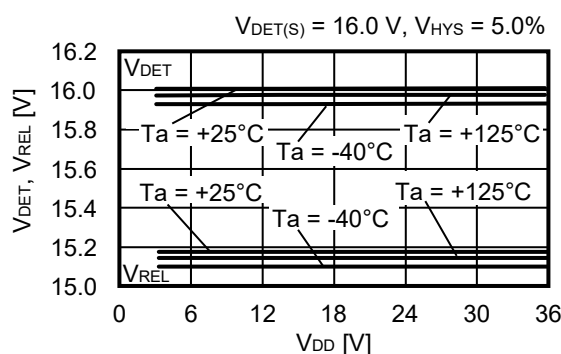
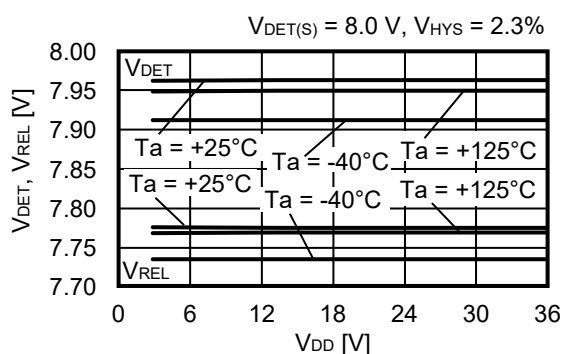
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise.  
Be careful of wiring adjoining SENSE pin wiring in actual applications.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Characteristics (Typical Data)

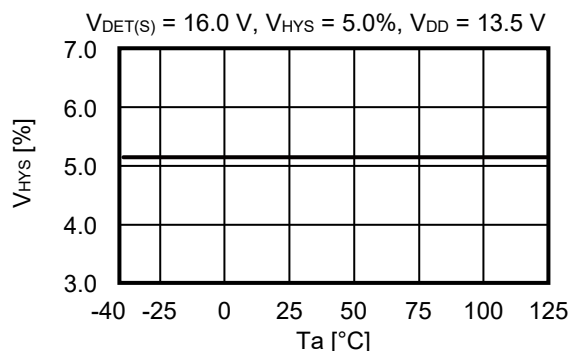
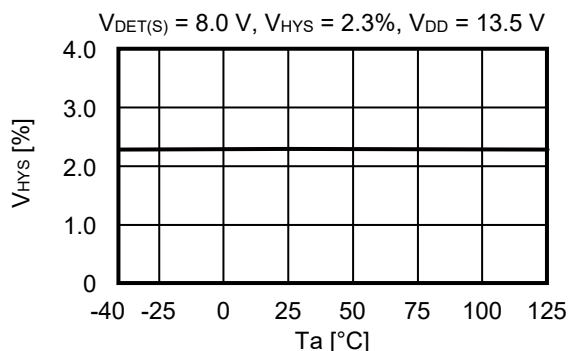
### 1. Detection voltage ( $V_{DET}$ ), Release voltage ( $V_{REL}$ ) vs. Temperature ( $T_a$ )



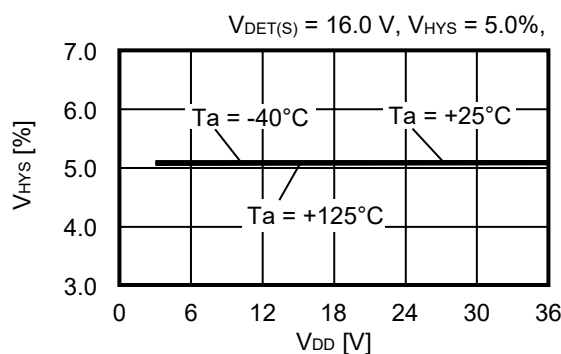
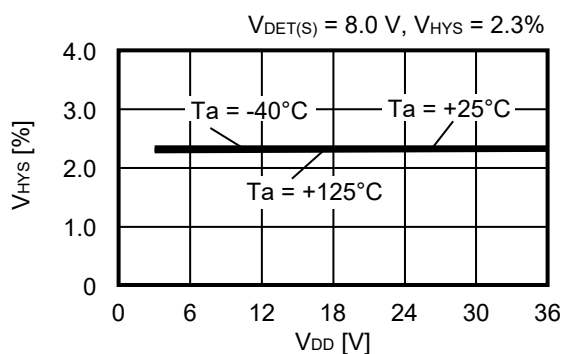
### 2. Detection voltage ( $V_{DET}$ ), Release voltage ( $V_{REL}$ ) vs. Power supply voltage ( $V_{DD}$ )



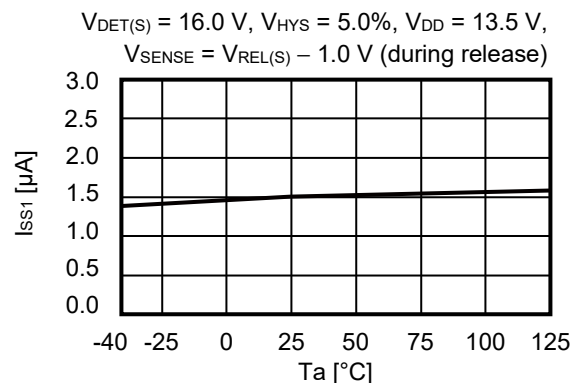
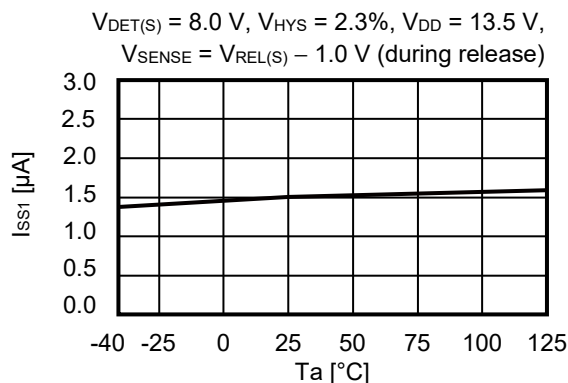
### 3. Hysteresis width ( $V_{HYS}$ ) vs. Temperature ( $T_a$ )



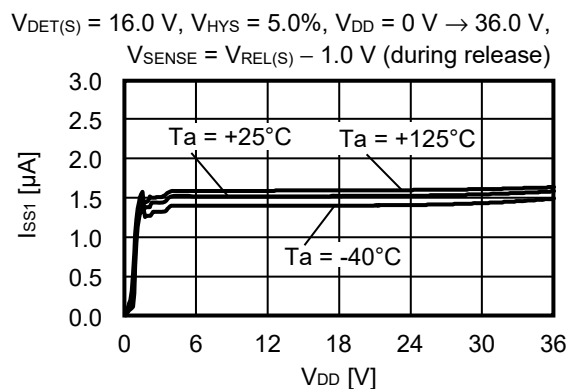
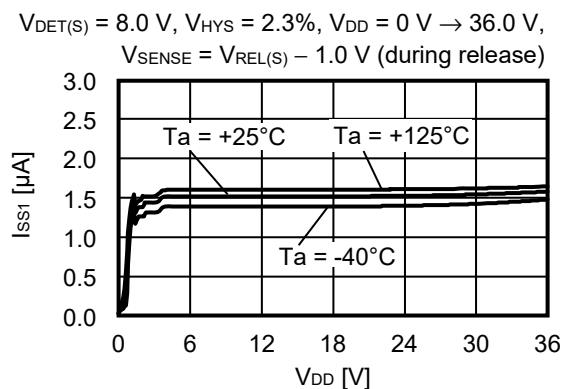
### 4. Hysteresis width ( $V_{HYS}$ ) vs. Power supply voltage ( $V_{DD}$ )



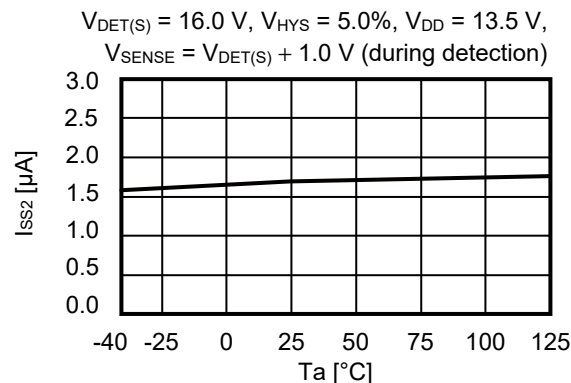
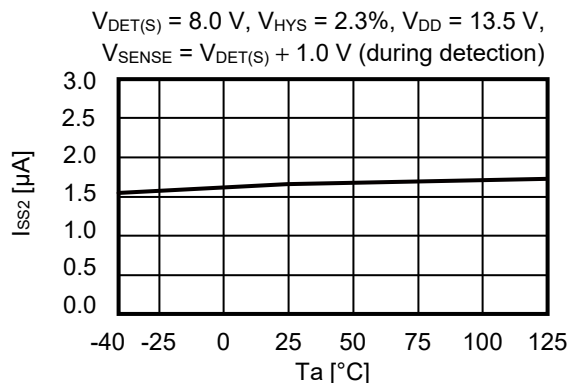
## 5. Current consumption ( $I_{SS1}$ ) vs. Temperature ( $T_a$ )



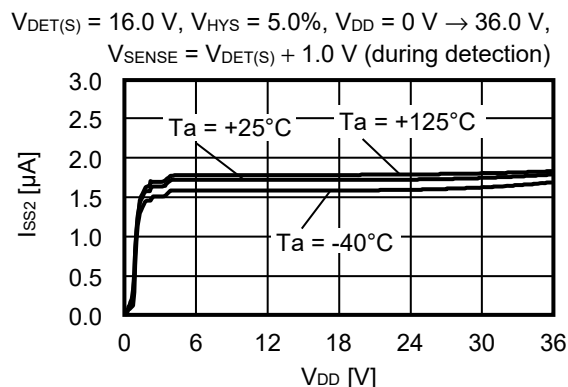
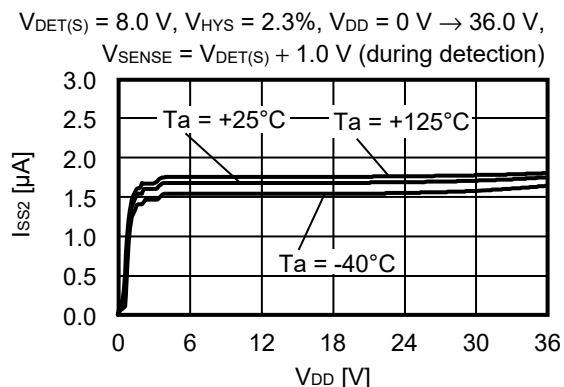
## 6. Current consumption ( $I_{SS1}$ ) vs. Power supply voltage ( $V_{DD}$ )



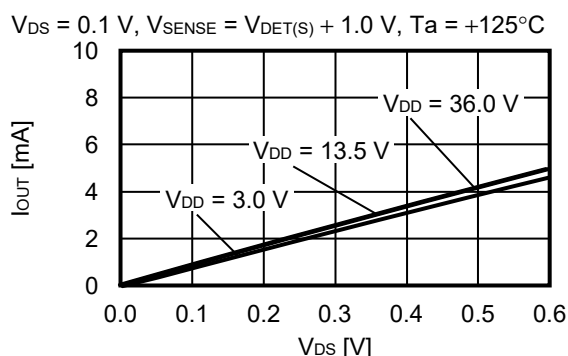
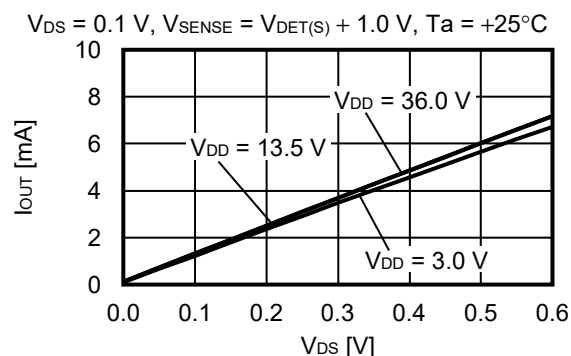
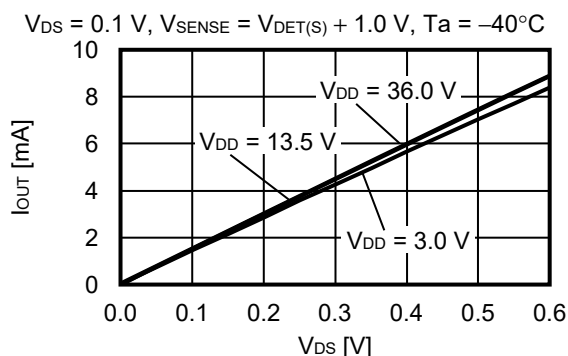
## 7. Current consumption ( $I_{SS2}$ ) vs. Temperature ( $T_a$ )



## 8. Current consumption ( $I_{SS2}$ ) vs. Power supply voltage ( $V_{DD}$ )

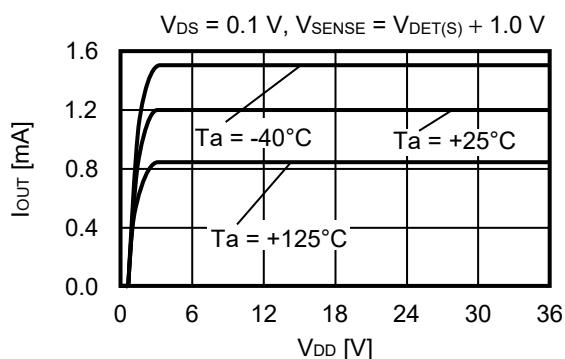


## 9. Nch transistor output current ( $I_{OUT}$ ) vs. $V_{DS}$



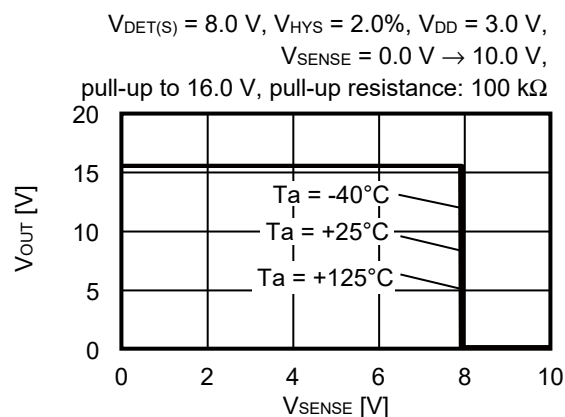
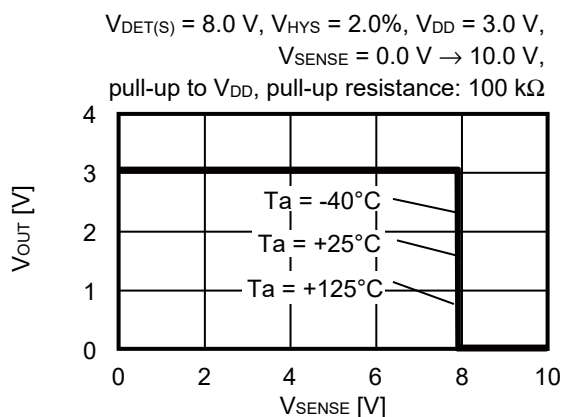
**Remark**  $V_{DS}$ : Drain-to-source voltage of the output transistor

## 10. Nch transistor output current ( $I_{OUT}$ ) vs. Power supply voltage ( $V_{DD}$ )

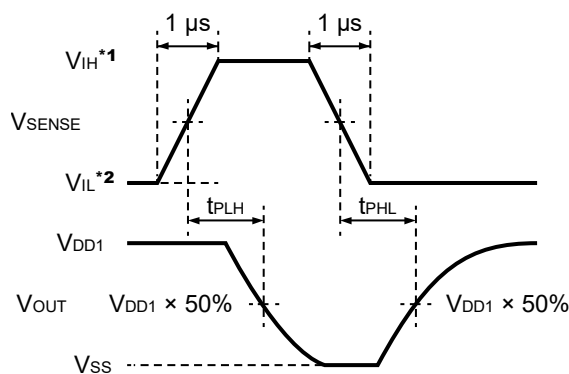
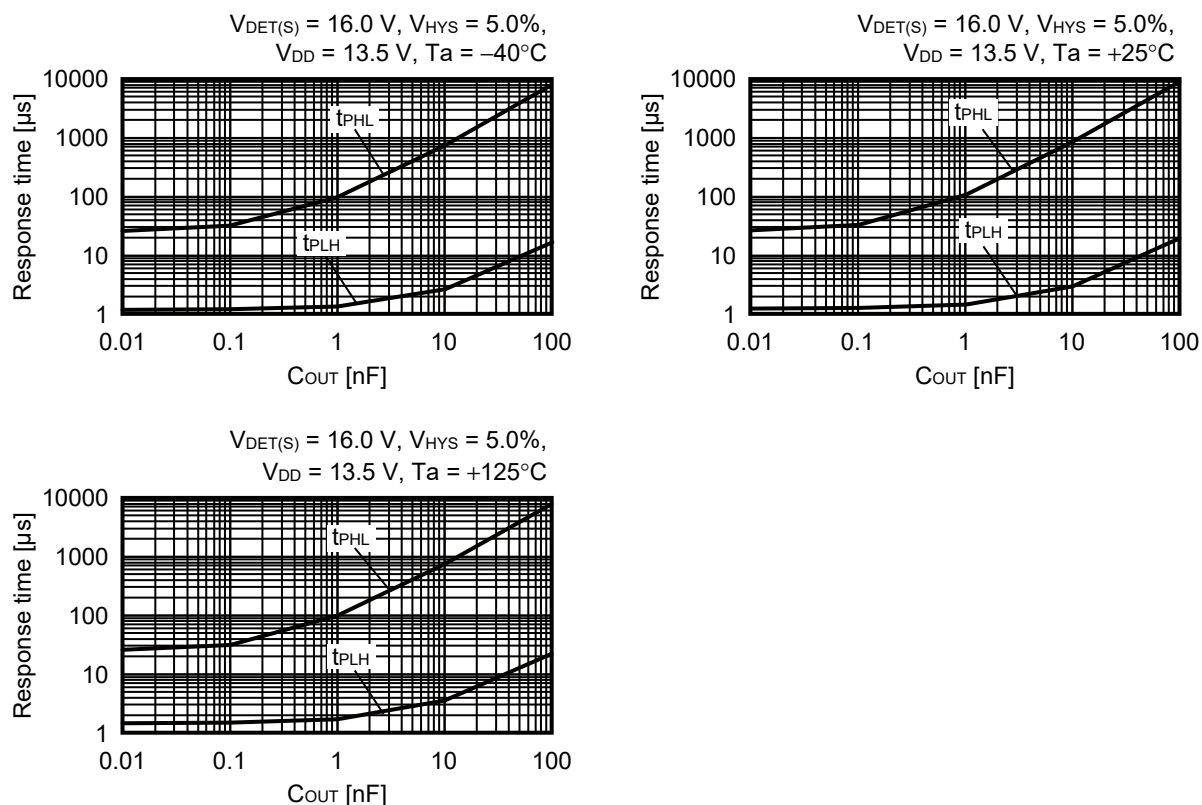


**Remark**  $V_{DS}$ : Drain-to-source voltage of the output transistor

## 11. Output voltage ( $V_{OUT}$ ) vs. SENSE pin voltage ( $V_{SENSE}$ )

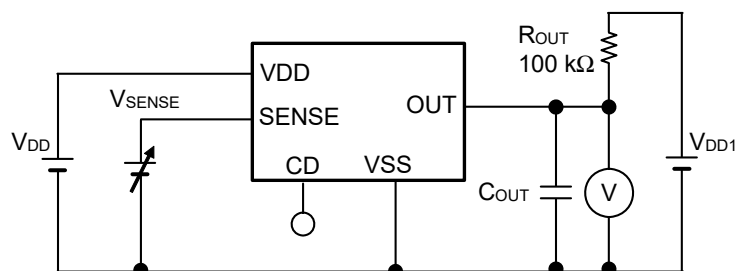


## 12. Dynamic response vs. Output pin capacitance ( $C_{OUT}$ ) (CD pin; open)



- \*1.  $t_{PLH}$ :  $V_{IH} = V_{DET(S)} + 1.0$  V,  $t_{PHL}$ :  $V_{IH} = V_{REL(S)} + 1.0$  V  
 \*2.  $t_{PLH}$ :  $V_{IL} = V_{DET(S)} - 1.0$  V,  $t_{PHL}$ :  $V_{IL} = V_{REL(S)} - 1.0$  V

**Figure 21 Test Condition of Response Time**

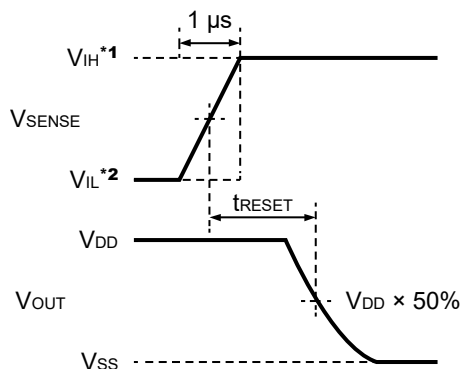
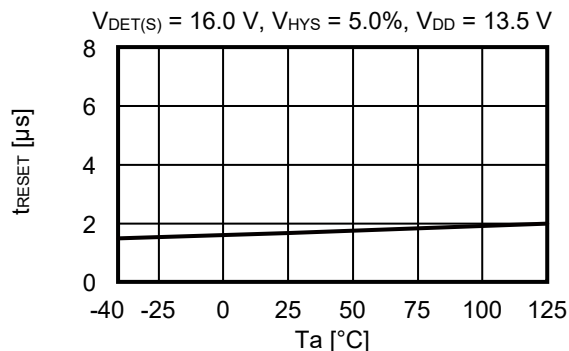


**Figure 22 Test Circuit of Response Time**

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

## ■ Reference Data

### 1. Detection response time ( $t_{\text{RESET}}$ ) vs. Temperature ( $T_a$ )



- \*1.  $V_{\text{IH}} = V_{\text{DET(S)}} + 1.0 \text{ V}$
- \*2.  $V_{\text{IL}} = V_{\text{DET(S)}} - 1.0 \text{ V}$

### 2. Detection response time ( $t_{\text{RESET}}$ ) vs. Power supply voltage ( $V_{\text{DD}}$ )

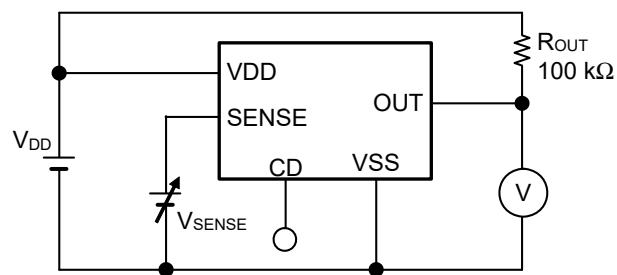
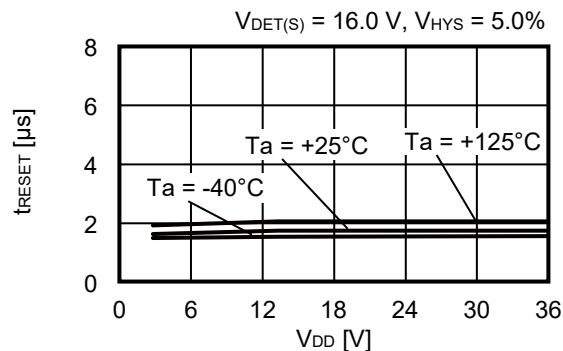


Figure 23 Test Condition of Detection Response Time

Figure 24 Test Circuit of Detection Response Time

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

### 3. Detection response time ( $t_{\text{RESET}}$ ) vs. Overdrive voltage ( $V_{\text{Overdrive}}$ )

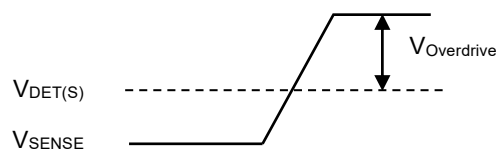
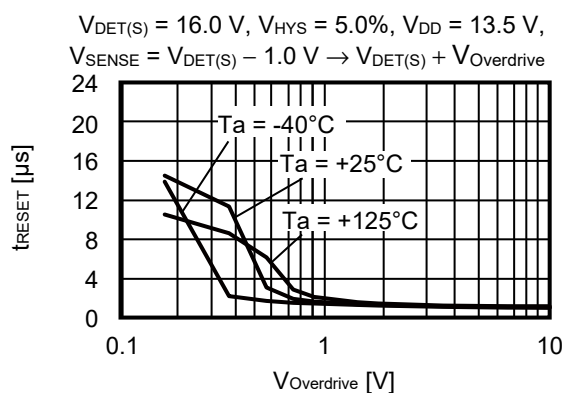
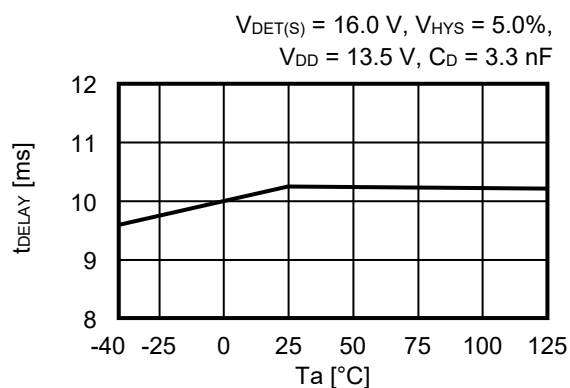


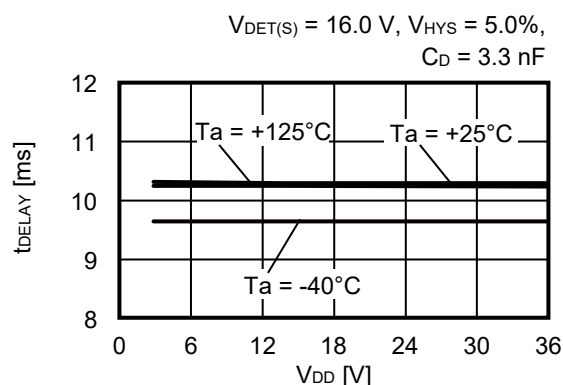
Figure 25



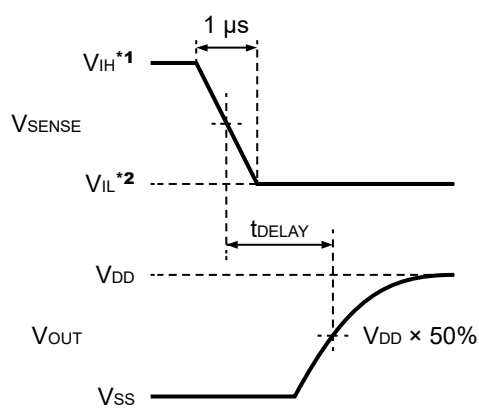
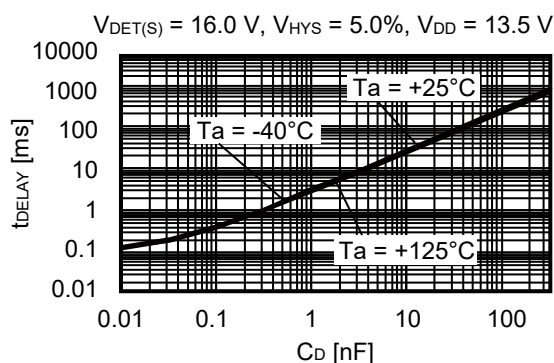
**4. Release delay time ( $t_{\text{DELAY}}$ ) vs. Temperature ( $T_a$ )**



**5. Release delay time ( $t_{\text{DELAY}}$ ) vs. Power supply voltage ( $V_{\text{DD}}$ )**

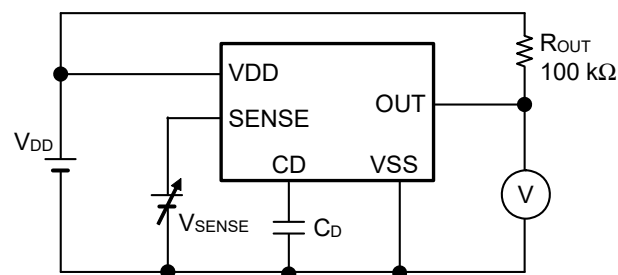


**6. Release delay time ( $t_{\text{DELAY}}$ ) vs. CD pin capacitance ( $C_D$ ) (Without output pin capacitance)**



- \*1.  $V_{\text{IH}} = V_{\text{REL(S)}} + 1.0 \text{ V}$
- \*2.  $V_{\text{IL}} = V_{\text{REL(S)}} - 1.0 \text{ V}$

**Figure 26 Test Condition of Release Delay Time**



**Figure 27 Test Circuit of Release Delay Time**

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

## 7. Load dump characteristics (Ta = +25°C)

### 7.1 $V_{DET(S)} = 17.0\text{ V}$ , $V_{HYS} = 5.0\%$

$V_{DD} = V_{SENSE} = 13.5\text{ V} \leftrightarrow 45.0\text{ V}$ ,  
 $C_D = 3.3\text{ nF}$

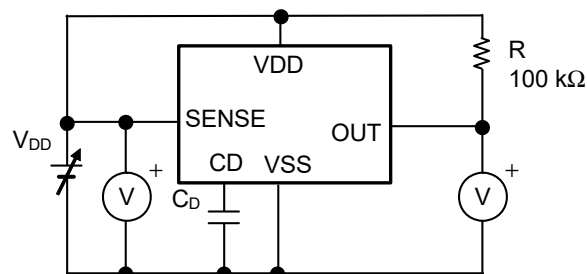
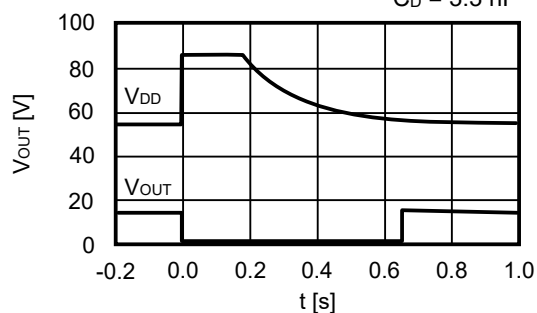
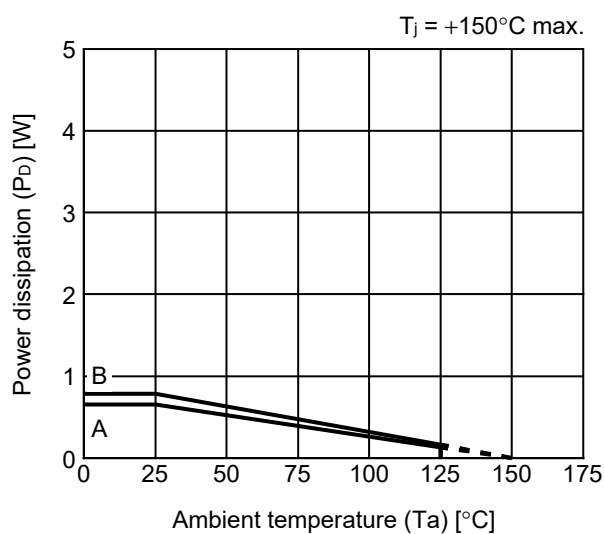


Figure 28

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

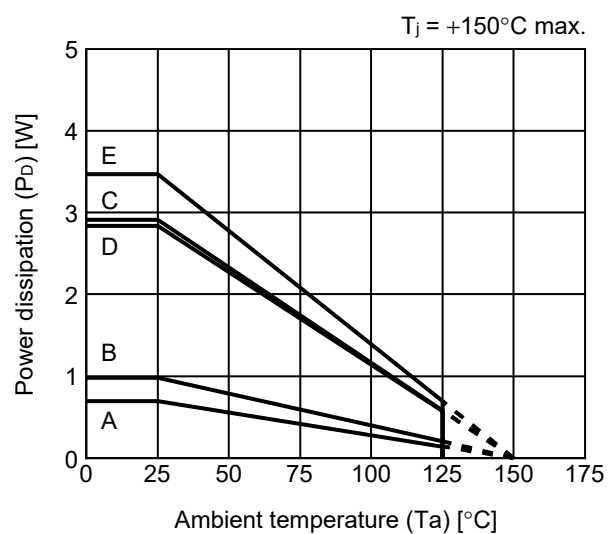
## ■ Power Dissipation

### SOT-23-5



| Board | Power Dissipation ( $P_D$ ) |
|-------|-----------------------------|
| A     | 0.65 W                      |
| B     | 0.78 W                      |
| C     | —                           |
| D     | —                           |
| E     | —                           |

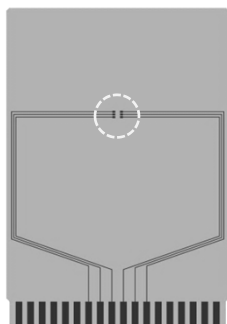
### HSNT-6(2025)



| Board | Power Dissipation ( $P_D$ ) |
|-------|-----------------------------|
| A     | 0.69 W                      |
| B     | 0.98 W                      |
| C     | 2.91 W                      |
| D     | 2.84 W                      |
| E     | 3.47 W                      |

# SOT-23-3/3S/5/6 Test Board

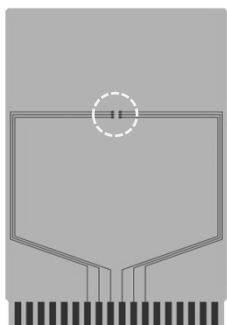
(1) Board A



 IC Mount Area

| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 2   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | -   |
|                             | 3 | -   |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | -   |

(2) Board B



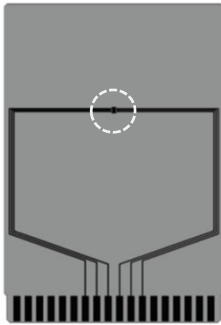
| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 4   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | 74.2 x 74.2 x t0.035                        |
|                             | 3 | 74.2 x 74.2 x t0.035                        |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | -   |

No. SOT23x-A-Board-SD-2.0

# HSNT-6(2025) Test Board

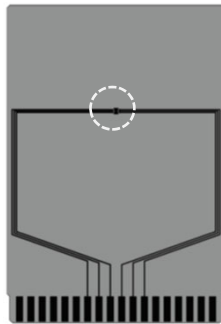
 IC Mount Area

(1) Board A



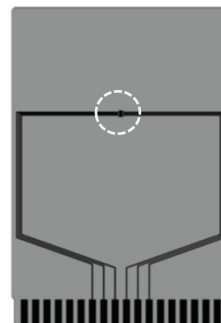
| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 2   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | -   |
|                             | 3 | -   |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | -   |

(2) Board B



| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 4   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | 74.2 x 74.2 x t0.035                        |
|                             | 3 | 74.2 x 74.2 x t0.035                        |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | -   |

(3) Board C



| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 4   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | 74.2 x 74.2 x t0.035                        |
|                             | 3 | 74.2 x 74.2 x t0.035                        |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | Number: 4<br>Diameter: 0.3 mm               |



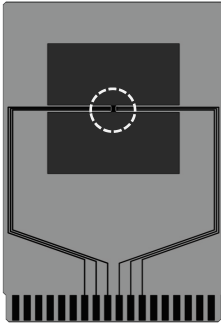
enlarged view

No. HSNT6-B-Board-SD-1.0

# HSNT-6(2025) Test Board



## (4) Board D

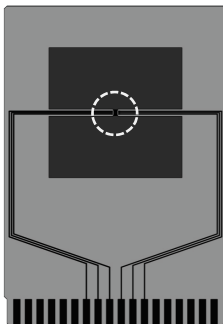


| Item                        |   | Specification  |
|-----------------------------|---|--|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                                    |
| Material                    |   | FR-4   |
| Number of copper foil layer |   | 4  |
| Copper foil layer [mm]      | 1 | Pattern for heat radiation: 2000mm <sup>2</sup> t0.070 |
|                             | 2 | 74.2 x 74.2 x t0.035                                   |
|                             | 3 | 74.2 x 74.2 x t0.035                                   |
|                             | 4 | 74.2 x 74.2 x t0.070                                   |
| Thermal via                 |   | -  |



enlarged view

## (5) Board E

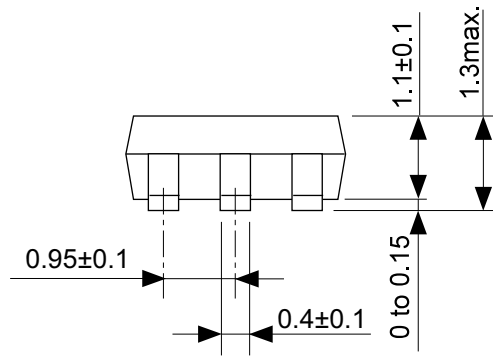
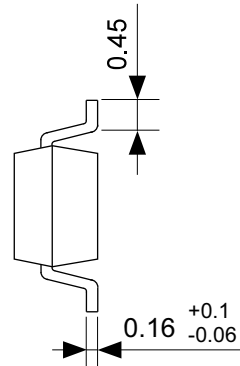
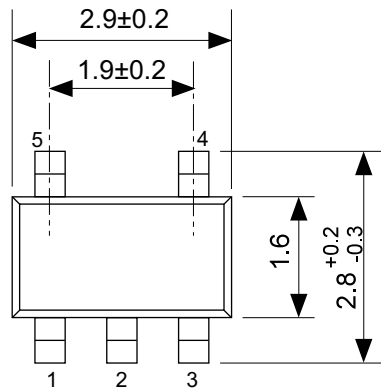


| Item                        |   | Specification  |
|-----------------------------|---|--|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                                    |
| Material                    |   | FR-4   |
| Number of copper foil layer |   | 4  |
| Copper foil layer [mm]      | 1 | Pattern for heat radiation: 2000mm <sup>2</sup> t0.070 |
|                             | 2 | 74.2 x 74.2 x t0.035                                   |
|                             | 3 | 74.2 x 74.2 x t0.035                                   |
|                             | 4 | 74.2 x 74.2 x t0.070                                   |
| Thermal via                 |   | Number: 4<br>Diameter: 0.3 mm                          |




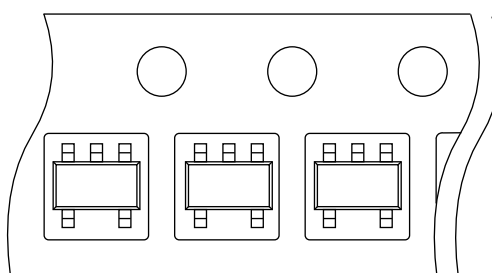
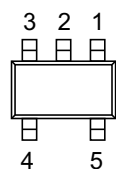
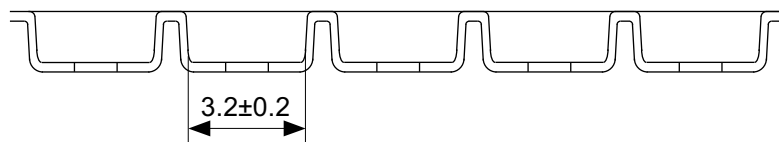
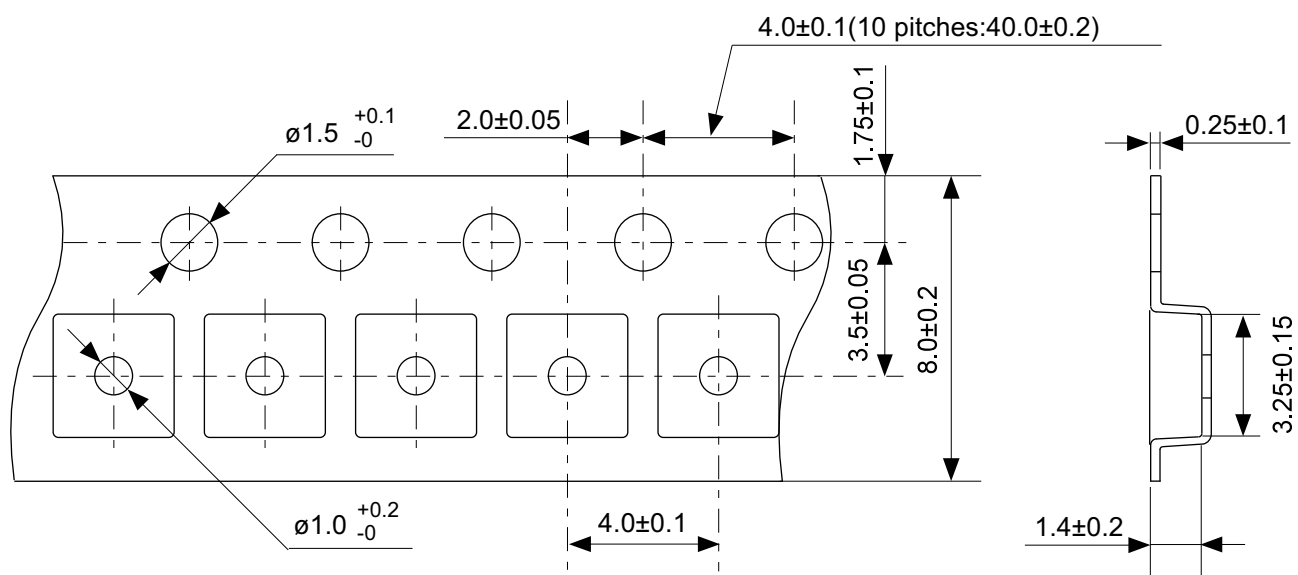
enlarged view

No. HSNT6-B-Board-SD-1.0



No. MP005-A-P-SD-1.3

|            |   |
|------------|---|
| TITLE      | SOT235-A-PKG Dimensions   |
| No.        | MP005-A-P-SD-1.3  |
| ANGLE      |  |
| UNIT       | mm  |
|            |   |
| ABLIC Inc. |   |

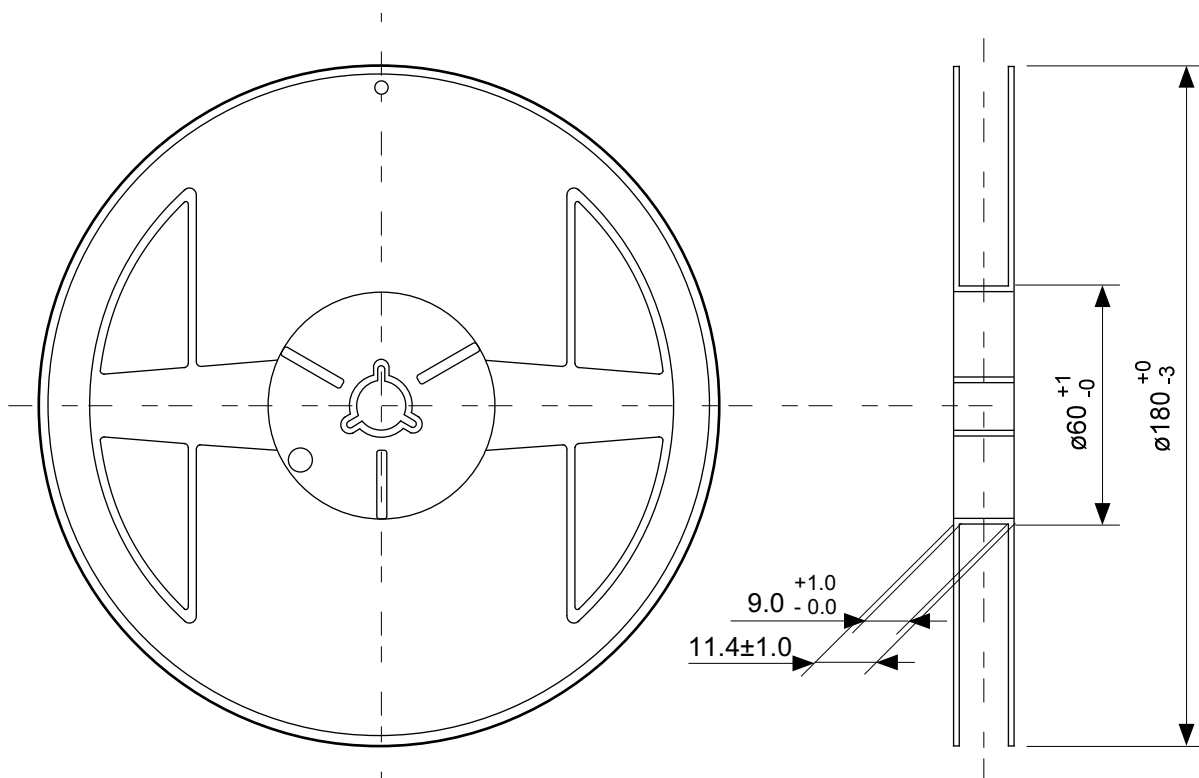


Feed direction

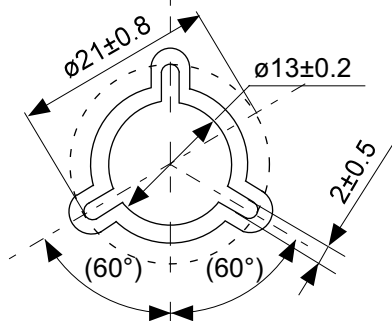
No. MP005-A-C-SD-2.1

|            |                       |
|------------|-----------------------|
| TITLE      | SOT235-A-Carrier Tape |
| No.        | MP005-A-C-SD-2.1      |
| ANGLE      |                       |
| UNIT       | mm                    |
| ABLIC Inc. |                       |



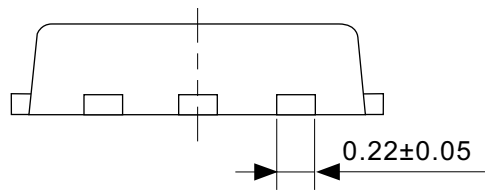
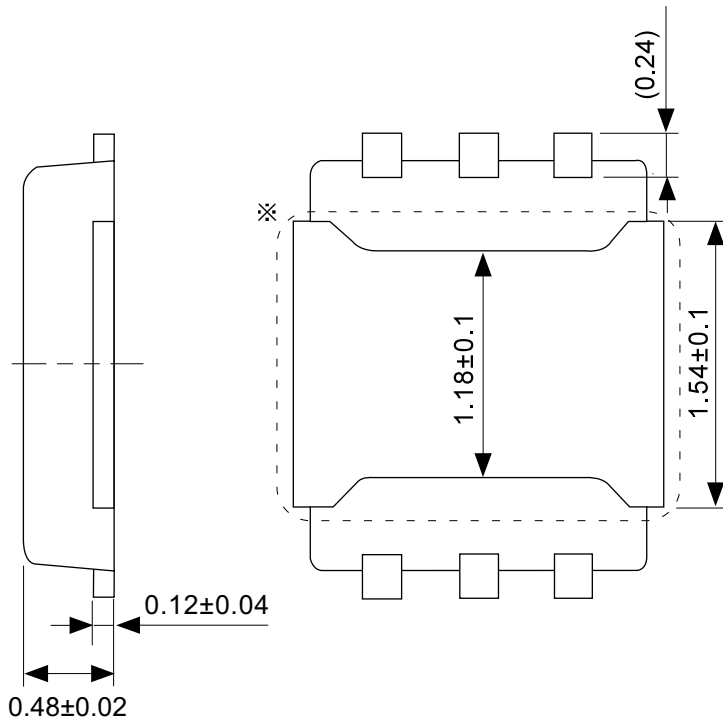
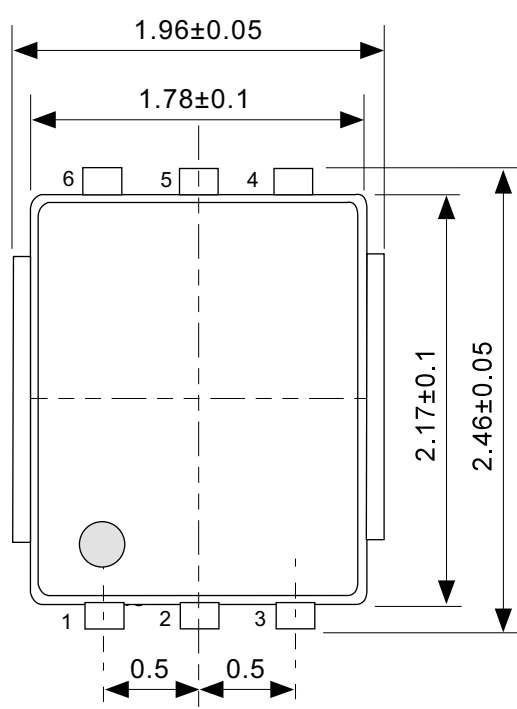


Enlarged drawing in the central part



No. MP005-A-R-SD-2.0

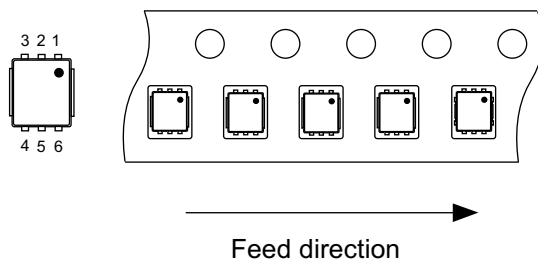
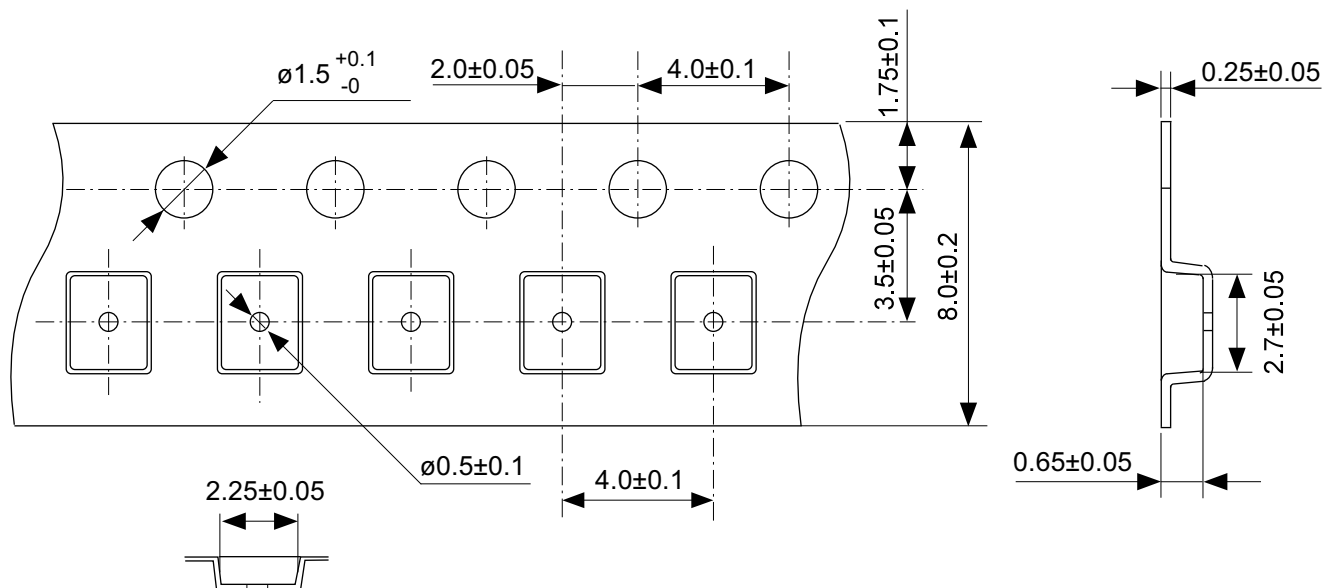
|            |                  |      |       |
|------------|------------------|------|-------|
| TITLE      | SOT235-A-Reel    |      |       |
| No.        | MP005-A-R-SD-2.0 |      |       |
| ANGLE      |                  | QTY. | 3,000 |
| UNIT       | mm               |      |       |
|            |                  |      |       |
| ABLIC Inc. |                  |      |       |



※ The heat sink of back side has different electric potential depending on the product.  
 Confirm specifications of each product.  
 Do not use it as the function of electrode.

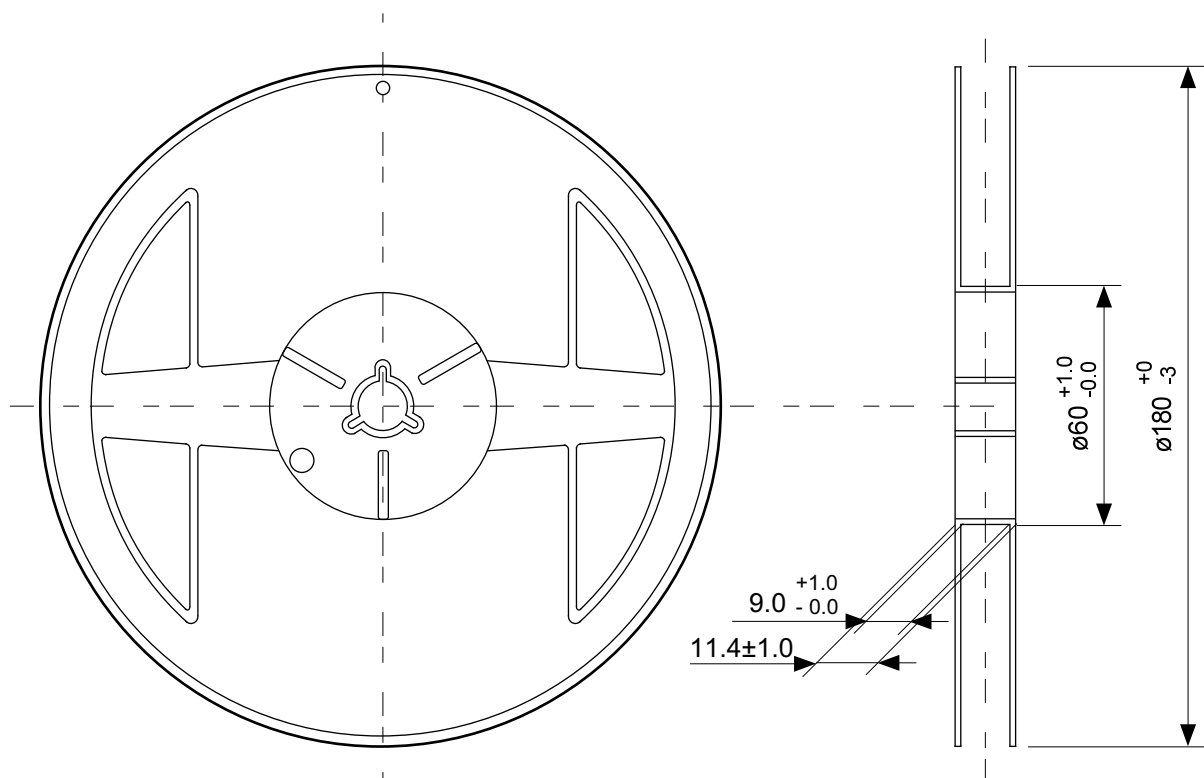
No. PJ006-B-P-SD-1.0

|            |                         |
|------------|-------------------------|
| TITLE      | HSNT-6-C-PKG Dimensions |
| No.        | PJ006-B-P-SD-1.0        |
| ANGLE      |                         |
| UNIT       | mm                      |
|            |                         |
| ABLIC Inc. |                         |

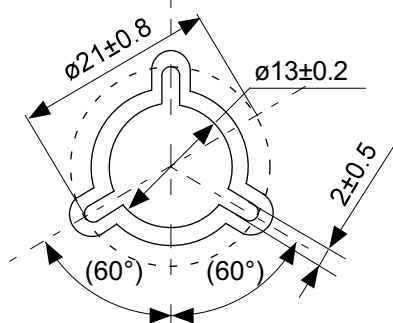


No. PJ006-B-C-SD-1.0

|            |                       |
|------------|-----------------------|
| TITLE      | HSNT-6-C-Carrier Tape |
| No.        | PJ006-B-C-SD-1.0      |
| ANGLE      |                       |
| UNIT       | mm                    |
|            |                       |
| ABLIC Inc. |                       |



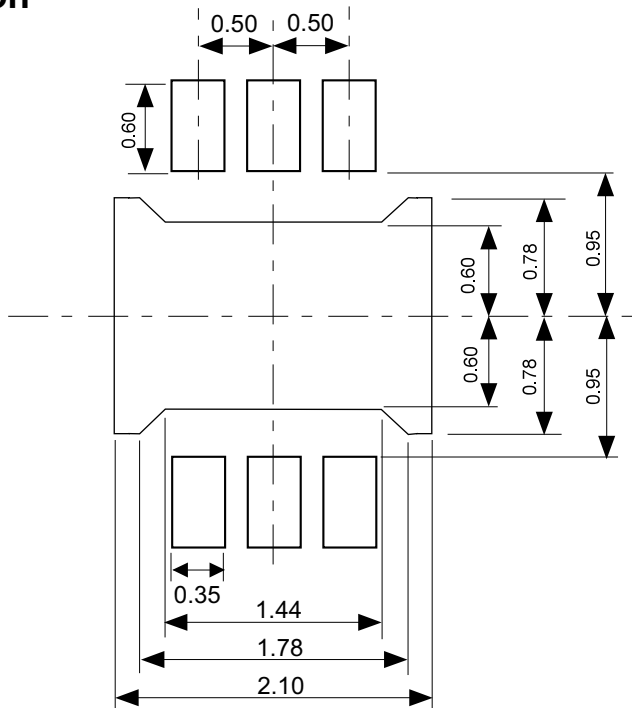
Enlarged drawing in the central part



No. PJ006-B-R-SD-1.0

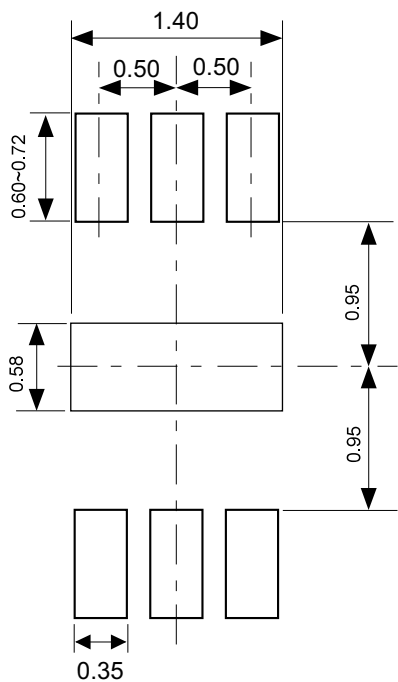
|            |                  |      |       |
|------------|------------------|------|-------|
| TITLE      | HSNT-6-C-Reel    |      |       |
| No.        | PJ006-B-R-SD-1.0 |      |       |
| ANGLE      |                  | QTY. | 5,000 |
| UNIT       | mm               |      |       |
|            |                  |      |       |
| ABLIC Inc. |                  |      |       |

Land Recommendation



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.  
注意 放熱性を確保する為に、PKGの裏面放熱板(ヒートシンク)を基板に半田付けする事を推奨いたします。

Stencil Opening



No. PJ006-B-LM-SD-1.0

Caution ① Mask aperture ratio of the lead mounting part is 100~120%.  
② Mask aperture ratio of the heat sink mounting part is 30%.  
③ Mask thickness: t0.12 mm  
④ Reflow atmosphere: Nitrogen atmosphere is recommended.  
(Oxygen concentration: 1000ppm or less)

注意 ①リード実装部のマスク開口率は100~120%です。  
②放熱板実装のマスク開口率は30%です。  
③マスク厚み：t0.12 mm  
④リフロー雰囲気・窒素雰囲気(酸素濃度1000ppm以下)推奨

|            |                                    |
|------------|------------------------------------|
| TITLE      | HSNT-6-C<br>-Land &Stencil Opening |
| No.        | PJ006-B-LM-SD-1.0                  |
| ANGLE      |                                    |
| UNIT       | mm                                 |
|            |                                    |
| ABLIC Inc. |                                    |

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2.4-2019.07

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